

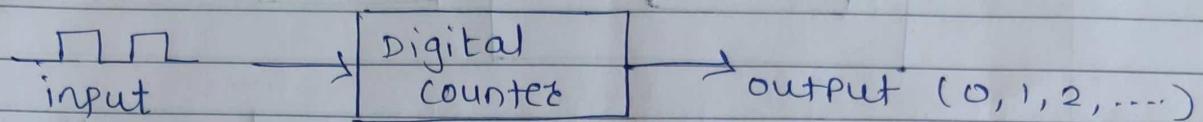
## Unit - III

### Sequential Logic Design

#### \* Counters

##### \* Counters -

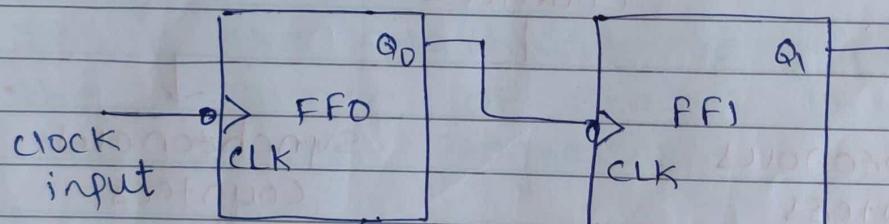
A counter is a register capable of counting the number of clock pulses arriving at its clock input.



##### \* Types of counters:-

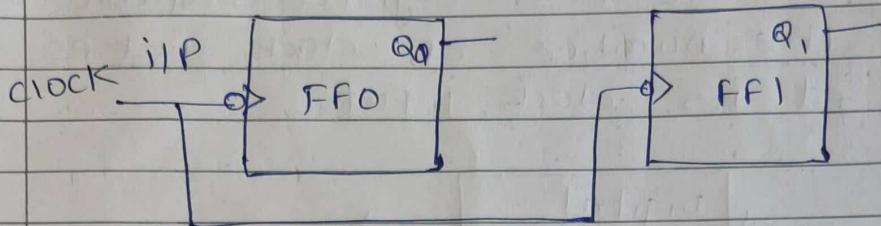
- 1) Asynchronous counter
- 2) Synchronous counter

##### ① Asynchronous counter:-



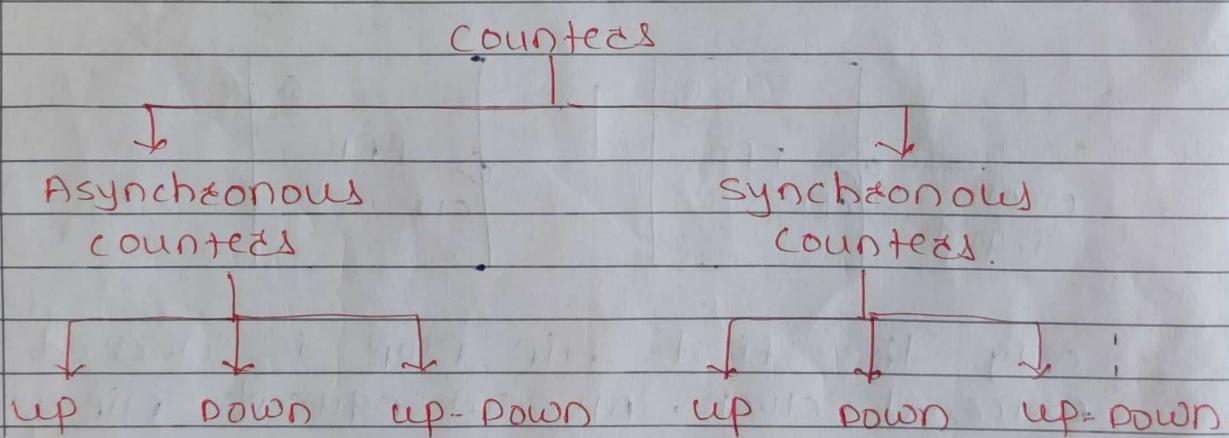
- only the first flip flop is clocked by an external clock. All subsequent flip flops are clocked by the output of the preceding flip flop.
- It is also called as ripple counters. because of the way the clock pulse ripples it way through the flip flops.
- In asynchronous counter all FFs are used in toggle mode.

2) Synchae nous counted:-



- All flip flops are clocked simultaneously by an external clock.
  - Faster than asynchronous counter because of the simultaneous clocking.

## classification of counters.



① up counted

Binary Counter									
Initial	000	001	010	011	100	101	110	111	000
Binary O/P	000	001	010	011	100	101	110	111	000
Decimal	0 →	1 →	2 →	3 →	4 →	5 →	6 →	7 →	0 →

### (2) Down counted

initial										
Binary	111	110	101	100	001	010	001	000	111	110
DIP										
Decimal	7	6	5	4	3	2	1	0	7	6

### (3) Up-down counted:-

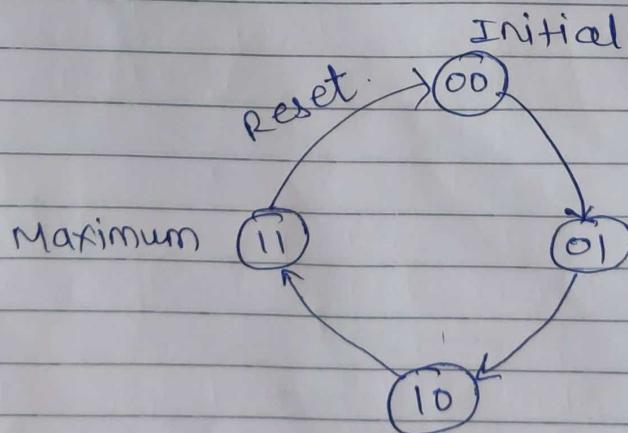
- One value of control unit I/P, the counter behave like up counter, & for the other value behave like down counter.

### \* State diagram:-

- It is the graphical representation of the sequence of states through which the counter progresses.

For 2 bit up counter the O/P sequence is

00 - 01 - 10 - 11 - 00



## \* Modulus of the counter (MOD-N counter)

- Modulus (MOD) of a counter represents the number of states through which the counter progresses during its operation.

It is denoted by N.

- MOD-N counter means the counter progresses through N states.
- MOD-4 counter means will have 4 states.  
6 counter means will have 6 states.

$$\text{MOD Number} = 2^N$$

counter TYPES	Modulus.
2-bit up   down	MOD-4
3-bit up   down	MOD-8
4-bit up   down	MOD-16

## Asynchronous UP counter

\* 2-bit Asynchronous up counter  
(MOD-4 up counter)

$$\rightarrow \text{NO. OF FLIP FLOPS} = 2$$

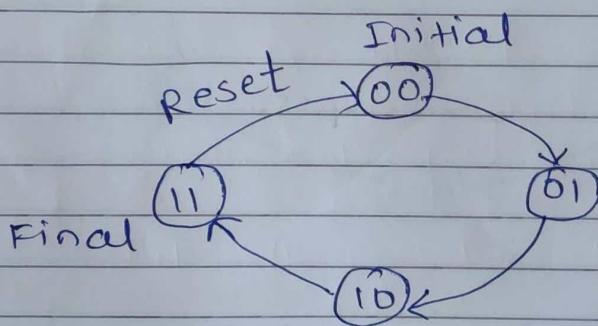
$$\text{NO. OF states} = 2^2 = 4 \quad (2^n)$$

$$\text{Maximum count} = 2^n - 1 = 2^2 - 1 = 3$$

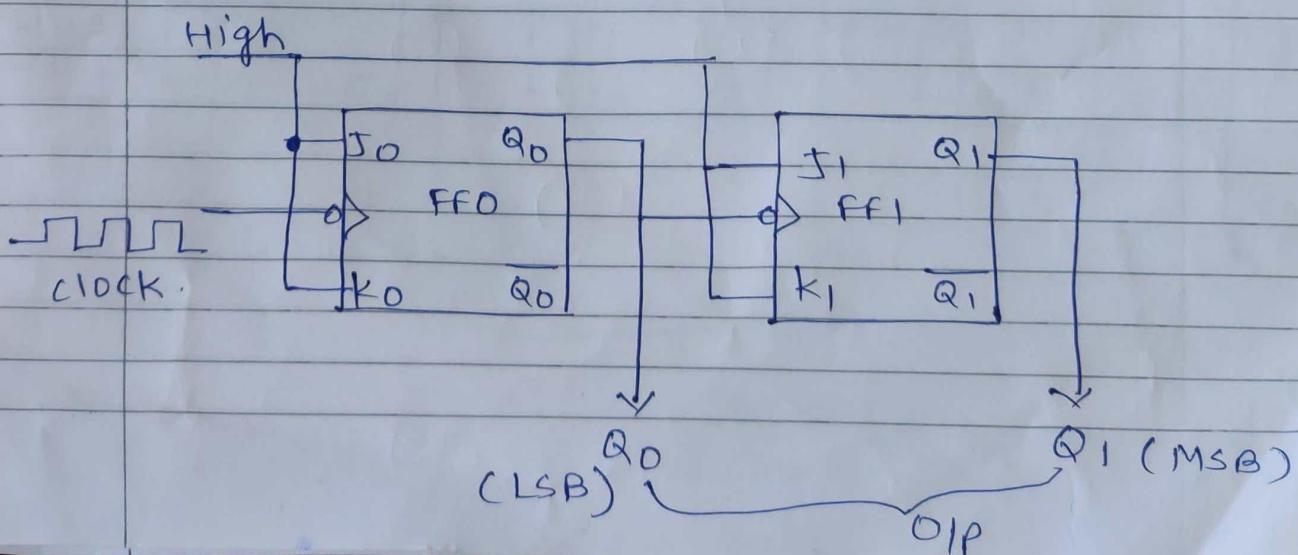
- so, the count will go from 0 to 3  
In binary form the sequence is  
00, 01, 10, 11

Step 1 → state diagram

Initially the count is 00, then 01, 10 & 11 & then 00 (Reset)



Step 2 → circuit diagram.



### Step 3:- Timing diagram:-

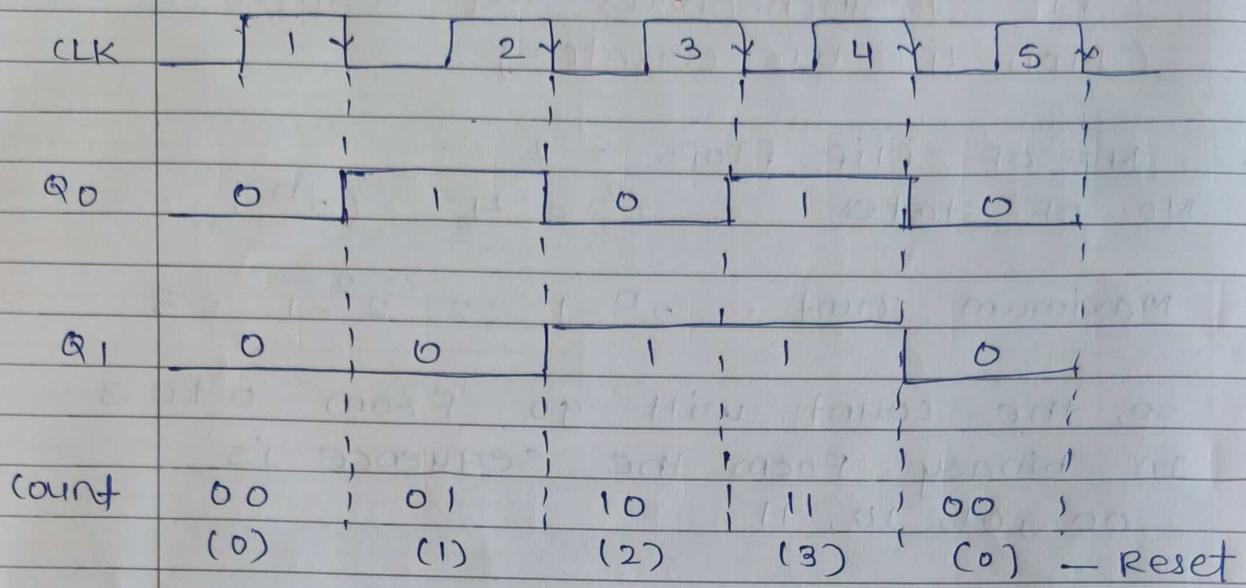


Fig: Timing diagram of a 2-bit asynchronous counter.

\* 3-bit Asynchronous up counter (MOD-8)

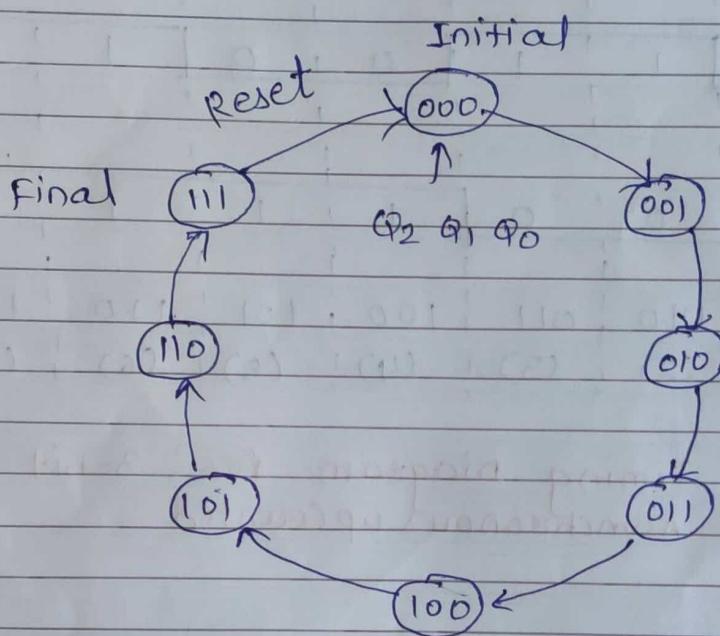
$$\rightarrow \text{No. of states} = 2^n = 2^3 = 8$$

NO. OF FLIP FLOPS = 3

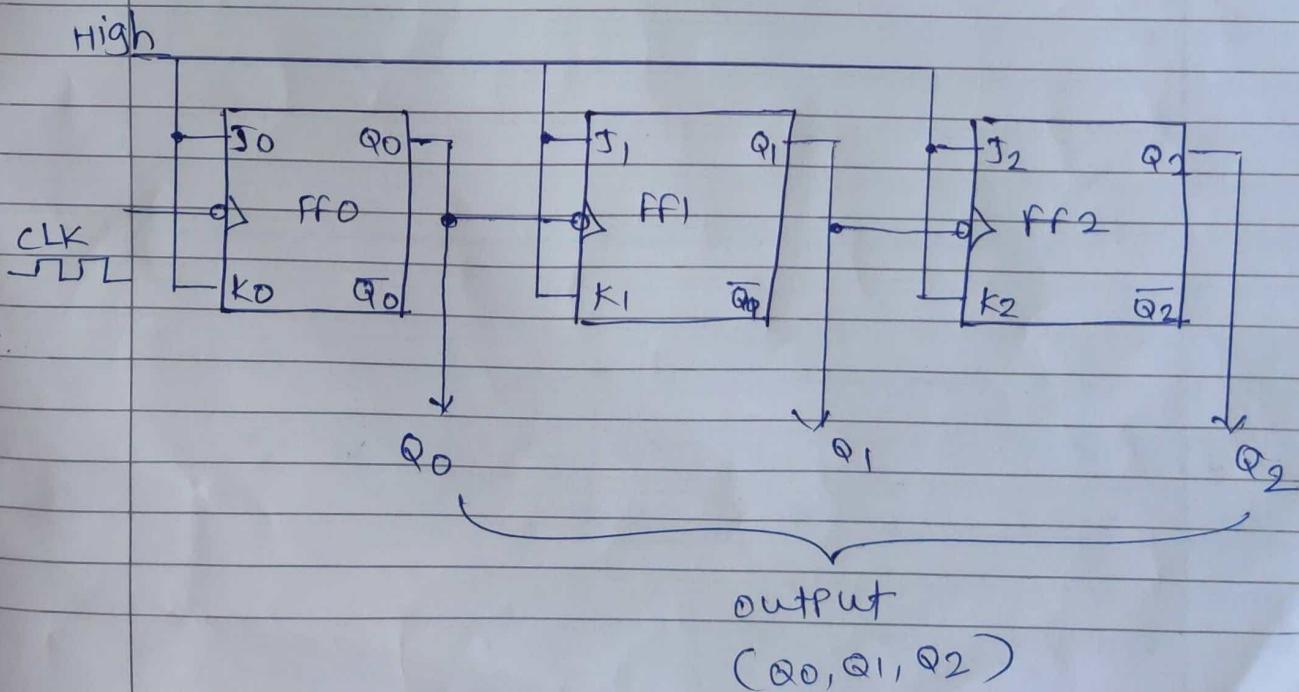
$$\text{Maximum count} = 2^n - 1 = 8 - 1 = 7$$

sequence    000, 001, 010, 011, 100, 101, 110, 111, 000

## \* state Diagram :



## \* Circuit Diagram:



## \* Timing Diagram

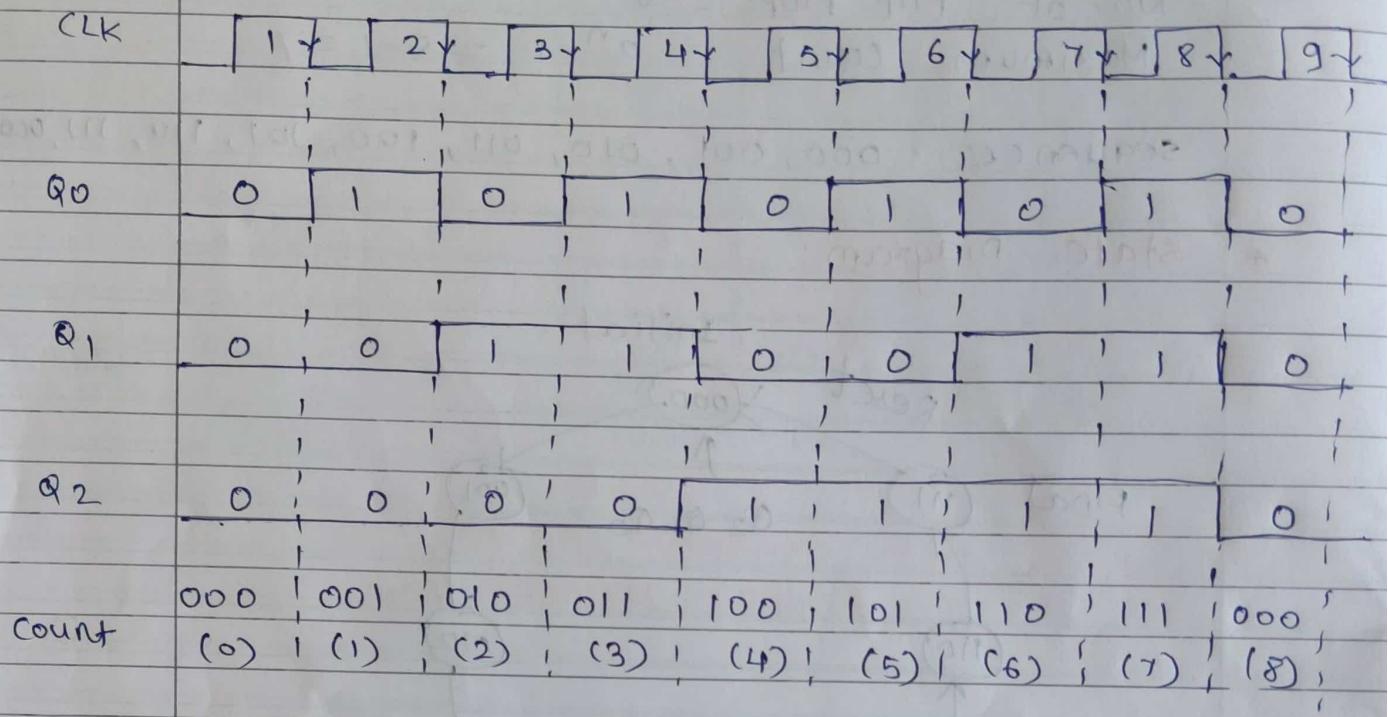


Fig: Timing Diagram for 3-bit Asynchronous up counter

Q. 4-bit Asynchronous up counter  
(Practice)

## Asynchronous DOWN counter.

\* 3-bit Asynchronous Down counter.

- Down counter will count the clock pulses from maximum value to zero.

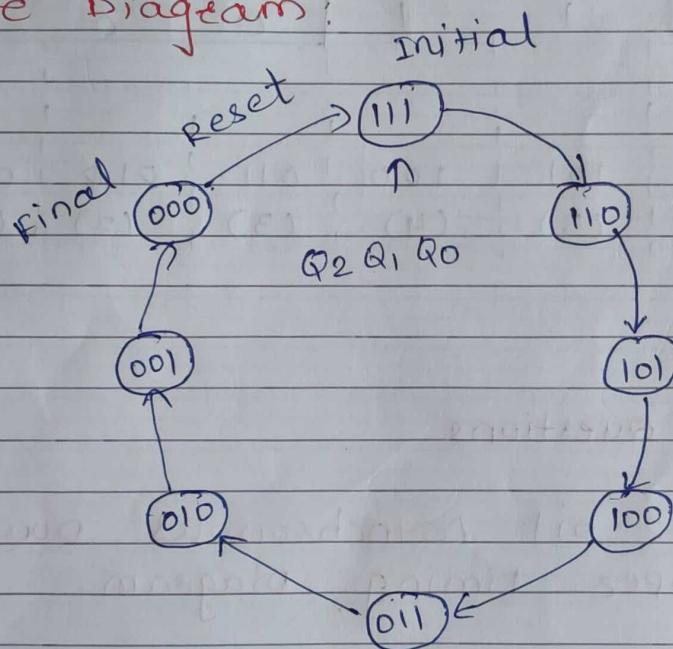
$$\text{No. of states} = 2^n = 2^3 = 8$$

$$\text{No. of flip flops} = 3$$

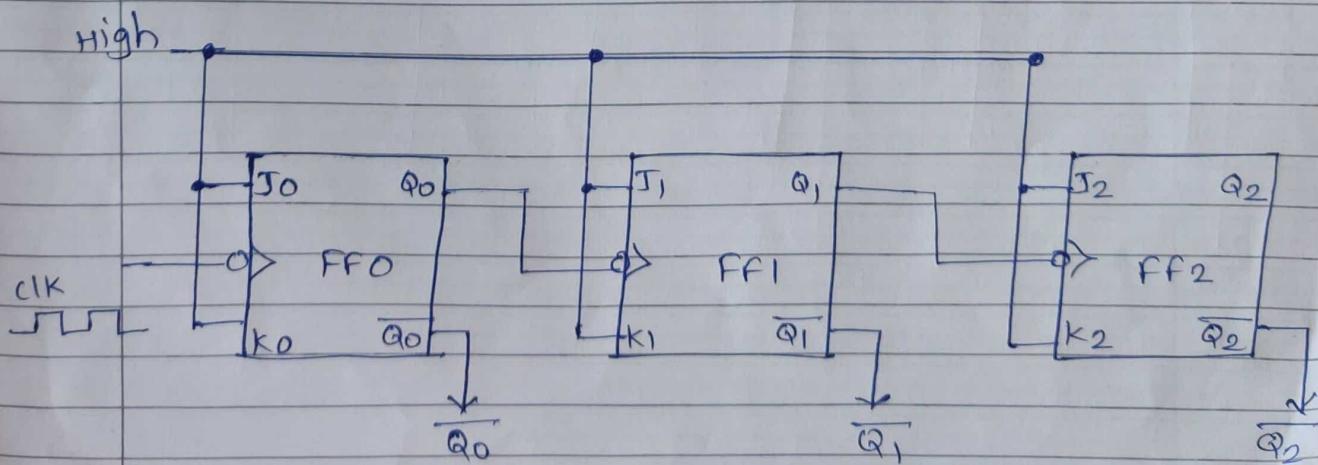
$$\text{Maximum count} = 2^n - 1 = 8 - 1 = 7$$

Counting sequence 111, 110, 101, 100, 011, 010, 001, 000

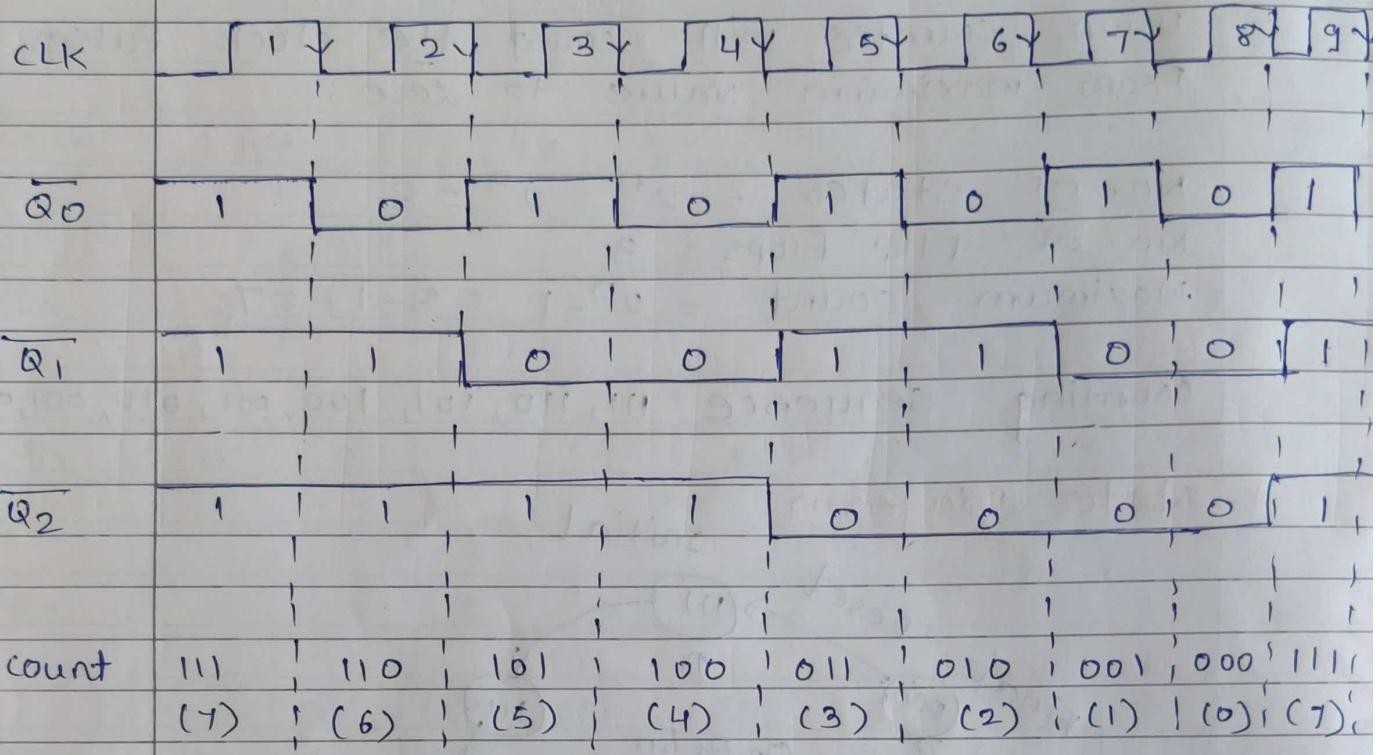
\* State Diagram:



\* Circuit Diagram:



\* Timing diagram :-



\* Practice Questions

- ① Explain 2-bit Asynchronous Down counter with Proper Timing diagram.
- ② Explain 4-bit Asynchronous Down counter with Proper timing diagram.

## Asynchronous UP | DOWN counter. (Bidirectional counter)

- In Asynchronous UP | DOWN counter, Control input is necessary to control the operation as up or down counter.
- In the UP | DOWN counter
  - We are using negative edge triggered FFs
  - External clock is applied only to the first FF.
  - The QP of the first FF is used as a clock to the next FF.
- In the UP | DOWN counter we use a control input ( $M$ ) which decides whether  $Q$  or  $\bar{Q}$  is to be connected to the clock of the next FF.
  - For one value of the control ( $M$ ),  $Q$  is connected and for other value  $\bar{Q}$  is connected.

For UP counter -  $Q$  is connected to CLK of next FF.

For DOWN counter -  $\bar{Q}$  is connected to CLK of next FF.

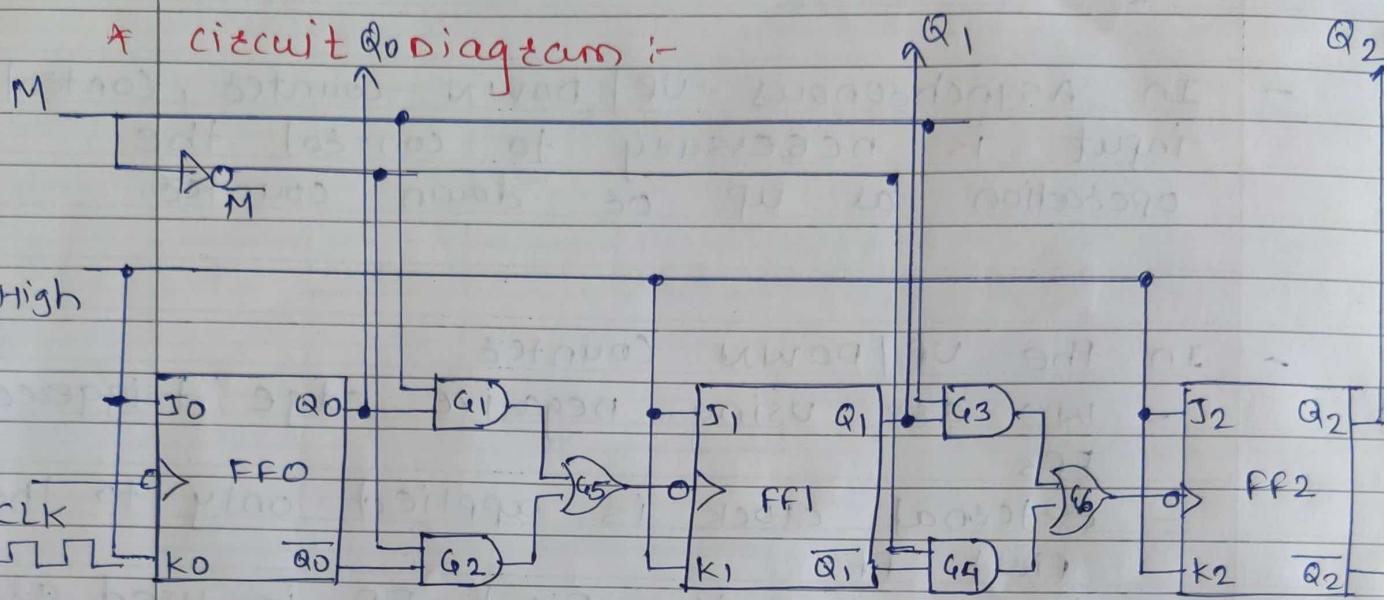


Fig: 3 bit up/down Asynchronous counter Using JK FF.

# Unit - III

## sequential logic design.

\* Synchronous counters.

① 2-Bit synchronous up counter. [MOD-4]

→ For 2 bit counter

$$\text{No. of states} = 2^n = 2^2 = 4$$

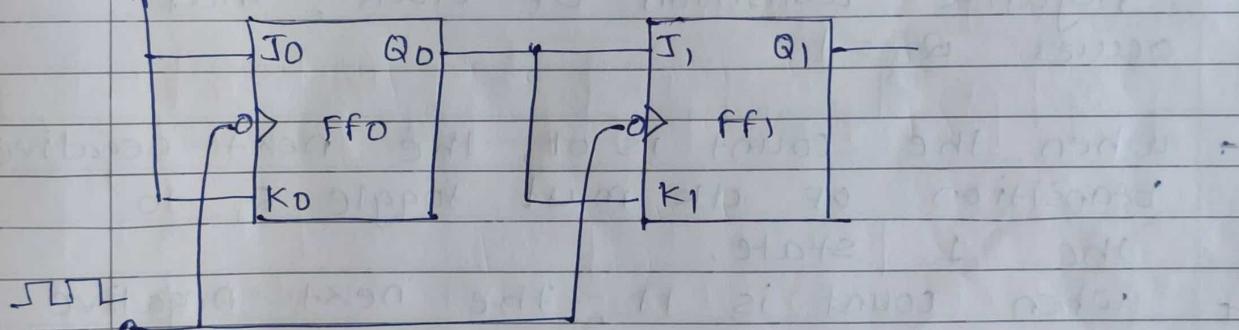
$$\text{No. of FF} = 2$$

① circuit diagram.

Logic diagram of 2 bit synchronous counter

Using JK flip flop.

High



$$\text{output} = Q_1 \ Q_0$$

fig: 2 bit synchronous up counter

count	sequence		count
CLK	Q <sub>1</sub>	Q <sub>0</sub>	
0	0	0	0
1	0	1	1
2	1	0	2
3	1	1	3

## ② Circuit operation:-

$$Q_1 Q_0 = 00 \text{ (Initially)}$$

case 1 ( 1<sup>st</sup> negative clock edge )

Q<sub>0</sub> bits are toggling at each negative transition of the clock.

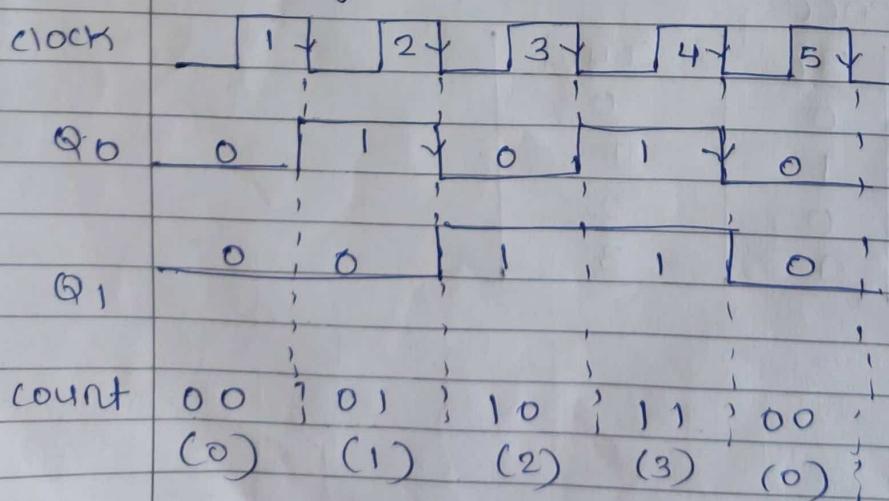
so, Q<sub>0</sub> will change from 0 to 1

case 2

FF1 must change states on each negative transition of clock, that occurs  $Q_0 = 1$

- when the count is 01, the next negative transition of clk must toggle Q<sub>1</sub> to the 1 state,
- when count is 11, the next negative transition of clk must toggle Q<sub>1</sub> to the 0.

## ③ Timing diagram.



\* 3-bit synchronous binary up counter.

Q. Design 3-bit synchronous up counter using JK flip flop.

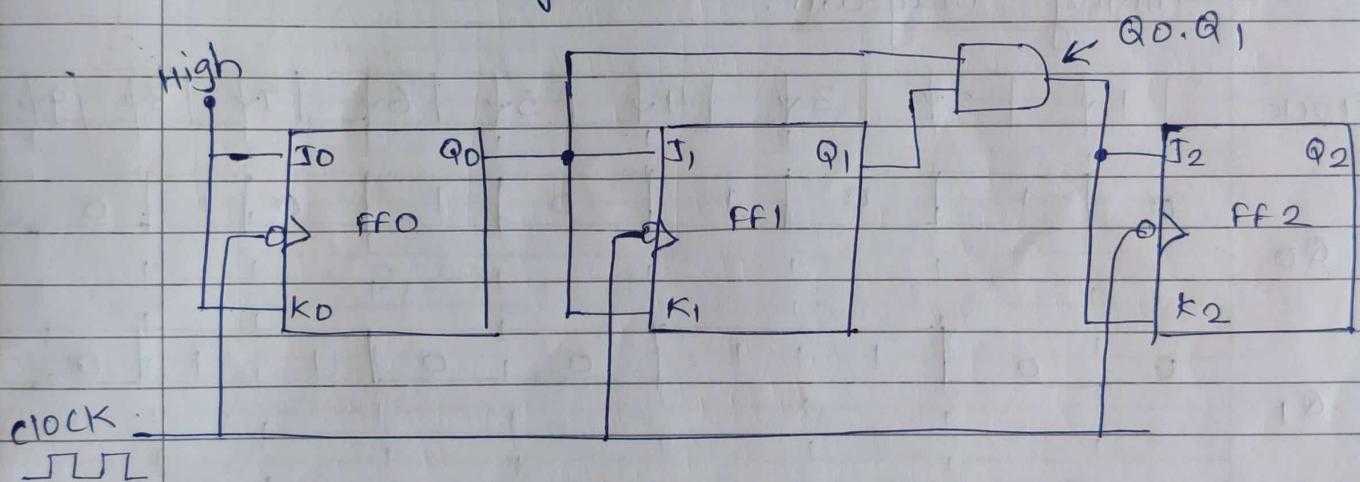
→ For 3 bit counter.

$$\text{No. of states} = 2^n = 2^3 = 8$$

$$\text{No. of FFs} = 3$$

Counting sequence in 3 bit up-counter is  
0, 1, 2, 3, 4, 5, 6, 7, 0, ...

① Circuit diagram



$$\text{outputs} = Q_2, Q_1, Q_0$$

Counting sequence

CLK	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	count
0	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7

\* Operations

Initially all FF's are in their reset state

$$Q_2 \ Q_1 \ Q_0 = 0 \ 0 \ 0$$

$$1^{\text{st}} \text{ clock} = Q_2 \ Q_1 \ Q_0 = 001$$

$$2^{\text{nd}} \text{ clock} = Q_2 \ Q_1 \ Q_0 = 010$$

$$3^{\text{rd}} \text{ clock} = Q_2 \ Q_1 \ Q_0 = 011$$

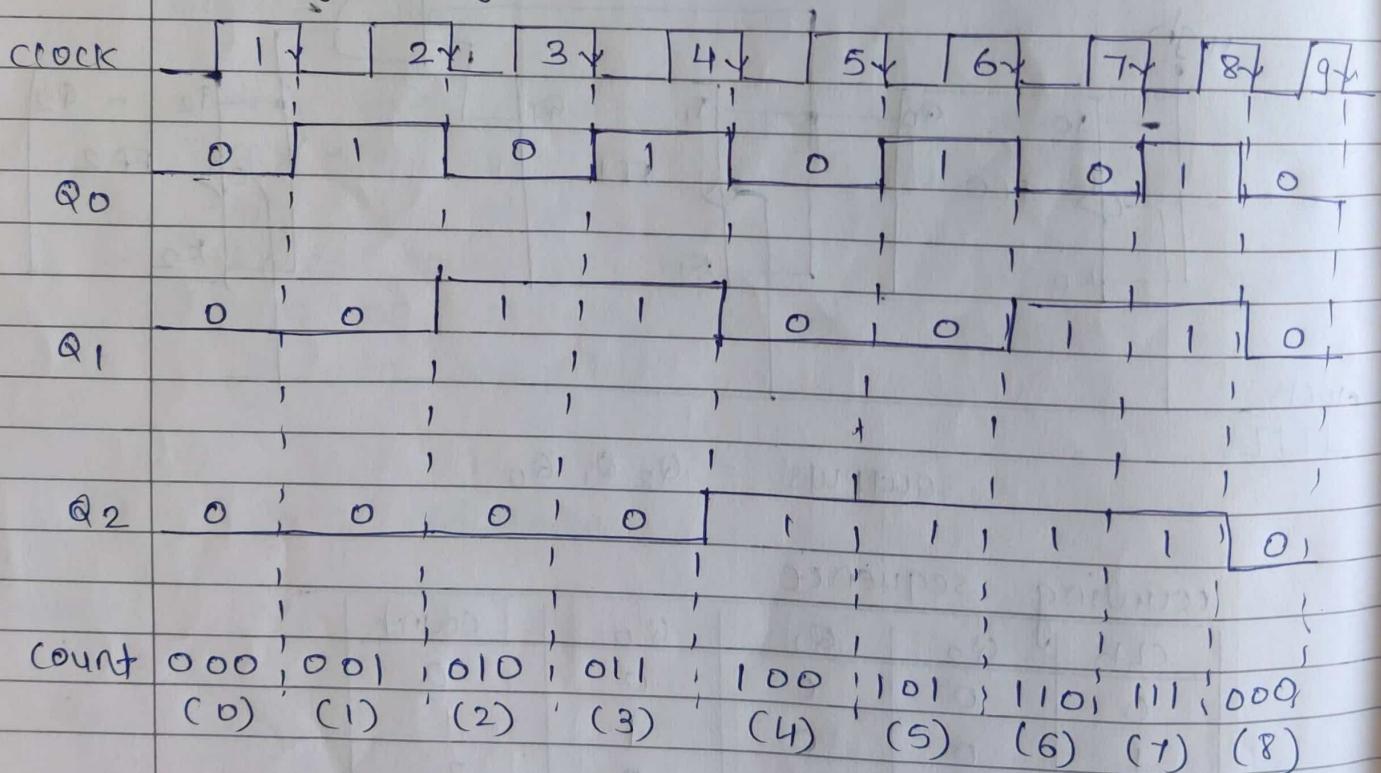
$$4^{\text{th}} \text{ clock} = Q_2 \ Q_1 \ Q_0 = 100$$

$$5^{\text{th}} \text{ } \rightarrow \text{---} = Q_2 \ Q_1 \ Q_0 = 101$$

$$6^{\text{th}} \text{ } \rightarrow \text{---} = Q_2 \ Q_1 \ Q_0 = 110$$

$$7^{\text{th}} \text{ } \rightarrow \text{---} = Q_2 \ Q_1 \ Q_0 = 111$$

\* Timing Diagram



\* 4-BIT (MOD-16) synchronous up counter

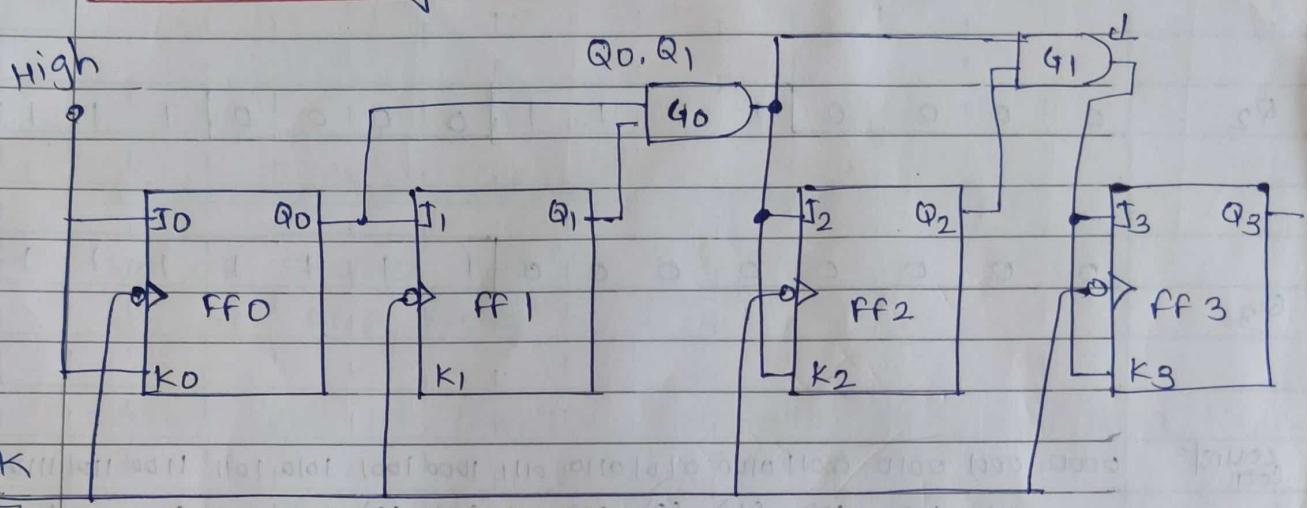
→ NO. OF states = 16

NO. OF FF's = 4

Counting sequence 0, 1, 2, 3, 4, 5, ... 14, 15, 0

① Circuit diagram:

$Q_0, Q_1, Q_2$



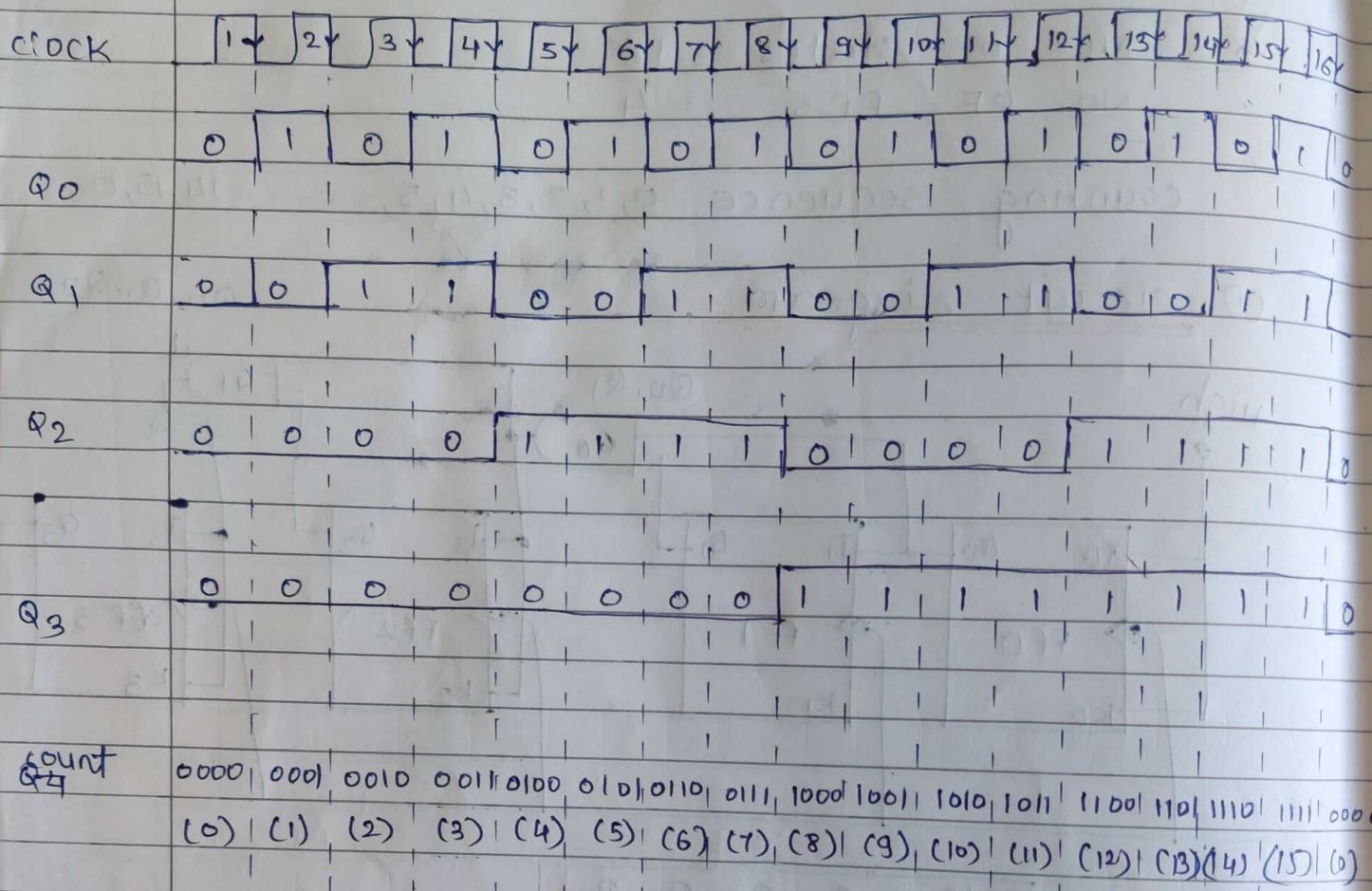
CLOCK

$$O/P = Q_3 \ Q_2 \ Q_1 \ Q_0$$

\* Counting sequence:

CLK	$Q_3$	$Q_2$	$Q_1$	$Q_0$	Count
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
10	1	0	1	0	10
11	1	0	1	1	11
12	1	1	0	0	12
13	1	1	0	1	13
14	1	1	1	0	14
15	1	1	1	1	15

## Timing Diagram



## \* Synchronous Down Counter

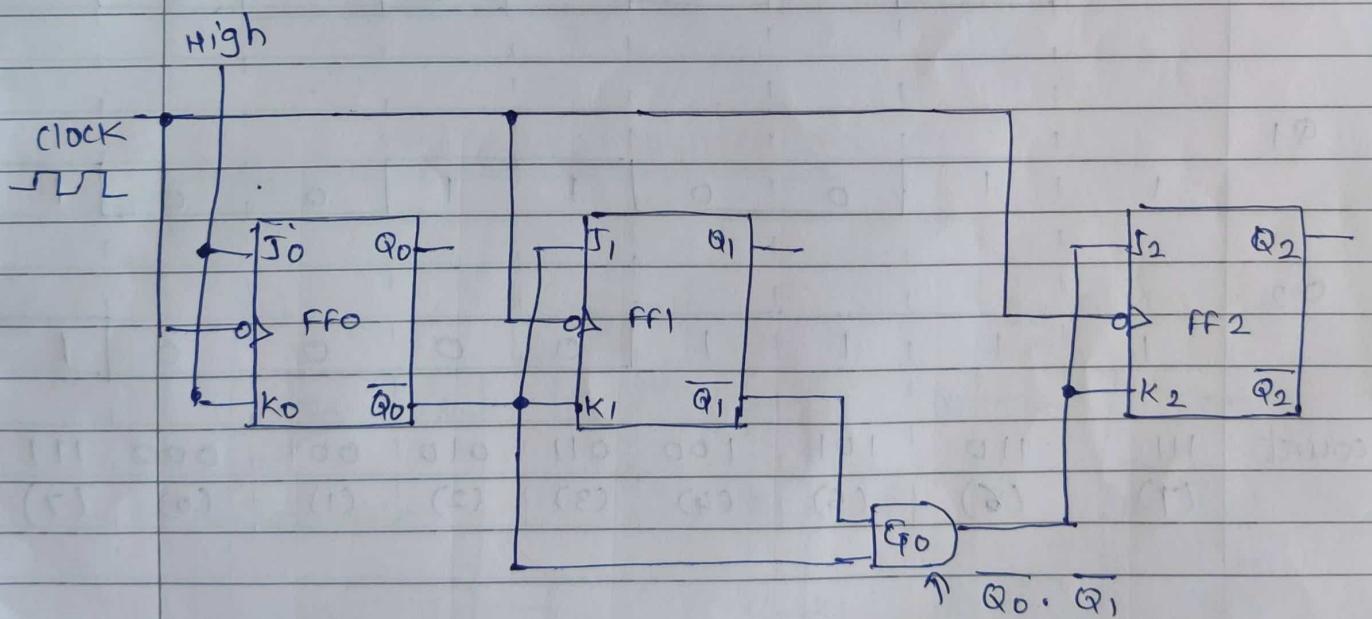
- As it is synchronous counter, same clock input is applied for all FF's
- In Down counter, the counter starts with all of its O/Ps HIGH & it's count down on the application of each clock pulse to zero, then the sequence repeat.

## \* 3-bit Synchronous Down Counter :-

$$\rightarrow \text{No. of states} - 2^n = 2^3 = 8 \\ \text{No. of flip flops} = 3$$

sequence 111, 110, 101, 100, 011, 010, 001, 000, 111, ...

## \* Circuit diagram:

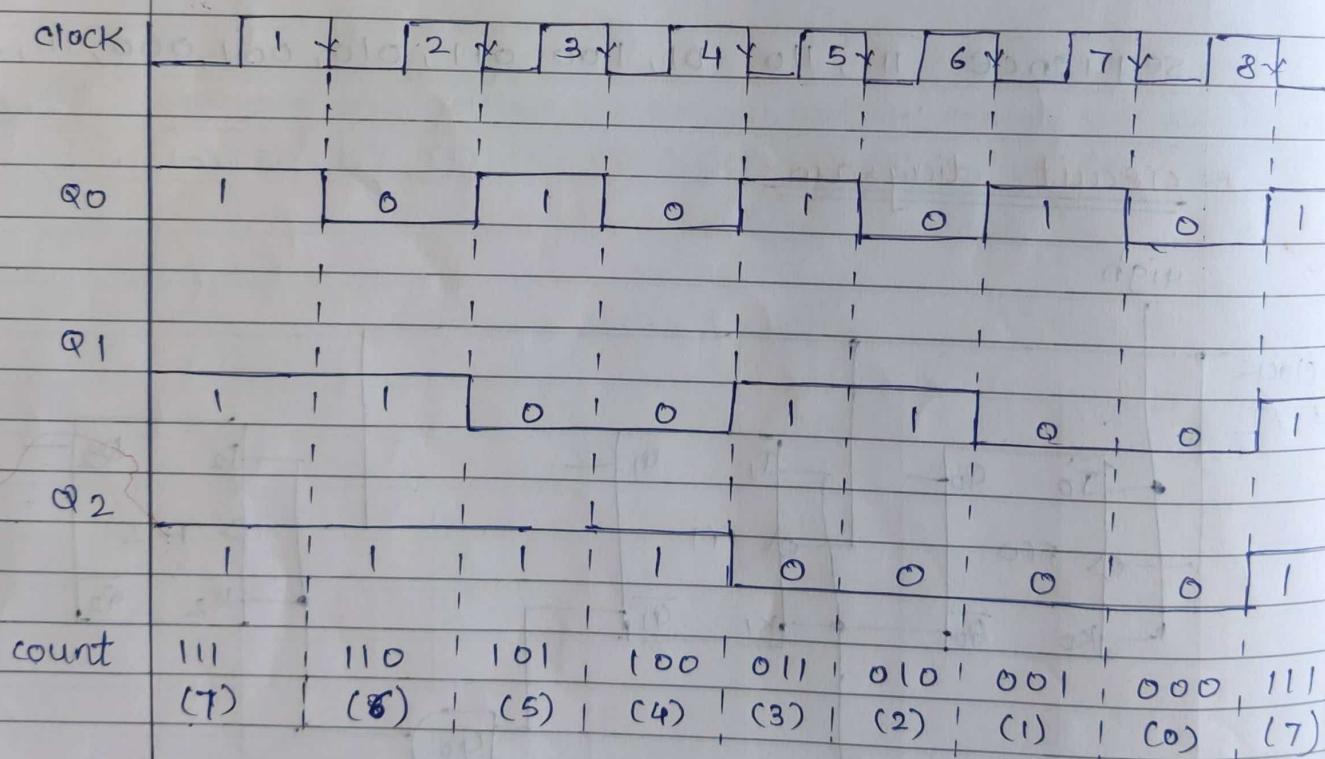


$$\text{output} = \overline{Q_0} \cdot \overline{Q_1} \cdot Q_2 + Q_1 \cdot Q_0$$

\* Counting Sequence :-

CLK	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	Count
0	1	1	1	7
1	1	1	0	6
2	1	0	1	5
3	1	0	0	4
4	0	1	1	3
5	0	1	0	2
6	0	0	1	1
7	0	0	0	0

\* Timing Diagram :-



Q. 4 bit synchronous down counted  
2 bit synchronous down counted.

## \* Synchronous UP | DOWN counter

### \* Synchronous UP | DOWN counter

- This counter performs both UP counting & Down counting using only one counter.
- When  $M=1$  - the counter performs UP counting.
- When  $M=0$  - performs DOWN counting.
- For UP & DOWN counters we have used following input connections for 3-bit counter.

Inputs for UP & DOWN counter.

UP counter [M=1]	DOWN counter [M=0]
$J_0 = K_0 = 1$ (High)	$J_0 = K_0 = 1$ (High)
$J_1 = K_1 = Q_0$	$J_1 = K_1 = \bar{Q}_0$
$J_2 = K_2 = Q_0 \cdot Q_1$	$J_2 = K_2 = \bar{Q}_0 \cdot \bar{Q}_1$

Q. 3-Bit UP | DOWN counter :-

control (M)

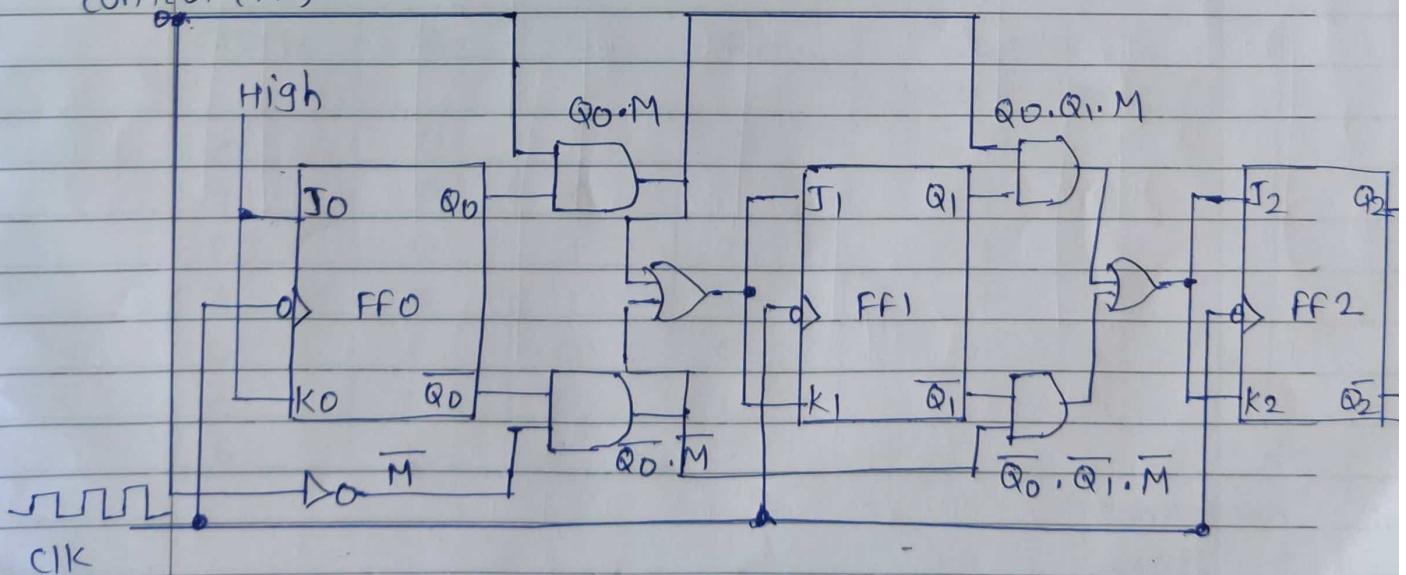


fig: circuit diagram.

(3 bit UP | DOWN counter)

Q. Design a MOD-6 asynchronous counter using JK flip flop.

→ Find the number of flip flops.

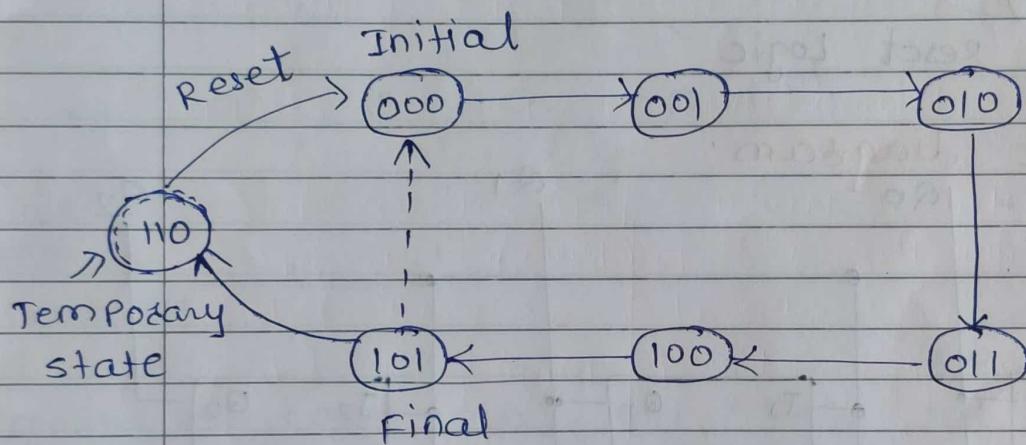
$$N=6$$

FF NO. OF STATES are 6

000, 001, 010, 011, 100, 101

$$\text{NO. OF FF's} = 3$$

\* State Diagram for MOD-6 counter.



\* Truth Table for mod-6

CLOCK	$Q_2$	$Q_1$	$Q_0$	Output Reset Logic (Y)
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	0

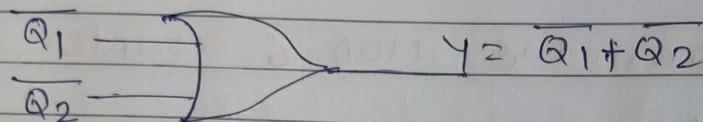
Temporary  
state  
(LOW)

\* K-map

		Q <sub>1</sub> Q <sub>0</sub>
		00 01 11 10
Q <sub>2</sub>		0 1
0	0	1 1
1	1	1 0

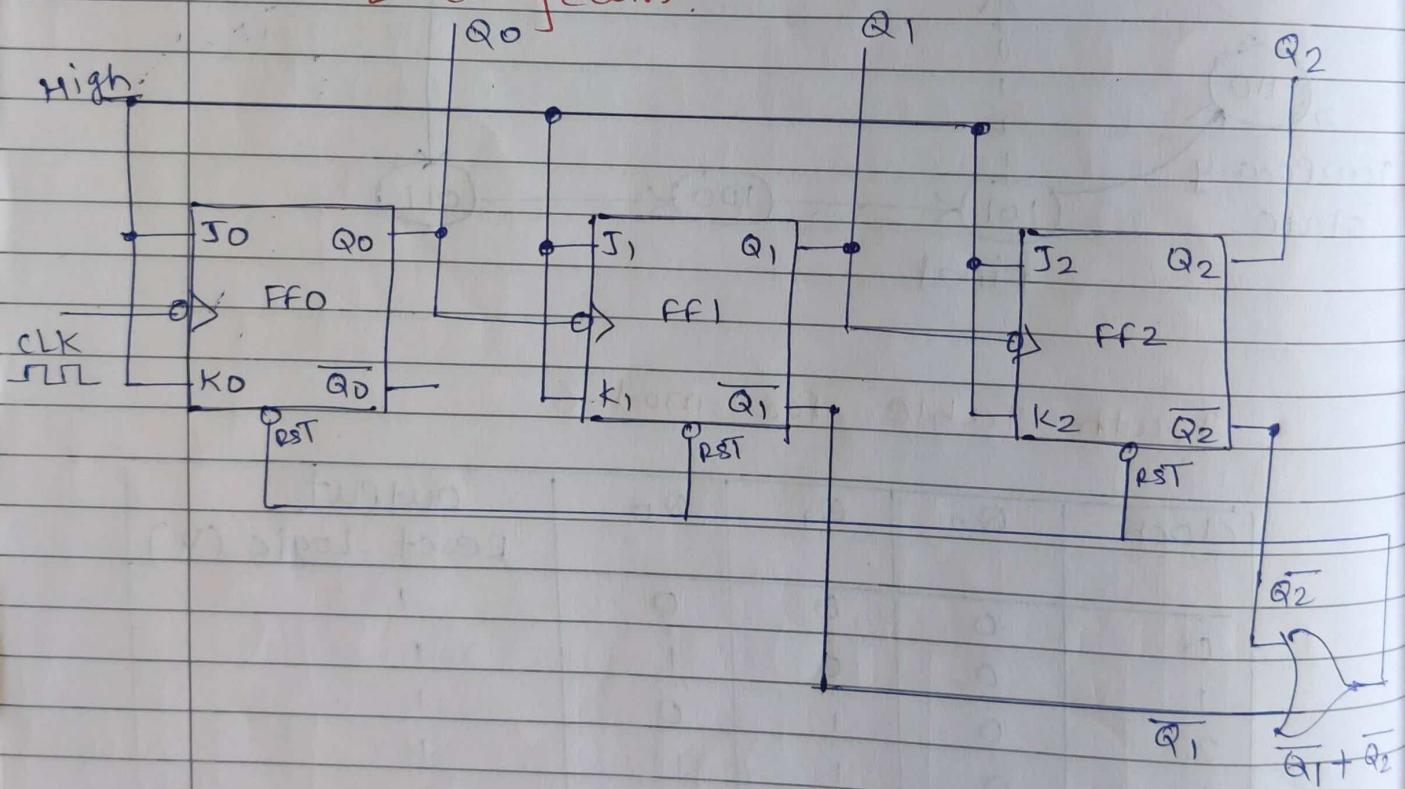
$\downarrow \bar{Q}_1$

$$Y = \bar{Q}_1 + \bar{Q}_2$$

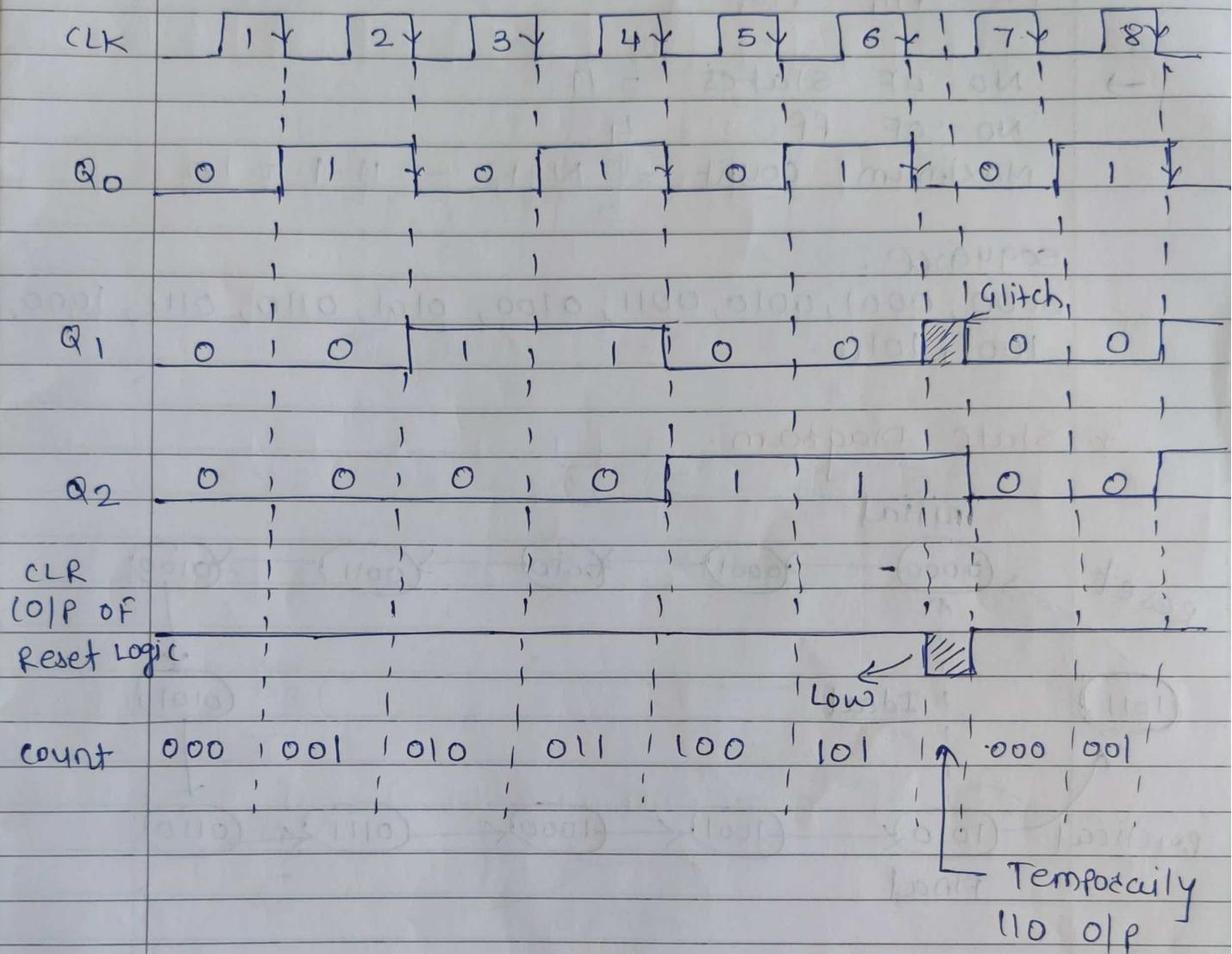


Reset Logic

\* circuit diagram:



## \* Timing Diagram :-



## A. Practice Question

Design a mod-6 asynchronous counter using T FF.  
(instead of JK FF's use T FF)

flip = asynchronous.

\* Design a mod 11 flip flop counter using JK flip flop

$$\rightarrow \text{NO. OF STATES} = 11$$

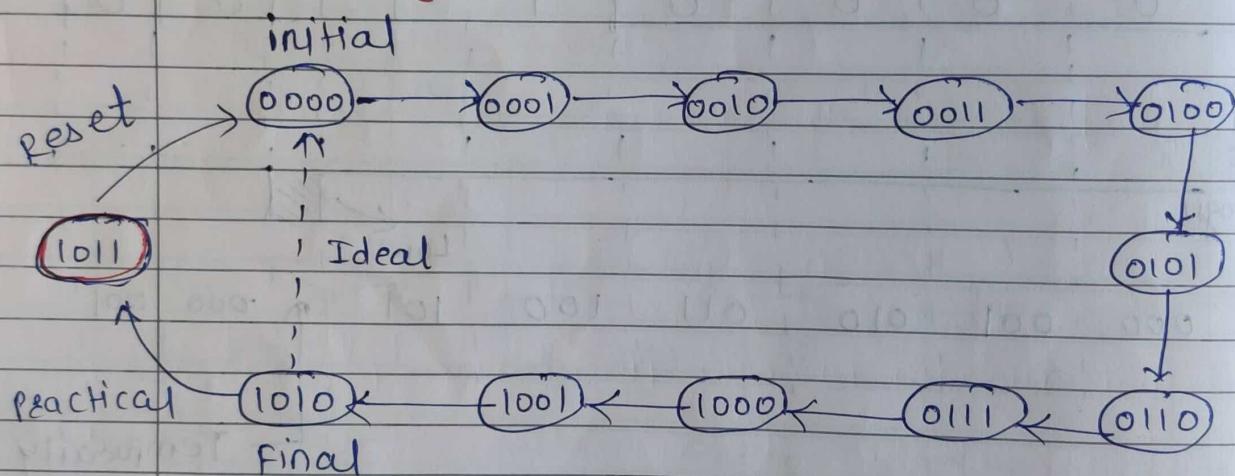
$$\text{NO. OF FF} = 4$$

$$\text{Maximum count} = N-1 = 11-1 = 10$$

sequence.

0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000  
1001, 1010.

\* State Diagram.



\* Truth Table

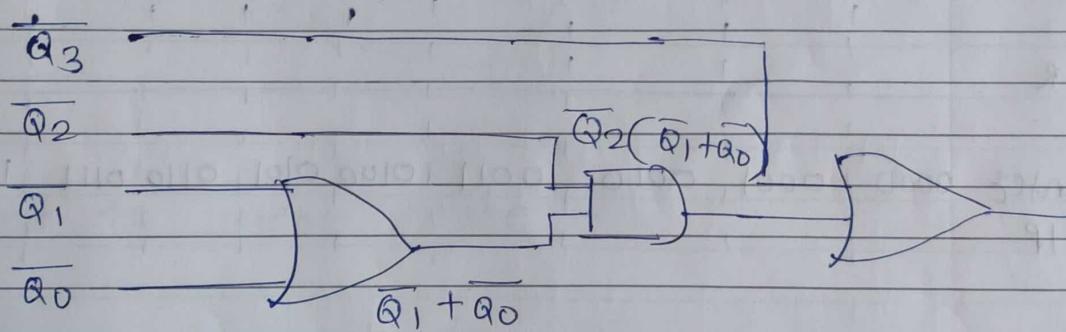
Clock	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	O/P	Reset Logic
0	0	0	0	0	0	1
1	0	0	0	1	1	1
2	0	0	1	0	1	1
3	0	0	1	1	1	1
4	0	1	0	0	1	1
5	0	1	0	1	1	1
6	0	1	1	0	1	1
7	0	1	1	1	1	1
8	1	0	0	0	0	1
9	1	0	0	1	1	1
10	1	0	1	0	1	1
11	1	0	1	1	0	1

\* K-map :

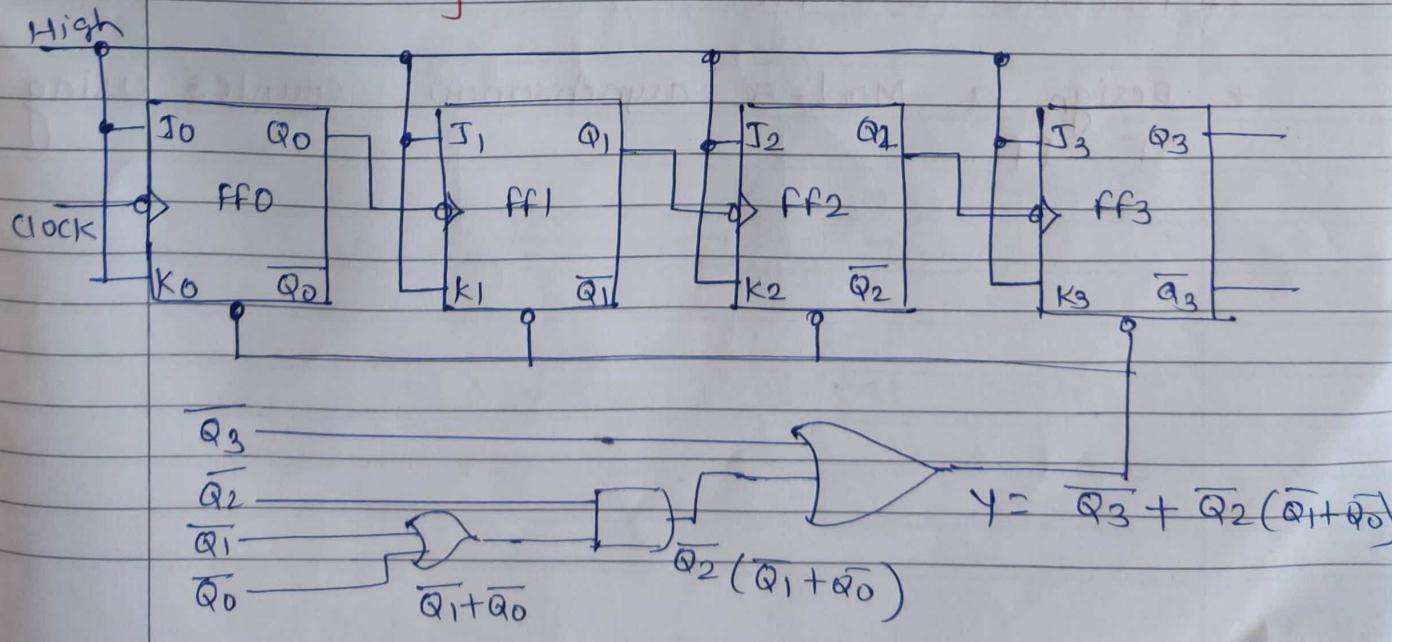
$\bar{Q}_3 \bar{Q}_2$	$\bar{Q}_1 \bar{Q}_0$				
00	00	01	11	10	
01	11	1	1	1	
11	0	0	0	0	
10	1	1	0	1	
					$\bar{Q}_3$
					$\bar{Q}_2 \bar{Q}_0$
		$\bar{Q}_2$	$\bar{Q}_1$		

$$Y = \bar{Q}_3 + \bar{Q}_2 \cdot \bar{Q}_1 + \bar{Q}_2 \cdot \bar{Q}_0$$

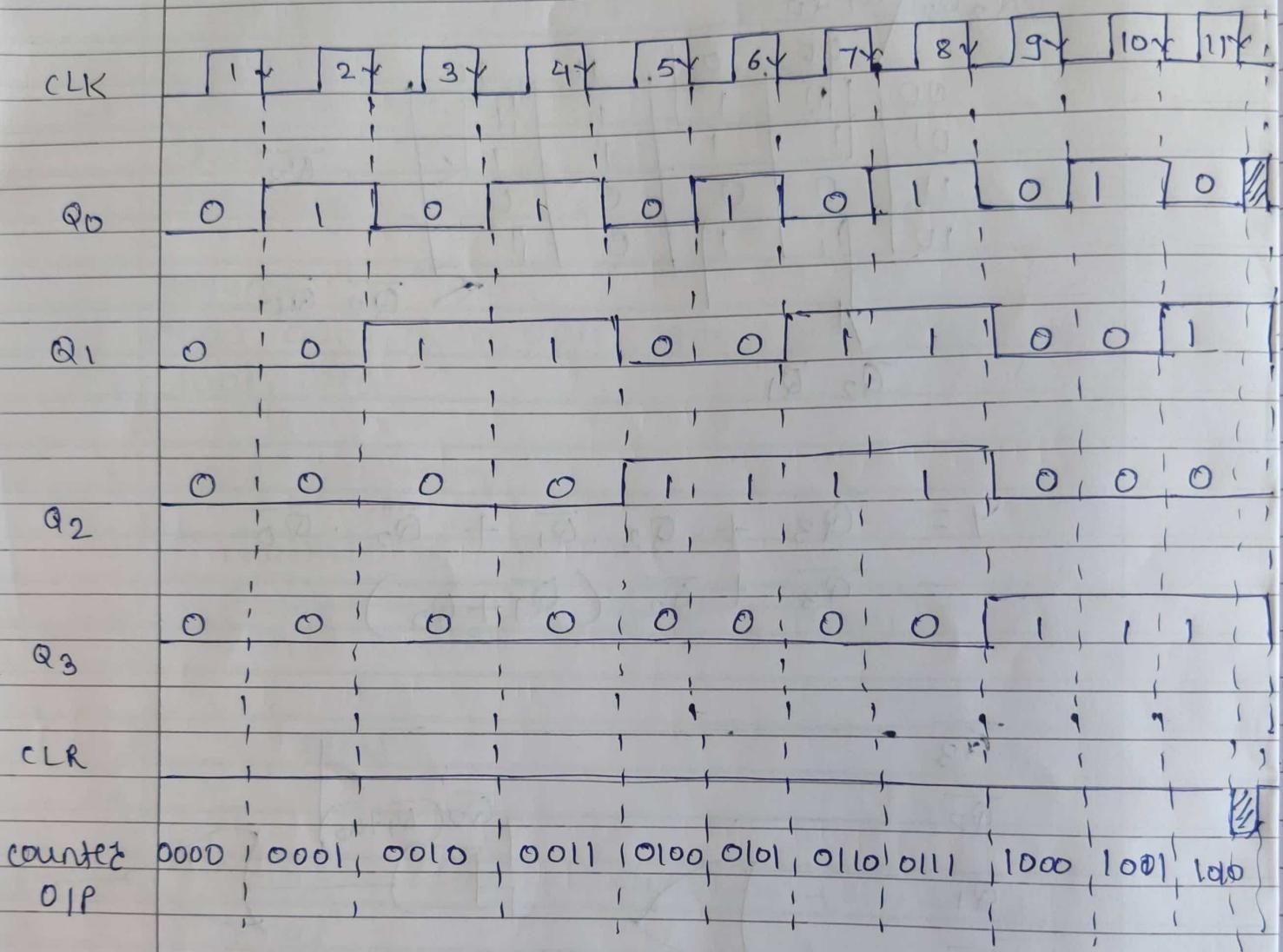
$$= \bar{Q}_3 + \bar{Q}_2 (\bar{Q}_1 + \bar{Q}_0)$$



\* Circuit diagram :



\* Timing Diagram:



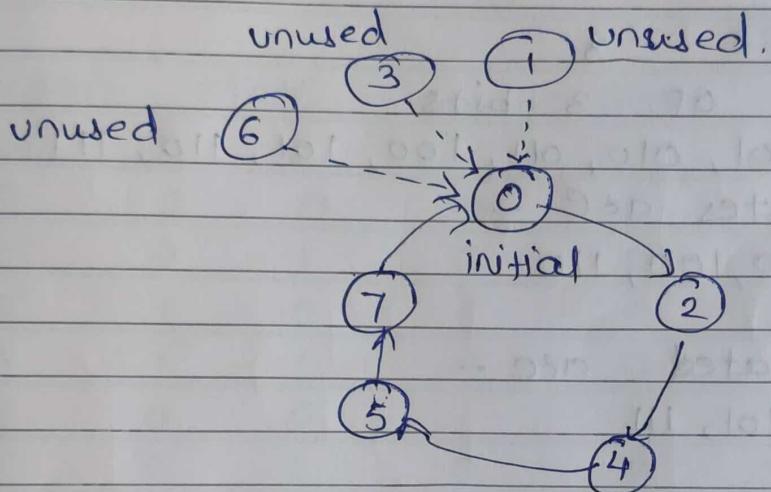
\* Practice Example:

- \* Design a Mod-5 asynchronous counter using T FF.

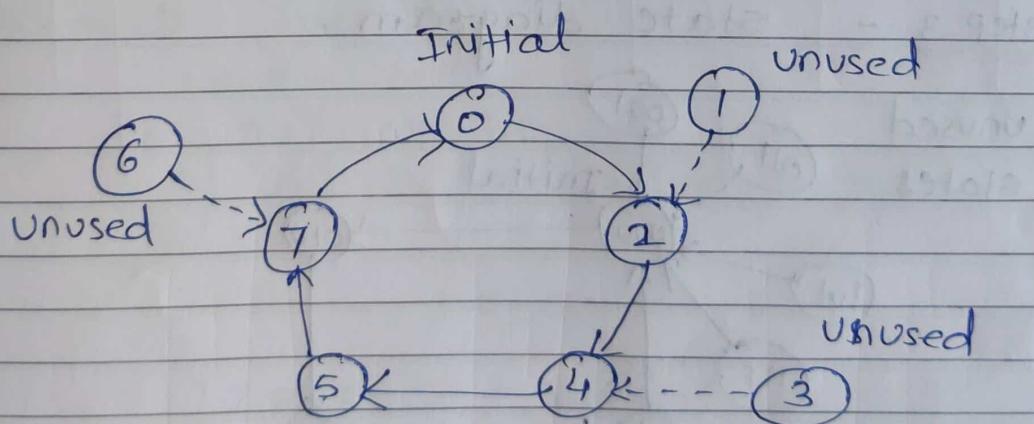
## Lockout condition in synchronous counter.

- The Lockout condition in a counter is a condition in which the counter goes into an unused state and is not able to active at a used state itself.
- The circuit that goes in lockout condition is called a bush less circuit.

a) unused to initial state -



b) unused to next state :-



b) unused to next state .

## [Take care of Lock out condition)

\* Example -

\* Design synchronous counter using T-type flip flops. For getting the following sequence 0-2-4-6-0.

Take care of lock out condition.

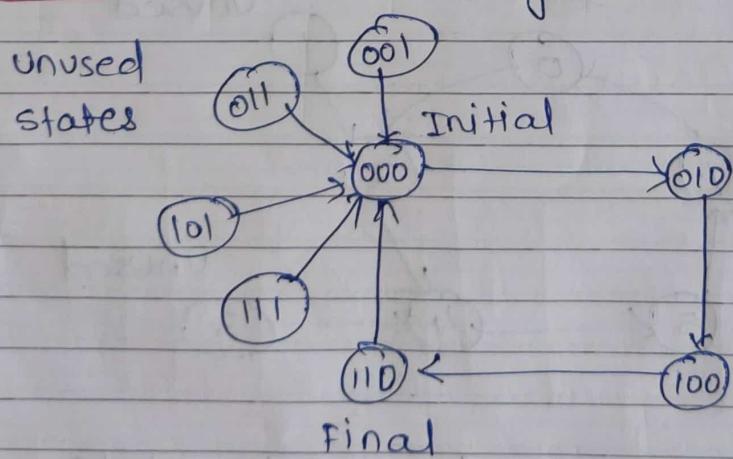
→ Step 1 - Find the number of FF's  
maximum count = 6 (3 bit)

- NO. of FF's = 3
- Sequence of 3 bits  
000, 001, 010, 011, 100, 101, 110, 111
- Used states are -  
000, 010, 100, 110
- Unused states are -  
001, 011, 101, 111

Step 2 :- Type of flip flop

- T FF.

Step 3 - State diagram.



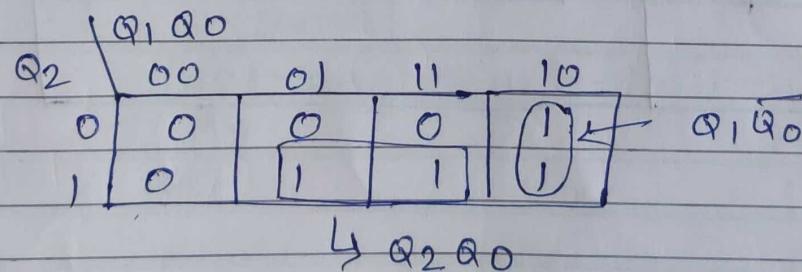
Step 4 - Excitation Table for T FF.

Present state	Next state	T
0	0	0
0	1	1
1	0	1
1	1	0

\* Step 5 - State Table

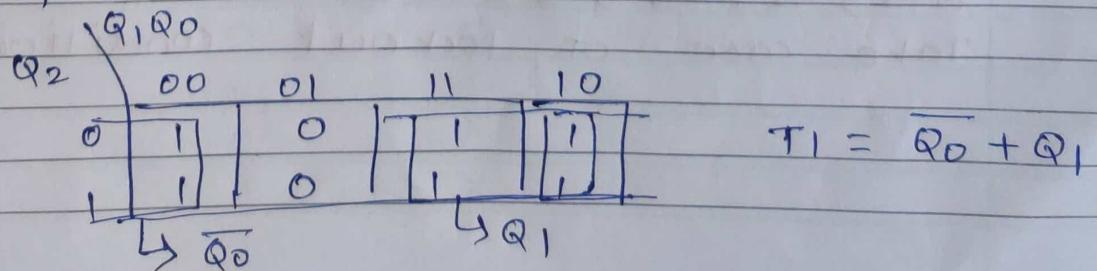
Unused	$Q_2$	Present state			Next state			Flip Flop		
		$Q_1$	$Q_0$	$Q_{2+1}$	$Q_{1+1}$	$Q_{0+1}$	$T_2$	$T_1$	$T_0$	
0	0	0	0	0	1	0	0	1	0	
0	0	1	0	0	0	0	0	0	1	
0	1	0	1	0	0	0	1	1	0	
0	1	1	0	0	0	0	0	1	1	
1	0	0	1	1	1	0	0	1	0	
1	0	1	0	0	0	0	1	0	1	
1	1	0	0	0	0	0	1	1	0	
1	1	1	0	0	0	0	1	1	1	

\* K-map for  $T_2$



$$T_2 = Q_2 Q_0 + Q_1 \bar{Q}_0$$

\* K-map for  $T_1$



$$T_1 = \bar{Q}_0 + Q_1$$

\* K-map for  $T_0$

		$Q_1 Q_0$			
		00	01	11	10
$Q_2$	0	0	(1)	(1)	0
	1	0	(1)	(1)	0

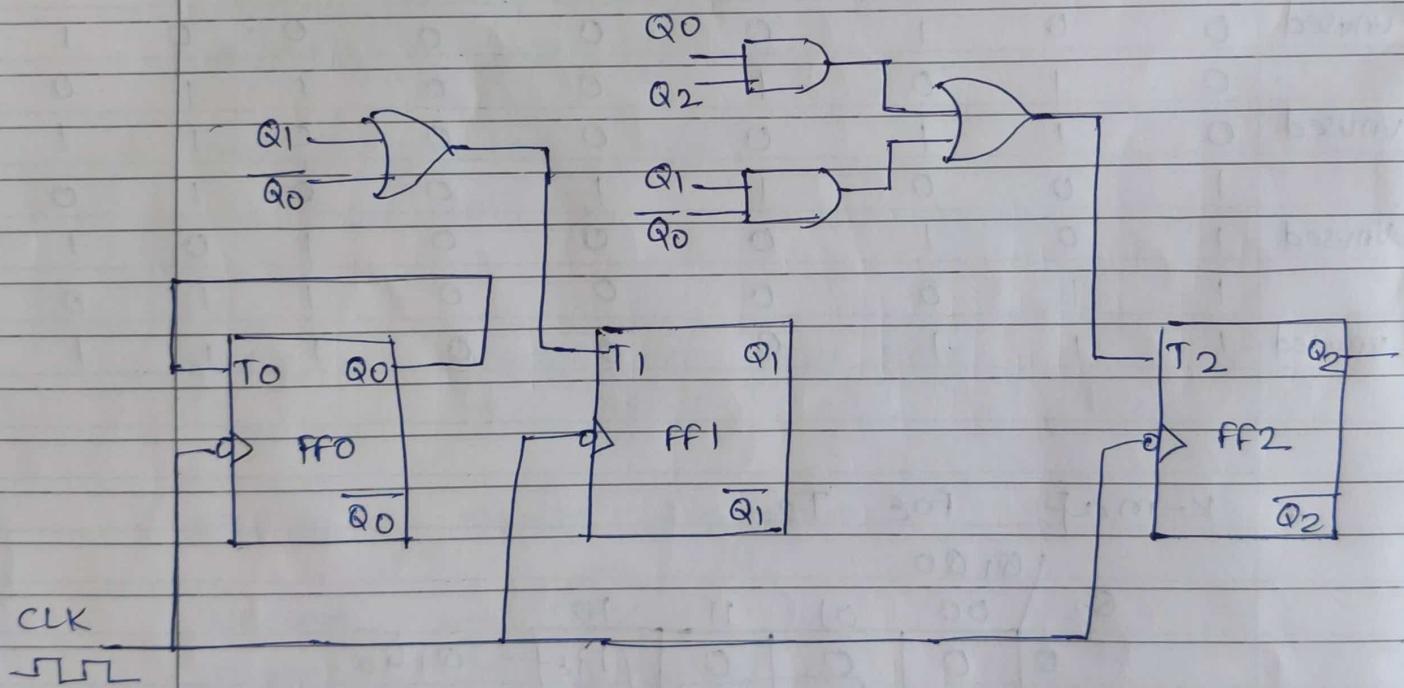
$T_0 = Q_0$

$$T_0 = Q_0$$

$$T_1 = Q_1 + \overline{Q_0}$$

$$T_2 = Q_0 Q_2 + Q_1 \overline{Q_0}$$

\* Circuit diagram:



\* Practice example:

\* Design synchronous counter using D-type ffs for getting the following sequence.  
 $0 \rightarrow 3 \rightarrow 1 \rightarrow 5 \rightarrow 6 \rightarrow 0$ .

Take care of lockout condition.

## (Avoid lock out condition)

Example -

- \* Design a synchronous counter to generate the following sequence:  
 $4 \rightarrow 6 \rightarrow 7 \rightarrow 3 \rightarrow 1 \rightarrow 4$ . Avoid lockout condition.  
use JK FF's for design.

→ Step 1 - Find the number of FFs.

5 states — 3 bit

NO. OF FF. — 3

Used state — 4, 6, 7, 3, 1

100, 110, 111, 011, 001

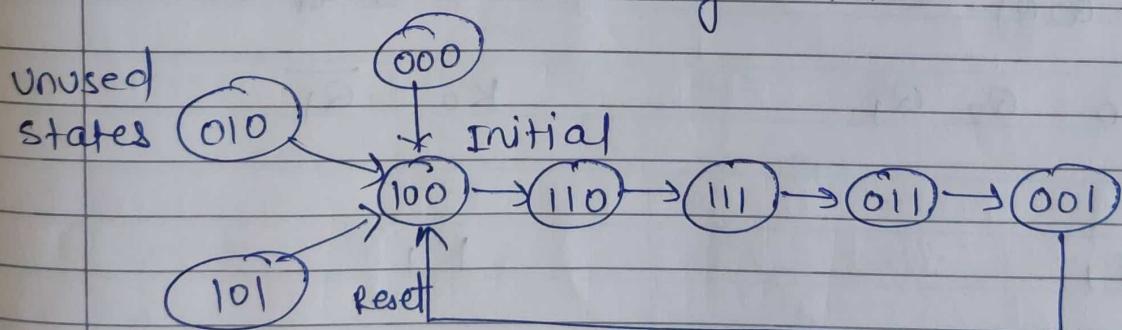
Unused state — 0, 2, 5

000, 010, 101

Step 2: Type of FF.

JK FF.

Step 3 - State diagram.



Step 4 - Excitation Table for JK FF

$Q_t$	$Q_{t+1}$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

## state Table

Present state			Next state			flip flop inputs.							
$Q_2$	$Q_1$	$Q_0$	$Q_2+1$	$Q_1+1$	$Q_0+1$	$J_2$	$K_2$	$J_1$	$K_1$	$J_0$	$K_0$		
0	0	0	1	0	0	1	X	0	X	0	X		
0	0	1	1	0	0	1	X	0	X	X	1		
0	1	0	1	0	0	1	X	X	1	0	X		
0	1	1	0	0	1	0	X	X	1	X	0		
1	0	0	1	1	0	X	0	1	X	0	X		
1	0	1	1	0	0	X	0	0	X	X	1		
1	1	0	1	1	1	X	0	X	0	1	X		
1	1	1	0	1	1	X	1	X	0	X	0		

K-map for

$J_0$

$K_0$

$Q_2$	$Q_1, Q_0$						
	00	01	11	10			
0	0	X	X	0			
1	0	X	X	X			

$Q_2 Q_1 \leftarrow$

$Q_2$	$Q_1, Q_0$						
	00	01	11	10			
0	X		0	X			
1	X		0	X			

$\Downarrow \overline{Q_1}$

$$J_0 = Q_2 Q_1$$

$$K_0 = \overline{Q_1}$$

$J_1$

$K_1$

$Q_2$	$Q_1, Q_0$						
	00	01	11	10			
0	0	0	X	X			
1	1	0	X	X			

$\Downarrow Q_2 \overline{Q_0}$

$$J_1 = Q_2 \overline{Q_0}$$

$Q_1, Q_0$

$Q_2$	$Q_1, Q_0$						
	00	01	11	10			
0	(X)	X		0			
1	X	X	0	0			

$\Downarrow \overline{Q_2}$

$$K_1 = \overline{Q_2}$$

$J_2$

		$Q_1 Q_0$
		00 01 11 10
$Q_2$	0	1 0 1
1	X X X X	

$\hookrightarrow \bar{Q}_1 + \bar{Q}_0$

$K_2$

		$Q_1 Q_0$
		00 01 11 10
$Q_2$	0	X X X
1	0 0 1 0	

$\hookrightarrow Q_1 Q_0$

$$J_2 = \bar{Q}_1 + \bar{Q}_0$$

$$K_2 = Q_1 Q_0$$

$$J_0 = Q_2 Q_1$$

$$K_0 = \bar{Q}_1$$

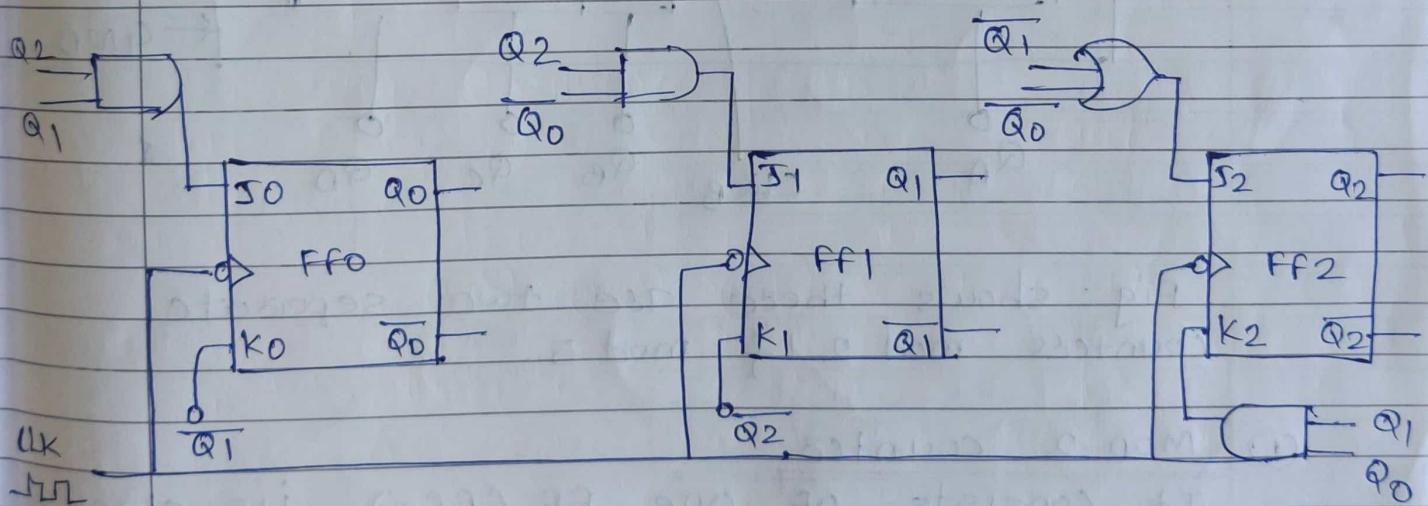
$$J_1 = \frac{Q_2}{Q_0}$$

$$K_1 = \bar{Q}_2$$

$$J_2 = \frac{Q_1}{Q_0} + \frac{Q_0}{Q_1}$$

$$K_2 = Q_1 Q_0$$

\* circuit diagram:-



## IC 7490

### \* IC 7490 - DECADE COUNTER.

- It is a 4-bit ripple type decade counter
- It can be used as a simple counter from 0 to 9, that is it has 10 distinct states hence called as a decade counter.

### \* Block diagram:

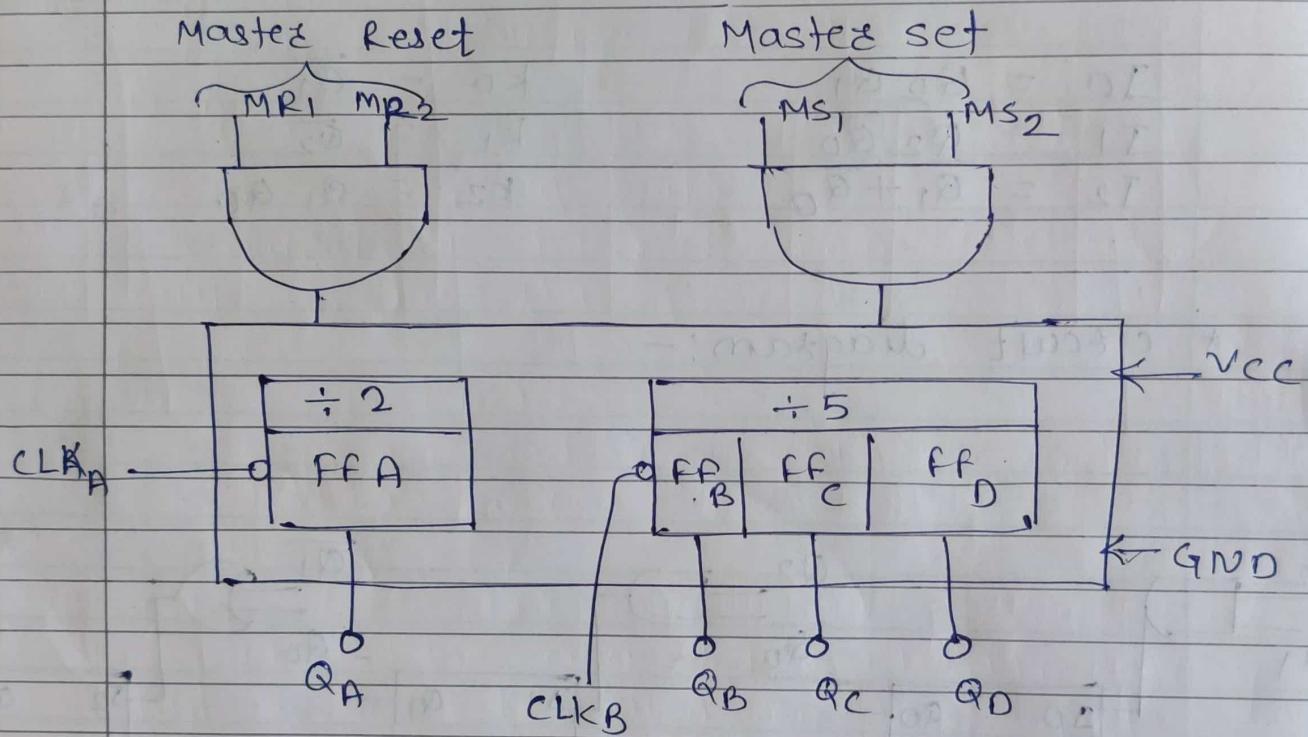


Fig: shows there are two separate counters, mod 2 & mod 5.

#### ① MOD 2 counter.

- It consists of one FF (FFA), its clock input is CLK<sub>A</sub> & output Q<sub>A</sub>
- The high to low transition on CLK<sub>A</sub> input toggles FFA

\* MOD 5 counter.

- It consist of three FFs ( $FF_B$ ,  $FF_C$ ,  $FF_D$ )  
output of these FF's are ( $Q_B$ ,  $Q_C$ ,  $Q_D$ )
- The state of these FFs changes when the clock input to the individual FF goes from HIGH to LOW.

\* Pin diagram :-

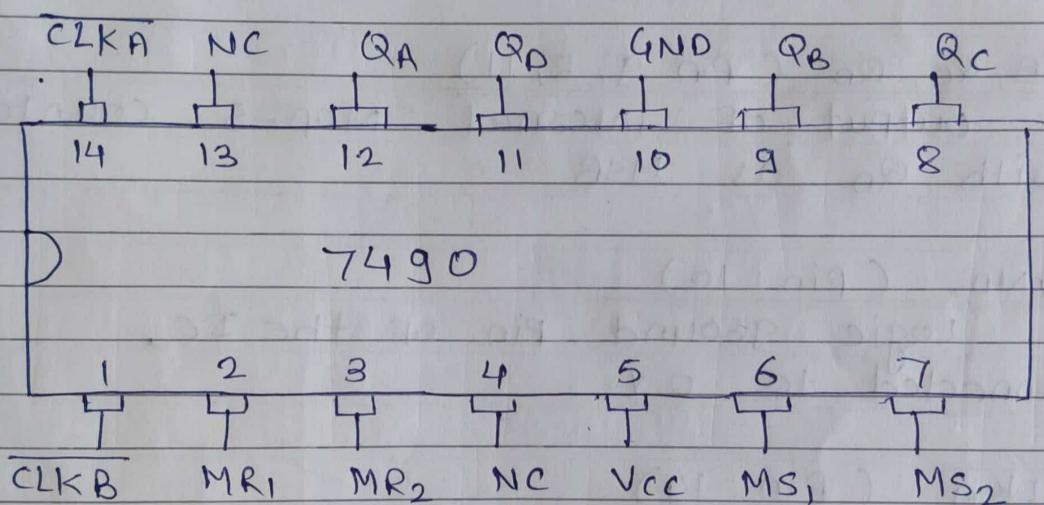


Fig: Pin Diagram of IC 7490.

Pin Description

1) Pin 1 ( $\overline{CLK_B}$ )

It is the clock i/p to  $FF_B$  in mod 5.  
high to low transition on this i/p toggles  $FF_B$

2)  $MR_1, MR_2$  (Pin 2, 3)

This are master reset i/p.  
High signals on these i/p force all o/p Low

3) NC (4, 13)

This is no connection pin.

2) Vcc (Pin 5)

This is the supply pin, to which +5V is connected.

3) MS<sub>1</sub>, MS<sub>2</sub> (Pin 6, 7)

These are master set inputs.  
High signals on these inputs sets the output to BCD nine (1001).

4) QA (Pin 12)

Output of internal mod-2 counter of FF-A.

5) QB, QC, QD (Pin 9, 8, 11)

Output of internal MOD-5 counter with QD as MSB.

6) GND (Pin 10)

Logic ground pin of the IC, connected to OR.

7) CLKA (Pin 14)

It is the clock input to FFA. Every high to low transition on this input toggles FFA.

Reset / count Truth Table (Mode selection)

RESET / SET inputs		outputs					
MR <sub>1</sub>	MR <sub>2</sub>	MS <sub>1</sub>	MS <sub>2</sub>	QA	QB	QC	QD
H(1)	H(1)	L(0)	X	L(0)	L(0)	L(0)	L(0)
H(1)	H(1)	X	L(0)	L(0)	L(0)	L(0)	L(0)
X	X	H(1)	H(1)	H(1)	L(0)	L(0)	H(1)
L(0)	X	L(0)	X				
X	L(0)	X	L(0)				
L(0)	X	X	L(0)				
X	L(0)	L(0)	X				

if CLK applied it will  
count or step from  
Previous to Next step.

## \* Applications of 7490

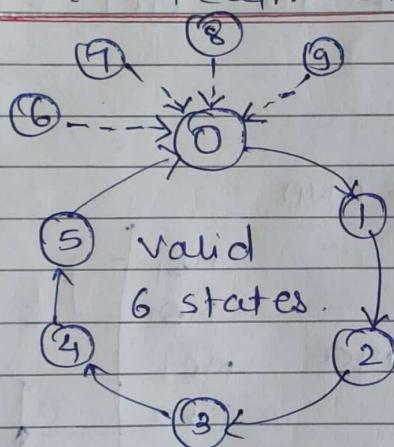
IC 7490 can be used as

- 1) Mod 2 or divide by 2 counter
- 2) Mod 5 or divide by 5 counter
- 3) Mod 10 counter
- 4) Mod N counter

## \* Example.

Q. Draw MOD 6 counter using IC 7490.

Solution  $\rightarrow$  Step 1 :- Truth state diagram.



0 - 5 - valid states

6 - 9 - Invalid states.

## Step 2 : Truth Table

Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>	Y	
0	0	0	0	0	
0	0	0	1	0	
0	0	1	0	0	
0	0	1	1	0	
0	1	0	0	0	
0	1	0	1	0	
0	1	1	0	1	
0	1	1	1	1	
1	0	0	0	1	
1	0	0	1	1	

valid states

invalid states.

### Step 3 - K-map.

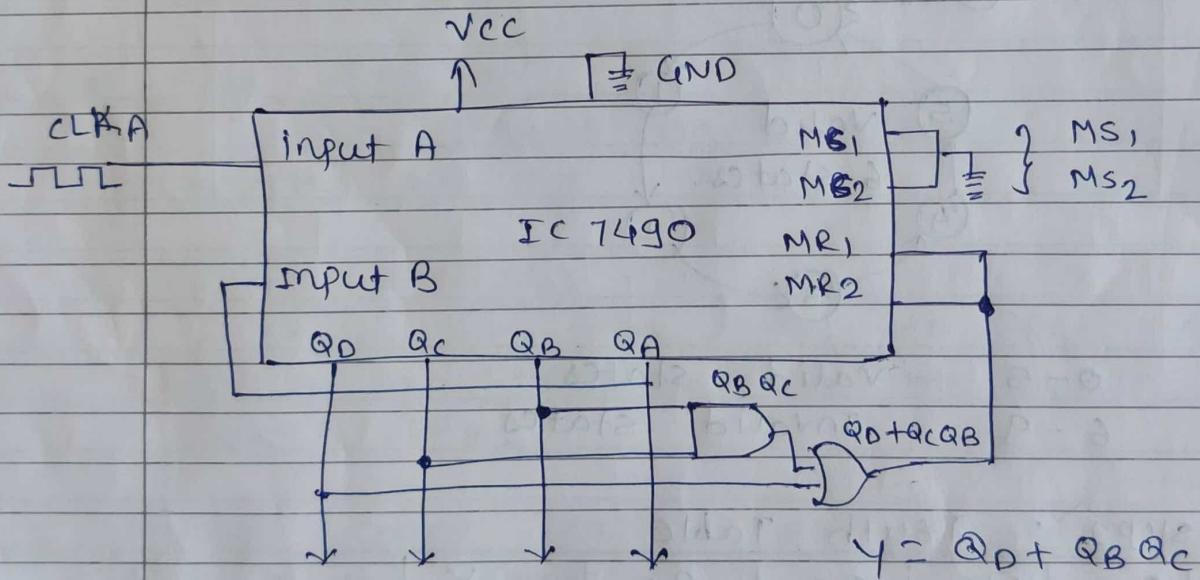
		QB	QA				
		QD	QC	00	01	11	10
00		00	00	00	01	03	02
01		04	05	17	16	15	14
11		18	19	13	11	10	15
10		18	19	11	10	15	16

$$Y = Q_D + Q_C Q_B$$

### Step 4 :- Diagram.

Total no. of states is 6

$Q_C$  &  $Q_B, Q_D$  connected to  $MR_1$  &  $MR_2$  (Pin 2, 3)



### \* Practice example

Q. Design MOD-7 counter using 7490.