

UNIT - 5

Logic Families.

classmate

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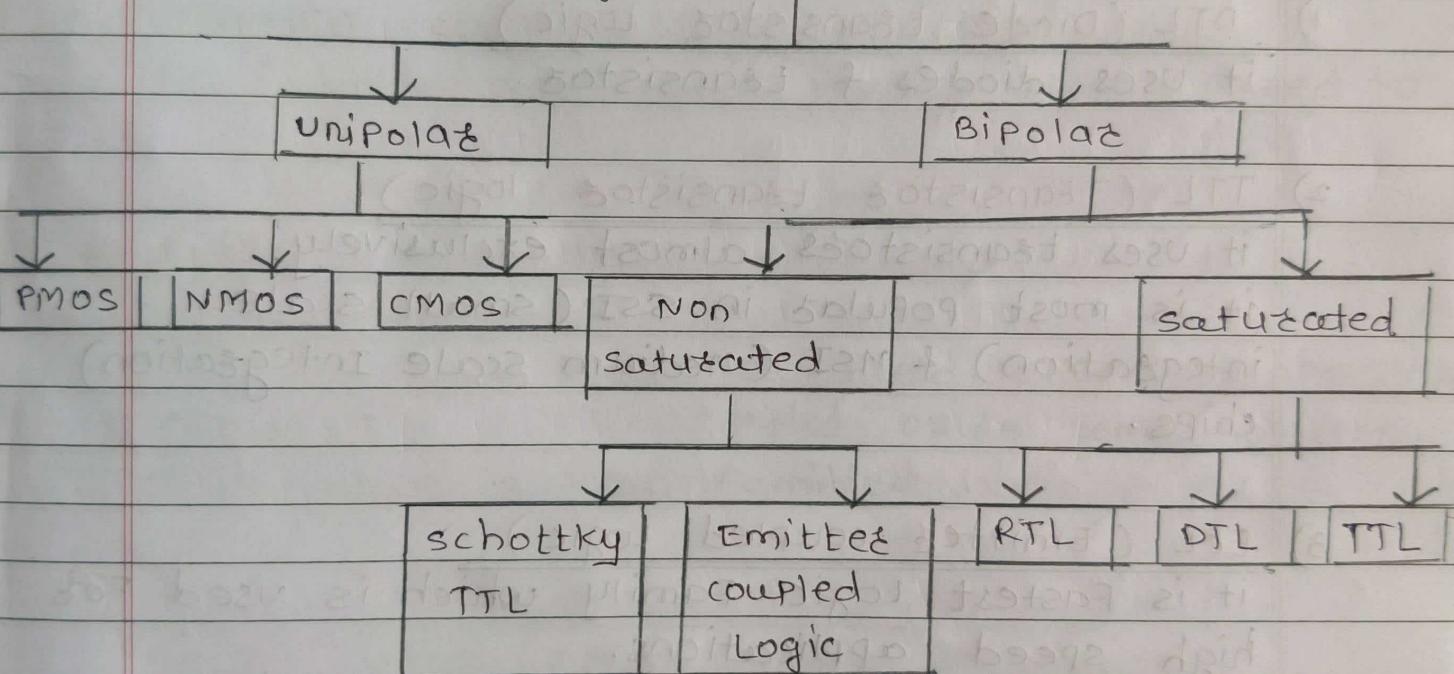
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* Logic family :-

Logic Family is a collection of different integrated circuits chips that have similar input, output & internal circuit char. but they perform different logic gate functions such as AND, OR, NOT, etc.

* Classification of Logic Family :-

Logic families.



PMOS - (P-channel MOSFET)

NMOS - (N-channel MOSFET)

CMOS - (complementary MOSFET)

IIL - Integrated injection logic.

RTL - Resistor Transistor Logic

DTL - Diode Transistor Logic

TTL - Transistor Transistor Logic

ECL - Emitter coupled Logic

DCTL - direct coupled transistor Logic

HTL - High threshold Logic.

* Bipolar Families:-

- It mainly uses bipolar devices like diodes, transistors, capacitors, resistors.
- In bipolar there are 3 basic families called -
 - Diode transistor logic (DTL)
 - Transistor transistor logic (TTL)
 - Emitter coupled logic (ECL)

1) DTL (Diode Transistor Logic)

it uses diodes & transistors.

2) TTL (Transistor Transistor logic)

it uses transistors almost exclusively.

it is most popular in SSI (small scale integration) & MSI (Medium scale Integration) chips.

3) ECL (Emitter coupled logic)

it is fastest logic family which is used for high speed applications.

* Saturated Bipolar Logic Family:-

- the bipolar transistors are used as the main device.

It is used as a switch & operates in saturation & cut-off regions.

Examp:-

- 1) Transistor Transistor logic (TTL)
- 2) Resistor Transistor logic (RTL)
- 3) Direct coupled Transistor logic (DCTL)

- 4) Diode transistor logic (DTL)
- 5) High threshold logic (HTL)
- 6) Integrated injection logic (IIL or I2L)

* Unsaturation bipolar logic Family:

- the bipolar transistor is not driven into hard saturation.
- these increases the speed of operation.

Example -

- 1) Schottky TTL
- 2) Emitter coupled Logic (ECL)
(both are much faster as compared to TTL)

* Unipolar Families:-

MOS Family :-

It uses the MOS field effect transistors (MOSFET) ^{↳ Metal oxide semiconductor.}

- These are 3 logic Families;

1) PMOS (p-channel MOSFET's Family)

It is the oldest & slowest type.

2) NMOS (n-channel MOSFET's Family)

It is used for large scale integration for microprocessors & memories.

3) CMOS (complementary MOSFET's Family)

It is used where low power consumption is needed such as in pocket calculators.

It is used in n-channel & p-channel as a push-pull arrangement.

Q. Explain characteristics of digital ICs.

- 1) Threshold voltage
- 2) Propagation delay.
- 3) Power dissipation.
- 4) Power delay Product
- 5) Voltage current parameters.
- 6) Fan in
- 7) Fan out
- 8) Noise margin
- 9) Operating temperature.
- 10) Threshold voltage :-

- It is the value of input voltage at which the output of a logic gate makes transition from one state to another.
- It is denoted by V_{TH} .

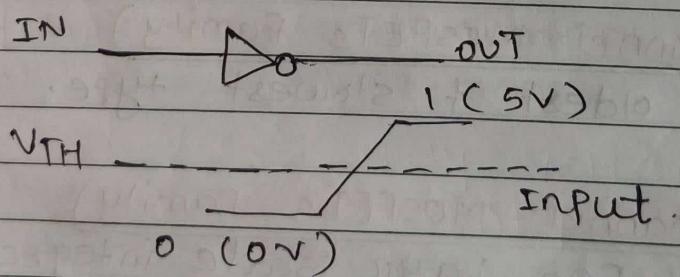


fig: Threshold voltage.

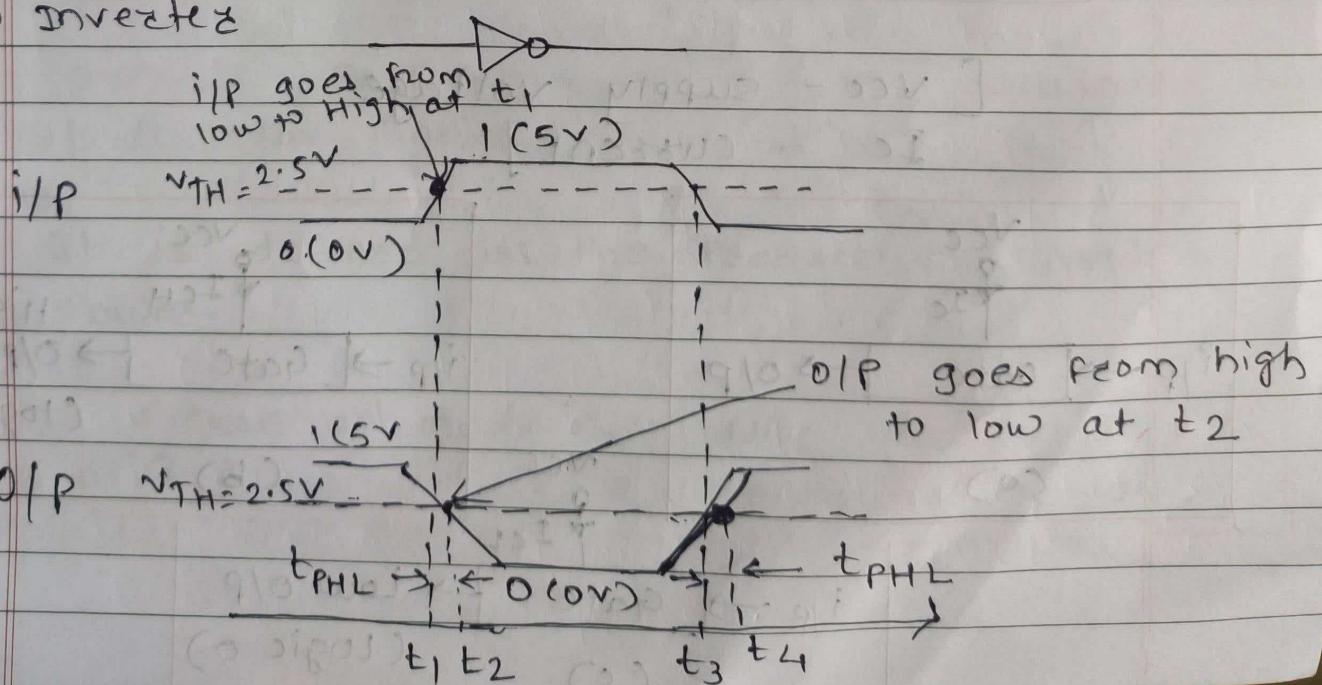
- It is a simple logic gate inverted with the input wave form.
- when i/p changes from 0 to 1, then the o/p changes from 1 to 0.

- when i/p voltage is less than V_{TH} then the o/p remains high.
- But when i/p voltage crossed V_{TH} while going from low to high then o/p will change state.

2) Propagation Delay (t_p)

- Propagation delay is the time taken by the o/p to change its state after input changes.
- It is denoted by $\underline{t_p}$.
- There is a time delay between two time instant is called as the propagation delay.
- Because of some delays in the gate circuit, the o/p of the gate does not change immediately, after i/p changes.
- It takes some time to respond to change in i/p.

a) Inverter



- Propagation delay when the o/p goes from High to low

$$t_{PH2} = t_2 - t_1$$

- Propagation delay when the o/p goes from low to High

$$t_{PLH} = t_4 - t_3$$

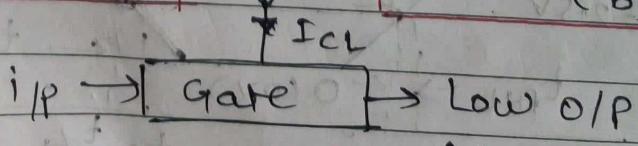
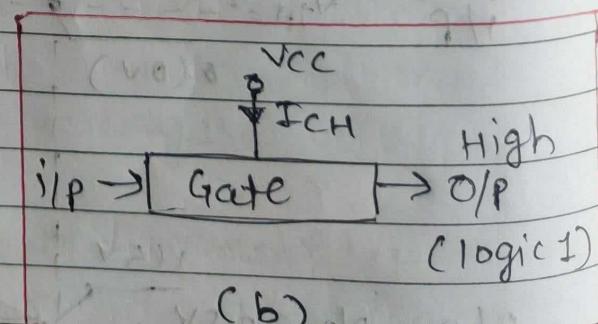
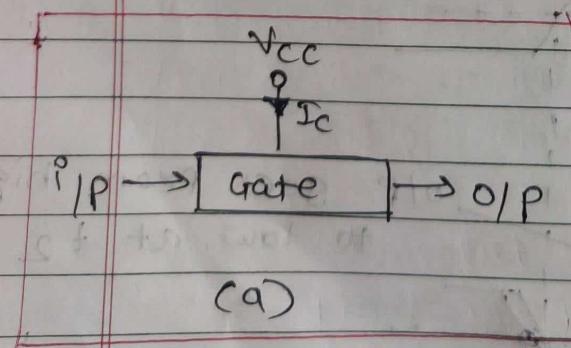
3) Power dissipation:

- Due to applied voltage & current flowing through the logic IC's, some power will be dissipated in it is called power dissipation.

The power dissipation of the gate is calculated from the voltage & current as.

$$P_D = \text{Power dissipation} = V_{CC} \times I_C$$

$$\begin{aligned} & [V_{CC} - \text{Supply voltage}] \\ & [I_C - \text{current}] \end{aligned}$$



I_{CH} \Rightarrow current drawn from the supply when the o/p is High. (fig b)

I_{CL} \Rightarrow current drawn from the supply when the o/p is Low (fig c)

calculate the power, take the avg of these two.

$$I_c(\text{avg}) = \frac{I_{CH} + I_{CL}}{2}$$

Now, the avg power is calculate as

$$P_D(\text{avg}) = V_{CC} \times I_c(\text{avg}) \text{ (watts)}$$

[usually this power is in milli watts]

4) Power delay Product :- (PDP)

Fig of merit

- overall performance I_c is calculated by the fig of merit
- It is defined as the product of speed & power.

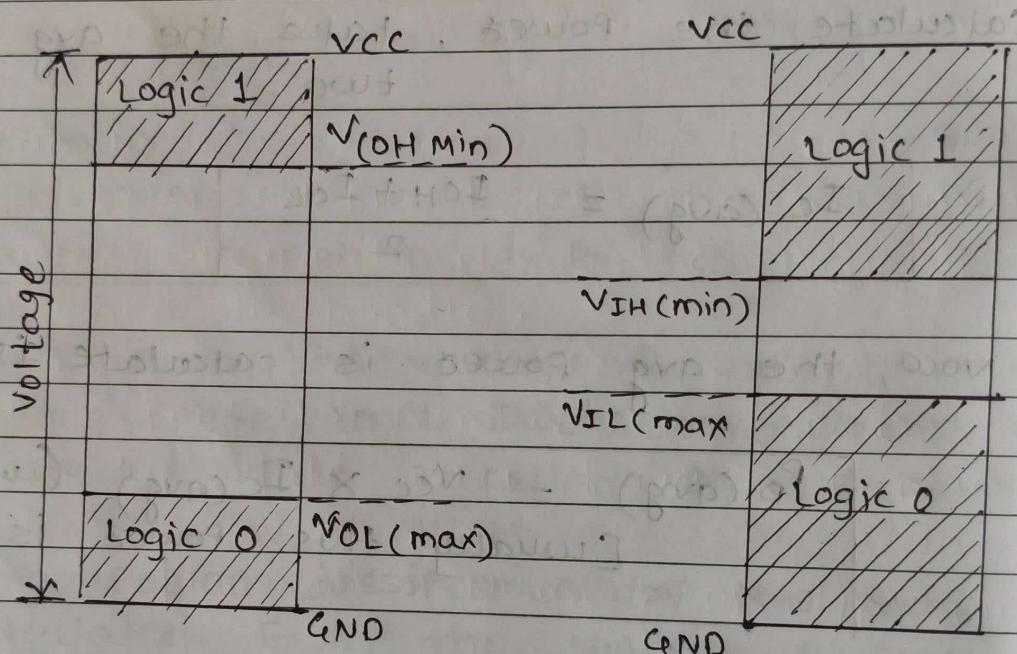
$$\text{Figure of merit} = \text{Power dissipation} \times (PDP) \times \text{Propagation delay.}$$

5) Voltage & current Parameters :-

- These are 2 voltage levels.

① input voltage level

② output voltage level.



input voltage levels of 0V & 5V are called as logic 0 & logic 1

$V_{OH\min}$ - High Level output voltage

$V_{OL\max}$ - Low Level output voltage

$V_{IH\min}$ - High Level input voltage

$V_{IL\max}$ - Low Level input voltage.

* Low level input voltage = $V_{IL\max}$

This is the maximum i/p voltage which is recognised by the gate as logic 0.

* High Level input voltage : $V_{IH}(\min)$

This is the minimum i/p voltage which is recognised by the gate as logic 1.

* Low Level output voltage : $V_{OL}(\max)$

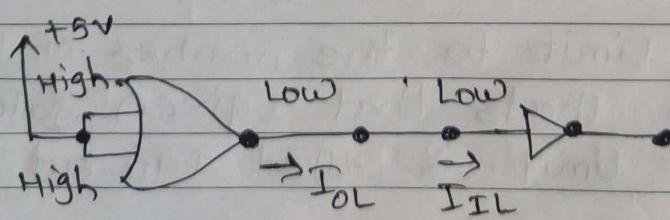
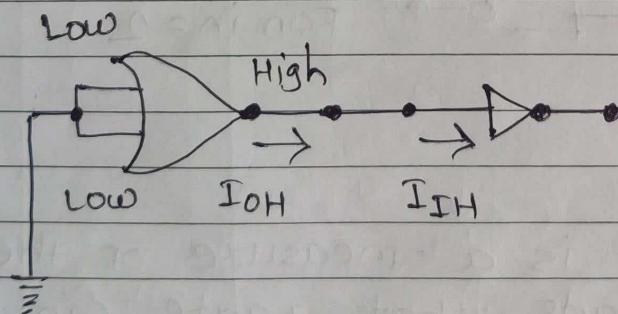
This is the maximum output voltage which is recognised by the gate as logic 0.

* High Level output voltage : $V_{OH}(\min)$

This is the minimum output voltage which is recognised by the gate as logic 1.

* current Levels :

- 1) High Level input current (I_{IH}) (1 Level vlg)
- 2) Low Level input current (I_{IL}) (0 Level vlg)
- 3) High Level output current (I_{OH}) (1 Level)
- 4) Low Level output current (I_{OL}) (0 Level)



* High Level supply current $I_{cc}(1)$

This is the supply current when the O/P of the gate is at logic 1.

High Level supply current $I_{cc}(0)$

This is the supply current when the O/P of the gate is at logic 0.

⑥

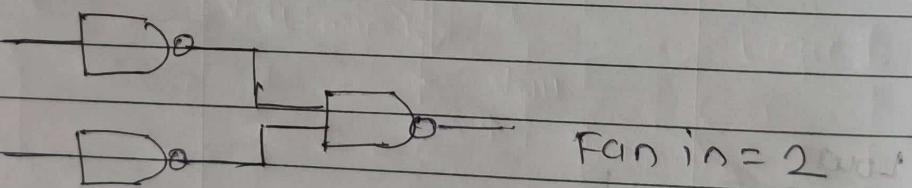
Fan-in :-

It is defined as the maximum number of inputs that the logic gate is designed to handle.

It effects to number of input pins.

Two I/P gates will have a fan-in = 2.

$\boxed{\text{Fan-in} = \text{Number of I/P pins}}$



⑦

Fan-out :-

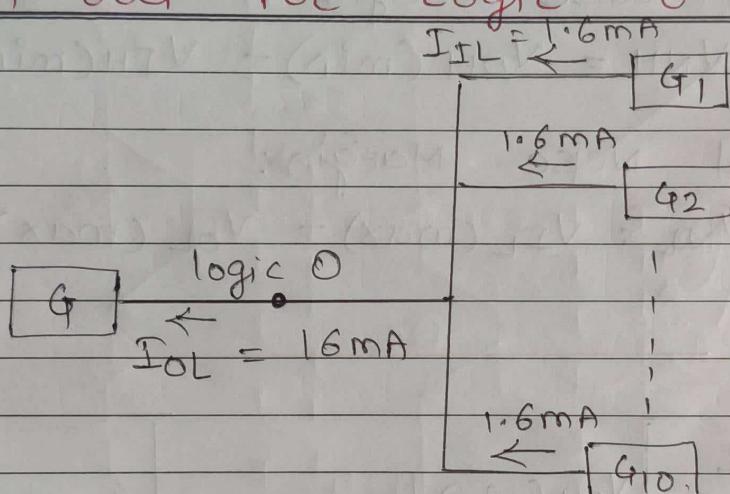
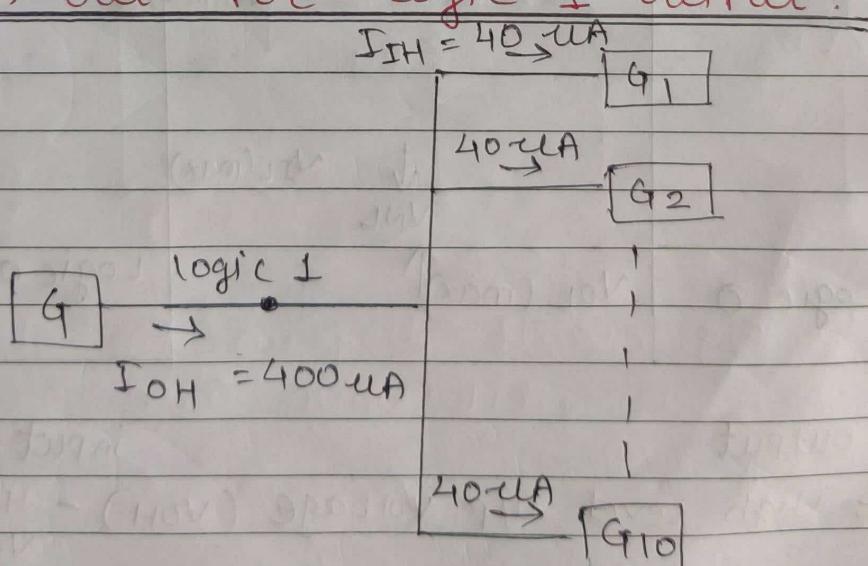
Fan-out is a measure of the number of loads that a gate can drive.

- There is a limit to the number of load gate inputs that a given gate can drive. The limit is called fan-out of the gate.

(Low state)

$$\text{Fan out} = \frac{I_{OL}(\text{max})}{I_{IL}(\text{max})}$$

$$\text{Fan out} = \frac{I_{OH}(\text{max})}{I_{IH}(\text{max})}$$

Fan-out for Logic 0 output :-Fan-out for Logic 1 output :-

8) Noise Margin :- (Noise immunity)

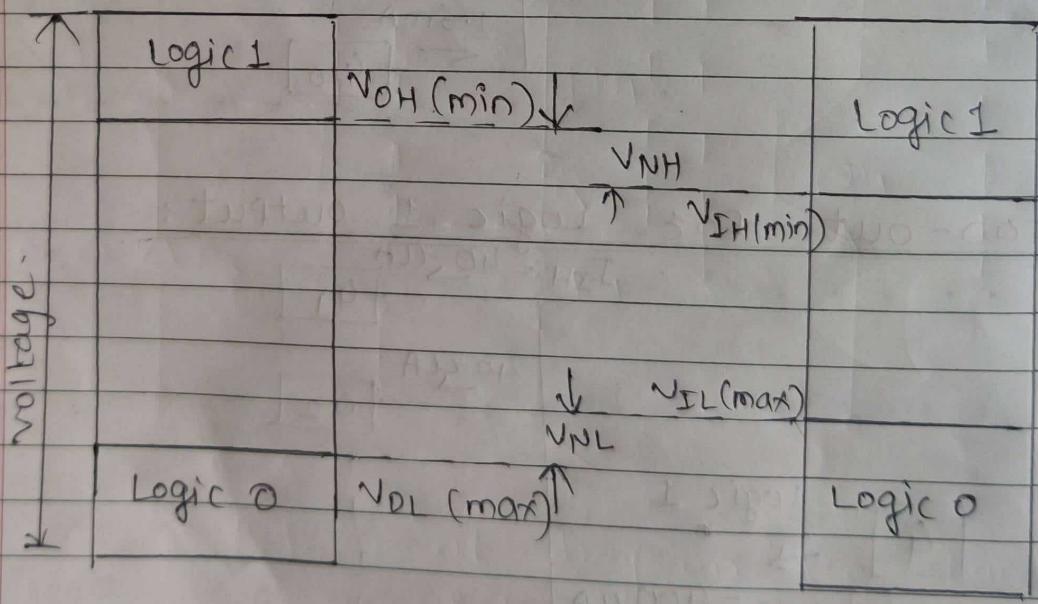
- Noise immunity is the ability of a circuit to get not affected by the noise in the system.
- A quantitative measure of a noise immunity is a noise margin.

High Level noise margin:

$$V_{NH} = V_{OH}(\text{min}) - V_{IH}(\text{min})$$

Low Level noise Margin:

$$V_{NL} = V_{IL}(\text{max}) - V_{OL}(\text{max})$$



Output

input

V_{NH} = High level O/P voltage (V_{OH}) - High level I/P voltage (V_{IH})

V_{NL} = Low level I/P voltage (V_{IL}) - Low level O/P voltage (V_{OL})

g) operating temperature °C

- The operating temperature is the range of ambient temp. within which a power supply, or any other electrical equipment, operate in.

Temperature range

For commercial : 0 to 70°C

For industrial : 0 to 85°C

For military : - 55°C to 125°C

Transistor Transistor Logic (TTL)

— NAND Gate.

Q. Explain the operation of TTL NAND Gate.

Diagram:

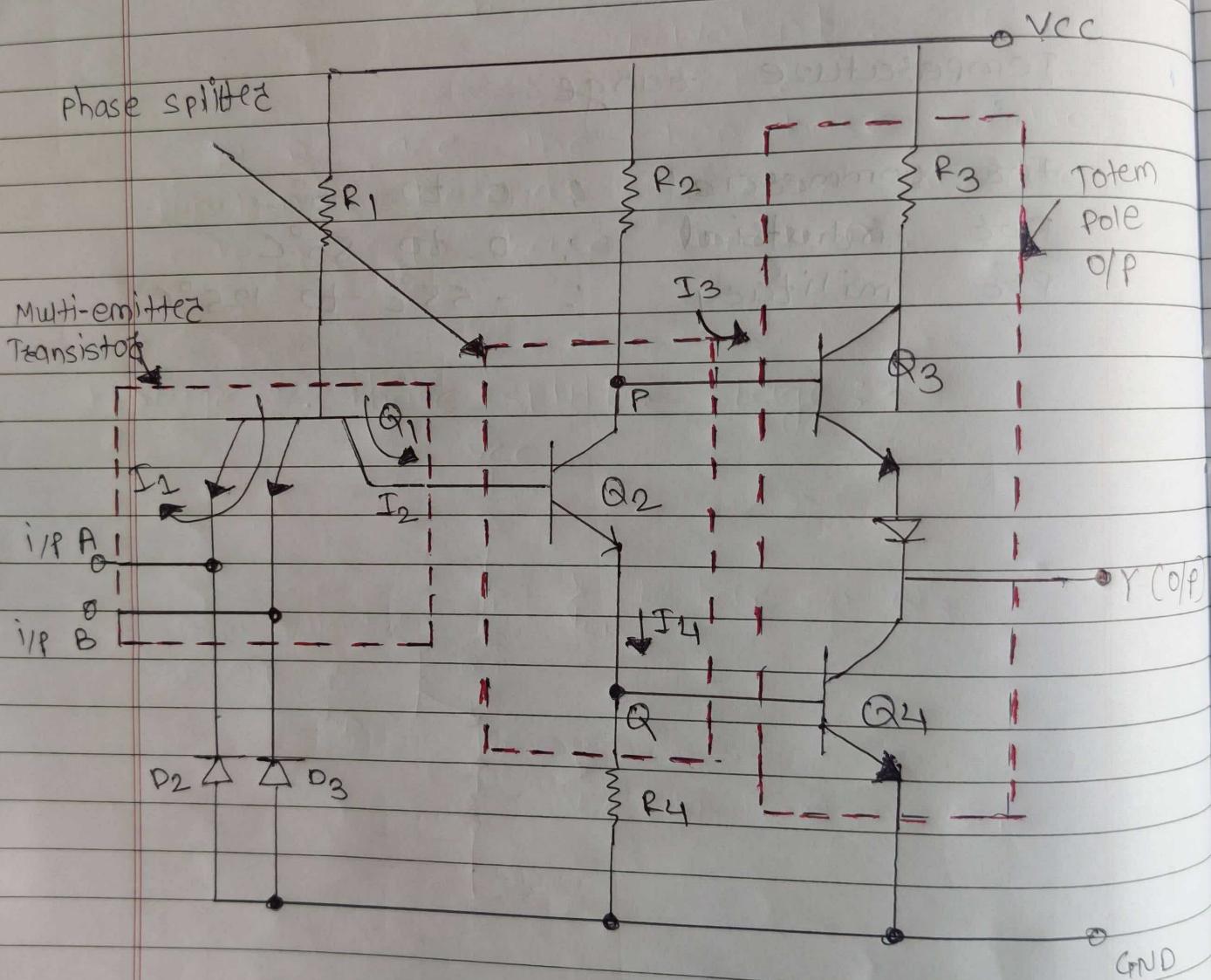


Fig: circuit diagram for standard
TTL NAND Gate.

- TTL NAND gate it mainly consist of 3 stages.

i) Multi-emitter transistors.

ii) Phase emitter splitter

iii) Totem pole output

- Two types of Transistors.

i) N-P-N Transistors (Negative - Positive - Negative)

ii) P-N-P Transistors (Positive - Negative - Positive)

- Resistors : use for current control

- Diode : unidirectional device

- Transistors : use as a switch — NPN, PNP.

Stage 1: Multi-emitter transistors:

- It has 3 terminals — Base, emitter, collector. one base terminal, one collector & NO. OF emitters.

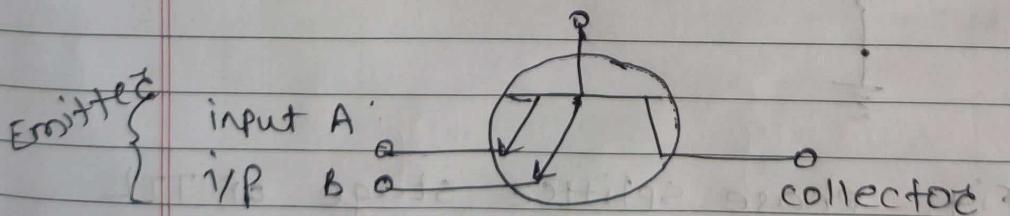


fig: Multi emitter Transistor symbol.

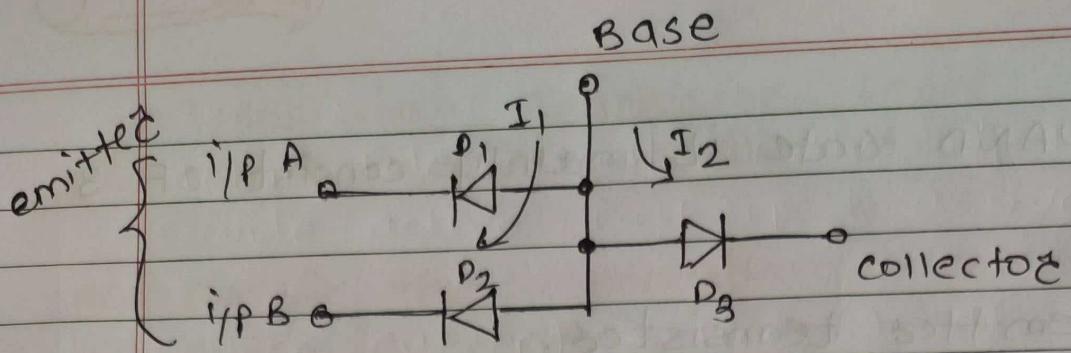


fig: Multi emitter transistor diode equivalent.

D_1 , D_2 are the two base emitted junction, whereas D_3 represents the collector to base Junction.

* Stage 2: Phase splitted stage :-

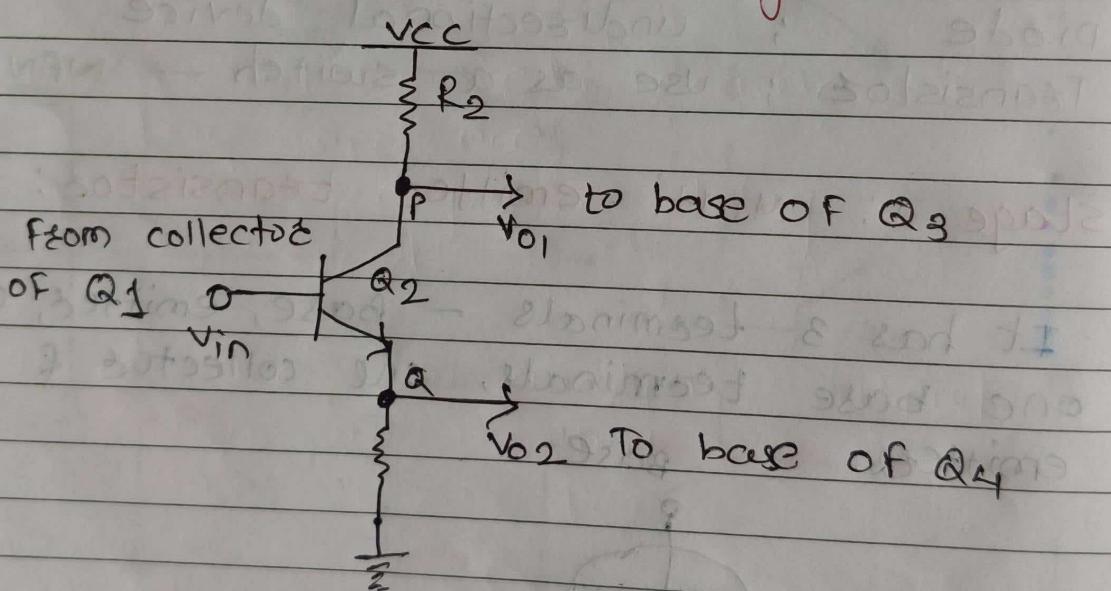


Fig: phase splitted stage of TTL

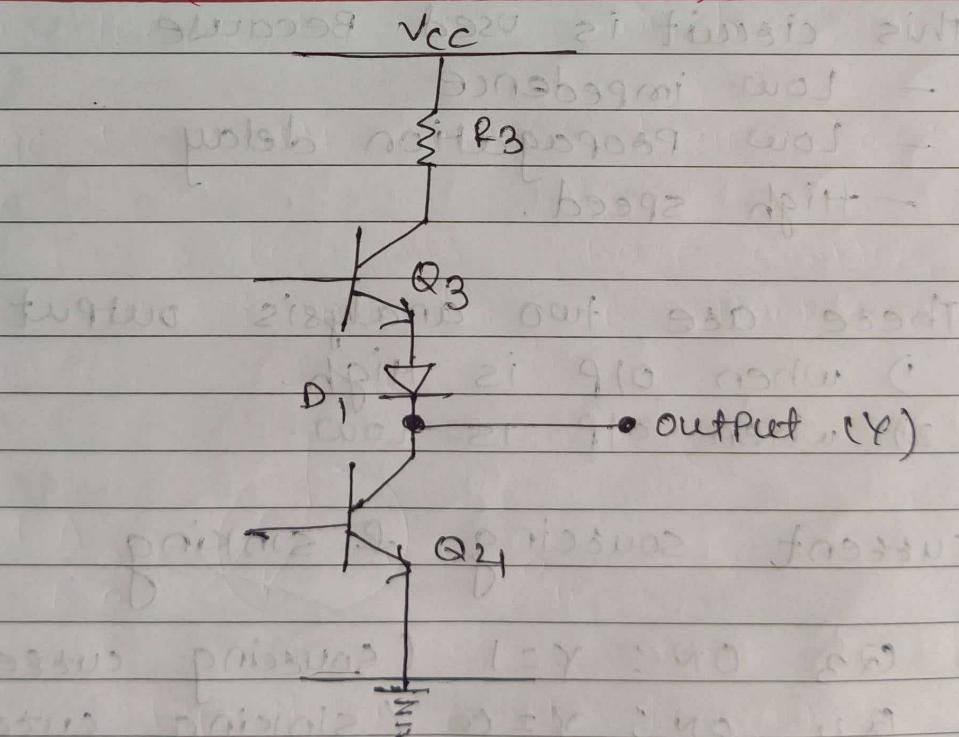
- this stage consist of transistors Q_2 , whose two O/P at point $P + Q$ are connected to bases of NPN transistors $Q_3 + Q_4$ of the next stage.

- The transistor Q_2 takes care that when Q_3 is ON then Q_4 is OFF & vice versa.
- When V_{in} is low, then Q_2 is OFF.
- When V_{in} is high, then Q_2 is ON.

$V_{in} = \text{HIGH} \Rightarrow Q_2 \text{ ON} \Rightarrow Q_3 \text{ OFF} \text{ &} Q_4 \text{ ON}$

$V_{in} = \text{LOW} \Rightarrow Q_2 \text{ OFF} \Rightarrow Q_3 \text{ ON} \text{ &} Q_4 \text{ OFF}$

~~SMP~~ Stage 3: Totem Pole output stage.
(Active pull up)

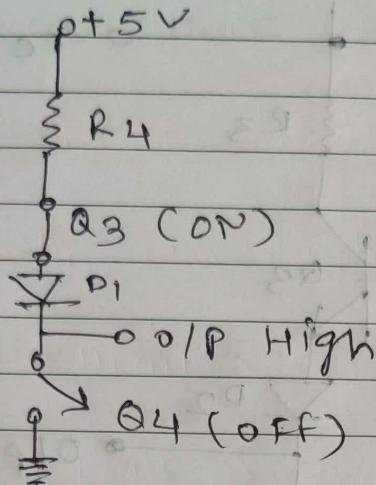


- totem-pole circuit on the o/p is used to provide active pull-up & active pull-down.
- source-current refers to the ability of the digital output port to supply current.
- sink current refers to the ability of the port to receive current.
- totem pole output used for reduce propagation delay.
- The totem pole used Transistor Q3, Diode D1, & transistor Q4.
- this circuit is used because.
 - low impedance
 - low propagation delay
 - high speed.
- There are two analysis output
 - 1) when o/p is High.
 - 2) when o/p is Low.
- current sourcing & sinking.

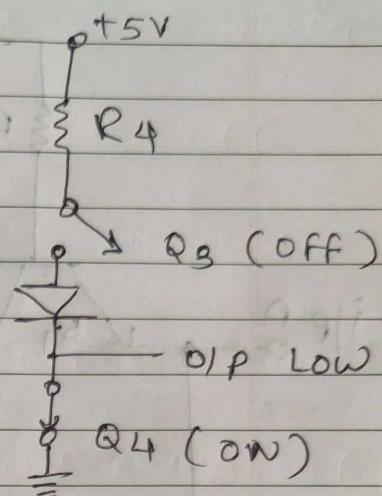
Q3 ON: $r=1$ (sourcing current)

Q4 ON: $r=0$ (sinking current)

static analysis when output is High



static analysis when output is Low.



Operations:

case 1 : AB = 00, 01, 10

Q₁ ON \rightarrow Q₂ OFF \rightarrow Q₃ ON \rightarrow Q₄ OFF

Result Y = 1

A = 0 \leftarrow B = 0 \rightarrow Y = 1

A = 0 \leftarrow B = 1 \rightarrow Y = 1

A = 1 \leftarrow B = 0 \rightarrow Y = 1

case 2 : AB = 11

Q₁ OFF \rightarrow Q₂ ON \rightarrow Q₃ OFF \rightarrow Q₄ ON.

Result Y = 1

A = 1 B = 1 \rightarrow Y = 0

i/p		Transistor				o/p	
A	B	Q ₁	Q ₂	Q ₃	Q ₄	Y	
0	0	ON	OFF	ON	OFF	1	
0	1	ON	OFF	ON	OFF	1	
1	0	ON	OFF	ON	OFF	1	
1	1	OFF	ON	OFF	ON	0	

* TTL Inverter :-

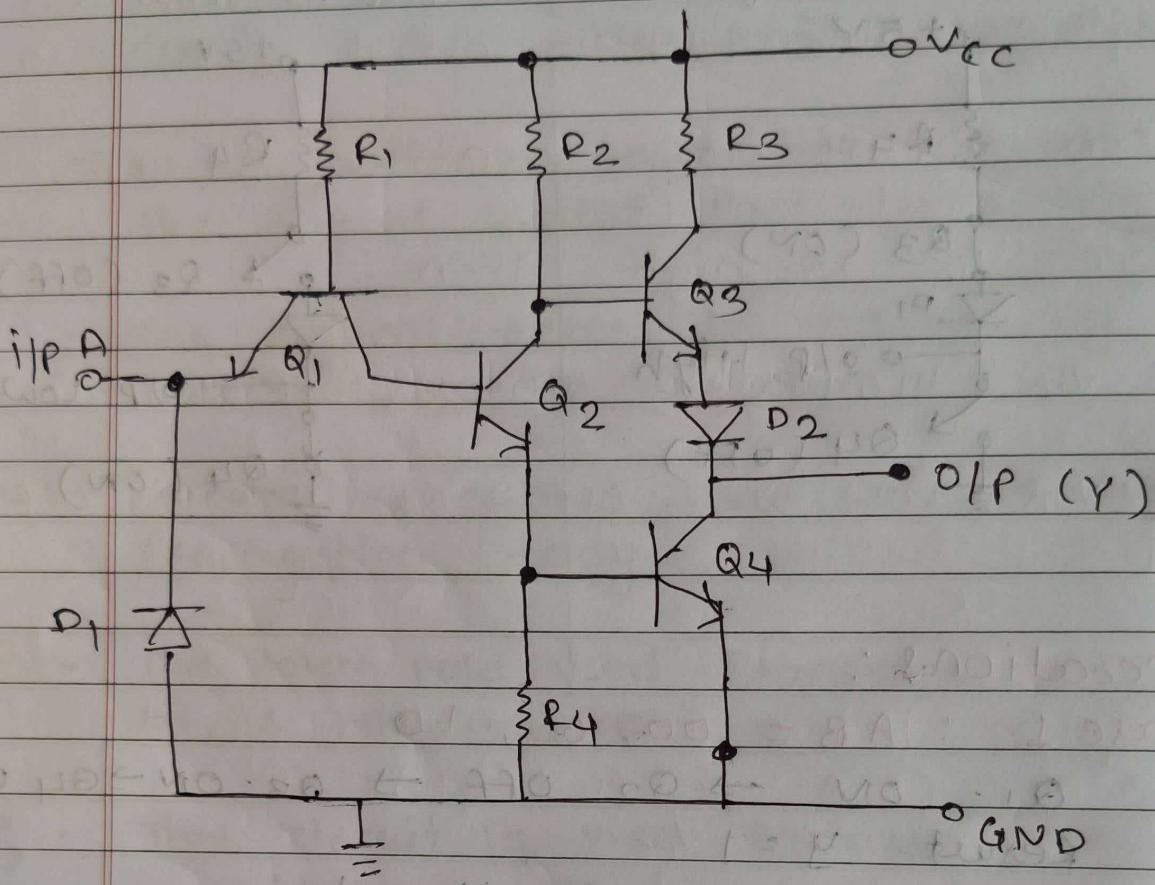


Fig: TTL Inverter circuit.

Operations.

- There are only one input (A) to the inverter, so there are only two possible combination
 $A = 0$ & $A = 1$

Case 1 $A = 0$

Here the emitter of Q1 is connected to a low voltage, making it ON, Q2 OFF

- When Q2 is off, it makes Q3 ON & Q4 OFF.

so, the o/p is connected to Vcc through Q3, result $Y = 1$

$$\boxed{A = 0 \rightarrow Y = 1}$$

case 2 $A = 1$

Hence the emitter of Q1 is connected to a high voltage, making it OFF, so Q2 turns ON.

when Q2 is ON, it makes Q3 OFF & Q4 ON. Result $Y = 0$

$$\boxed{A = 1 \rightarrow Y = 0}$$

Truth Table.

input	Transistor				output
A	Q1	Q2	Q3	Q4	Y
0	ON	OFF	ON	OFF	1
1	OFF	ON	OFF	ON	0

Table 1.15.1 : Characteristics of TTL sub families

Performance rating	74	74L	74H	74S	74LS	74AS	74ALS
Propagation delay (ns)	9	33	6	3	9.5	1.7	4
Dissipation (mW)	10	1	23	20	2	8	1.2
Power product (pJ)	90	33	138	60	19	13.6	4.8
Clock rate (MHz)	35	3	50	125	45	200	70
(same series)	10	20	10	20	20	40	20
Margin (V)	0.4	0.4	0.4	0.7	0.7	0.5	0.5

1.16 CMOS SUBFAMILIES

All of the CMOS devices have part numbers of the form "74FAMnn," where "FAM" is an alphabetic family mnemonic and nn is a numeric function designator.

Devices in different families with the same value nn perform the same function.

For example, the 74HC30, 74HCT30, 74AC30, 74ACT30, and 74AHC30 are all 8-input NAND gates.

The prefix "74" is simply a number that was used by early, popular supplier of TTL devices, Texas Instruments. The prefix "54" is used for identical parts that are specified for operation over a wider range of temperature and power-supply voltage, for use in military applications.

The first commercially successful CMOS family was 4000-series CMOS.

Advantages

Low Power Dissipation

Disadvantages

Very slow

Not easy to interface with the most popular logic family of the time, bipolar TTL

Thus, the 4000 series was supplanted in most applications by the more capable CMOS families.

HC and HCT

The first two 74-series CMOS families are HC (High-speed CMOS) and HCT (High-speed CMOS, TTL compatible).

HC and VHCT

HC (Very High-Speed CMOS) and VHCT (Very High-Speed CMOS, TTL compatible).

- These families are about twice as fast as HC/HCT while maintaining backwards compatibility with their predecessors.

► FCT and FCT-T

- In the early 1990s, another CMOS family FCT was launched.
- The key benefit of the *FCT* (*Fast CMOS, TTL compatible*) family was its ability to meet or exceed the speed and the output drive capability of the best TTL families while reducing power consumption and maintaining full compatibility with TTL.
- A variation of the family, *FCT-T* (*Fast CMOS, TTL compatible with TTL VOH*), was quickly introduced with circuit innovations to reduce the HIGH-level output voltage, thereby reducing both power consumption and switching noise while maintaining the same high operating speed as the original FCT.

► 1.17 TTL CHARACTERISTICS

UQ. Explain the standard TTL characteristic in detail.

Q. 3(a), May 13, 8 Marks

► 1.17.1 Supply Voltage

- They can operate with a single supply V_{CC} and ground. Typical values are

$$74 \text{ series} = V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$$

$$54 \text{ series} = V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$$

► 1.17.2 Threshold Voltage

- Typically for TTL logic 0 represents 0 V and logic 1 represents 5 V. Threshold voltage is calculated as the average of these two,

$$V_{TH} = \frac{0 + 5}{2} = 2.5 \text{ V}$$

► 1.17.3 Current Specifications

Currents at input and output are different for HIGH and LOW states.

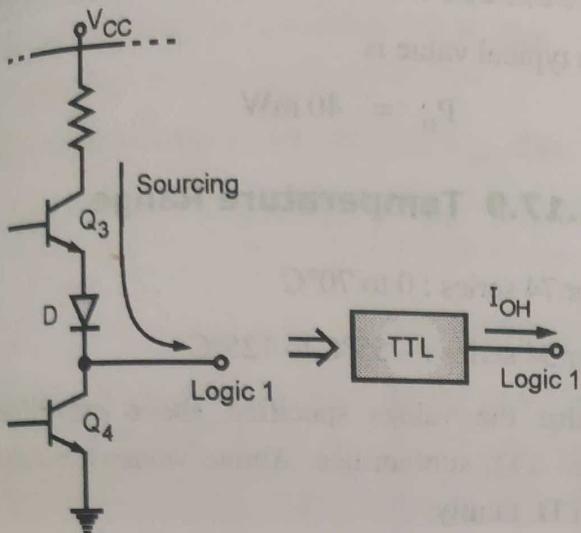
(A) Output current sourcing and sinking

- In HIGH output state, TTL output sources the current as shown in Fig. 1.17.1(a). While in LOW state it sinks

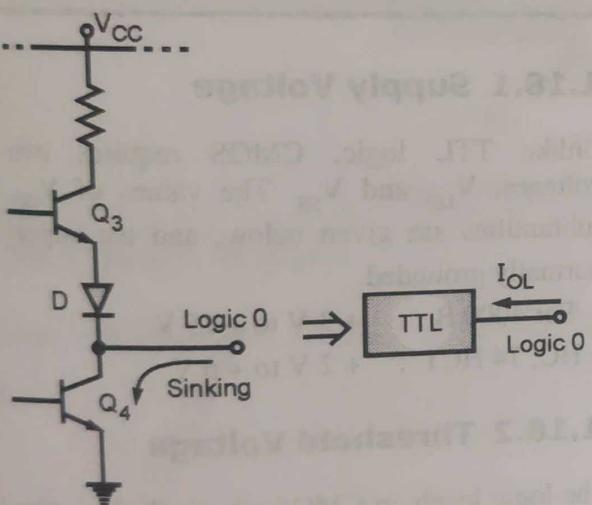
the current as shown in Fig. 1.17.1(b). Typical values are

$$I_{OL} = -400 \mu A \text{ (out)}$$

$$I_{OH} = 16 \text{ mA (in)}$$



(a) Output current in HIGH state



(b) Output current in LOW state

Fig. 1.17.1 : Output currents of TTL

(B) Input current sourcing and sinking

When logic 0 is applied at input, TTL input sources the current as shown in Fig. 1.17.2(a). While for logic 1 at the input it sinks the current as shown in Fig. 1.17.2(b). Typical values are

$$I_{IL} = -1.6 \text{ mA (out)}$$

$$I_{IH} = 40 \mu A \text{ (in)}$$

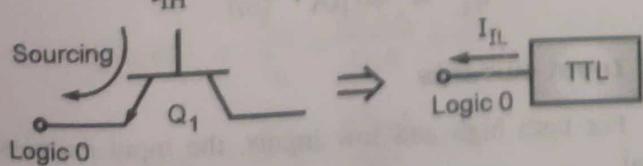
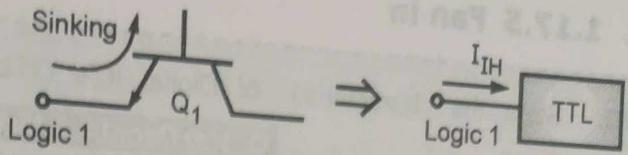


Fig. 1.17.2(a) : Input current in LOW state



(b) Input current in HIGH state

Fig. 1.17.2 : Input currents of TTL

1.17.4 Voltage Specifications

UQ. Define the term and mention its standard value for TTL logic family : Voltage parameter.

Q. 6(b), May 19, 1 Mark

Voltages at input and output are different for HIGH and LOW states.

(A) Input voltages

Input voltage range which TTL input recognises as logic 0 or logic 1 is shown in Fig. 1.17.3(a). Typical ratings are

$$V_{IL}(\text{max}) = 0.8 \text{ V}$$

$$V_{IH}(\text{min}) = 2 \text{ V}$$

(B) Output voltages

The range of voltage which represents logic 0 or logic 1 at the output is shown in Fig. 1.17.3(b). Typical values are :

$$V_{OL}(\text{max}) = 0.4 \text{ V}$$

$$V_{OH}(\text{min}) = 2.4 \text{ V}$$

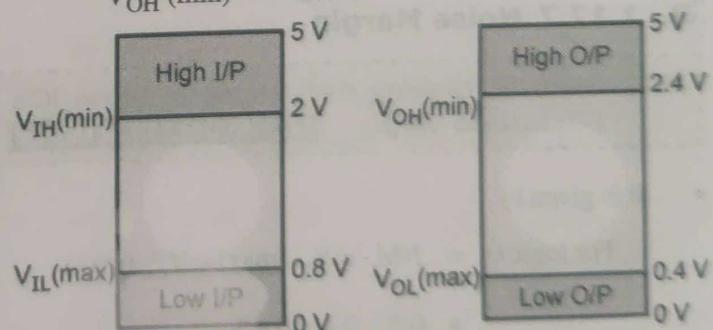


Fig. 1.17.3 : Showing voltage specifications

1.17.5 Fan in

UQ. State the characteristic of Digital IC's (TTL) : Fan in **Q. 1(a) Dec. 14, 4 Marks**

It is equal to number of inputs of a TTL gate.



Fan in	1	2	3
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Fig. 1.17.4

1.17.6 Fan out

UQ. State the characteristic of Digital IC's (TTL) : Fan out. **Q. 1(a) Dec. 14, 4 Marks**

UQ. Define the term and mention the standard values for TTL logic family : Fan out. **Q. 5(b), Dec. 17, 2 Marks**

Fan out in LOW and HIGH states are obtained as

$$\text{fanout}_L = \text{fanout in LOW state} = \frac{I_{OL}}{I_{IL}} = \frac{16 \text{ mA}}{1.6 \text{ mA}} = 10$$

$$\text{fanout}_H = \text{fanout in HIGH state} = \frac{I_{OH}}{I_{IH}} = \frac{400 \mu\text{A}}{40 \mu\text{A}} = 10$$

$$\text{fanout} = \min(\text{fanout}_L, \text{fanout}_H) = 10$$

1.17.7 Noise Margin

UQ. State the following characteristic of Digital IC's (TTL) : Noise Margin **Q. 1(a) Dec. 14, 4 Marks**

- It is given by,

$$\begin{aligned} \text{For logic 0} &= NM_L = V_{IL}(\text{max}) - V_{OL}(\text{max}) \\ &= 0.8 - 0.4 = 0.4 \text{ V} \end{aligned}$$

$$\begin{aligned} \text{For logic 1} &= NM_H = V_{OH}(\text{min}) - V_{IH}(\text{min}) \\ &= 2.4 - 2 = 0.4 \text{ V} \end{aligned}$$

$$NM = \min(NM_L, NM_H) = 0.4 \text{ V}$$

1.17.8 Power Dissipation

UQ. Mention the standard values for TTL logic family : Power Dissipation. **Q. 5(b), Dec. 17, 1 Marks**

Its typical value is

$$P_D = 40 \text{ mW}$$

1.17.9 Temperature Range

For 74 series : 0 to 70°C

For 54 series : -55°C to 125°C

Note that the values specified above are different for different TTL subfamilies. Above values are valid for 74 series TTL family.

1.18 CMOS CHARACTERISTICS

1.18.1 Supply Voltage

- Unlike TTL logic, CMOS requires two supply voltages, V_{DD} and V_{SS} . The values of V_{DD} for two subfamilies are given below, and the supply V_{SS} is normally grounded.

For 4000 B : +3 V to +15 V

For 74 HC; 74 HCT : +2 V to +6 V

1.18.2 Threshold Voltage

The logic levels in CMOS are nearly V_{DD} (for logic 1) and 0 V (for logic 0). Then threshold voltage is

$$V_{TH} = \frac{V_{DD} + 0}{2} = \frac{V_{DD}}{2} \text{ (Volts)}$$

1.18.3 Current Specifications

(A) Output Currents

In both high and low state output, the currents are equal.

$$I_{OH} = -40 \mu\text{A} \text{ (out)}$$

$$I_{OL} = 40 \mu\text{A} \text{ (in)}$$

(B) Input currents

For both high and low inputs, the input currents are equal.

$$I_{IH} = 1 \mu\text{A} \text{ (in)}$$

Table 9.9.3 : Important parameters of TTL logic family

Sr. No.	Parameter	Values
1.	Supply voltage	74 series : (4.75 to 5.25 V) 54 series : (4.5 to 5.5 V)
2.	Temperature range	74 series : 0 to 70° C 54 series : - 55 to 125° C
3.	Voltage levels	$V_{IL\ (max)} = 0.8\ V$ $V_{OL\ (max)} = 0.4\ V$ $V_{IH\ (min)} = 2\ V$ $V_{OH\ (min)} = 2.4\ V$
4.	Noise margin	0.4 V
5.	Power dissipation	10 mW
6.	Propagation delay	10 nanosec.

Sr. No.	Parameter	Values
7.	Fan out	10
8.	Figure of merit	100

9.10 Advantages and Disadvantages of TTL :

9.10.1 Advantages of TTL : ✓

1. TTL circuits are fast.
2. Low propagation delay.
3. Power dissipation is not dependent on frequency.
4. Compatible to all the other families.
5. Latch ups do not take place.
6. These are not susceptible to the damage due to static charges.
7. Higher current sourcing and sinking capabilities.

9.10.2 Disadvantages of TTL : ✓

1. Large power dissipation.
2. Fan out is lower than that of CMOS.
3. Less component density.
4. Can operate only on + 5 V power supply.
5. Poor noise immunity.

9.11 MOS - Logic Families

DLF (22) PMOS as a switch

For PMOS it is exactly opposite to NMOS.

The PMOS device is ON when low voltage is applied at input (G) and it behaves like switch is closed.

The PMOS device is OFF when high voltage is applied at input (G) and it behaves like switch is open. It is shown in Fig. 1.11.4.

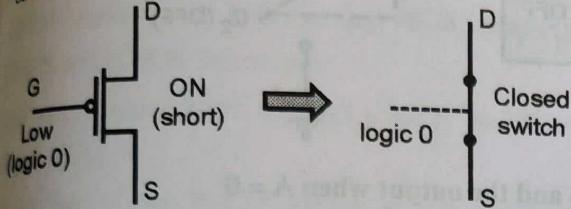


Fig. 1.11.4(a) : PMOS device as a closed switch

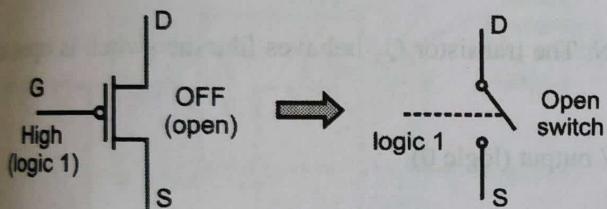


Fig. 1.11.4(b) : PMOS device as a open switch

For PMOS	
Input	State
logic 0	closed switch
logic 1	open switch

1.12 CMOS INVERTER

UQ. Draw and explain operation of two input CMOS inverter.

Q. 4(b) May 18, 6 Marks, Q. 5(a), Dec. 17, 5 Marks

UQ. Explain with neat diagram working of CMOS inverter. OR Implement CMOS inverter.

Q. 3(b), Dec. 18, Q. 1(c), Dec. 19, 3 Marks,

Q. 7(a), May 17, 4 Marks

(1) **CMOS stands for complementary MOS**, it uses both PMOS and NMOS transistors.

- (2) CMOS inverter circuit uses both PMOS (Q_1) and NMOS (Q_2) transistors connected in series as shown in Fig. 1.12.1.
- (3) The input terminal of the inverter (A) is connected to both the gate terminals (G) of Q_1 and Q_2 .
- (4) The output of the inverter (Y) is connected to both the drain (D) terminals of Q_1 and Q_2 .
- (5) The supply voltage V_{DD} is connected to the source (S) terminal of PMOS (Q_1) transistor, while the source (S) terminal of NMOS (Q_2) is connected to the ground terminal.
- (6) The input A can be a logic low (0) or a logic high (1). For some input when one transistor is ON then the other will be OFF.

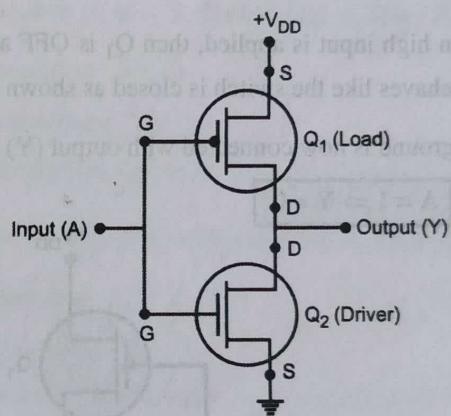


Fig. 1.12.1 : CMOS Inverter

1.12.1 Operation

- (1) Before we explain the operation, remember

Q_1 (PMOS) \rightarrow ON when input LOW

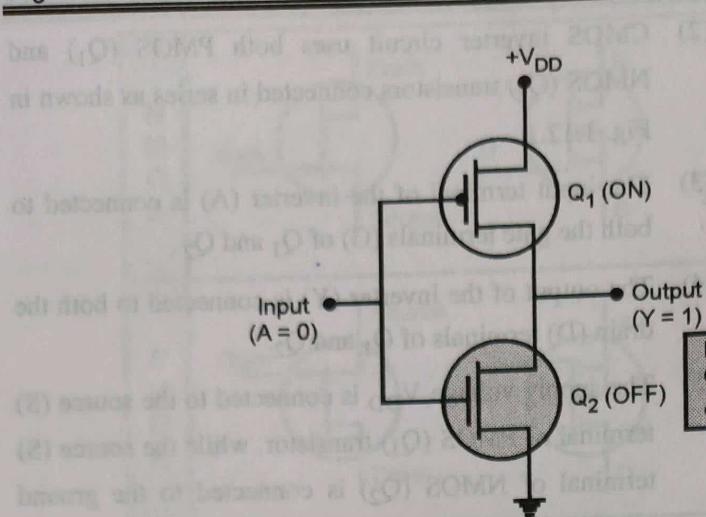
Q_2 (NMOS) \rightarrow ON when input HIGH

CASE (i) $A = 0$

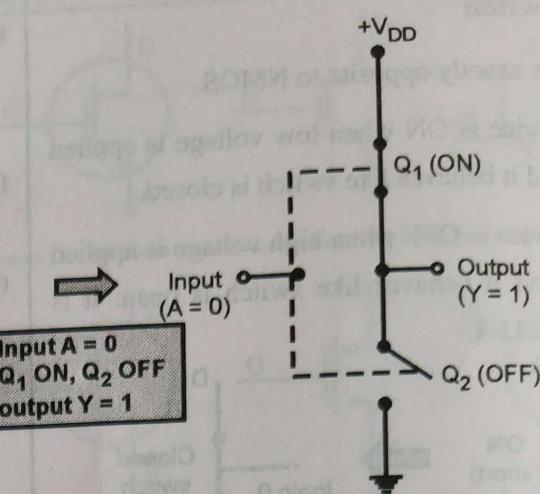
- (1) When low input is applied then Q_1 is ON and Q_2 is OFF. So Q_1 behaves like the switch is closed and Q_2 behaves like the switch is open as shown in Fig. 1.12.2.
- (2) The supply voltage V_{DD} is connected to the output (Y) resulting in HIGH output (logic 1).

$$A = 0 \Rightarrow Y = 1$$





**Input A = 0
Q₁ ON, Q₂ OFF
output Y = 1**

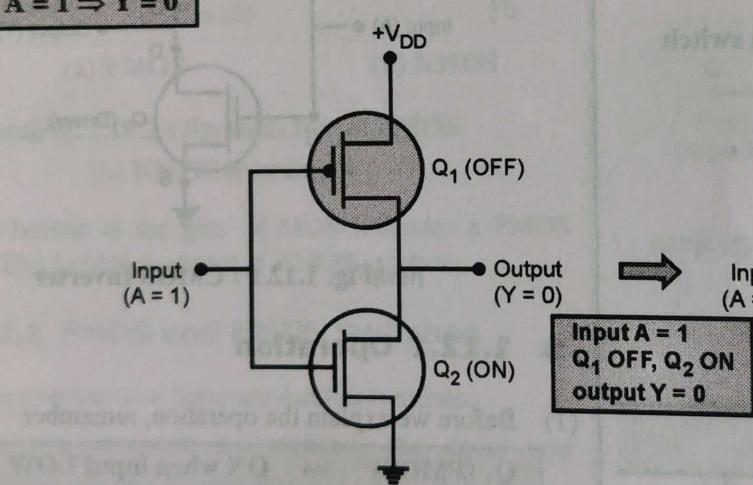


(1B14) Fig. 1.12.2 : showing states of Q₁, Q₂ and the output when A = 0

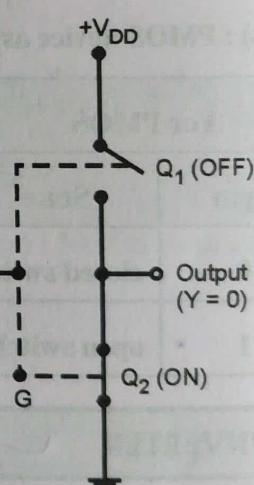
CASE (ii) : A = 1

- When high input is applied, then Q₁ is OFF and Q₂ will be ON. The transistor Q₁ behaves like the switch is open and Q₂ behaves like the switch is closed as shown in Fig. 1.12.3.
- The ground is now connected with output (Y) resulting in LOW output (logic 0).

A = 1 \Rightarrow Y = 0



**Input A = 1
Q₁ OFF, Q₂ ON
output Y = 0**



(1B15) Fig. 1.12.3 : Showing states of Q₁, Q₂ and the output when A = 1

- The input combinations and the corresponding output are written in truth table form as shown.

Input A	Q ₁	Q ₂	Output Y
0	ON	OFF	1
1	OFF	ON	0

This is the truth table of an inverter. This is how CMOS circuit in Fig. 1.12.1 behaves like an inverter.

1.13 CMOS NAND GATE

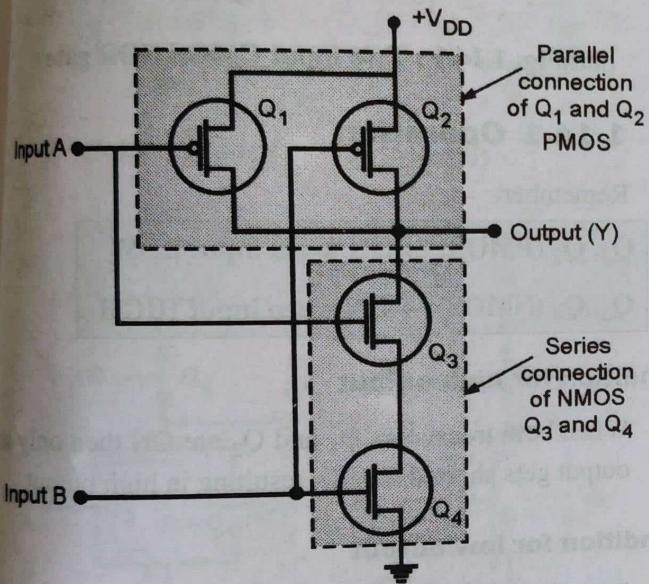
- Q. Draw and explain the working of 2-input CMOS NAND gate. [Q. 1(a), Dec. 13, Q. 2(a), Dec. 15, Q. 4(a), May 17, Q. 3(a), Dec. 17, 6 Marks]

- Q. Explain with neat diagram two input CMOS NAND gate. [Q. 2(b), Dec. 14, Q. 2(b), May 14, 6 Marks]

CMOS stands for complementary MOS, it uses both PMOS and NMOS transistors.

The two input CMOS NAND gate is as shown in Fig. 1.13.1.

It consists of two PMOS transistors (Q_1 and Q_2) and two NMOS transistors (Q_3 and Q_4).



(1B25)Fig. 1.13.1 : Two input CMOS NAND gate

- 3) Two PMOS transistors (Q_1 and Q_2) are connected in parallel, while two NMOS transistors (Q_3 and Q_4) are connected in series.
- 4) The common end of the parallel series connection is connected at the output (Y).
- 5) Input A is applied to Q_1 and Q_3 , while input B is applied to Q_2 and Q_4 .

1.13.1 Operation

Remember

Q_1, Q_2 (PMOS) \rightarrow ON when input LOW
 Q_3, Q_4 (NMOS) \rightarrow ON when input HIGH

Condition For high output

When any of the transistors Q_1 and Q_2 or both are ON, then the output gets shorted to V_{DD} resulting in high output.

Condition for low output

When both transistors Q_3 and Q_4 are ON then only the output gets shorted to ground resulting in low output.

Now let us check the operation of circuit using different input conditions.

CASE (i) $A = 0, B = 0$ (Refer Fig. 1.13.2(a))

ON transistors : Q_1, Q_2

OFF transistors : Q_3, Q_4

The output gets shorted to V_{DD} resulting in $Y = 1$.

CASE (ii) : $A = 0, B = 1$ (Refer Fig. 1.13.2(b))

ON transistors : Q_1, Q_4

OFF transistors : Q_2, Q_3

The output gets shorted to V_{DD} resulting in $Y = 1$.

CASE (iii) : $A = 1, B = 0$ (Refer Fig. 1.13.2(c))

ON transistors : Q_2, Q_3

OFF transistors : Q_1, Q_4

The output gets shorted to V_{DD} resulting in $Y = 1$.

CASE (iv) : $A = 1, B = 1$ (Refer Fig. 1.13.2(d))

ON transistors : Q_3, Q_4

OFF transistors : Q_1, Q_2

The output gets shorted to ground resulting in $Y = 0$.

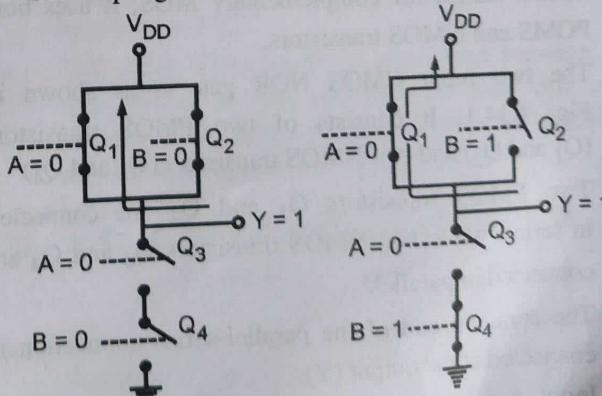


Fig. 1.13.2 (Contd...)



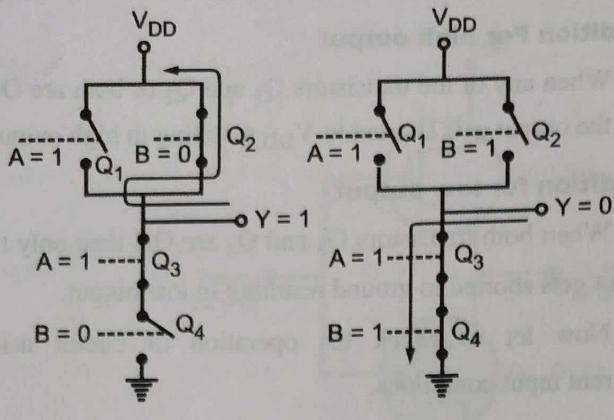


Fig. 1.13.2(a, b, c, d) : Showing different input conditions

- (1) All these input conditions and the corresponding outputs are shown in the truth table.

Inputs		Transistor				Output Y
A	B	Q ₁	Q ₂	Q ₃	Q ₄	
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

This is the truth table of a NAND gate.

► 1.14 CMOS NOR GATE

UQ. Draw CMOS circuit for NOR gate.

Q. 2(a), May 14, 2 Marks, Q. 1(c), Dec. 19, 2.5 Marks,

May 14, Q. 6(c), 4 Marks, Q. 5(a), Dec. 16, 2 Marks

UQ. Draw and explain the working of 2 input CMOS NOR gate.

Q. 2(a), Dec. 14, 6 Marks, Q. 3(b), May 13, 8 Marks

- (1) CMOS stands for complementary MOS, it uses both PMOS and NMOS transistors.
- (2) The two input CMOS NOR gate is as shown in Fig. 1.14.1. It consists of two PMOS transistors (Q_1 and Q_2) and two NMOS transistors (Q_3 and Q_4)
- (3) Two PMOS transistors Q_1 and Q_2 are connected in series, while two NMOS transistors Q_3 and Q_4 are connected in parallel.
- (4) The common end of the parallel-series connection is connected at the output (Y).
- (5) Input A is applied to Q_1 and Q_3 , while input B is applied to Q_2 and Q_4 .

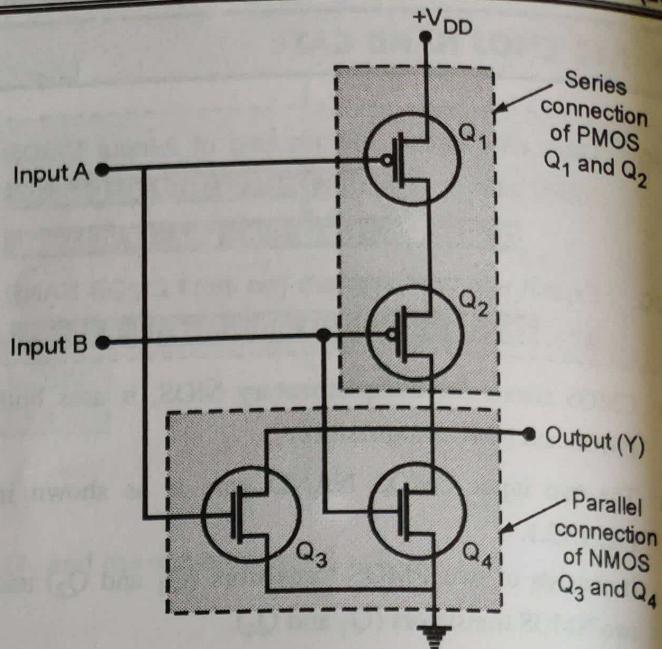


Fig. 1.14.1 : Two input CMOS NOR gate

1.14.1 Operation

- Remember

Q_1, Q_2 (PMOS) → ON when input LOW

Q_3, Q_4 (NMOS) → ON when input HIGH

Condition for high output

- When both transistors Q_1 and Q_2 are ON then only the output gets shorted to V_{DD} resulting in high output

Condition for low output

- When any of the transistors Q_3 and Q_4 or both are ON, then the output gets shorted to ground resulting in low output.

CASE (i) $A = 0, B = 0$ (Refer Fig. 1.14.2(a))

ON transistors : Q_1, Q_2

OFF transistors : Q_3, Q_4

The output gets shorted to V_{DD} resulting in $Y = 1$

CASE (ii) : $A = 0, B = 1$ (Refer Fig. 1.14.2(b))

ON transistors : Q_1, Q_4

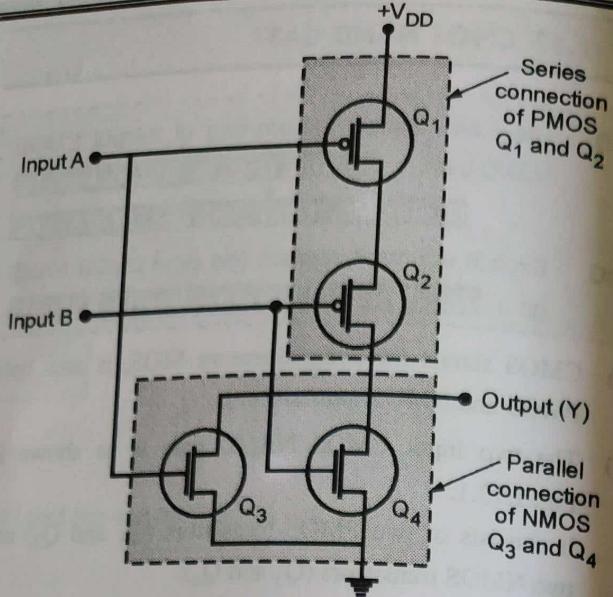
OFF transistors : Q_2, Q_3

The output gets shorted to ground resulting in $Y = 0$

CASE (iii) : $A = 1, B = 0$ (Refer Fig. 1.14.2(c))

ON transistors : Q_2, Q_3





(1B28)Fig. 1.14.1 : Two input CMOS NOR gate

1.14.1 Operation

- Remember

Q₁, Q₂ (PMOS) → ON when input LOW

Q₃, Q₄ (NMOS) → ON when input HIGH

Condition for high output

- When both transistors Q₁ and Q₂ are ON then only the output gets shorted to V_{DD} resulting in high output

Condition for low output

- When any of the transistors Q₃ and Q₄ or both are ON, then the output gets shorted to ground resulting in low output.

CASE (i) A = 0, B = 0 (Refer Fig. 1.14.2(a))

ON transistors : Q₁, Q₂

OFF transistors : Q₃, Q₄

The output gets shorted to V_{DD} resulting in Y = 1

CASE (ii) : A = 0, B = 1 (Refer Fig. 1.14.2(b))

ON transistors : Q₁, Q₄

OFF transistors : Q₂, Q₃

The output gets shorted to ground resulting in Y = 0

CASE (iii) : A = 1, B = 0 (Refer Fig. 1.14.2(c))

ON transistors : Q₂, Q₃

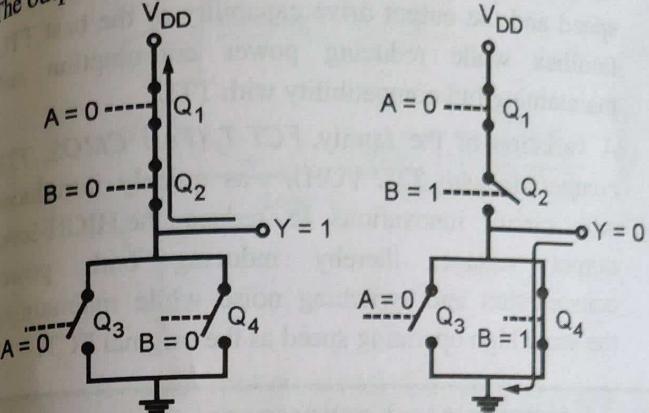
Digital Ele
OFF transistors : Q₁, Q₄

The output gets shorted to ground resulting in Y = 0
CASE (iv) A = 1, B = 1 (Refer Fig. 1.14.2(d))

ON transistors : Q₃, Q₄

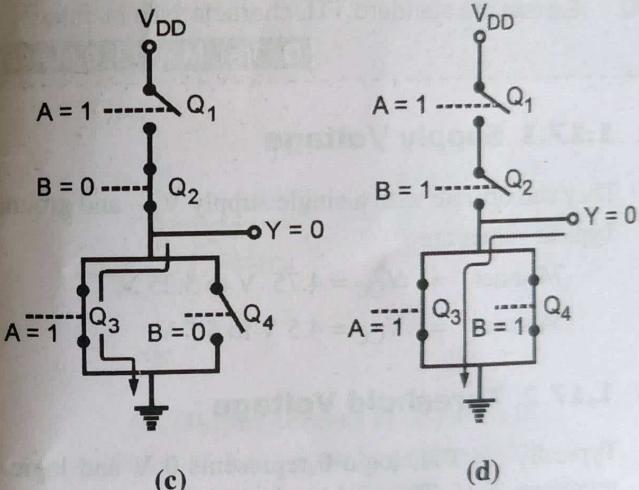
OFF transistors : Q₁, Q₂

The output gets shorted to ground resulting in Y = 0.



(1B29)(a)

(1B29)(b)



(c)

(d)

(1B30)Fig. 1.14.2(a, b, c, d) : Showing different input conditions

- All these input conditions and the corresponding outputs are shown in the truth table

Inputs		Transistor				Output
A	B	Q ₁	Q ₂	Q ₃	Q ₄	Y
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

This is the truth table of a NOR gate.



► 1.18 CMOS CHARACTERISTICS

➤ 1.18.1 Supply Voltage

- Unlike TTL logic, CMOS requires two supply voltages, V_{DD} and V_{SS} . The values of V_{DD} for two subfamilies are given below, and the supply V_{SS} is normally grounded.

For 4000 B : + 3 V to + 15 V

For 74 HC; 74 HCT : + 2 V to + 6 V

➤ 1.18.2 Threshold Voltage

The logic levels in CMOS are nearly V_{DD} (for logic 1) and 0 V (for logic 0). Then threshold voltage is

$$V_{TH} = \frac{V_{DD} + 0}{2} = \frac{V_{DD}}{2} \text{ (Volts)}$$

➤ 1.18.3 Current Specifications

(A) Output Currents

In both high and low state output, the currents are equal.

$$I_{OH} = -40 \mu A \text{ (out)}$$

$$I_{OL} = 40 \mu A \text{ (in)}$$

(B) Input currents

For both high and low inputs, the input currents are equal.

$$I_{IH} = 1 \mu A \text{ (in)}$$

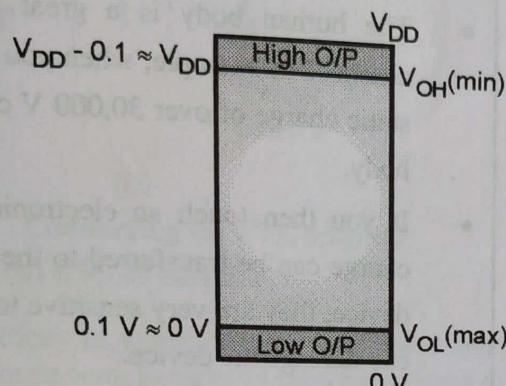
$$I_{IL} = -1 \mu A \text{ (out)}$$

1.18.4 Voltage Specifications

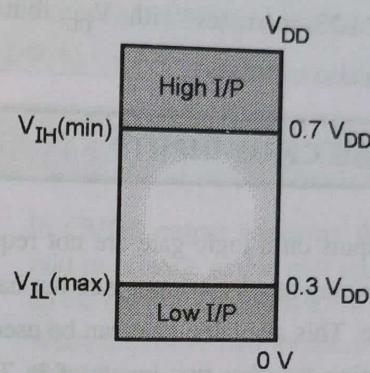
(a) Output voltages

LOW output voltage is very close to 0 V, thus
 $V_{OL}(\max) = 0 \text{ V}$ (typically 0.1 V)

HIGH output voltage is very close to V_{DD} , thus
 $V_{OH}(\min) = V_{DD}$ (typically $V_{DD} - 0.1$)



(a)



(b)

Fig. 1.18.1 : Output and input voltage profiles

1.18.5 Noise Margin

- In high and low states, the noise margin is calculated as,

$$\begin{aligned} NM_H &= V_{OH}(\min) - V_{IH}(\min) \\ &= V_{DD} - 0.7 V_{DD} = 0.3 V_{DD} \\ NM_L &= V_{IL}(\max) - V_{OL}(\max) \\ &= 0.3 V_{DD} - 0 = 0.3 V_{DD} \\ NM &= \min(NM_L, NM_H) = 0.3 V_{DD} \end{aligned}$$

1.18.6 Fan In

Fan in = number of inputs of CMOS gate

1.18.7 Fan Out

- In high and low states, it is given by

$$\text{Fanout}_L = \frac{I_{OL}}{I_{IL}} = \frac{40 \mu A}{1 \mu A} = 40$$

$$\text{Fanout}_H = \frac{I_{OH}}{I_{IH}} = \frac{40 \mu A}{1 \mu A} = 40$$

(B) Input voltages

- Input voltage levels are expressed as a percentage of V_{DD} value.

$$V_{IL}(\max) = 30\% \text{ of } V_{DD} = 0.3 V_{DD}$$

$$V_{IH}(\min) = 70\% \text{ of } V_{DD} = 0.7 V_{DD}$$
- The input and output voltage profiles are shown in Fig. 1.18.1.

$$\text{Fanout} = \min(\text{Fanout}_L, \text{Fanout}_H) = 40$$

- This large value of fanout is obtained at frequency less than 1 MHz. The fanout decreases when the frequency is increased.

1.18.8 Power Dissipation

- In static case, that is when the output is not changing, the power dissipation is extremely small, typically

$$P_D(\text{static}) = 2.5 \text{ nW when } V_{DD} = 5 \text{ V}$$

- But it increases with the operating frequency and the supply voltage.

$$P_D(\text{Static}) = 10 \text{ nW when } V_{DD} = 10 \text{ V}$$

- With $V_{DD} = 10 \text{ V}$
 - at $f = 100 \text{ KHz} : P_D = 0.1 \text{ mW/gate}$
 - at $f = 1 \text{ MHz} : P_D = 1 \text{ mW/gate}$



☞ 1.18.9 Switching Speed

UQ. State the characteristic of CMOS ICs : Speed of operation

Q. 6(a), Dec. 16, 3 Marks, Q. 1(a)(i), Dec. 15, 2 Marks

- It is represented by the propagation delay t_{pd} . It increases with increase in V_{DD} . Typically

$$t_{pd} = 50 \text{ nS at } V_{DD} = 5 \text{ V}$$

$$\text{and } t_{pd} = 25 \text{ nS at } V_{DD} = 10 \text{ V}$$

- So, speed of CMOS increases with V_{DD} , but then power dissipation also increases.

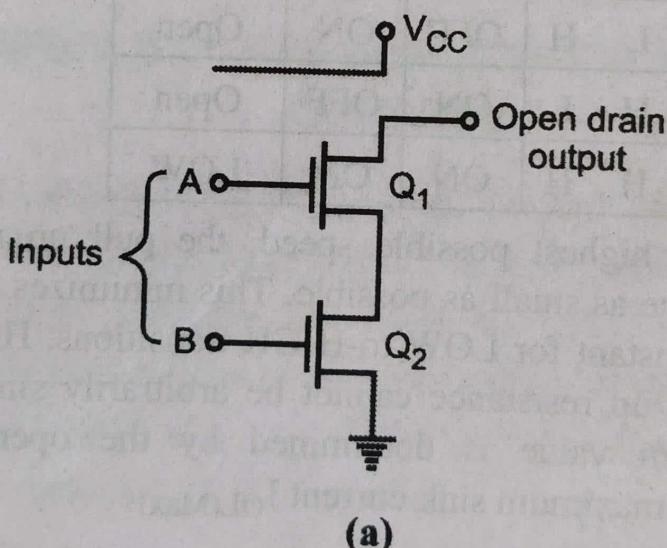
► 1.19 FLOATING CMOS INPUTS

- Sometimes all inputs on a logic gate are not required. For example, you may require n-input gate but have an $(n + 1)$ input gate. This available gate can be used as n input gate by

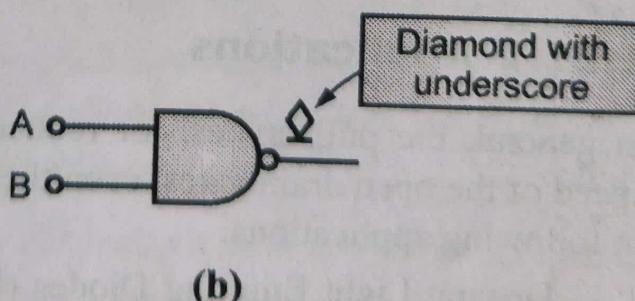
Conventional CMOS outputs should never be tied together.

► 1.21 OPEN DRAIN OUTPUTS

- In CMOS output structure, the PMOS transistors are said to provide active pull up, since they actively pull up the output voltage on a low to HIGH transition.
- When the active pull up transistor is removed from the CMOS circuit, it results in **open drain output**.
- It is similar to removing active pull up transistor from totem pole output stage of TTL circuit.
- In open drain circuit, the output is taken at the drain of the N channel pull down MOSFET, which is an open circuit (i.e. not connected to any other circuitry). It is shown in Fig. 1.21.1(a). In the figure two PMOS transistors connected to V_{cc} are removed to form open drain CMOS NAND gate.



(a)



(b)

Fig. 1.21.1(a) : Open drain CMOS NAND gate
(b) Logic symbol

Digital Electronics (B6)

- The underscored diamond in the symbol in Fig. 1.21.1(b) is sometimes used to indicate an open drain output.
- An open drain output requires an external pull up resistor to provide passive pull up to the HIGH level. Fig. 1.21.2 show an open drain CMOS NAND gate, with a pull up resistor, driving a load.

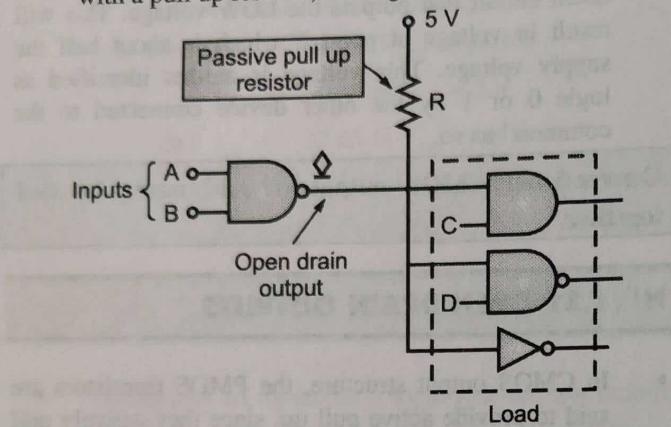


Fig. 1.21.2 : Open drain CMOS NAND with passive pull up resistor

- As the drain of the topmost NMOS transistor is left unconnected internally, then if the output is not LOW it is open. This is shown in functional Table 1.21.1.

Table 1.21.1 : Functional table

A	B	Q_1	Q_2	Output
L	L	OFF	OFF	Open
L	H	OFF	ON	Open
H	L	ON	OFF	Open
H	H	ON	ON	LOW

- For the highest possible speed, the pull up resistor should be as small as possible. This minimizes the RC time constant for LOW-to-HIGH transitions. However the pull up resistance cannot be arbitrarily small, the minimum value is determined by the open drain outputs maximum sink current $I_{OL(\text{Max})}$.

1.21.1 Applications

- In general, the pull up resistor reduces the switching speed of the open drain gates, even then they are useful in following applications.
 - Driving Light Emitting Diodes (LEDs) and other devices.
 - Driving multisource buses, and
 - Performing wired logic.

1.22 WIRED LOGIC

- When the outputs of several open drain gates are tied together with a single pull up resistor, then **wired logic** is performed.
- As shown in Fig. 1.22.1, the open drain gates share a common connection, the common wire is HIGH by default due to the pull up resistor.
- When any one (or more) of the gate outputs pulls it LOW, the 5 V are dropped across R_p and the common connection is in the Low state.
- Since the common output is HIGH only when all the outputs are in the HIGH state, connecting the outputs in this way performs the logic AND function. This is why, it is called as **Wired-AND connection**. This is shown symbolically by the dotted AND gate symbol. There is no actual AND gate there.

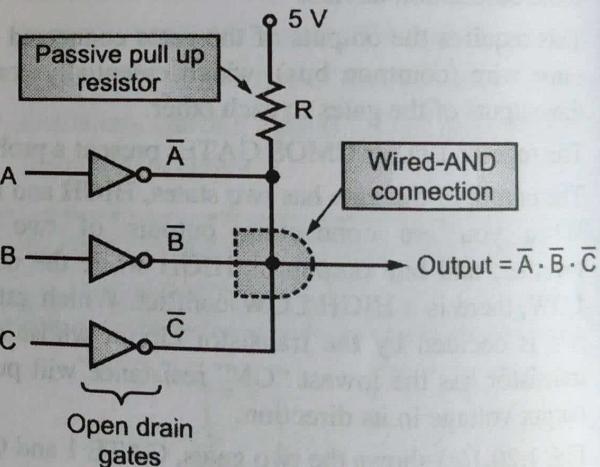


Fig.1.22.1 : Wired AND operation

- Note that, wired logic cannot be performed using gates with active pull up. Two such outputs wired together and trying to maintain opposite logic values result in a very high current flow and an abnormal output voltage. This phenomenon is sometimes called as **fighting**.
- The exact output voltage depends on the relative “strengths” of the fighting transistors, but with a 5 V CMOS devices it is typically about 1-2 V, which is a non logic Voltage (neither 0 or 1).

1.25 COMPARISON OF TTL AND CMOS

- UQ.** Differentiate between standard TTL and CMOS logic circuit with respect to :
1. Propagation delay 2. Fan out
 3. Figure of merit
 5. Noise margin 6. Speed power product
 7. Voltage and current parameters
 4. Power dissipation
- UQ.** Give comparison between TTL, ECL and CMOS logic families. **Q. 1(c), Dec. 13, 6 Marks, Q. 3(b), Dec. 16, 6 Marks**
- UQ.** Compare CMOS and TTL logic family. **Q. 4(a), May 14, 4 Marks, Q. 3(b), May 19, 4 Marks**
- UQ.** Differentiate between standard TTL and CMOS logic circuit with respect to :
1. Propagation delay 2. Fan out 3. Figure of merit.
- 1(c), May 16, 5 Marks, Q. 1(c), Dec. 13, 6 Marks**

Sr. No.	Criteria	TTL	CMOS
1.	Stands for	It stands for transistor transistor logic.	It stands for complementary metal oxide semiconductor .
2.	Consists of	It uses bipolar junction transistors	It uses NMOS and PMOS transistors.
3.	Power supply	$V_{CC} = 5 \text{ V} \pm 10\%$	For 4000 series, $3 \text{ V} \leq V_{DD} \leq 18 \text{ V}$ For HC family, $2 \text{ V} \leq V_{DD} < 6 \text{ V}$
4.	Noise margin	Small, typically 0.4 V	Large, typically 0.3 V_{DD}
5.	Fan out	Less, typically 10	Large, typically 40
6.	Power dissipation	Fixed, 10 mW	Depends on V_{DD} and frequency. P_D (static) = 2.5 nW for $V_{DD} = 5 \text{ V}$ $P_D = 1 \text{ mW/gate at } f = 1 \text{ MHz}, V_{DD} = 10 \text{ V}$
7.	Propagation delay	Small (10 nS)	Large (70 nS)
8.	Figure of merit	100 pJ	0.7 pJ
9.	Basic gate	NAND	NAND, NOR
10.	Packaging density	Less	Very high as the size of CMOS is very small.
11.	Cost	Less expensive but not as economical as CMOS.	More expensive than TTL but are less costly at a system level.
12.	Design	More complex design with BJT and resistors.	Simpler design with NMOS and PMOS transistors.
13.	Interconnection	Cannot drive CMOS directly, requires a pull up resistor.	Can directly drive TTL.