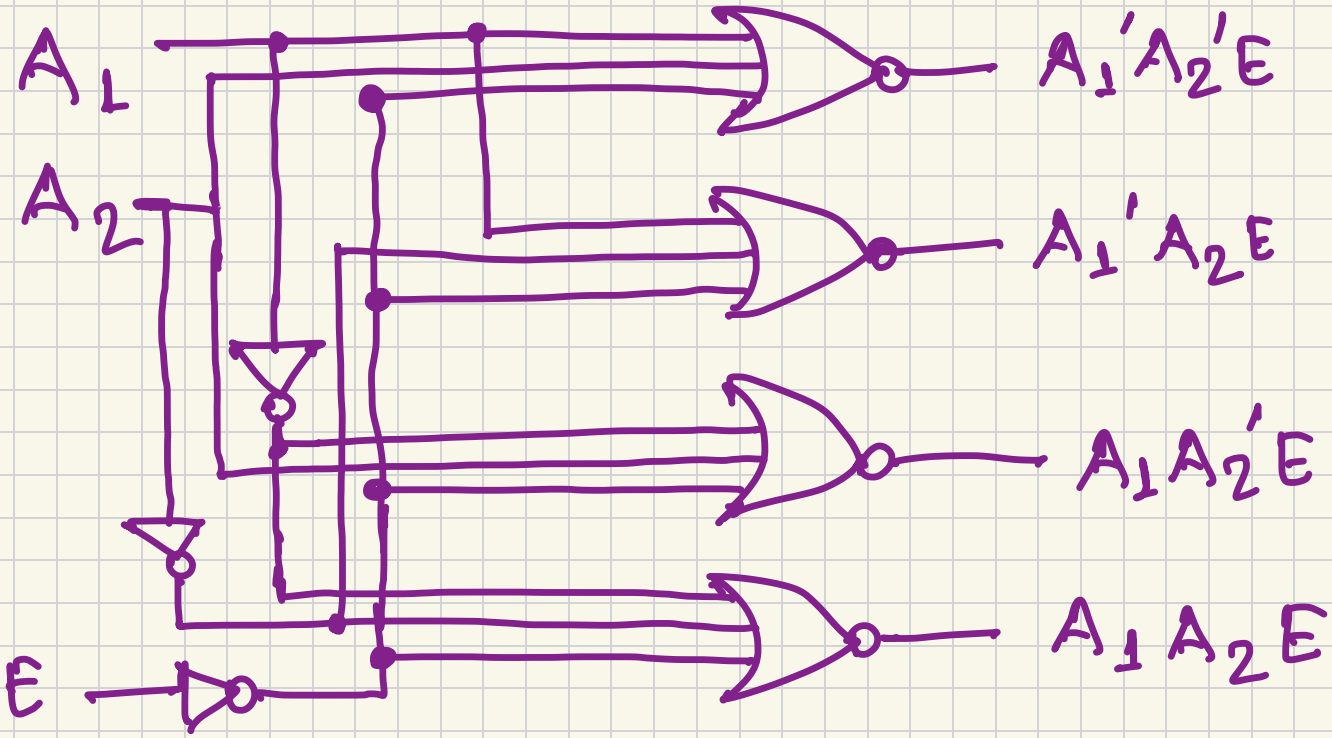
Quiz 3 (Solutions)

1. Clearly, the inputs are the two lines - call them A_1 and A_2. There is also an enable input - let us call it E.

The outputs clearly are $A_1'A_2'E$, $A_1'A_2E$, $A_1A_2'E$, and A_1A_2E.

The logic diagram can be drawn (using NOR and inverter gates) as follows.


A1
A2
E
A1'A2'E
A1'A2E
A1A2'E
A1A2E

2.

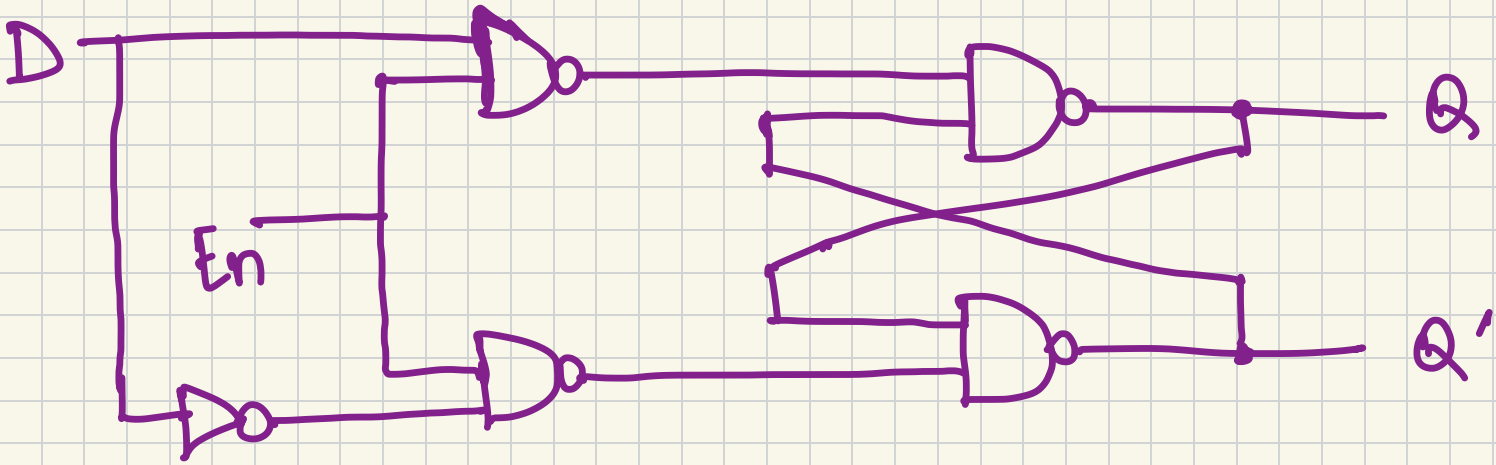
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	a	y	z	v
0	0	0	0	0	0	0	0	X	X	X	0
1	0	0	0	0	0	0	0	0	0	0	1
X	1	0	0	0	0	0	0	0	0	1	1
X	X	1	0	0	0	0	0	0	1	0	1
X	X	X	1	0	0	0	0	0	1	1	1
X	X	X	X	1	0	0	0	1	0	0	1
X	X	X	X	X	1	0	0	1	0	1	1
X	X	X	X	X	X	1	0	1	1	0	1
X	X	X	X	X	X	X	1	1	1	1	1

The row enclosed in a blue rectangle is the one that corresponds to D_3 and D_5 being 1, and everything else being 0.

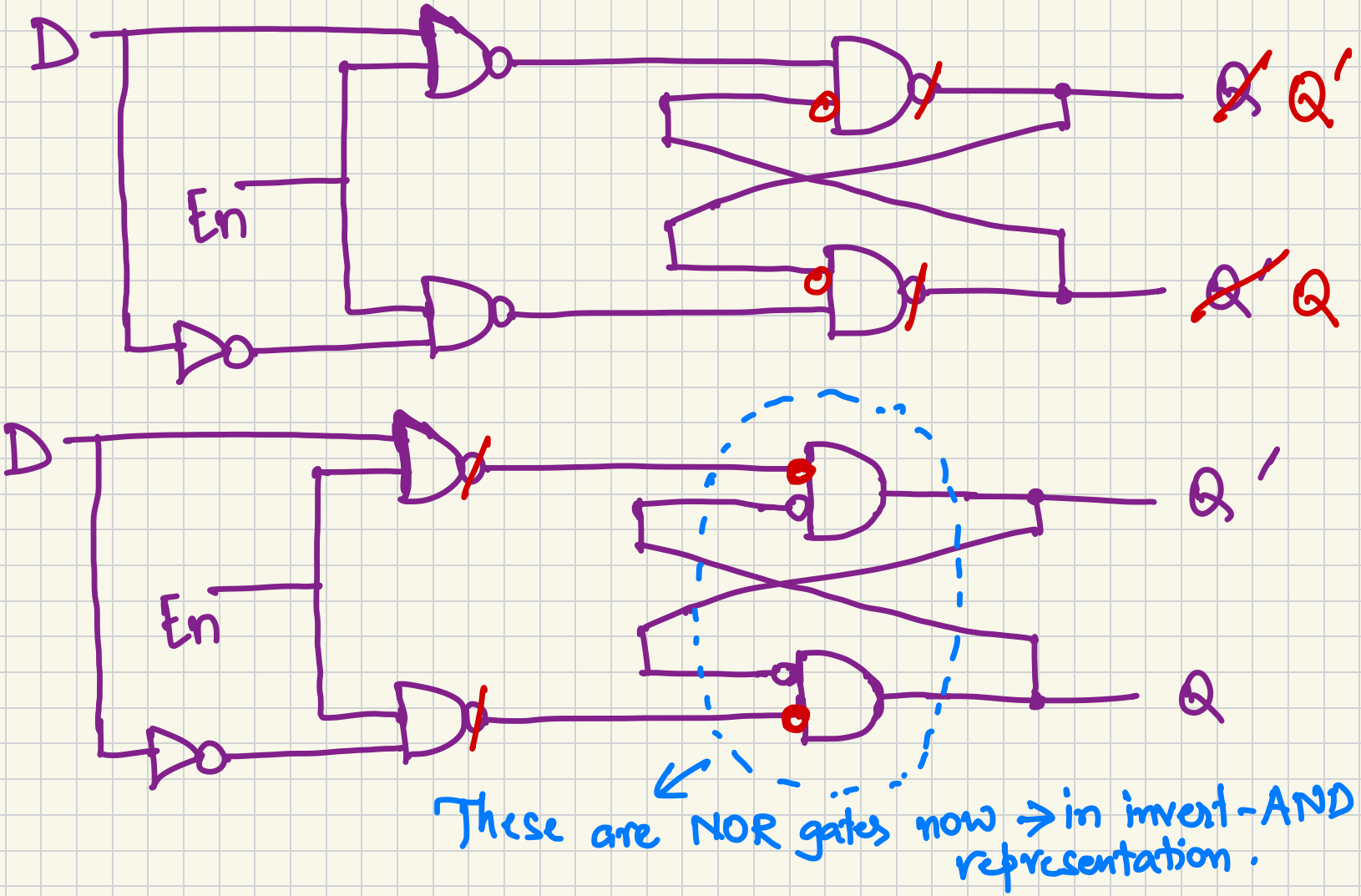
The corresponding output, as clearly seen in the table is

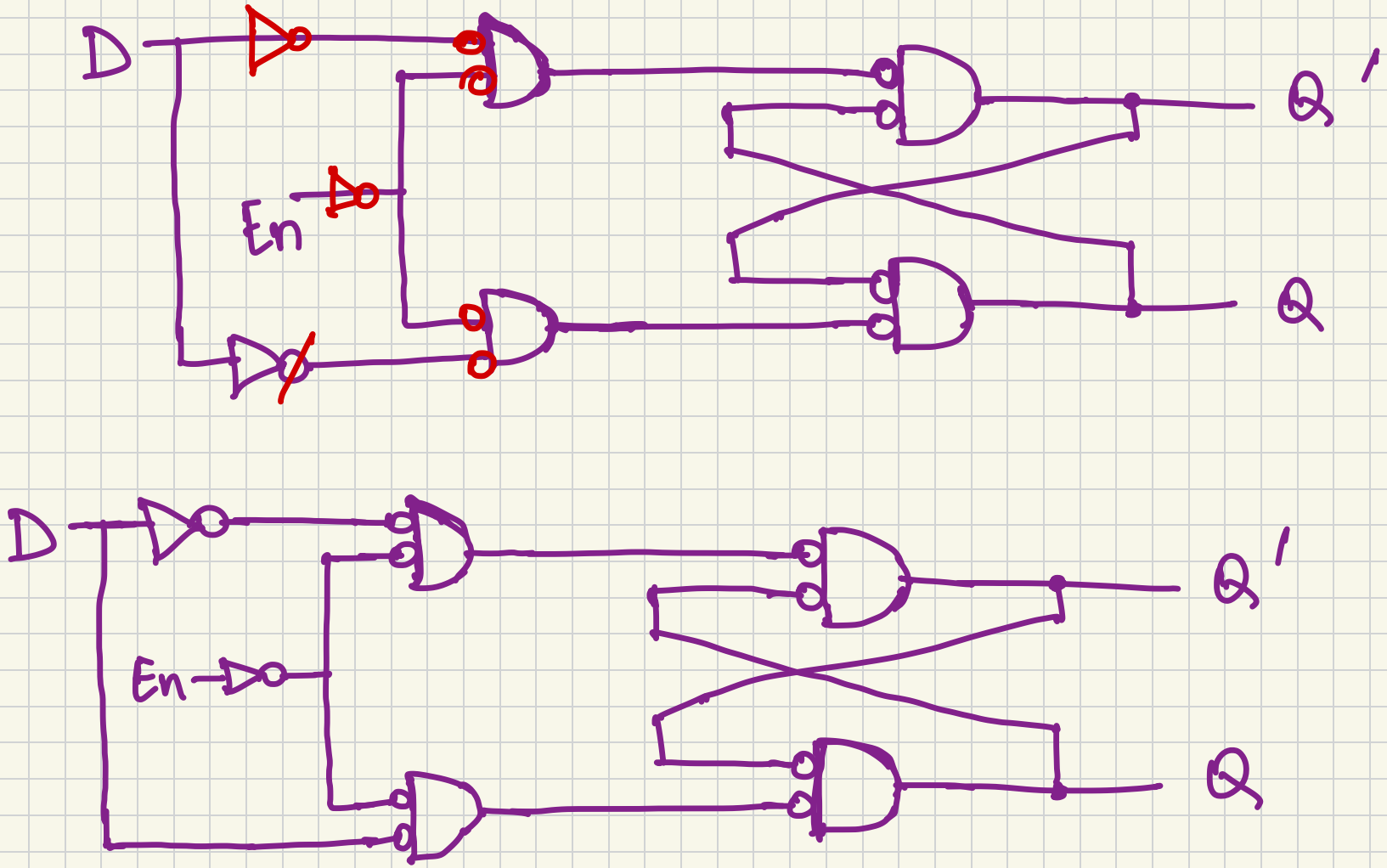
x	y	z	V
1	0	1	1

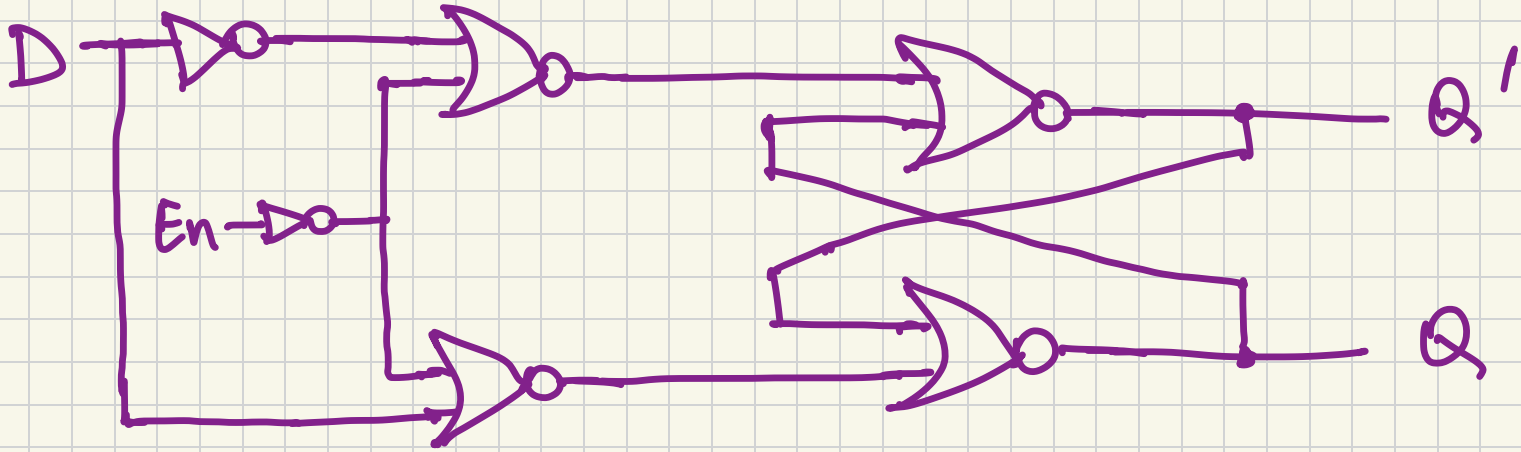
3. Here is the D (transparent) latch using four NAND gates (and an inverter).



Let us try to modify this step-by-step to get the desired form.


D
En
Q'
Q
D
En
Q'
Q
These are NOR gates now → in invert-AND representation.


D
En
Q'
Q
D
En
Q'
Q

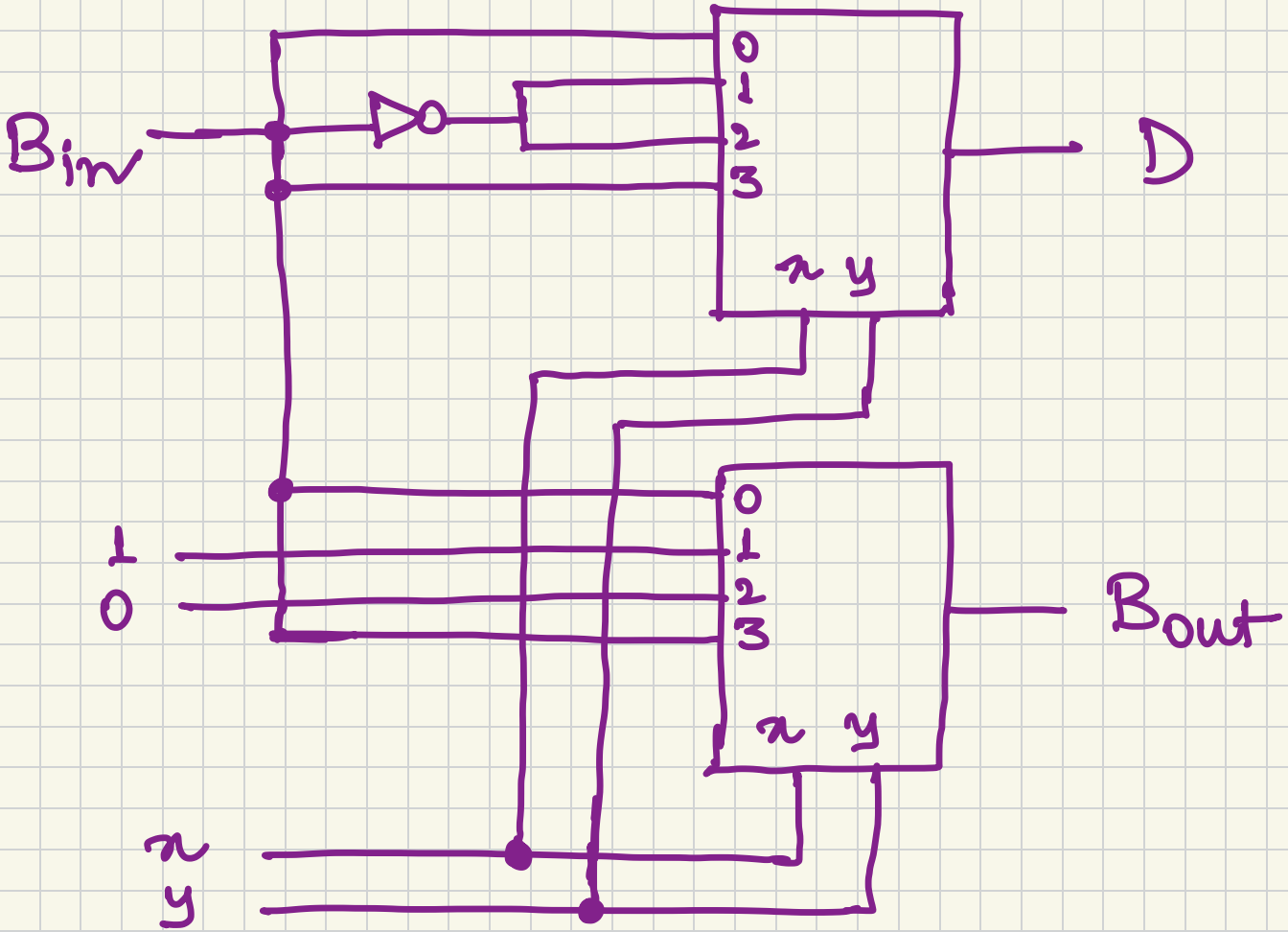


We can verify that this circuit behaves as per the following function table.

En	D	Q(t+1)
0	X	Q(t)
1	0	0
1	1	1

4. Recall, from the mid-term paper, that the truth table of a full subtractor is as follows.

x	y	B_{in}	B_{out}	D	B_{out}	D
0	0	0	0	0	B_{in}	B_{in}
0	0	1	1	1		
0	1	0	1	1	1	B_{in}'
0	1	1	1	0		
1	0	0	0	1	0	B_{in}'
1	0	1	0	0		
1	1	0	0	0	B_{in}	B_{in}
1	1	1	1	1		


B_{in}
0
1
2
3
x y
D
1
0
0
1
2
3
x y
B_{out}
x
y