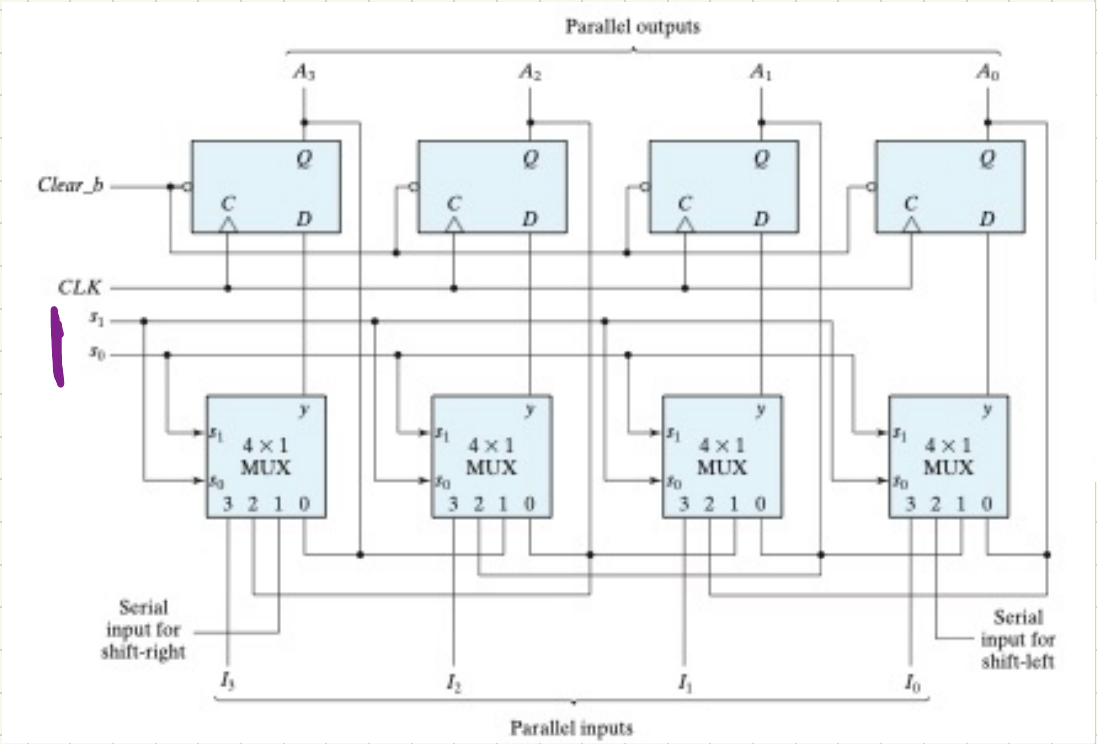
ACOL 215

Universal Shift Register (18th Nov.)



s_1	s_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

4-bit universal shift register

Counters

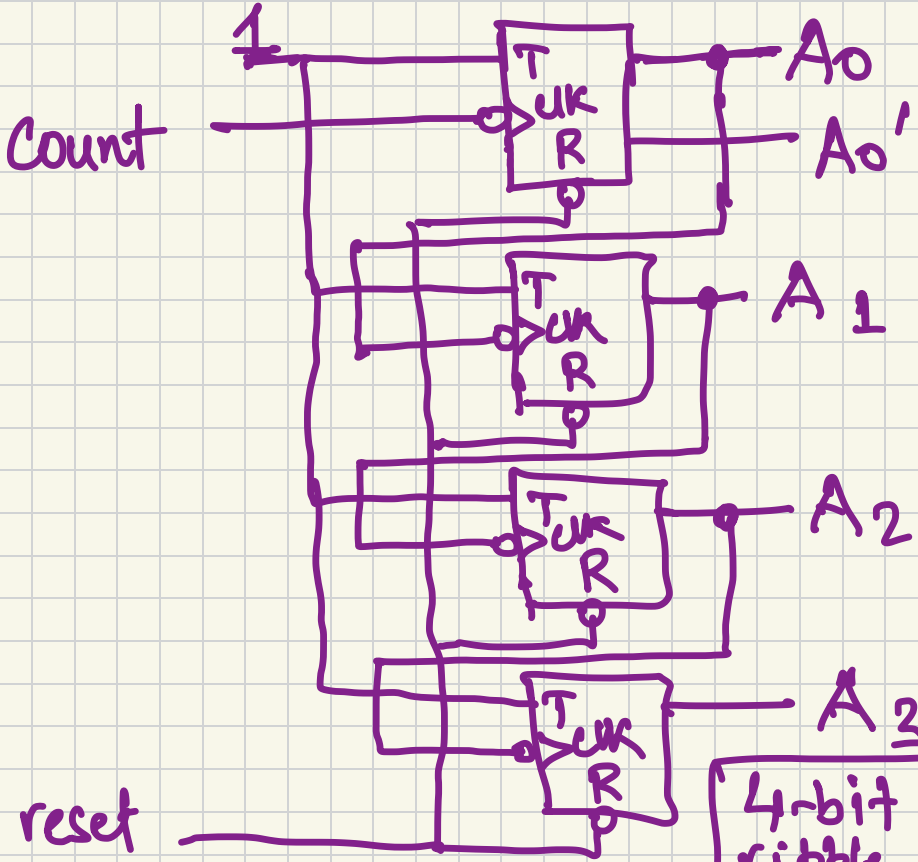
→ ripple counter

a flip-flop output transition serves a source for triggering other flip-flops

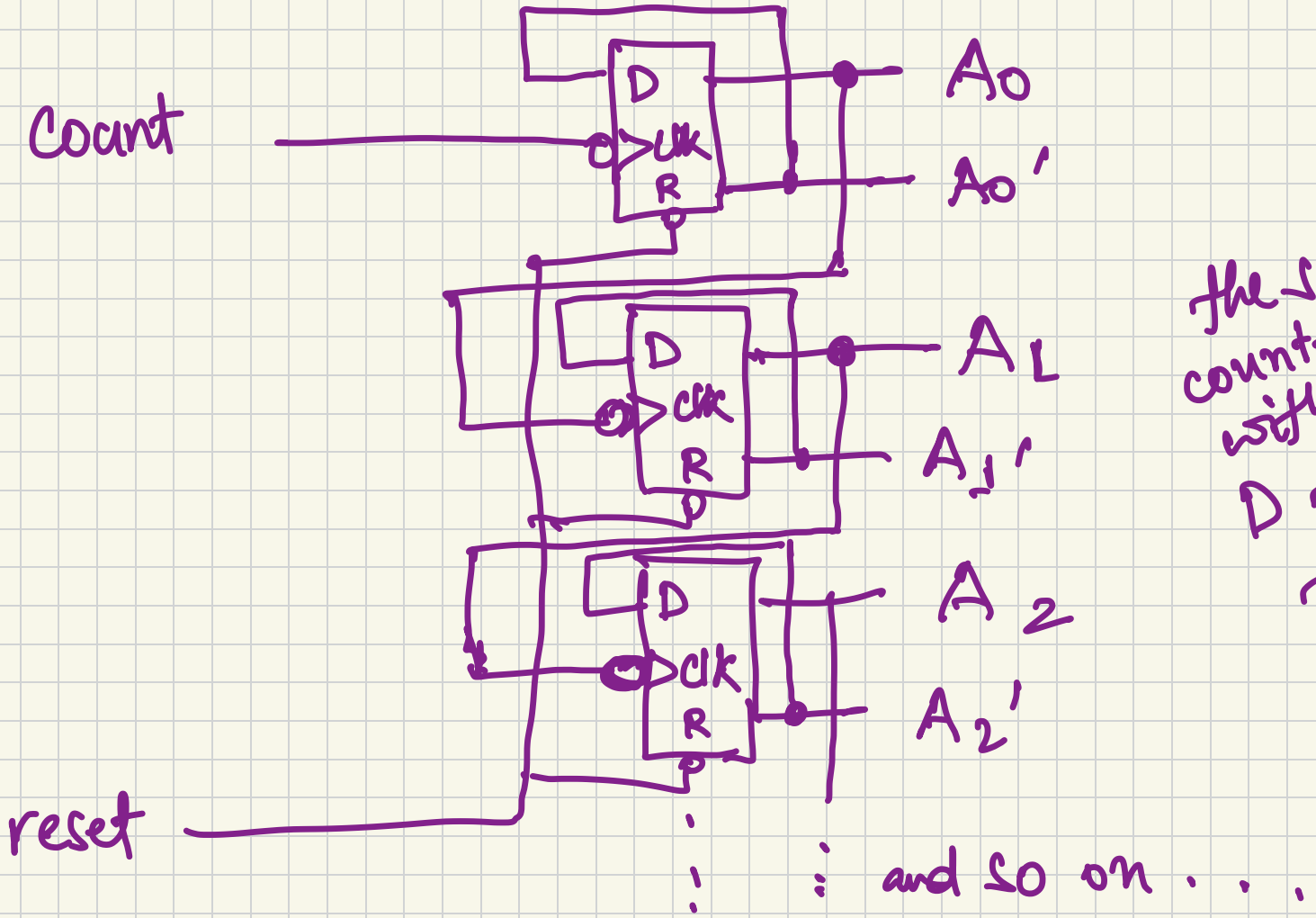
→ synchronous counter

the clock input of all the flip-flops comes from a common clock

Binary Ripple Counter

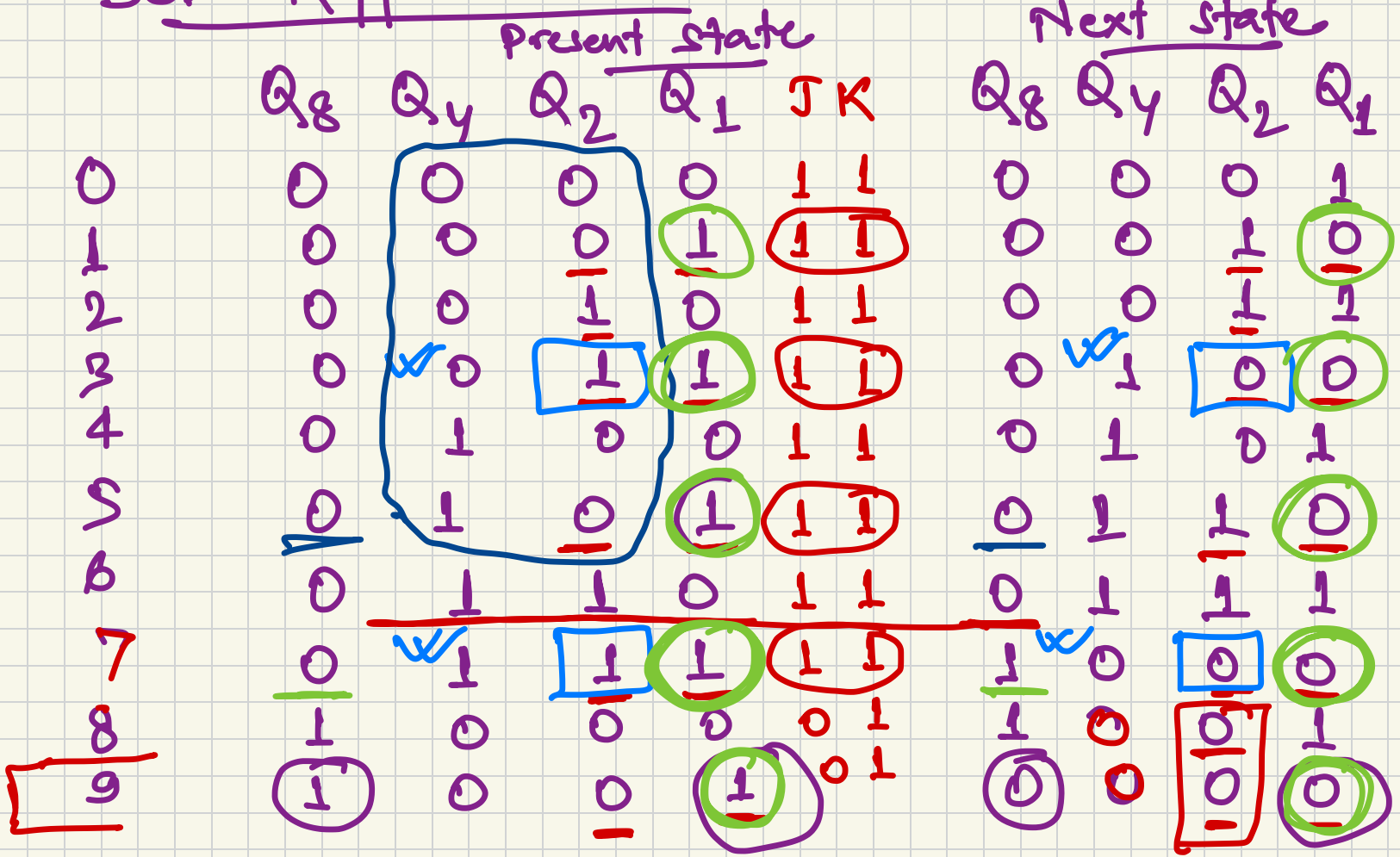


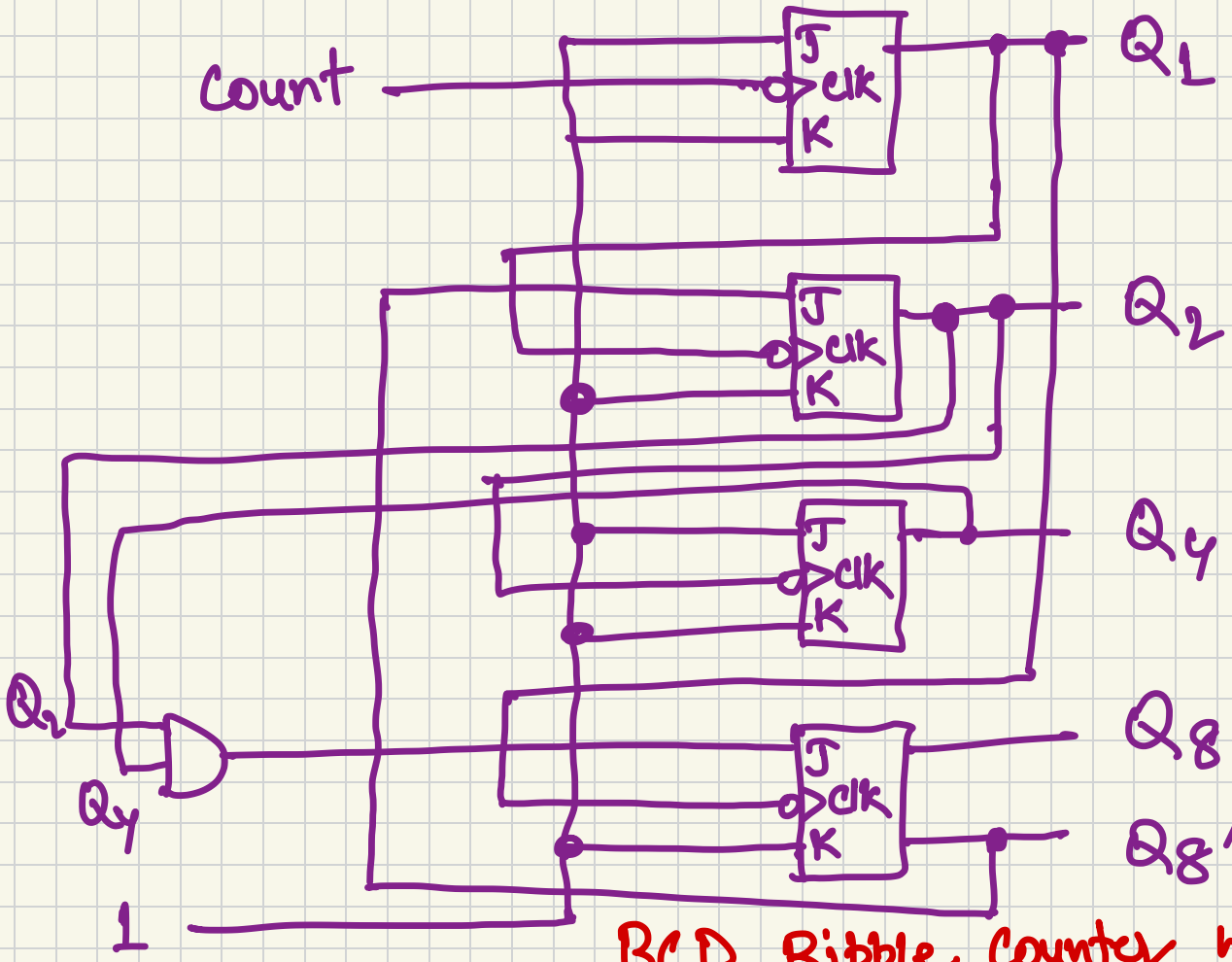
A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0



the same counter with D flip-flops.

BCD Ripple counter





Q_8 remains at 0 as long as either Q_2 or Q_4 is 0.

When Q_2 and Q_4 become 1, Q_8 complements when Q_1 goes from 1 to 0.

BCD Ripple Counter with JK flip-flops