ACOL 215 (06 Oct.)

Binary Addition / Subtraction

Addition of two binary digits

$0 + 0 = 0$

$0 + 1 = 1$

$1 + 0 = 1$

$1 + 1 = 10$ } produces a carry

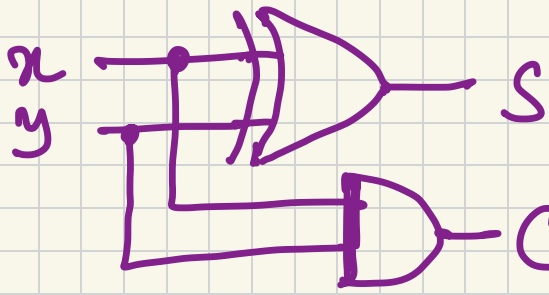
A combinational circuit that performs the addition of two bits is called a half-adder.

And one that performs addition of three bits (two bits and a previous carry) is called a full-adder.

x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$S = x'y + xy' \quad (x \oplus y)$$

$$C = xy$$

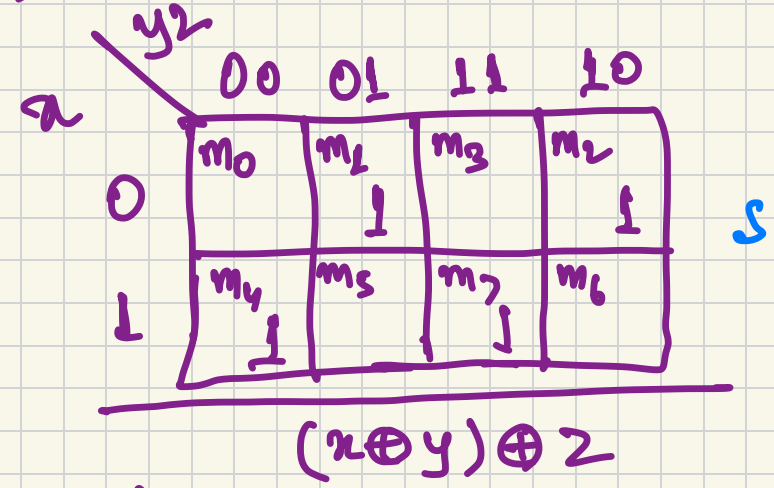


/ half-adder.

What about a full-adder?

(carry)

x	y	z	c	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



$$S = (x \oplus y) \oplus z$$

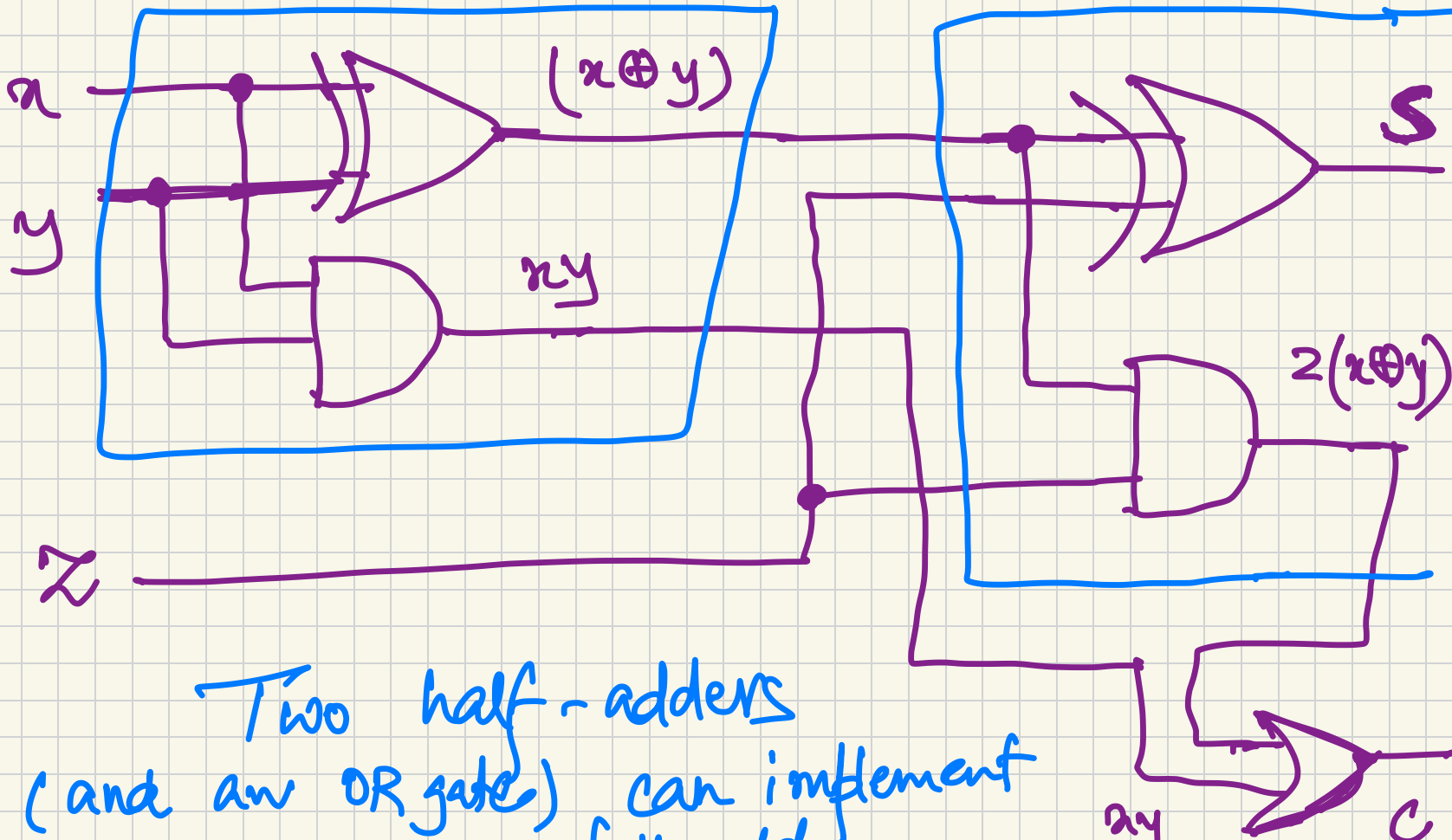
$$C = xy + xz + yz$$

$$= xy + z(x+y)$$

$$= xy + z((x \oplus y) + xy)$$

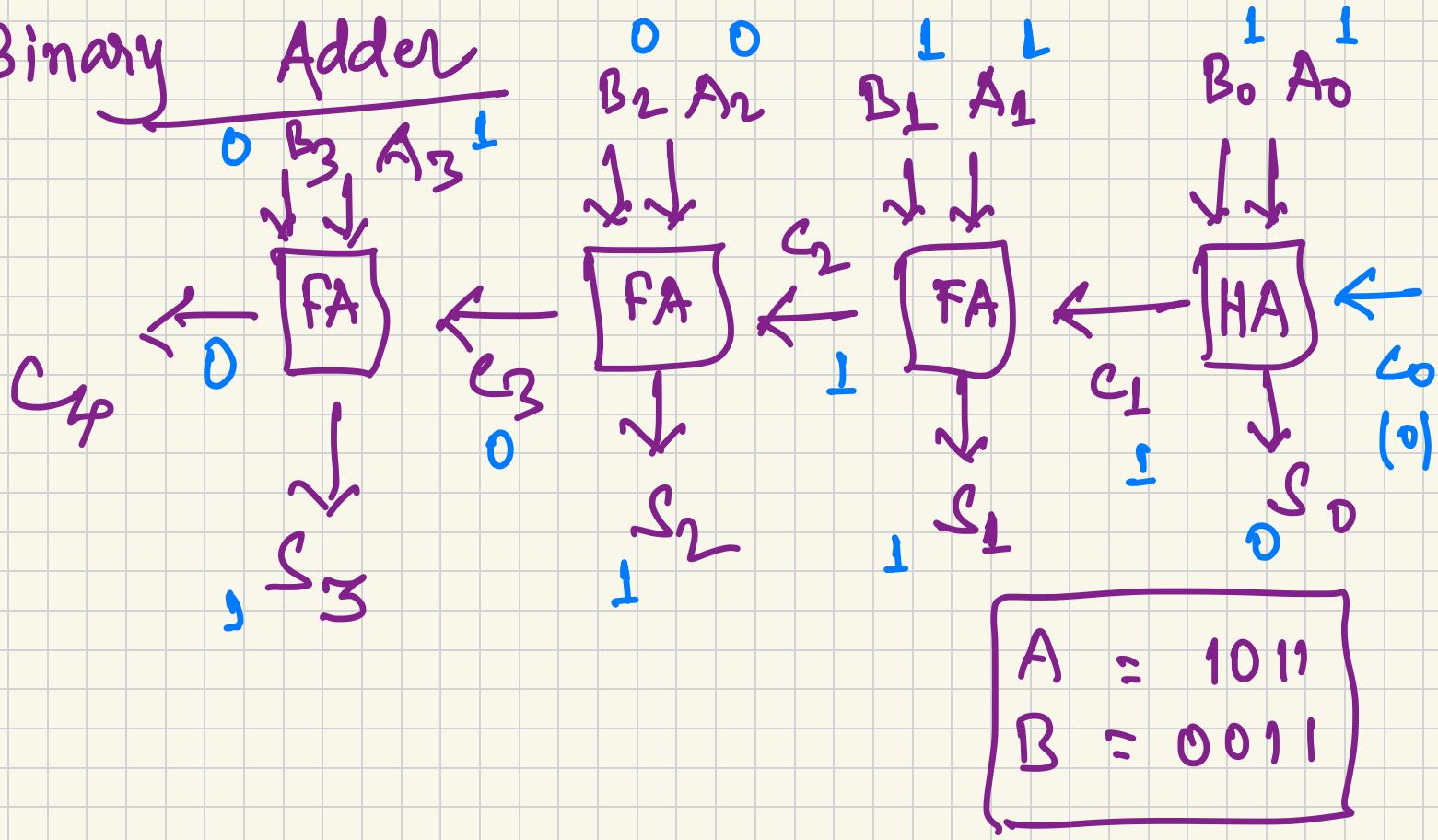
$$= \underbrace{xy + zxy} + z(x \oplus y)$$

$$= xy + z(x \oplus y)$$



Two half-adders (and an OR gate) can implement a full-adder.

Binary Adder



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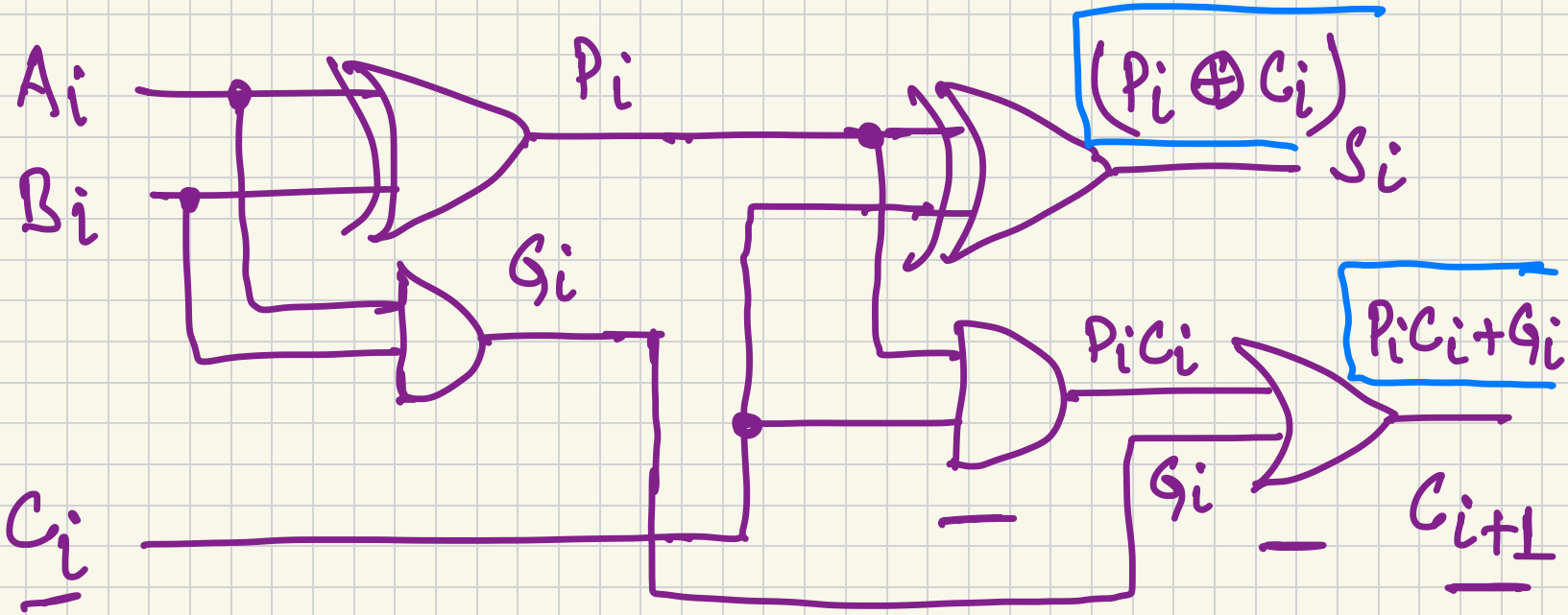
Carry Propagation



defined two new binary variables

$P_i = A_i \oplus B_i$ → carry propagate

$G_i = A_i B_i$ → carry generated

C_0 = input carry

$C_1 = P_0 C_0 + G_0$

$C_2 = P_1 C_1 + G_1$

$= P_1 (P_0 C_0 + G_0) + G_1$

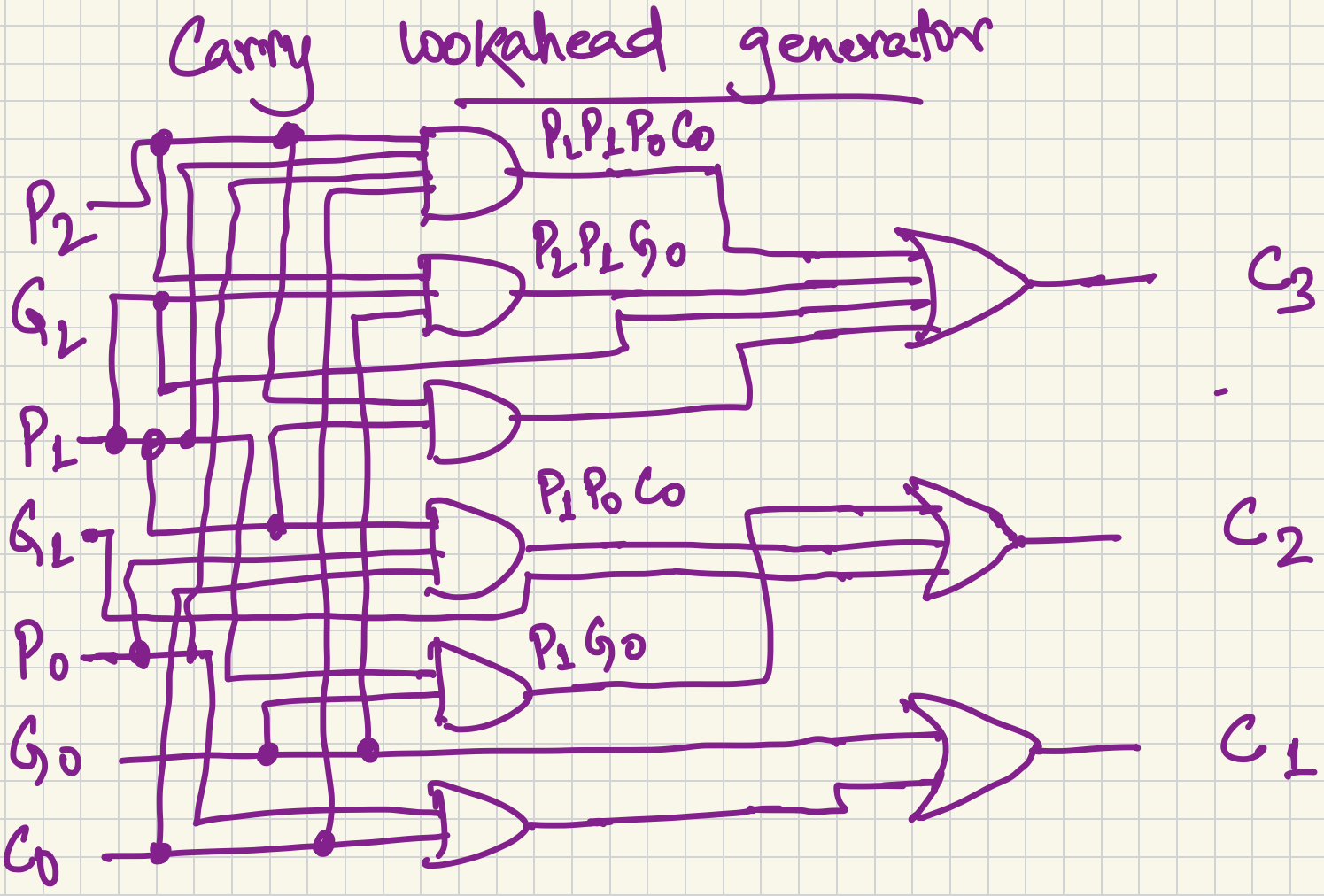
$= P_1 P_0 C_0 + P_1 G_0 + G_1$

$C_3 = P_2 C_2 + G_2$

$= P_2 (P_1 P_0 C_0 + P_1 G_0 + G_1) + G_2$

$= P_2 P_1 P_0 C_0 + P_2 P_1 G_0 + P_2 G_1 + G_2$

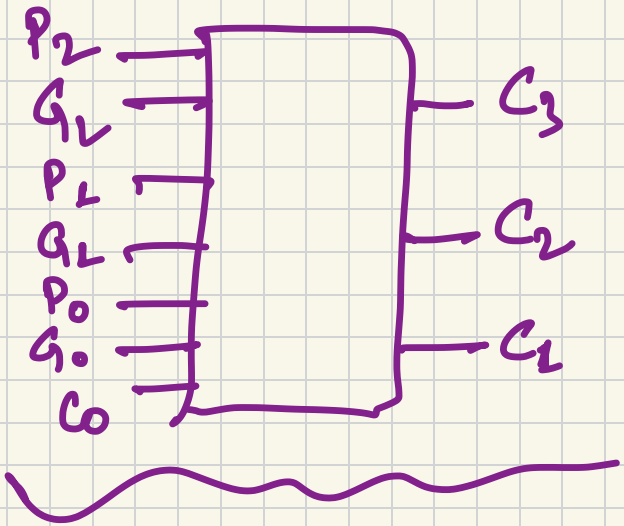
Carry lookahead generator

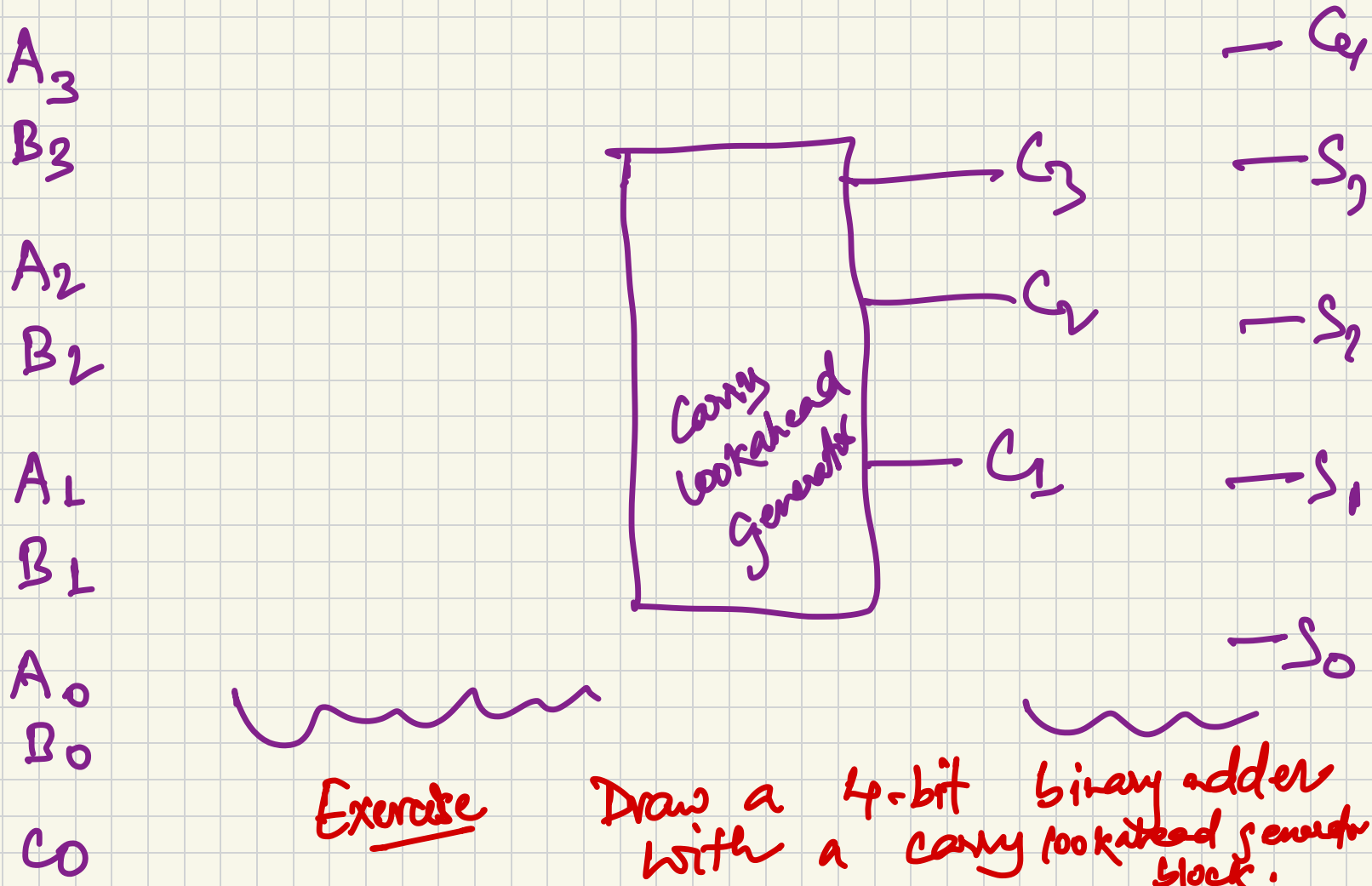


4-bit adder

$P_i = A_i \oplus B_i$

$G_i = A_i B_i$





Exercise: Draw a 4-bit binary adder with a carry lookahead generator block.