ACOL 215 (26th Nov.)

Ring counter

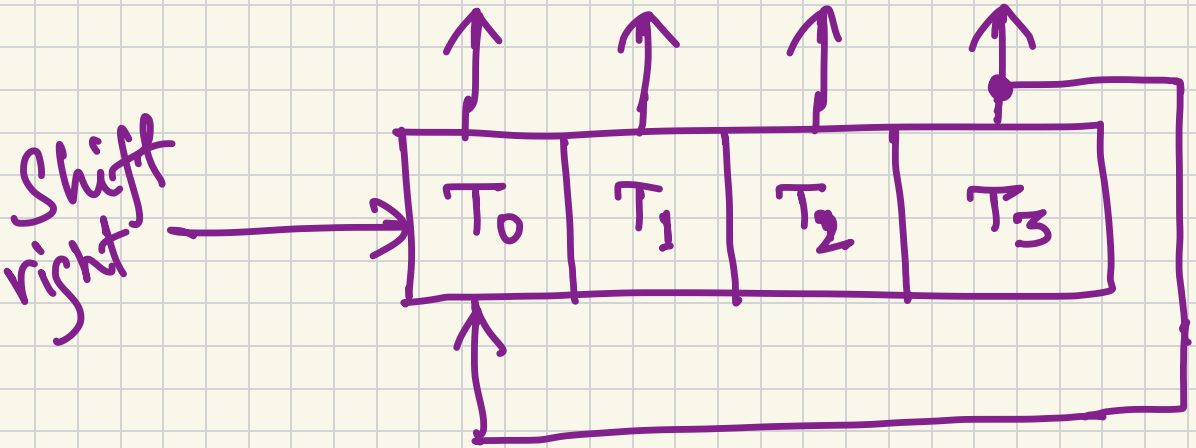
Timing signals

↳ control the sequence of operations in a digital system

↳ can be generated using a shift register (or by a counter using a decoder).

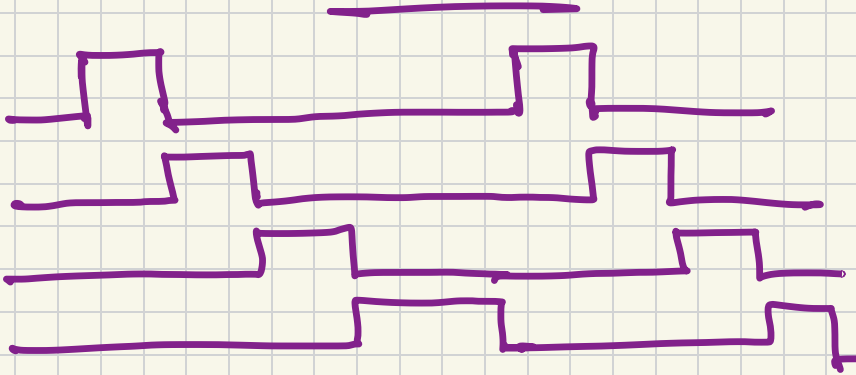
A ring counter is a circular shift register with only one flip-flop being set at any particular time.

→ And this single bit is shifted from one flip-flop to the next to produce the timing signals.

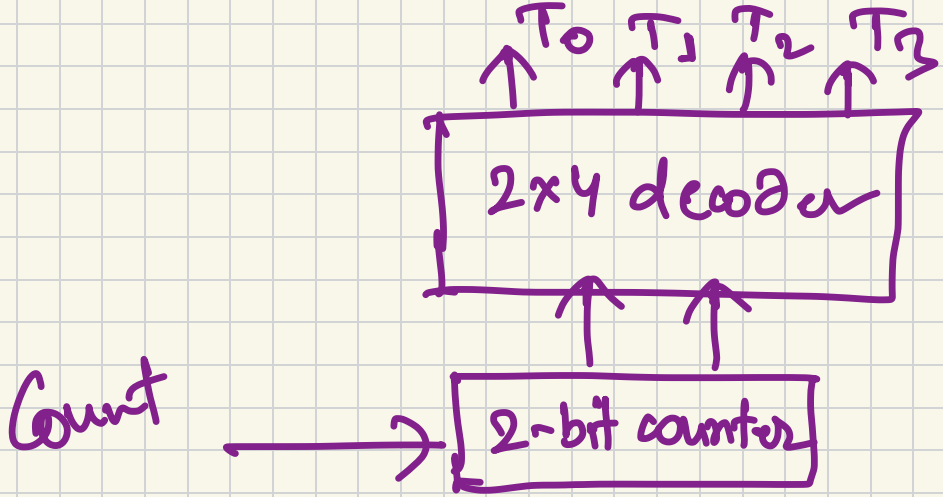


Initialised to 1000

T_0	1	0	0	0
T_1	0	1	0	0
T_2	0	0	1	0
T_3	0	0	0	1



An alternate design is to use a two bit counter that goes through four distinct states and then use a 2-to-4-line decoder.



In general, to generate 2^n timing signals, we need either a shift register with 2^n flip-flops, or an n-bit counter with n-to-2^n-line decoder.

16 flip-flops

4 flip-flop
+ 16 AND-gates
(4-input AND gate)

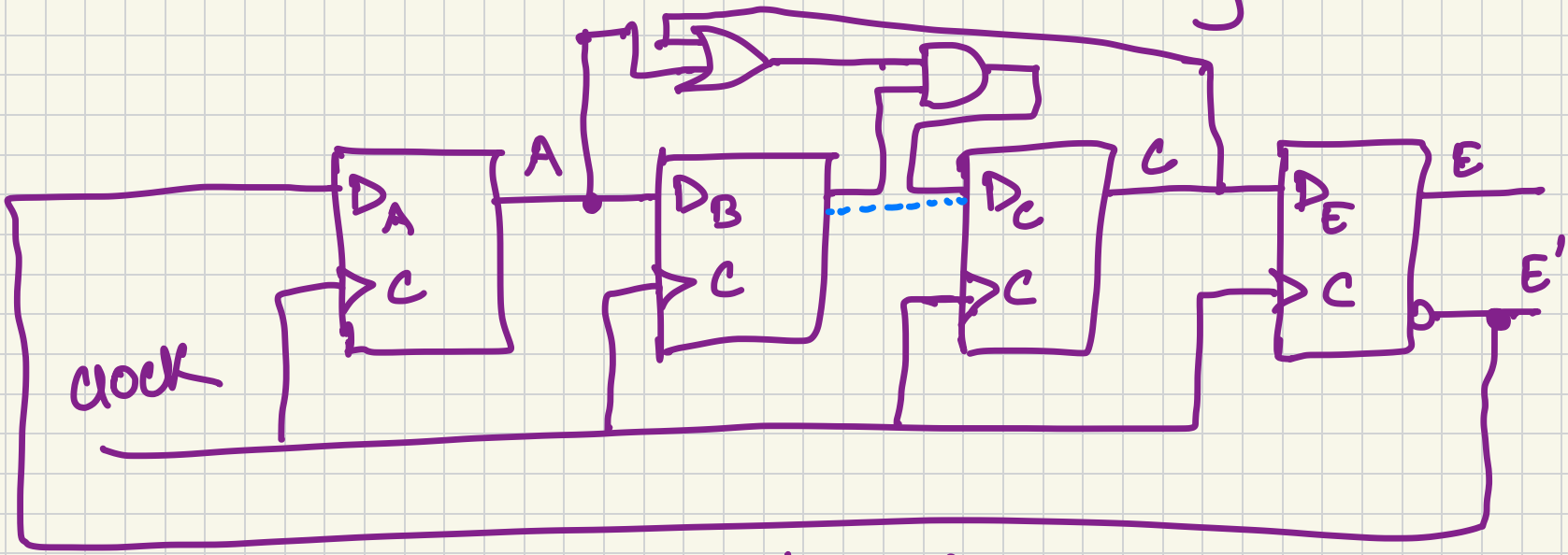
Johnson's counter

→ uses fewer than 2^n flip-flops

→ decodes only using two-input AND-gates.

Idea A K-bit ring counter circulates a single bit among the flip-flops to provide K distinguishable states.

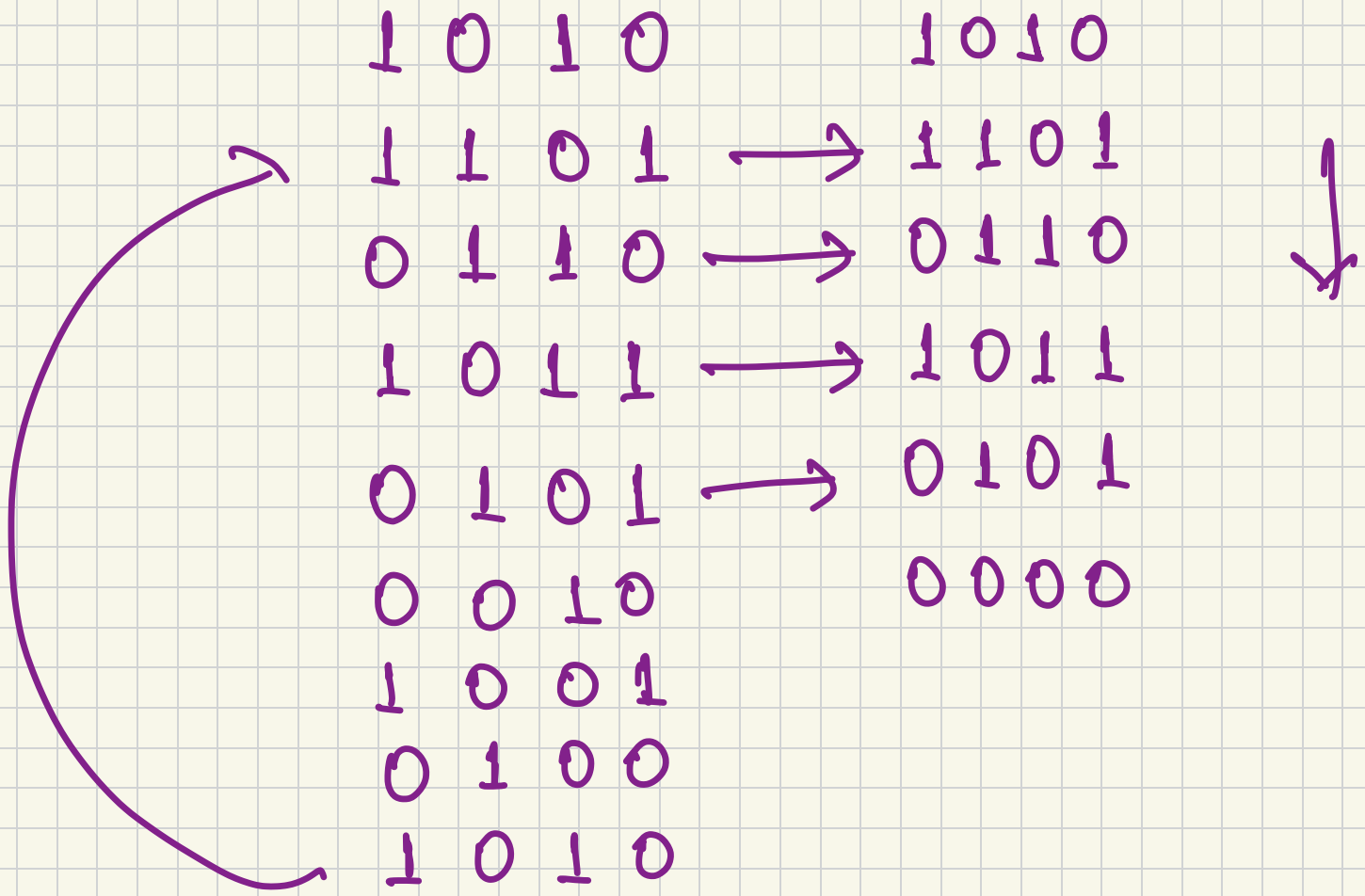
this number can be doubled if the shift register is connected as a switch-tail ring counter.



$$D_C = (A+C)B$$

Flip flop outputs			
A	B	C	E
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

AND-gate required for output
$A'E'$
AB'
BC'
CE'
AE
$A'B$
$B'C$
$C'E$


1 0 1 0
1 1 0 1
0 1 1 0
1 0 1 1
0 1 0 1
0 0 1 0
1 0 0 1
0 1 0 0
1 0 1 0
1 0 1 0
1 1 0 1
0 1 1 0
1 0 1 1
0 1 0 1
0 0 0 0