

ACOL 215

(04 Nov.)

Flip-flops are constructed in such a way that they operate properly when they are part of a sequential circuit that uses a common clock.

Two ways to modify a latch to a flip-flop

isolate the output
and prevent it from being
affected while the input is changing

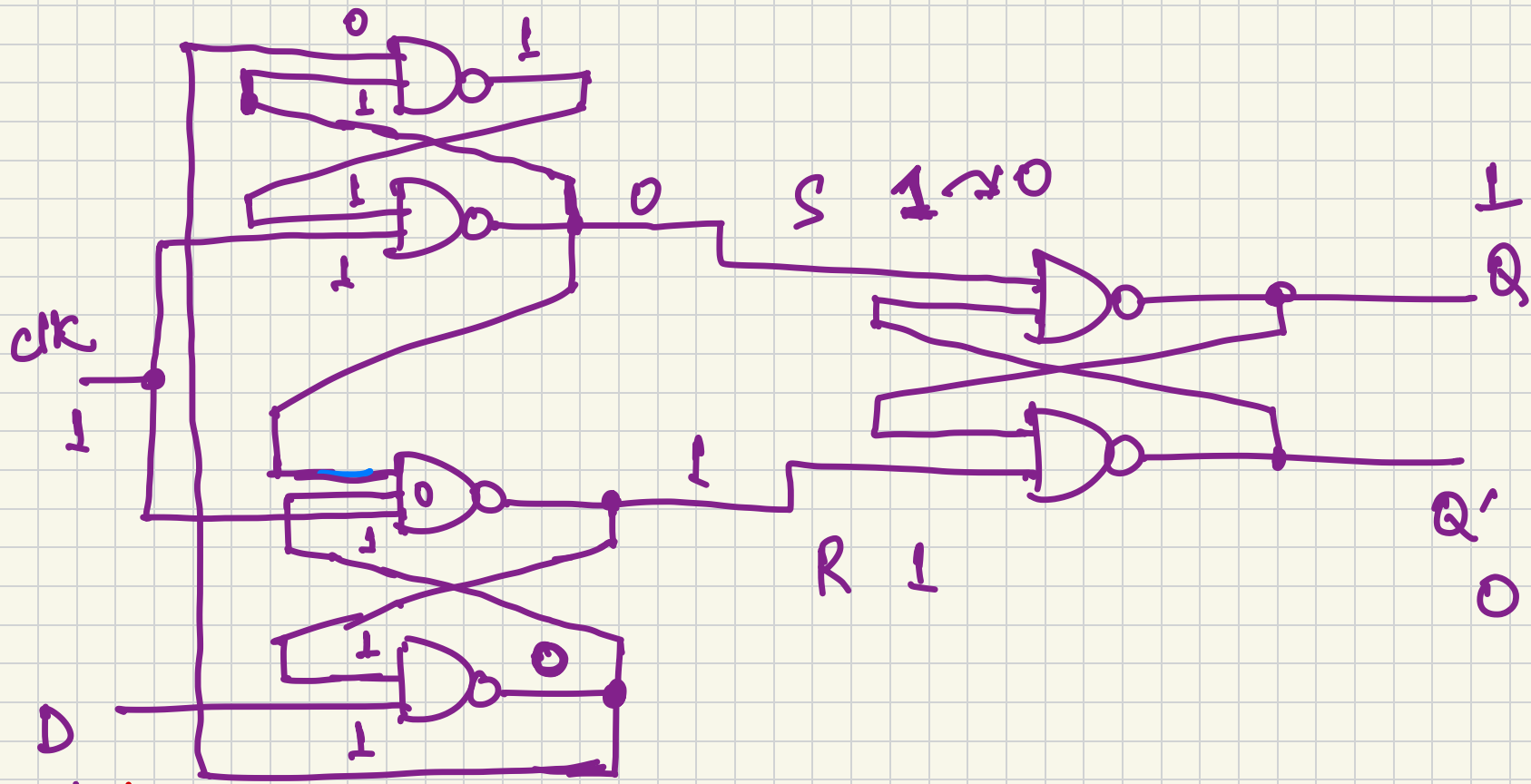
leader-follower

leader-follower

↓

produce a
flip-flop
that triggers
only during
a signal
transition

⇔



1/0 \rightarrow nothing changes at the output

The S-R inputs of the output latch are maintained at logic-1 level when $clk = 0$.

Therefore, the outputs remain in their present state.

What happens when clk changes to 1?

If $D = 0$ when clk becomes 1

→ R becomes 0 ←

→ Flip-flop goes to reset state making $Q = 0$ }

If D becomes 1 while the clk remains at 1

→ R continues to be 0

→ S continues to be 1

→ therefore no change in output

Similarly, if $D = 1$ when clk becomes 1, R becomes 1; S changes to 0

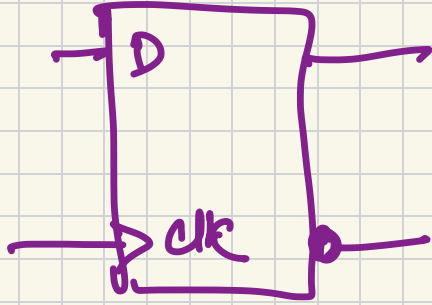
Flip-flop goes to the set state making $Q = 1$ ←

Note 1. When the input clock in the positive-edge triggered flip flop makes a positive transition, the value of D is transferred to Q.

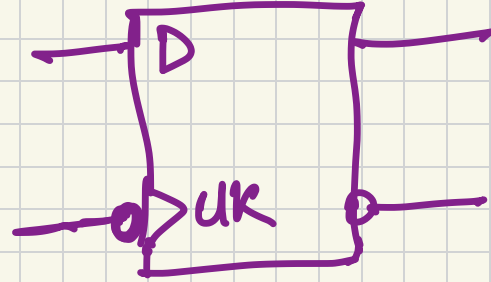
2. A negative transition of the clock does not affect the output.

3. changes in D when the clk is in the steady state (logic-1 / logic-0) does not affect the output.

Graphical symbols for edge-triggered D flip-flop



Positive edge
triggered

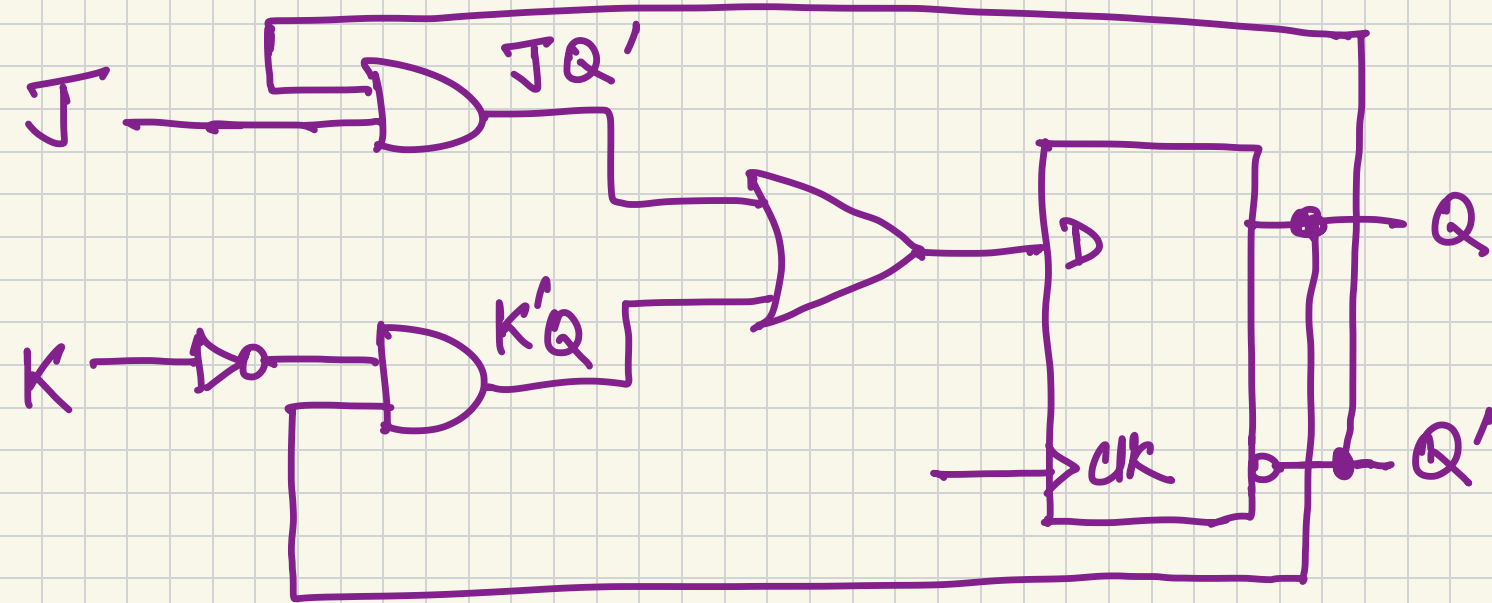


Negative edge
triggered

setup time - min time for which D must be maintained at a constant value prior to the occurrence of the clock transition

hold time - min time for which D must not change after the positive clock transition.

JK flip flop



$$D = JQ' + K'Q$$

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When $J = 1, K = 0$

$$D = 1$$

(next clock edge
sets $Q = 1$)

$J = 0, K = 1$

$$D = 0$$

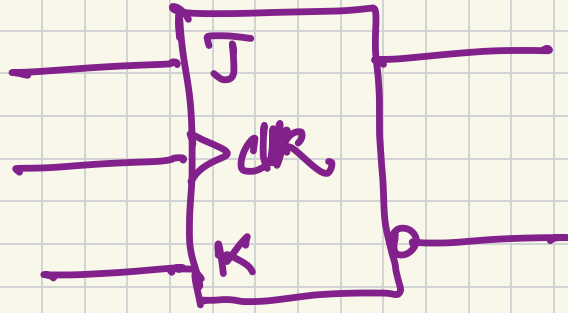
(next clock edge
set $Q = 0$)

$$J = K = 1$$

$$J = K = 0$$

$D = Q'$
(next clock edge complements the output)

$D = Q$
(next clock edge does not change the output)



Graphical symbol
for a JK flip
flop

T flip flop
(toggle)

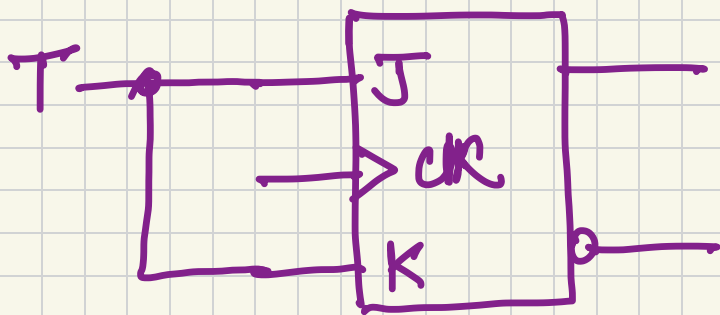
J and K are tied together

$T = 0$

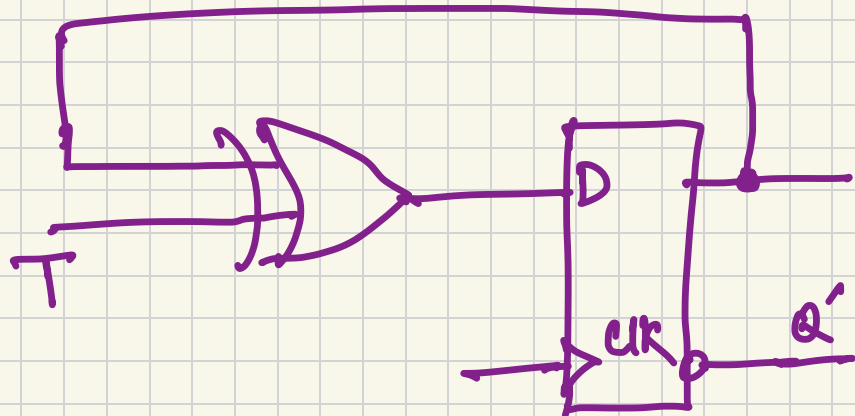
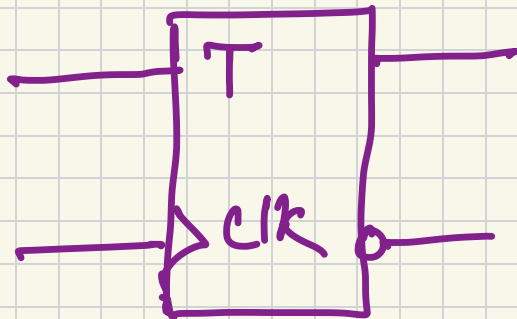
clock edge does not
change the output

$T = 1$

clock edge complements
the output



From JK flip
flop



From D flip
flop

graphical
symbol

Characteristic Tables

D flip-flop

$$\begin{bmatrix} D & Q(t+1) \\ 0 & 0 \\ 1 & 1 \end{bmatrix}$$

T flip-flop

$$\begin{bmatrix} T & Q(t+1) \\ 0 & Q(t) \\ 1 & Q(t)' \end{bmatrix}$$

J-K flip flop

$$Q(t+1)$$

No change

reset

set

set complement $Q(t)'$

100%

K
o
o
o

Characteristic equations

$$D = Q(t+1)$$

$$T \oplus Q(t) = Q(t+1)$$

$$T Q(t)' + K' Q(t) = Q(t+1)$$