ACOL 215

(03rd Dec.)

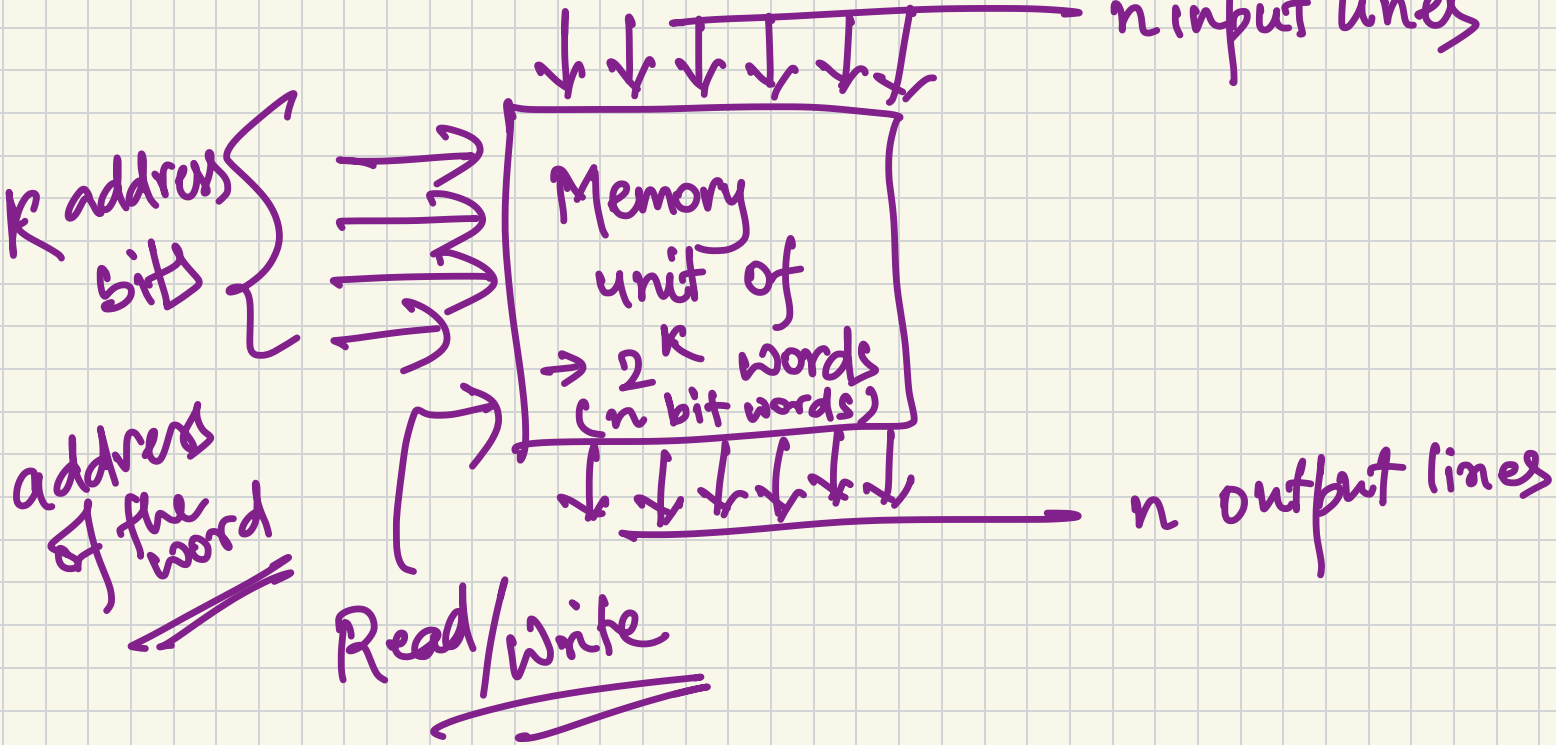
Memory

A memory unit is a device to which binary information is transferred for storage and from which information is read for processing.

Through read and write operations

Two types → RAM (random-access)
→ ROM (read-only)

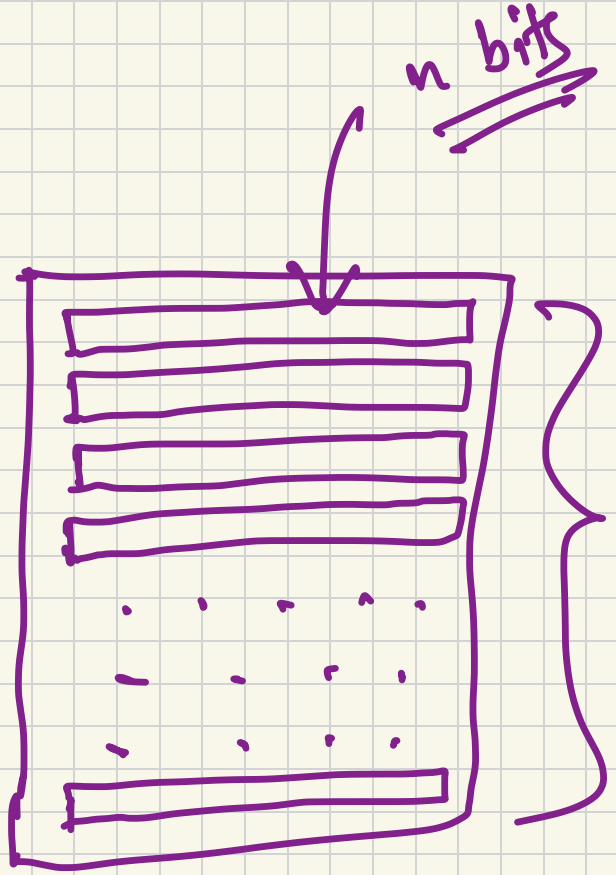
binary information is usually stored in groups of bits called "words".

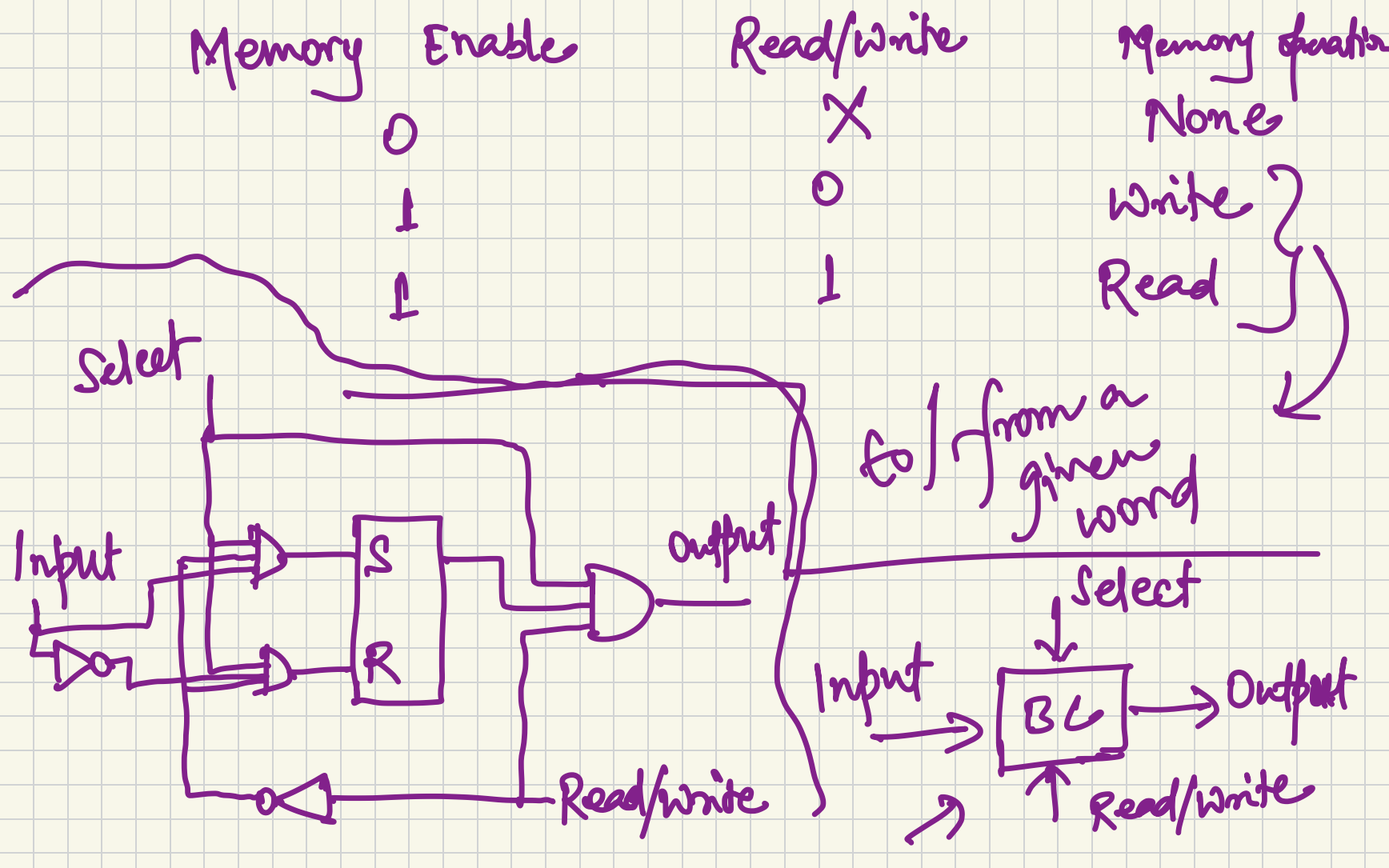


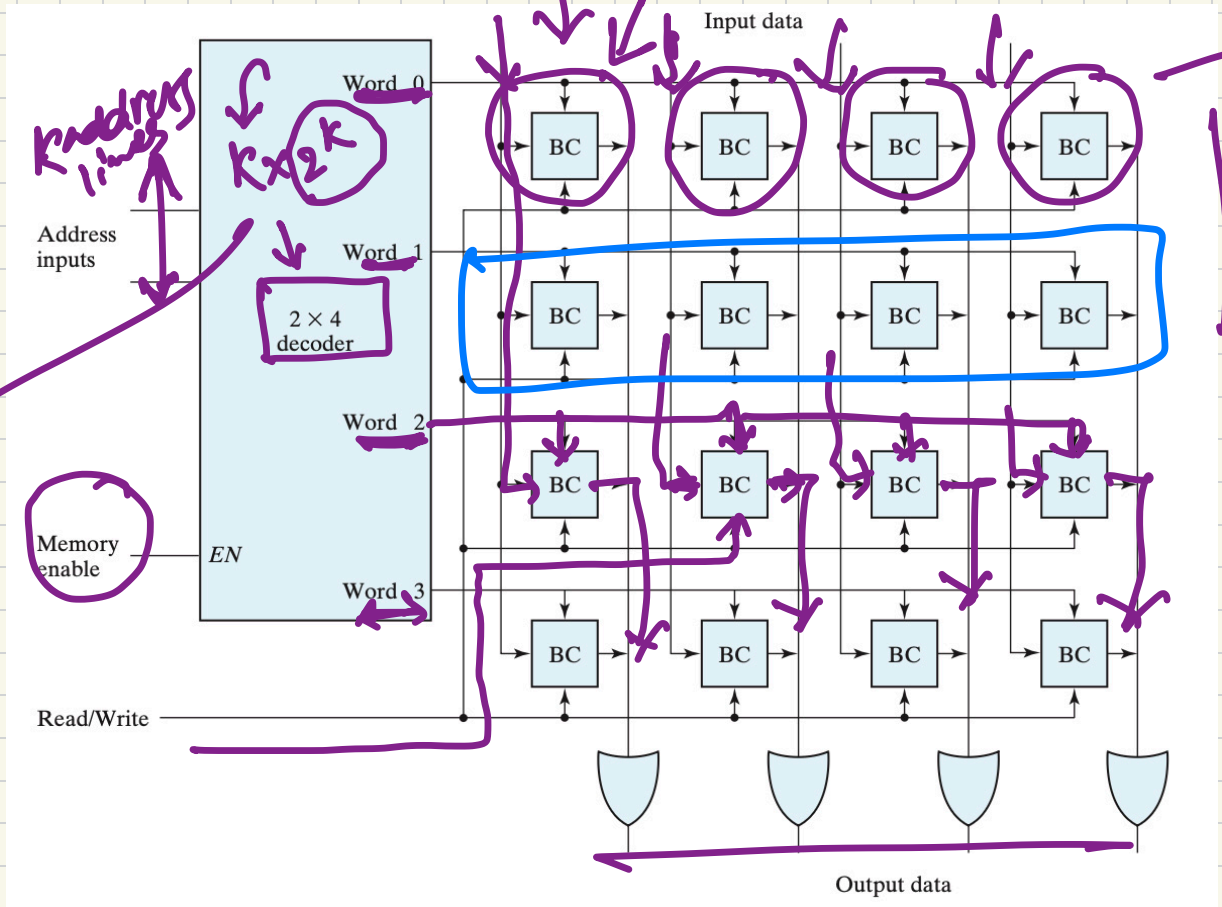
Memory addess

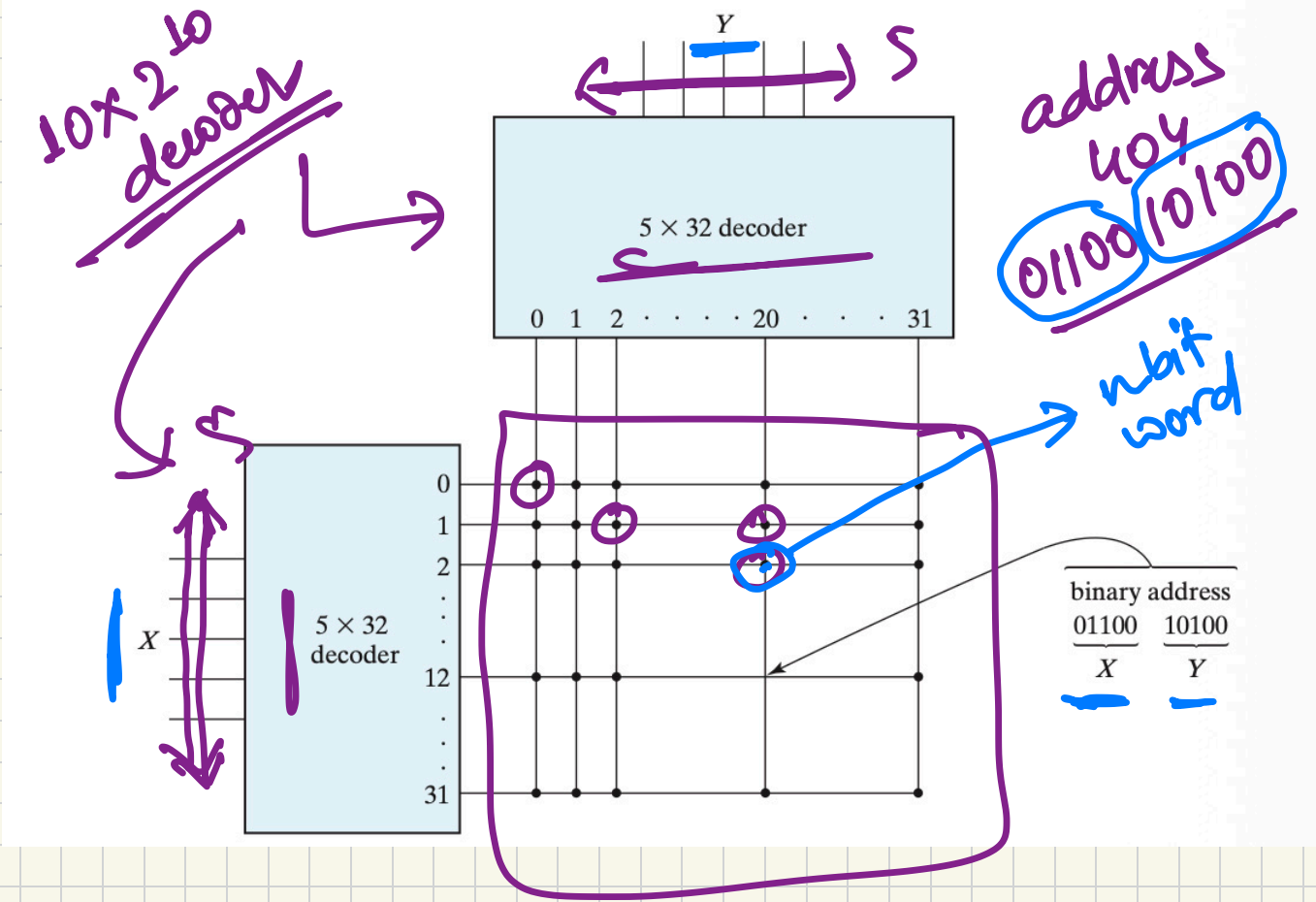
Binary	Decimal
00000 ... 0	0
00000 ... 1	1
— — — — 10	2
— — — —	3
— — — —	⋮
— — — —	⋮
1111111111	1023

10 bits




Memory Enable
Read/Write
Memory operation
0
1
1
X
0
1
None
Write
Read
Select
Input
S
R
Output
Read/write
to/from a given word
Select
Input
BC
Output
Read/write


Input data
Word 0
Word 1
Word 2
Word 3
Address inputs
2 × 4 decoder
Memory enable
EN
Read/Write
BC
Output data


10x2 to decoder
Y
5
5 × 32 decoder
0 1 2 · · · · 20 · · · 31
address
404
01100
10100
n-bit word
X
5 × 32 decoder
0
1
2
12
31
binary address
01100
10100
X
Y

Address Multiplexing

RAM → Static RAM (SRAM)

RAM → Dynamic RAM (DRAM)

SRAM memory cells typically contain six transistors.

DRAM cells contain a single (MOS) transistor and a capacitor.

disadvantage capacitors discharge with time.

(addressed by refreshing the dynamic memory)

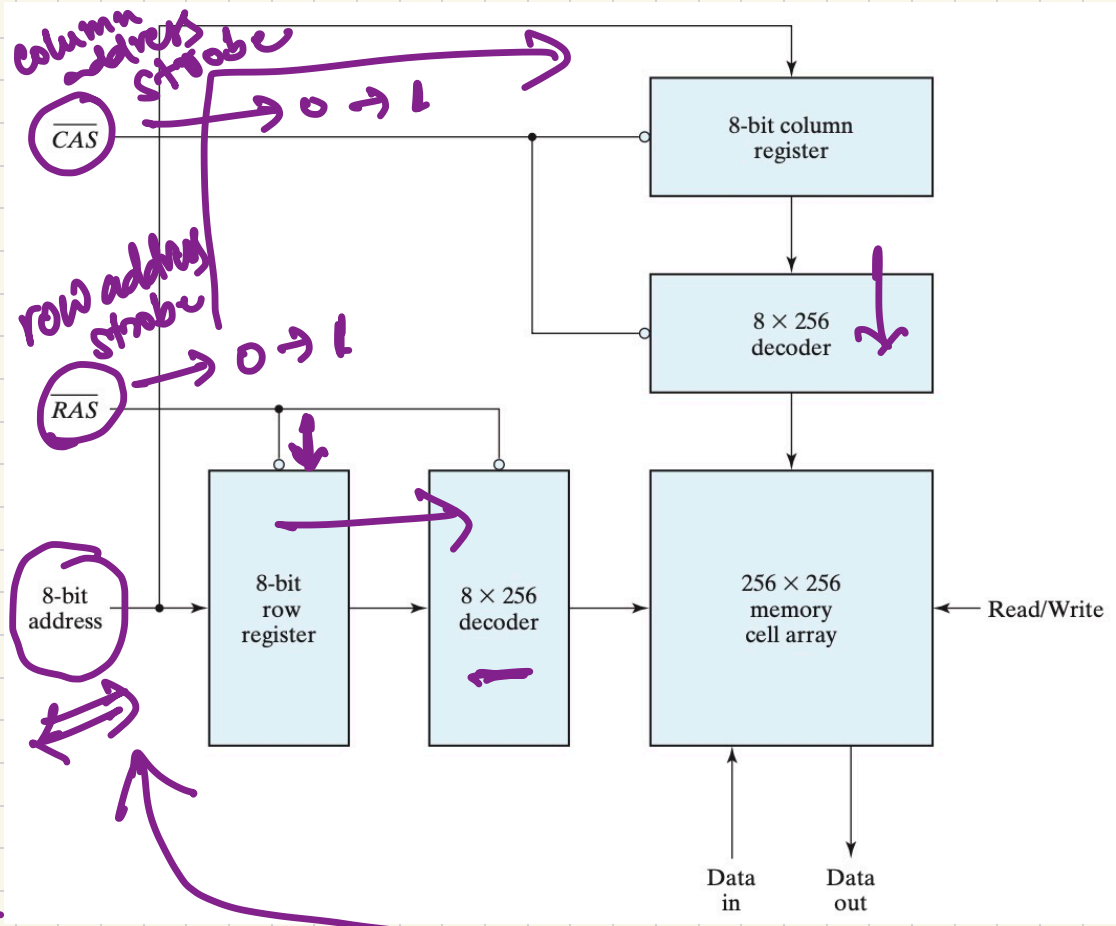
cycle through the words every few milliseconds to restore the decaying charge.

advantage allows four-times as much memory as SRAMs on a given chip-size

this necessitates address multiplexing

→ DRAMs are a preferred technology in compact devices like personal computers.

the address is applied in two parts - row address and column address



address multiplexing

64 K word memory

64 x 1024

$= 2^6 \times 2^{10}$

$= 2^{16}$

16 bits

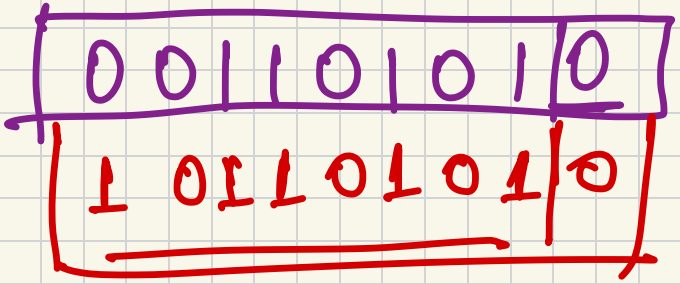
8 row + 8 column bits

And the same address pins are used for both.

Error detection and correction

↳ to improve the reliability of memory units

→ eg. a parity bit could be generated and stored along with the word:



An error correcting code generates multiple parity bits that are stored with the data word.

Hamming code

→ most common error-correcting code used in RAMs.

k parity bits are added to an n bit word, forming a word of (n+k) bits.

data word :

4 parity bits

1 1 0 0 0 1 0 0

Bit positions

1	2	3	4	5	6	7	8	9	10	11	12
P_1	P_2	1	P_4	1	0	0	P_8	0	1	0	0
0	0		1				1				

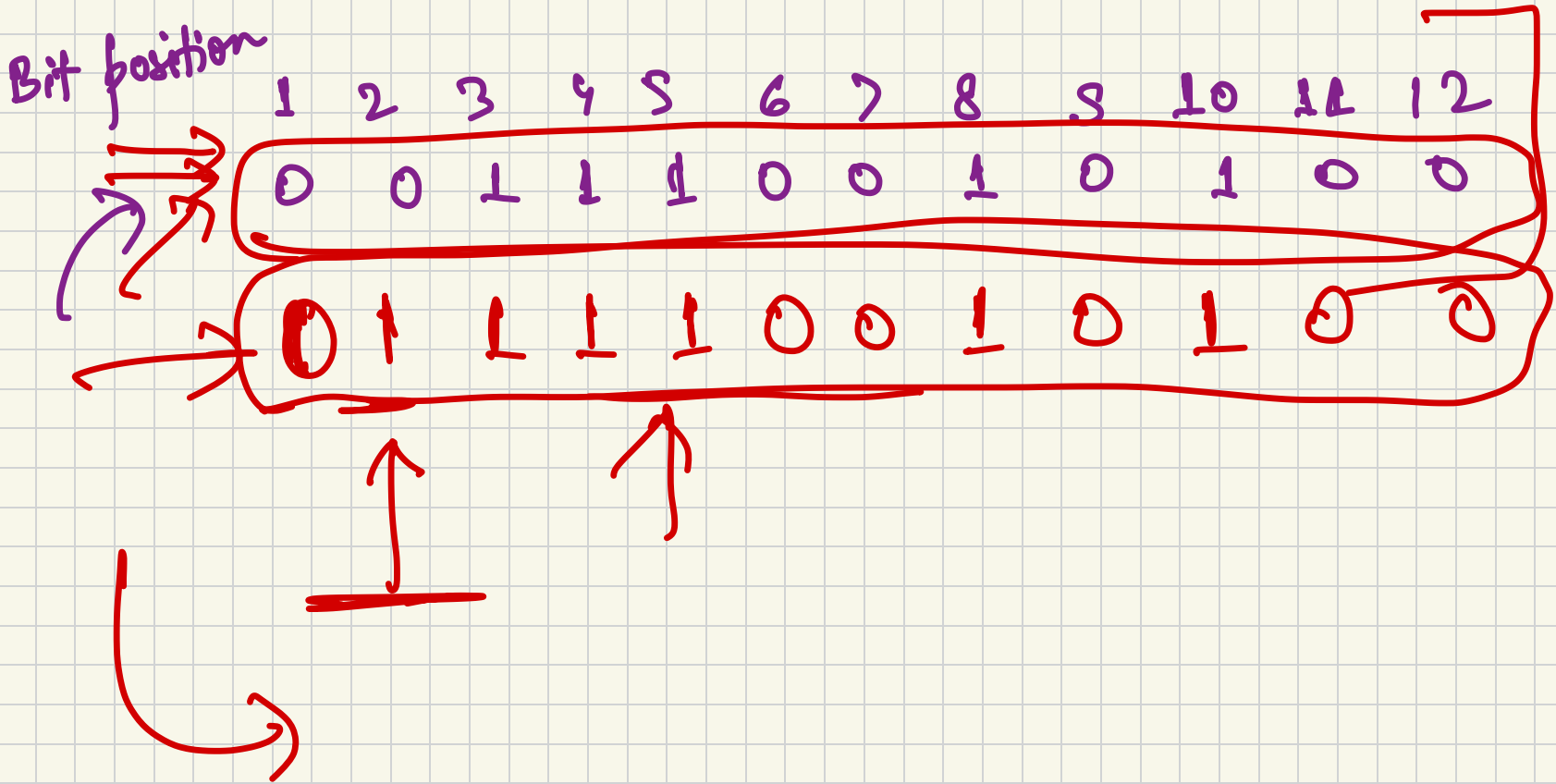
powers of 2 bit-positions

P_1 = XOR (3, 5, 7, 9, 11) = 0 ←

P_2 = XOR (3, 6, 7, 10, 11) = 0

P_4 = XOR (5, 6, 7, 12) = 1

P_8 = XOR (9, 10, 11, 12) = 1


Bit position
1 2 3 4 5 6 7 8 9 10 11 12
0 0 1 1 1 0 0 1 0 1 0 0
0 1 1 1 1 0 0 1 0 1 0 0