

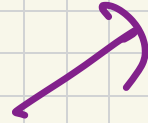
ACOL 215

(12th Nov.)

Designing Clocked Sequential Circuits

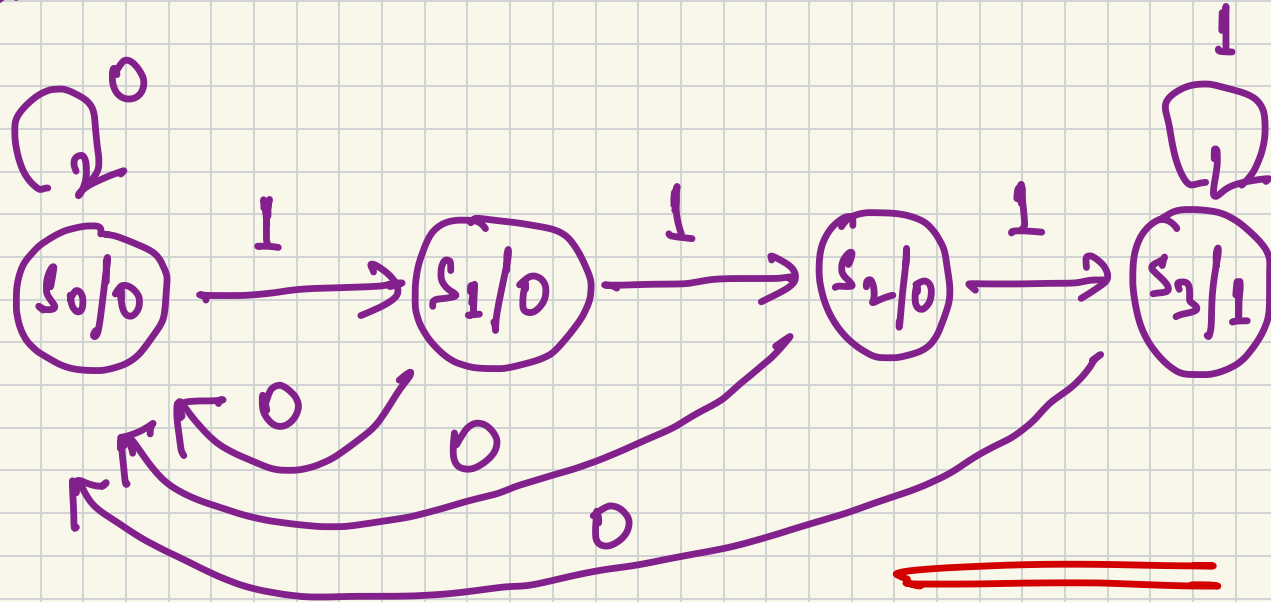
Set of specifications → Logic diagram

↓ State tables/
State diagrams



Suppose we wish to design a circuit that detects a sequence of three or more consecutive 1's in an input bitstream.

4 states
↓
2 flip-flops
to represent
them



State table

A	B
0	0
0	0
0	1
0	1
1	0
1	0
1	0
1	1
1	1

01010101

$$\begin{array}{cc} A & B \\ 1 & 0 \\ 1 & 0 \\ 1 & 1 \\ 0 & 0 \\ 1 & 0 \\ 0 & 0 \\ 1 & 1 \\ 0 & 0 \\ 1 & 0 \end{array}$$

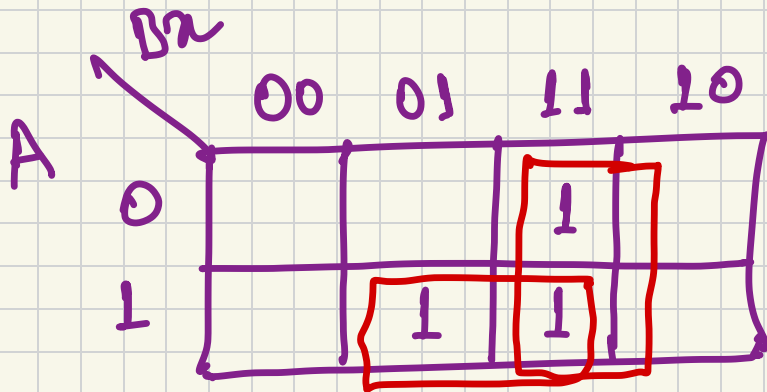
zyooyoyt

With a D flip flop, we know that

$$A(t+1) = \underline{D_A(A, B, x) = \Sigma(3, 5, 7)}$$

$$B(t+1) = \underline{D_B(A, B, x) = \Sigma(1, 5, 7)}$$

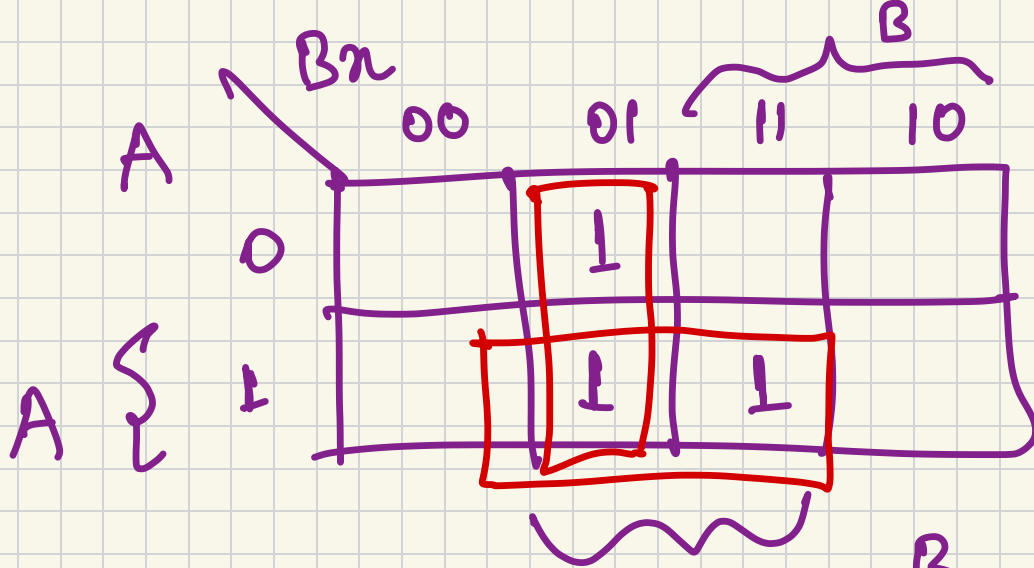
$$y(A, B, x) = \Sigma(6, 7)$$



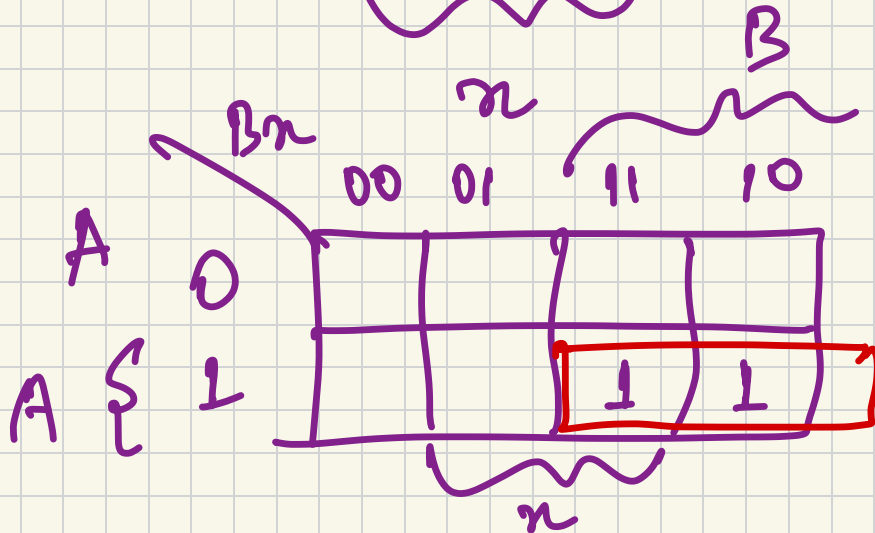
A Karnaugh map for the function D_A with variables A and Bx . The map is a 2x4 grid. The columns are labeled Bx with values 00, 01, 11, 10. The rows are labeled A with values 0 and 1. The cells contain 1s at (A=0, Bx=11), (A=1, Bx=01), and (A=1, Bx=11). These three cells are grouped together by a red rectangle, indicating the sum of minterms $\Sigma(3, 5, 7)$.

	Bx			
	00	01	11	10
$A=0$			1	
$A=1$		1	1	

$$\underline{D_A = Ax + Bx}$$

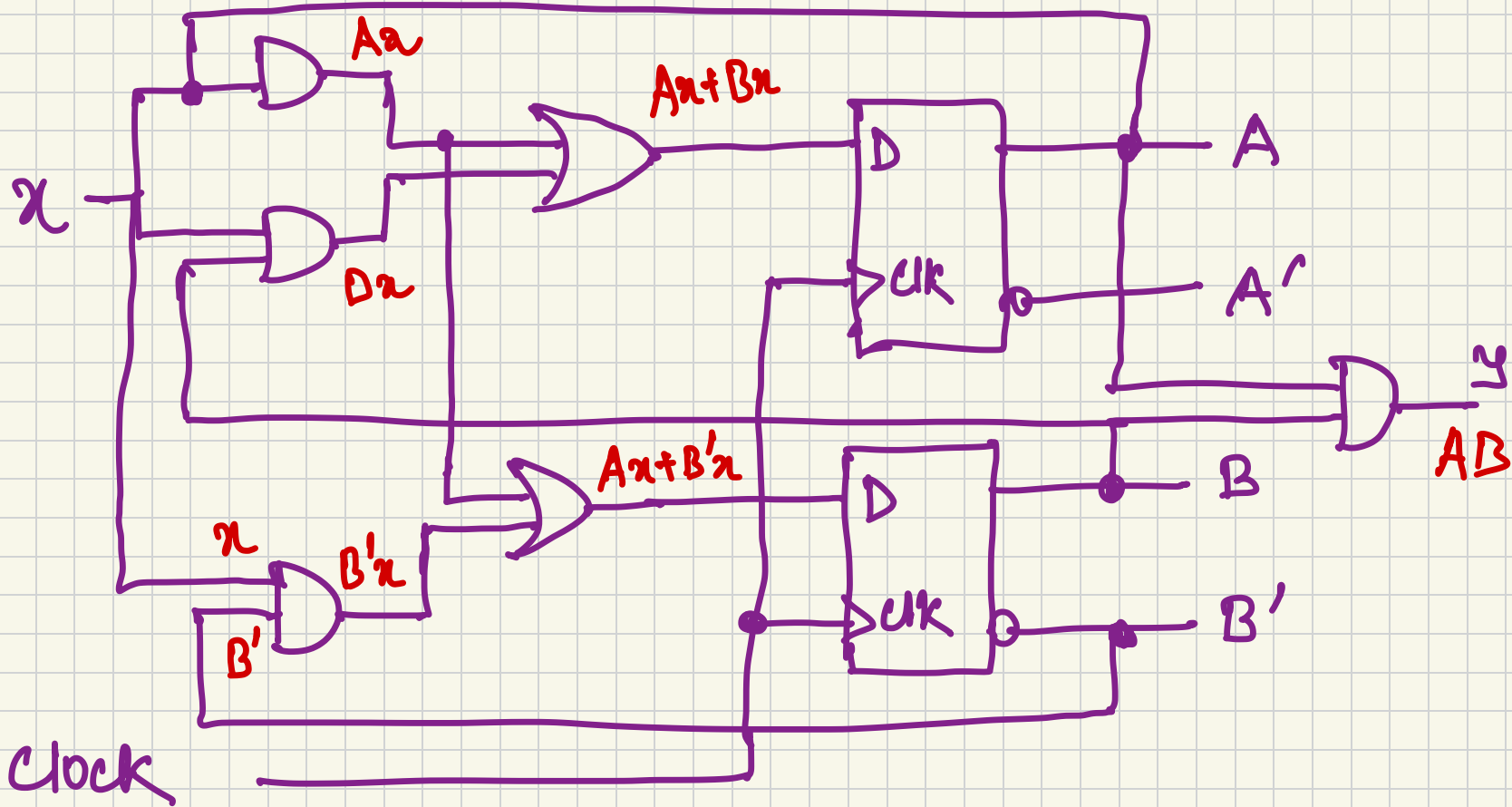


$$D_B = Ax + B'x$$



$$y = AB$$

$$D_A = A\alpha + B\alpha \quad ; \quad D_B = A\alpha + B'\alpha \quad ; \quad y = AB$$



Recall the JK and T flip-flop characteristic tables

J	K	$Q(t+1)$	T	$Q(t+1)$
0	0	$Q(t)$	0	$Q(t)$
0	1	0 (reset)	1	$Q'(t)$
1	0	1 (set)		
1	1	$Q'(t)$		

From the characteristic tables,
we can get the following
excitation tables

$Q(t)$	$Q(t+1)$	J	K			
0	0	0	X	$Q(t)$	$Q(t+1)$	T
0	1	1	X	0	0	0
1	0	X	1	1	1	1
1	1	X	0	1	0	1
				1	1	0

State table

Flip flop inputs

Present State Input Next State Output

A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	1	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	1

J _A	K _A	J _B	K _B
0	x	0	x
0	x	1	x
0	x	x	1
1	x	x	1
x	1	0	x
x	0	1	x
x	1	x	1
x	0	x	0

J_A $B\pi$

	00	01	11	10
A 0	0	0	1	0
A 1	X	X	X	X

$J_A = B\pi$

K_A $B\pi$

	00	01	11	10
A 0	X	X	X	X
A 1	1	0	0	1

$K_A = \pi'$

J_B $B\pi$

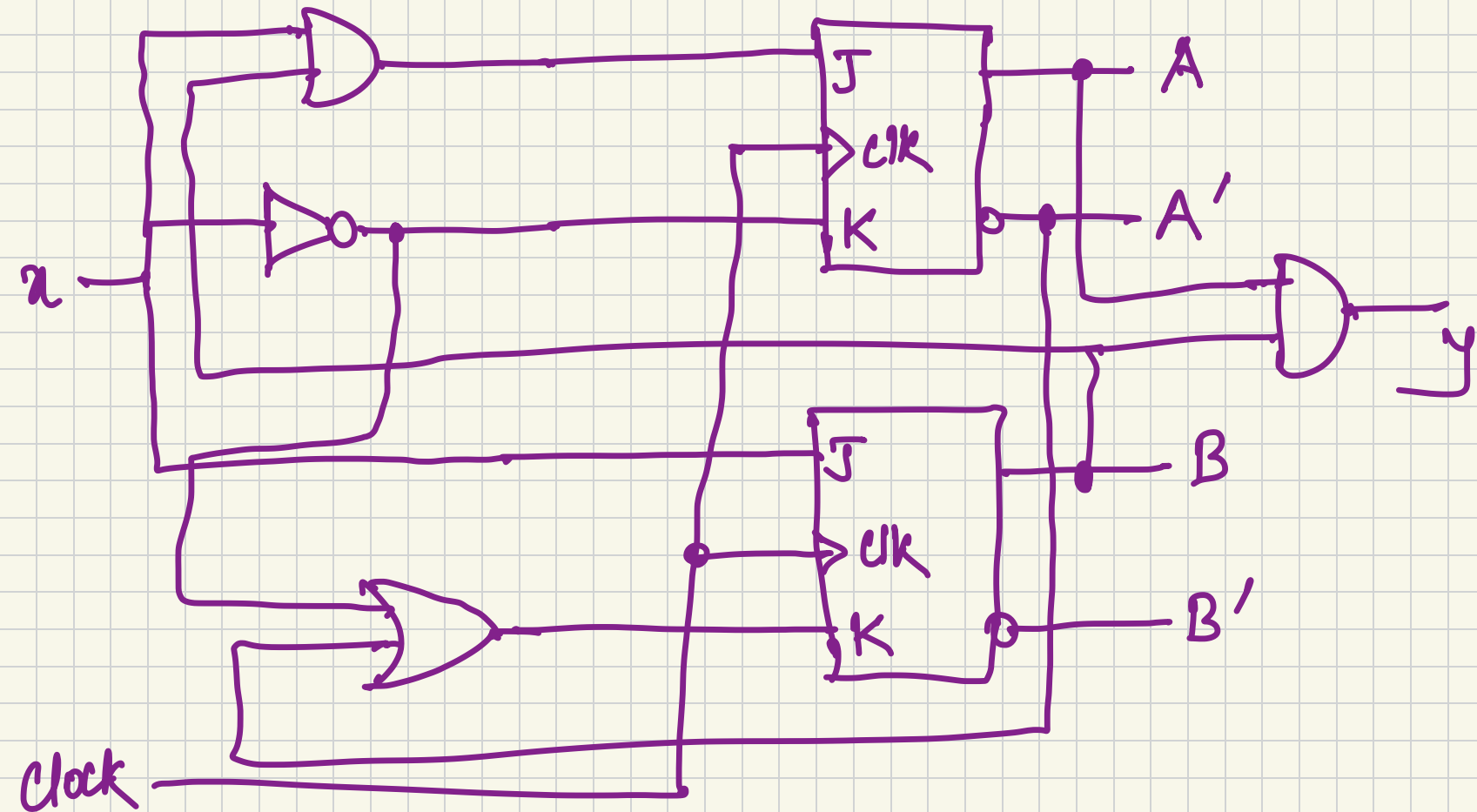
	00	01	11	10
A 0	0	1	X	X
A 1	0	1	X	X

$J_B = \pi$

K_B

	00	01	11	10
A 0	X	X	1	1
A 1	X	X	0	1

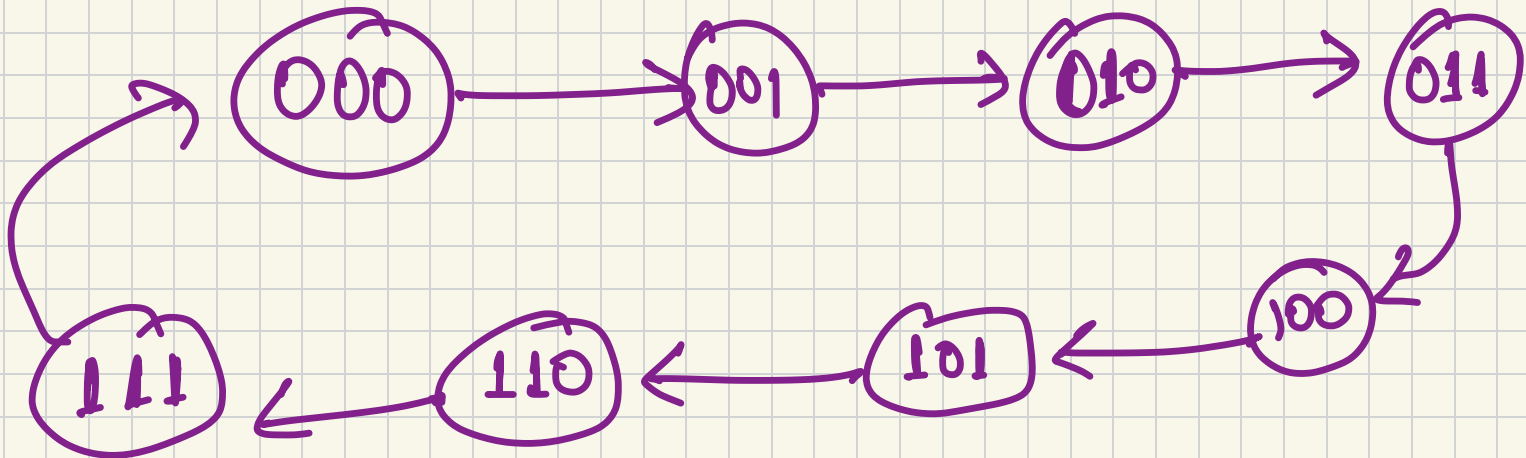
$K_B = \pi' + A'$



Synthesis with T flip flops

n-bit binary counter

→ 0 to $2^n - 1$



State Table

Present state

A_2	A_1	A_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Next state

A_2	A_1	A_0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0

Flipflop inputs

T_{A_2}	T_{A_1}	T_{A_0}
0	0	1
0	1	1
0	0	1
1	1	1
0	0	1
0	1	1
0	0	1
1	1	1

$A_1 A_0$

A_2

	00	01	11	10
0	0	0	1	0
1	0	0	1	0

$$T_{A_2} = A_1 A_0$$

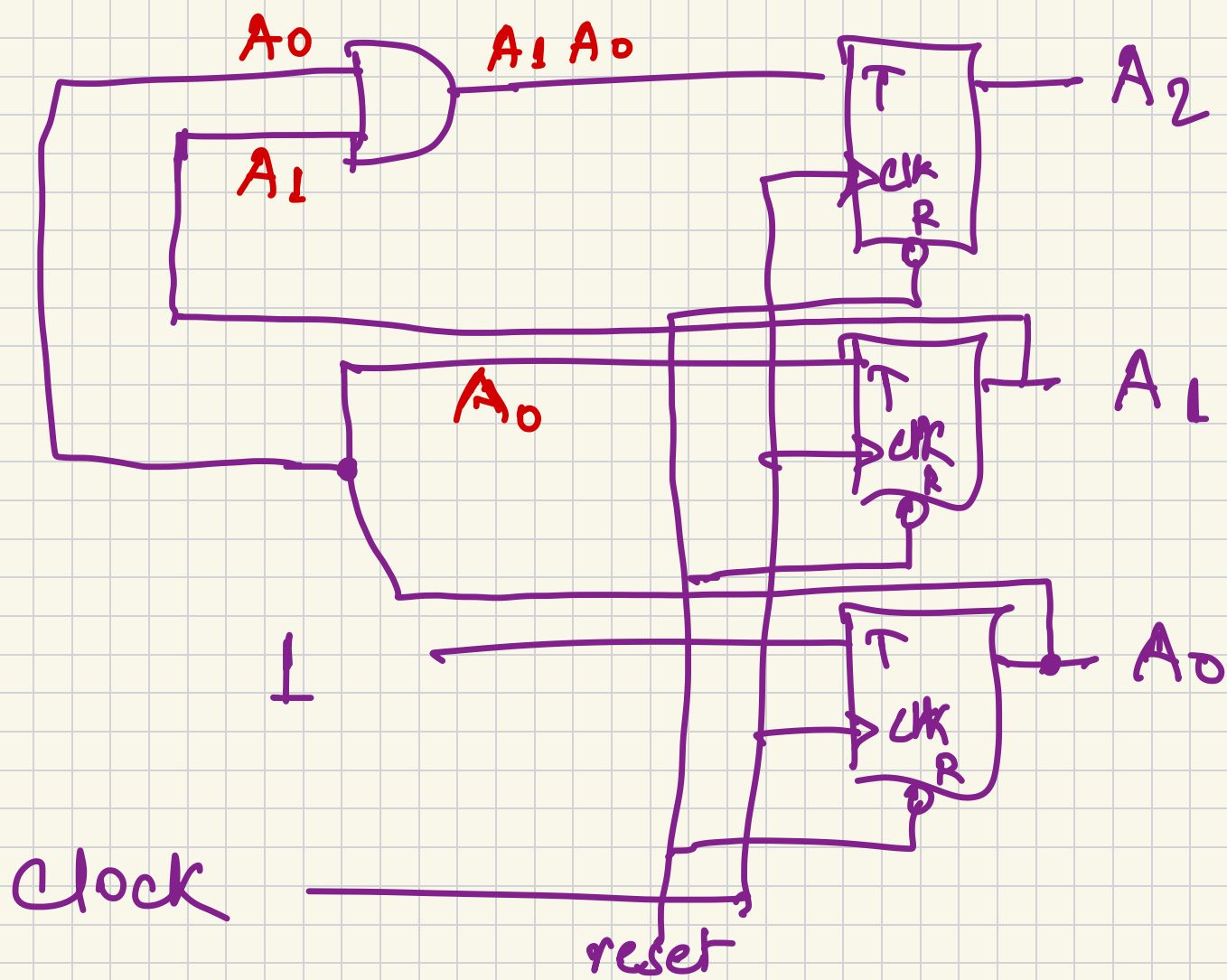
$A_1 A_0$

A_2

	0	1	1	0
0	0	1	1	0
1	0	1	1	0

$$T_{A_1} = A_0$$

$$T_{A_0} = 1$$



Exercise Synthesize a circuit for the given state table using JK flip-flops.

<u>Present state</u>		<u>Input</u>	<u>Next state</u>	
A	B	x	A	B
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0