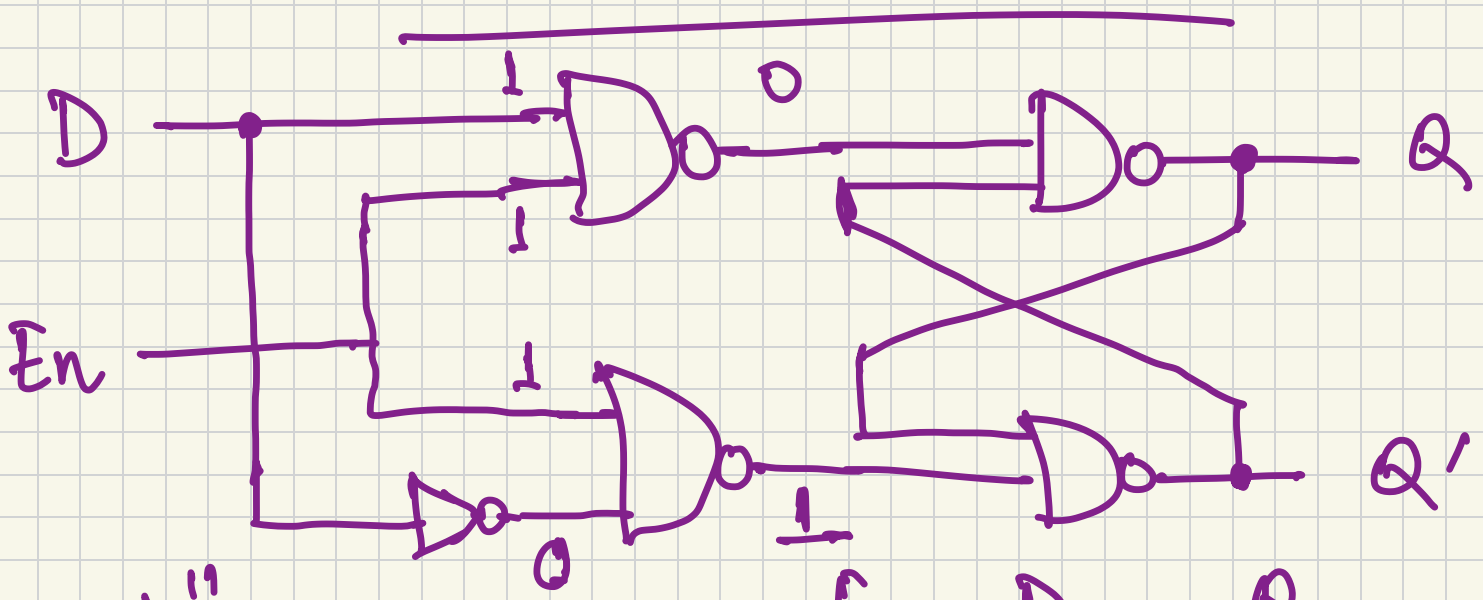
ACOL 215 (Nov. 3)

One way to eliminate the undesirable "forbidden" condition is to ensure that S, R are never 1 at the same time.

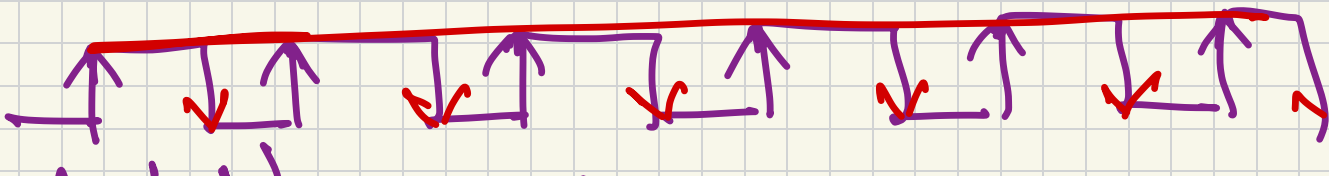
D (Transparent) Latch



"Transparent" because D is visible at the output.

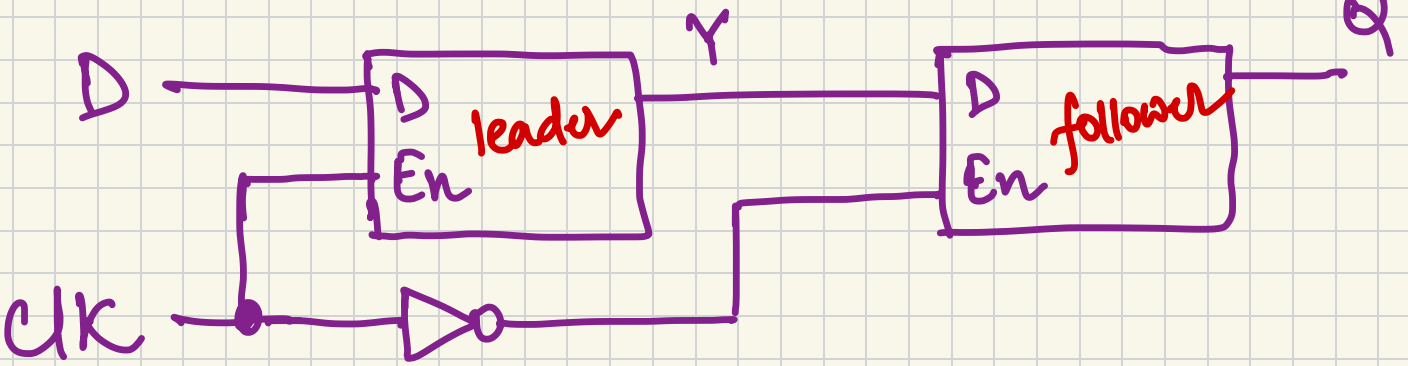
En	D	Q
0	X	No change
1	0	Q = 0
1	1	Q = 1

Edge-triggered D flip-flop



positive edges (0 to 1)

negative edges (1 to 0)



When clk = 0, Q equals Y.
(follower is enabled)
(leader is disabled)

When the clock pulse changes to logic-1 level, leader is enabled, and follower is disabled.

↳ any change in D does not affect the output.

When the clk now goes from 1 to 0, leader is disabled, and the value of Y is transferred to Q.

↳ negative edge triggered D flip-flop

Exercise construct ~ positive edge triggered D flip flop.