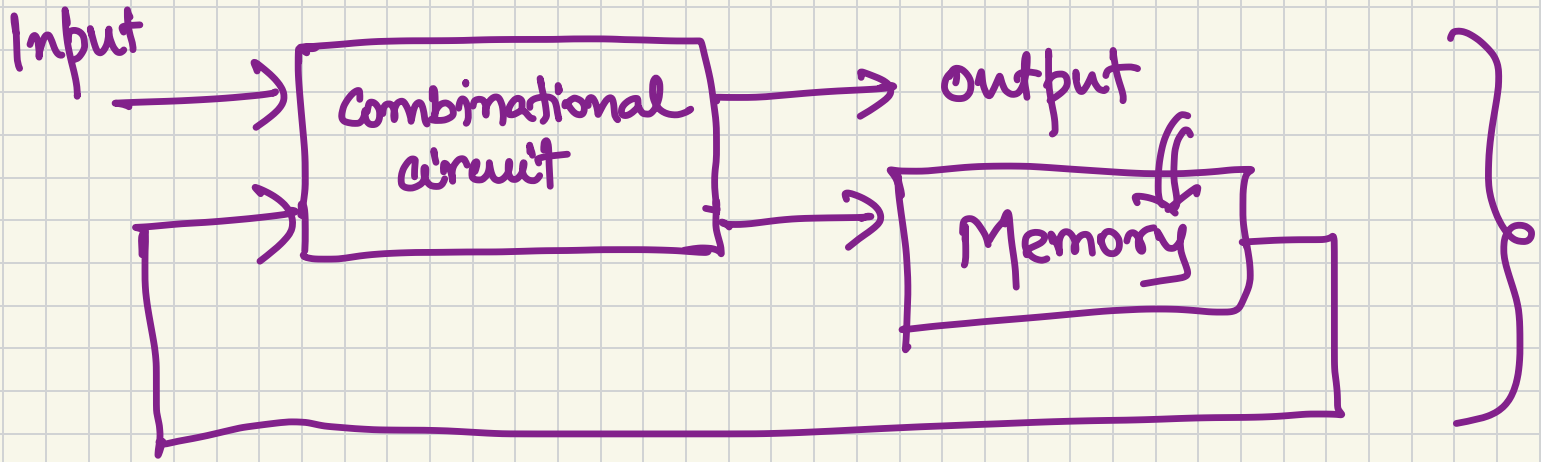
ACOL 215 (Oct. 29)

Synchronous Sequential Logic

Digital electronic devices have components that can store information.

In contrast, the circuits that we have seen so far have been **combinational**

↳ outputs depend only (and immediately) on the inputs.



Sequential circuit (Block diagrams)

Synchronous

It employs signals that affect the storage element at only discrete instants of time

Asynchronous

any time

&

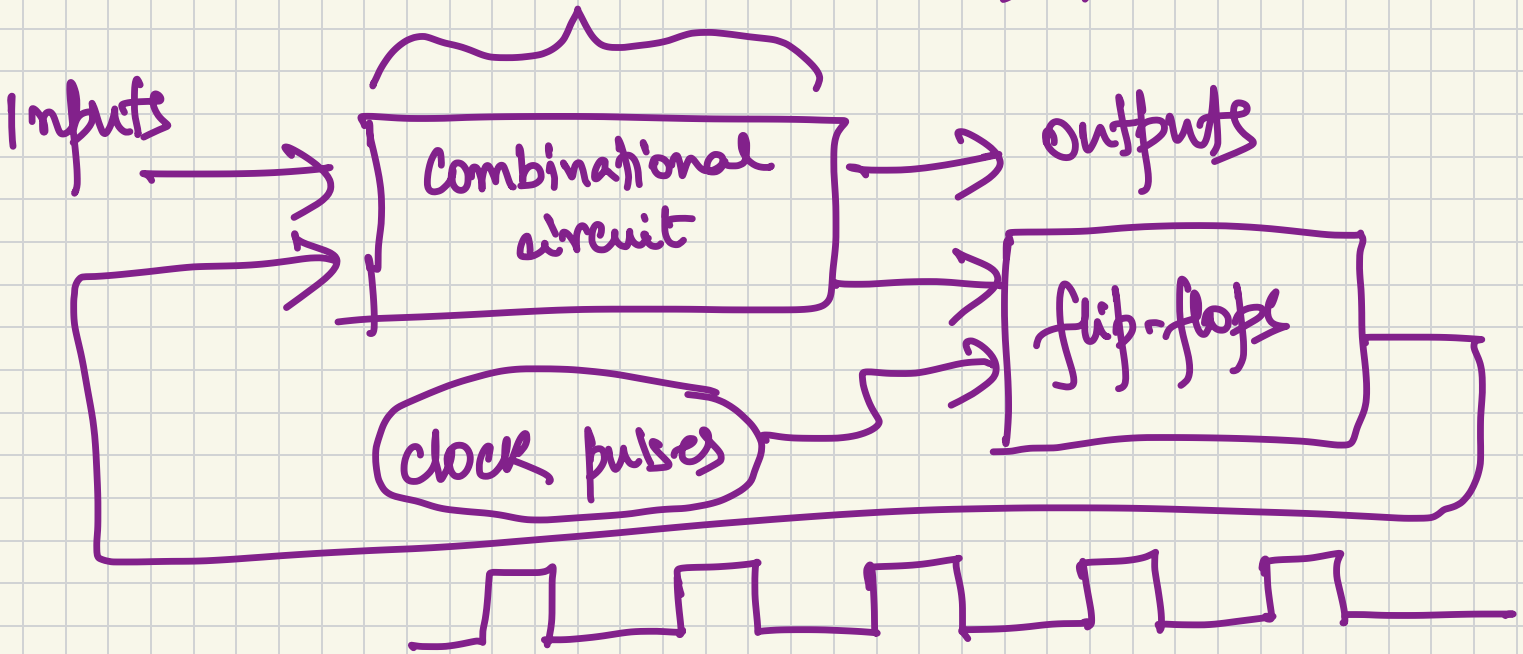
We will restrict ourselves to Synchronous sequential circuits.

↳ How is this synchronization achieved ?

→ through clock signals (clk)

clocked sequential circuits } || periodic sequence of clock pulses.

The storage element used in clocked sequential circuits are called flip-flops.



Timing diagram of clock pulses

Note that the speed at which the combinational circuit operates is critical.

If the clock pulses arrive at regular intervals, the combinational circuit must respond to a change in the state of the flip-flop in time (to be updated before the next pulse arrives)

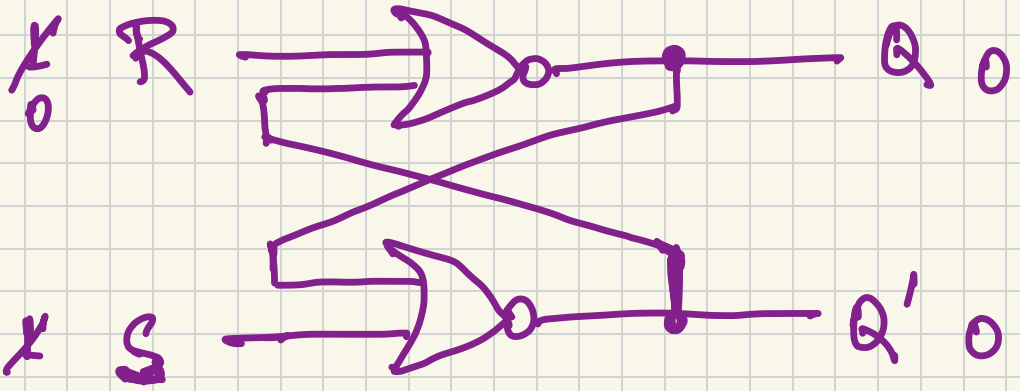
Therefore, propagation delay plays an important role in determining the interval between clock pulses.

Storage elements : Latches

are the basic circuit from which flip-flops are constructed.

SR Latch

→ circuit with two cross-coupled NOR gates
(or two cross-coupled NAND gates)



SR Latch has two useful states

$Q = 1 \; ; \; Q' = 0$

set state

$Q = 0 \; ; \; Q' = 1$

reset state

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

What happens when $S = 1$, $R = 1$?

$Q = 0 \; ; \; Q' = 0$

After this when the inputs are removed ($S = 0, R = 0$) →

→ $Q = 0 \; ; \; Q' = 1$

→ $Q = 1 \; ; \; Q' = 0$

$S = 1$; $R = 0$

$Q = 1$; $Q' = 0$

↳ inputs are removed ($S = 0$; $R = 0$)

$\boxed{Q = 1 \text{ ; } Q' = 0}$ → remains in memory

$S = 0$; $R = 1$

$Q = 0$; $Q' = 1$

↳ when the inputs are removed now ($S = 0$, $R = 0$)

$\boxed{Q = 0 \text{ ; } Q' = 1}$ → remains in memory

What happens when S=1, R=1 ?

Q=0 ; Q'=0

(after this when the inputs are removed

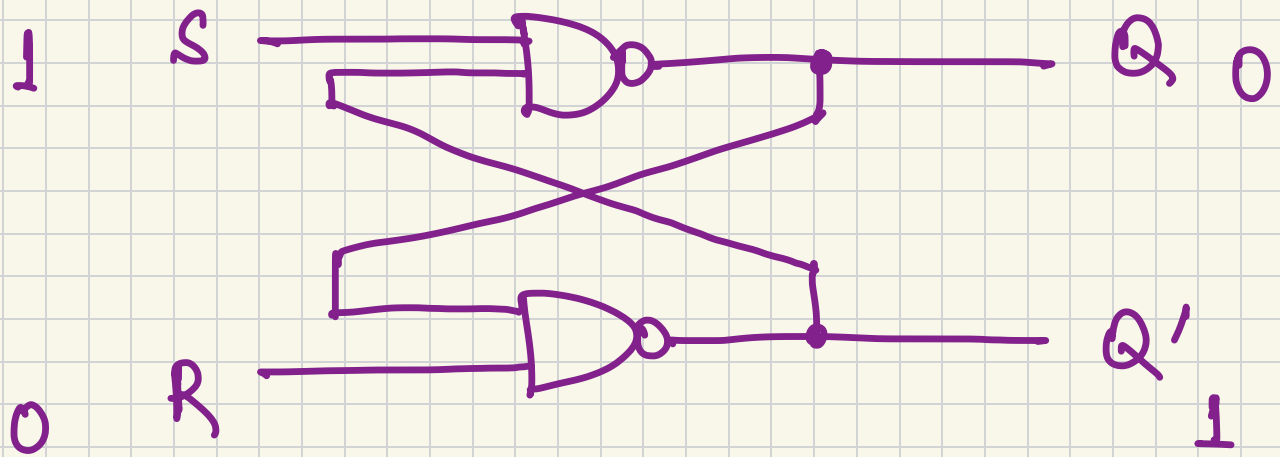
(S=0, R=0) → Q=0 ; Q'=1

→ Q=1 ; Q'=0)

Therefore, setting both S and R to 1 is forbidden.

S	R	Q	Q′	
1	0	1	0	
0	0	1	0	(after S=1, R=0)
0	1	0	1	
0	0	0	1	(after S=0, R=1)
1	1	0	0	(forbidden)

SR latch with NAND gates



Exercise

Verify

S	R	Q	Q'
1	0	0	1
1	1	0	1

(after S=1, R=0)

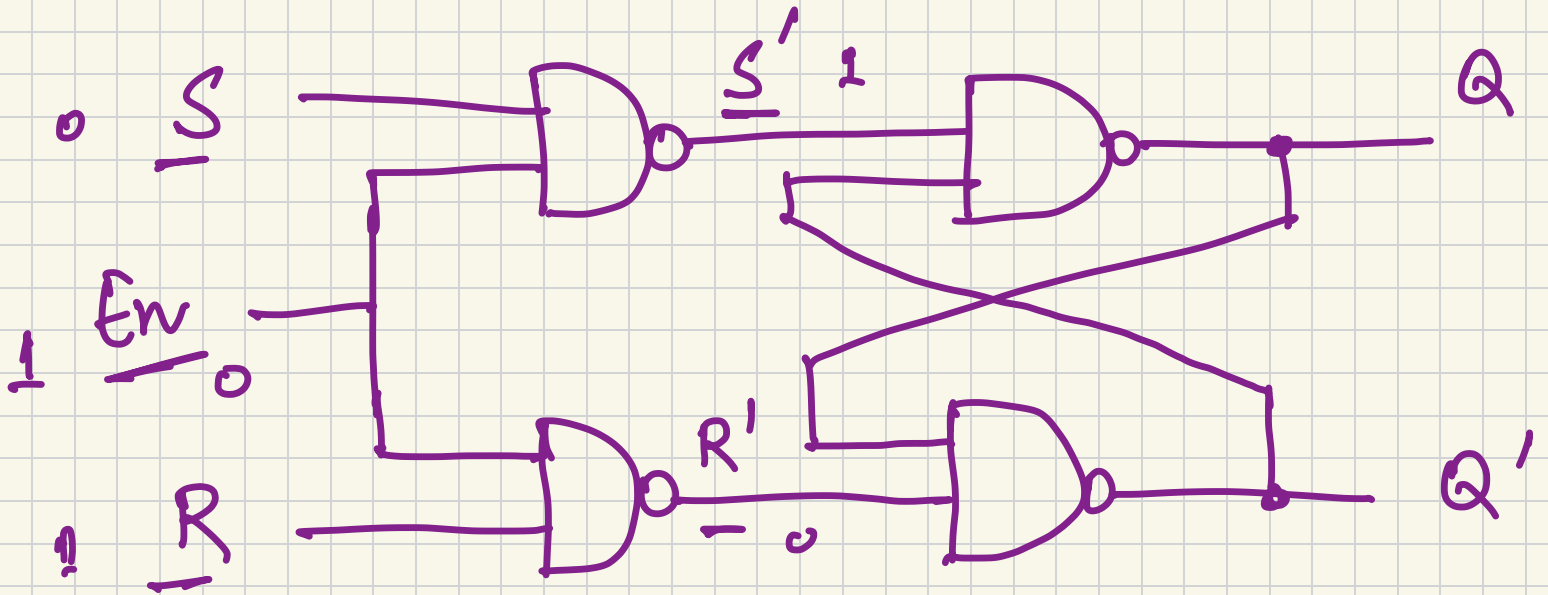
S	R	Q	Q'
0	1	1	0
1	1	1	0

(after S=0, R=1)

S	R	Q	Q'
0	0	1	1

(forbidden)

SR latch with control input



When En = 0, there is no change in Q and Q'

When En = 1, we are effectively having S' and R' after the first-level NAND gates

En	S	R	
1	0	0	No change
1	0	1	Q = 0, Q' = 1
1	1	0	Q = 1, Q' = 0
1	1	1	forbidden