ACOL 215

(Sept. 21st)

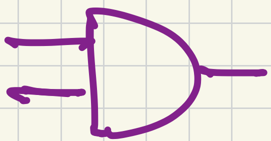
x	y	x AND y	x OR y	x XOR y (x OR y, but not both)
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	1	0

x	y	NOR (NOT-OR) $(x \downarrow y)$	NAND (NOT-AND) $(x \uparrow y)$
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0

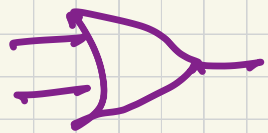
$x \uparrow y$

x	y	F (constant function)	F'	Equivalence (NOT-XOR)
0	0	0	1	1
0	1	0	1	0
1	0	0	1	0
1	1	0	1	1

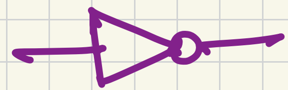
(Exclusive-NOR)



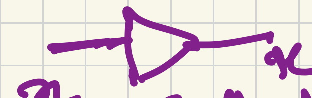
AND



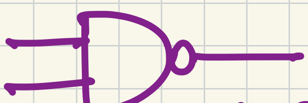
OR



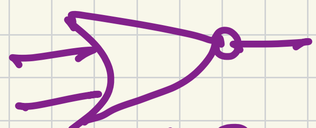
NOT



(Buffer)

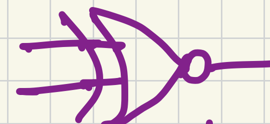


NAND



NOR

XOR



Equivalence

Extension to multiple inputs

A gate can be extended to multiple inputs if the binary operation that it represents is commutative and associative.

NAND and NOR are commutative but not associative.

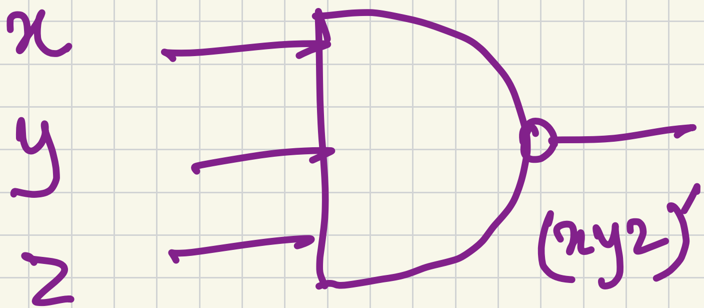
$$(x \downarrow y) \downarrow z = ((x+y)' + z)'$$
$$= ((x+y)')' \cdot z'$$
$$= (x+y) \cdot z' = xz' + yz'$$
$$x \downarrow (y \downarrow z) = (x + (y+z)')'$$
$$= x' \cdot (y+z)$$
$$= x'y + x'z$$

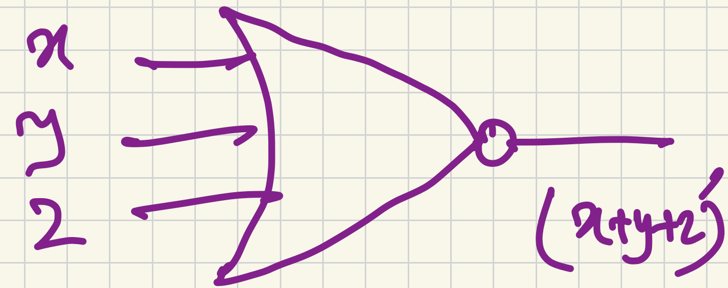
Therefore, we define multiple NOR gate as a complemented OR gate.

$$x \downarrow y \downarrow z = (x+y+z)'$$

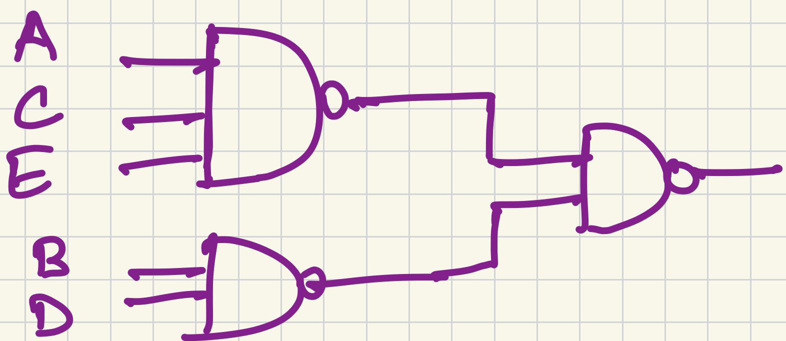
Similarly we define multiple NAND gate as a complemented AND gate.

$$x \uparrow y \uparrow z = (xyz)'$$





<u>Exercise</u> What is the Boolean function computed by this circuit?



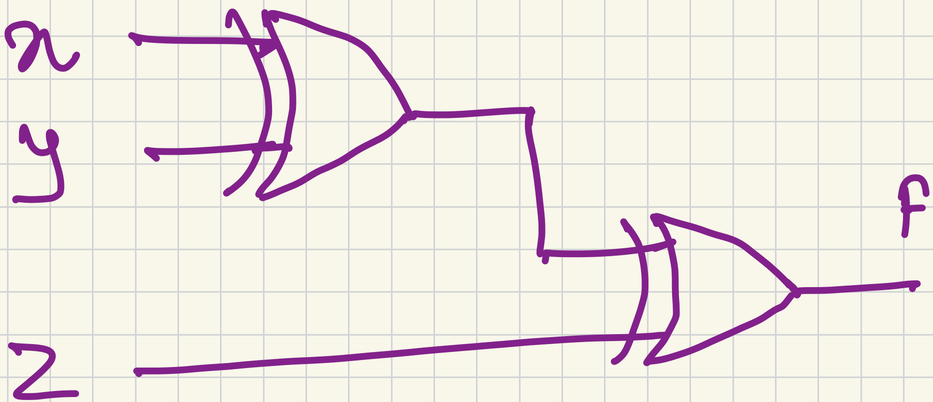
?

<u>ACE + BD</u>

What about XOR ?

" " " " XNOR ?

Commutative and associative



$F = (x \oplus y) \oplus z$

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Exclusive-OR is an odd function (equals 1 if the input variables have an odd number of 1's).

Positive and Negative Logic

Hardware digital gates are defined in terms of signal values — H and L.

Two signal values → two logic values

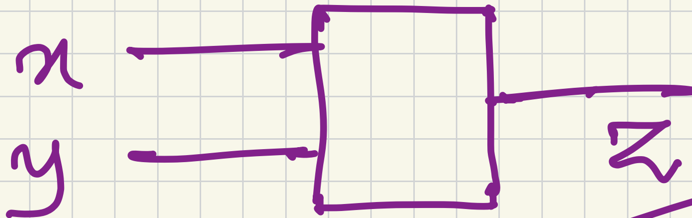
1 → H
0 → L

positive logic system

0 → H
1 → L

negative logic system

Consider the electronic gate

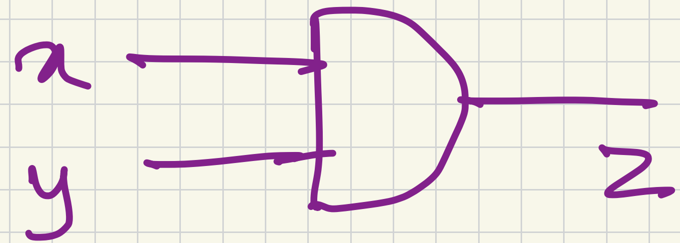


The "physical behaviour" of this gate is specified as

x	y	z
L	L	L
L	H	L
H	L	L
H	H	H

If you assume a positive logic system (assignment) then we get the following behaviour

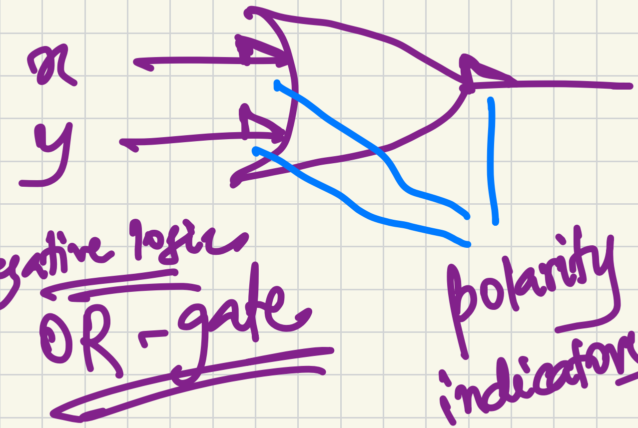
x	y	z
0	0	0
0	1	0
1	0	0
1	1	1



AND gate

If, however, we assume a negative logic system (assignment) then we get the following behaviour.

x	y	z
1	1	1
1	0	1
0	1	1
0	0	0



Negative logic OR-gate

Exercise

Implement the Boolean function

$$F = xz + x'z' + x'y$$

with i) NAND and NOT (inverter) gates

ii) NOR and NOT (inverter) gates

To be discussed in the next class

Integrated Circuits

called a chip || An IC is fabricated on a die of a silicon semiconductor crystal

on a microchip

Digital ICs are categorized in terms of complexity of their circuits (the number of logic gates in a single package)

Small-scale integration circuits

(SSI) ~ 10 gates in a style package

Medium | MSI (~10-1000 gates)

Large | LSI (several thousand gates)

Very large VLSI (millions of gates)

Ultra large ULSI (— " —)

Digital ICs are also classified by the specific circuit technology to which they belong.

digital logic family

Some of the popular ones include

standard || TTL Transistor - transistor logic

high speed || ECL Emitter - coupled logic

high component density || MOS Metal - oxide semiconductor

low power || CMOS Complementary "

CMOS is used in many handheld portable devices.

Exercise

Please read sect. 2.9 from the book.