ACOL 215 (Nov. 17th)

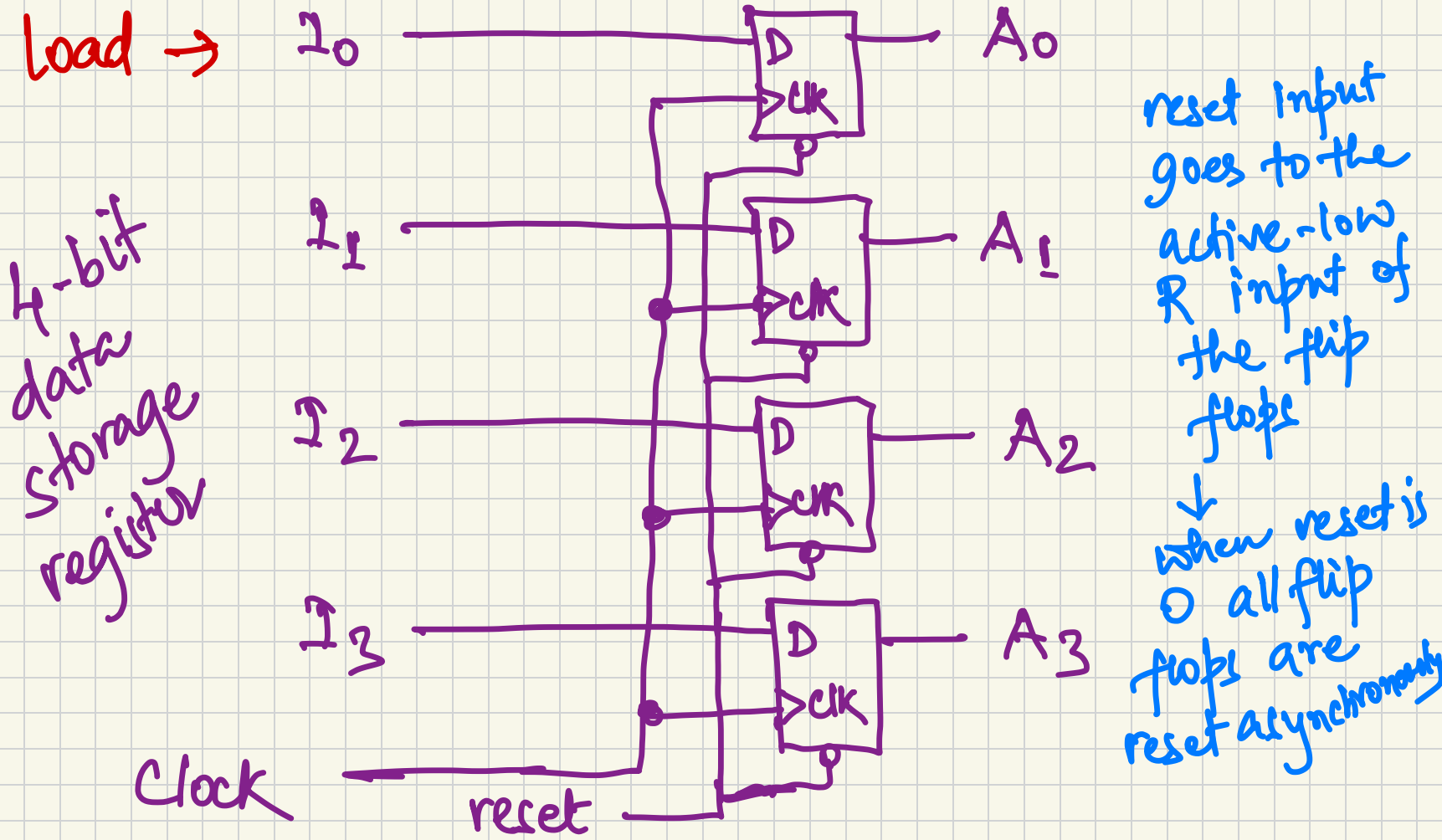
Clocked Sequential Circuits

→ Registers

→ Counters

Registers → group of flip flops connected by a common clock

→ each flip-flop can store one bit



4-bit data storage register

reset input goes to the active-low R input of the flip flops

↓

when reset is 0 all flip flops are reset asynchronously

The transfer of new inputs into a register is called "loading" the register.

↳ if all bits are loaded simultaneously, then it is said that the loading is done in parallel.

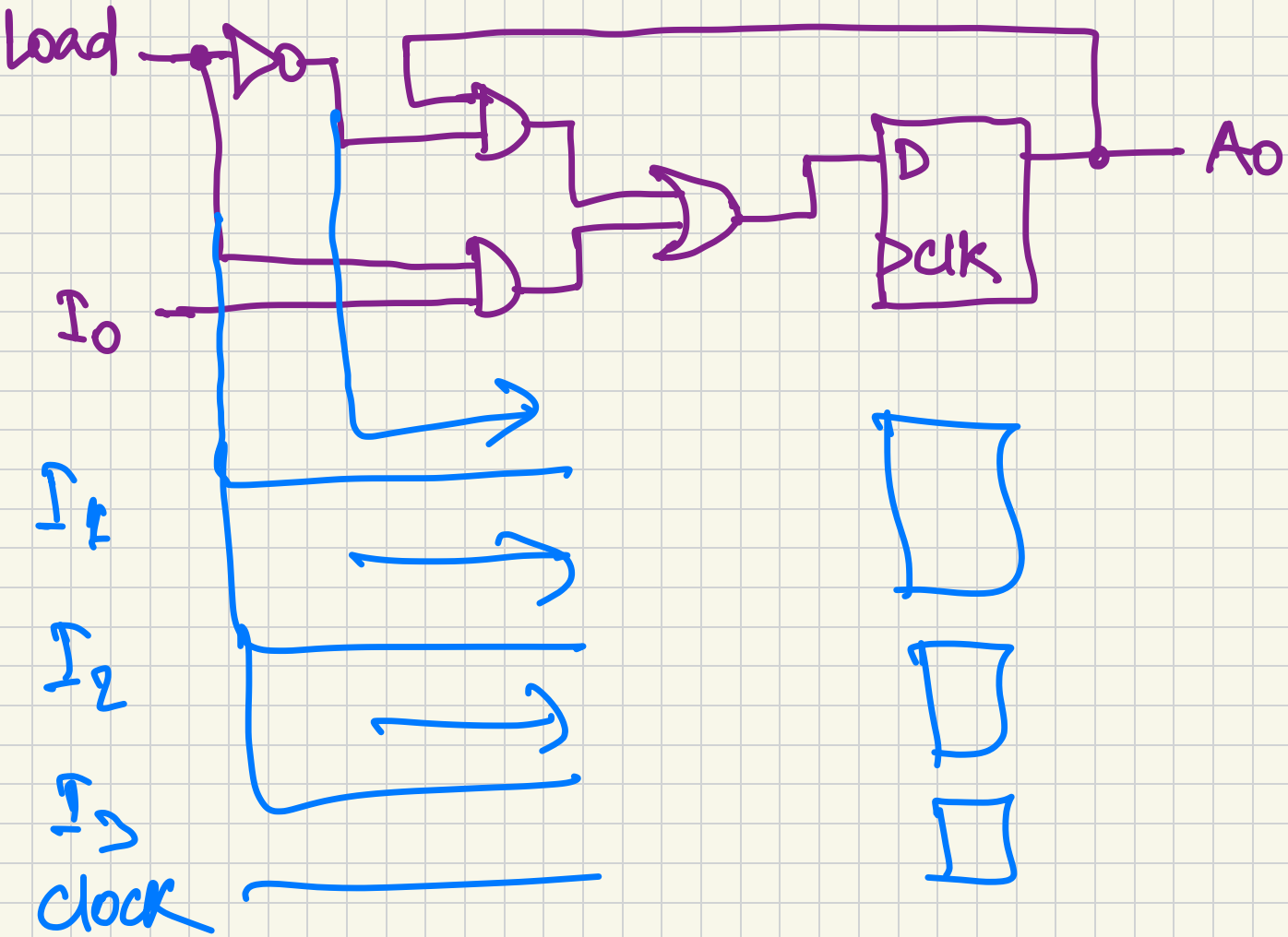
If the content of a register must be left unchanged, we must either

→ maintain the inputs

→ prevent the clock pulse from reaching the circuit.

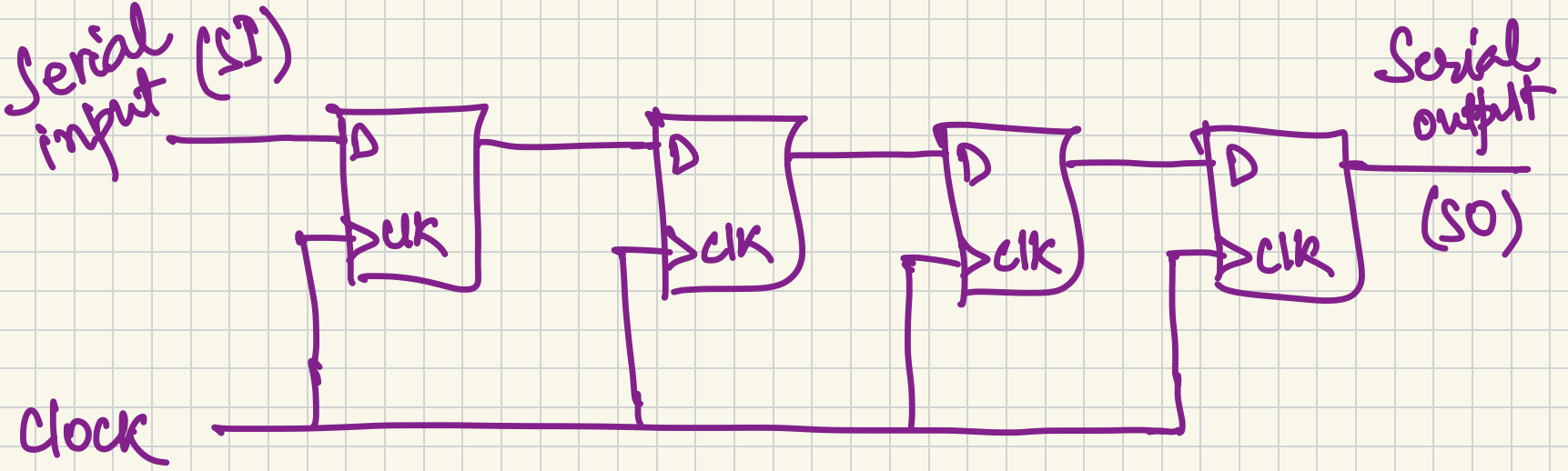
this can be done by clock gating → not a good idea

We will gate the data path instead

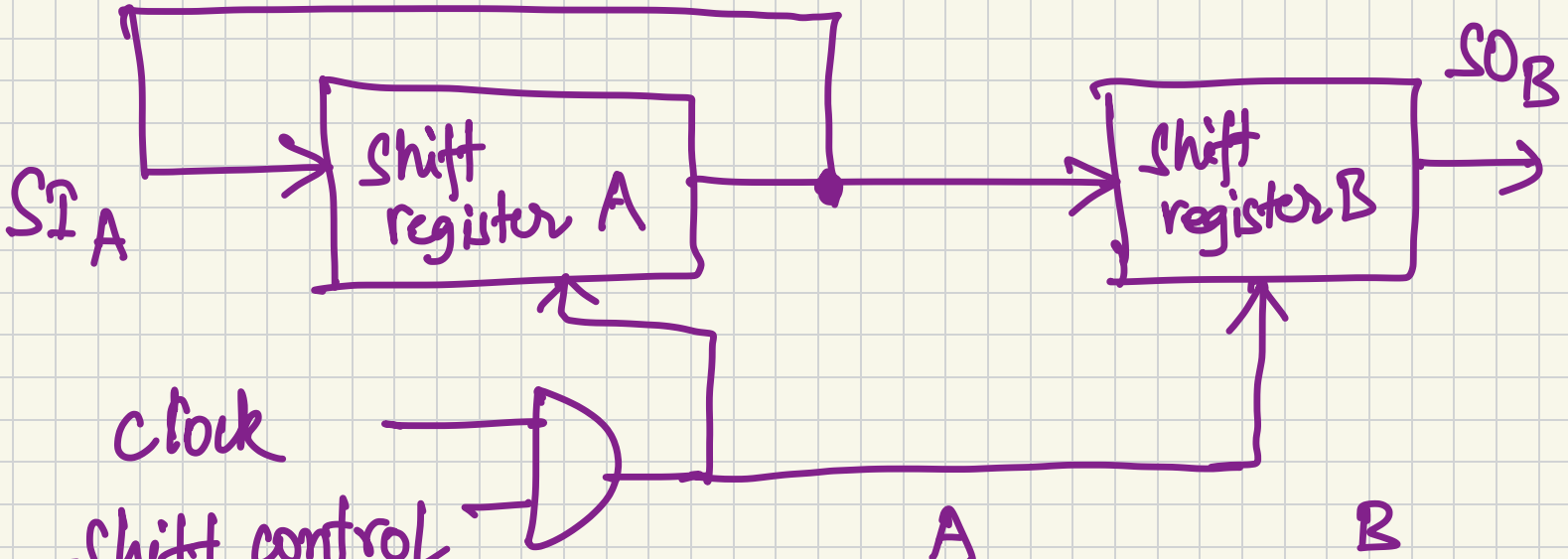

Load
I_0
D
Clk
A_0
I_1
I_2
I_3
clock

Shift Registers

A register capable of shifting the binary information held in each cell to its neighboring cell.

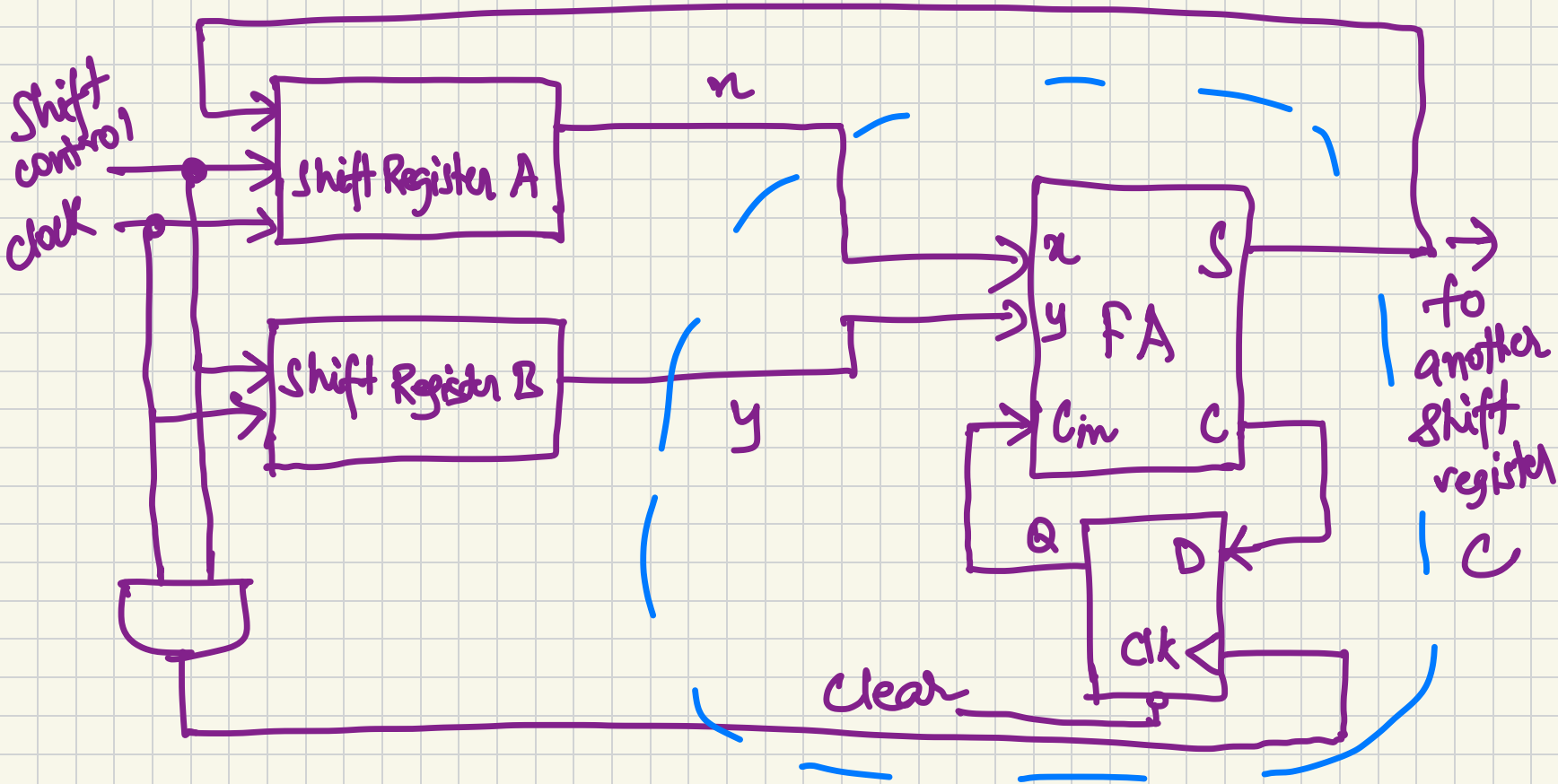


Serial Transfer



	A	B
Beginning	1011	0011
After 1st pulse	1101	1001
2nd pulse	1110	1100
3rd pulse	0111	0110
4th pulse	1011	1011

Serial Addition -

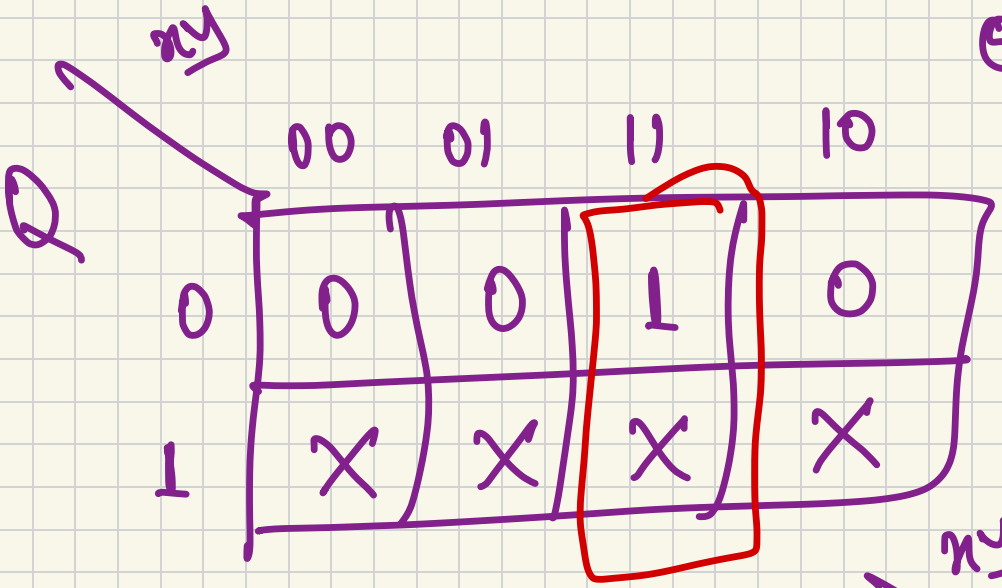


Serial Adder State Table

Present State	Inputs		Next state	Output	Flip-flop inputs	
Q	x	y	Q	S	J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

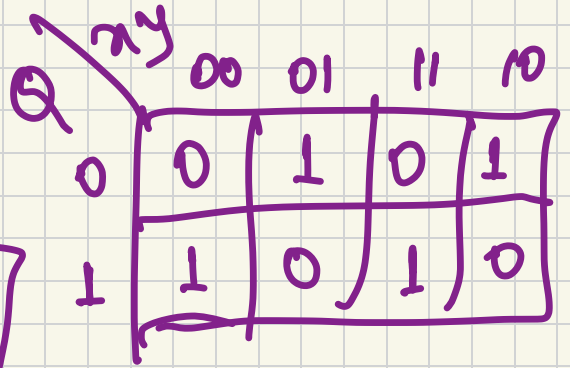
Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0



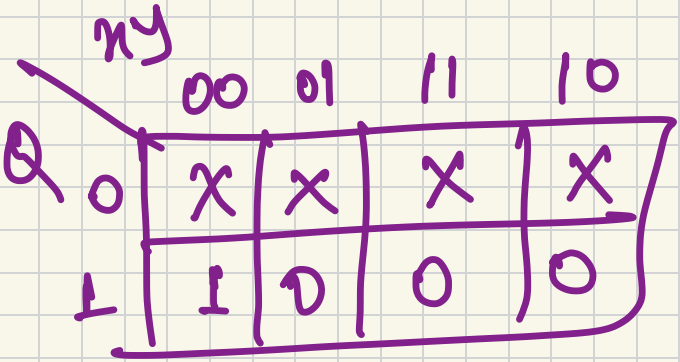
$J_Q = xy$

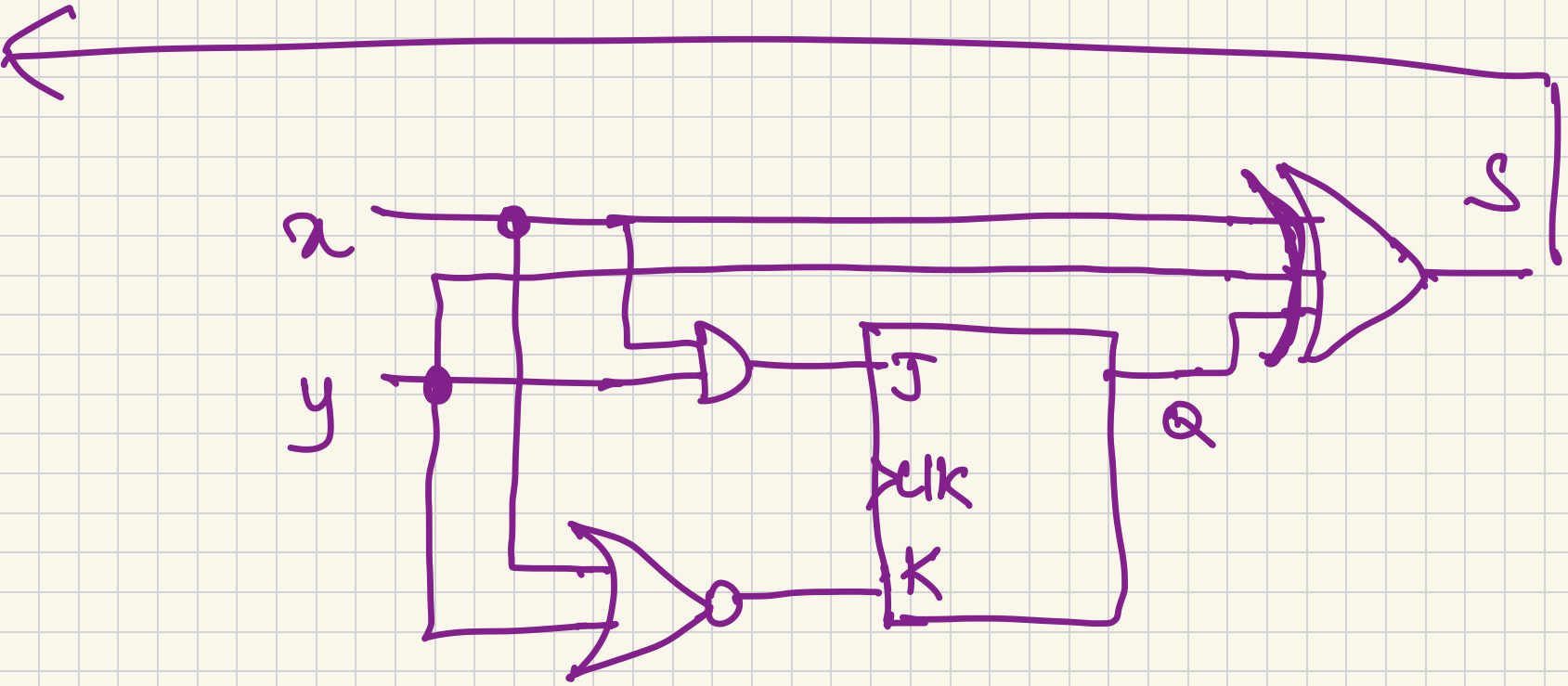
$K_Q = x'y'$

$= (x+y)'$



$C = Q \oplus x \oplus y$





Exercise → Implement using D flip flop.