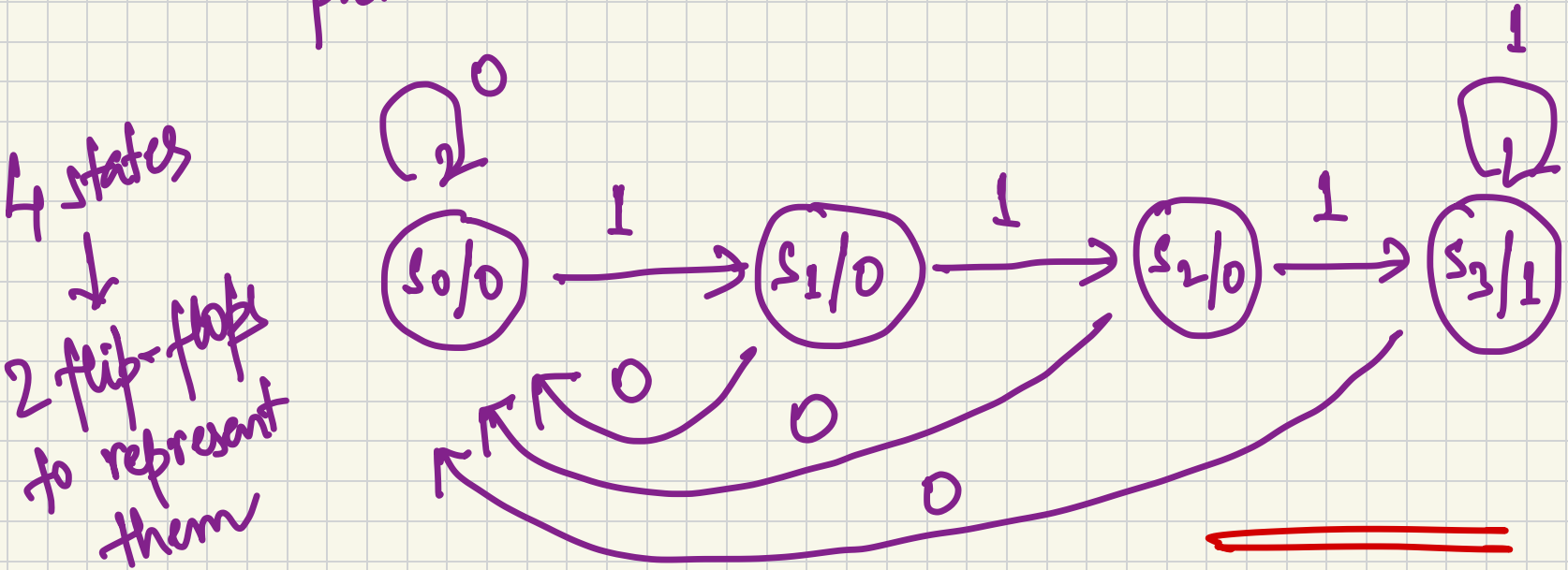
ACOL 215 (12th Nov.)

Designing Clocked Sequential Circuits

Set of specifications → Logic diagram

↓ State tables/ State diagrams ↗

Suppose we wish to design a circuit that detects a sequence of three or more consecutive 1's in an input bitstream.



State table

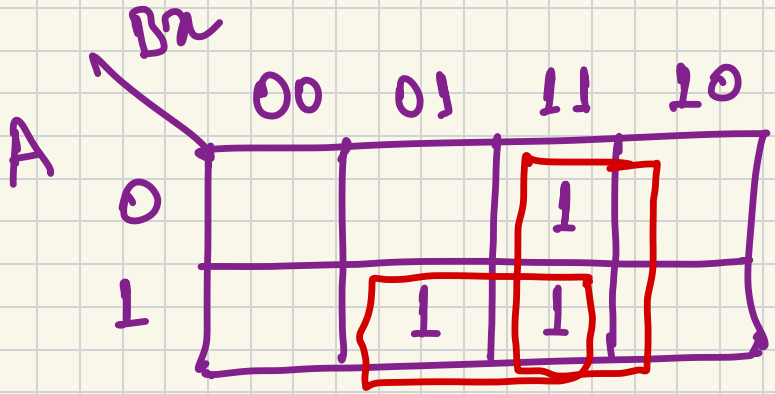
Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

With a D flip flop, we know that

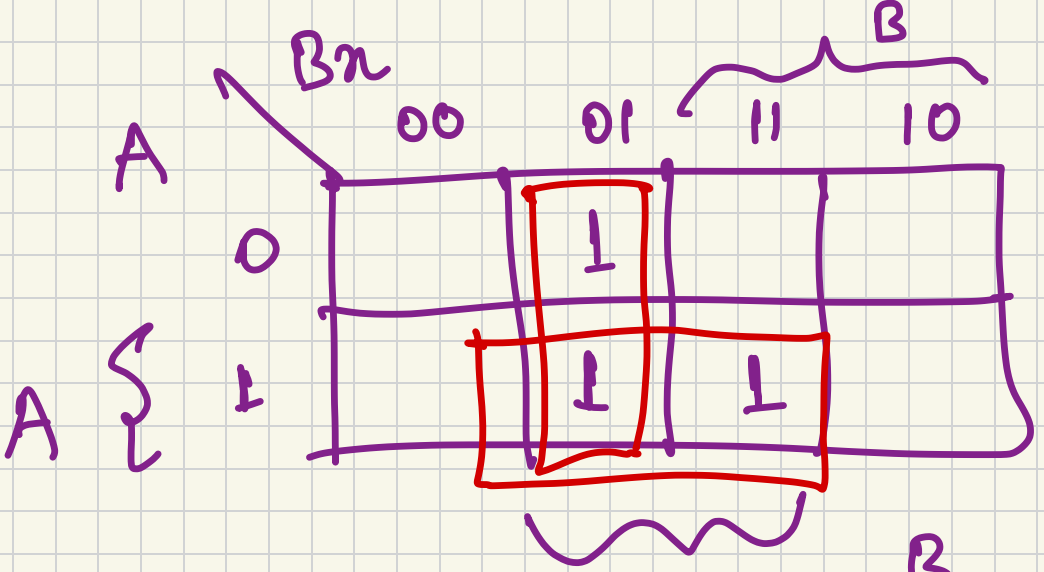
$$A(t+1) = D_A(A,B,x) = \Sigma(3,5,7)$$

$$B(t+1) = D_B(A,B,x) = \Sigma(1,5,7)$$

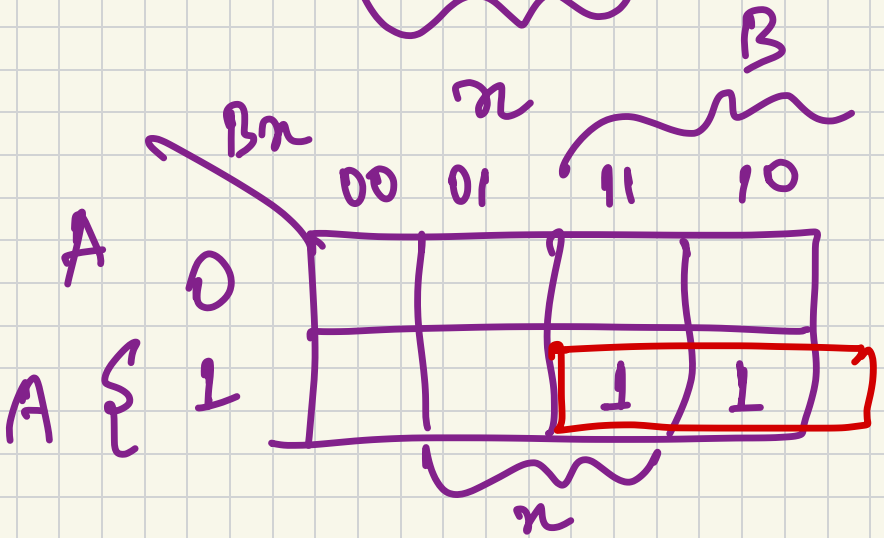
$$y(A,B,x) = \Sigma(6,7)$$



$$D_A = Ax + Bx$$

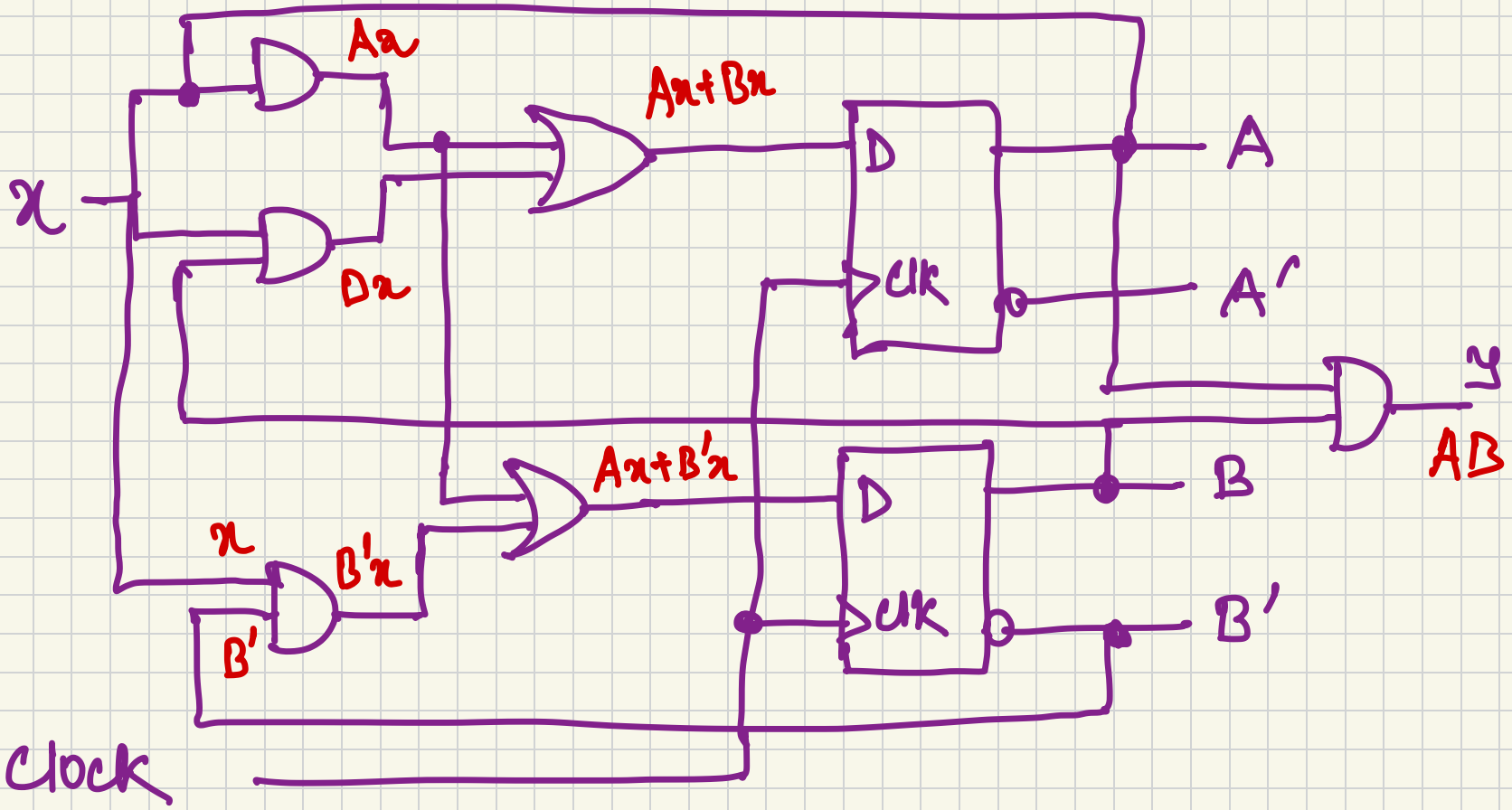


$$D_B = Ax + B'x$$



$$y = AB$$

$D_A = Ax + Bx$; $D_B = Ax + B'x$; $y = AB$



Recall the JK and T flip-flop characteristic tables

J	K	Q(t+1)
0	0	Q(t)
0	1	0 (reset)
1	0	1 (set)
1	1	Q'(t)

T	Q(t+1)
0	Q(t)
1	Q'(t)

From the characteristic tables, we can get the following excitation tables

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

State table

Present State		Input	Next State		Output	Flip-flop inputs			
A	B	x	A	B	y	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	0	X	1	X
0	1	0	0	0	0	0	X	X	1
0	1	1	1	0	0	1	X	X	1
1	0	0	0	0	0	X	1	0	X
1	0	1	1	1	0	X	0	1	X
1	1	0	0	0	1	X	1	X	1
1	1	1	1	1	1	X	0	X	0

J_A

A \ Bx	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_A = Bx$

K_A

A \ Bx	00	01	11	10
0	X	X	X	X
1	1	0	0	1

$K_A = x'$

J_B

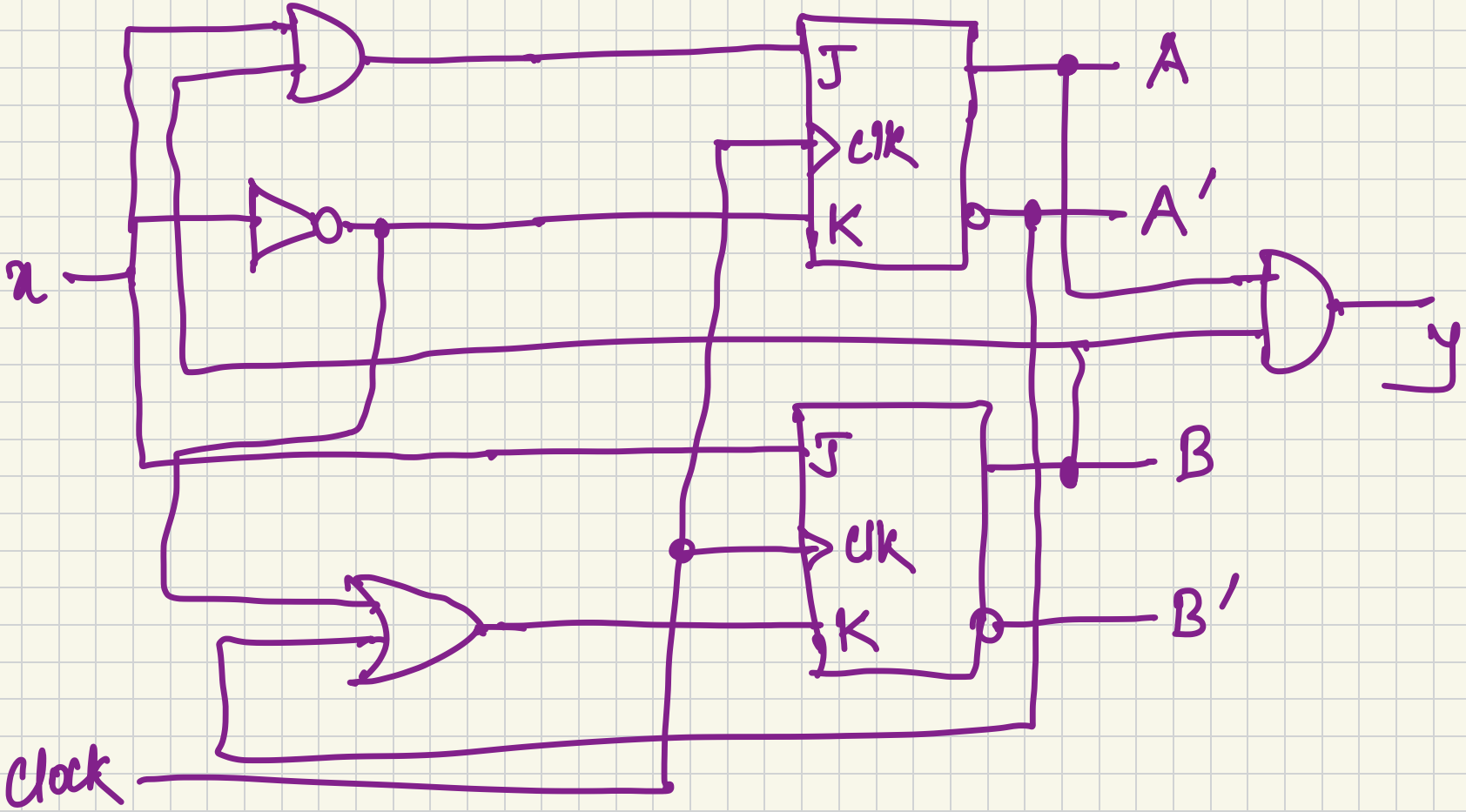
A \ Bx	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$J_B = x$

K_B

A \ Bx	00	01	11	10
0	X	X	1	1
1	X	X	0	1

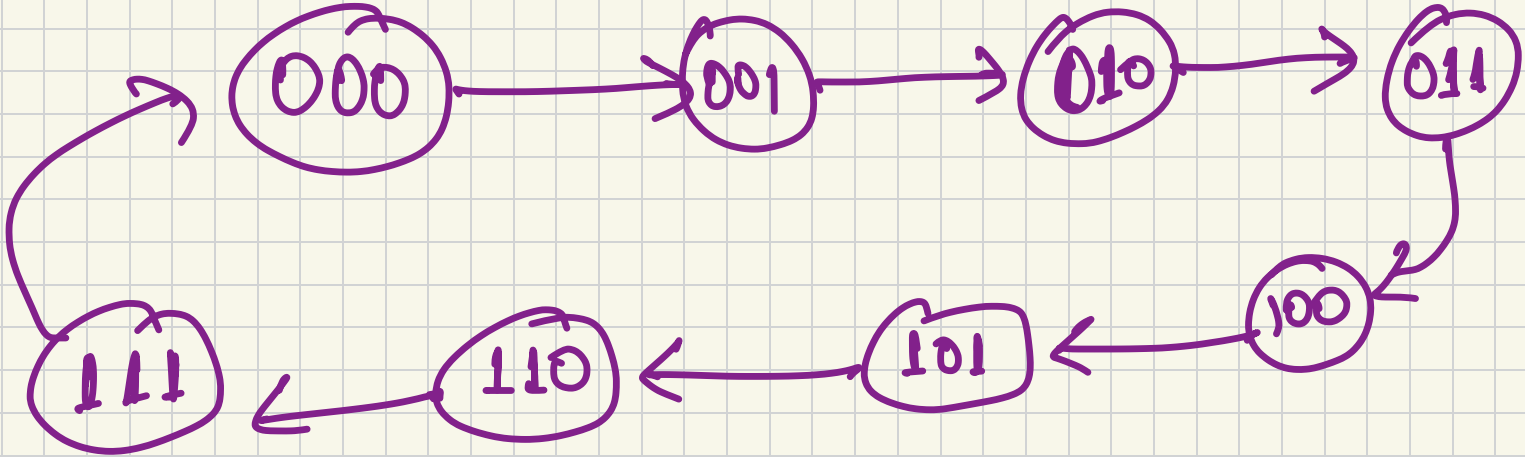
$K_B = x' + A'$


x
J
Clk
K
A
A'
y
J
Clk
K
B
B'
Clock

Synthesis with T flip flops

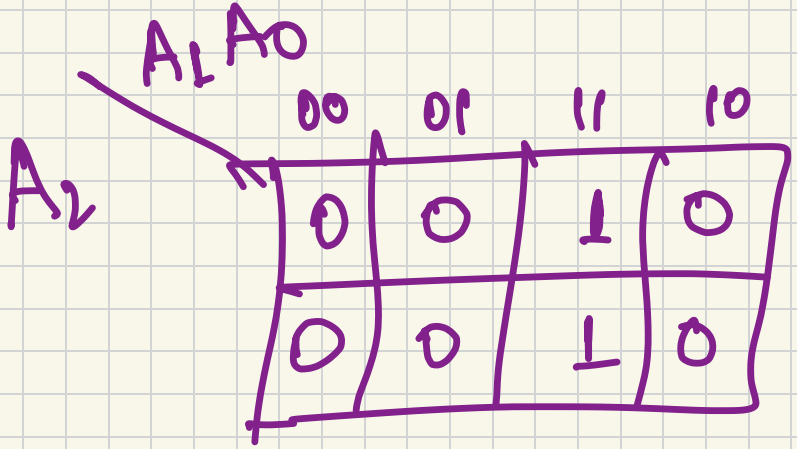
n-bit binary counter

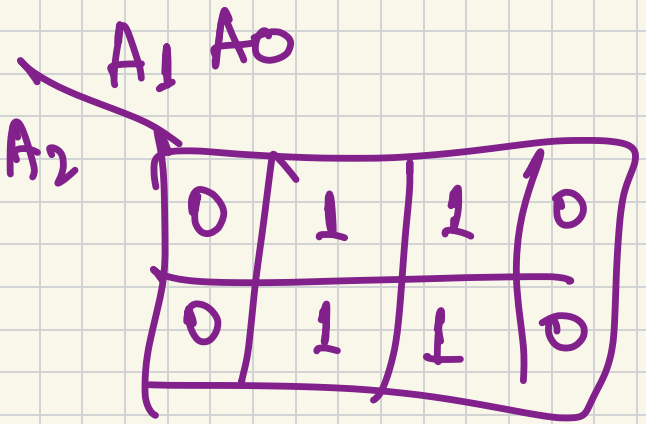
→ 0 to $2^n - 1$



State Table

Present state			Next state			Flip-flop inputs		
A_2	A_1	A_0	A_2	A_1	A_0	TA_2	TA_1	TA_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

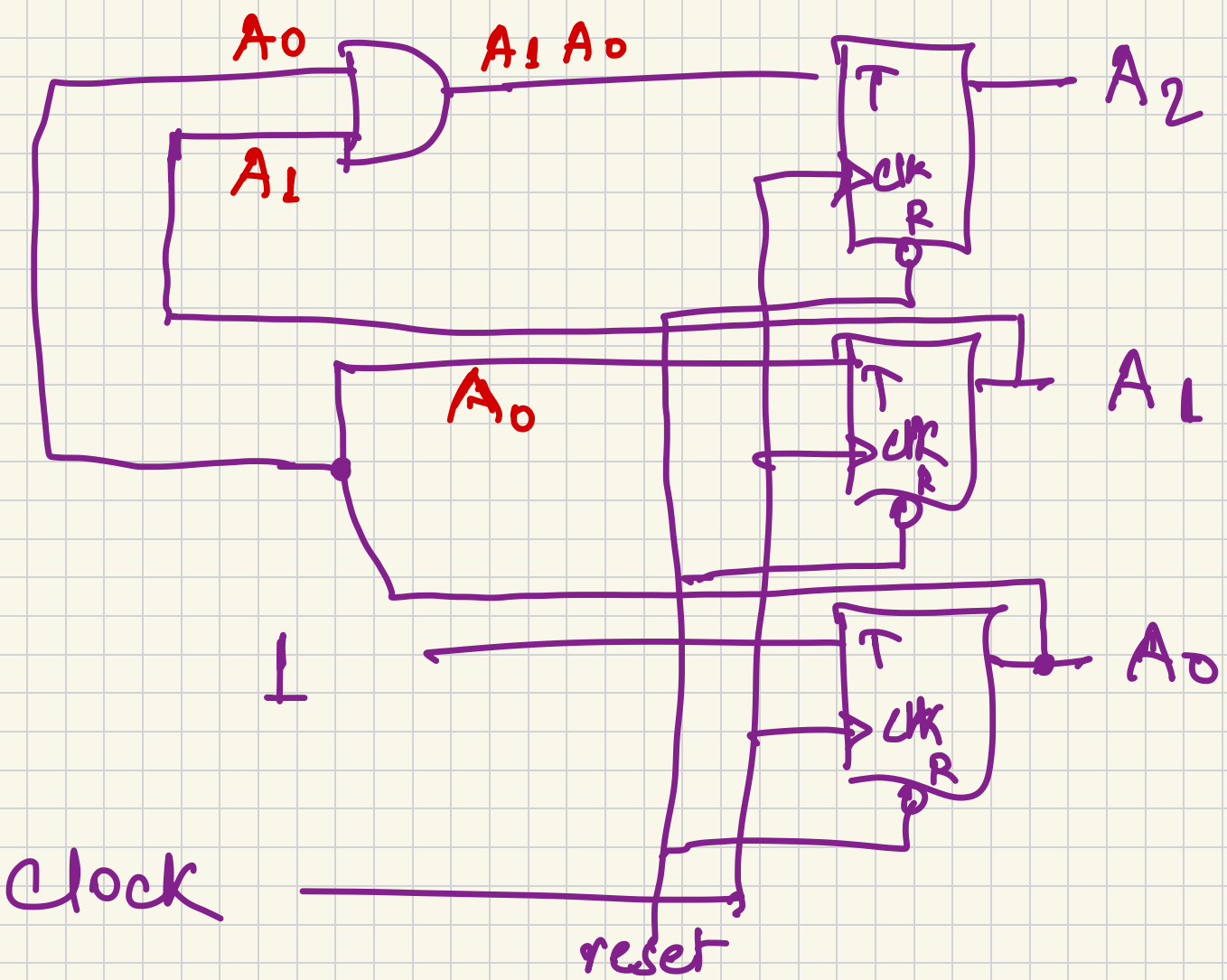




$$T_{A_2} = A_1 A_0$$

$$T_{A_1} = A_0$$

$$T_{A_0} = 1$$


A0
A1 A0
A1
T
CLK
R
A2
A0
T
CLK
R
A1
1
T
CLK
R
A0
Clock
reset

Exercise Synthesize a circuit for the given state table using JK flip-flops.

Present State		Input	Next state	
A	B	x	A	B
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0