

ACOL 215

(04 Nov.)

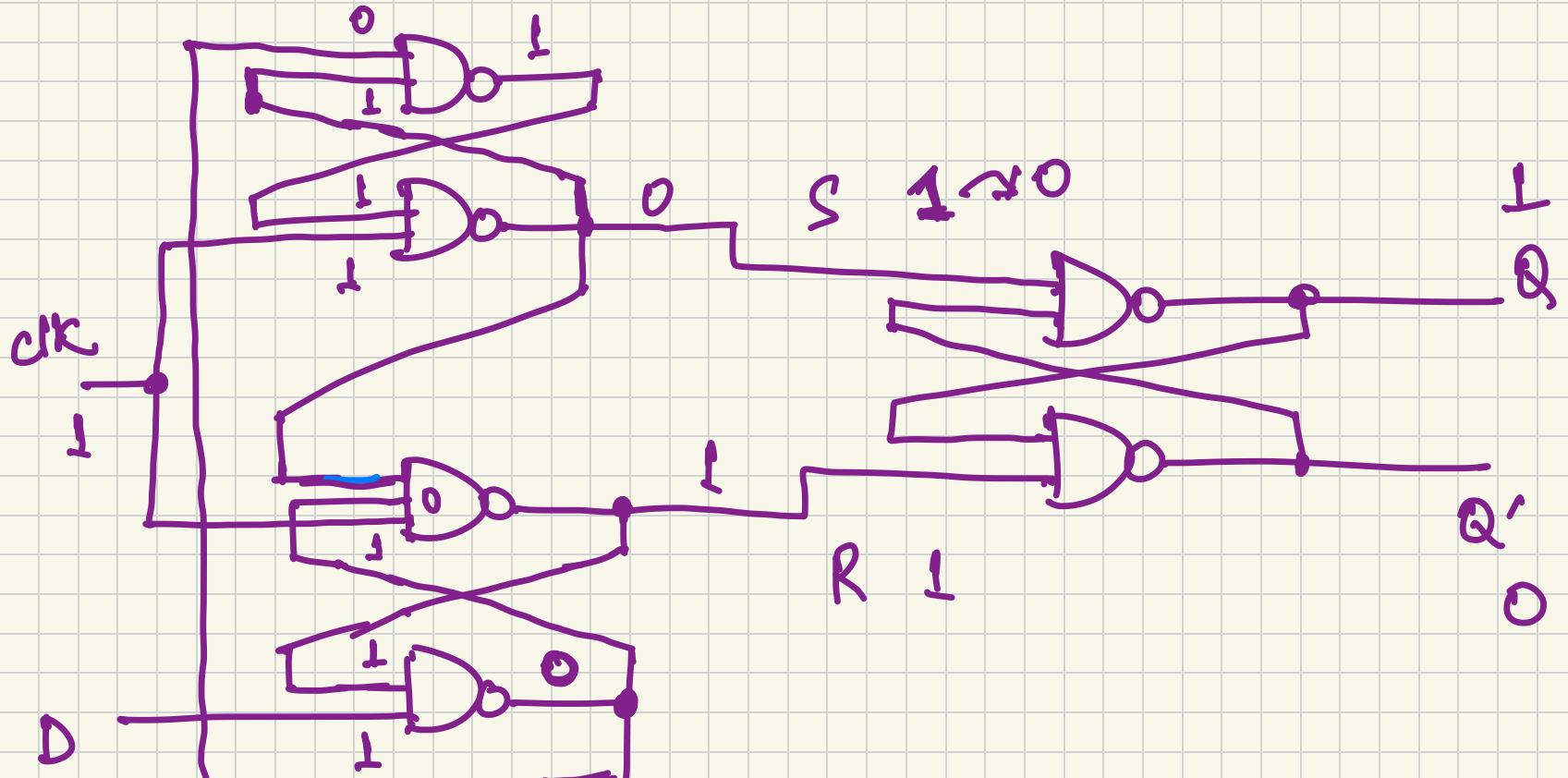
flip-flops are constructed in such a way that they operate properly when they are part of a sequential circuit that uses a common clock.

Two ways to modify a latch to a flip-flop

isolate the output
and prevent it from being
affected while the input is changing

leader - follower

produce a flip-flop
that triggers
only during
a signal transition



$\frac{1}{0}$ → nothing changes at the output

The S-R inputs of the output latch are maintained at logic-1 level when $\text{CLR} = 0$.

Therefore, the outputs remain in their present state.

What happens when CLR changes to 1?

If $D = 0$ when CLR becomes 1

$\rightarrow R$ becomes 0 \leftarrow

\rightarrow flip-flop goes to reset state
making $Q = 0$

If D becomes 1 while the
 CLR remains at 1

→ R continues to be 0

→ S continues to be 1

→ therefore no change in output.

Similarly, if $D = 1$ when CLR becomes 1, R becomes 1; S changes to 0

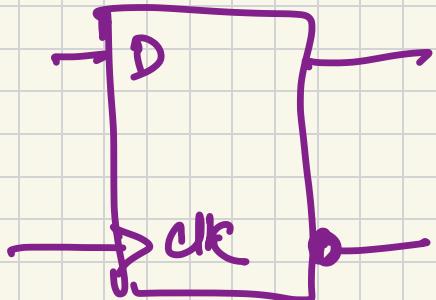
Flip-flop goes to the set state making $Q = 1$ ←

Note 1. When the input clock in the positive-edge triggered flip flop makes a positive transition, the value of D is transferred to Q.

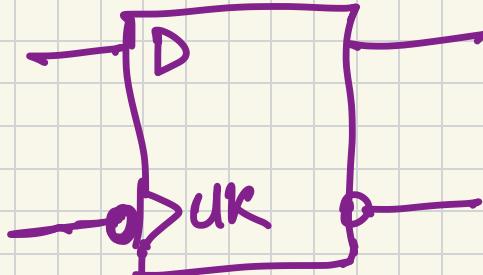
2. A negative transition of the clock does not affect the output.
3. Changes in D when the CLK is in the steady state (logic-1 / logic-0) does not affect the output.

Graphical symbols for edge-triggered

D flip-flop



Positive edge
triggered

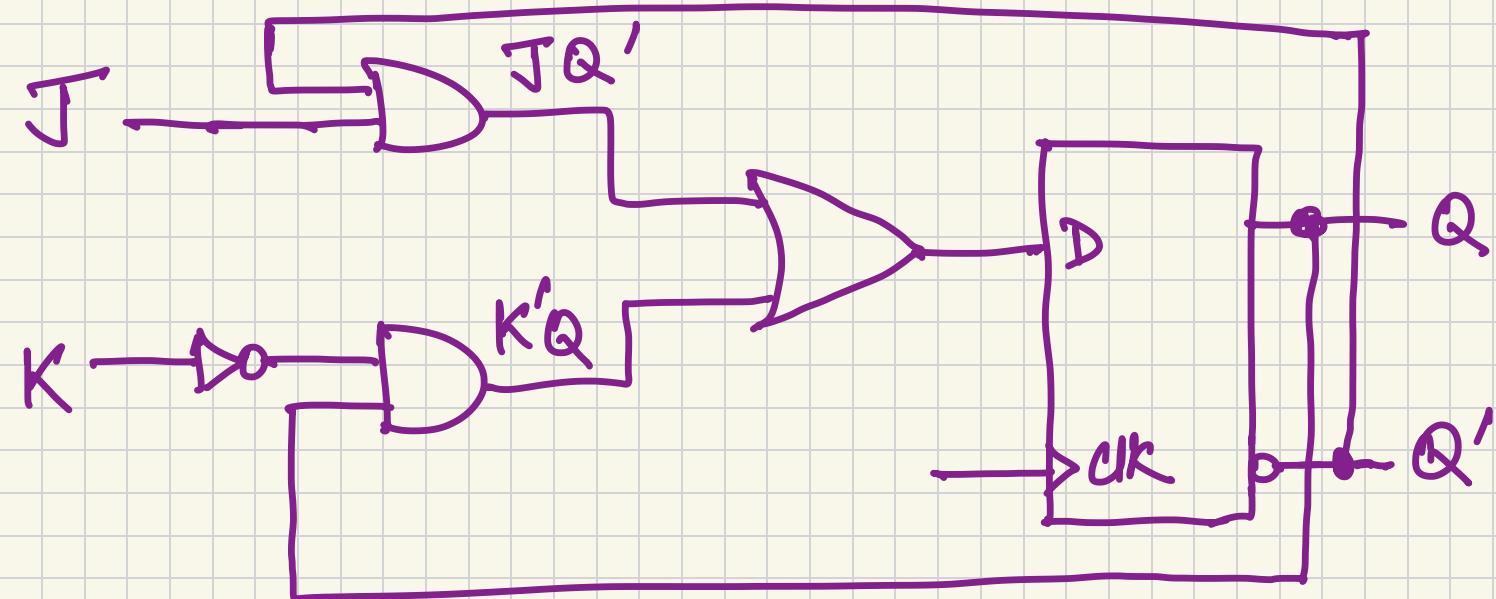


Negative-edge
triggered

setup time - min time for which D must be maintained at a constant value prior to the occurrence of the clock transition

hold time - min time for which D must not change after the positive clock transition.

JK flip flop



$$D = JQ' + K'Q$$

$$D = JQ' + K'Q$$

When $J=1, K=0$

$$D = 1$$

(next clock edge
sets $Q=1$)

$J=0, K=1$

$$D = 0$$

(next clock edge
set $Q=0$)

$J=K=1$

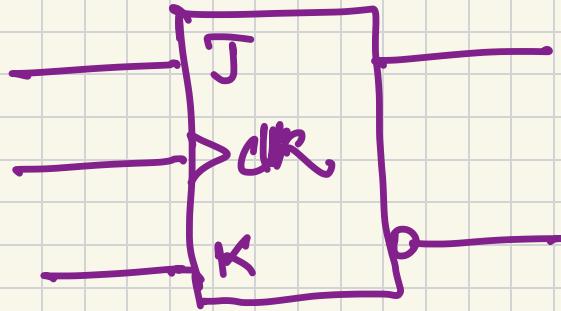
$J=K=0$

(next clock edge complements the output)

$$D = Q'$$

$$D = Q$$

(next clock edge does
not change the output)



Graphical symbol
for a JK flip
flop

T flip flop
(toggle)

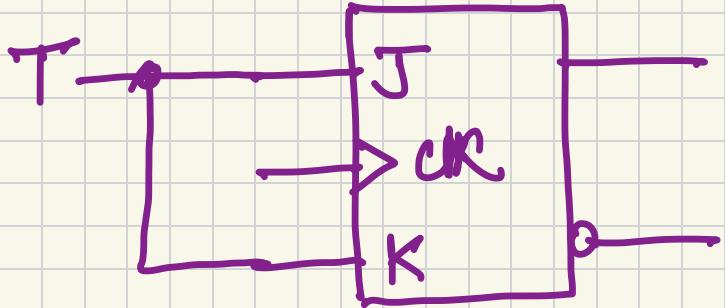
J and K are tied together

T = 0

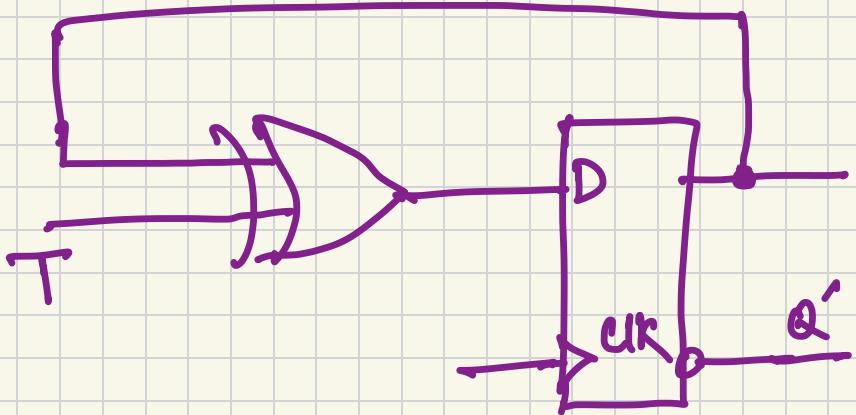
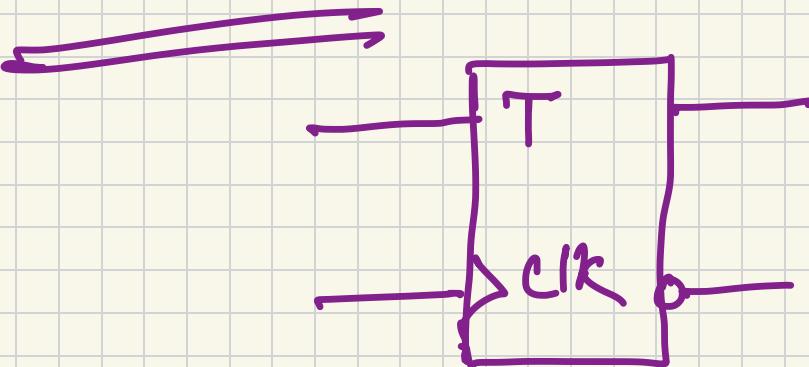
clock edge does not
change the output

T = 1

clock edge complements
the output



From JK flip flop



From D flip flop

graphical symbol

Characteristic Tables

D flip-flop

D	Q(t+1)
0	0
1	1

T flip-flop

T	Q(t+1)
0	Q(t)
1	$Q(t)'$

J-K flip flop

J	K
0	0
0	1
1	0
1	1

$Q(t+1)$
 No change
 reset
 set
 complement $Q(t)'$

$Q(t)'$

Characteristic equations

$$D = Q(t+1)$$

$$T \oplus Q(t) = Q(t+1)$$

$$\tau Q(t)' + \kappa' Q(t) = Q(t+1)$$