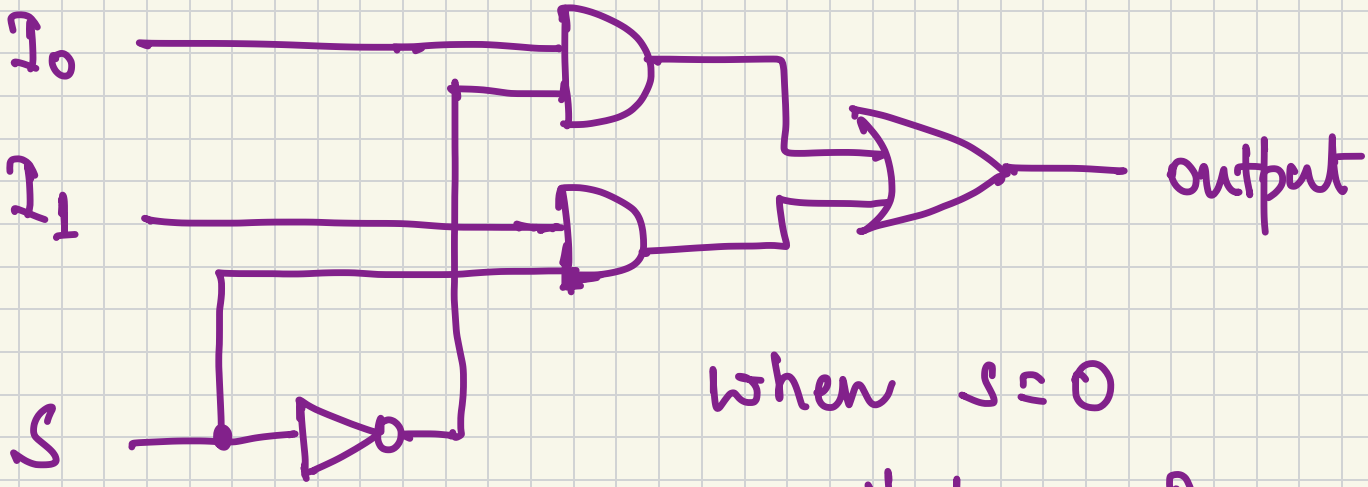
Multiplexers

ACOL215

(28th Oct.)

Combinational circuits that select binary information from one of many input lines and directs it to a single line.



(selection line)

when $S = 0$

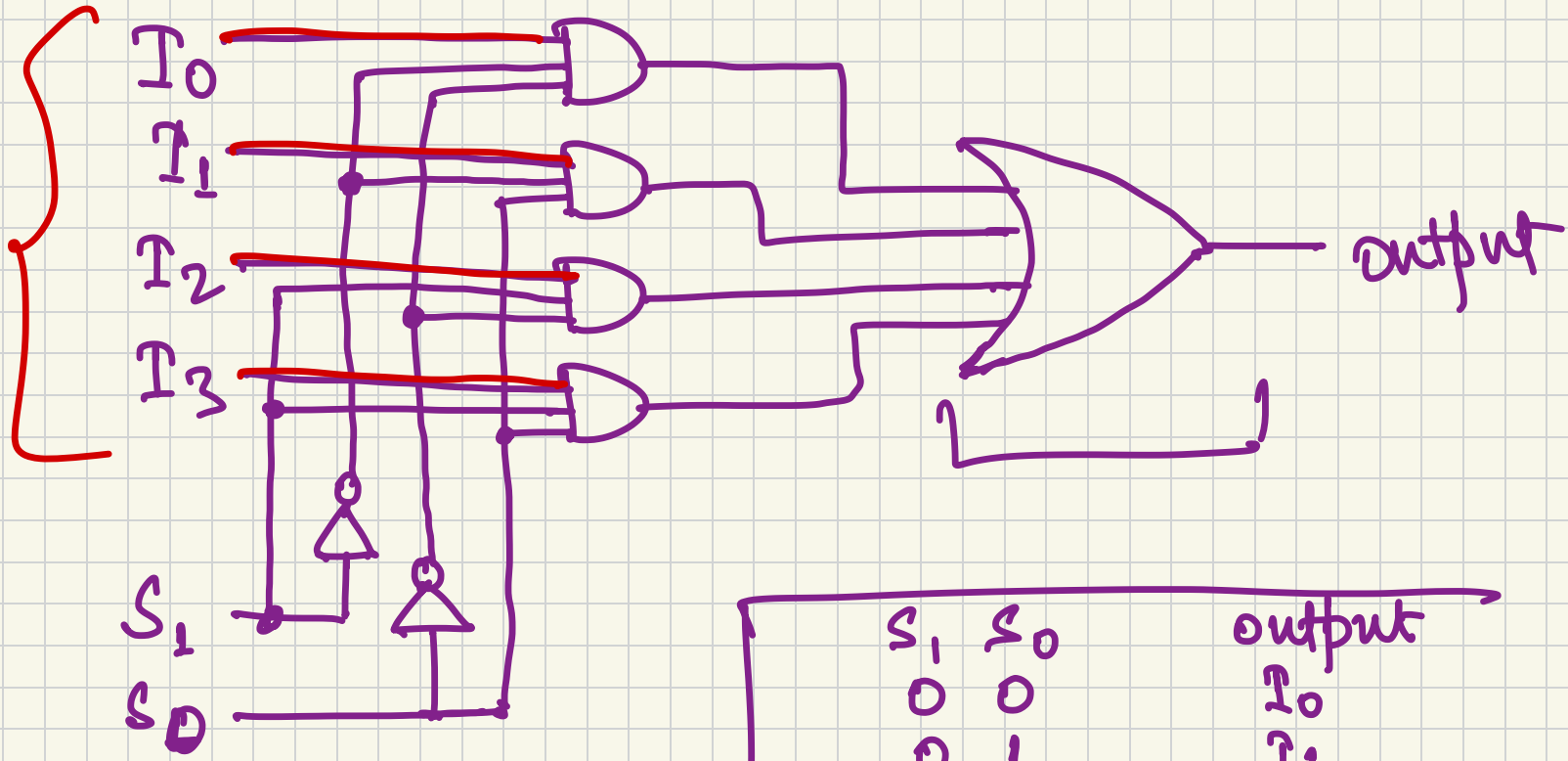
output = I_0

when $S = 1$

output = I_1

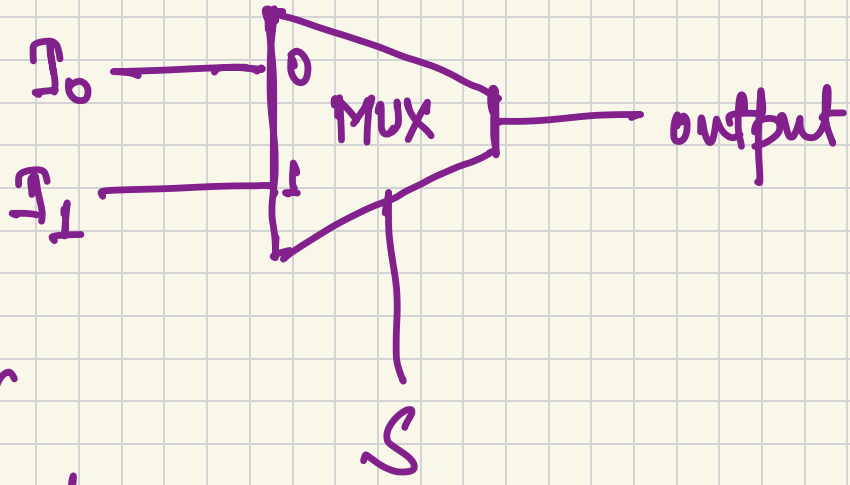
Two-to-one line multiplexer

Four-to-one line multiplexer



S_1	S_0	output
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Block diagram



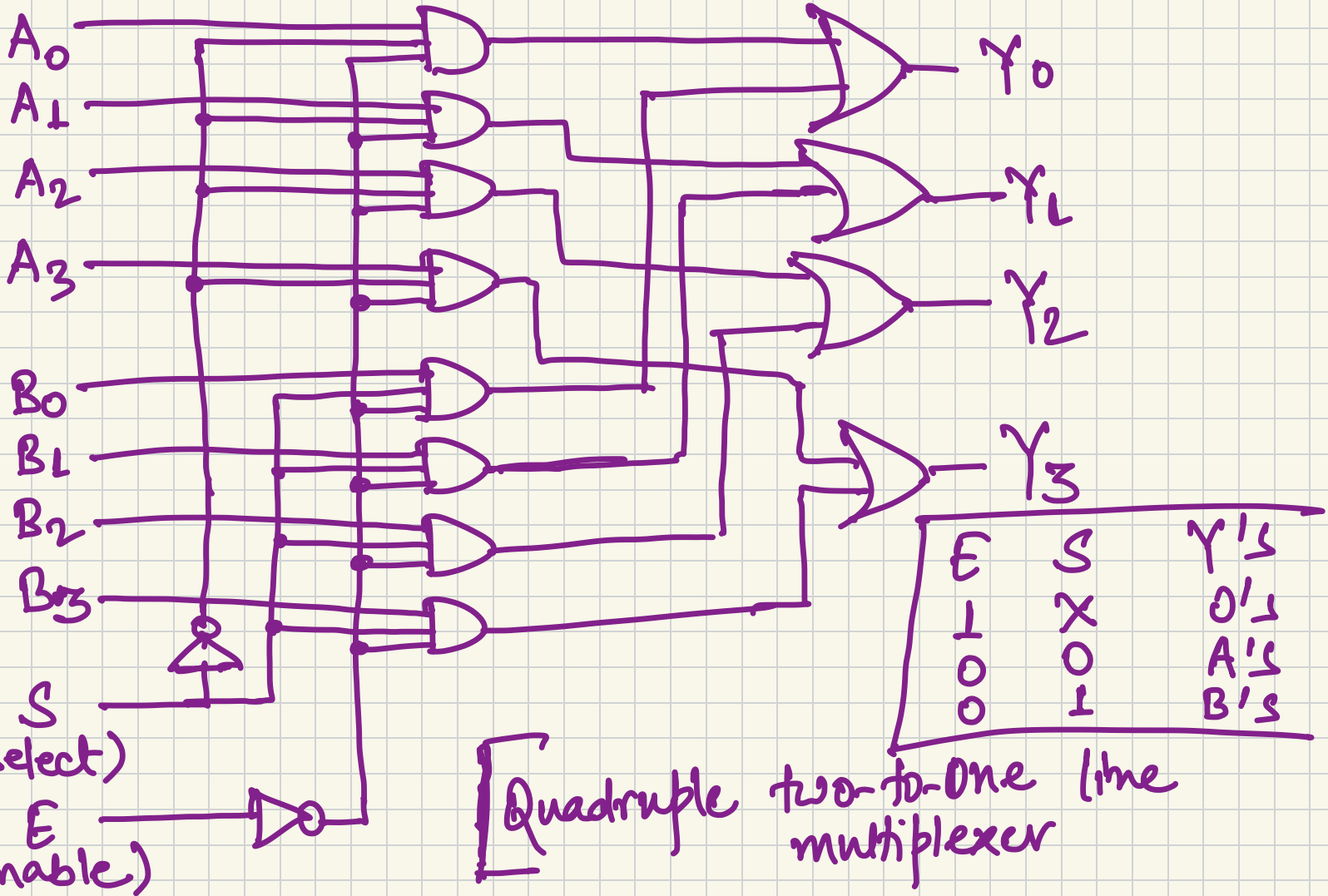
A multiplexer is also called a data-selector.

The AND gates (and the inverter gates) "decode" the selection input lines.

A 2^n-to-1 line multiplexer is constructed from an n-to-2^n line decoder by adding 2^n input lines to it (one line to each AND gate) and the outputs of the AND gates are applied to a single OR gate.

Like in decoders, multiplexers can also have an enable input to control its operation.

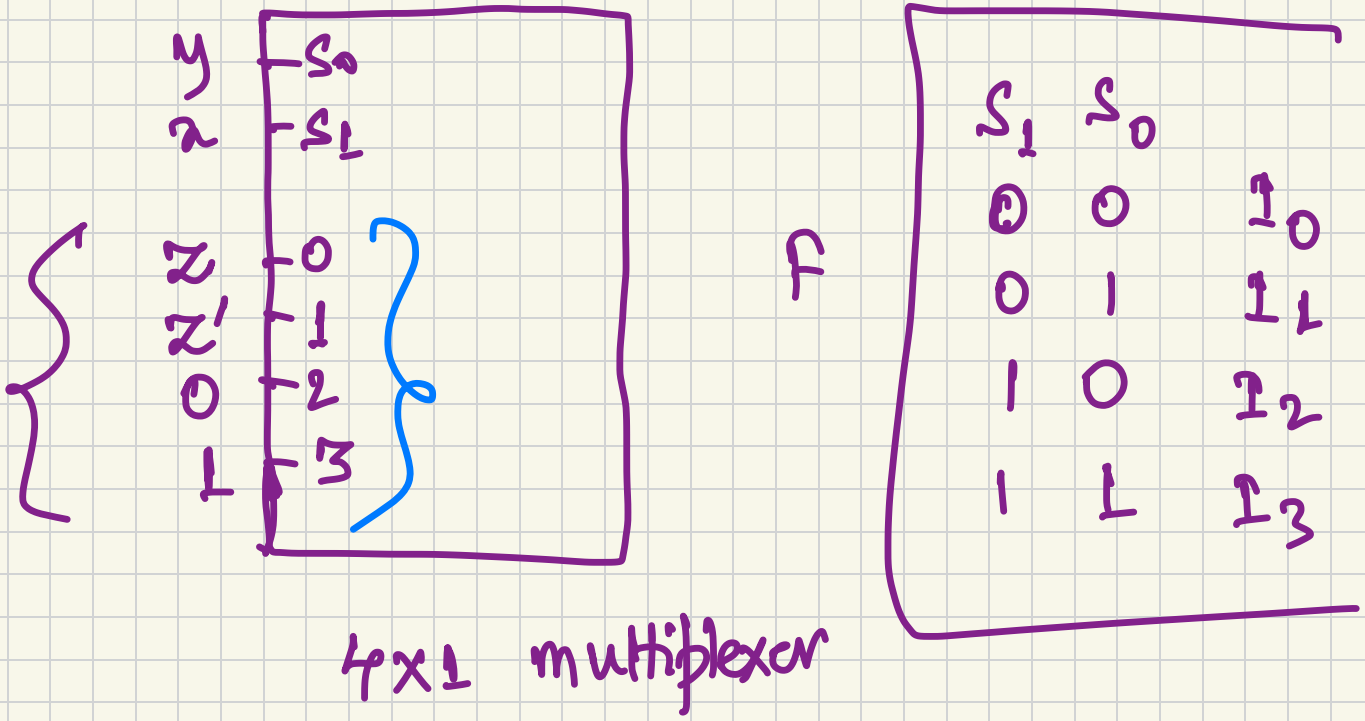
(Example on next slide)


A0
A1
A2
A3
B0
B1
B2
B3
S
(select)
E
(enable)
Y0
Y1
Y2
Y3
E S Y's
1 X 0's
0 0 A's
0 1 B's
Quadruple two-to-One line multiplexer

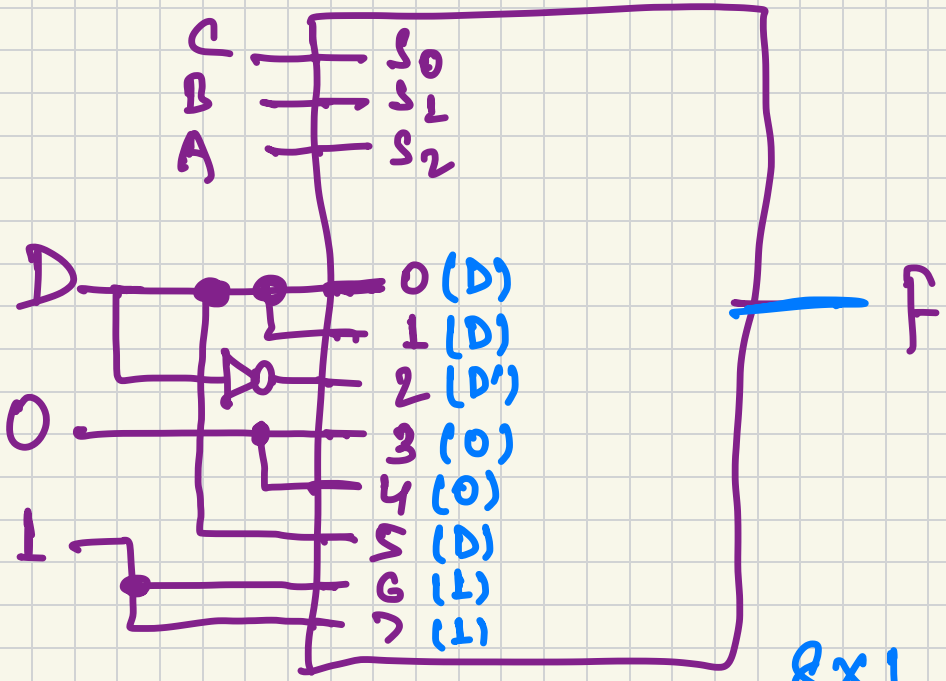
Implement Boolean Functions with Multiplexers

$$f(x, y, z) = \Sigma(1, 2, 6, 7)$$

x	y	z	f	
0	0	0	0	z
0	0	1	1	
0	1	0	1	z'
0	1	1	0	
1	0	0	0	0
1	0	1	0	
1	1	0	1	1
1	1	1	1	


y
z
S_0
S_1
z
z'
0
1
0
2
1
3
f
S_1 S_0
0 0 I_0
0 1 I_1
1 0 I_2
1 1 I_3
4x1 multiplexer

$$F(A,B,C,D) = \sum(1,3,4,11,12,13,14,15)$$



8x1 MUX

A	B	C	D	F	
0	0	0	0	0	D
0	0	0	1	1	
0	0	1	0	0	D
0	0	1	1	1	
0	1	0	0	1	D'
0	1	0	1	0	
0	1	1	0	0	0
0	1	1	1	0	
1	0	0	0	0	0
1	0	0	1	0	
1	0	1	0	0	D
1	0	1	1	1	
1	1	0	0	1	1
1	1	0	1	1	
1	1	1	0	1	1
1	1	1	1	1	

Exercise

Implement

$F(A, B, C) = \sum(3, 5, 6, 7)$

with a multiplexer.

Reading Exercise

Three-state gates

(Page No. 204 in the book)

Next class

Synchronous Sequential Logic

(chapter 5).