ACOL 215 (22nd Sept.)

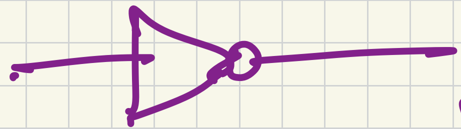
Integrated circuits (ICs)

Important parameters that distinguish logic families

i) fan-out → the number of outputs
ii) fan-in → the number of inputs for a gate

iii) power dissipation : power consumed by the circuit (that must be obtained from the power supply).

iv) propagation -delay

x  x'

$0 \to 1$ $\qquad$ $1 \to 0$

t $\qquad$ $\underline{\underline{t+\delta}}$

v) <u>noise margin</u> maximum external noise voltage that can be added to an input signal without causing an undesirable change in behaviours.

Computer-Aided Design of VLSI Circuits

Circuit will "behave" as expected

Before the circuit is fabricated

Hardware Description Languages ← Verilog, VHDL

CAD-Tools

"verification"

Hardware verification

encode the good/desirable behaviour + encode the design in this language

Gate-Level Minimization

- → finding an optimal gate-level implementation of a Boolean function.

- → complexity of the digital logic gates that implement a given function is directly proportional to the complexity of the algebraic expression that represents the function.

→ function can have different equivalent representation

→ simplifying the representation

We've seen them but not systematically

What we mean by "simple" here?

→ We will assume that the "simplest" algebraic expression will have the least number of terms and the smallest number of literals in each term.

Karnaugh Maps (or K-maps)

Two variable K-map

x, y

4 minterms

$x'y'$, xy', $x'y$, xy

m_0 m_2 m_1 m_3

$x \backslash y$	0	1
0	m_0 $x'y'$	m_1 $x'y$
1	m_2 xy'	m_3 xy

How do we use these to represent Boolean functions?

$x \backslash y$	0	1
0	m_0	m_1 1
1	m_2 1	m_3 1

$x+y$

$x \backslash y$	0	1
0	m_0	m_1
1	m_2	m_3 1

xy

$x \backslash y$	0	1
0	m_0	m_1 1
1	m_2 1	m_3

$x \oplus y$

Three-variable K-map

x \ yz	00	01	11	10
0	m_0 $x'y'z'$	m_1 $x'y'z$	m_3 $x'yz$	m_2 $x'yz'$
1	m_4 $xy'z'$	m_5 $xy'z$ 1	m_7 xyz 1	m_6 xyz'

1's in adjacent cells then the expression can be simplified.

$$f = xy'z + xyz = xz(y'+y) = xz$$

Any two minterms that are in adjacent cells when combined with an "OR" lead to removal of the dissimilar variable.

Example

$$F(x,y,z) = \boxed{\sum(2,3,4,5)}$$

$x \backslash yz$	00	01	11	10
0	m_0	m_1	m_3 1	m_2 1
1	m_4 1	m_5 1	m_7	m_6

$x'y$

xy'

$$F(x,y,z) = xy' + x'y$$

Example

$$F(x,y,z) = \sum(3,4,6,7)$$

yz

$x \backslash yz$	00	01	11	10
0	m_0	m_1	m_3 1	m_2
1	m_4 1	m_5	m_7 1	m_6 1

xyz'

$xy'z'$

adjacent

xz'

$$\boxed{x'yz + xy'z' + xy(z+z')}$$

$$F(x,y,z) = xz' + yz$$

Example

$$F(x,y,z) = \sum(0,2,4,5,6)$$

$x \backslash yz$	00	01	11	10
0	m_0 1	m_1	m_3	m_2 1
1	m_4 1	m_5 1	m_7	m_6 1

$$z' + xy'z$$

$$z' + xy'$$