peeks@tamu.edu LinkedIn **PEEYUSH KUMAR SINHA** (979)922-0985

OBJECTIVE: Actively seeking full-time opportunities in ASIC Design and Implementation roles.

EDUCATION: **Texas A&M University, College Station** **May 2020**
Masters in Computer Engineering GPA: 4.0/4.0
COURSES: Operating Systems, Advanced Computer Architecture, Microprocessor System Design, Hardware Design Verification Deep Learning in Computer Graphics, VLSI Machine Learning Systems, VLSI System Design, Digital Systems Testing

National Institute of Technology, Warangal **May 2016**
B.Tech in Electronics and Communication Engineering GPA: 8.05/10
COURSES: Real Time Operating System, Computer Architecture, Microprocessor & Microcontroller, Embedded System Design

PROJECTS:
- Implemented Cache Replacement Policies Hawkeye and Harmony and achieved a speedup of 8.4% over LRU
- Zynq-7000 FPGA implementation of Linux based device driver for interrupt driven IR Remote Sensor System
- Hardware Accelerators for Convolutional Neural Networks (CNNs) for image processing (similar to Eyeriss) and Long Short Term Memory Networks (LSTMs) for speech recognition dataset (similar to this)
- Complete Verification of a HTAX Crossbar design in UVM Environment
- Image Super-resolution using Generative Adversarial Networks (GANs), and Object Detection using CNNs

SOFTWARE SKILLS: C/C++, SystemVerilog, Perl, Tcl, Python, Linux shell scripting

TOOLS / SIMULATORS: Design Compiler, IC Compiler, Innovus, PrimeTime, Conformal, Seahawk, IC Validator, Pytorch, ChampSim, Design Vivado, VCS, SimVision, Cadence Incisive, Logic Vision, Spyglass

WORK EXPERIENCE: NVIDIA Santa Clara
Co-op Engineer, GPU Design Implementation **May 2019 - May2020**
- End to End (Netlist to GDS) implementation of Physical Design activities consisting of Floor-planning and power planning, Logic placement, Clock-tree synthesis, Routing and optimization strategies to improve Power, Performance and Area of design
- Logic Retiming to improve performance of hard-macro; debugged, enhanced and fixed issues and checks in the PnR flow.
- SAIF generation and Vector based IR drop analysis, EM analysis, antenna checks, and exploring ways to tackle these violations.
- Parasitic extraction, MCMM Static Timing Analysis; performing Timing ECOs for timing closure and design convergence
- Physical Verification at Partition level for cleaning up DRC issues and LVS errors along with Functional ECOs implementation

QUALCOMM India Pvt Ltd. Bangalore, India
Associate Engineer, GPU Design Implementation **July 2016 - August 2018**
- GPU RTL Integration, cleaning up Clock Domain Crossing (CDC) violations and resolved Linting errors.
- RTL MBIST insertion and simulation/verification, cleaning up CLP on RTL, generating UPF for power aware synthesis
- Physically aware RTL Synthesis (DC-Graphical), logic retiming and optimized recipes resulting in improved Netlist QoR
- DFT insertion and CLP cleanup on post-DFT netlist, followed by RTL→Netlist Equivalency check (Formal Verification)
- Generation and validation of Functional and Test mode constraints; Multi-corner multi-mode (MCMM) Static Timing Analysis Timing correlation for design between DCG-PT with POCV PVT conditions, ECO implementation and quick Netlist delivery

Engineering Intern, GPU Implementation Methodology **May 2015 – July 2015**
- Explored clustering techniques for single bit to multibit flop merging, targeted at timing and congestion improvements.
- Explored leakage power reduction opportunities by std cell swapping on non-timing critical paths.

RECOGNITION:
- Qualstar for achieving higher performance on a design without exceeding std cell area and power limits
- Winner at IdeaQuest 2015, a design challenge organized for interns at Qualcomm India, Bangalore.
- Selected to present an idea as a paper from amongst several paper submissions at QBUZZ-2016.
- Amul Vidya Shree and Vidya Bhushan for academic excellence in Standard 10^{th} and 12^{th} respectively.
- School Representative at JBNSTS, a Science workshop and meetup, organized by Government of India

LEADERSHIP:
- Organized and Managed Paper presentations at QBUZZ-2016 (Qualcomm India technical conference)
- Mentored undergrad students at HACKATHON-2015, in problem solving and debugging technical issues
- Mentor at Innovation Garage, a 24x7 multidisciplinary workspace for innovation
- Leader of School Quiz Club for various inter and intra school quizzing competitions.

WORKSHOPS:
- Fundamentals of Deep Learning for computer vision using Caffe and Digits (NVIDIA sponsored)
- Fundamentals of Accelerated Computing with CUDA in C/C++ (NVIDIA sponsored)
- Developing an ARM Cortex A9 based SoC using Zynq-7000 FPGA (Intel and NITW sponsored)

WORK AUTHORIZATION: Authorized to work for 3 years under OPT (Optional Practical Training) without Sponsorship.