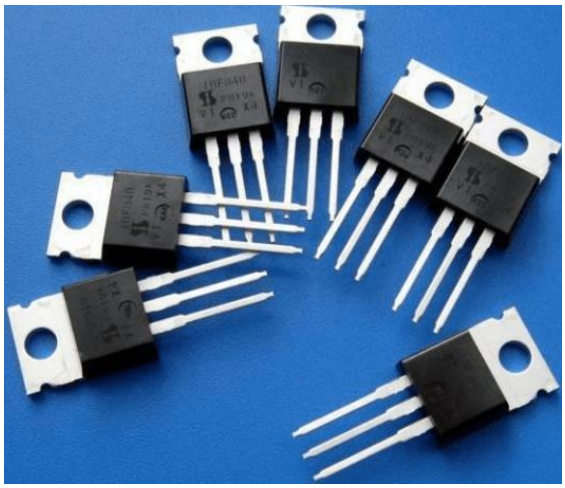
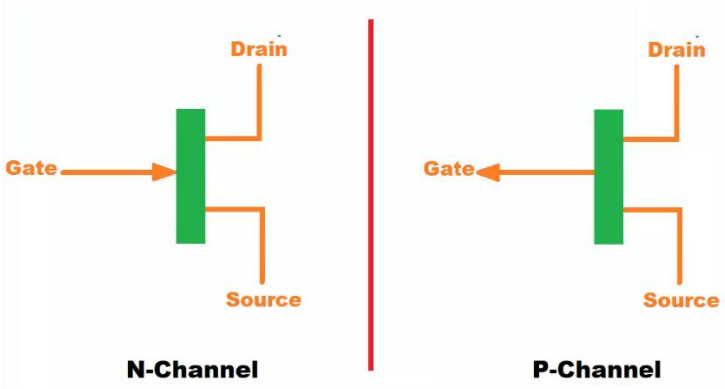
Introduction to Field Effect Transistor:

A Field Effect Transistor (FET) is a three-terminal Active semiconductor device, where the output current is controlled by an electric field generated by the input voltage.

A Field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, amplifying wireless signals). The device can amplify analog or digital signals. FETs are also used in high power switching applications, as voltage-variable resistors (VVRs) in operational amplifiers (Op-Amps), and tone controls, etc., for mixer operation on FM and TV receivers and in logic circuits.



FET Symbol:



- **Source**: The first terminal is the source. The current that enters through the source is denoted by I_S.
- **Drain**: The current that leaves through the drain is denoted by I_D. There is a presence of voltage between drain and source which is denoted by V_{DS}.
- **Gate**: Gate controls and modulates the conductivity of the channels. It is denoted by G. By applying a voltage at the gate, the current that leaves through the drain can be controlled.
- The direction of the arrowhead reflects the direction of the electric field.

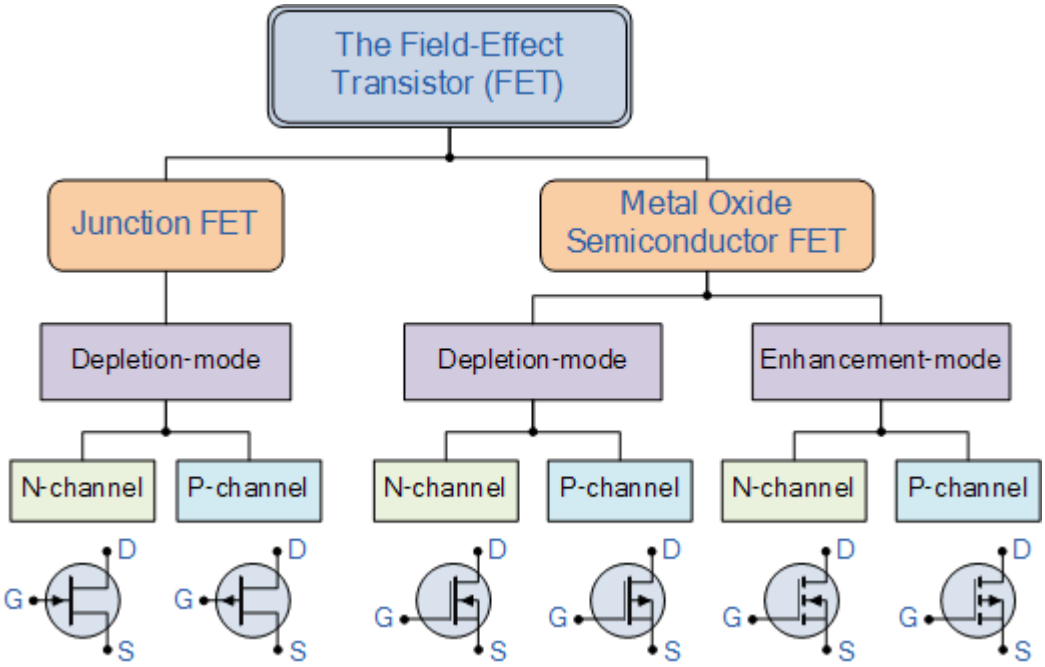
- The symbol is slightly different for two different types of field-effect transistors FETs, they can either be N channel FET or P channel FET.

FETs are also known as unipolar transistors because, unlike bipolar transistors, FETs only have either

electrons or holes operating as charge carriers. FET uses the voltage applied to its input terminal (called the Gate), to control the current flow from the source to drain, making the Field Effect Transistor a “Voltage” operated device.

The primary difference between the two types is BJT is a Current Controlled device ($I_C=\beta I_B$), FET is a Voltage Controlled device. Most important characteristic is it has High-Input Impedance, which is important to design a Linear AC Amplifiers. In general FET’s are more stable in temperature variation than BJT’s and are smaller in construction, which is particularly useful in Integrated-Circuit Chips (IC’s)

Types Of FETS:



A Field Effect Transistor is a voltage-controlled device i.e. the output characteristics of the device are controlled by input voltage. There are two basic types of field effect transistors: Junction field effect transistor (JFET) and Metal oxide semiconductor field effect transistor (MOSFET). MOSFET’s are also called IGFET (Insulated Gate Field Effect Transistor).

The depletion mode MOSFET transistors are generally ON at zero gate-source voltage (VGS). The conductivity of the channel in depletion MOSFETs is less compared to the enhancement type of MOSFETs.

The Enhancement mode MOSFET is equivalent to “Normally Open” switch and these types of transistors require a gate-source voltage to switch ON the device.

Here, we can observe that a broken line is connected between the source and drain, which represents the enhancement mode type. In enhancement mode MOSFETs, the conductivity increases by increasing the oxide layer, which adds the carriers to the channel. The Arrow head indicates the direction of current

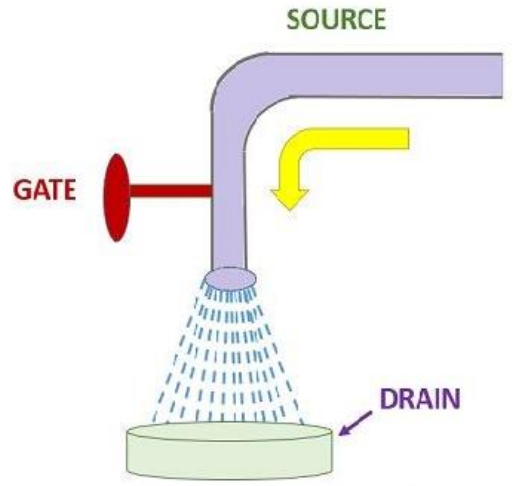
Comparison between Bipolar Junction Transistor and Field Effect Transistor:

Parameter	BJT	FET
Full form	BJT stands for Bipolar Junction Transistor.	FET stands for Field Effect Transistor.
Definition	A type of transistor which uses two types of charge carries viz. electrons and holes for conduction is known as bipolar junction transistor (BJT).	A type of transistor in which electric field is used to control the flow of current in a semiconductor is known as field effect transistor (FET).
Drive type	In BJT, the current flow is due to both majority and minority charge carriers. Thus, it is a bipolar device.	In FET, the electric current flows only due to majority charge carriers. Thus, it is a unipolar device.
Terminals	BJT has three terminals viz. Emitter, Base and Collector.	FET also has three terminals viz. Source, Drain and Gate.
Control element	BJT is a current-controlled device.	FET is a voltage controlled device.
Types	BJT are of two types: NPN transistor and PNP transistor.	FET are also of two types: N-channel FET and P-channel FET.
Configuration	BJT has three configurations: common emitter (CE), common base (CB) and common collector (CC).	FET also has three configurations: common source (CS), common gate (CG) and common drain (CD).
Size	BJT is large in size and hence requires more space. Therefore, it is more complicated to fabricate as an IC	FET is comparatively smaller in size. Hence, it is easier to fabricate as an IC.
Sensitivity	BJT is more sensitive to the changes in the applied voltage.	FET is less sensitive to the variations in the applied voltage.
Relationship between input and output	BJT has linear relationship between input and output.	FET has non-linear relationship between input and output.
Thermal noise	BJT has more thermal noise.	The thermal noise in case of FET is much lower.
Thermal runway	Thermal runway exits in BJT.	Thermal runway does not exist in FET.
Thermal stability	BJT has less thermal stability.	FET has good thermal stability due to absence of minority charge carriers.
Input impedance	In case of BJT, the input circuit is forward biased. Thus, the BJT has low input impedance.	FET has high input impedance due to reverse bias of input circuit.
Temperature coefficient at high current levels	BJT has positive temperature coefficient.	FET has negative temperature coefficient.
Suitability	BJT is suitable for low current applications.	FET is suitable for high current applications.
Switching speed	The switching speed of BJT is low.	FET has higher switching speed.
Effect of radiation	BJT is susceptible to radiation.	FET is relatively immune to radiation.
Gain bandwidth product	BJT has higher gain bandwidth product.	FET has lower gain bandwidth product.
Minority carrier storage effect	BJT suffers from minority carrier storage effect.	FET does not suffer from minority carrier storage effect.
Cost	BJT is cheaper to manufacture.	FET is relatively expensive to manufacture.
Installation	BJT does not require special handling during installation.	FET demands special handling during installation.

Applications	BJT is used as switch (in saturation and cut-off region) and amplifier (in active region).	FET is used as switch (in saturation and cut-off region) and as amplifier (in Ohmic region

Water Analogy to understand the concept of JFET:

To understand how an FET works, let's use an analogy. Analogies often make things simple to understand even a complex concept. The water source can be understood as the source of FET, the vessel which collects water is analogous to the drain terminal of FET. Let's have a quick look at the below diagram, after that understanding the concept of FET will be a cake walk.

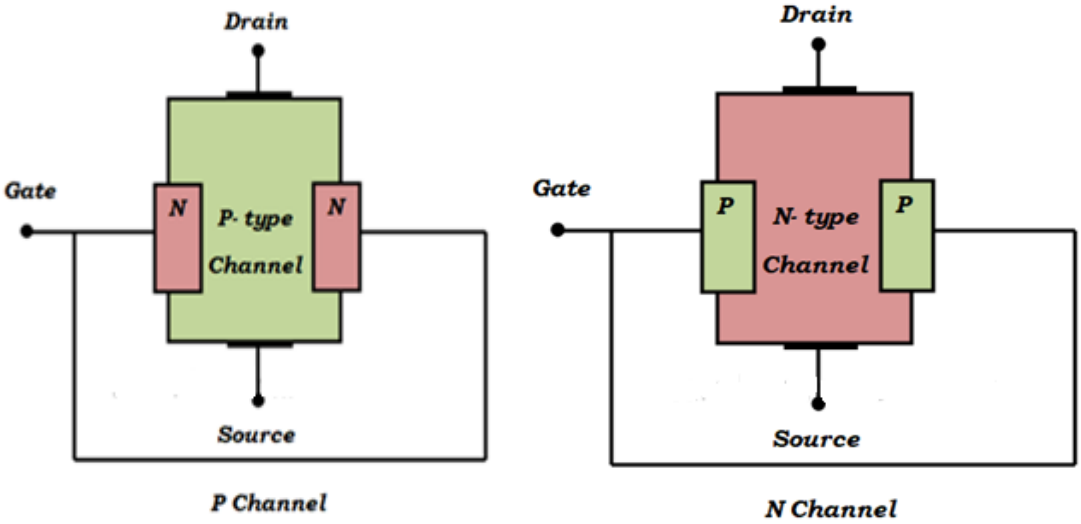


Water Analogy for Understanding FET

The controlling tap which controls the flow of water. Now, the way in which the controlling tap modulate the quantity of water coming from the outlet, in the same way, the voltage at gate terminal controls the flow of current from source to drain terminal.

JFET is one of the types of FET. It is voltage controlled device. JFET is used as a voltage controlled resistor or switch or as an amplifier. There are two types of JFET namely N-Channel JFET and P-Channel JFET.

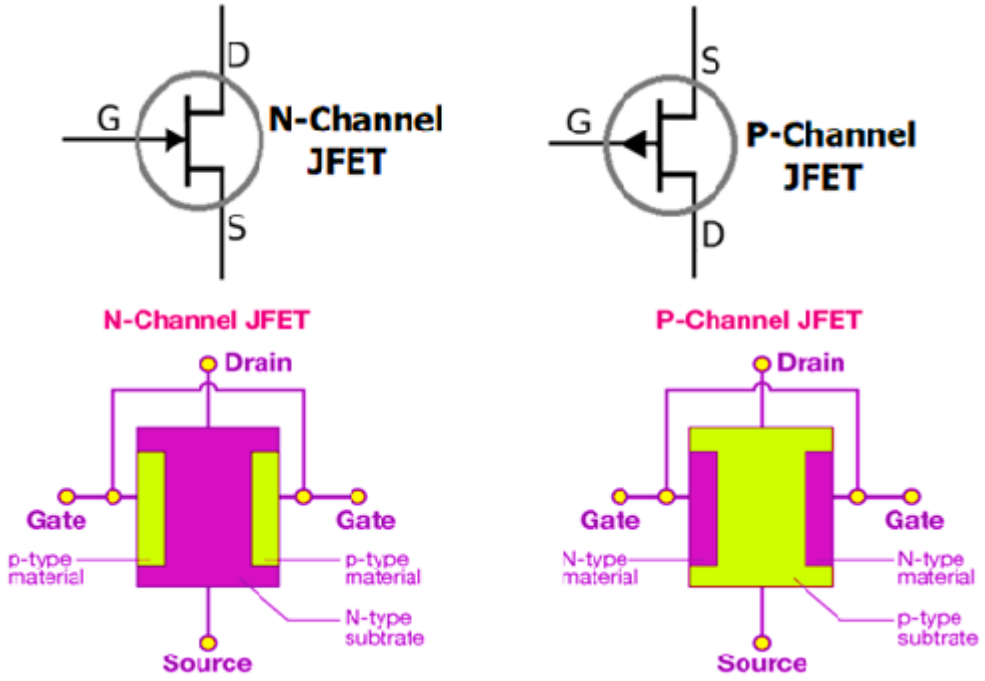
In N channel the generation of the current is due to the movement of electrons, in P channel the generation of current is due to the movement of holes. Since the movement of electrons is faster than the movement of holes, N- Channel JFET is preferred more than the P-Channel JFET.



- JFET has a high impedance.
- JFETs are low power consumption devices.
- JFET can be fabricated in a smaller size, and as a result, they occupy less space in circuits due to their smaller size.

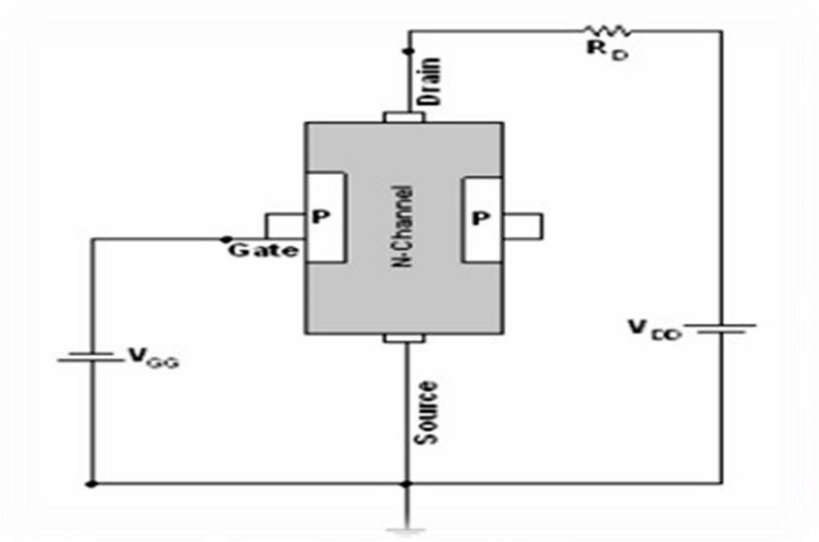
Junction Field Effect Transistor (JFET)

A JFET is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes. The current conduction is controlledby means of an electric field between the gate and the conducting channel of thedevice. The JFET has high input impedance and low noise level.



A JFET consists of a p-type or n-type silicon bar containing two p-n junctions at the sides as shown in fig. The bar forms the conducting channel for the charge carriers. If the bar is of p-type, it is called p-channel JFET and if the bar is of n- type, it is called n-channel JFET as shown in the above figures. The two p-n junctions forming diodes are connected internally and a common terminal gate is taken out. Other terminals are source and drain taken out from the bar. Thus, a JFET has three terminals such as, gate (G), source (S) and drain (D).

N-Channel JFET Circuit



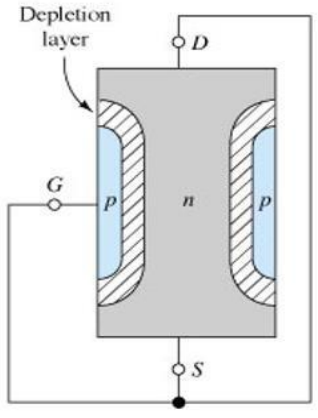
The input circuit (i.e., gate to source) of a JFET is reverse biased. This means that the device has high input impedance. The drain is so biased with respect to source that drain current I_D flows from the source to drain. In all JFETs, source current I_S is equal to the drain current i.e. $I_S = I_D$.

Operation of an N-Channel JFET

There are four basic operating conditions for a JFET:

- When $V_{GS} = 0$ and $V_{DS} = 0$
- When $V_{GS} = 0$ and V_{DS} is increasing
- When V_{GS} = -ve and V_{DS} is increasing
- When V_{GS} = +ve and V_{DS} is increasing

Case (a): When $V_{DS} = 0$ and $V_{GS} = 0$:



(a) Bias is zero and depletion layer is thin; low-resistance channel exists between the drain and the source

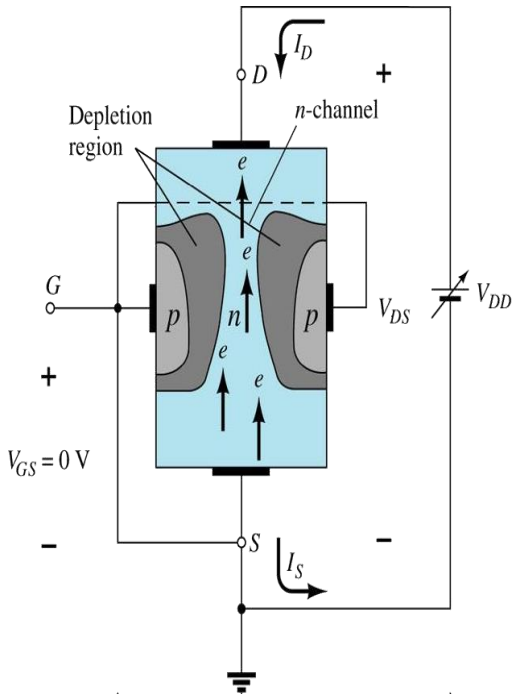
- When $V_{DS} = 0$ and $V_{GS} = 0$, the thickness of depletion region around the p-n junction is uniform as shown. The depletion region penetrates more into the channel since gate is heavily doped.

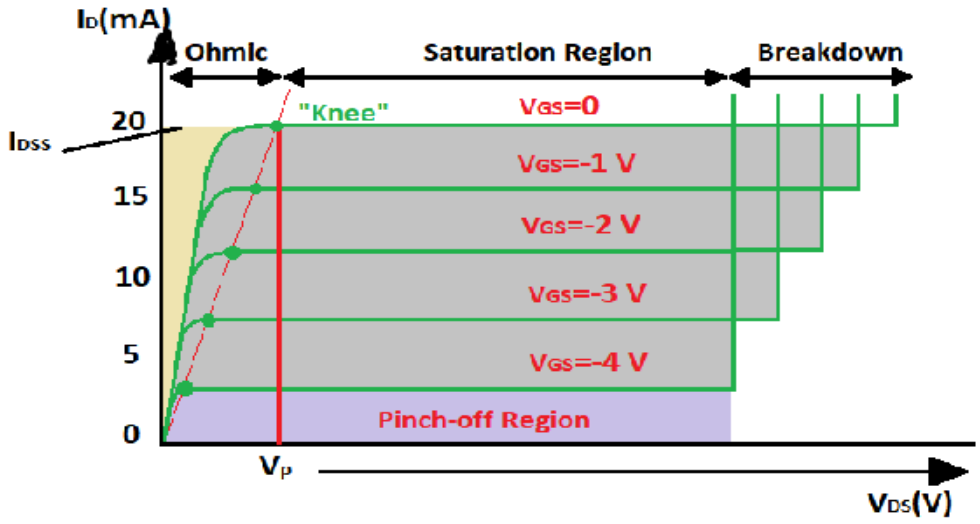
Case (b): VGS = 0, VDS increasing to some positive value:

Three things happen when $V_{GS} = 0$ and V_{DS} is increased from 0 to a more positive voltage:

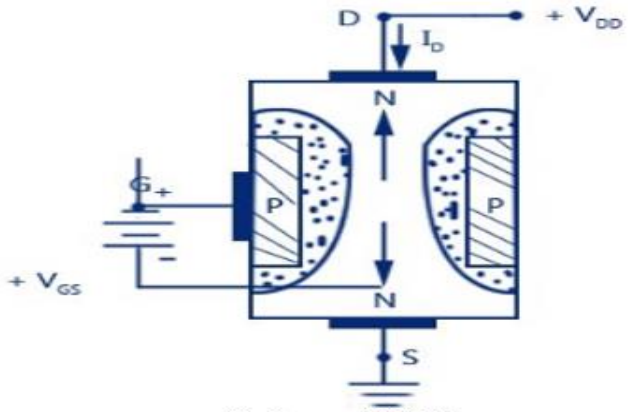
- The depletion region between p-gate and n-channel increases as electrons from n-channel combine with holes from p-gate.
- Increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.
- But even though the n-channel resistance is increasing, the current (I_D) from Source to Drain through the n-channel is increasing, since V_{DS} increased.
- As V_{DS} increases, I_D increases and the region is called OHMIC REGI

DRAIN CHARACTERISTICS:





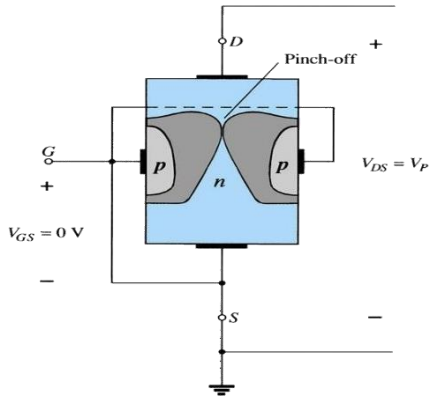
- As V_{DS} increases, reverse bias increases and depletion region width increases. It is seen that the penetration of depletion region is unequal. It penetrates more that in the drain side than at the source side as shown in the figure below:
- I_D will establish the voltage level through the channel.
- Voltage drop across the upper region of the p-type material is greater than lower region (greater applied reverse bias, the wider depletion region).
- Hence the shape of the depletion region is WEDGE SHAPED as shown inthe figure below.



N-channel JFET

As V_{DS} increases, depletion region penetrates more into the channel and at some point it closes the channel near the drain side as shown in figure

- The effective channel height decreases.
- This saturation is called PINCH OFF.
- At this voltage , channel is said to be pinched off and the drain voltage V_P is called PINCHOFF VOLTAGE.

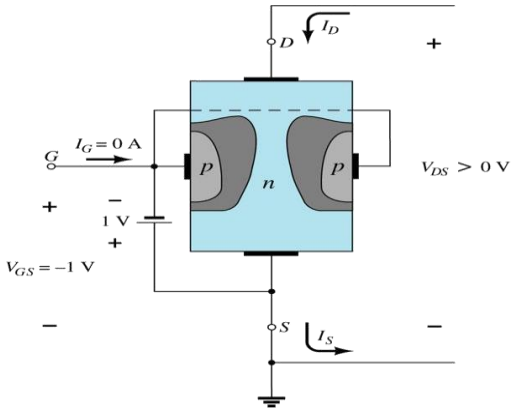


- After Vp, if V_{DS} is further increased, I_D does not increase and remains constant. This region in drain characteristics is called CONSTANT CURRENT REGION (or) SATURATION REGION.
- At pinch off, I_D maintains the saturation level defined as I_{DSS} .Therefore at $V_{GS} = 0$, I_D is maximum, then $I_D = I_{DSS}$.

- I_{DSS} is the max drain current of a JFET and is defined by the conditions $V_{GS} = 0V$ and $V_{DS} > |V_p|$.
- If V_{DS} is further increased, due to AVALANCHE MULTIPLICATION or BREAKDOWN, drain current drastically increases as shown in drain characteristics.

Case (c): V_{GS} = -ve, V_{DS} is increasing

- V_{GS} is the controlling voltage of the JFET.
- For n-channel devices, the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0V$ level.
- The effect of the applied negative V_{GS} is to establish depletion regions similar to those obtained with $V_{GS}=0V$ but a lower level of V_{DS} to reach the saturation level at a lower level of V_{DS}.



- When $V_{GS} = -V_p$ will be sufficiently negative to establish saturation level that is essentially 0mA, the device has been 'turn off'.
- The level of the V_{GS} that results in $I_D = 0$ mA is defined by $V_{GS} = V_p$, withV_p being a negative voltage for n-channel devices and a positive voltage f or p-channel JFETs.
- A V_{GS} becomes more and more negative, the slope of each curve becomes more and more horizontal.

Case (d): V_{GS} = +ve, V_{DS} is increasing

- When V_{GS} is positive , width of the depletion region decreases. Hence, at larger values of V_{DS} pinch off and breakdown occurs lately as shown in drain characteristics.

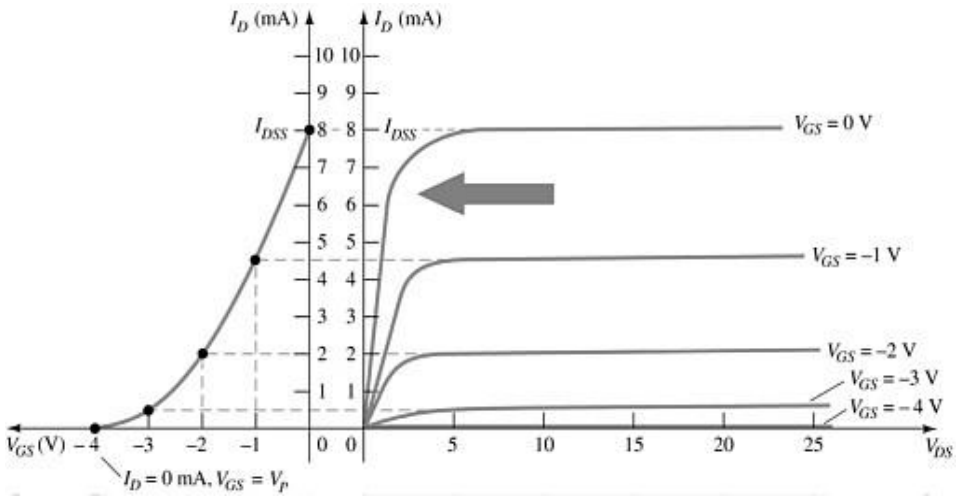
Transfer Characteristics

The input-output transfer characteristic of the JFET is not as straight forward as it is in BJT

In a BJT, (h_{FE}) defined the relationship between I_B (input current) and I_C(output current).

In a JFET, the relationship (Shockley's Equation) between V_{GS} (input voltage)and I_D (output current) is used to defined as the transfer characteristics, and a little more complicated (and not linear).

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

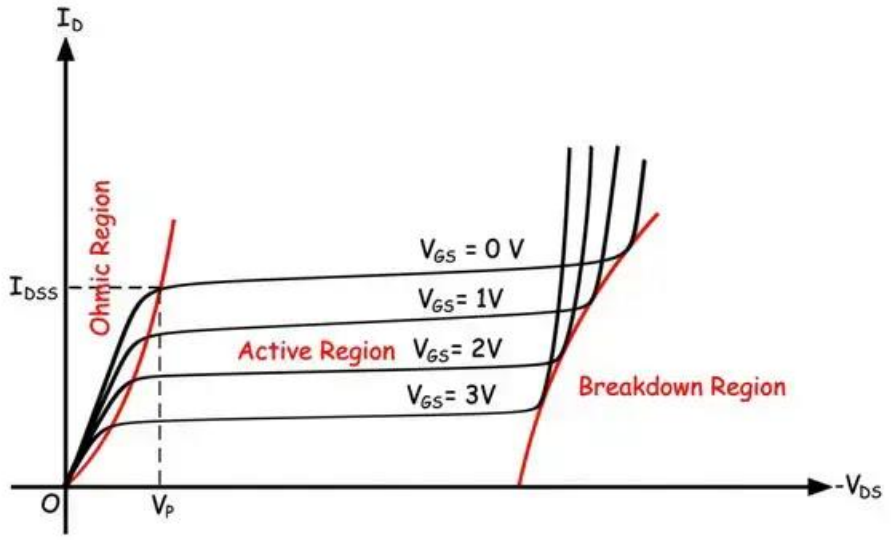


P-Channel Junction Field Effect Transistor:

- The device could be made of p type bar with n type gates.
- The device characteristics of n type and p type JFET is similar, the only difference being that in n channel JFET the current is carried by electrons while in p-channel JFET, it is carried by holes.
- In a p-channel JFET the source is positive with respect to the drain.
- Here the source is the source of holes which flow through the channel to the drain.
- The pinch-off is achieved by making the source to gate voltage, source to gate voltage negative there by reverse biasing the p-n junction diode formed by the channel and the gate.
- The figure shows the V_I characteristics of p channel JFET.

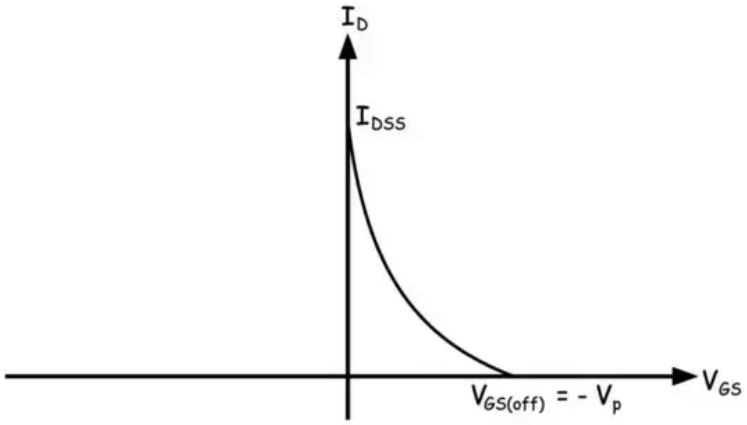
Characteristic of P-Channel JFET

In p channel JFET we apply negative potential at drain terminal. If we make both source and gate terminals grounded and increase the negative potential of the drain from zero, we will get the same curve as in the case of n channel JFET. Here at the beginning the drain current flowing from source to drain due to drift of holes in the same direction, linearly gets increased with increasing negative drain voltage. As the negative potential of the channel is more towards drain terminal hence the reverse biasing of the junction nearer to drain is more. This causes a thicker depletion layer towards drain terminal. So just like the previous case the pinch-off occurs after a certain negative drain voltage and the curve becomes horizontal. If we go on increasing negative drain voltage, after a certain negative drain voltage the depletion layers go through avalanche breakdown and the channel gets free from any further obstruction and drain current suddenly rises to a higher value. Hence, the curve will have a linear region at the beginning, an active region in the middle and breakdown region at the end. Now if we apply positive voltages at the gate terminal, the reverse biasing of the junction becomes more rapid and as a result, the characteristic curve gets shifted downward as shown below.



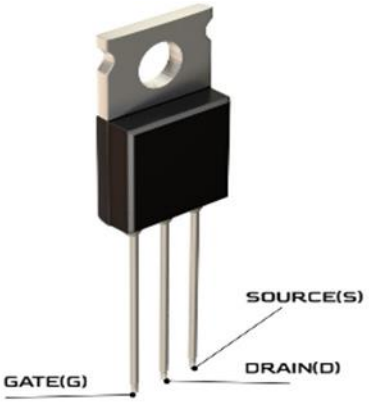
Transfer Characteristic of P Channel JFET

This is drawn between positive gate voltage and drain current. The pattern will be the same as in the case of n channel JFET but the polarity of the applied voltage and direction of the drain current differ.

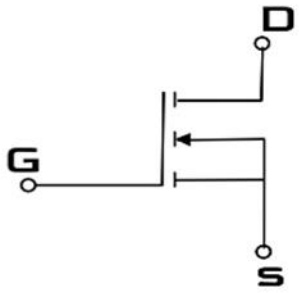


What is a MOSFET:

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device that is widely used for switching purposes and for the amplification of electronic signals in electronic devices. A MOSFET is either a core or integrated circuit where it is designed and fabricated in a single chip because the device is available in very small sizes. The introduction of the MOSFET device has brought a change in the domain of **switching in electronics**.



MOSFET

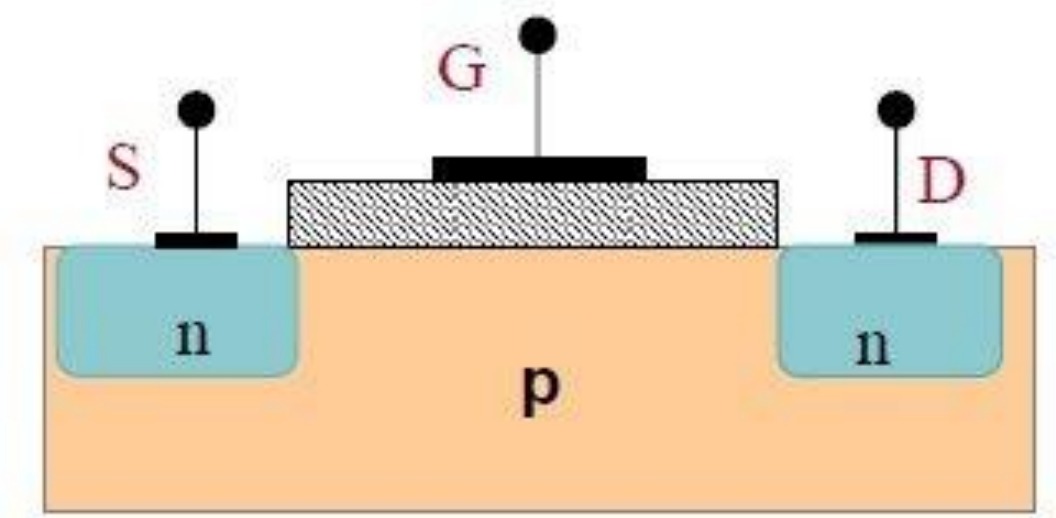


SYMBOL OF MOSFET

The metal (or conductive silicon) gate terminal is separated from these by a nonconductive oxide layer. By applying voltage to the gate, it changes the electrical properties of the semiconductor underlying, either allowing or inhibiting the flow of electricity between the source and drain.

The functionality of MOSFET depends on the electrical variations happening in the channel width along with the flow of carriers (either holes or electrons). The charge carriers enter into the channel through the source terminal and exit via the drain.

MOSFETs have characteristics similar to JFETs and additional characteristics that make them very useful.



MOSFET Structure

There are 2 types of MOSFET's:

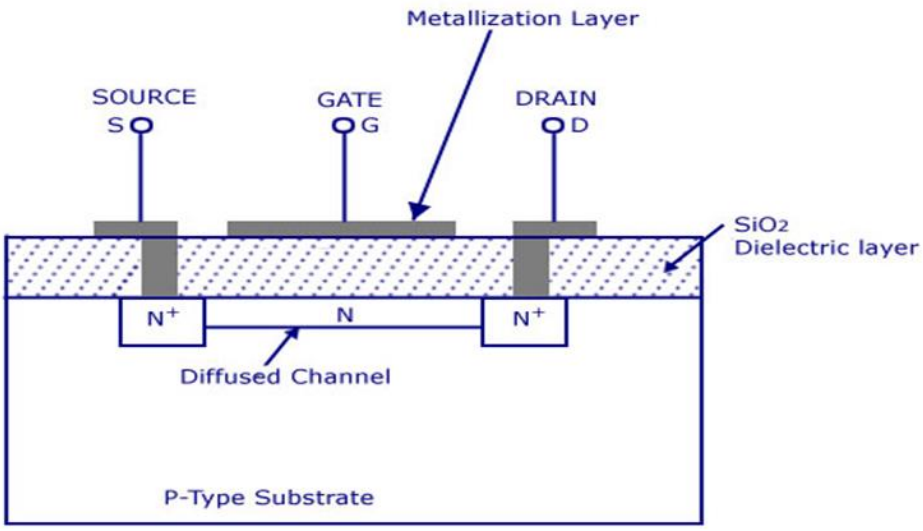
- Depletion mode MOSFET (D-MOSFET)
    - Operates in Depletion mode the same way as a JFET when $V_{GS} \leq 0$
    - Operates in Enhancement mode like E-MOSFET when $V_{GS} > 0$
- Enhancement Mode MOSFET (E-MOSFET)
    - Operates only in Enhancement mode
    - $I_{DSS} = 0$ until $V_{GS} > V_T$ (threshold voltage)

JFET Vs MOSFET

- JFETs can only be operated in the **depletion mode** whereas MOSFETs can be operated in either depletion or in **enhancement mode**.
- In a JFET, if the gate is forward biased excess- carrier injunction occurs, and the gate current is substantial. Thus, channel conductance is enhanced to some degree due to excess carriers, but the device is never operated with gate forward biased because gate current is undesirable.
- MOSFETs have input impedance much higher than that of JFETs. This is due to negligible small leakage current.
- JFETs have characteristic curves flatter than those of MOSFETs indicates high drain resistance.
- When JFET is operated with a reverse bias on the junction, the gate current I_G is larger than it would be in a comparable MOSFET.
- For the above reasons, and also because MOSFETs are somewhat easier to manufacture, they are more widely used than are the JFET.

BASIC CONSTRUCTION OF N CHANNEL DEPLETION TYPE MOSFET:

- Two highly doped N regions are diffused into a lightly doped p type substrate that may have an additional terminal connection called SS(Substrate)
- The two highly doped n regions represent source and drain connected via an n-channel. The N-channel is formed by diffusion between the source and drain. The type of impurity for the channel is the same as for the source and drain.
- Metal is deposited through the holes to provide drain and source terminals, and on the surface area between drain and source, a metal plate is deposited. This layer constitutes the gate. The n-channel is connected to the Gate (G) via a thin insulating layer of SiO_2.
- The thin layer of SiO_2 dielectric is grown over the entire surface and holes are cut through the SiO_2 (silicon-dioxide) layer to make contact with the N-type blocks (Source and Drain).

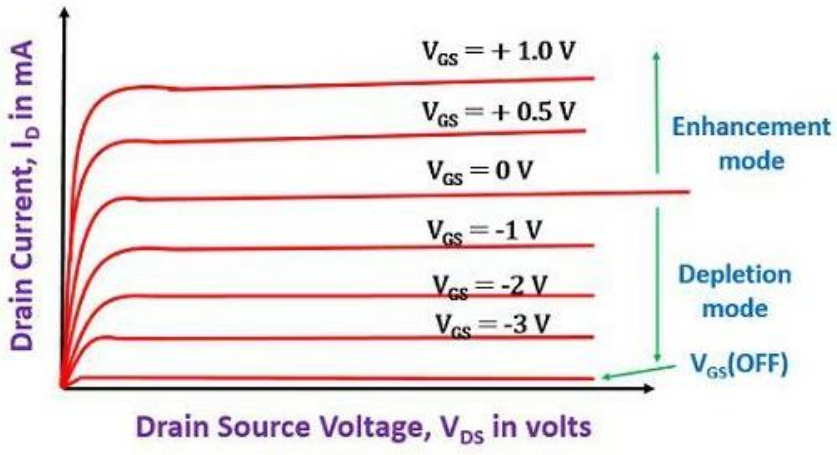


N-Channel DE-MOSFET Structure

Case(a)V_{gs}=0V and V_{DS}=+ve:

- When V_{GS} =0 and drain is made positive with respect to source current (in the form of free electrons) can flow between source and drain, even with zero gate potential and the MOSFET is said to be operating in Enhancement mode. In this mode of operation gate attracts the charge carriers from the P-substrate to the N-channel and thus reduces the channel resistance which increases the drain-current.
- When V_{GS} = negative with respect to the substrate, the gate repels some of the negative charge carriers out of the N-channel and attracts holes from the p type substrate. This initiates recombination of holes and electrons. This creates a depletion region in the channel and therefore reduces the number of free electrons in the n channel, increases the channel resistance and reduces the drain current. The more negative the gate, the less the drain current. In this mode of operation, the device is referred to as a **depletion-mode MOSFET**. Here too much negative gate voltage can pinch-off the channel.
- The more positive the gate is made, more number of electrons from p substrate due to reverse leakage current and collisions between accelerating particles the more drain current flows.

Drain characteristics:



- For V_{GS} exceeding zero the device operates in **enhancement mode**.
- These drain curves again display an ohmic region, a constant-current source region and a cut-off region.
- For a specified drain-source voltage V_{DS}, V_{GS} (OFF) is the gate-source voltage at which drain current reduces to a certain specified negligibly small value,
- For V_{GS} between $V_{GS\ (0FF)}$ (-ve value) and zero, the device operates in depletion-mode.

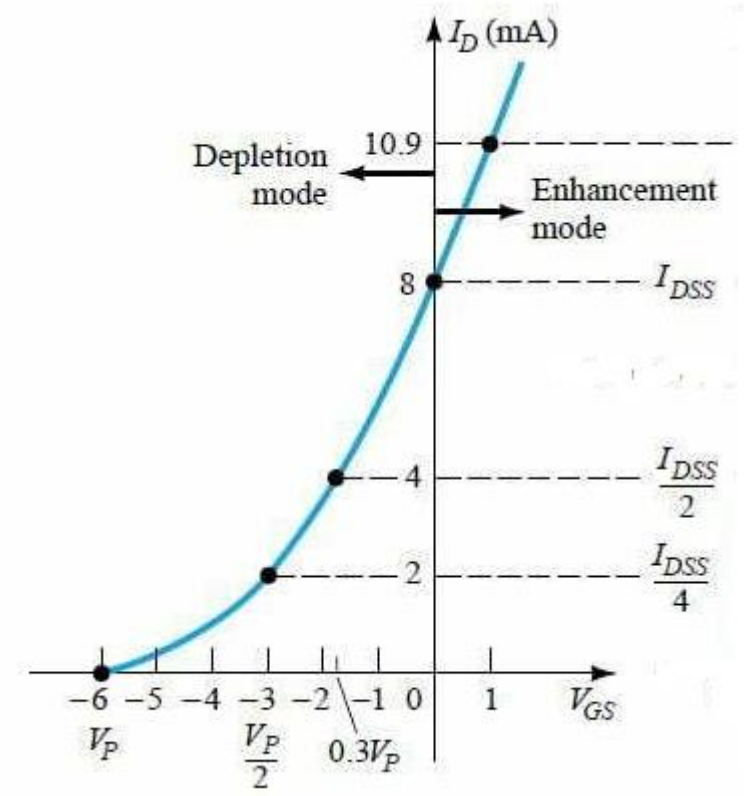
TRANSFER CHARACTERISTICS:

- The transfer characteristics of N channel depletion MOSFET is similar to JFET. These characteristics define the main relationship between the I_D and V_{GS} for the fixed V_{DS} value. For the positive V_{GS} values, we can also get the I_D value.

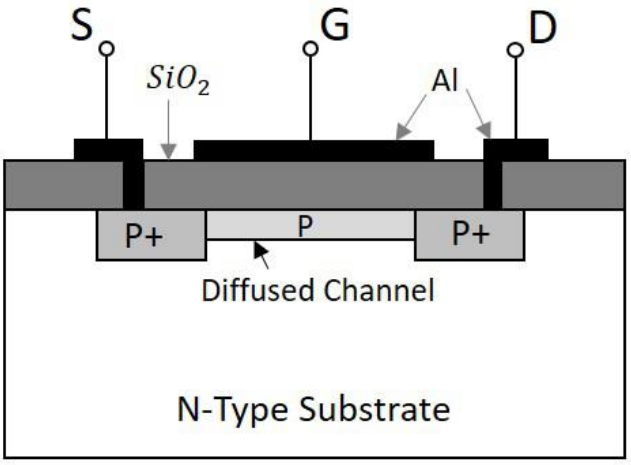
- So due to that, the curve in the characteristics will extend to the right-hand side. Whenever the V_{GS} value is positive, the no. of electrons within the channel will increase. When the VGS is positive then this region is the enhancement region. Similarly, when the VGS is negative then this region is known as the depletion region.

- The main relationship between the I_D and V_{GS} can be expressed as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



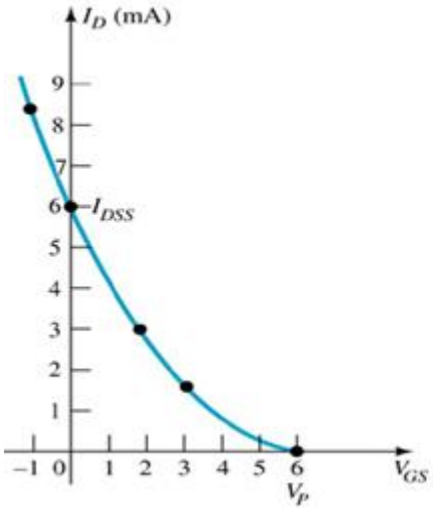
P-CHANNEL MOSFET:

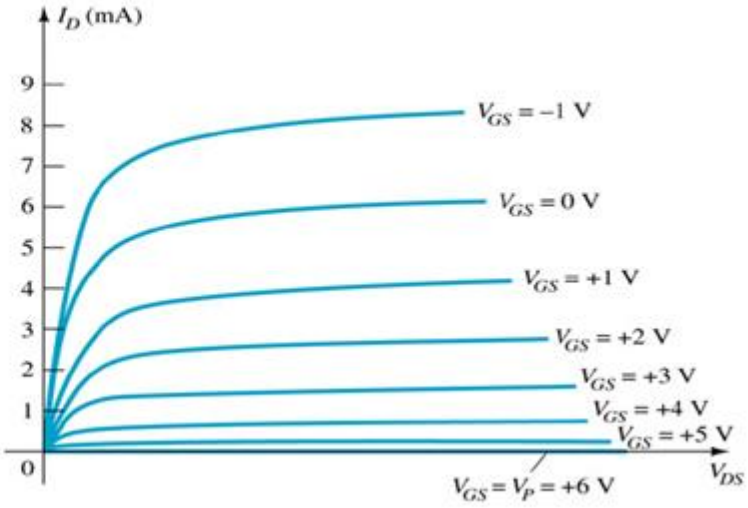


Structure of P-channel MOSFET

- The p-channel Depletion mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.

TRANSFER & DRAIN CHARACTERISTICS OF P-CHANNEL MOSFET:



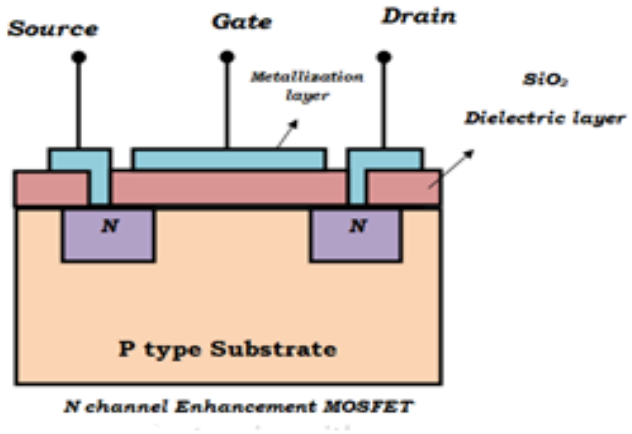


ENHANCEMENT MOSFET CHARACTERISTICS:

N-CHANNEL ENHANCEMENT MOSFET CONSTRUCTION:

- The main difference between the construction of DE-MOSFET and that of E-MOSFET, the E-MOSFET substrate extends all the way to the silicon dioxide (SiO_2) and no channels are doped between the source and the drain.
- Two highly doped n regions are diffused into a lightly doped p substrate that may have an additional terminal connection called SS.
- The source and drain are taken out through metallic contacts to n doped regions. These n-doped regions are not connected via an n-channel without an external voltage.
- The Gate (G) connects to the p-doped substrate via a thin insulating layer of SiO_2

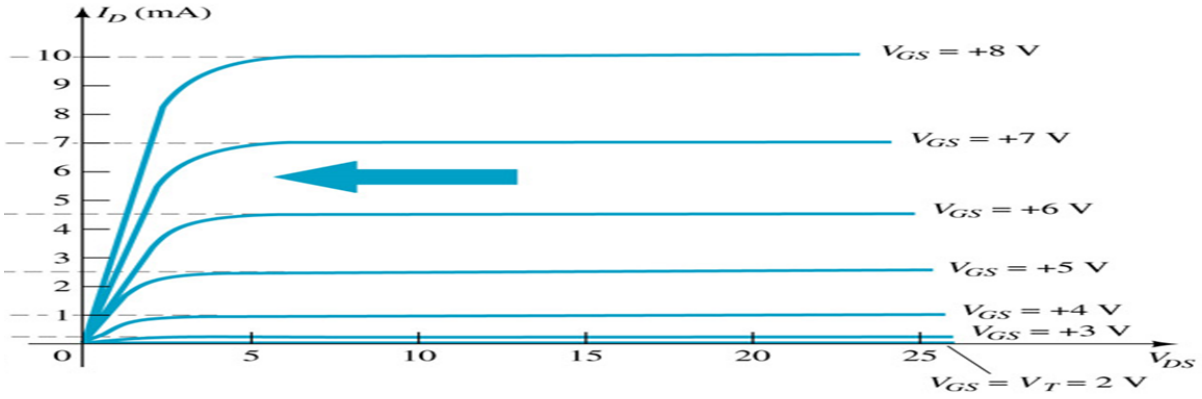
- Channels are electrically induced in these MOSFETs, when a positive gate-source voltage V_{GS} is applied to it.



- This MOSFET operates only in the enhancement mode and has no depletion mode. It operates with large positive gate voltage only.
- When drain is applied with positive voltage with respect to source and no potential is applied to the gate , a very small drain current that is, reverse leakage current flows
- When the gate is made positive with respect to the source and the substrate, negative (i.e. minority) charge carriers within the substrate are attracted to the positive gate and accumulate close to the-surface of the substrate. As the gate voltage is increased, more and more electrons accumulate under the gate. Since these electrons cannot flow across the insulated layer of silicon dioxide to the gate, so they accumulate at the surface of the substrate just below the gate. When this occurs, a channel is induced by forming an ***inversion layer*** (N-type). Now a drain current start flowing through the channel.

DRAIN CHARACTERISTICS:

- The Enhancement mode MOSFET only operates in the enhancement mode.
- VGS is always positive.
- IDSS = 0 when VGS < VT
- When VGS is greater than VT, the device turns- on and the drain current ID is controlled by the gate voltage. As VGS increases above VT, the density of electrons in the induced channel increases and ID increases. If VGS is kept constant and VDS is increased, then ID saturates (IDSS)
- The almost vertical components of the curves correspond to the ohmic region, and the horizontal components correspond to the constant current region.
- Thus E-MOSFET can be operated in either of these regions i.e. it can be used as a variable-voltage resistor (WR) or as a constant current source.

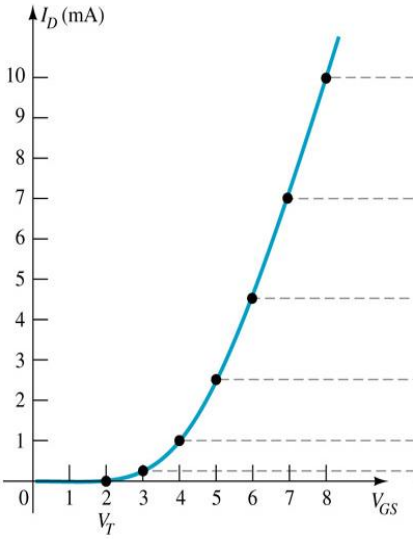


TRANSFER CHARACTERISTICS:

- The current I_{DSS} at V_{GS} <=0 is very small, When the V_{GS} is made positive, the drain current I_D increases slowly at first, and then much more rapidly with an increase in V_{GS}.
- The gate-source threshold voltage V_{GST} at which the drain current I_D attains some defined small value, say 10 u A.
- The equation for the transfer characteristic of E-MOSFETs is given as:

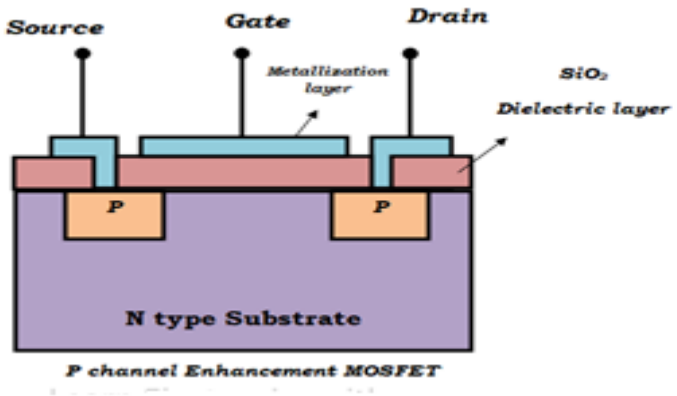
$$\mathbf{I_D = k\,(V_{GS} - V_T)^2}$$

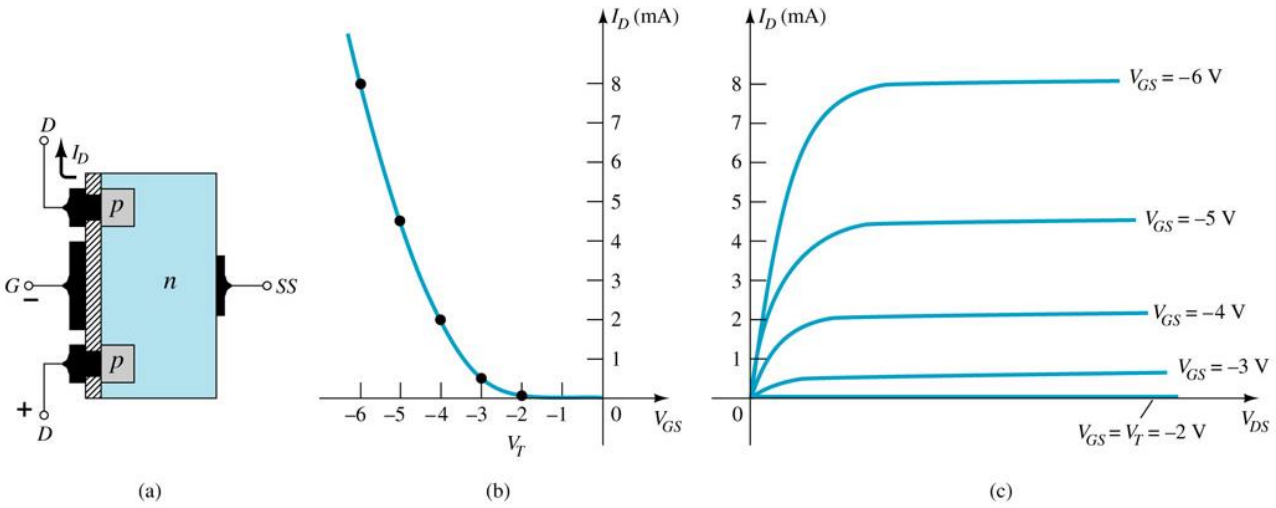
$$\mathbf{k = \frac{I_{D(on)}}{(V_{GS(ON)} - V_T)^2}}$$



P-CHANNEL ENHANCEMENT MODE MOSFETS:

The p-channel Enhancement mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.





Single Stage Amplifiers:

Amplifier is a device which increases the strength of the input signal applied. The amplification is done to improve the strength of the signal sometimes above the noise signal. Also in some cases the input signal is weak to drive a load of a subsequent stage.

Depending upon the amount of amplification to be done, the amplifiers are either single stage amplifiers or multi stage amplifiers i.e. more than one stage say two stage or three stage etc.

Figure 1: Amplifier Block Diagram

The Figure 1 shows the general Amplifier Block Diagram where input is taken as x(t) and output is taken as y(t)
The general Amplifier equation is given by:

$$y(t) = Ax(t)$$

Here **A** is called the gain.

NEED OF BIASING:

In electronics, **Biasing** is the setting of initial operating conditions (current and voltage) of an active device in an amplifier. Many electronic devices, such as diodes, transistors and vacuum tubes, whose function is processing time-varying (AC) signals, also require a steady (DC) current or voltage at their terminals to operate correctly**. *This current or voltage is a bias.*** The AC signal applied to them is super-positioned on this DC bias current or voltage.

For proper working of a transistor, it is essential to apply external voltages of correct polarity across its emitter-base and collector-base junctions. This is *transistor biasing*.

Unlike BJTs, thermal runaway does not occur with FETs. However, the wide differences in maximum and minimum transfer characteristics make I_D levels unpredictable with simple fixed-gate bias voltage. To obtain reasonable limits on quiescent drain currents I_D and drain-source voltage V_{DS}, source resistor and potential divider bias techniques must be used. With few exceptions, MOSFET bias circuits are similar to those used for JFETs.

Field Effect Transistor (FET) amplifiers provide an excellent voltage gain and high input impedance. Because of high input impedance and other characteristics of JFETs they are preferred over BJTs for certain types of applications. They are also low-power-consumption configurations with good frequency range and minimal size and weight.

There are 3 basic FET circuit configurations:

i)Common Source
ii)Common Drain
iii) Common Gain

Similar to BJT CE, CC and CB circuits, only difference is in BJT large output collector current is controlled by small input base current whereas FET controls output current by means of small input voltage. In both the cases output current is controlled variable. FET amplifier circuits use voltage-controlled nature of the JFET. In Pinch off region, I_D depends only on V_{GS}.

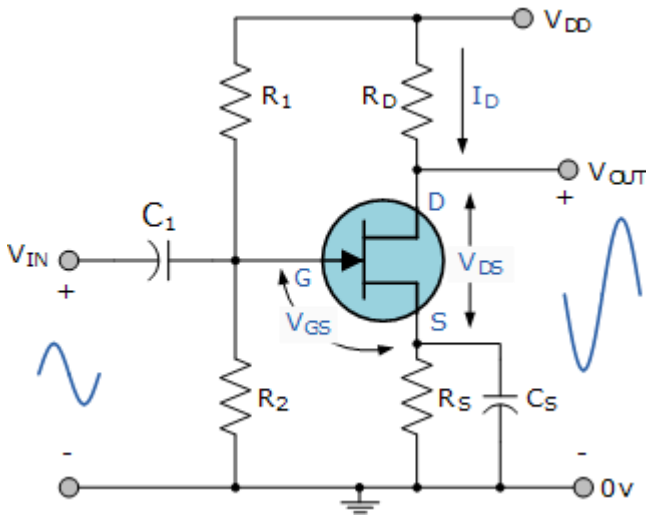
The Junction Field Effect Transistor (JFET) can be operated mainly in three regions. Those are the Cut-off, Ohmic and Saturation regions. We must operate the JFET in the Ohmic or linear regions for amplification. We will use the respective JFET amplifier based on the requirement.

JFET Amplifier / Common Source JFET Amplifier:

The common source JFET amplifier has one important advantage compared to the common-emitter BJT amplifier in that the FET has an extremely high input impedance and along with a low noise output makes them ideal for use in amplifier circuits that require very small input voltage signals.

Transistor amplifier circuits such as the common emitter amplifier are made using Bipolar Transistors, but small signal amplifiers can also be made using Field Effect Transistors. The design of an amplifier circuit based around a junction field effect transistor or "JFET" or even a metal oxide silicon FET or "MOSFET" is exactly the same principle as that for the bipolar transistor circuit.

A suitable quiescent point or "Q-point" needs to be found for the correct biasing of the JFET amplifier circuit with single amplifier configurations of Common-source (CS), Common-drain (CD) or Source-follower (SF) and the Common-gate (CG) available for most FET devices. **Common Source JFET Amplifier** as this is the most widely used JFET amplifier design.



The JFET gate voltage Vg is biased through the potential divider network set up by resistors R_1 and R_2 and is biased to operate within its saturation region which is equivalent to the active region of the bipolar junction transistor.

Unlike a bipolar transistor circuit, the junction FET takes virtually no input gate current allowing the gate to be treated as an open circuit. Then no input characteristics curves are required. Since the N-Channel JFET is a depletion mode device is normally "ON" with a negative gate to source voltage is required to modulate or control the drain current. This negative voltage can be provided by biasing from a separate power supply voltage or by a self-biasing arrangement as long as a steady current flows through the JFET even when there is no input signal present, and Vg maintains a reverse bias of the gate-source p-n junction.

The biasing is provided from a potential divider network allowing the input signal to produce a voltage fall at the gate as well as voltage rise at the gate with a sinusoidal signal.

Any suitable pair of resistor values in the correct proportions would produce the correct biasing voltage so the DC gate biasing voltage Vg is given as:

$$V_G = \frac{V_{DD}\,R_2}{R_1 + R_2} = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

Note that this equation only determines the ratio of the resistors R_1 and R_2, but in order to take advantage of the very high input impedance of the JFET as well as reducing the power dissipation within the circuit, we need to make these resistor values as high as possible, with values in the order of 1MΩ to 10MΩ being common.

The input signal, (Vin) of the common source JFET amplifier is applied between the Gate terminal and the zero volts rail, (0v). With a constant value of gate voltage Vg applied the JFET operates within its "Ohmic region" acting like a linear resistive device. The drain circuit contains the load resistor, R_d. The output voltage, V_{out} is developed across this load resistance.

The efficiency of the common source JFET amplifier can be improved by the addition of a resistor, R_s included in the source lead with the same drain current flowing through this resistor. Resistor, R_s is also used to set the JFET amplifiers "Q-point".

When the JFET is switched fully "ON" a voltage drop equal to $R_s * I_d$ is developed across this resistor raising the potential of the source terminal above 0v or ground level. This voltage drop across Rs due to the drain current provides the necessary reverse biasing condition across the gate resistor, R_2 effectively generating negative feedback.

So in order to keep the gate-source junction reverse biased, the source voltage, Vs needs to be higher than the gate voltage, Vg. This source voltage is therefore given as:

$$V_S = I_D \times R_S = V_G - V_{GS}$$

Then the Drain current, I_d is also equal to the Source current, I_s as "No Current" enters the Gate terminal and this can be given as:

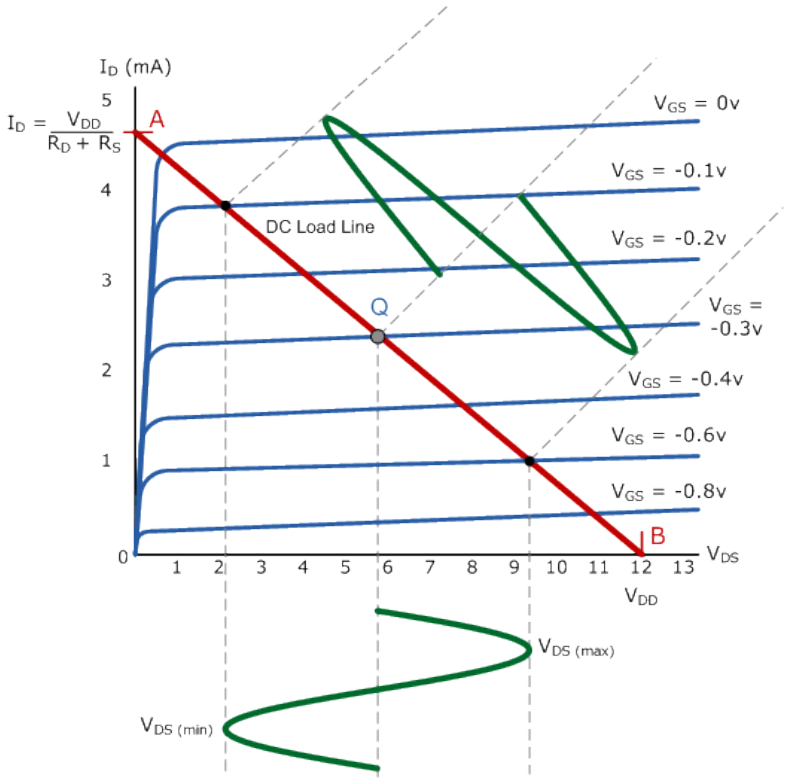
$$I_D = \frac{V_S}{R_S} = \frac{V_{DD}}{R_D + R_S}$$

This potential divider biasing circuit improves the stability of the common source JFET amplifier circuit when being fed from a single DC supply compared to that of a fixed voltage biasing circuit. Both resistor, R_s and the source by-pass capacitor, C_s serve basically the same function as the emitter resistor and capacitor in the common emitter bipolar transistor amplifier circuit, namely to provide good stability and prevent a reduction in the loss of the voltage gain. However, the price paid for a stabilized quiescent gate voltage is that more of the supply voltage is dropped across R_s.

Then the value in farads of the source by-pass capacitor is generally fairly high above 100uF and will be polarized. This gives the capacitor an impedance value much smaller, less than 10% of the transconductance, g_m (the transfer coefficient represents gain) value of the device. At high frequencies the by-pass capacitor acts essentially as a short-circuit and the source will be effectively connected directly to ground.

The basic circuit and characteristics of a **Common Source JFET Amplifier** are very similar to that of the common emitter amplifier. A DC load line is constructed by joining the two points relating to the drain current, I_d and the supply voltage, V_{dd} remembering that when I_d = 0: ($V_{dd} = V_{ds}$) and when V_{ds} = 0: ($I_d = V_{dd}/R_L$). The load line is therefore the intersection of the curves at the Q-point as follows.

Common Source JFET Amplifier Characteristics Curves



As with the common emitter bipolar circuit, the DC load line for the common source JFET amplifier produces a straight line equation whose gradient is given as: $-1/(R_d + R_s)$ and that it crosses the vertical I_d axis at point A equal to $V_{dd}/(R_d + Rs)$. The other end of the load line crosses the horizontal axis at point B which is equal to the supply voltage, V_{dd}.

The actual position of the Q-point on the DC load line is generally positioned at the mid center point of the load line (for class-A operation) and is determined by the mean value of V_g which is biased negatively as the JFET is a depletion-mode device. The output of the **Common Source JFET Amplifier** is 180^o out of phase with the input signal.

One of the main disadvantages of using Depletion-mode JFET is that they need to be negatively biased. Should this bias fail for any reason the gate-source voltage may rise and become positive causing an increase in drain current resulting in failure of the drain voltage, V_d.

Also the high channel resistance, $R_{ds(on)}$ of the junction FET, coupled with high quiescent steady state drain current makes these devices run hot so additional heatsink is required. However, most of the problems associated with using JFET's can be greatly reduced by using enhancement-mode MOSFET devices instead.

MOSFET's or Metal Oxide Semiconductor FET's have much higher input impedance's and low channel resistances compared to the equivalent JFET. Also the biasing arrangements for MOSFETs are different and unless we bias them positively for N-channel devices and negatively for P-channel devices no drain current will flow, then we have in effect a fail safe transistor.

Performance Parameters of JFET

1. **AC Drain Resistance:** The ratio of change in voltage across the drain-source terminal and the change in drain current is termed as AC drain resistance. But the ratio should be considered at a point when the gate-source voltage is kept constant. Its value is in range of 10 kΩ to 1 MΩ. It is also referred as **dynamic resistance (r_d),** it should not be confused with the resistance of channel (R_{DS}), R_{ds} is purely DC while r_d is not.

AC Drain Resistance (r_d)

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

2. **DC Drain Resistance:** R_{DS} is a symbol used for DC drain resistance. It is the ratio between the change in drain-source voltage and the change in drain current. The value of DC drain resistance is static. Thus it is also termed as **static or ohmic resistance.**

DC Drain Resistance (R_{DS})

$$R_{DS} = \frac{V_{DS}}{I_D}$$

3. **Transconductance:** It is the ratio between the change in drain current and the change in gate-source voltage but at constant drain-source voltage. It is represented by gm.

Transconductance(g_m)

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

4. **Amplification factor:** The amplification factor is obtained by determining the ratio between the change in drain-source voltage with respect to change in gate-source voltage but keeping the value of drain current constant.

Amplification factor (μ)

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

It is represented by μ. The value of amplification factor can be high as 100.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta V_{DS}}{\Delta V_{GS}} = r_d \times g_m$$

μ = Ac drain resistance × transconductance

The Significance of the amplification factor is that it helps to determine the control of gate to source voltage on the value of drain current in comparison to that of the drain to source voltage.

JFET Amplifier Current and Power Gains

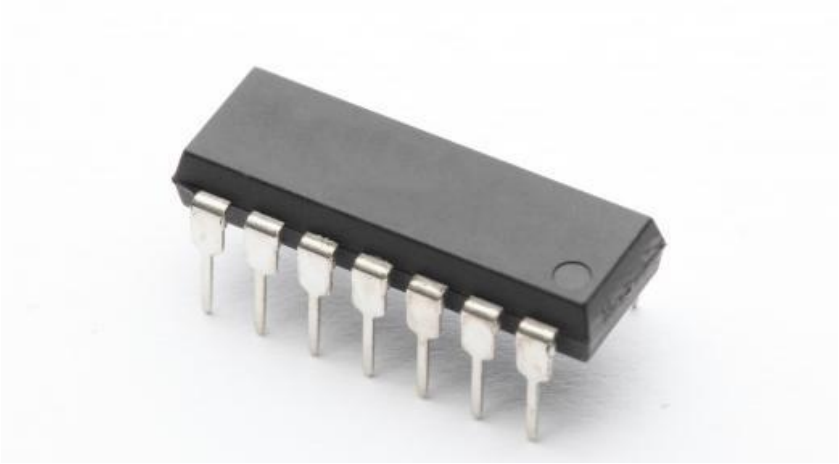
The input current(I_g) of a common source JFET amplifier is very small because of the extremely high gate impedance, R_g. A common source JFET amplifier therefore has a very good ratio between its input and output impedances and for any amount of output current, I_{OUT} the JFET amplifier will have very high current gain Ai.

Because of this common source JFET amplifiers are extremely valuable as impedance matching circuits are used as voltage amplifiers. Likewise, because: Power = Voltage x Current, (P = V*I) and output voltages are usually several millivolts or even volts, the power gain, A_p is also very high.

What is a complementary metal-oxide semiconductor (CMOS)?

A complementary metal-oxide semiconductor (CMOS) is the semiconductor technology used in most of today's integrated circuits (ICs), also known as *chips* or *microchips*. CMOS transistors are based on metal-oxide semiconductor field-effect transistor (MOSFET) technology. MOSFETs serve as switches or amplifiers that control the amount of electricity flowing between source and drain terminals, based on the amount of applied voltage.

There are two primary types of MOSFETs: p-channel MOS (PMOS) and n-channel MOS (NMOS). Both PMOS and NMOS transistors use p-type and n-type semiconductors. In a PMOS transistor, the source and drain use a p-type semiconductor, and the substrate uses an n-type semiconductor. An NMOS transistor takes the opposite approach. The source and drain use an n-type semiconductor, and the substrate uses a p-type semiconductor.



Before the introduction of CMOS, PMOS and NMOS were widely used in electronic devices. NMOS eventually became the favored approach to integrated circuitry because it was faster and cheaper to produce, although it was not without its own limitations, such as its static power consumption.

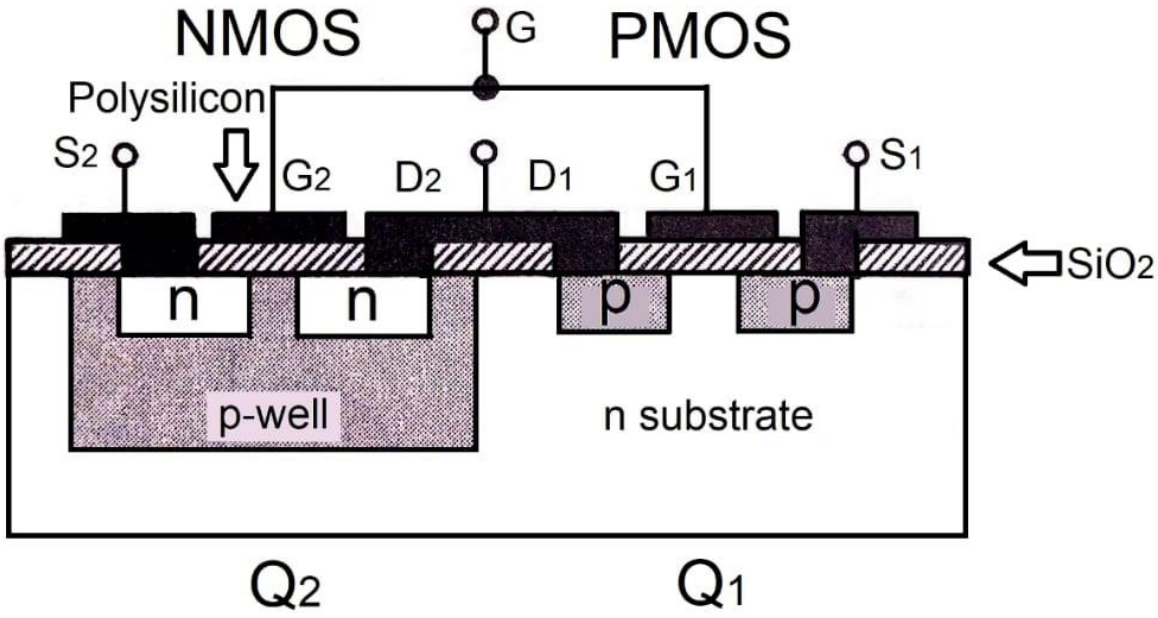
CMOS addressed the issues inherent in PMOS and NMOS by incorporating both types in a single IC that contains symmetrical (complementary) PMOS-NMOS pairs. When used together, the two types of transistors provide greater flexibility in circuitry design, while reducing complexity and susceptibility to electronic noise.

Another advantage of complementary PMOS-NMOS pairs is that they require less power. This is because current is applied briefly when switching between on and off states. In fact, CMOS ICs use almost no power during static conditions. By extension, the lower power consumption also means that CMOS-based ICs generate less heat, compared to those based on either PMOS or NMOS alone.

Because power consumption and heat generation are two core concerns in designing ICs, CMOS logic is now widely used in microprocessors, microcontrollers, static RAM, image sensors and other ICs. By all accounts, its use will continue to dominate the industry.

COMPLEMENTARY METAL OXIDE SEMICONDUCTOR(CMOS):

- The term CMOS stands for "Complementary Metal Oxide Semiconductor". This one is the most popular technology in the computer chip design industry and it is broadly used today to form integrated circuits in numerous and varied applications.
- This technology makes use of both P channel and N channel semiconductor devices.
- One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology.
- This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application-specific integrated circuits (ASICs).
- In CMOS gate both the NMOS and PMOS transistors are implemented on the same chip. A p-channel is induced on the right and an n-channel on the left for the p- and n-channel devices.
- In this arrangement, the PMOS transistor is carried out directly in the n-type substrate (body) and the NMOS transistor in a p-type region commonly referred to as the p-well.
- A well is a significant, low-doping-level deep diffusion that functions as the substrate for one device and offers isolation between the two device types.
- The importance of CMOS in semiconductor technology is its low power dissipation and low operating currents. It is manufactured using fewer steps as compared to the Bipolar Junction transistors.



- The n-channel MOSFET is called NMOS. It has a substrate of p-type, which consists of the majority carrier's holes.

- The n-channel consists of the majority carrier's electrons. The flow of electrons is fast as compared to holes.
- Hence, NMOS transistors are more rapid than PMOS transistors.
- The p-channel MOSFET is called PMOS. It has a substrate of n-type, which consists of the majority carrier's electrons.
- When a negative voltage is applied to the gate end of the PMOS, it repels the electrons.
- The attraction of holes results in the formation of the channel called the p-channel. The channel is formed between the source and drain.
- The slow flow of holes makes the current controlled process of PMOS easy as compared to NMOS transistors.

What is a CMOS :

The term CMOS stands for "Complementary Metal Oxide Semiconductor". This is one of the most popular technology in the computer chip design industry and it is broadly used today to form integrated circuits in numerous and varied applications. Today's computer memories, CPUs, and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices. One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application-specific integrated circuits (ASICs).

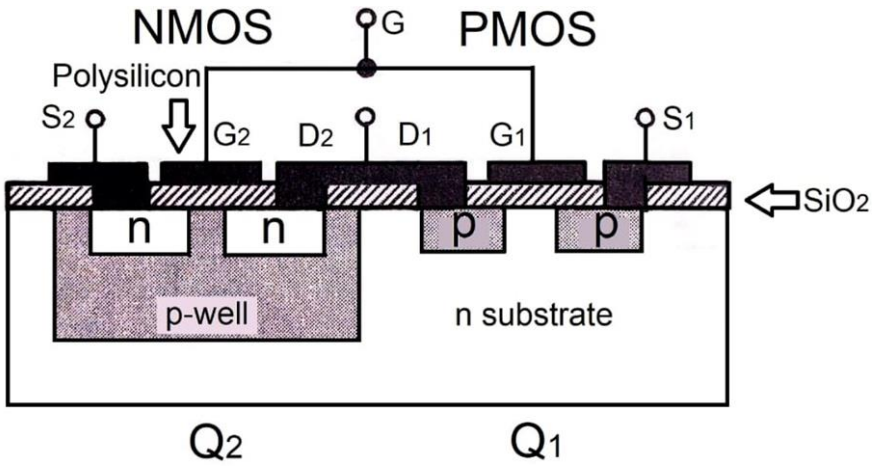
Introduction to MOS Technology

In the IC design, the basic and most essential component is the transistor. So MOSFET is one kind of transistor used in many applications. The formation of this transistor can be done like a sandwich by including a semiconductor layer, generally a wafer, a slice from a single crystal of silicon; a layer of silicon dioxide & a metal layer. These layers allow the transistors to be formed within the semiconductor material. A good insulator like Sio2 has a thin layer with a hundred molecules thickness.

The transistors which we use polycrystalline silicon (poly) instead of metal for their gate sections. The Polysilicon gate of FET can be replaced almost using metal gates in large scale ICs. Sometimes, both polysilicon & metal FET's are referred to as IGFET's which means insulated gate FETs, because the Sio2 below the gate is an insulator.

CMOS (Complementary Metal Oxide Semiconductor):

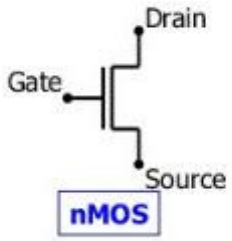
The main advantage of CMOS over NMOS and BIPOLAR technology is the much smaller power dissipation. Unlike NMOS or BIPOLAR circuits, a Complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows integrating more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. Complementary Metal Oxide Semiconductor transistor consists of P-channel MOS (PMOS) and N-channel MOS (NMOS). Please refer to the link to know more about the fabrication process of CMOS transistor.



CMOS (Complementary Metal Oxide Semiconductor)

NMOS:

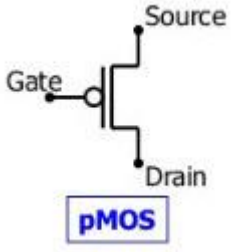
NMOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority of carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.



NMOS Transistor

PMOS:

P- channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate. The majority of carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices.

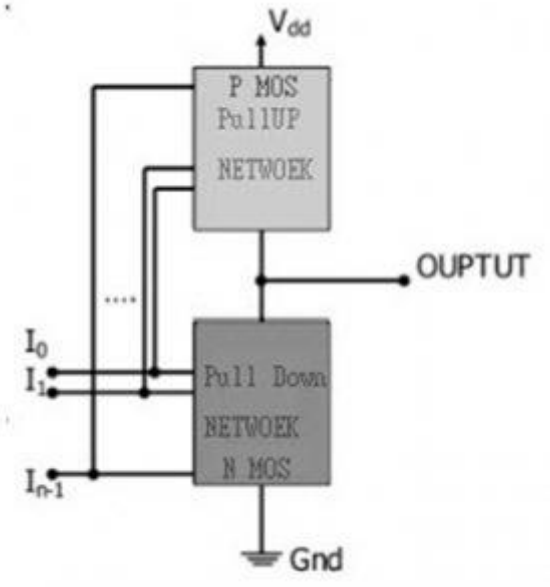


PMOS Transistor

CMOS Working Principle:

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.

In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).



CMOS using Pull Up & Pull Down

Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern as shown in the figure below.

CMOS offers relatively high speed, low power dissipation, high noise margins in both states, and will operate over a wide range of source and input voltages (provided the source voltage is fixed). Furthermore, for a better understanding of the Complementary Metal Oxide Semiconductor working principle, we need to discuss in brief CMOS logic gates as explained below.

Which Devices use CMOS?

Technology like CMOS is used in different chips like microcontrollers, microprocessors, SRAM (static RAM) & other digital logic circuits. This technology is used in a wide range of analog circuits which includes data converters, image sensors & highly incorporated transceivers for several kinds of communication.

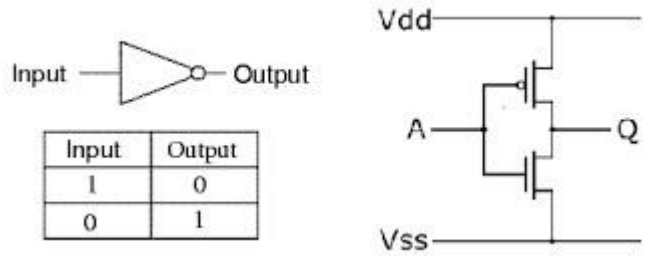
CMOS as an Invertor

Introduction

CMOS is a type of MOSFET, where its fabrication process uses complementary & symmetrical P-type & N-type MOSFET pairs for logic functions. The main CMOS devices characteristics are consumption of low static power & high noise immunity. The inverter is accepted universally as the basic logic gate while performing a Boolean operation on a single i/p variable. A basic inverter circuit is used to accomplish a logic variable by complementing from A to A'. So, a CMOS inverter is a very simple circuit, designed with two opposite-polarity MOSFETs within a complementary way.

What is CMOS Inverter?

CMOS inverter definition is a device that is used to generate logic functions is known as CMOS inverter and is the essential component in all integrated circuits. A CMOS inverter is a FET (field effect transistor), composed of a metal gate that lies on top of oxygen's insulating layer on top of a semiconductor. These inverters are used in most electronic devices which are accountable for generating data n small circuits.

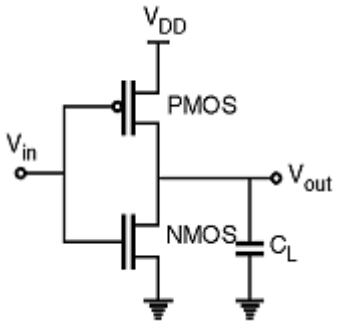


Input	Output
1	0
0	1

CMOS Inverter Symbol & Truth Table

CMOS Inverter Schematic Diagram

The logic element like an inverter reverses the applied input signal. In digital logic circuits, binary arithmetic & switching or logic function's mathematical manipulation are best performed through the symbols 0 & 1. The CMOS inverter truth table is shown above. If the input logic is zero (0) then the output will be high (1) whereas, if the input logic is one (1), then the output will be low (0).



CMOS Inverter Circuit

The CMOS inverter circuit diagram is shown below. The general CMOS inverter structure is the

combination of both the PMOS & NMOS transistors where the pMOS is arranged at the top & nMOS is arranged at the bottom.

The connection of both the PMOS & NMOS transistors in the CMOS inverter can be done like this. The NMOS transistor is connected at the drain (D) & gate (G) terminals, a voltage supply (VDD) is connected at the source terminal of PMOS & a GND terminal is connected at the source terminal of NMOS. Input voltage (Vin) is connected to both the gate terminals of transistors & output voltage (Vout) is connected to the drain (D) terminals of the transistor.

It is very significant to observe that the CMOS device does not have any resistors, so it will be more power-efficient. Once the input voltage of CMOS changes between 0 to 5 volts, then both the transistors state will be changed accordingly. If we design every transistor like a simple switch that is operated through input voltage (Vin), then operations of the inverter can be observed very simply.

CMOS Inverter Operation & Working

The working of CMOS inverter is the same as other types of FETs except depends on an oxygen layer to divide electrons within the gate & semiconductor. They are designed with a power supply, input voltage terminal, output voltage, gate, drain, and PMOS & NMOS transistors which are connected to the gate & the drain terminals.

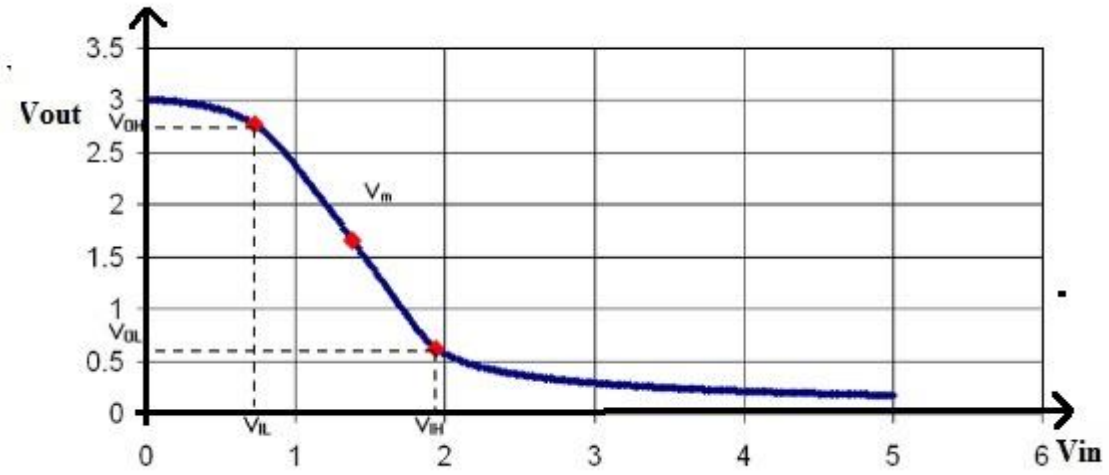
When the low input voltage is given to the CMOS inverter, then the PMOS transistor is switched ON whereas the NMOS transistor will switch OFF by allowing the flow of electrons throughout the gate terminal & generating high logic output voltage.

Similarly, when the high input voltage is given to the CMOS inverter then, the PMOS transistor is switched OFF whereas the NMOS transistor will be switched ON avoiding as many electrons from attaining the output voltage & generating low logic output voltage.

Thus, direct current supplies from the supply voltage (VDD) to the output voltage (Vout) & the load capacitor (CL) can be charged and shows that Vout = VDD. As a result, the above circuit works like an inverter.

Inverter Static Characteristics or VTC

The quality of the inverter can be measured frequently by using the VTC or voltage transfer curve, which is plotted between input voltage (Vin) and output voltage (Vo). From the following static characteristics, the parameters of devices like gain, operating logic levels & noise tolerance, and noise can be obtained.



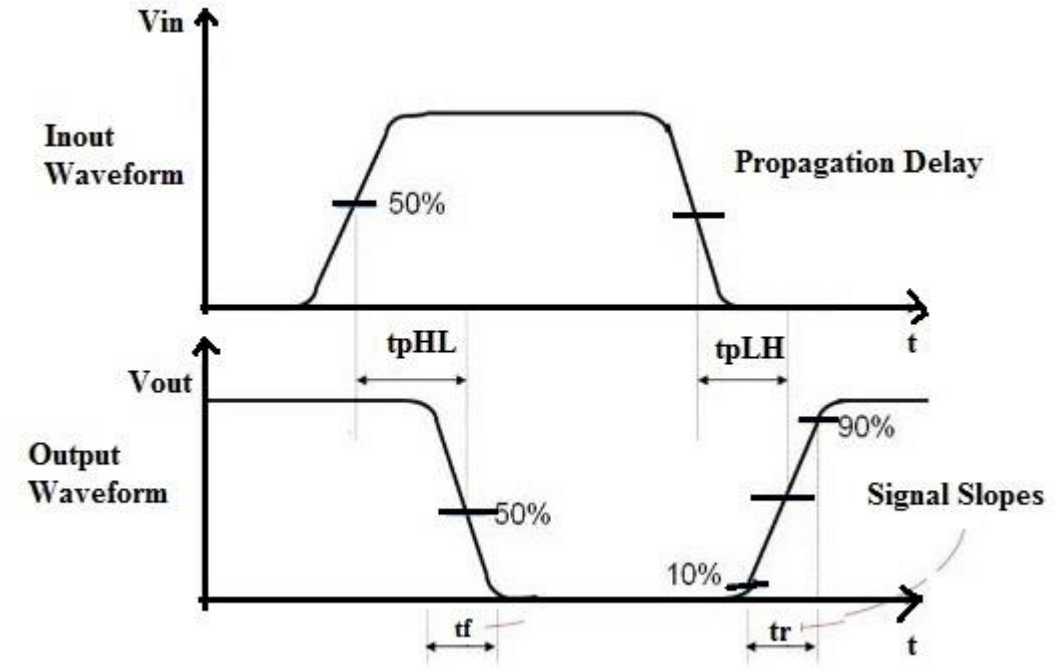
Voltage Transfer Curve:

The VTC or voltage transfer curve looks like an inverted step-function that specifies accurate switching in between ON & OFF however in real devices, a gradual transition region exists. The voltage transfer curve specifies that for less input voltage Vin, the circuit generates high voltage Vout, whereas, for high input, it generates 0 volts.

The transition region slope is a measure of quality – steep slopes yield exact switching. The tolerance toward noise can be calculated by evaluating the smallest input to the highest output for every region of ON or OFF operation.

Inverter Dynamic Characteristics

The CMOS inverter dynamic characteristics are shown below. So, some of the following formal definitions of different parameters are discussed below. Here, all the percentage (%) values are the steady-state values.



Dynamic Characteristics of CMOS Inverter

- Rise Time or tr: Rise time is the time used to increase the signal from 10% to 90%.
- Fall Time or tf: Fall time is the time used to drop the signal from 90% to 10%
- Edge Rate or trf : It is (tr + tf)/2.
- The propagation delay from high to low or tpHL: The time used to drop from VOH – 50%.
- The propagation delay from low to high or tpLH: The time used to increase from 50%- VOL.
- Propagation Delay or tp: It is (tpHL + tpLH)/2.
- Contamination Delay or tcd: It is the smallest time from the 50% input crossing to the 50% output crossing.

Advantages:

- The CMOS inverter's steady-state power dissipation is negligible virtually, apart from small power dissipation because of leakage currents.
- The VTC (voltage transfer characteristic) exhibits a complete o/p voltage swing in between 0 V & VDD, and the transition of voltage transfer characteristic is normally very sharp. Thus, the characteristics of the CMOS inverter look like an ideal inverter.
- These inverters use electricity once they are switched ON & OFF resulting in less power consumption. As a result, these inverters generate extremely less waste heat to make them highly efficient, so used in small and delicate electronic devices.

- These inverters include high noise immunity, which lets them block both incoming & outgoing frequency spikes.
- These are low-cost to produce mass.

Disadvantages:

- As compared to other inverters, the switching speed of the CMOS inverter is high.
- These are very difficult to fabricate due to both the transistors used on the same Silica piece.
- It uses two transistors to make an inverter, so it uses more space on the IC as compared to the NMOS inverter.

Applications:

The applications of CMOS inverters include the following.

- CMOS inverters are used in different ICs (integrated circuits) like microprocessors, static RAM, microcontrollers, data converters, image sensors & transceivers.
- These are found in mobile devices, digital cameras, home computers, cell phones, routers, network servers, modems & virtually each other electronic device that needs logic functions.