

# Design of a Fully Differential Operational Amplifier with Adjustable Output Common-Mode Voltage

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*Abstract—This project focuses on implementing fully differential operational amplifier with adjustable output common mode voltage including reference circuit and DAC by using XFAB XH018 (180nm High Voltage CMOS) technology using Cadence Virtuoso. Variation of the reference voltage with temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  is less than 1.12%. Variation with supply voltage in the range of 1.2V to 3.3V is 1.16 %. Current consumption is 149.6 nA. PSRR of the reference circuit is 91.26 dB @50kHz. Op-amp has current consumption of 279.4  $\mu\text{A}$ , DC gain of 84.9 dB, unity-gain bandwidth of 76.4 MHz, phase margin of 59.7°, slew rate of 40.29 V/us when load capacitance is 5pF, PSRR of 102.04 dB, CMRR of 166.71 dB @50kHz, output common mode range of adjustable between 0.6V to 1.5V, input common mode range of -0.3V to 2.2V, current driving capability of 29.2  $\mu\text{A}$ . Nominal value of the supply voltage is 3.3V. In this paper overall circuit operation is explained, simulation results including PVT corner analysis are shared.*

**Keywords—OP-AMP, Reference Circuit, Low Pass Filter, Subthreshold, Folded Cascode, Common-Mode Feedback, Adjustable Output Common Mode Level**

## I. INTRODUCTION

Fully differential op-amps are highly used devices in analog electronics and communication systems. Moreover, providing a high gain with low power consumption, and supporting a wide range of input common mode voltages together with an adjustable common mode voltage are quite important specifications for the today's op-amps. At the same time, preserving the functionality under different temperature and supply voltages are crucial for high performance reference circuits. Therefore, in this paper, a high gain fully differential op-amp with adjustable output common mode voltage, and a high performance, low power reference circuit are designed. The proposed op-amp and reference circuit are verified with simulations in Cadence environment, providing promising results. Moreover, the design is also verified with a simple application circuit with a Digital-to-Analog Converter (DAC), where the current output of the DAC is converted to a differential voltage, and the output common mode voltages are set to a desired value using the designed op-amp.

## II. CIRCUIT ARCHITECTURE AND DESIGN PROCEDURE

In this part, the circuit architecture of the designed fully differential operational amplifier with adjustable output common-mode voltage, and the following design procedure are explained in detail. The overall circuit consists of five main parts. First, a two stage fully differential amplifier with high gain, high input and output common mode ranges, low power, and high unity-gain frequency is designed. In the first stage, a folded-cascode amplifier with PMOS inputs to obtain

large input common mode range, and to support slightly negative voltages, is used. As the second stage, to boost the gain and obtain large output common mode range, an NMOS common source topology is used. Since the fully differential architecture requires equalizing the output common-mode voltages to operate properly, a common-mode feedback circuit is designed using an active loaded, single-ended differential amplifier. With the help of this feedback loop, the output common mode voltage can be set to any value between 0.6V and 1.5V by giving an external  $V_{cm}$  input. To sense the common mode voltage, two NMOS transistors are used. The common-mode feedback loop is designed such that the loop stability is ensured. Similarly, to ensure stability and increase the phase margin, frequency compensation is used with precise right half plane zero placement. Moreover, to supply bias voltages and currents, a high-performance reference circuit is designed with low power consumption, low temperature and supply dependency, low PSRR, and large supply voltage range support. Using the reference voltage generated by the designed reference circuit, a biasing stage is designed with low power consumption to create necessary bias voltages for the amplifier. After completing the op-amp, an application circuit with DAC, where the current output of the DAC is converted to a differential voltage using the designed op-amp, is designed and constructed. In the following sub-sections, the architectures and design procedures of the sub-blocks are presented.

### A. Two Stage Fully Differential Folded Cascode / Common Source Amplifier

For the fully differential amplifier, two stages are used. In the first stage, folded cascode architecture is chosen to obtain high gain and wide input common mode range. PMOS transistors are used as the input transistors since the amplifier should support slightly negative input common mode voltages. The drawback of this input stage topology is relatively high-power consumption. Therefore, biasing currents should be chosen carefully.

As the second stage, common source configuration is chosen to increase both gain and output common mode range. For high gain, NMOS transistors are used in the second stage due to their greater electron mobility. The schematic of the two-stage amplifier is shown in Figure 1. The gain and output resistance expressions are also given in Equation 1 and 2, respectively. It can be clearly seen that high gain values with high input and output common mode ranges can be achieved by using this two-stage topology with the cost of high output resistance, which can cause problematic dominant poles and decrease bandwidth of the amplifier.

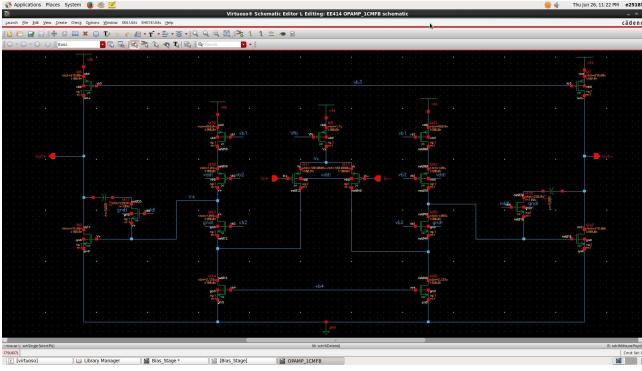


Fig. 1. Two-stage fully differential folded cascode/common source amplifier

$$A_{d,de} = g_{m11}[g_{m40}r_{o40}r_{o39} // g_{m43}r_{o43}(r_{o44}//r_{o11})] \cdot g_{m9}(r_{o9}//r_{o6}) \quad (1)$$

$$R_{OUT} = r_{o9}//r_{o6} \quad (2)$$

As the design procedure, first, the biasing currents are determined according to the power dissipation and slew rate specifications. Initially, the allocated currents for the first and second stages are 200  $\mu$ A and 100  $\mu$ A, respectively. In the first stage, 200  $\mu$ A current is allocated symmetrically in a way that 50  $\mu$ A current is passing through each input PMOS transistor. Then, according to the input and output common mode range specifications, bias voltages (vb1, vb2, vb3, vb4) are determined roughly. When the bias voltages and currents are selected, W/L ratios are obtained based on the current expression in saturation region with a rough hand calculation. Obviously, the circuit cannot operate properly in the first iteration. Therefore, several iterations for the bias voltages and W/L ratios are done until a satisfactory result is obtained.

In this topology, there are two critical nodes with high resistance and capacitance for frequency response of the amplifier. These nodes are the output nodes of the first and second stages. In the output node, 5 pF load capacitors are used according to the project specifications, which is a relatively high capacitance. Since the output resistance of the common source configuration is also high, the output node introduces a critical pole which is approximately given in Equation 3. Moreover, for stability, frequency compensation technique is used. Between the output of the first and second stages, a capacitor is added in series with an NMOS transistor. The NMOS transistor is designed to operate in linear region where it acts as a voltage controllable resistor. Due to Miller effect, the compensation capacitor is multiplied by the gain and reflected to the first stage. In this way, the critical pole at the output of the first stage is shifted toward left to ensure stable operation with 60° degree phase margin. A very rough approximation for the critical pole at the output of the first stage after Miller compensation is given in Equation 4. However, this compensation also results in a right half plane zero, whose approximate formula is given in Equation 5, which affects the frequency response. This right half plane zero should be placed very carefully and precisely to cancel a critical pole, or to place it at infinity.

The unity-gain bandwidth is directly related to the added compensation capacitor according to the approximate expression given in Equation 6. Therefore, first, according to

the unity-gain bandwidth specification, the compensation capacitor is chosen as 500 fF by parametric sweep simulations. Then, to ensure stable amplifier with 60° degree phase margin, length and width of the NMOS transistor in linear region are obtained by again parametric sweep simulations, which actually imitates the  $R_Z$  resistor.

$$\omega_{p1} \approx \frac{1}{(r_{o9}/r_{o6})C_L} \quad (3)$$

$$\omega_{p2} \approx \frac{1}{[g_{m40}r_{o40}r_{o39} // g_{m43}r_{o43}(r_{o44}/r_{o11})] * [C_C * g_{m9}(r_{o9}/r_{o6})]} \quad (4)$$

$$\omega_Z = \frac{g_{m9}}{C_C * (R_Z g_{m9} - 1)} \quad (5)$$

$$\text{Unity - Gain Bandwidth} = \frac{g_{m11}}{C_C} \quad (6)$$

### B. Common Mode Feedback Circuit

The designed operational amplifier is fully differential. Therefore, it has a significant drawback that should be handled. Since the output is taken differentially, the common mode voltages at the two outputs should be exactly the same to have a non-distorted differential signal. However, these nodes are normally floating, and their voltages can obtain a range of values where the NMOS and PMOS transistors in the output common source stage stay in saturation region. Therefore, a special technique called common mode feedback should be used to define a single, stable common mode voltage at both outputs. In the presented design, the output common mode voltage can be set to a desired value with an external input  $V_{CM}$ .

There are two parts in the common mode feedback loop: common mode sensing and feedback circuits, which are shown in Figure 2. First, the actual output common mode voltages are sensed with two resistors. Two NMOS transistors are used replacing the resistors. The gates of these NMOS transistors are short-connected to their source terminals. In this way, no channel is formed, and it leads to a very high resistance, which reduces the effect of common mode sensing to the overall gain and the output resistance. After sensing the output common mode voltage called "VCM\_stage2" in the schematic, it is compared with the external input  $V_{CM}$  which is the desired output common mode voltage by using a simple active loaded, single ended differential amplifier. If the transistors are managed to operate in saturation region, VCM and VCM\_stage2 should be the same since their sources are connected to each other, and the currents are matched (equal) with the help of the upper current mirror (active load). The feedback output  $V_{FB}$  is fed back to the gate of the PMOS bias transistor M8 of the input transistors, as shown in Figure 1. With this feedback, the active loaded differential amplifier arranges the bias of M8 such that the actual common mode VCM\_stage2 and the external common mode input  $V_{CM}$  become equal. The bias voltage  $v_{b4}$  and W/L ratios of the transistors are selected considering the output common mode range specification ensuring all transistors stay in saturation region across the

whole range, and loop stability. The CMFB loop gain expression is given in Equation 7. This loop gain of the CMFB network is adjusted such that the fully differential amplifier with the feedback loop is stable.

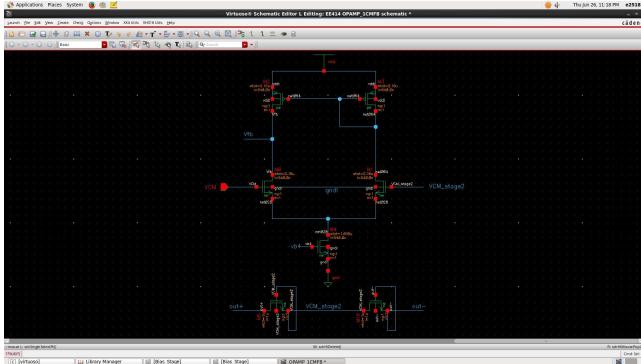


Fig. 2. Common mode sensing and feedback circuits

$$A_{CMFB} = \frac{1}{2} g_{m8} g_{m1} (r_{o1}/r_{o2}) * [g_{m40} r_{o4} r_{o39} / (g_{m43} r_{o43} (r_{o44}/r_{o11})) * g_{m9} (r_{o9}/r_{o6})] \quad (7)$$

### C. Reference Circuit

In order to ensure that the operational amplifier can cope with extreme conditions which will be tested later by corner analysis, temperature and supply independent reference circuit must be used before the biasing stage. In Figure 3, reference circuit topology is shown. In this topology to yield minimum current consumption, each transistor except M2 and M13 operate in subthreshold region. M2 operates in linear region, and it transforms current coming from drain terminal to reference voltage. Reference circuit degrades the TCF to 0 in particular temperature to obtain desired reference voltage by neutralizing negative and positive thermal coefficient of the current that sinks to M2 transistor. Aspect ratio of the transistors M2-M7 are adjusted such that TCF=0 point is at 25 °C by Equation 8. W0-7 is aspect ratio of the transistor M0-7,  $K_B$  is referred to Boltzman constant, T is temperature in Kelvin, m is the coefficient of threshold voltage with respect to temperature [1].

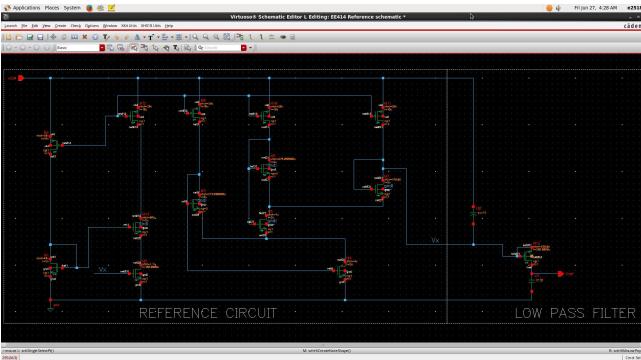


Fig. 3. Reference circuit

$$\frac{dV_{ref}}{dT} = -m + \frac{n \cdot K_B}{q} \ln \left( \frac{6nqm}{K_B(n-1)} \frac{w_2 w_3 w_5}{w_4 w_6 w_7} \ln \left( \frac{w_0}{w_1} \right) \right) \quad (8)$$

After obtaining temperature and supply independent reference voltage, by making sweep simulation of W/L ratio of the M14, reference voltage is adjusted to 900 mV without going into strong inversion region. 900 mV is determined such that biasing circuit can operate as desired. Adjusting the aspect ratio of the M14 transistor shifts the TCF=0 point from 25 °C to 5 °C. However, temperature sensitivity is still quite acceptable in the full range of -40° C to +85° C as shown in the Result and Simulation section.

In order to increase the PSRR of the reference circuit, a low pass filter is added at the end of the reference circuit. Low pass filter composes of C4 and M13 whose gate is short connected to source terminal, so that no channel is formed at all, which leads to high resistance as desired to create a low pass filter. C4 value is determined such that low pass characteristics suppress the gain at 50kHz. C0 capacitor is also used for suppressing AC gain.

### D. Biasing Circuit

While designing differential amplifier, desired biasing voltages are determined as in Table 1.

TABLE I. BIAS VOLTAGES FOR THE DIFFERENTIAL AMPLIFIER

Vb1	Vb2	Vb3	Vb4
2.25V	1.5V	2.1V	0.9V

In the biasing circuit, different desired biasing voltages are obtained from reference voltage. At the schematic of biasing voltage shown in Figure 4, output of the reference circuit biases the M22 transistor. In the circuit there are three current branches. The current values of each branch are allocated as approximately 5 μA. It is determined such that current consumption of overall op-amp does not exceed 300 μA. After determining branch current, the aspect ratio of each transistor is determined to obtain the required bias voltages by using saturation current equation. It is worth noting that even though Vref is exactly equal to Vb4, Vref cannot be directly biased the differential amplifier since the driving capability of the reference circuit is low. Therefore, Vb4 is obtained through the same current mirror approach.

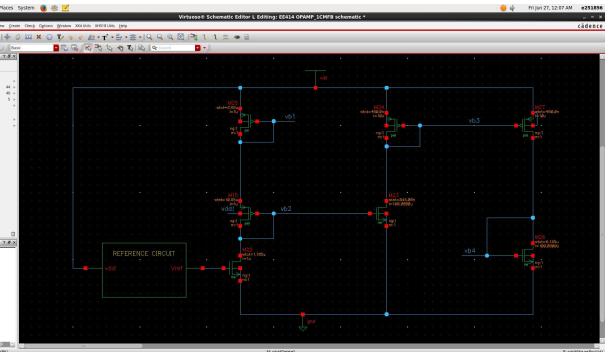


Fig. 4. Biasing circuit

### E. Application Circuit with DAC

For implementing Digital-to-Analog Converter, simple current sources and resistor are used as shown in Figure 5. AC voltage for differential inputs of the op-amp is obtained

by AC current going through the  $1\Omega$  resistor. Current sources model analog output of the DAC. Common mode level of the output of the DAC is floating therefore output common mode level should be stabilized through the common mode feedback circuit.

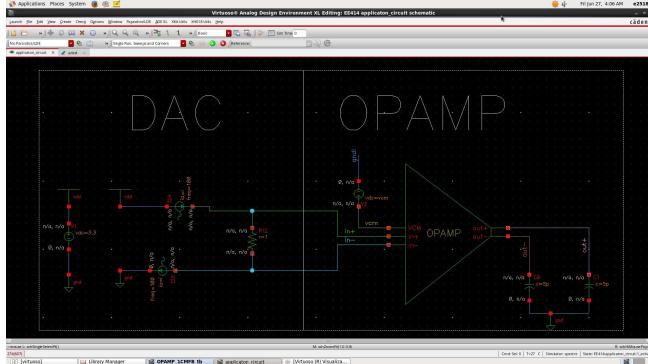


Fig. 5. Application circuit with DAC

### III. RESULTS AND SIMULATION

#### A. Simulation Results for the Reference Circuit

##### a) Current Consumption

The testbench of the reference circuit is shown at Figure 6. By making DC analysis, current consumption is measured as 149.6 nA.

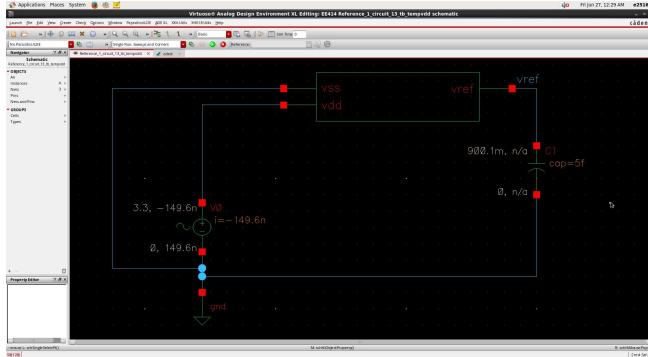


Fig. 6. Test bench of reference circuit and current consumption

##### b) Variation with Temperature ( $VDD=3.3$ V)

To measure the variation with temperature of the reference circuit, temperature is swept from  $-40^\circ C$  to  $+85^\circ C$  and, variation of the output reference voltage is calculated as 1.12% of the nominal value according to Figure 7. As explained at the design procedure of the reference circuit, after TCF=0 point is located at  $25^\circ C$ , while adjusting the reference voltage value to 900mV, TCF=0 point is shifted to  $5^\circ C$  from  $25^\circ C$ ; however, it is still satisfied the specification of  $<5\%$ .

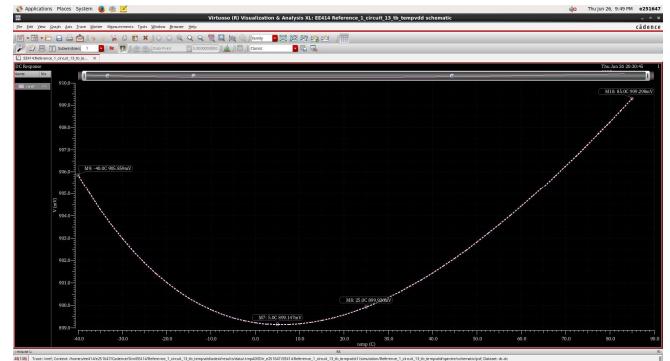


Fig. 7. Variation of reference voltage with temperature

##### c) Variation with Supply Voltage

To measure the variation of the reference voltage, supply voltage is swept from 1.2V to 3.3V. Variation of the reference voltage is calculated as 1.16 % with the full range of supply voltage according to Figure 8.

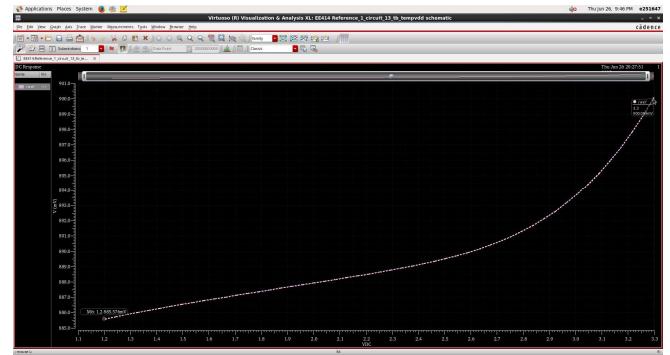


Fig. 8. Variation of reference voltage with supply voltage

##### d) PSRR (@50 kHz)

To measure PSRR, AC input voltage is given from supply voltage to the reference circuit. Gain at the output is measured as  $-91.26$ dB at 50kHz according to Figure 9. It results in  $+91.26$ dB of PSRR.

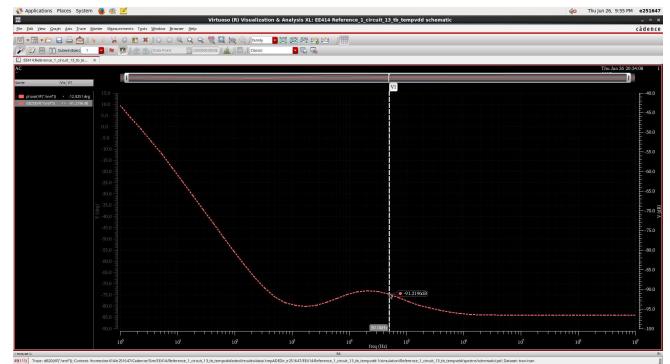


Fig. 9. Magnitude response of the reference circuit when input is given from  $V_{dd}$

#### B. Simulation Results for the Overall Amplifier

##### a) Power Dissipation (No Load)

For the power dissipation test of the overall differential amplifier including all biasing and reference circuits, the testbench in Figure 10 is used without any load. The total DC current consumption of the overall circuit is 279.4  $\mu$ A as also

shown in Figure 10. Moreover, the current consumption results for all PVT corners (wp, ws, wo, wz) is given in Figure 11, and Table 2. As expected, maximum current consumption is obtained in worst-case power (wp) corner whereas minimum current consumption is obtained in worst-case speed (ws) corner.

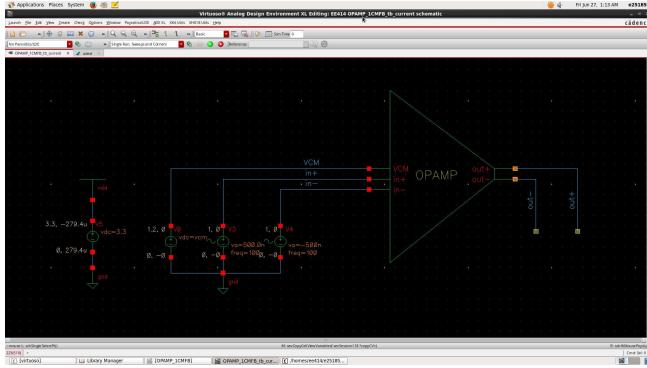


Fig. 10. Testbench for power consumption



Fig. 11. Current consumption across PVT corners

TABLE II. CURRENT CONSUMPTION ACROSS PVT CORNERS  
(VICM=1V, VCM=1.2V)

Nominal (nom)	Worst-case one (wo)	Worst-case power (wp)	Worst-case speed (ws)	Worst-case zero (wz)
279.4 $\mu$ A	358.2 $\mu$ A	424.4 $\mu$ A	180.3 $\mu$ A	249.1 $\mu$ A

### b) DC Gain

To do all the other tests, 5 pF load capacitance is used for both outputs of the op-amp. AC analysis is done for DC gain, and the bode plot showing the magnitude of the gain of the amplifier, together with the phase, when the input common mode voltage is 1V and the output common mode voltage is 1.2V, is shown in Figure 12. Moreover, parametric sweep for the output common mode voltage (from 0.6V to 1.5V) is done for the same AC analysis. It can be seen that the gain and phase of the amplifier remain similar for different output common mode voltages, showing that the adjustable common mode voltages do not change the gain and stability of the amplifier significantly.



Fig. 12. Magnitude (dB) and phase plot of the amplifier (VICM=1V, VCM=1.2V)

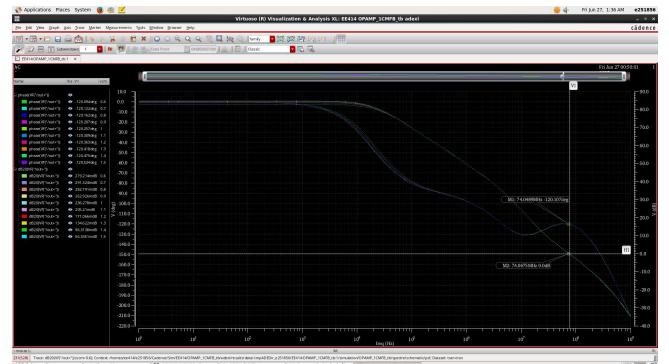


Fig. 13. Magnitude (dB) and phase plot of the amplifier for different output common mode voltages (VICM=1V, Vcm=[0.6V, 1.5V])

Moreover, the AC analysis results for all PVT corners (wp, ws, wo, wz) is given in Figure 14, 15, 16, and 17, respectively. Input and output common mode voltages are again set to 1V, and 1.2V, respectively. The DC gain values for the PVT corners together with the nominal case are also given in Table 3. From these results, it can be observed that except “worst-case one (wo)” corner, the gain values are very similar, which are all above 80 dB. In the worst-case one (wo) corner, where NMOS transistors are fast whereas PMOS transistors are slow, the amplifier does not operate properly and there is no gain observed. The reason for this may be that PMOS transistors are used as the input transistors in the first stage meaning that their relative speed with respect to NMOS transistors is quite important.

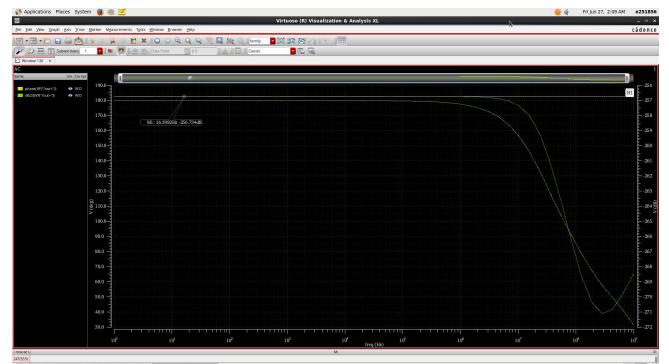


Fig. 14. Magnitude (dB) and phase plot of the amplifier for the worst-case one (wo) corner (VICM=1V, Vcm=1.2V)

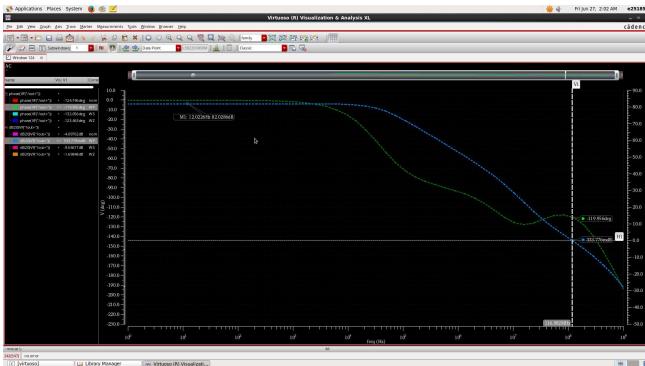


Fig. 15. Magnitude (dB) and phase plot of the amplifier for the worst-case power (wp) corner ( $V_{ICM}=1V$ ,  $V_{CM}=1.2V$ )

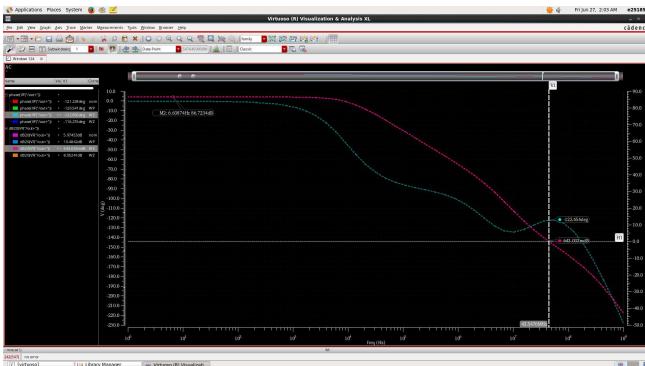


Fig. 16. Magnitude (dB) and phase plot of the amplifier for the worst-case speed (ws) corner ( $V_{ICM}=1V$ ,  $V_{CM}=1.2V$ )

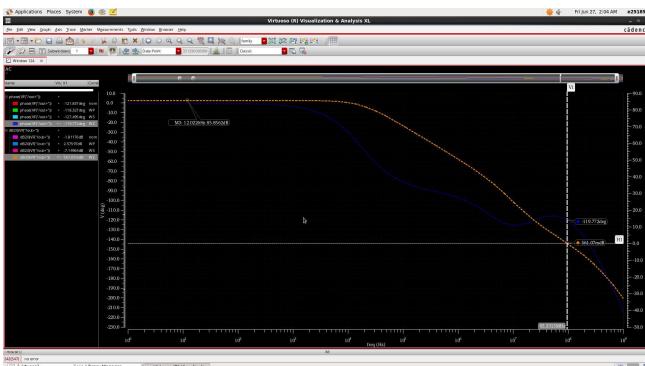


Fig. 17. Magnitude (dB) and phase plot of the amplifier for the worst-case zero (wz) corner ( $V_{ICM}=1V$ ,  $V_{CM}=1.2V$ )

TABLE III. DC GAIN ACROSS PVT CORNERS ( $V_{ICM}=1V$ ,  $V_{CM}=1.2V$ )

Nominal (nom)	Worst-case one (wo)	Worst-case power (wp)	Worst-case speed (ws)	Worst-case zero (wz)
84.9 dB	x	82 dB	86.7 dB	85.8 dB

### c) Unity-Gain Bandwidth

From the AC analysis plots shown in Figure 12, 13, 14, 15, 16, and 17, unity-gain bandwidth can also be extracted by obtaining the frequency where the gain is down to 0 dB. From Figure 13, it can be concluded that output common mode voltage does not have a significant effect on unity-gain bandwidth similar to DC gain. Moreover, the obtained unity-gain bandwidth values for all PVT corners together with the nominal case are given in Table 4. The UGB value for the worst-case one (wo) corner cannot be given since the circuit does not operate properly in that PVT corner. Unity-gain bandwidth is correlated with the speed of the op-amp

showing how well the amplifier can handle high frequency signals. Therefore, the lowest UGB is obtained in the worst-case speed (wp) corner. On the other hand, worst-case power (wp) corner results in the highest UGB since when the power is increased, the speed also generally (not always) increases.

TABLE IV. UNITY-GAIN BANDWIDTH ACROSS PVT CORNERS ( $V_{ICM}=1V$ ,  $V_{CM}=1.2V$ )

Nominal (nom)	Worst-case one (wo)	Worst-case power (wp)	Worst-case speed (ws)	Worst-case zero (wz)
76.4 MHz	x	116.9 MHz	43.5 MHz	93.3 MHz

### d) Phase Margin

From the AC analysis plots shown in Figure 12, 13, 14, 15, 16, and 17, phase margin can also be extracted by measuring the phase where the gain is down to 0 dB and subtracting it from  $-180^\circ$  assuming unity gain feedback. From Figure 13, it can be concluded that output common mode voltage does not affect the phase margin significantly, and it is always close to  $60^\circ$ . Moreover, the obtained phase margin values for all PVT corners together with the nominal case are given in Table 5. In worst-case one (wo) corner, the circuit is unstable since it does not operate functionally. The lowest phase margin is obtained in the worst-case speed (ws) corner; however, the values are very close to each other meaning that stability is ensured for all the cases except worst-case one (wo) corner.

TABLE V. PHASE MARGIN ACROSS PVT CORNERS ( $V_{ICM}=1V$ ,  $V_{CM}=1.2V$ )

Nominal (nom)	Worst-case one (wo)	Worst-case power (wp)	Worst-case speed (ws)	Worst-case zero (wz)
$59.7^\circ$	x	$60^\circ$	$57.4^\circ$	$60.3^\circ$

### e) Slew Rate

To obtain the slew rate of the op-amp, a step input should be given to one of inputs while the other one is connected to ground or  $V_{DD}$ . In the designed op-amp, the inputs are connected to PMOS transistors meaning that when an input is high, the corresponding PMOS is off. On the other hand, when the input is low, the corresponding NMOS becomes on and starts to conduct. In the test for the slew rate, since PMOS transistors are used as inputs,  $V_{DD}$  is connected to both inputs. In this case, both transistors are off. After some time, one of the inputs are set to 0 as a step input whereas the other input remains as  $V_{DD}$ . Then, the load capacitor starts to discharge almost linearly with a fixed current. This discharging is simulated for all PVT corners as shown in Figure 18. The slew rate is defined as the rate of change of the output voltage as given in Equation 9. Therefore, the negative slopes of the curves in Figure 18 give slew rates for different PVT corners as given in Table 6. Similar to the other parameters, the worst slew rate is obtained in worst-case zero (wo) corner due to the functionality of the circuit. Slew rate is a parameter that measures the speed of an op-amp. Therefore, the results are similar to the unity-gain bandwidth results given in Table 4. The highest slew rate values are achieved in worst-case power (wp) and worst-case zero (wz) corners. It is because more power means more current, and more current means higher slew rates according to Equation 9. Moreover, the biasing transistors in the second stage of the main amplifier

are PMOS. Therefore, when PMOS transistors are fast (worst-case zero corner), currents are larger that charge the output resulting in a high slew rate.



Fig. 18. Plot for the slew rates in all PVT corners (Vicm=1V, Vcm=1.2V)

$$\text{Slew Rate} = \frac{\Delta V_{out}}{\Delta t} = \frac{I_{BIAS}}{C_C} \quad (9)$$

TABLE VI. SLEW RATE ACROSS PVT CORNERS (VICM=1V, VCM=1.2V)

Nominal (nom)	Worst-case one (wo)	Worst-case power (wp)	Worst-case speed (ws)	Worst-case zero (wz)
40.29 V/μs	16.4 V/μs	52.7 V/μs	28.36 V/μs	52.7 V/μs

#### f) PSRR

For calculating PSRR, gain from supply to output is measured as -17.1dB (Nominal value) which is 0.139 V/V in linear scale as shown in Figure 19. Differential gain is 17.579k (84.9 dB). Nominal value of PSRR is calculated from Equation 10 as 102.22 dB.

$$PSRR = \frac{\text{Differential Gain}}{\text{Supply Gain}} \quad (10)$$

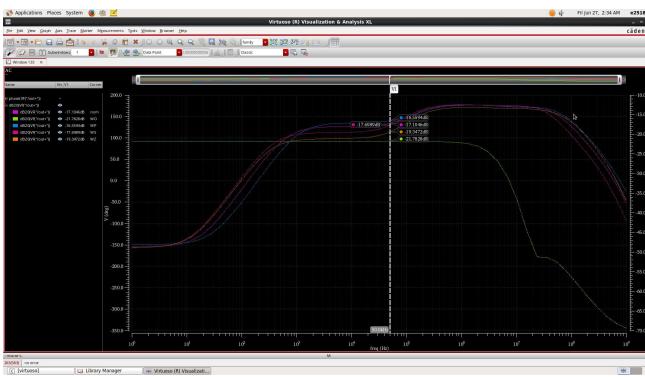


Fig. 19. Gain from supply of the op-amp for different corners.

At Table 7 below, PSRR under different corners are reported.

TABLE VII. PSRR OF DIFFERENT CORNERS (VICM=1V, VCM=1.2V)

	Nominal (nom)	Worst-case one (wo)	Worst-case power (wp)	Worst-case speed (ws)	Worst-case zero (wz)
DC Gain	84.9 dB	x	82 dB	86.7 dB	85.8 dB
Supply gain	-17.14dB	-21.78dB	-16.56 dB	-17.7dB	-19.35dB
PSRR	102.04 dB	x	98.56 dB	104.4 dB	105.15dB

Highest PSRR is obtained at the WZ corner. This may be expected since, input stage of the op-amp is composed of PMOS transistors. Therefore, it rejects supply gain maximum in this case. Since in WO corner amplifier does not work DC gain and PSRR are left blank.

#### g) CMRR

For calculating CMRR, common mode gain is measured as -81.81dB shown in Figure 20. Differential gain is 84.9 dB. Nominal value of CMRR is calculated from Equation 11 as 166.71 dB.

$$CMRR = \frac{\text{Differential Gain}}{\text{Common mode Gain}} \quad (11)$$

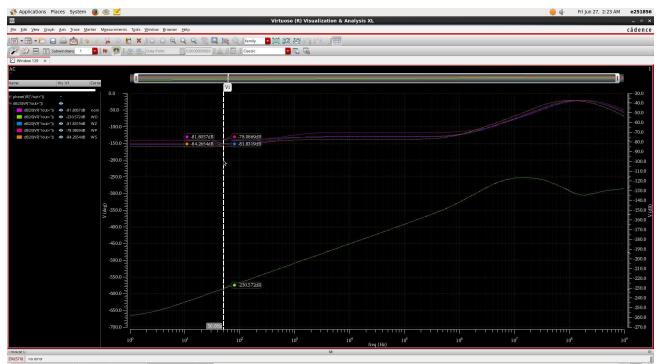


Fig. 20. Common mode gain of the op-amp for different corners

At Table 8 below, CMRR under different corners are reported.

TABLE VIII. CMRR OF DIFFERENT CORNERS (VICM=1V, VCM=1.2V)

	Nominal (nom)	Worst-case one (wo)	Worst-case power (wp)	Worst-case speed (ws)	Worst-case zero (wz)
DC Gain	84.9 dB	x	82 dB	86.7 dB	85.8 dB
Common Mode gain	-81.81dB	-230.572 dB	-78.1 dB	-84.26 dB	-81.83dB
CMRR	166.71 dB	x	160.1 dB	170.96 dB	167.63dB

CMRR are similar in all corners except WO. Since in WO corner amplifier does not work DC gain and CMRR are left blank.

#### h) Input Common-Mode Range

Transient analysis is performed by sweeping input common mode voltage to obtain the input common mode range, which is measured as -0.3V to 2.2V as shown in Figure

21. As explained in the design procedure section to satisfy the slightly negative input common mode range, main transistors of the first stage are chosen PMOS transistors.

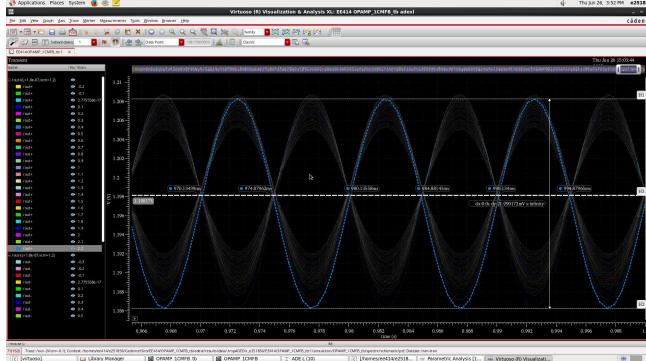


Fig. 21. Output transient analysis with input common mode sweep

To reach input common mode range up to +3V, folded cascode is needed to be converted into complementary (both NMOS and PMOS main transistors) folded cascode. An example circuit topology is shown Figure 22 [2].

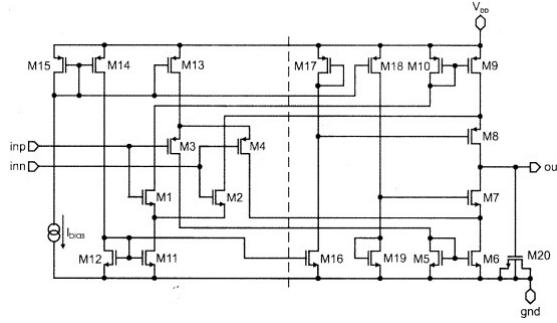


Fig. 22. Complementary Folded-Cascode Amplifier

For the small input common mode range, PMOS main transistor is on, for the large common mode range of the NMOS main transistor is on. Therefore, input common mode range is larger than a rail-to-rail swing.

The disadvantage of complementary folded-cascode topology is that, gain of the circuit varies significantly according to input common mode. For some input range, both NMOS and PMOS are on, and for some input range either NMOS or PMOS is on. This leads to variation of gain. Therefore, gm equalizer circuit is necessary for this topology for stable gain and operation [3]. All these requirements are factors that increase the current consumption, which is not preferred for this design.

### i) Output Common-Mode Range ( $V_{cm}$ )

To test common mode feedback circuit and output common mode range transient analysis is performed while sweeping  $V_{cm}$  reference voltage. According to Figure 23, output common mode range is measured as 0.6V to 1.5V meaning that common mode feedback can adjust the output common mode level precisely with this range.

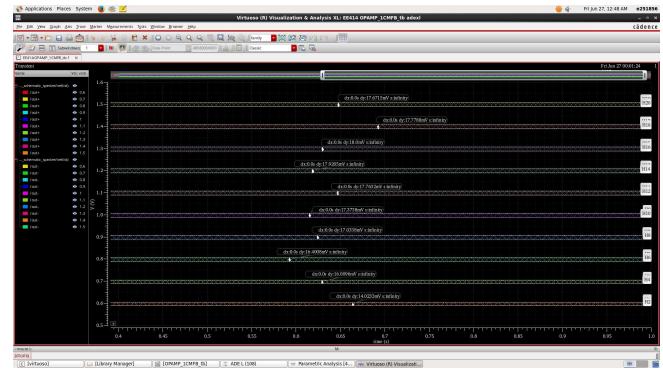


Fig. 23. Output transient analysis of the op-amp while sweeping  $V_{cm}$  voltage when differential input is 1  $\mu$ V peak to peak ( $V_{icm}=1V$ )

According to the results, the gain of the op-amp at different common mode voltages is reported Table 9 below.

TABLE IX. GAIN AT DIFFERENT  $V_{cm}$  VALUES ( $V_{icm}=1V$ )

$V_{cm}$	0.6V	0.8V	1V	1.2V	1.5V
Gain	14.02k (V/V)	16.4k (V/V)	17.37k (V/V)	17.92k (V/V)	17.67k (V/V)

A similar test is performed for  $V_{cm}=1.2V$  for different process corners. According to Figure 24, the common mode feedback circuit can adjust output to 1.2V except for the WO corner.

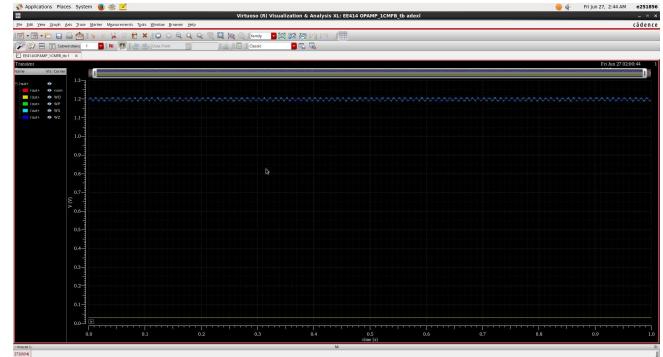


Fig. 24. Output transient analysis of the op-amp for different corners when  $V_{cm} = 1.2V$  when differential input is 1  $\mu$ V peak to peak ( $V_{icm} = 1V$ )

In order to increase the output common mode range to 0.6V-2.4V, two different common mode feedback circuits can be used for each stage of the amplifier. To implement this idea, alternative differential-amplifier topology is built which is shown at Figure 25. Second common mode feedback (right at Figure 25) circuit adjusts the output common mode of the first stage, and the left common mode feedback circuit, which was same as explained before, stabilizes the output mode level of the second stage. With two feedback circuit output common mode range can be increased to 0.6V-2.4V as shown in Figure 26.

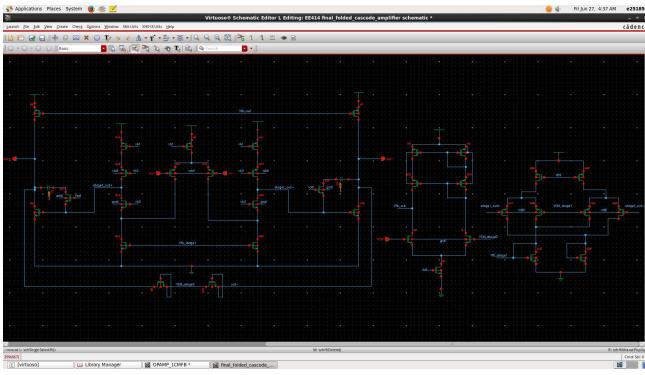


Fig. 25. Alternative op-amp with two common-mode feedback loops to achieve large output common voltage range



Fig. 26. Output transient analysis for different  $V_{CM}$  levels for the alternative differential amplifier circuit with two feedback loops when differential input is 1  $\mu$ V peak to peak ( $V_{ICM}=1V$ )

TABLE X. GAIN AT DIFFERENT  $V_{CM}$  VALUES FOR THE ALTERNATIVE CIRCUIT TOPOLOGY ( $V_{ICM}=1V$ )

$V_{CM}$	0.6V	1.2V	1.8V	2.4V
Gain	26.2k	34.82k	34k	19.03k

Output common mode range is adjustable from 0.6V to 2.4V in the alternative topology. The disadvantage of this topology is that, due to the second feedback loop, biasing current cannot be adjusted as desired; therefore it does not have a large bandwidth, and this topology is not preferred in this paper.

#### j) Output Current Drive (Source)

The output current drive is the maximum current that the op-amp can source or sink, showing the driving capability. To measure it, load capacitances are disconnected from the circuit, and a resistor is connected to each output of the op-amp. Then, DC sweep analysis is done by sweeping the resistance value from  $1\Omega$  to  $10M\Omega$ , and plotting the current flowing through one of the resistors. The plot for the output current drive (source) is shown in Figure 27. It can be seen that maximum amount of current that can be supplied by the op-amp from each of the outputs is  $29.2 \mu A$ .

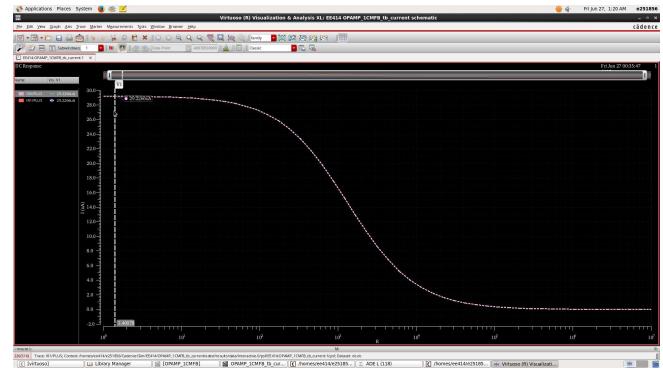


Fig. 27. DC sweep simulation for output current drive (source) of the op-amp

#### C. Simulation Results for the Application Circuit

To test the application circuit with DAC connected to the designed op-amp, shown in Figure 5, the current input pairs given in Table 11 are used. Then the corresponding differential output voltages, output common mode voltages, and overall gains (V/A) are obtained as also shown in Table 11. Transient analyses for the test cases 1 and 2 are shown in Figure 28 and 29, respectively. In those plots, the two outputs at the same output common mode voltage (set externally), and the differential output signal (difference of the two outputs) can be seen. Moreover, output common mode voltage is swept from 0.6V to 1.5V while applying the same current inputs, and the output waveforms (single-end) at those common mode voltages are shown in Figure 30. This proves that the designed op-amp can set and stabilize the output common mode voltage externally without causing any distortion, and it works quite well in a simple application using DAC.

TABLE XI. GAIN AT DIFFERENT  $V_{CM}$  VALUES FOR THE ALTERNATIVE CIRCUIT TOPOLOGY ( $V_{ICM}=1V$ )

Test Cases	Current Inputs (Magnitude)	Differential Output (Peak to Peak)	Output Common -Mode Voltage	Gain $(\frac{V_{out}^+ - V_{out}^-}{I_{in}^+ - I_{in}^-})$
1	$I_{in}^+ = +50 \mu A$ $I_{in}^- = -50 \mu A$	1.41 V ( $V_{out}^+ > V_{out}^-$ )	1.2 V	14100 V/A (83 dB)
2	$I_{in}^+ = -50 \mu A$ $I_{in}^- = +50 \mu A$	1.41 V ( $V_{out}^+ > V_{out}^-$ )	1.2 V	14100 V/A (83 dB)

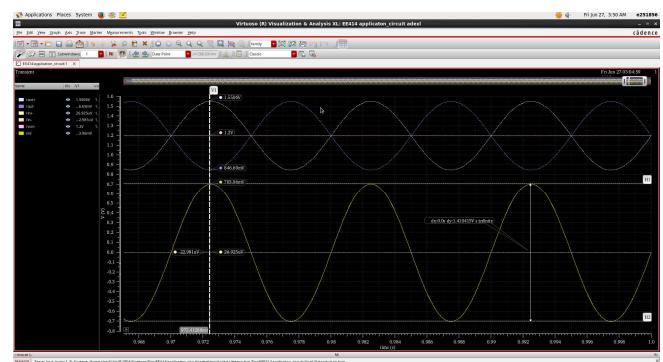


Fig. 28. Transient simulation of test case 1 for the application circuit ( $I_{in}^+ = +50 \mu A$ ,  $I_{in}^- = -50 \mu A$ )

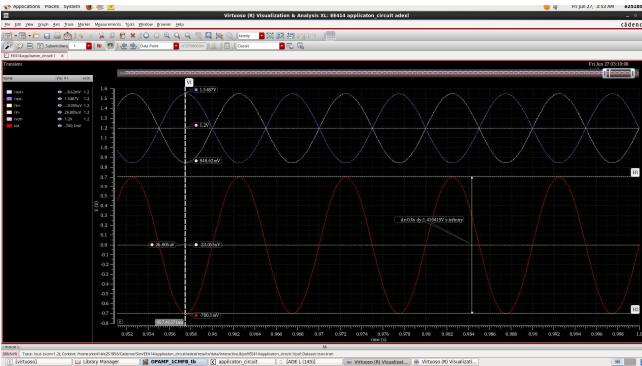


Fig. 29. Transient simulation of test case 2 for the application circuit ( $I_{in^+} = -50\mu A$ ,  $I_{in^-} = +50 \mu A$ )

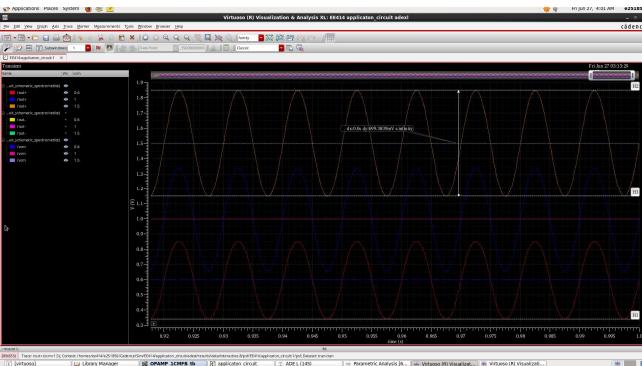


Fig. 30. Transient simulation for the application circuit where output common mode voltage is swept from  $0.6V$  to  $1.5V$  ( $V_{cm}=1V$ )

The overall performance results for each design specification of the reference circuit and the fully differential op-amp are given in Table 12.

TABLE XII. RESULTS FOR REFERENCE CIRCUIT AND OP-AMP

Parameter	Result
<b>Reference Circuit</b>	
Variation with Temperature ( $VDD=3.3 V$ ) (-40°C to +85°C)	1.12%.
Variation with Supply Voltage (1.2 V – 3.3 V)	1.16 %.
PSRR (@50 kHz)	91.26 dB
Current consumption	149.6 nA
<b>OP-AMP</b>	
Supply Voltage	3.3 V
Current consumption (No Load)	279.4 $\mu A$
DC Gain	84.9 dB
Unity-Gain Bandwidth	76.4 MHz
Phase Margin	59.7°
Slew Rate	40.29 V/ $\mu s$
PSRR	102.04 dB
CMRR	166.71 dB
Load Capacitance	5pF
Input Common-Mode Range	-0.3V to 2.2V
Output Common-Mode Range (Vcm)	0.6V to 1.5V
Output Current Drive (Source)	29.2 $\mu A$ .

#### IV. CONCLUSION

In this paper high gain, low power fully differential op-amp has been presented. The designed circuit has satisfied most of the targeted specifications. For the specifications that were not satisfied, alternative circuit topologies have been proposed. After analyzing the PVT corners, it is concluded that designed circuit can operate under extreme corners except for the “WO” corner.

The designing procedure offered us valuable experiences for Analog IC design. Future research will include improving circuit performance under extreme conditions with the state-of-the-art techniques.

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