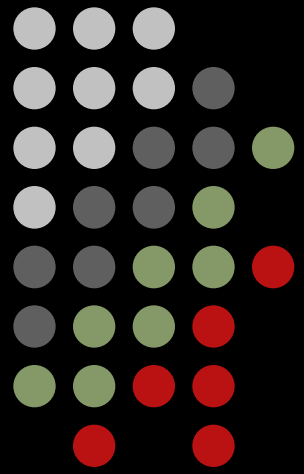
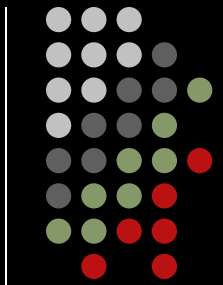
Welcome



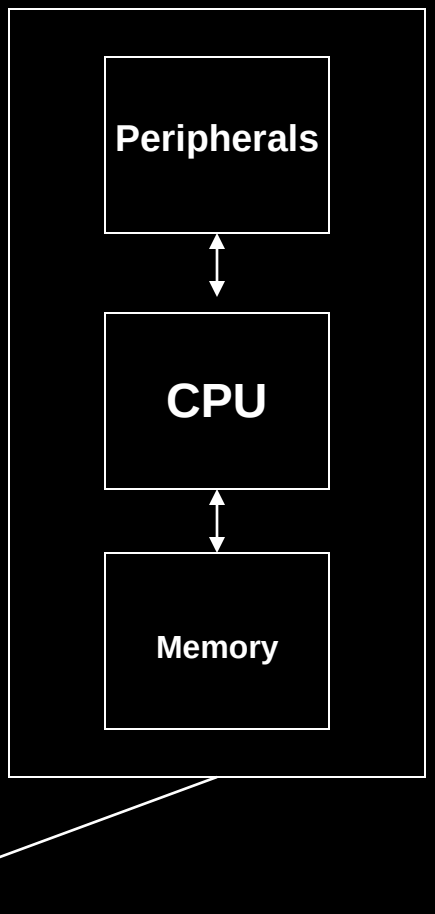
ARM Technology



- Versatile and popular CPU Technology
- Favorite for PM's
- 50% of 32bit Digital world ruled by ARM
- Every Embedded company has ARM Project
- Most Efficient in 32bit platform
- Competitors
  - PowerPC , Free Scale , MPC etc..

Introduction

- ARM9 is 32 bit General Purpose CPU architecture.
- Designed and Developed by ARM Technologies Ltd.
  (Advanced RISC Machine)
- ARM9 is used as the core CPU for Designing 32 bit Embedded Micro controllers.



Features of ARM9

- High Performance
- Low Power
- Low Cost

Features of ARM9

- High Performance------- 1 MIPS per Mhz
- Low Power ---------- 0.05mw per Mhz
- Low Cost---------- $ 8

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Application of ARM :

Telecommunication- Cellphone , Cellphone Base station , Routers , Gateways , etc….

Portable Devices- Handheld computers, Cellphones,PDA devices, GPS devices , etc….

Consumer Electronics- DVD Players , MP3 Players , iPod , Gamming Devices etc….

ARM is a RISC Processor

RISC	CISC
Reduced Instruction Set Computer	Complex Instruction Set Computer
Fewer number of instructions	Larger number of instructions
Ex: ARM , PIC , PowerPC , Free Scale , TI DSP's , MIPS … etc	Ex: 8085 , 8086 , 80386 , 80486 , Pentium , Dual-core … etc
Instructions finished in single cycle.	Instructions finished in multiple cycles.
Low hardware Complexity	High hardware Complexity
Hardware based Decoder and Control Unit.	Micro programmed Decoder And Control Unit.
Large Code Size	Small code Size
Low Cycles Per Second	High Cycles Per Second
Word sized Instruction	Instruction length varies

CPU Operations

Conventional CPU Execution cycle.

Fetch → Decode → Execute → Write Back

F1 D1 E1 W1 **F2 D2 E2 W2** **F3 D3 E3 W3**

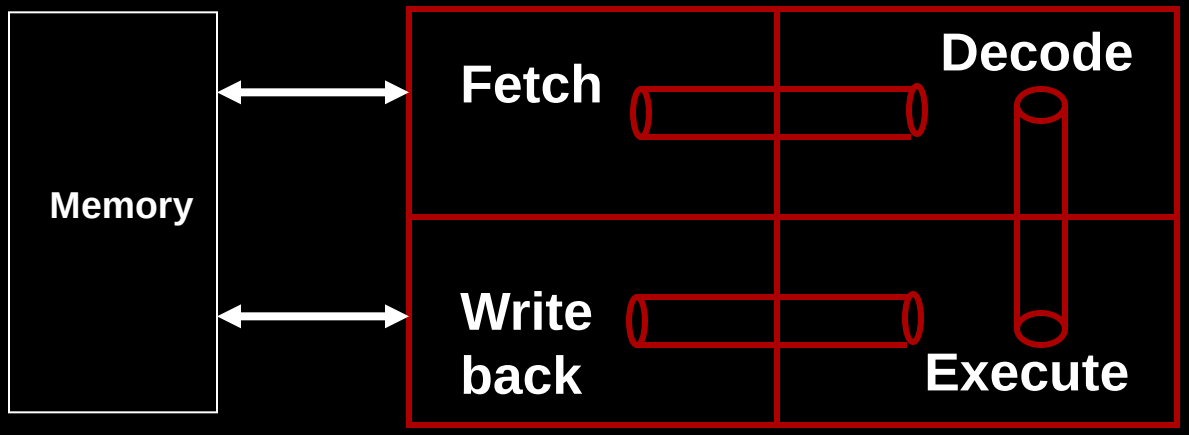
F6 D6 E6 W6 **F5 D5 E5 W5** **F4 D4 E4 W4**

F7 D7 E7 W7 **……**

Performance is ¼ or 25% of CPU time used for Execution.

ARM is a Pipelined Architecture

Pipelined CPU architecture.



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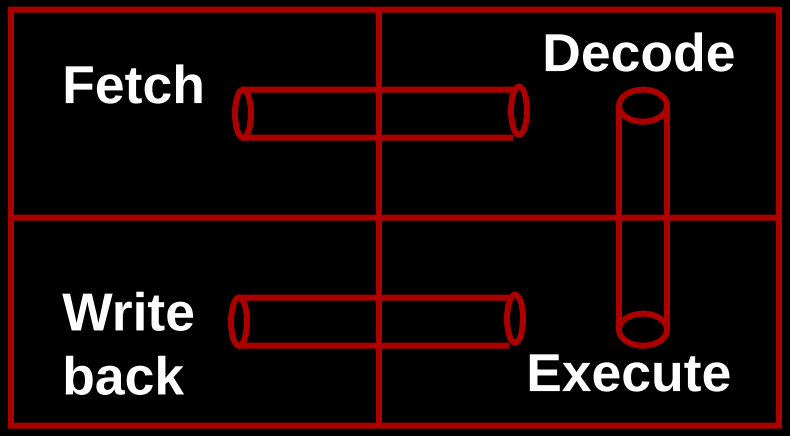


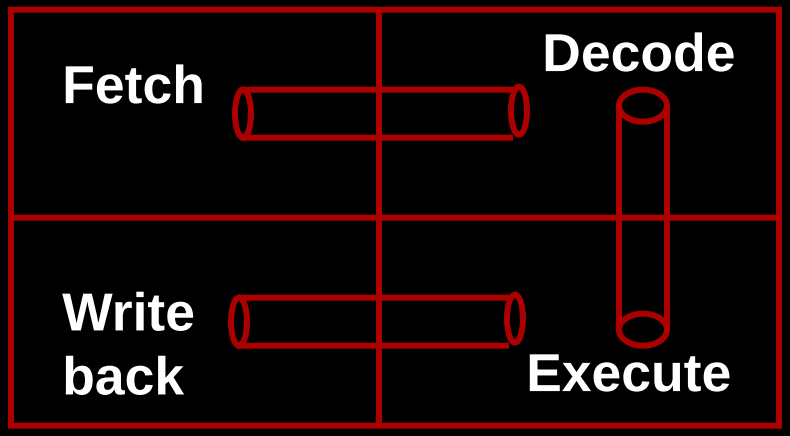
F1	D1	E1	W1					
	F2	D2	E2	W2				
		F3	D3	E3	W3			
			F4	D4	E4	W4		
				F5	D5	E5	W5	

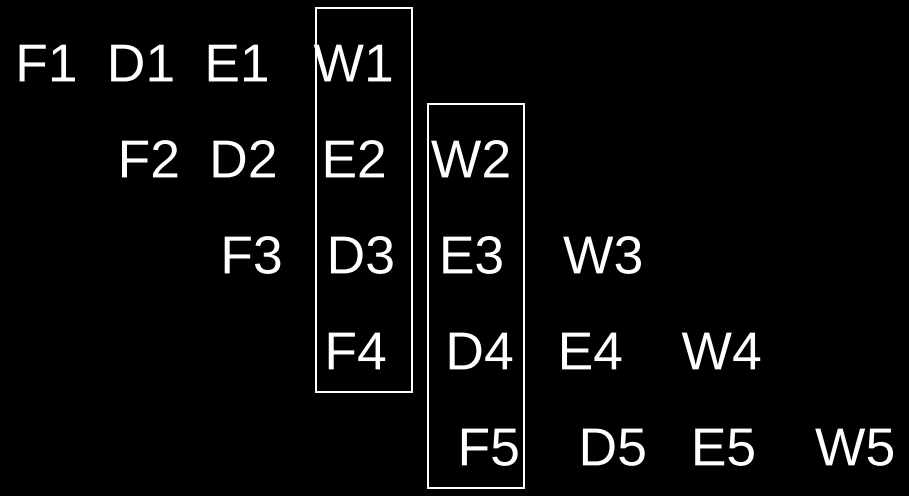
ARM is a Pipelined Architecture

Conventional CPU Execution cycle.

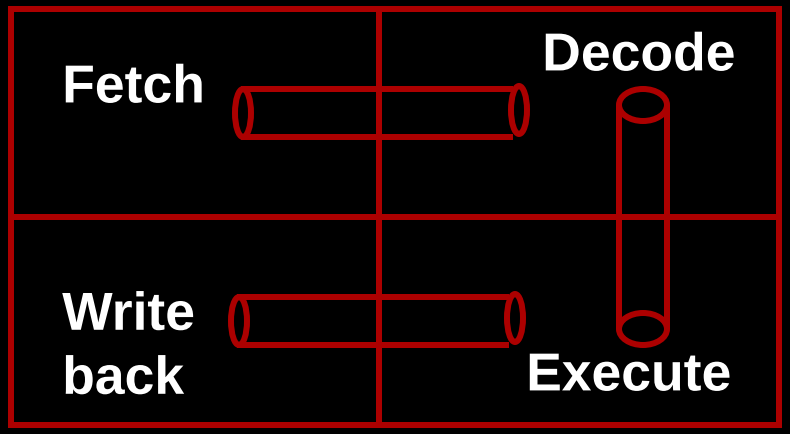
Fetch → Decode → Execute → Write Back

Pipelined CPU architecture.

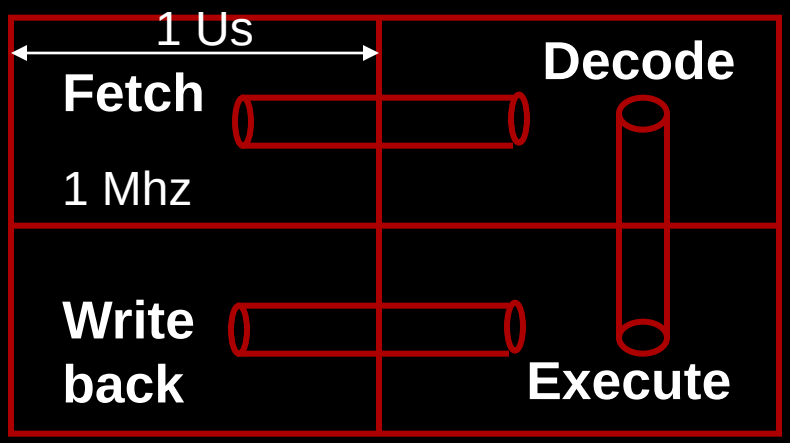




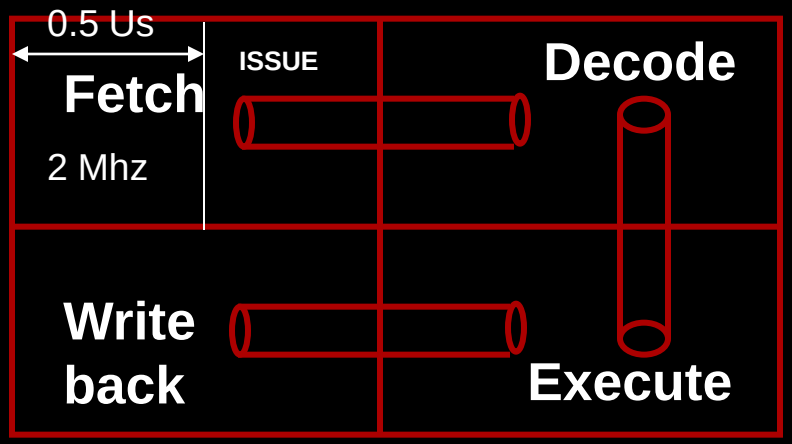
3 stage Pipelining



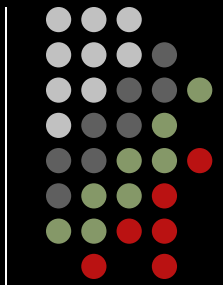
ARM is a Pipelined Architecture



ARM is a Pipelined Architecture



ARM is a Pipelined Architecture



- ARM7 uses 3 stage pipelining
- ARM9 uses 5 stage pipelining
- ARM10 uses 6 stage pipelining
- ARM11 uses 8 stage pipelining

Thumb Strategy

- **ARM9 Employs an unique architectural strategy called THUMB.**
- **THUMB is suitable for projects with high volume application with memory restriction.**
- **THUMB is suitable for applications where code density is an issue.**

What is THUMB

- THUMB is not one more parallel Architecture in the CPU
- THUMB is all about an another Instruction set in addition to the ARM Instruction
- So Essentially there need to be 2 decoders

1. ARM Decoder
2. THUMB Decoder

Thumb Concept

- **Super Reduced Instruction Set.**
- **ARM Instructions are of 32 bit whereas THUM instruction are of 16 bit.**
- **THUMB code provides twice the density of standard ARM code.**

MOV r0,r1 …… ARM…….. 32bit

MOV r0,r1 ……THUMB……. 16 bit

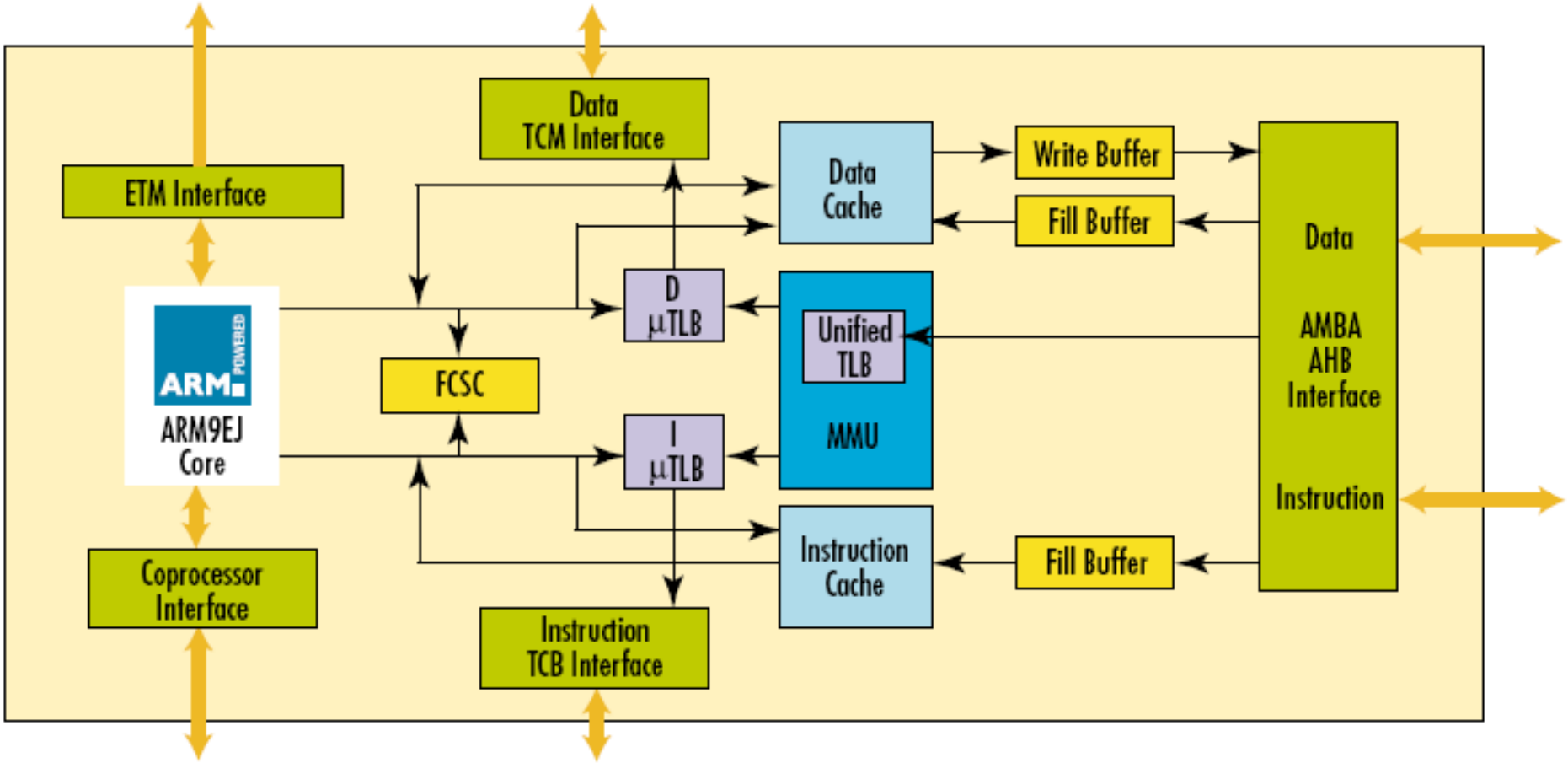
Advantages of Thumb

- **THUMB can manipulate 32 bit integer with single instruction.**
- **32 bit architecture with 16 bit instruction.**
- **Fast interrupt functions or DSP Functions could be coded ARM instruction Set and can be linked with THUMB functions.**

THUMB-2

New Thumb-2 extensions for the ARM architecture blend 16- and 32-bit instructions to enable higher performance, greater energy efficiency and lower memory costs.

Functional Block Diagram



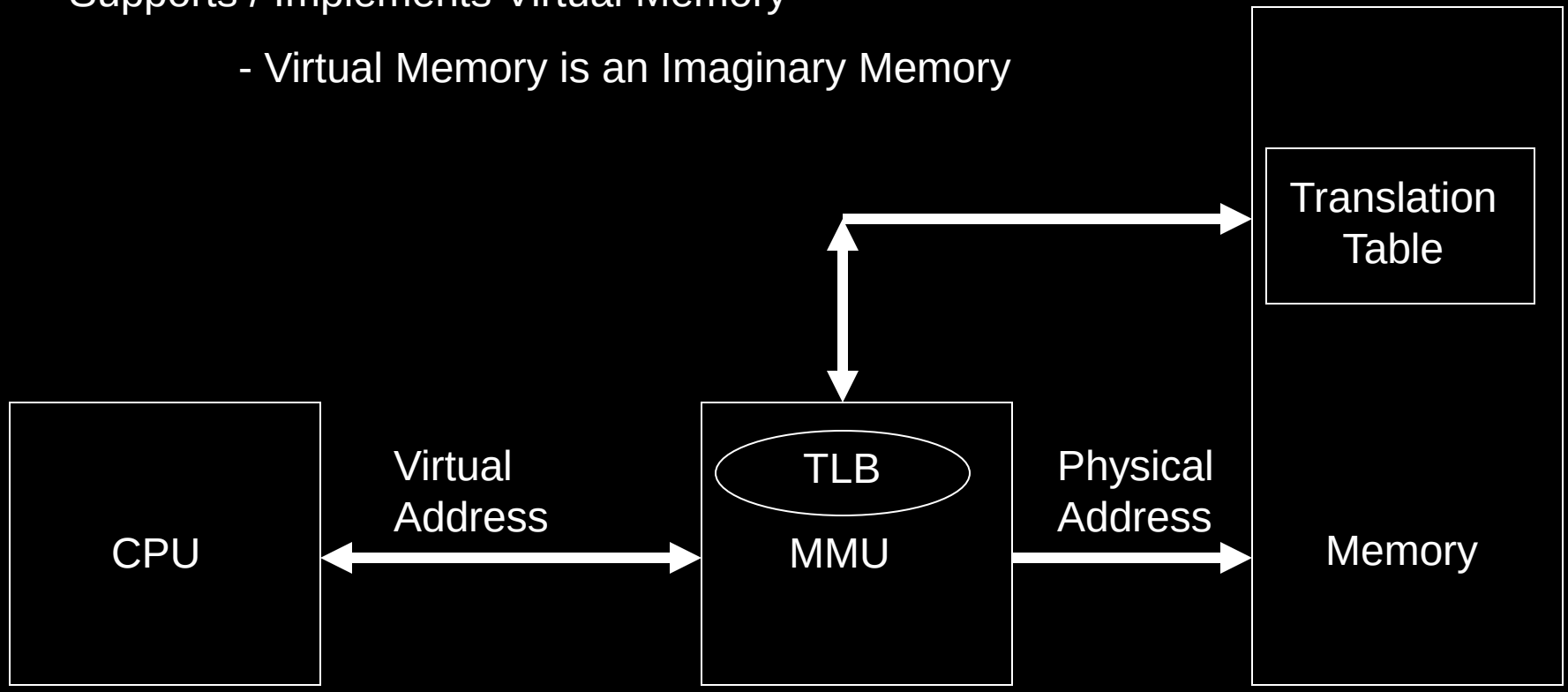
ARM926EJ-S architecture

MMU

Protects Memory from Unauthorized access

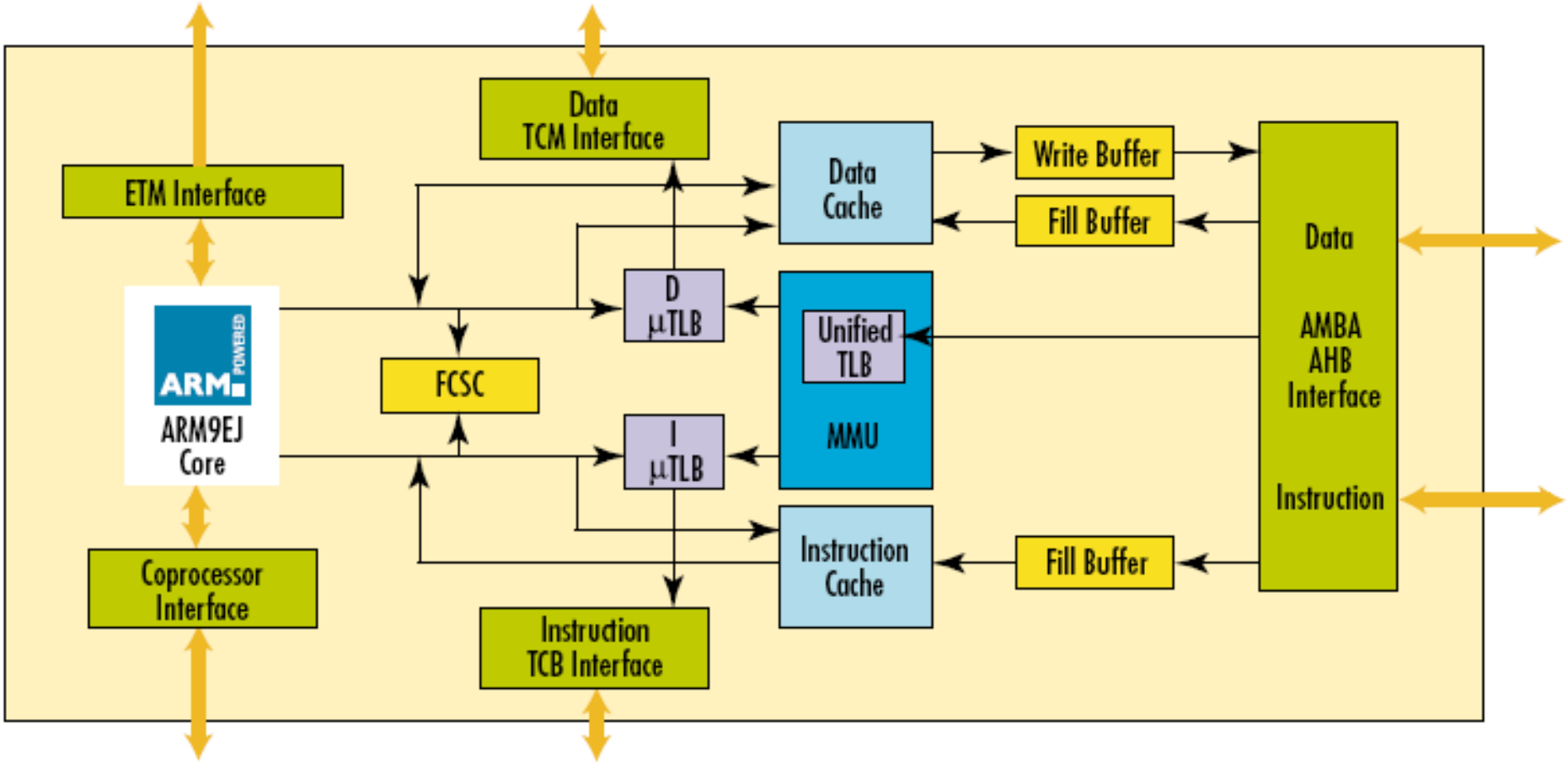
Supports / Implements Virtual Memory

- Virtual Memory is an Imaginary Memory



Translation Look aside Buffer is a cache for MMU to hold recently accessed Translation information from Translation Table

Functional Block Diagram



ARM926EJ-S architecture

AMBA BUS

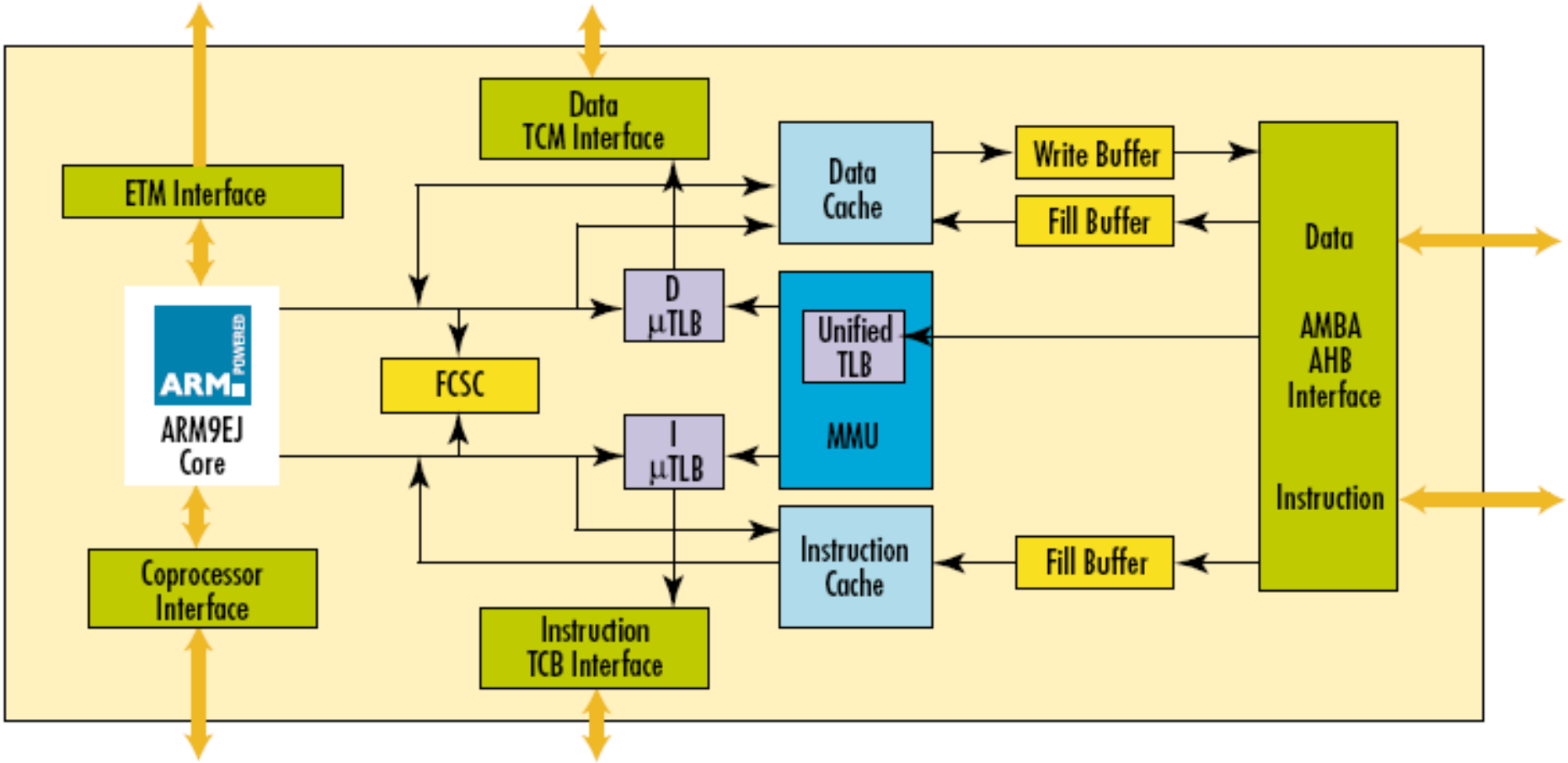
AMBA – Advanced Microcontroller BUS Architecture

AMBA is internal BUS in ARM used to connect on chip Memory & Peripheral systems

AMBA is available in 3 Flavors

1. ASB – Advanced System BUS
2. AHB - Advanced High-Performance BUS
3. APB - Advanced Peripheral BUS
4. ATB – Advanced TRACE Bus
5. AXI – AMBA Extensible Interface

Functional Block Diagram



ARM926EJ-S architecture

ARM Co-Processors

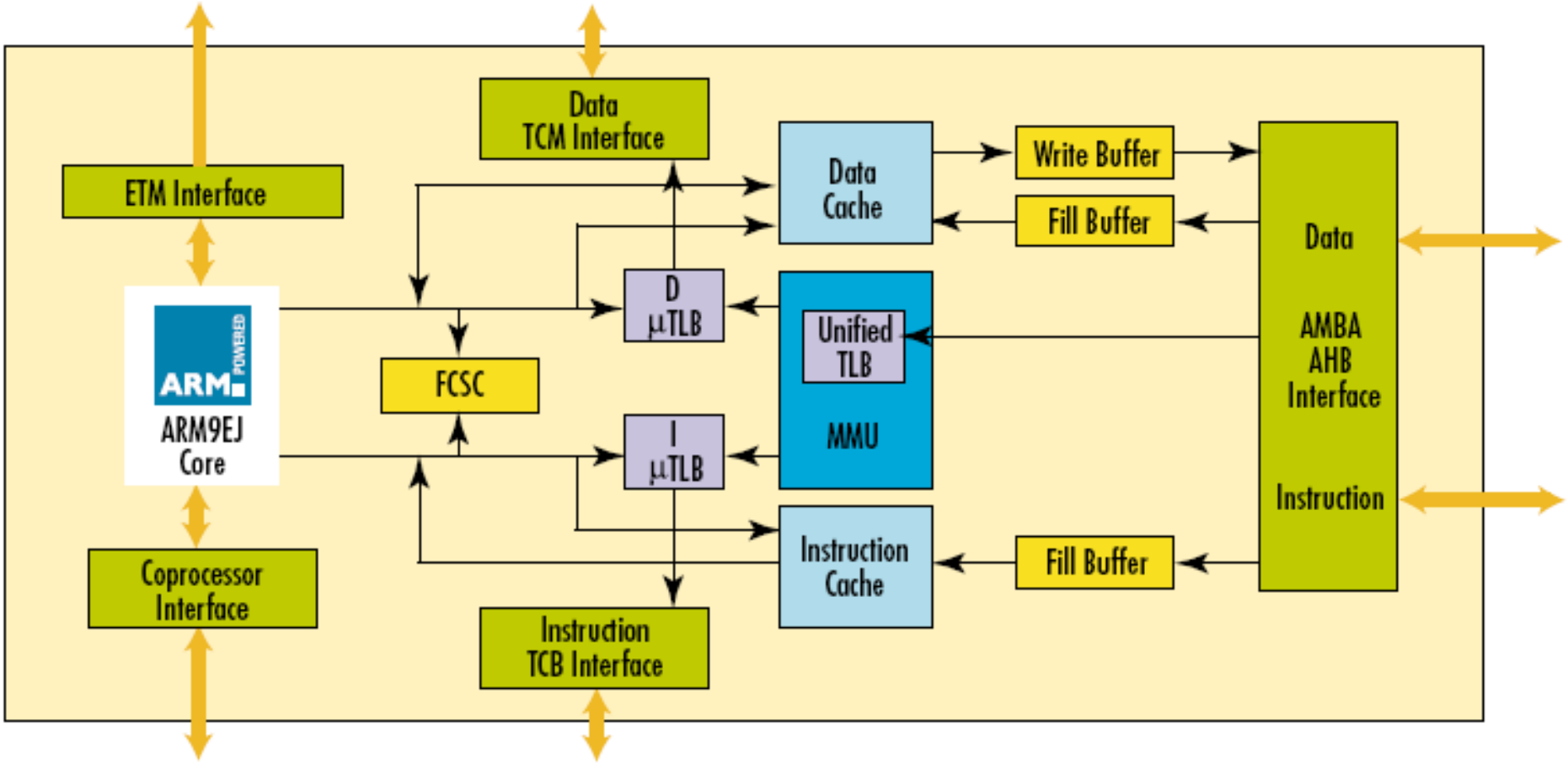
ARM supports 16 co-processors

They are referred as CP0 to CP15

MMU is one of the coprocessor on the core

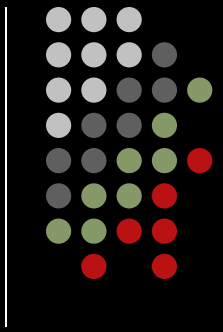
MMU is CP15

Functional Block Diagram



ARM926EJ-S architecture

ETM Interface

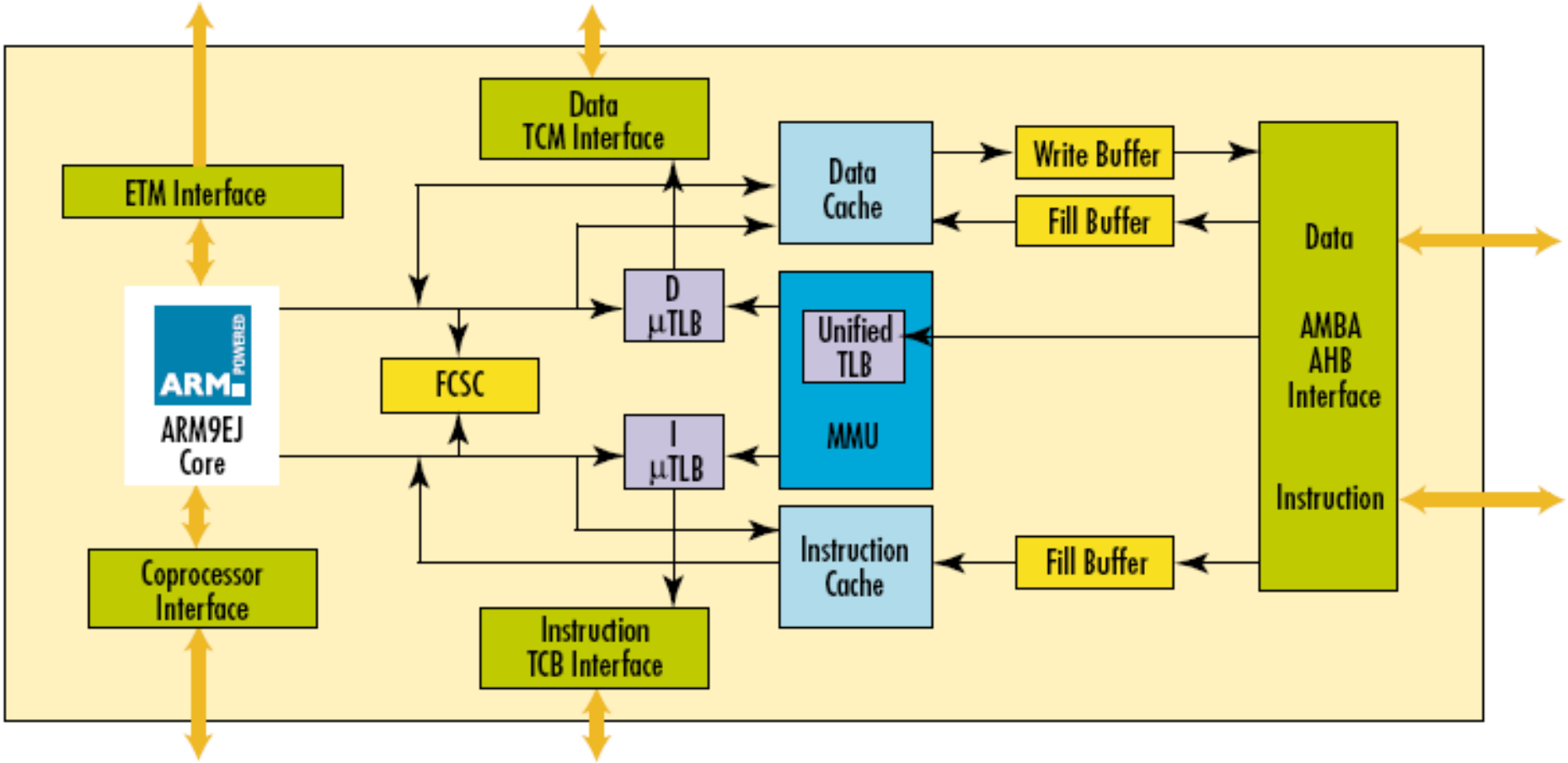


Embedded Trace Macro cell

Is used as interface between HOST & TARGET

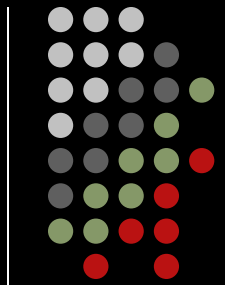
ETM is used for Debugging the Target

Functional Block Diagram



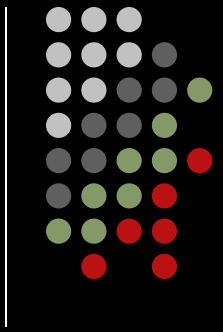
ARM926EJ-S architecture

Programming Model



- **Processor Operating States**
- **Processor Switching States**
- **Instruction Length**
- **Memory Formats**
- **Registers**
- **Operating Modes**
- **Exception Types**

Processing Operating States



- **ARM State - which executes 32 bit word aligned ARM instructions.**
- **THUMB State - which executes 16 bit THUMB instruction.**
- **Java State - which executes 8 bit Java byte code**

Switching States

BX	Branch & Exchange
BX R0	R0 shall have the branch address

Switching States

- **Switching from ARM to THUMB state**

  Execute BX instruction with state bit set(bit 0 of operand register.)

  Ex: BX R0 where bit 0 of R0 register is 1

- **Switching from THUMB to ARM state**

  Execute BX instruction with state bit cleared (bit 0 of operand register)

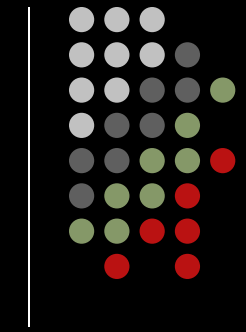
  Ex: BX R0 where bit 0 of R0 register is 0.

Switching States (contd..)

Switching from ARM state to JAVA State

BXJ R0

Memory Formats



Data

B4	B3	B2	B1

B1	a
B2	a+1
B3	a+2
B4	a+3
	.
	.
	.
	.
	.

LITTLE ENDIAN

Lower address

Upper Address

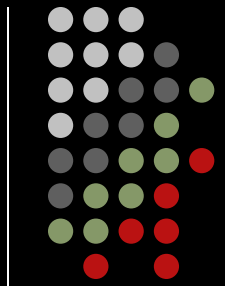
a	B4
a+1	B3
a+2	B2
a+3	B1
.	
.	
.	
.	
.	

BIG ENDIAN

Instruction Length

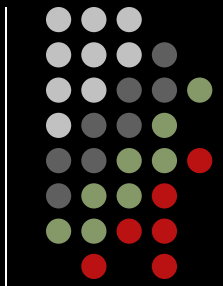
- ARM state - 32 bit
- THUMB state - 16 bit
- JAVA - 8 bit (Native)

Data Types



- 8 bit (Byte data)
- 16 bit (half word data)
- 32 bit(Word data)

Operating modes



ARM9 supports 7 operating modes.

User (usr): The normal ARM program execution state

IRQ (irq): Used for general-purpose interrupt handling

FIQ (fiq): Designed to support a data transfer or channel process

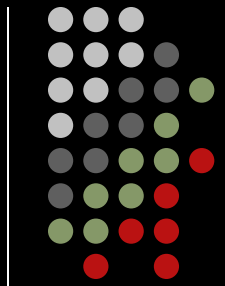
Supervisor (svc): Protected mode for the operating system

Abort mode (abt): Entered after a data or instruction pre etch abort

System (sys): A privileged user mode for the operating system

Undefined (und): Entered when an undefined instruction is executed

Registers

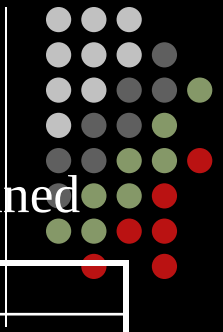


- ARM9 has total 37 registers each is of 32 bit in length.

Of them

- 30 registers are general purpose
- A Program Counter
- 6 registers are status

ARM state General Purpose / status registers

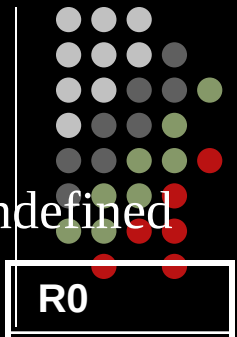


System & user	FIQ	Supervisor mode	Abort	IRQ	Undefined
R0	R0	R0	R0	R0	R0
R1	R1	R1	R1	R1	R1
R2	R2	R2	R2	R2	R2
R3	R3	R3	R3	R3	R3
R4	R4	R4	R4	R4	R4
R5	R5	R5	R5	R5	R5
R6	R6	R6	R6	R6	R6
R7	R7	R7	R7	R7	R7
R8	R8_fiq	R8	R8	R8	R8
R9	R9_fiq	R9	R9	R9	R9
R10	R10_fiq	R10	R10	R10	R10
R11	R11_fiq	R11	R11	R11	R11
R12	R12_fiq	R12	R12	R12	R12
R13	R13_fiq	R13_svc	R13_abt	R13_irq	R13_und
R14	R14_fiq	R14_svc	R14_abt	R14_irq	R14_und
R15(PC)	R15(PC)	R15(PC)	R15(PC)	R15(PC)	R15(PC)

ARM state program status registers

CPSR	CPSR	CPSR	CPSR	CPSR	CPSR
	SPSR_fiq	SPSR_svc	SPSR_abt	SPSR_irq	SPSR_und

THUMB state General Purpose /status Registers

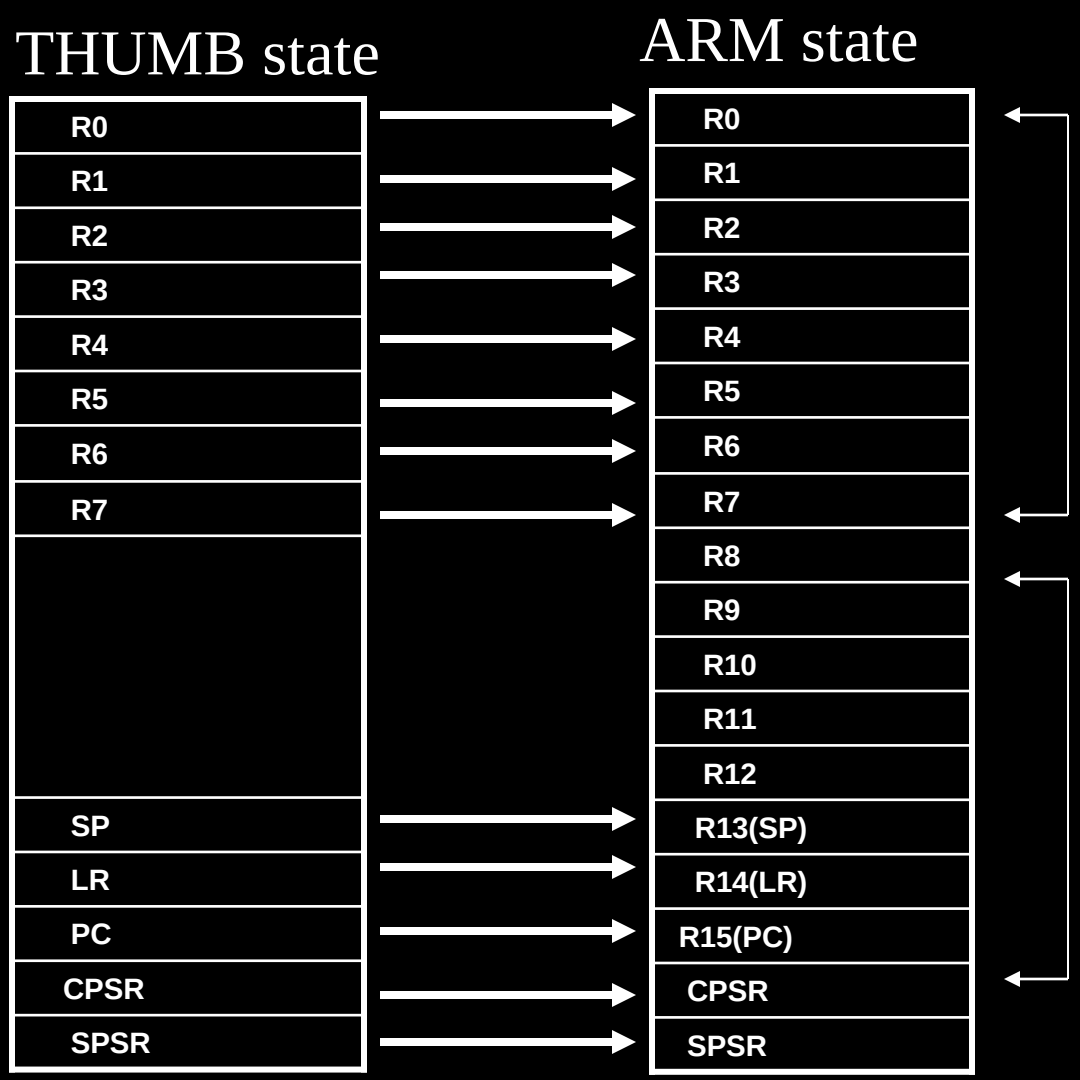


System & user	FIQ	Supervisor mode	Abort	IRQ	Undefined
R0	R0	R0	R0	R0	R0
R1	R1	R1	R1	R1	R1
R2	R2	R2	R2	R2	R2
R3	R3	R3	R3	R3	R3
R4	R4	R4	R4	R4	R4
R5	R5	R5	R5	R5	R5
R6	R6	R6	R6	R6	R6
R7	R7	R7	R7	R7	R7
SP	SP_fiq	SP_svc	SP_abt	SP_irq	SP_und
LR	LR_fiq	LR_svc	LR_abt	LR_irq	LR_und
PC	PC	PC	PC	PC	PC

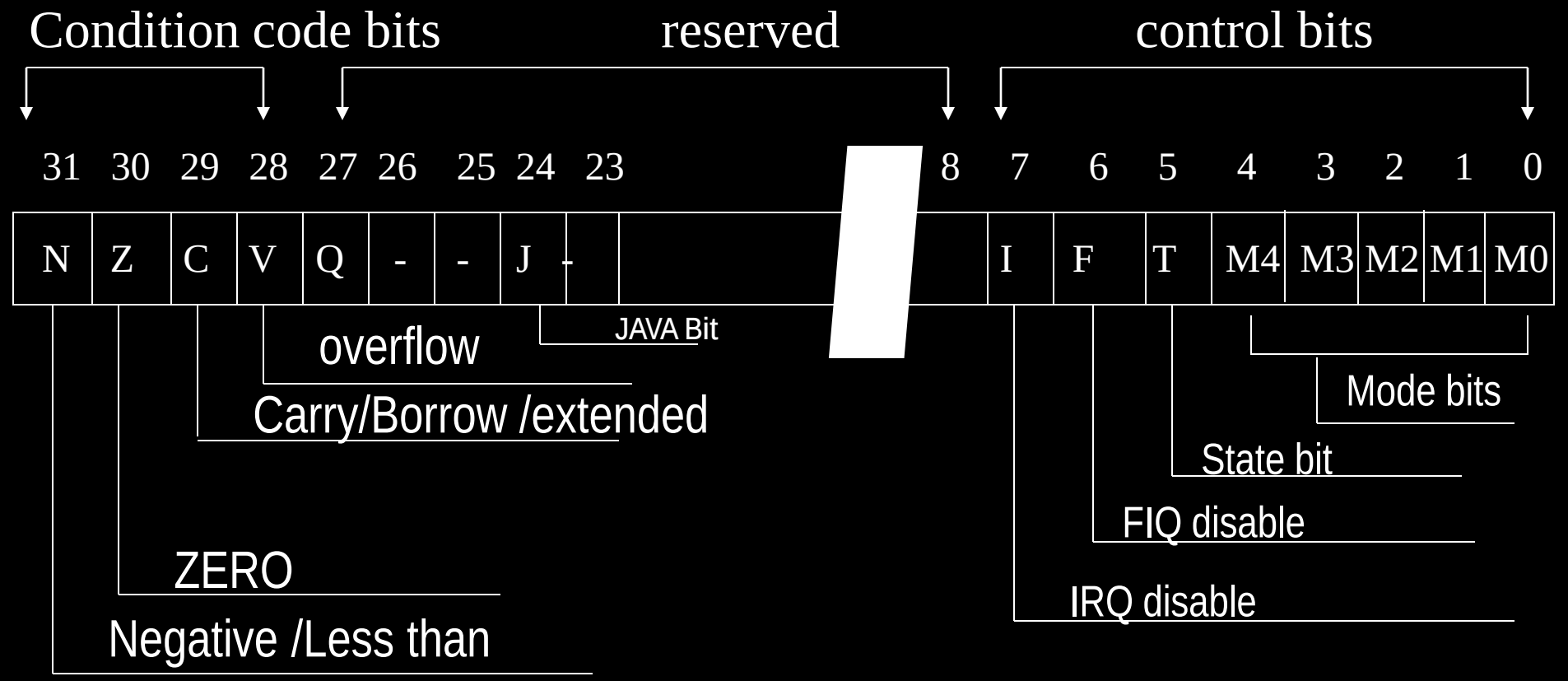
THUMB state program status registers

CPSR	CPSR	CPSR	CPSR	CPSR	CPSR
	SPSR_fiq	SPSR_svc	SPSR_abt	SPSR_abt	SPSR_abt

ARM & THUMB state register mapping



PSR Detail

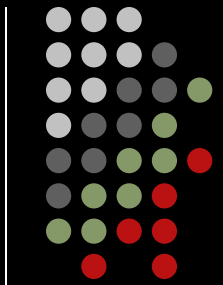

Condition code bits
reserved
control bits
31 30 29 28 27 26 25 24 23 8 7 6 5 4 3 2 1 0
N Z C V Q - - J - I F T M4 M3 M2 M1 M0
JAVA Bit
overflow
Carry/Borrow /extended
Mode bits
State bit
FIQ disable
IRQ disable
ZERO
Negative /Less than

EXCEPTIONS

Exceptions is an event which causes temporary suspension of the program flow to service source of the exception

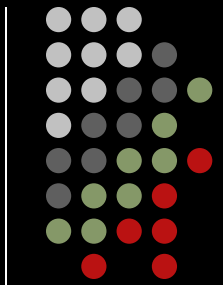
Vector Address	Exception	Priority	Mode on entry
0x00000000	Reset	1 Highest	Supervisor
0x00000004	Undefined instruction	6 Lowest	Undefined
0x00000008	Software interrupt	6 Lowest	Supervisor
0x0000000C	Abort(prefetch)	5	Abort
0x00000010	Abort(data)	2	Abort
0x00000014	Reserved		Reserved
0x00000018	IRQ	3	IRQ
0x0000001C	FIQ	4	FIQ

Action on entering Exception



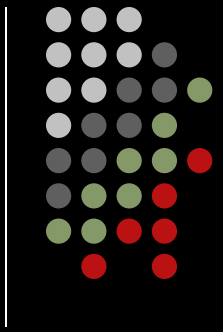
- ✓ Preserves the address of the next instruction in an appropriate Lin register(LR)
- ✓ Copies CPSR into appropriate SPSR
- ✓ Forces CPSR mode bits to a value to mode on entry of that exception occurred
- ✓ Forces PC to fetch next instruction from relevant vector address

Action on leaving exception



- ✓ Moves the Lin register(LR) to PC
- ✓ Copies SPSR to CPSR
- ✓ Clears interrupt disable flag,if any where set during entry

Nomenclature



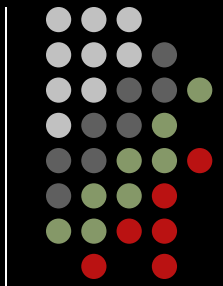
ARM {x} {y} {z} {T} {D} {M} {I} {E} {J} {F} {-s}

x – Family
y – Memory management/protection unit
z – Cache
T – Thumb 16-bit decoder
D – JTAG debug
M – fast multiplier
I – Embedded ICE macro cell
E – Enhanced instructions (assumes TDMI)
J – Jazelle
F – Vector floating-point unit
-S – Synthesizible version

Nomenclature (contd..)

x	y	z	Description	Example
7	*	*	ARM7 Processor Core	ARM7TDMI
9	*	*	ARM9 Processor Core	ARM926EJ-S
10	*	*	ARM10 Processor Core	ARM1026EJ-S
11	*	*	ARM11 Processor Core	ARM1136EJ-S
*	2	*	Cache and MMU	ARM920T
*	3	*	Cache and MMU with Physical Address Tagging	ARM1136EJ-S
*	4	*	Cache and an MPU	ARM946E-S
*	6	*	Write buffer but no cache	ARM966E-S
*	*	0	Standard cache size	ARM920T
*	*	2	Reduced Cache size	ARM922T
*	*	6	Includes TCM	ARM946E-S

Family Attribute Comparison



	ARM 7	ARM9	ARM10	ARM11
Pipeline depth	three-stage	Five-stage	Six-stage	Eight-stage
Typical MHz	80	150	260	335
mW/Mhz[a]	0.06mW/MHz	0.19mW/MHz (+ Cache)	0.5mW/MHz (+ Cache)	0.4mW/MHz (+ Cache)
MIPS[b] / MHz	0.97	1.1	1.3	1.2
Architecture	VonNeumann	Harvard	Harvard	Harvard
Multiplier	8 x 32	8x32	16x32	16x32

ARM926EJ-S

- ARM926EJ-S processor is a member of the ARM9 family of general-purpose microprocessors.

- ARM926EJ-S processor is targeted at
  - Multi-tasking applications
  - Where full memory management,
  - High performance,
  - Low die size, and
  - Low power.

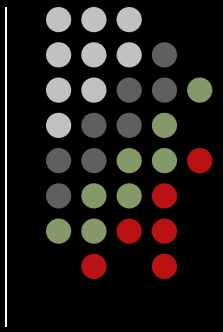
ARM926EJ-S

ARM926EJ-S is a fully synthesizable 32 bit RISC processor comprising an

- ARM926EJ-S JAVA enhanced processor core.
- Instruction and data caches
- Tightly coupled memory interfaces
- Memory Management Unit
- Separate Instruction and data AMBA – AHB bus interfaces
- New Power management system that allows
  - System level power down
  - Architectural clock stopping
  - Logic level clock gating

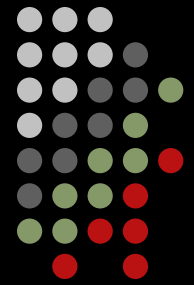
- The sizes of both caches and TCM memories can all be specified independently.
- The MMU supports virtual memory based platform operating systems such as
  - EPOC
  - LINUX
  - WindowsCE
  - PalmOS

Target Applications



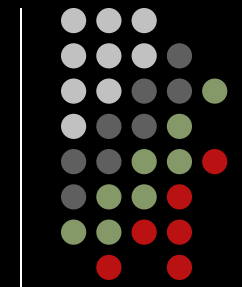
- Java enabled Mobile, Smart phones and PDAs
- Applications requiring a ploat OS:
  - EPOC
  - Linix
  - PalmOS
  - WindowsCE
- Wireless internet applications
- Networking applications
- Digital set to boxes
- Automative
  - Hands-free interfaces
  - Infotainment
- MPEG4 Video encoding and Decoding
- Autdio decoding
  - Doble AC3 digital
  - High-end MP3 players
  - AASC
- Speech Codes

Benefits



- Integrated single chip microcontroller, DSP and Java solution
- Very efficient Java byte code execution
- Reduced power consumption and chip complexity over a Java coprocessor solution
- Flexibility with tightly coupled memory system and variable size caches
- Rapid ASIC or ASSO integration with a short time-to-market
- Interface to ETM9 for real time trace support

END OF SESSION 1



THANK YOU