
AC8972A8 Datasheet

Zhuhai Jieli Technology Co.,LTD

Version: 1.0

Date: 2020.06.30

Copyright © Zhuhai Jieli Technology Co.,LTD. All rights reserved.

AC8972A8 Features

CPU

- 32-bit DSP supports hardware Float Point Unit(FPU)
- Up to 160MHz programmable processor
- 64Vectored interrupts
- 4 Levels interrupt priority

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codecs supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Acoustic echo cancellation/suppression (AEC,AES)
- Single analog MIC, Dual digital MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 20-band EQ configuration for voice Effects

Audio Codec

- Two channels 24-bit DAC, SNR >= 101dB
- Two channels 24-bit ADC , SNR >= 92dB
- Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
- One analog MIC amplifier, build-in MIC bias generator
- Supports two PDM digital MIC inputs
- One channel Stereo analog MUX
- Supports cap-less, single-ended, and differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth V5.1+BR+EDR+BLE specification

- Meet class1 class2 and class3 transmitting power requirement
- Support GFSK and $\pi/4$ DQPSK all packet types
- Provides amaximum+8dBm transmitting power
- receiver with -94dBm sensitivity
- Fast AGC for enhanced dynamic range
- Supports a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap gatt\rfcomm\sdp\l2cap profile

Peripherals

- One full speed USB 2.0 OTG controller
- Six multi-function 32-bit timers, support capture and PWM mode
- Three full-duplex basic UART, support DMA mode
- One hardware IIC interface supports host and device mode
- Two Built-in low power Cap Sense Keys
- Built-in Cap Sense Key controller
- 10-bit ADC for analog sampling
- External wake up/interrupt on all GPIO

PMU

- Low voltage LDO and DC-DC for internal digital and analog circuit supply
- 2uA current consumption in the soft-off mode
- Built-in LDO and DC-DC for the core, I/O, Bluetooth and flash
- VBAT is 2.2V to 4.5V
- VDDIO is 2.2V to 3.4V

Packages

- QFN22(3mm*2.5mm)

Temperature

- Operating temperature: -40°C to +85°C

● Storage temperature: -65°C to +150°C

Applications

● Bluetooth TWS headset



1、 Pin Definition

1.1 Pin Assignment

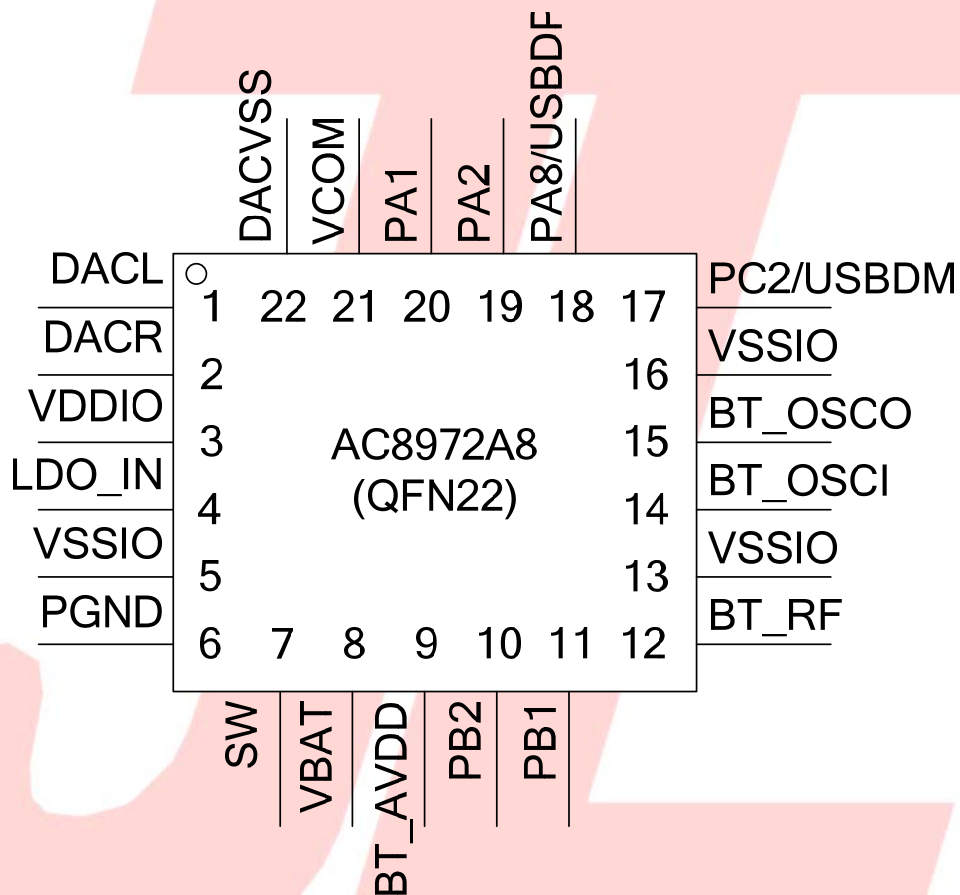


Figure 1-1 AC8972A8 Package Diagram

1.2 Pin Description

Table 1-1 AC8972A8 Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	DACL	O	/		DAC Left Channel
2	DACR	O	/		DAC Right Channel
3	VDDIO	P	/		IO Power 3.3v
4	LDO_IN	P	/		Charge Power 5v
5	VSSIO	P	/		Ground
6	PGND	P	/		DCDC Ground
7	SW	P	/		DC-DC switch output, connected to inductor
8	VBAT	P	/		LDO Power,connect
9	BT_AVDD	P	/		BT Power
10	PB2	I/O	8/24	GPIO	UART2RXC: Uart2 Data Input(C); CAP5: Timer5 Capture; ADC7: ADC Input Channel 7; LP_TH1: Low Power Touch Channel 1
11	PB1	I/O	8/24	GPIO (pull up)	Long Press Reset; UART2TXC: Uart2 Data Output(C) ADC6: ADC Input Channel 6; LP_TH0: Low Power Touch Channel 0
12	BT_RF	/	/		BT Antenna
13	VSSIO	P	/		Ground
14	BT_OSCI	I	/		BTOSC In
15	BT_OSCO	O	/		BTOSC Out
16	VSSIO	P	/		Ground
17	PC2	I/O	8/24	GPIO	UART0TXD: Uart0 Data Output(D); TMR1: Timer1 Clock Input;
	USBDM	I/O	4	USB Negative Data	UART1RXD: Uart1 Data Input(D); IIC_SDA_A: IIC SDA(A); ADC11: ADC Input Channel 11;
18	USBDP	I/O	4	USB Positive Data	UART1TXD: Uart1 Data Output(D); IIC_SCL_A: IIC SCL(A); ADC10: ADC Input Channel 10;
	PA8	I/O	8/24	GPIO	UART2RXB: Uart2 Data Input(B); ADC3: ADC Input Channel 3; Touch5: Touch Input Channel 5;

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

19	PA2	I/O	8/24	GPIO	MIC_BIAS0: MIC0 Bias Output; MIC0_N: Different MIC0 Negative CAP3: Timer3 Capture; UART1RXC: Uart1 Data In(C);
20	PA1	I/O	8/24	GPIO	MIC0: MIC0 Input Channel ; MIC0_P: Different MIC0 Positive PWM0: Timer0 PWM Output; UART1TXC: Uart1 Data Output(C);
21	VCOM	P	/		DAC reference voltage
22	DACVSS	P	/		Ground

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
T _{opt}	Operating temperature	-40	+85	°C
T _{stg}	Storage temperature	-65	+150	°C
V _{BAT}	Supply Voltage	-0.3	4.5	V
LDO_IN	Charger Voltage	-0.3	6	V
V _{3.3IO}	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 Recommended Operating Conditions

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{BAT}	Voltage Input	2.2	3.7	4.5	V	
LDO_IN	Charger Voltage	4.5	5.0	5.5	V	
V _{3.3}	Voltage output	2.2	3.0	3.4	V	V _{BAT} = 4.2V, 100mA loading
V _{BT_AVDD}	Voltage output	1.2	1.25	1.35	V	V _{BAT} =4.2V, 100mA loading
I _{L3.3}	Loading current	—	—	150	mA	V _{BAT} = 4.2V

2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDO_IN	Charge Input Voltage	4.5	5	5.5	V	—
V _{Charge}	Charge Voltage	4.15	4.2	4.25	V	—
I _{Charge}	Charge Current	20		200	mA	Charge current at fast charge mode
I _{Trikl}	Trickle Charge Current	20	45	70	mA	V _{BAT} < V _{Trikl}

2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Low-Level Input Voltage	-0.3	—	$0.3 * V_{DDIO}$	V	$V_{DDIO} = 3.3V$
V_{IH}	High-Level Input Voltage	$0.7 * V_{DDIO}$	—	$V_{DDIO} + 0.3$	V	$V_{DDIO} = 3.3V$
IO output characteristics						
V_{OL}	Low-Level Output Voltage	—	—	0.33	V	$V_{DDIO} = 3.3V$
V_{OH}	High-Level Output Voltage	2.7	—	—	V	$V_{DDIO} = 3.3V$

2.5 Internal Resistor Characteristics

Table 2-5

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA1,PA2 PC2 PB1 ,PB2 PA8	8mA	24mA	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull down 3、internal pull-up/pull-down resistance accuracy $\pm 20\%$
USBDP	4mA	—	1.5K	15K	
USBDM	4mA	—	180K	15K	

2.6 DAC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	—	20K	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	—	-80	—	dB	
S/N	—	101	—	dB	
Crosstalk	—	-80	—	dB	
Output Swing	—	0.45	—	Vrms	
Dynamic Range	—	90	—	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
DAC Output Power	—	4	—	mW	32ohm loading

2.7 ADC Characteristics

Table 2-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		80		dB	1KHz/-60dB
S/N	—	92	93	dB	1KHz/-60dB
THD+N	—	-75	—	dB	
Crosstalk	—	-80	—	dB	

2.8 BT Characteristics

2.8.1 Transmitter

Basic Data Rate

Table 2-8

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		6	8	dBm	25℃, Power Supply VBAT=5V 2441MHz
RF Power Control Range		20		dB	
20dB Bandwidth		950		KHz	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Enhanced Data Rate

Table 2-9

Parameter	Min	Typ	Max	Unit	Test Conditions
Relative Power		-1		dB	25℃, Power Supply VBAT=5V 2441MHz
$\pi/4$ DQPSK Modulation Accuracy	DEVM RMS	6		%	
	DEVM 99%	10		%	
	DEVM Peak	15		%	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2.8.2 Receiver

Basic Data Rate

Table 2-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25°C, Power Supply VBAT=5V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel Interference Rejection	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Enhanced Data Rate

Table 2-11

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25°C, Power Supply VBAT=5V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel Interference Rejection	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

3、 Package Information

3.1 QFN22_3.0x2.5

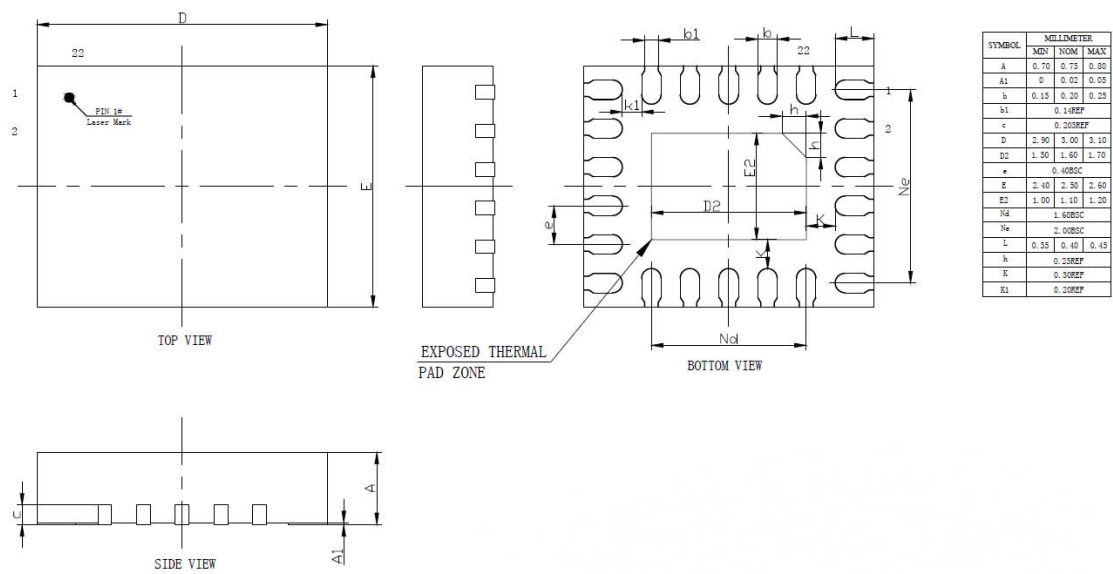


Figure 3-1 AC8972A8 Package

4、Revision History

Date	Revision	Description
2020.06.30	V1.0	Initial Release

Confidential

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.