PISA REFERENCE DATA

PISA

Category	Name	Fmt	Syntax	Description	Addressing Mode	Opcode	Func
Data	Addition	R	Addp Rd, Rs1, Rs2	Rd = Rs1 + Rs2	Register	000	00
Data	Subtraction	R	Subp Rd, Rs1, Rs2	Rd = Rs1 - Rs2	Register	000	01
Data	Multiplication	R	Mulp Rd, Rs1, Rs2	Rd = Rs1 * Rs2	Register	000	10
Data	Division	R	Divp Rd, Rs1, Rs2	Rd = Rs1 / Rs2	Register	000	11
Data	And	R	Andp Rd, Rs1, Rs2	Rd = Rs1 & Rs2	Register	001	00
Data	Or	R	Orp Rd, Rs1, Rs2	Rd = Rs1 | Rs2	Register	001	01
Data	Compare	R	Cmpp Rs1, Rs2	Rs1 ? Rs2	Register	001	10
Data	Addition Immediate	I	Addip Rd, Rs1, Imm	Rd = Rs1 + Imm	Immediate	010	00
Data	Shift Left Logic Immdiate	I	Sllip Rd, Rs1, Imm	Rd = Rs1 << Imm[0:4]	Immediate	010	01
Data	Shift Right Logic Immdiate	I	Srlip Rd, Rs1, Imm	Rd = Rs1 >> Imm[0:4]	Immediate	010	10
Load/Store	Load Byte	I	Lbp Rd, Rs1, Imm	Rd = M[Rs1 + Imm]	Immediate (Base + Offset)	011	00
Load/Store	Load Word	I	Lwp Rd, Rs1, Imm	Rd = M[Rs1 + Imm]	Immediate (Base + Offset)	011	01
Load/Store	Store Byte	S	Sbp Rs2, Rs1, Imm	M[Rs1 + Imm] = Rs2	Immediate (Base + Offset)	100	00
Load/Store	Store Word	S	Swp Rs2, Rs1, Imm	M[Rs1 + Imm] = Rs2	Immediate (Base + Offset)	100	01
Control	Branch Less Than	B	Bltp Dir	If(Rs1 < Rs2) PC += Imm	Immediate	101	00
Control	Branch Greater Equal	B	Bgep Dir	If(Rs1 >= Rs2) PC += Imm	Immediate	101	01
Control	Jump	B	Jump Dir	PC += Imm	Immediate	101	10

Basic Instruction Formats

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
mat\Bits	19:15					14:10					9:5					4:3		2:0	
R-type	Rs2					Rs1					Rd					Funct2		Opco	
I-type	Imm[4:0]					Rs2					Rd					Funct3		Opco	
S-type	Rs2					Rs3					Imm[4:0]					Funct4		Opco	
B-type	Imm[14:0]															Funct5		Opco	

Register Name And Usage

Register	Name	Description
x0	zero	Hard-wired zero
x1	v0	Function return value
x2-x5	a0-a3	Return values
x6-x15	s0-s9	Saved register
x16-x31	t0-t15	Temporaries