

# Kunal Banerjee

Research Scientist

Intel Parallel Computing Lab

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## Research Interests

Formal Verification, Formal Methods, Program Analysis, Parallel Programming.

## Education

2010–2016 **PhD, Computer Science and Engineering**, Indian Institute of Technology Kharagpur, India.

Thesis: *Translation Validation of Optimizing Transformations of Programs using Equivalence Checking*

Supervisors: Prof. Chittaranjan Mandal and Prof. Dipankar Sarkar

GPA: 9.28/10 (based on courses taken)

2004–2008 **B.Tech.(Honors), Computer Science and Engineering**, Heritage Institute of Technology, (West Bengal University of Technology).

Thesis: *TDMA Scheduling in Wireless Sensor Networks*

Supervisor: Prof. Nabanita Das, Indian Statistical Institute, Kolkata

GPA: 8.49/10

## Publications

### Journals

- 1 **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.  
Deriving Bisimulation Relations from Path Extension Based Equivalence Checkers.  
*IEEE Transactions on Software Engineering (TSE)*, (accepted).
- 2 **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.  
Deriving Bisimulation Relations from Path Based Equivalence Checkers.  
*Formal Aspects of Computing (FAOC)*, vol. 29, no. 2, 2017, pages: 365–379.
- 3 Soumyadip Bandyopadhyay, Dipankar Sarkar, Chittaranjan Mandal, **Kunal Banerjee**, Krishnam Raju Duddu.  
A Path Construction Algorithm for Translation Validation using PRES+ Models.  
*Parallel Processing Letters (PPL)*, vol. 26, no. 2, 2016, pages: 1–25.
- 4 **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.  
Extending the FSM-D Framework for Validating Code Motions of Array-Handling Programs.  
*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no. 12, 2014, pages: 2015–2019.
- 5 **Kunal Banerjee**, Chandan Karfa, Dipankar Sarkar, Chittaranjan Mandal.  
Verification of Code Motion Techniques using Value Propagation.  
*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no. 8, 2014, pages: 1180–1193.
- 6 Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.  
Verification of Loop and Arithmetic Transformations of Array-Intensive Behaviours.  
*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 11, 2013, pages: 1787–1800.

### Conferences / Workshops

- 1 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.  
An Equivalence Checking Framework for Array-Intensive Programs.  
*Automated Technology for Verification and Analysis (ATVA)*, Pune, India, 2017, (accepted).
- 2 Soumyadip Bandyopadhyay, Santonu Sarkar, **Kunal Banerjee**.  
An End-to-end Formal Verifier for Parallel Programs.  
*International Conference on Software Technologies (ICSOT)*, Madrid, Spain, 2017, pages: 388–393.

- 3 Soumyadip Bandyopadhyay, **Kunal Banerjee**.  
PRESGen: A Fully Automatic Equivalence Checker for Validating Optimizing and Parallelizing Transformations.  
*Software Engineering Methods for Parallel and High Performance Applications (SEM4HPC)*, Washington D.C., United States, 2017, pages:13–20.
- 4 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.  
Translation Validation of Loop and Arithmetic Transformations in the Presence of Recurrences.  
*ACM SIGPLAN/SIGBED Conference on Languages, Compilers, Tools and Theory for Embedded Systems (LCTES)*, Santa Barbara, United States, 2016, pages: 31–40.
- 5 **Kunal Banerjee**, Soumyadip Banerjee, Santonu Sarkar.  
Data-Race Detection: The Missing Piece for an End-to-End Semantic Equivalence Checker for Parallelizing Transformations of Array-Intensive Programs.  
*ACM SIGPLAN International Workshop on Libraries, Languages and Compilers for Array Programming (ARRAY)*, Santa Barbara, United States, 2016, pages: 1–8.
- 6 Soumyadip Bandyopadhyay, **Kunal Banerjee**.  
Implementing an Efficient Path Based Equivalence Checker for Parallel Programs.  
*Software Engineering Methods for Parallel and High Performance Applications (SEM4HPC)*, Kyoto, Japan, 2016, pages: 3–10.
- 7 K. K. Sharma, **Kunal Banerjee**, Chittaranjan Mandal.  
Determining Equivalence of Expressions: An Automated Evaluator’s Perspective.  
*Technology for Education (T4E)*, Warangal, India, 2015, pages: 35–36.
- 8 K. K. Sharma, **Kunal Banerjee**, Chittaranjan Mandal.  
Establishing Equivalence of Expressions: An Automated Evaluator Designer’s Perspective.  
*Mining Intelligence and Knowledge Exploration (MIKE)*, Hyderabad, India, 2015, pages: 415–423.
- 9 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.  
A Translation Validation Framework for Symbolic Value Propagation Based Equivalence Checking of FSM-DAs.  
*Source Code Analysis and Manipulation (SCAM)*, Bremen, Germany, 2015, (accepted).
- 10 Soumyadip Bandyopadhyay, Dipankar Sarkar, **Kunal Banerjee**, Chittaranjan Mandal.  
A Path-Based Equivalence Checking Method for Petri net based Models of Programs.  
*International Conference on Software Engineering and Applications (ICSOFT-EA)*, Colmar, France, 2015, pages: 319–329.
- 11 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.  
Translation Validation of Transformations of Embedded System Specifications using Equivalence Checking.  
*IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Montpellier, France, 2015, pages: 183–186, (**received Best PhD Forum Paper Award**).
- 12 K K Sharma, **Kunal Banerjee**, Chittaranjan Mandal.  
A Scheme for Automated Evaluation of Programming Assignments using FSM-D based Equivalence Checking.  
*IBM Collaborative Academia Research Exchange (I-CARE)*, Bangalore, India, 2014, pages: 10:1–10:4.
- 13 Partha De, **Kunal Banerjee**, Chittaranjan Mandal, Debdeep Mukhopadhyay.  
Circuits and Synthesis Mechanism for Hardware Design to Counter Power Analysis Attacks.  
*Euromicro Conference on Digital System Design (DSD)*, Verona, Italy, 2014, pages: 520–527.
- 14 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.  
Extending the Scope of Translation Validation by Augmenting Path Based Equivalence Checkers with SMT Solvers.  
*International Symposium on VLSI Design and Test (VDATE)*, Coimbatore, India, 2014, pages: 1–6.
- 15 Partha De, **Kunal Banerjee**, Chittaranjan Mandal.  
A BDD based Secure Hardware Design Method to Guard Against Power Analysis Attacks.  
*International Symposium on VLSI Design and Test (VDATE)*, Coimbatore, India, 2014, pages: 1–2.
- 16 Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.  
Experimentation with SMT Solvers and Theorem Provers for Verification of Loop and Arithmetic Transformations.  
*IBM Collaborative Academia Research Exchange (I-CARE)*, Delhi, India, 2013, pages: 3:1–3:4, (**received Best Paper Award**).

- 17 Partha De, **Kunal Banerjee**, Chittaranjan Mandal, Debdeep Mukhopadhyay.  
Designing DPA Resistant Circuits Using BDD Architecture and Bottom Pre-charge Logic.  
*Euromicro Conference on Digital System Design (DSD)*, Santander, Spain, 2013, pages: 641–644.
- 18 **Kunal Banerjee**, Chandan Karfa, Dipankar Sarkar, Chittaranjan Mandal.  
A Value Propagation Based Equivalence Checking Method for Verification of Code Motion Techniques.  
*International Symposium on Electronic System Design (ISED)*, Kolkata, India, 2012, pages: 67–71.
- 19 Soumyadip Bandyopadhyay, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.  
Translation Validation for PRES+ Models of Parallel Behaviours via an FSM-D Equivalence Checker.  
*International Symposium on VLSI Design and Test (VDATE)*, Shibpur, India, 2012. Published in Lecture Notes in Computer Science (LNCS), vol. 7373, pages: 69–78.
- 20 Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.  
Equivalence Checking of Array-Intensive Programs.  
*IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Chennai, India, 2011, pages: 156–161.
- 21 **Kunal Banerjee**, Priyanko Basuchaudhuri, Debesh Sadhukhan, Nabanita Das.  
A Fair Multiple-Slot Assignment Protocol for TDMA Scheduling in Wireless Sensor Network.  
*Workshop on Mobile Systems (WoMS)*, Kolkata, India, 2008, pages: 65–71.

## Others

- 1 Abhisek Kundu, **Kunal Banerjee**, Naveen Mellempudi, Dheevatsa Mudigere, Dipankar Das, Bharat Kaul, Pradeep Dubey.  
Ternary Residual Networks.  
*arXiv:1707.04679*, pages: 1–19.
- 2 **Kunal Banerjee**.  
Translation Validation of Transformations of Embedded System Specifications using Equivalence Checking.  
*Inter-Research-Institute Student Seminar in Computer Science (IRISS)*, Goa, India, 2015, pages: 1–2.
- 3 **Kunal Banerjee**.  
An Equivalence Checking Mechanism for Handling Recurrences in Array-Intensive Programs.  
*ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages (POPL): Student Research Competition*, Mumbai, India, 2015, pages: 1–2.
- 4 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.  
Deriving Bisimulation Relations from Path Extension Based Equivalence Checkers.  
*IMPECS-POPL Workshop on Emerging Research and Development Trends in Programming Languages (WEPL)*, Mumbai, India, 2015, pages: 1–2.

## Professional Experience

2015–present **Parallel Computing Lab, Intel Labs.**

Designation: Research Scientist

Domains: Parallel programming, code optimization, unsupervised learning

2009–2012 **Sponsored Research and Industrial Consultancy, Indian Institute of Technology Kharagpur.**

Designation: Senior Research Fellow

Project Title: Extending the scope of equivalence checking in complex embedded system design verification

Sponsor: Department of Science and Technology, Govt. of India

2008–2009 **Tata Consultancy Services Ltd.**

Designation: Assistant System Engineer

Project Title: Database management for McGraw-Hill Education

## Teaching Experience

**Indian Institute of Technology Kharagpur**

## Teaching Assistant

Autumn 2014 *Programming and Data Structures* for Prof. Soumyajit Dey  
Spring 2014 *Programming and Data Structures* for Prof. Niloy Ganguly  
Autumn 2013 *Discrete Structures* for Prof. Animesh Mukherjee  
Spring 2013 *Programming and Data Structures* for Prof. Partha Bhowmick  
Autumn 2012 *Theory of Computation* for Prof. Goutam Biswas  
Spring 2012 *Computer Architecture and Operating Systems* for Prof. Dipankar Sarkar  
Spring 2011 *Formal Systems* for Prof. Sujoy Ghose  
Autumn 2010 *Discrete Structures* for Prof. Sudeshna Sarkar  
Spring 2010 *Programming and Data Structures Lab* for Prof. Goutam Biswas  
Autumn 2009 *Computer Organization and Architecture Lab* for Prof. Indranil Sengupta, Prof. Dipankar Sarkar, Prof. Chittaranjan Mandal, Prof. Debdeep Mukhopadhyay

## Instructor, AVLSI Lab Summer Course

Summer 2010 Gave a lecture on “Logic Synthesis”, Student co-ordinator for the digital group

## Talks

- 1 Translation Validation of Embedded System Specifications using Equivalence Checking, *Tata Research Development and Design Centre (TRDDC)*, Pune, India, 2014.
- 2 Translation Validation using Path Based Equivalence Checkers Augmented with SMT Solvers, *Formal Methods Update Meeting 2014*, Kharagpur, India, 2014.

## Awards/Achievements

2017 Invited to present our TSE 2017 paper at ESEC/FSE 2017  
2015 Best PhD Forum Paper Award in the conference ISVLSI 2015  
2013 Best Paper Award in the conference I-CARE 2013  
2012 TCS Research Fellowship

## Technical Skills

Programming: C, C++, Java, Python, PL/SQL, Scheme, Prolog, Lisp, Visual Basic and others along with some scripting and markup languages  
Tools: ACL2, Caffe, CUDD, CVC, ISL, Yices, Z3  
Languages: Bengali, English, Hindi

## References

Available on request.