Kunal Banerjee

Research Scientist

Intel Parallel Computing Lab
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Research Interests

Program Analysis, Formal Methods, High-Performance Computing, Deep Learning.

Education

2010–2016 **PhD, Computer Science and Engineering**, *Indian Institute of Technology Kharagpur*, India.
Thesis: *Translation Validation of Optimizing Transformations of Programs using Equivalence Checking*
Supervisors: Prof. Chittaranjan Mandal and Prof. Dipankar Sarkar
GPA: 9.28/10 (based on courses taken)

2004–2008 **B.Tech.(Honors), Computer Science and Engineering**, *Heritage Institute of Technology*, (West Bengal University of Technology).
Thesis: *TDMA Scheduling in Wireless Sensor Networks*
Supervisor: Prof. Nabanita Das, Indian Statistical Institute, Kolkata
GPA: 8.49/10

Selected Publications

Journals

1 Ramanuj Chouksey, Chandan Karfa, **Kunal Banerjee**, Pankaj Kalita, Purandar Bhaduri.
A Counter-Example Generation Procedure for Path based Equivalence Checkers.
IET Software, (accepted).

2 **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Deriving Bisimulation Relations from Path Extension Based Equivalence Checkers.
IEEE Transactions on Software Engineering (TSE), vol. 43, no. 10, 2017, pages: 946–953.

3 **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Deriving Bisimulation Relations from Path Based Equivalence Checkers.
Formal Aspects of Computing (FAOC), vol. 29, no. 2, 2017, pages: 365–379.

4 Soumyadip Bandyopadhyay, Dipankar Sarkar, Chittaranjan Mandal, **Kunal Banerjee**, Krishnam Raju Duddu.
A Path Construction Algorithm for Translation Validation using PRES+ Models.
Parallel Processing Letters (PPL), vol. 26, no. 2, 2016, pages: 1–25.

5 **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Extending the FSMD Framework for Validating Code Motions of Array-Handling Programs.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 33, no. 12, 2014, pages: 2015–2019.

6 **Kunal Banerjee**, Chandan Karfa, Dipankar Sarkar, Chittaranjan Mandal.
Verification of Code Motion Techniques using Value Propagation.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 33, no. 8, 2014, pages: 1180–1193.

7 Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Verification of Loop and Arithmetic Transformations of Array-Intensive Behaviours.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 32, no. 11, 2013, pages: 1787–1800.

Conferences / Workshops

1 Evangelos Georganas, Sasikanth Avancha, **Kunal Banerjee**, Dhiraj Kalamkar, Greg Henry, Hans Pabst, Alexander Heinecke.
Anatomy Of High-Performance Deep Learning Convolutions On SIMD Architectures.
International Conference for High Performance Computing, Networking, Storage, and Analysis (SC), Dallas, USA, 2018, pages: 66:1–66:12.

2 **Kunal Banerjee**, Ramanuj Chouksey, Chandan Karfa, Pankaj Kumar Kalita.
Poster: Automatic Detection of Inverse Operations while Avoiding Loop Unrolling.
International Conference on Software Engineering (ICSE), Gothenburg, Sweden, 2018, pages: 175–176.

3 Dipankar Das, Naveen Mellempudi, Dheevatsa Mudigere, Dhiraj Kalamkar, Sasikanth Avancha, **Kunal Banerjee**, Srinivas Sridharan, Karthik Vaidyanathan, Bharat Kaul, Evangelos Georganas, Alexander Heinecke, Pradeep Dubey, Jesus Corbal, Nikita Shustrov, Roma Dubtsov, Evarist Fomenko, Vadim Pirogov.
Mixed Precision Training of Convolutional Neural Networks using Integer Operations.
International Conference on Learning Representations (ICLR), Vancouver, Canada, 2018, pages: 1–11.

4 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.
An Equivalence Checking Framework for Array-Intensive Programs.
Automated Technology for Verification and Analysis (ATVA), Pune, India, 2017, pages: 84–90.

5 Soumyadip Bandyopadhyay, Santonu Sarkar, **Kunal Banerjee**.
An End-to-end Formal Verifier for Parallel Programs.
International Conference on Software Technologies (ICSOFT), Madrid, Spain, 2017, pages: 388–393.

6 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.
Translation Validation of Loop and Arithmetic Transformations in the Presence of Recurrences.
Languages, Compilers, Tools and Theory for Embedded Systems (LCTES), Santa Barbara, USA, 2016, pages: 31–40.

7 **Kunal Banerjee**, Soumyadip Banerjee, Santonu Sarkar.
Data-Race Detection: The Missing Piece for an End-to-End Semantic Equivalence Checker for Parallelizing Transformations of Array-Intensive Programs.
International Workshop on Libraries, Languages and Compilers for Array Programming (ARRAY), Santa Barbara, USA, 2016, pages: 1–8.

8 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.
A Translation Validation Framework for Symbolic Value Propagation Based Equivalence Checking of FSMDAs.
Source Code Analysis and Manipulation (SCAM), Bremen, Germany, 2015, pages: 247–252.

9 Soumyadip Bandyopadhyay, Dipankar Sarkar, **Kunal Banerjee**, Chittaranjan Mandal.
A Path-Based Equivalence Checking Method for Petri net based Models of Programs.
International Conference on Software Engineering and Applications (ICSOFT-EA), Colmar, France, 2015, pages: 319–329.

10 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.
Translation Validation of Transformations of Embedded System Specifications using Equivalence Checking.
IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Montpellier, France, 2015, pages: 183–186, **(received Best PhD Forum Paper Award)**.

11 Partha De, **Kunal Banerjee**, Chittaranjan Mandal, Debdeep Mukhopadhyay.
Circuits and Synthesis Mechanism for Hardware Design to Counter Power Analysis Attacks.
Euromicro Conference on Digital System Design (DSD), Verona, Italy, 2014, pages: 520–527.

12 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.
Extending the Scope of Translation Validation by Augmenting Path Based Equivalence Checkers with SMT Solvers.
International Symposium on VLSI Design and Test (VDAT), Coimbatore, India, 2014, pages: 1–6.

13 Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Experimentation with SMT Solvers and Theorem Provers for Verification of Loop and Arithmetic Transformations.
IBM Collaborative Academia Research Exchange (I-CARE), Delhi, India, 2013, pages: 3:1–3:4, **(received Best Paper Award)**.

14 Partha De, **Kunal Banerjee**, Chittaranjan Mandal, Debdeep Mukhopadhyay.
Designing DPA Resistant Circuits Using BDD Architecture and Bottom Pre-charge Logic.
Euromicro Conference on Digital System Design (DSD), Santander, Spain, 2013, pages: 641–644.

15 **Kunal Banerjee**, Chandan Karfa, Dipankar Sarkar, Chittaranjan Mandal.
A Value Propagation Based Equivalence Checking Method for Verification of Code Motion Techniques.
International Symposium on Electronic System Design (ISED), Kolkata, India, 2012, pages: 67–71.

16 Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Equivalence Checking of Array-Intensive Programs.
IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Chennai, India, 2011, pages: 156–161.

Others

1 **Kunal Banerjee**, Chandan Karfa.
A Quick Introduction to Functional Verification of Array-Intensive Programs.
arXiv:1905.09137, pages: 1–7.

2 **Kunal Banerjee**, Evangelos Georganas, Dhiraj Kalamkar, Alexander Heinecke.
Optimizing Deep Learning LSTM Topologies on Intel Xeon Architecture.
ISC High Performance, Frankfurt, Germany, 2019, (Research Poster).

3 Alexander Heinecke, Evangelos Georganas, **Kunal Banerjee**, Dhiraj Kalamkar, Narayanan Sundaram, Anand Venkat, Greg Henry, Hans Pabst.
Understanding the Performance of Small Convolution Operations for CNN on Intel Architecture.
International Conference for High Performance Computing, Networking, Storage and Analysis (SC), Denver, USA, 2017, (Poster abstract).

4 Abhisek Kundu, **Kunal Banerjee**, Naveen Mellempudi, Dheevatsa Mudigere, Dipankar Das, Bharat Kaul, Pradeep Dubey.
Ternary Residual Networks.
arXiv:1707.04679, pages: 1–19.
(Accepted as extended abstract in SysML 2018. Presented at Intel AI DevCon 2018.)

5 **Kunal Banerjee**.
An Equivalence Checking Mechanism for Handling Recurrences in Array-Intensive Programs.
Principles of Programming Languages (POPL): Student Research Competition, Mumbai, India, 2015, pages: 1–2.

Professional Experience

2015–present **Parallel Computing Lab**, *Intel Labs*.
Designation: Research Scientist
Domains: Parallel programming, code optimization, deep learning

2009–2012 **Sponsored Research and Industrial Consultancy**, *Indian Institute of Technology Kharagpur*.
Designation: Senior Research Fellow
Project Title: Extending the scope of equivalence checking in complex embedded system design verification
Sponsor: Department of Science and Technology, Govt. of India

2008–2009 **Tata Consultancy Services Ltd**.
Designation: Assistant System Engineer
Project Title: Database management for McGraw-Hill Education

Teaching Experience

Indian Institute of Technology Kharagpur

Teaching Assistant
Autumn 2014 *Programming and Data Structures* for Prof. Soumyajit Dey
Spring 2014 *Programming and Data Structures* for Prof. Niloy Ganguly

Autumn 2013	*Discrete Structures* for Prof. Animesh Mukherjee
Spring 2013	*Programming and Data Structures* for Prof. Partha Bhowmick
Autumn 2012	*Theory of Computation* for Prof. Goutam Biswas
Spring 2012	*Computer Architecture and Operating Systems* for Prof. Dipankar Sarkar
Spring 2011	*Formal Systems* for Prof. Sujoy Ghose
Autumn 2010	*Discrete Structures* for Prof. Sudeshna Sarkar
Spring 2010	*Programming and Data Structures Lab* for Prof. Goutam Biswas
Autumn 2009	*Computer Organization and Architecture Lab* for Prof. Indranil Sengupta, Prof. Dipankar Sarkar, Prof. Chittaranjan Mandal, Prof. Debdeep Mukhopadhyay
	Instructor, AVLSI Lab Summer Course
Summer 2010	Gave a lecture on "Logic Synthesis", Student co-ordinator for the digital group

Tutorials / Talks

1. Compiler-agnostic Translation Validation, *Innovations in Software Engineering Conference (ISEC)*, Hyderabad, India, 2018.
2. Translation Validation of Embedded System Specifications using Equivalence Checking, *Tata Research Development and Design Centre (TRDDC)*, Pune, India, 2014.
3. Translation Validation using Path Based Equivalence Checkers Augmented with SMT Solvers, *Formal Methods Update Meeting 2014*, Kharagpur, India, 2014.

Awards/Achievements

2018	Division Recognition Award from Intel
2018	Techno Inventor Award (PhD) 2017 from India Electronics & Semiconductor Association (IESA)
2018	Best PhD Thesis Award at VLSI Design 2018
2017	Invited to present our TSE 2017 paper at ESEC/FSE 2017
2015	Best PhD Forum Paper Award in the conference ISVLSI 2015
2013	Best Paper Award in the conference I-CARE 2013
2012	TCS Research Fellowship

Technical Skills

Programming:	C, C++, Java, Python, PL/SQL, Scheme, Prolog, Lisp, Visual Basic and others along with some scripting and markup languages
Tools:	ACL2, Caffe, CUDD, CVC, ISL, Yices, Z3
Languages:	Bengali, English, Hindi

References

Available on request.