Kunal Banerjee

Staff Data Scientist
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Research Interests

Deep Learning, High-Performance Computing, Program Analysis, Formal Methods.

Education

2010–2016 **PhD, Computer Science and Engineering**, *Indian Institute of Technology Kharagpur*, India.
Thesis: *Translation Validation of Optimizing Transformations of Programs using Equivalence Checking*
Supervisors: Prof. Chittaranjan Mandal and Prof. Dipankar Sarkar
GPA: 9.28/10 (based on courses taken)

2004–2008 **B.Tech.(Honors), Computer Science and Engineering**, *Heritage Institute of Technology*, (West Bengal University of Technology).
Thesis: *TDMA Scheduling in Wireless Sensor Networks*
Supervisor: Prof. Nabanita Das, Indian Statistical Institute, Kolkata
GPA: 8.49/10

Professional Experience

Sep 2020–Present **Data Science Foundation**, *Walmart Global Tech*.
Designation: Principal Data Scientist (May 2023 – Present)
Designation: Staff Data Scientist (Sep 2020 – Apr 2023)
Domains: Machine Learning, Data Science, High Performance Computing
Description:

- **A/B Testing:** Showcased the efficacy of incorporating sequential testing (using $\alpha/\beta-$spending methods) in A/B Testing framework — ∼50% of the experiments in our dataset terminated early with a maximum savings of 70% for an individual experiment. The results were praised by the Pillar Head and incorporated into Walmart's experimentation framework, and is expected to save upwards of 1 Billion USD annually. Following the success of this initial collaboration with the experimentation team, new ML-based projects have been incorporated into the roadmap.
- **Expedite Deep Learning Models with DeepSpeed:** Empirically established the potency of Microsoft's DeepSpeed library in training deep learning models; for our CNN-based OCR model, the time-to-train was reduced by 35% on 1 Nvidia V100 GPU and by 65% on 4 GPUs, whereas for Transformer-based BERT model, the training time was reduced by 50%. Based on the success of this project, Walmart launched training-as-a-service for the first time in contrast to earlier inference-as-a-service only model. Integrating DeepSpeed into our AI Services is expected to result in 250K USD in savings annually.
- **Explainability in Change Risk Assessment:** Predicting the risk associated with a software change using ML technology can be of crucial importance; in fact, this project has helped save more than 2.6 Million USD for Walmart in a single quarter. However, initially, there was a push back from the human change risk assessors for the ML solution; introducing explainability through decision tree-based global surrogate model and LIME for local explanations helped in building trust and adoption of the ML solution.
- **Comparative Analysis for AI Governance:** Collaborated with system engineers from the ML Platform team in Walmart to assess various products related to AI Governance – these products were from different companies including Google, Microsoft, IBM and Seldon. Personally, looked into fairness, explainability and drift detection capabilities provided by these tools. This analysis helped shape Walmart's processes in AI Governance domain.

Jan 2020–Aug 2020 **Artificial Intelligence Products Group**, *Intel Corp.*

Designation: Senior Deep Learning R&D Engineer

2015–2019 **Parallel Computing Lab**, *Intel Labs.*

Designation: Research Scientist

Domains: Parallel Programming, Code Optimization, Deep Learning

Description:

- **Code Optimization for Intel Architecture (IA):** Implemented convolution using Winograd algorithm in the open source LIBXSMM library (and later in Intel MKL-DNN framework), which provides up to 3x performance gain relative to direct convolution (e.g., Overfeat topology) on Xeon and Xeon Phi architectures. Also implemented RNN, LSTM and GRU layers in LIBXSMM which exceeds MKL-DNN performance by 1.4x on Skylake CPUs. Showcased that the single batch-reduce GEMM kernel implemented in LIBXSMM can act as the innermost kernel for a variety of deep learning topologies delivering SOTA performance – thereby boosting programmer productivity which otherwise is spent tuning various kernels across different topologies. Note that these libraries have been adopted in several software products including TensorFlow, Caffe, MS CNTK, Apache MXNet, Chainer, OpenVINO among others for enhanced performance on IA.
- **Low Precision DNN:** Developed and implemented the concept of Ternary Residual Network (TRN) in Intel Caffe, which uses 8-bits for activations and 2-bits for weights (with residual edges, if required) for neural networks. The resulting low precision models have been shown to deliver close to SOTA accuracy in FP32 (with <1% loss) for ResNet-50, ResNet-101, GoogLeNet v3, Alexnet, VGG-A, DC-GAN, GNMT. Intel Altera (FPGA) has shown interest to adopt TRN in their future product. As a member of Intel Numerics Workgroup showcased the effectiveness of BFLOAT16 datatype which eventually led to the adoption of this datatype across various silicon products not only in Intel but by competition as well such as, Nvidia, AMD, Google.
- **DNN Framework Extension:** Implemented the layers – deconvolution, dilated convolution, different variants of unpooling, temporal and spatial sparsity – in our in-house PCL-DNN framework; code for some of these layers is used in publicly available Intel Caffe framework. Trained Winner-Take-All autoencoder to SOTA accuracy using this code. Designed wrappers for supporting LIBXSMM LSTM cell in TensorFlow which was used to scale Google's Neural Machine Translation (GNMT) workload on Intel CPU cluster for the first time.

2009–2012 **Sponsored Research and Industrial Consultancy**, *Indian Institute of Technology Kharagpur.*

Designation: Senior Research Fellow

Project Title: Extending the scope of equivalence checking in complex embedded system design verification

Sponsor: Department of Science and Technology, Govt. of India

Description: Developed new and efficient verification methodologies to validate various code optimization and parallelizing transformations; emphasis is given on both publication in reputed journals/conferences and robust coding. The software tools developed by us comprise more than 30K lines of code which involve automated interaction with third-party tools, such as Integer Set Library and SMT solvers; code, binaries and benchmarks for some of these tools can be downloaded from `https://github.com/kunalbanerjee`.

2008–2009 **Tata Consultancy Services Ltd.**

Designation: Assistant System Engineer

Project Title: Database management for McGraw-Hill Education

Description: Data accumulation followed by application of data compaction techniques and finally storing the compact data in Oracle database.

Awards/Achievements

2023 AV Luminary Award (Top 10 Data Scientists) from Analytics Vidhya

2022 Emerging Leaders in Data & Analytics award at Data World Summit

2022 Received Impact Driver, Energizer and Collaborator badges from colleagues at Walmart
2021 Nominated for Best Poster Award in the conference DeLTA 2021
2020 Elevated to IEEE Senior Member
2019 Gordy Award (Intel Labs' highest award) for "BFLOAT-16 impact across Intel roadmap"
2019 Invited paper in the journal Supercomputing Frontiers and Innovations
2019 Best Research Poster Award in "Artificial Intelligence and Machine Learning" track in the conference ISC 2019
2018 Divisional Recognition Award from Intel
2018 Techno Inventor Award (PhD) 2017 from India Electronics & Semiconductor Association (IESA)
2018 Best PhD Thesis Award at VLSI Design 2018
2017 Invited to present our TSE 2017 paper at Foundations of Software Engineering 2017
2015 Best PhD Forum Paper Award in the conference ISVLSI 2015
2013 Best Paper Award in the conference I-CARE 2013
2012 TCS Research Fellowship

Patents

1 Saptarshi Misra, Anirban Chatterjee, Pranay Dugar, **Kunal Banerjee**, Lalitdutt Parsai.
System and Method for Enhancing Text in Images based on Super-Resolution. *(US Patent Record No. 81462813, 2022)*.

2 Anirban Chatterjee, **Kunal Banerjee**, Binay Gupta, Lalitdutt Parsai, Geet Vudata.
System and Method for Automatically Assessing Change Requests. *(US Patent Record No. 81461389, 2022)*.

Selected Publications

Journals

1 **Kunal Banerjee**, Evangelos Georganas, Dhiraj D. Kalamkar, Barukh Ziv, Eden Segal, Cristina Anderson, Alexander Heinecke.
Optimizing Deep Learning RNN Topologies on Intel Architecture.
Supercomputing Frontiers and Innovations, vol. 6, no. 3, 2019, pages: 64–85, **invited paper**.

2 Ramanuj Chouksey, Chandan Karfa, **Kunal Banerjee**, Pankaj Kalita, Purandar Bhaduri.
A Counter-Example Generation Procedure for Path based Equivalence Checkers.
IET Software, vol. 13, no. 4, 2019, pages: 280–285.

3 **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Deriving Bisimulation Relations from Path Extension Based Equivalence Checkers.
IEEE Transactions on Software Engineering (TSE), vol. 43, no. 10, 2017, pages: 946–953.

4 **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Deriving Bisimulation Relations from Path Based Equivalence Checkers.
Formal Aspects of Computing (FAC), vol. 29, no. 2, 2017, pages: 365–379.

5 Soumyadip Bandyopadhyay, Dipankar Sarkar, Chittaranjan Mandal, **Kunal Banerjee**, Krishnam Raju Duddu.
A Path Construction Algorithm for Translation Validation using PRES+ Models.
Parallel Processing Letters (PPL), vol. 26, no. 2, 2016, pages: 1–25.

6 **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Extending the FSMD Framework for Validating Code Motions of Array-Handling Programs.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 33, no. 12, 2014, pages: 2015–2019.

7 **Kunal Banerjee**, Chandan Karfa, Dipankar Sarkar, Chittaranjan Mandal.
Verification of Code Motion Techniques using Value Propagation.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 33, no. 8, 2014, pages: 1180–1193.

8 Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Verification of Loop and Arithmetic Transformations of Array-Intensive Behaviours.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 32, no. 11, 2013, pages: 1787–1800.

Conferences / Workshops

1 Soumik Dasgupta, Anurag Wagh, Lalitdutt Parsai, Binay Gupta, Geet Vudata, Shally Sangal, Sohom Majumdar, Hema Rajesh, **Kunal Banerjee**, Anirban Chatterjee.
waLLMartCache: A Distributed, Multi-Tenant and Enhanced Semantic Caching System for LLMs.
International Conference on Pattern Recognition (ICPR), Kolkata, India, 2024, (accepted).

2 Saptarshi Misra, **Kunal Banerjee**, Anirban Chatterjee.
BARGAIN: A Super-Resolution Technique to Gain High-Resolution Images for Barcodes.
International Conference on Data Science & Management of Data (CODS-COMAD), Bangalore, India, 2024, pages: 464–468.

3 Binay Gupta, Saptarshi Misra, Anirban Chatterjee, **Kunal Banerjee**.
Are you a Foodie looking for New Cookies to try out? Better not ask an LLM.
AIMLSystems, Bangalore, India, 2023, pages: 40:1–40:4.

4 Archit Bansal, **Kunal Banerjee**, Abhijnan Chakraborty.
These Deals Won't Last! Longevity, Uniformity and Bias in Product Badge Assignment in E-Commerce Platforms.
SIGIR Workshop On eCommerce (eCOM), Taipei, Taiwan, 2023, pages: 1–17.

5 Saptarshi Misra, Pranay Dugar, Anirban Chatterjee, Lalitdutt Parsai, **Kunal Banerjee**.
Designing a Vision Transformer based Enhanced Text Extractor from Product Images.
International Conference on Data Science & Management of Data (CODS-COMAD), Mumbai, India, 2023, pages: 208–212.

6 Meet Maheshwari, Binay Gupta, Anirban Chatterjee, **Kunal Banerjee**.
A Dynamic Attention Based Graph Neural Network for Anomaly Prediction in Multi-Variate Time-Series & Its Application in Network Monitoring.
International Conference on Data Science & Management of Data (CODS-COMAD), Mumbai, India, 2023, pages: 233–237.

7 Subhadip Paul, Anirban Chatterjee, Binay Gupta, **Kunal Banerjee**.
Developing a Noise-Aware AI System for Change Risk Assessment with Minimal Human Intervention.
CIKM Workshop on Human-in-the-Loop Data Curation (HIL-DC), Atlanta, USA, 2022, pages: 1–5.

8 Rahul Bajaj, **Kunal Banerjee**, Lalitdutt Parsai, Deepansh Goyal, Sachin Parmar, Divyajyothi Bn, Balamurugan Subramaniam, Chaitanya Sai, Tarun Balotia, Anirban Chatterjee, Kailash Sati.
WALTS: Walmart AutoML Libraries, Tools and Services.
Euromicro Conference on Software Engineering and Advanced Applications (SEAA), Gran Canaria, Spain, 2022, pages: 21–28.

9 Pranay Dugar, Aditya Vikram, Anirban Chatterjee, **Kunal Banerjee**, Vijay Agneeswaran.
Don't Miss the Fine Print! An Enhanced Framework To Extract Text From Low Resolution Images.
International Conference on Computer Vision Theory and Applications (VISAPP), Online, 2022, pages: 664–671.

10 Binay Gupta, Anirban Chatterjee, Subhadip Paul, Matha Harika, Lalitdutt Parsai, **Kunal Banerjee**, Vijay Agneeswaran.
Look Before You Leap! Designing a Human-Centered AI System for Change Risk Assessment.
International Conference on Agents and Artificial Intelligence (ICAART), Online, 2022, pages: 655–662.

11 Arkadip Basu, Rishi Singh, Chenyang Yu, Amarjeet Prasad, **Kunal Banerjee**.
Designing, Developing and Deploying an Enterprise Scale Network Monitoring System.
Innovations in Software Engineering Conference (ISEC), Gandhinagar, India, 2022, pages: 18:1–18:5.

13 **Kunal Banerjee**, Vishak Prasad C, Rishi Raj Gupta, Karthik Vyas, Anushree H, Biswajit Mishra.
Exploring Alternatives to Softmax Function.
Deep Learning Theory and Applications (DeLTA), Online, 2021, pages: 81–86,
(nominated for Best Poster Award).

14 Arkadip Basu, **Kunal Banerjee**.
Designing a Bot for Efficient Distribution of Service Requests.
Bots in Software Engineering (BotSE), Madrid, Spain, 2021, pages: 16–20.

15 Evangelos Georganas, **Kunal Banerjee**, Dhiraj Kalamkar, Sasikanth Avancha, Anand Venkat, Michael Anderson, Greg Henry, Hans Pabst, Alexander Heinecke.
Harnessing Deep Learning via a Single Building Block.
International Parallel & Distributed Processing Symposium (IPDPS), New Orleans, USA, 2020, pages: 222–233.
(Preliminary version accepted as research poster in SuperComputing 2019.)

16 Brunno F Goldstein, Sudarshan Srinivasan, Dipankar Das, **Kunal Banerjee**, Leandro Santiago, Victor C. Ferreira, Alexandre S. Nery, Sandip Kundu, Felipe M. G. Franca.
Reliability Evaluation of Compressed Deep Learning Models.
Latin American Symposium on Circuits and Systems (LASCAS), San Jose, Costa Rica, 2020, pages: 1–5.

17 Dhiraj Kalamkar, **Kunal Banerjee**, Sudarshan Srinivasan, Srinivas Sridharan, Evangelos Georganas, Mikhail E. Smorkalov, Cong Xu, Alexander Heinecke.
Training Google Neural Machine Translation on an Intel CPU Cluster.
International Conference on Cluster Computing (CLUSTER), Albuquerque, USA, 2019, pages: 1–10.

18 Evangelos Georganas, Sasikanth Avancha, **Kunal Banerjee**, Dhiraj Kalamkar, Greg Henry, Hans Pabst, Alexander Heinecke.
Anatomy Of High-Performance Deep Learning Convolutions On SIMD Architectures.
International Conference for High Performance Computing, Networking, Storage, and Analysis (SC), Dallas, USA, 2018, pages: 66:1–66:12.

19 **Kunal Banerjee**, Ramanuj Chouksey, Chandan Karfa, Pankaj Kumar Kalita.ewline Poster: Automatic Detection of Inverse Operations while Avoiding Loop Unrolling.
International Conference on Software Engineering (ICSE), Gothenburg, Sweden, 2018, pages: 175–176.

20 Dipankar Das, Naveen Mellempudi, Dheevatsa Mudigere, Dhiraj Kalamkar, Sasikanth Avancha, **Kunal Banerjee**, Srinivas Sridharan, Karthik Vaidyanathan, Bharat Kaul, Evangelos Georganas, Alexander Heinecke, Pradeep Dubey, Jesus Corbal, Nikita Shustrov, Roma Dubtsov, Evarist Fomenko, Vadim Pirogov.
Mixed Precision Training of Convolutional Neural Networks using Integer Operations.
International Conference on Learning Representations (ICLR), Vancouver, Canada, 2018, pages: 1–11.

21 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.
An Equivalence Checking Framework for Array-Intensive Programs.
Automated Technology for Verification and Analysis (ATVA), Pune, India, 2017, pages: 84–90.

22 Soumyadip Bandyopadhyay, Santonu Sarkar, **Kunal Banerjee**.
An End-to-end Formal Verifier for Parallel Programs.
International Conference on Software Technologies (ICSOFT), Madrid, Spain, 2017, pages: 388–393.

23 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.
Translation Validation of Loop and Arithmetic Transformations in the Presence of Recurrences.
ACM SIGPLAN/SIGBED Conference on Languages, Compilers, Tools and Theory for Embedded Systems (LCTES), Santa Barbara, USA, 2016, pages: 31–40.

24 **Kunal Banerjee**, Soumyadip Banerjee, Santonu Sarkar.
Data-Race Detection: The Missing Piece for an End-to-End Semantic Equivalence Checker for Parallelizing Transformations of Array-Intensive Programs.
International Workshop on Libraries, Languages and Compilers for Array Programming (ARRAY), Santa Barbara, USA, 2016, pages: 1–8.

25 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.
A Translation Validation Framework for Symbolic Value Propagation Based Equivalence Checking of FSMDAs.
Source Code Analysis and Manipulation (SCAM), Bremen, Germany, 2015, pages: 247–252.

26 Soumyadip Bandyopadhyay, Dipankar Sarkar, **Kunal Banerjee**, Chittaranjan Mandal.
A Path-Based Equivalence Checking Method for Petri net based Models of Programs.
International Conference on Software Engineering and Applications (ICSOFT-EA), Colmar, France, 2015, pages: 319–329.

27 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.
Translation Validation of Transformations of Embedded System Specifications using Equivalence Checking.
IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Montpellier, France, 2015, pages: 183–186, **(received Best PhD Forum Paper Award)**.

28 Partha De, **Kunal Banerjee**, Chittaranjan Mandal, Debdeep Mukhopadhyay.
Circuits and Synthesis Mechanism for Hardware Design to Counter Power Analysis Attacks.
Euromicro Conference on Digital System Design (DSD), Verona, Italy, 2014, pages: 520–527.

29 **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.
5Extending the Scope of Translation Validation by Augmenting Path Based Equivalence Checkers with SMT Solvers.
International Symposium on VLSI Design and Test (VDAT), Coimbatore, India, 2014, pages: 1–6.

30 Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Experimentation with SMT Solvers and Theorem Provers for Verification of Loop and Arithmetic Transformations.
IBM Collaborative Academia Research Exchange (I-CARE), Delhi, India, 2013, pages: 3:1–3:4, **(received Best Paper Award)**.

31 Partha De, **Kunal Banerjee**, Chittaranjan Mandal, Debdeep Mukhopadhyay.
Designing DPA Resistant Circuits Using BDD Architecture and Bottom Pre-charge Logic.
Euromicro Conference on Digital System Design (DSD), Santander, Spain, 2013, pages: 641–644.

32 **Kunal Banerjee**, Chandan Karfa, Dipankar Sarkar, Chittaranjan Mandal.
A Value Propagation Based Equivalence Checking Method for Verification of Code Motion Techniques.
International Symposium on Electronic System Design (ISED), Kolkata, India, 2012, pages: 67–71.

33 Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.
Equivalence Checking of Array-Intensive Programs.
IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Chennai, India, 2011, pages: 156–161.

Others

1 Vishwas Choudhary, Binay Gupta, Anirban Chatterjee, Subhadip Paul, **Kunal Banerjee**, Vijay Srinivas Agneeswaran.
Detecting Concept Drift in the Presence of Sparsity - A Case Study of Automated Change Risk Assessment System.
Engineering Dependable and Secure Machine Learning Systems (EDSMLS)@AAAI, Online, 2022.

2 Abhisek Kundu, Sudarshan Srinivasan, Eric C. Qin, Dhiraj Kalamkar, Naveen K. Mellempudi, Dipankar Das, **Kunal Banerjee**, Bharat Kaul, Pradeep Dubey.
K-TanH: Hardware Efficient Activations For Deep Learning.
arXiv:1909.07729, pages: 1–11.

3 Dhiraj Kalamkar, Dheevatsa Mudigere, Naveen Mellempudi, Dipankar Das, **Kunal Banerjee**, Sasikanth Avancha, Dharma Teja Vooturi, Nataraj Jammalamadaka, Jianyu Huang, Hector Yuen, Jiyan Yang, Jongsoo Park, Alexander Heinecke, Evangelos Georganas, Sudarshan Srinivasan, Abhisek Kundu, Misha Smelyanskiy, Bharat Kaul, Pradeep Dubey.
A Study of BFLOAT16 for Deep Learning Training.
arXiv:1905.12322, pages: 1–10.

4 **Kunal Banerjee**, Chandan Karfa.
A Quick Introduction to Functional Verification of Array-Intensive Programs.
arXiv:1905.09137, pages: 1–7.

5 **Kunal Banerjee**, Evangelos Georganas, Dhiraj Kalamkar, Alexander Heinecke.
Optimizing Deep Learning LSTM Topologies on Intel Xeon Architecture.
ISC High Performance, Frankfurt, Germany, 2019, pages: 1, **(received Best Research Poster Award in "Artificial Intelligence and Machine Learning" track)**.

6 Alexander Heinecke, Evangelos Georganas, **Kunal Banerjee**, Dhiraj Kalamkar, Narayanan Sundaram, Anand Venkat, Greg Henry, Hans Pabst.
Understanding the Performance of Small Convolution Operations for CNN on Intel Architecture.
International Conference for High Performance Computing, Networking, Storage and Analysis (SC), Denver, USA, 2017, (Research Poster).

7 Abhisek Kundu, **Kunal Banerjee**, Naveen Mellempudi, Dheevatsa Mudigere, Dipankar Das, Bharat Kaul, Pradeep Dubey.
Ternary Residual Networks.
arXiv:1707.04679, pages: 1–19.
(Accepted as extended abstract in SysML 2018. Presented at Intel AI DevCon 2018.)

8 **Kunal Banerjee**.
An Equivalence Checking Mechanism for Handling Recurrences in Array-Intensive Programs.
Principles of Programming Languages (POPL): Student Research Competition, Mumbai, India, 2015, pages: 1–2.

Professional Memberships

IEEE Senior Member

ACM Senior Member

Tutorials / Talks

1 Compiler-agnostic Translation Validation, *Innovations in Software Engineering Conference (ISEC)*, Hyderabad, India, 2018.

2 Translation Validation of Embedded System Specifications using Equivalence Checking, *Tata Research Development and Design Centre (TRDDC)*, Pune, India, 2014.

3 Translation Validation using Path Based Equivalence Checkers Augmented with SMT Solvers, *Formal Methods Update Meeting 2014*, Kharagpur, India, 2014.

Technical Skills

Programming: C, C++, Java, Python, PL/SQL, Scheme, Prolog, Lisp, Visual Basic and others along with some scripting and markup languages

Tools: ACL2, Caffe, CUDD, CVC, ISL, PyTorch, TensorFlow, Yices, Z3

Languages: Bengali, English, Hindi

References

Available on request.