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**Project (CSE 490/590 – Summer 2023)**

Assigned Parameters:  
**456.hmmer**

***L1 data cache size,  
 L1 instruction cache size,***

***L1 data associativity,***

***L2 associativity,***

***Block Size***

1. Baseline Command: csh gemTest.csh 456.hmmer baseline **1kB 1kB** 1kB **1** 1 **1 16**

csh gemTest.csh <benchmark name> <output name> **<L1D size>** **<L1I size>** <L2 size> **<L1D assoc>** <L1I assoc> **<L2 assoc>** **<Block Size>**

**Parameter Varied: *L1 data cache size <L1D size*>**

Baseline Command: csh gemTest.csh 456.hmmer baseline **1kB** 1kB 1kB 1 1 1 16

1. csh gemTest.csh 456.hmmer L1D\_size\_2kB **2kB** 1kB 1kB 1 1 1 16
2. csh gemTest.csh 456.hmmer L1D\_size\_4kB **4kB** 1kB 1kB 1 1 1 16
3. csh gemTest.csh 456.hmmer L1D\_size\_8kB **8kB** 1kB 1kB 1 1 1 16
4. csh gemTest.csh 456.hmmer L1D\_size\_16kB **16kB** 1kB 1kB 1 1 1 16

**Parameter Varied: *L1 instruction cache size <L1I size*>**

Baseline Command: csh gemTest.csh 456.hmmer baseline 1kB **1kB** 1kB 1 1 1 16

1. csh gemTest.csh 456.hmmer L1I\_size\_2kB 1kB **2kB** 1kB 1 1 1 16
2. csh gemTest.csh 456.hmmer L1I\_size\_4kB 1kB **4kB** 1kB 1 1 1 16
3. csh gemTest.csh 456.hmmer L1I\_size\_8kB 1kB **8kB** 1kB 1 1 1 16
4. csh gemTest.csh 456.hmmer L1I\_size\_16kB 1kB **16kB** 1kB 1 1 1 16

**Parameter Varied: *L1 data associativity <L1D assoc>***

Baseline Command: csh gemTest.csh 456.hmmer baseline 1kB 1kB 1kB **1** 1 1 16

1. csh gemTest.csh 456.hmmer L1D\_assoc\_2 1kB 1kB 1kB **2** 1 1 16
2. csh gemTest.csh 456.hmmer L1D\_assoc\_4 1kB 1kB 1kB **4** 1 1 16
3. csh gemTest.csh 456.hmmer L1D\_assoc\_8 1kB 1kB 1kB **8** 1 1 16
4. csh gemTest.csh 456.hmmer L1D\_assoc\_16 1kB 1kB 1kB **16** 1 1 16

**Parameter Varied: *L2 associativity <L2 assoc>***

Baseline Command: csh gemTest.csh 456.hmmer baseline 1kB 1kB 1kB 1 1 **1** 16

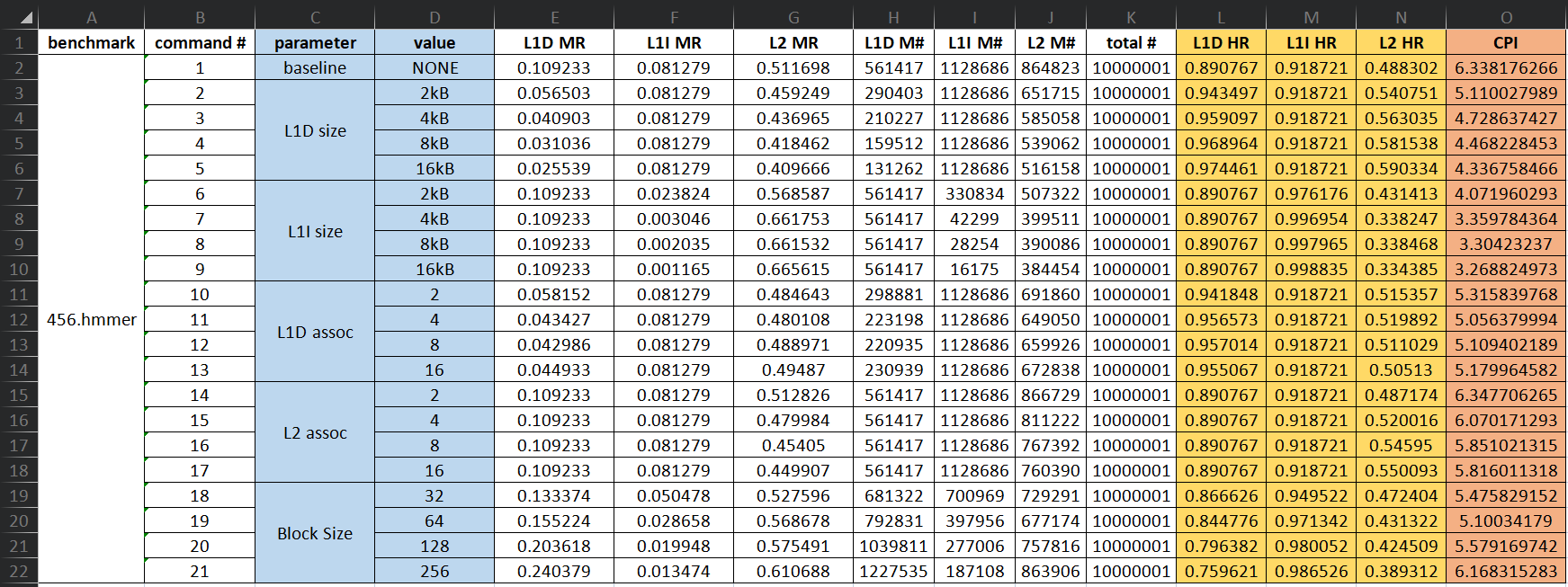
1. csh gemTest.csh 456.hmmer L2\_assoc\_2 1kB 1kB 1kB 1 1 **2** 16
2. csh gemTest.csh 456.hmmer L2\_assoc\_4 1kB 1kB 1kB 1 1 **4** 16
3. csh gemTest.csh 456.hmmer L2\_assoc\_8 1kB 1kB 1kB 1 1 **8** 16
4. csh gemTest.csh 456.hmmer L2\_assoc\_16 1kB 1kB 1kB 1 1 **16** 16

**Parameter Varied: *Block Size <Block Size>***

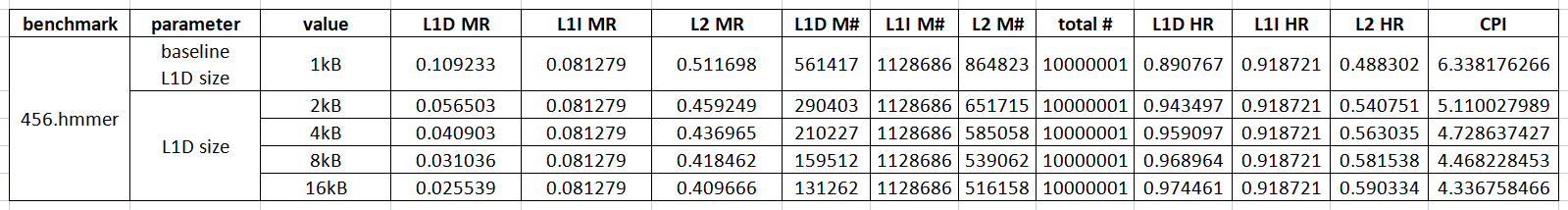
Baseline Command: csh gemTest.csh 456.hmmer baseline 1kB 1kB 1kB 1 1 1 **16**

1. csh gemTest.csh 456.hmmer Block\_Size\_32 1kB 1kB 1kB 1 1 1 **32**
2. csh gemTest.csh 456.hmmer Block\_Size\_64 1kB 1kB 1kB 1 1 1 **64**
3. csh gemTest.csh 456.hmmer Block\_Size\_128 1kB 1kB 1kB 1 1 1 **128**
4. csh gemTest.csh 456.hmmer Block\_Size\_256 1kB 1kB 1kB 1 1 1 **256**

Following is the tabular result for all the executions:



**L1 data cache size <L1D size>:**



Explanation (Observation):

We can be observe that as the L1 data cache size increases, the CPI (cycles per instruction) decreases. This implies that larger L1 data cache sizes lead to improved performance.

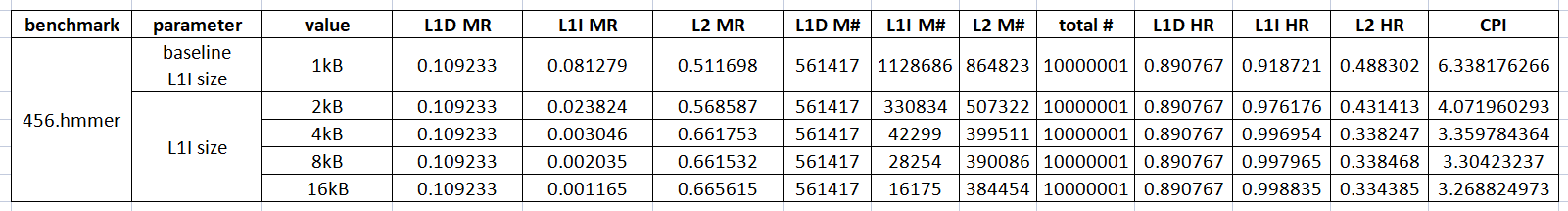
Graphically, when plotting the L1 data cache size (in kilobytes) on the x-axis and the corresponding CPI values on the y-axis, the graph shows a decreasing trend. The graph would start with a higher CPI value at a smaller cache size (1kB) and gradually decrease as the cache size increases (2kB, 4kB, 8kB, and 16kB). The rate of decrease in CPI vary at different points, with larger cache size increments resulting in smaller performance gains.

Explanation (Reasoning):

The CPI (cycles per instruction) decreased as the L1 data cache size increased because the processor was able to find the data it needed more quickly in the larger cache. When the cache size was 1kB, the processor had to access main memory more often, which resulted in a higher CPI. As the cache size increased, the processor was able to find the data it needed more often in the cache, which reduced the number of main memory accesses and resulted in a lower CPI.

The trend is consistent with the principle of locality of reference, which states that data that is accessed recently or frequently is likely to be accessed again in the near future. By increasing the L1 data cache size, the processor was able to store more of the data that was likely to be accessed, which reduced the number of main memory accesses and improved performance.

**L1 instruction cache size <L1I size>:**



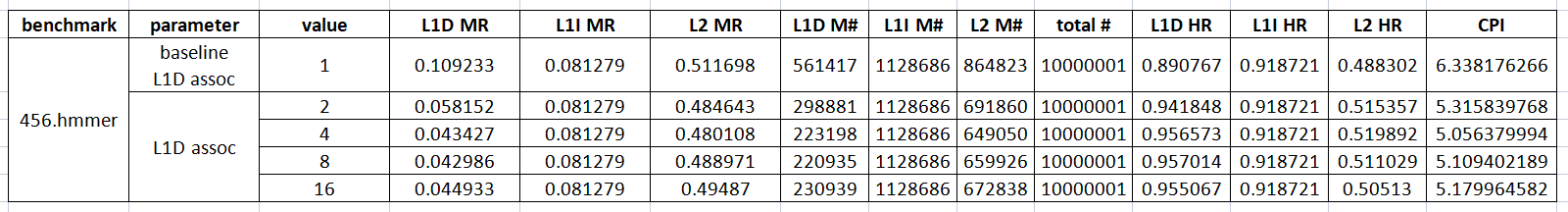
Explanation (Observation):

We can be observe that increasing the L1 instruction cache size leads to a significant improvement in performance, as indicated by the decreasing CPI values.

The graph represents the relationship between L1 instruction cache size (in kilobytes) and CPI exhibits a clear downward trend. As the cache size increases from 1kB to 16kB, the CPI consistently decreases, indicating better performance. The rate of improvement vary at different cache size increments, with larger cache size increases resulting in more significant performance gains initially and diminishing returns at larger cache sizes.

Explanation (Reasoning):  
As the L1 instruction cache size increases, the CPI decreases. This is because the L1 instruction cache is responsible for storing the instructions that the processor is currently executing. A larger L1 instruction cache means more instructions can be stored and hence there is a higher chance that the instruction the processor needs is already in the cache, which can significantly reducing the frequency of instruction cache misses and subsequent stalls in the processor's pipeline. Consequently, the CPI decreases, indicating that instructions are fetched and executed more efficiently, leading to improved overall performance.

**L1 data associativity <L1D assoc>:**



Explanation (Observation):

Changing the L1 data cache associativity has a moderate impact on performance, as indicated by the slight variations in CPI values. Increasing the data cache associativity from 1 to 2 initially leads to a slight improvement in performance, as indicated by the decreased CPI. However, as the associativity further increases to 4, 8, and 16, the CPI values fluctuate within a relatively narrow range without a clear trend of improvement or degradation.

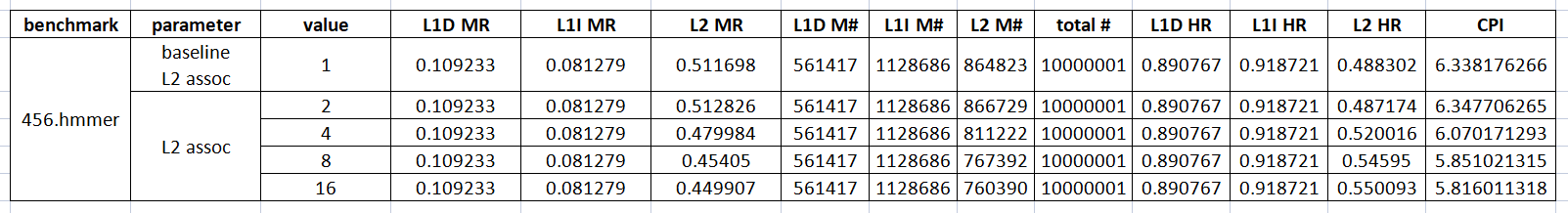
Explanation (Reasoning):

Data associativity refers to the number of cache sets that can store a particular data item. Higher associativity allows for a larger number of cache sets and reduces the likelihood of cache conflicts.

When the L1 data associativity is low, such as 1 or 2, the cache sets are limited, resulting in a higher probability of cache conflicts. Cache conflicts occur when multiple memory blocks compete for the same cache set, leading to evictions and frequent cache misses. As a result, the processor needs to access the main memory more frequently, incurring higher latency and increasing the number of cycles required to complete instructions, thus elevating the CPI.

As the L1 data associativity increases to 4, 8, and 16, the cache sets become more numerous, reducing the likelihood of cache conflicts. With more cache sets available, data blocks have a higher chance of finding a vacant set, leading to fewer evictions and cache misses. Consequently, the processor can access data more efficiently from the cache, reducing memory latency and the number of cycles needed to complete instructions. This results in a decrease in CPI as the L1 data associativity increases.

**L2 associativity <L2 assoc>:**



Explanation (Observation):

We can be observe that changing the L2 cache associativity has a limited impact on performance, as indicated by the slight variations in CPI values.

The graph representing the relationship between L2 cache associativity and CPI shows a relatively flat trend. The CPI values does show minor fluctuations as the associativity increases, but the changes are not significant enough.

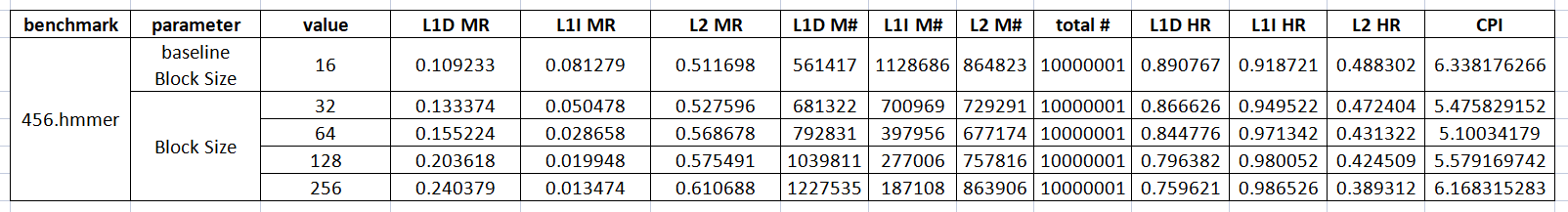
Explanation (Reasoning):

L2 associativity refers to the number of cache lines or blocks that can be mapped to each set in the L2 cache. A higher associativity allows for a larger number of cache lines to be mapped to each set, reducing the likelihood of cache conflicts and improving cache hit rates. As the L2 associativity increases, cache conflicts decrease, resulting in improved cache performance. This, in turn, reduces the number of cycles required to fetch data from the L2 cache, thereby lowering the CPI.

With lower associativity, cache conflicts may occur more frequently, leading to longer access times and increased CPI. The decreasing trend in CPI as L2 associativity increases indicates that the x86 processor benefits from larger and more associative L2 caches, allowing for more efficient data retrieval and improved overall performance.

However, increasing associativity also introduces increased complexity and potential latency in cache access, which might counterbalance the benefits.

**Block Size <Block Size>:**



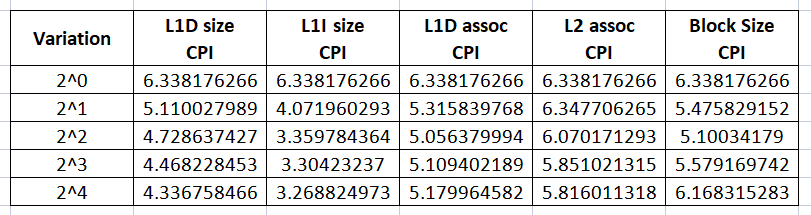
Explanation (Observation):

The trend observed in the CPI values as the block size changes indicate that there is an optimal block size (64) that minimizes cache misses and improves performance. Increasing the block size initially leads to reduced CPI as it allows more data to be fetched at once, reducing cache misses. However, if the block size becomes too large, it can lead to cache conflicts and contention, resulting in increased CPI and degraded performance.

Explanation (Reasoning):

The larger the block size, the less likely it is that a cache miss will occur. This is because a larger block size means that more data is stored in each cache line, which means that there is a smaller chance that the next data access will require a cache miss. As a result, the CPI decreases as the block size increases. However, there is a trade-off to consider. A larger block size also means that more memory is required to store the cache lines. This can lead to a decrease in the overall performance of the system if the memory bandwidth is not sufficient to keep the cache lines filled.

**Comparision:**



Explanation (Observation):

Since the value for each parameter was different, the x-axis consists of relative increment of the respective values. And the y-axis represents the CPI value.  
We can clearly see that modifying the **L1I size** parameter positively affects the CPI a lot more compared to other parameters.

Explanation (Reasoning):

The L1I cache size is a more important factor in CPI than the other parameters. This is because instructions are typically smaller than data, they are accessed more frequently, and the L1I cache is closer to the CPU core. Other parameters have less of an impact on CPI because they do not affect the performance of the CPU as directly as L1I size does.