# Kunal Chandan

University of Waterloo B.A.Sc Honours Electrical & Computer Engineering kchandan@uwaterloo.ca

647-785-1313 linkedin/kunal-chandan

chandan.one github/kunalchandan

#### **Software**

- · KiCAD
- · LTSpice/PySpice
- · Cadence
- LavoutEditor
- · Quartus Prime
- · Linux

#### Languages

- · Python
  - · Numpy
  - · Pandas
  - · Scipy
  - · Sympy
  - · TensorFlow
  - · Pytorch
- · C++
- · SQL
- · Rust
- · nalgebra
- · Rayon
- · MATLAB
- · Go
- · Verilog
- · RISC-V
- · Shell
- · LaTeX

## Lab Skills

- · PCB Design
- · Oscilliscope
- · Network Analyzer
- · Probe Station
- · Wirebonder
- · Diebonder
- · Plasma Cleaner & Asher
- · Dicing saw
- · HMDS Oven
- · Spincoater
- SEM
- · X-Ray Spectroscopy

107.6pt 557.94pt

## **Summary of Qualifications**

- · Multidisciplinary generalist electrical engineering skills specialist in software development at scale in data engineering with **Python** and performance critical development in **C++**
- · Experienced electrical engineering skills with clean-room and hands-on electrical lab-work
- · Strong electrical engineering foundation through coursework in semiconductor device physics, RF devices, computer architecture, control systems, and IC design

#### **Experience**

RESEARCH ELECTRICAL ENGINEER | University of Waterloo

Sept 2022 - Apr 2023 | Waterloo, ON

- $^{\cdot}$  Developed research plan for packaging of  $\mu$ LEDs onto TFT packplanes using indium electroplating
- · Characterized results using SEM and X-Ray Spectroscopy,
- · Simulation

### **Projects**

#### BEAMFORMING HEARING AID PCB @

- · Designed 4 channel microphone array PCB in **KiCAD**, PCB does active analog bandpass filtering, differential amplification, and multichannel **ADC** over **SPI** to Raspberry Pi
- · R-Pi does compression and sends audio over Flask server for further digital filtering and beamforming
- Pytorch to create quantized voice isolation model and minimize latency and maintain performance
- · Used multiprocessing, asyncio, and websockets to maximize throughput and performance

#### PIPELINED RISC-V CORE

- Designed 5-stage pipelined RISC-V 32-bit core in Verilog using only synthesizable constructs
- · Core synthesized on FPGA and successfully ran programs. Testbenches used to ensure cycle accuracy

#### RAY TRACING ENGINE &

- · Implemented 3D recursive path-tracing for arbitrary materials on basic geometric shapes
- · Used nalgebra for arbitrary rotations & positions of camera & objects
- · Parallel processing of ray-tracing using rayon yielding ~10X performance speed-up

### **Education**

UNIVERSITY OF WATERLOO

#### B.A.SC ELECTRICAL & COMPUTER ENGINEERING 23'

- · Electronic devices, Semiconductor physics, Analog/Digital integrated circuits
- · Analog/Digial/Multivariable control systems
- · Radio frequency and microwave circuits

733.84pt 477.72pt