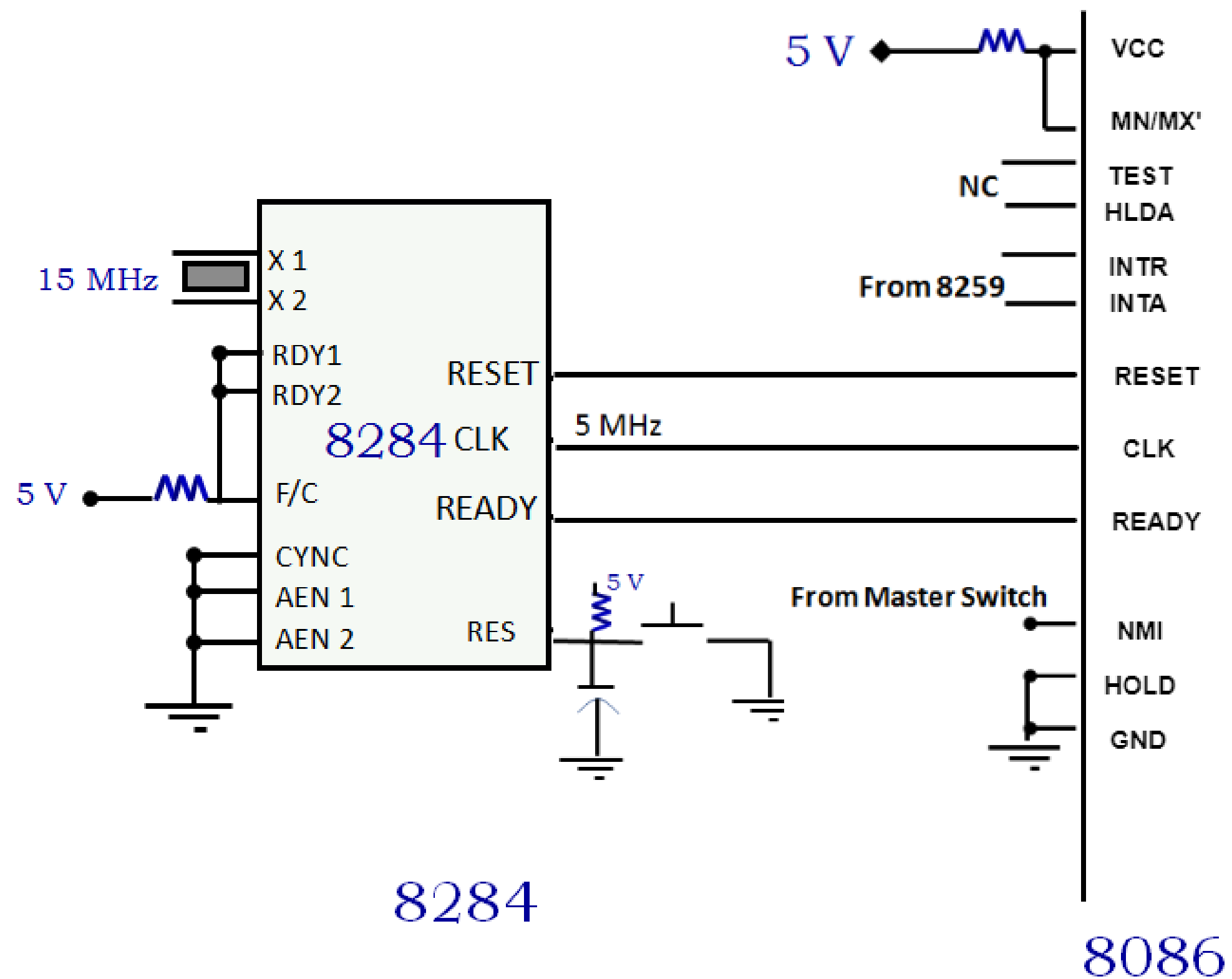


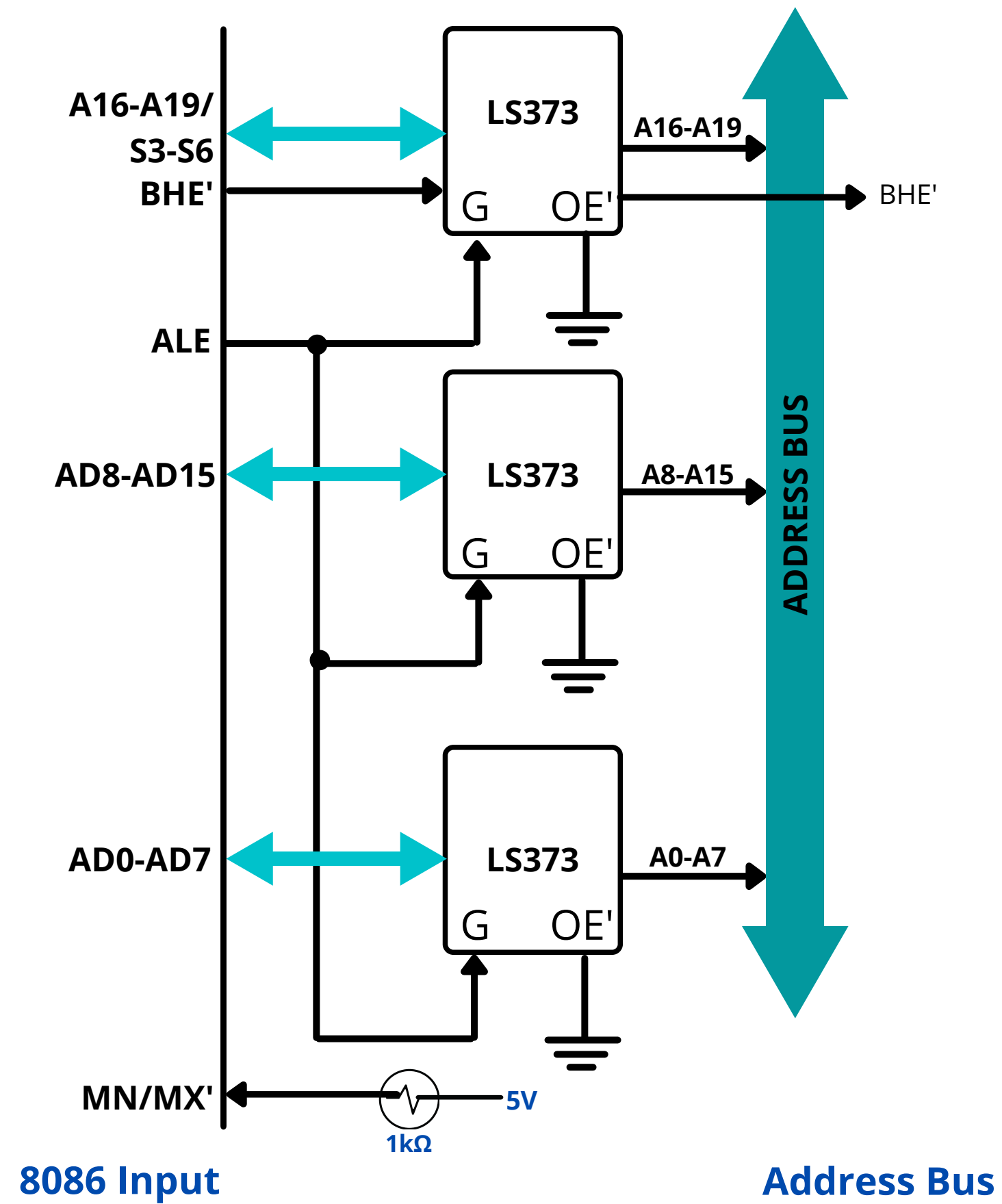
Hardware Diagrams

1. 8284
2. Address Bus
3. Data & Control Bus
4. Logic Circuit for Control Bus Signals
5. 8086
6. LS128 - 1 Memory Decoder
7. Memory Interfacing
8. LS128 - 2 I/O Decoder
9. 8255 - 1
10. 8255 - 2
11. ADC0808 - 1
12. ADC0808 - 2
13. 8254
14. 8254 Counters
15. 8259
16. Relay Mechanism for Valves
17. Conversion Circuit from 4-20mA to 0-5V

8284



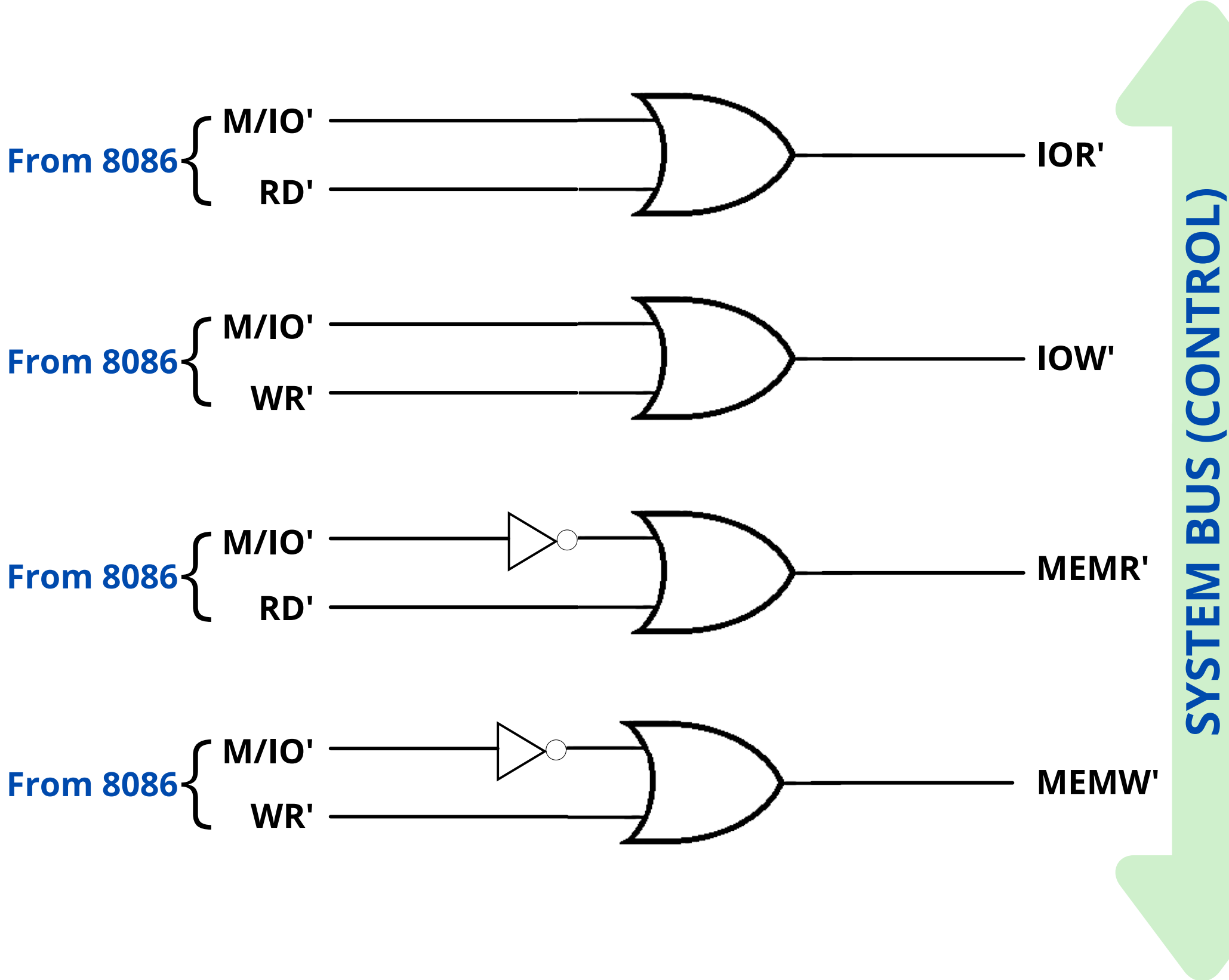
Address Bus Latching



Data & Control Bus Latching

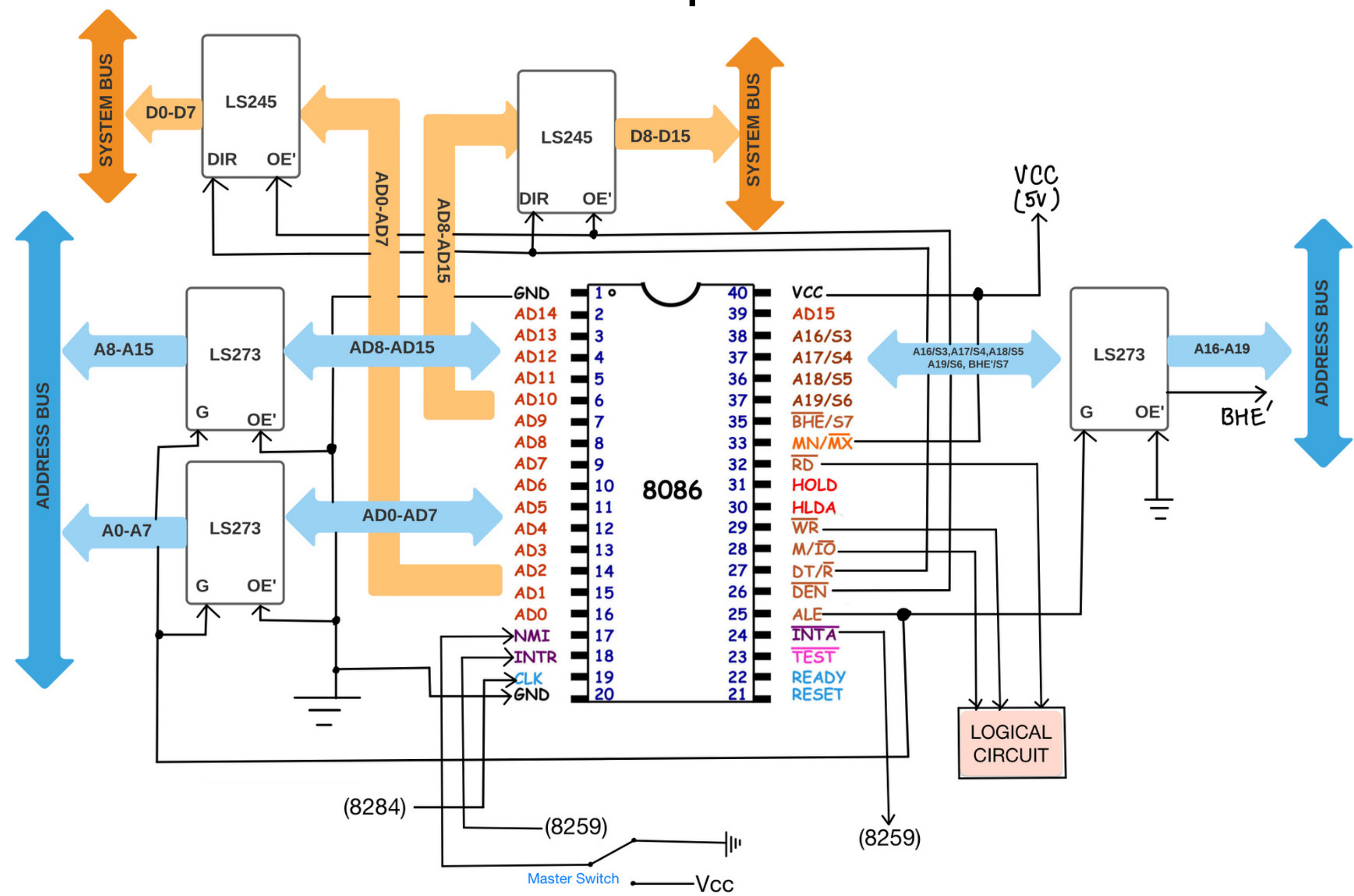


Logic Circuit to get Control Bus Signals

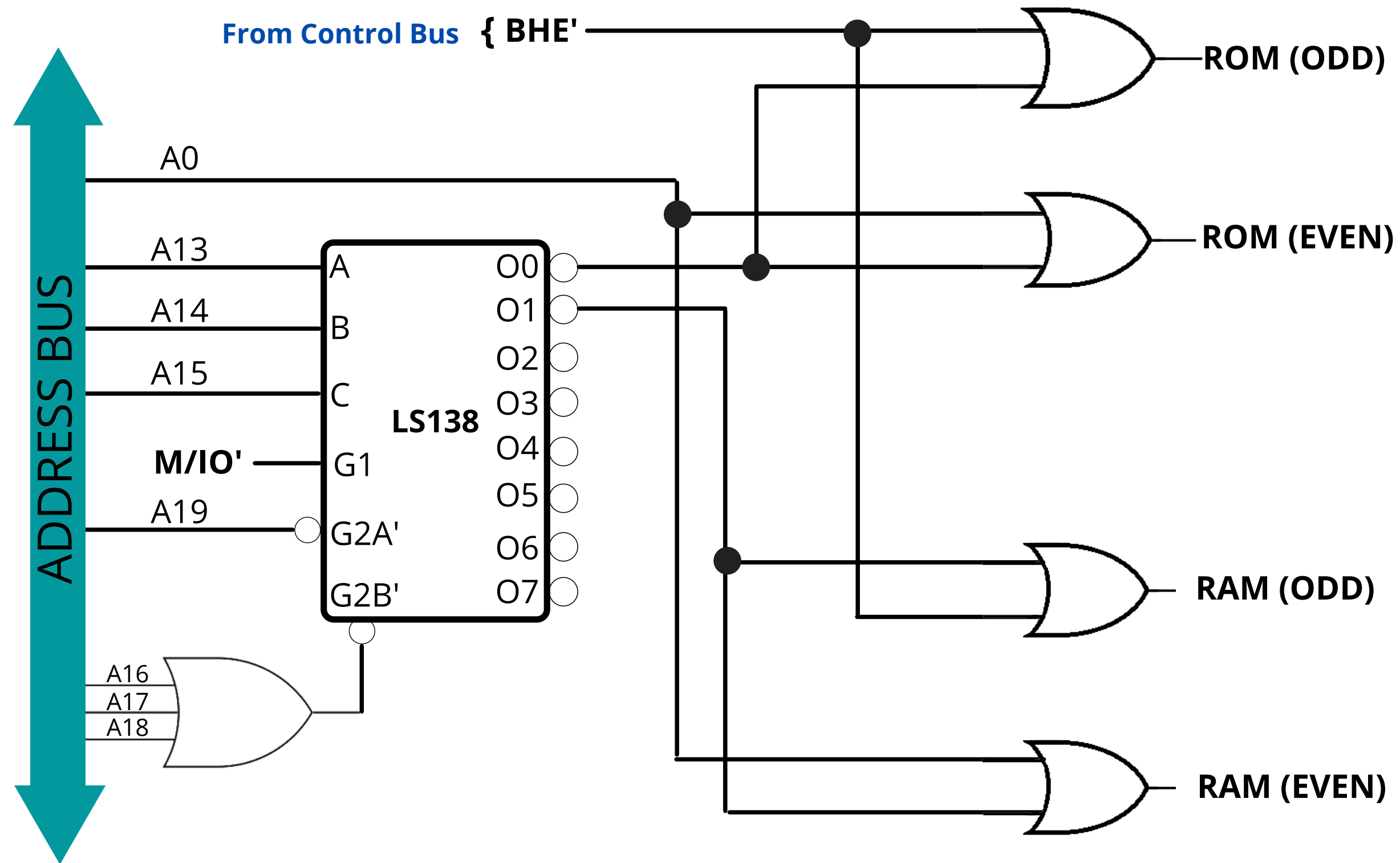


| M/IO' | RD' | WR' | Bus Cycle |
|-------|-----|-----|-----------|
| 1 | 0 | 1 | MEMR' |
| 1 | 1 | 0 | MEMW' |
| 0 | 0 | 1 | IOR' |
| 0 | 1 | 0 | IOW' |

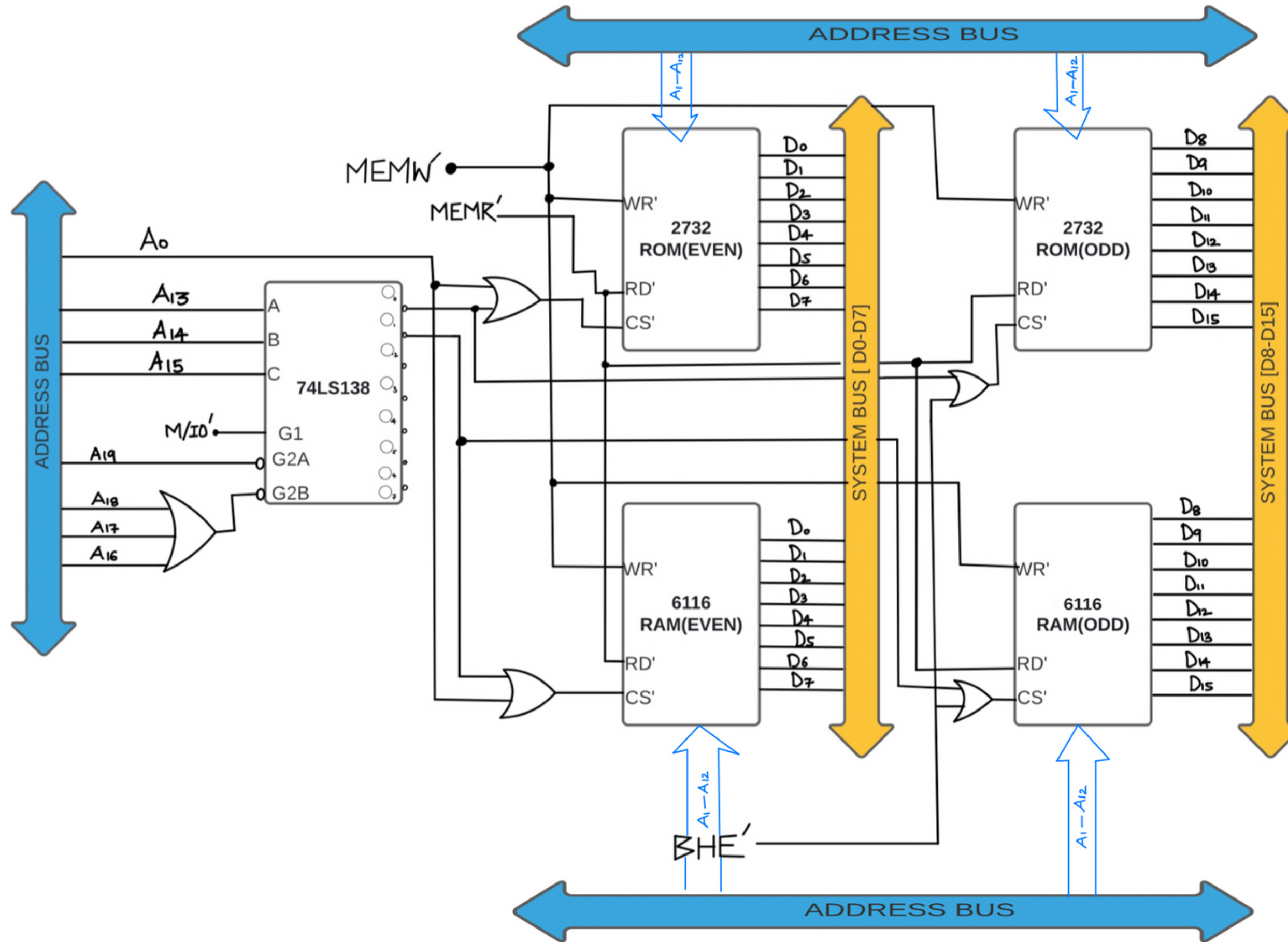
8086 Microprocessor



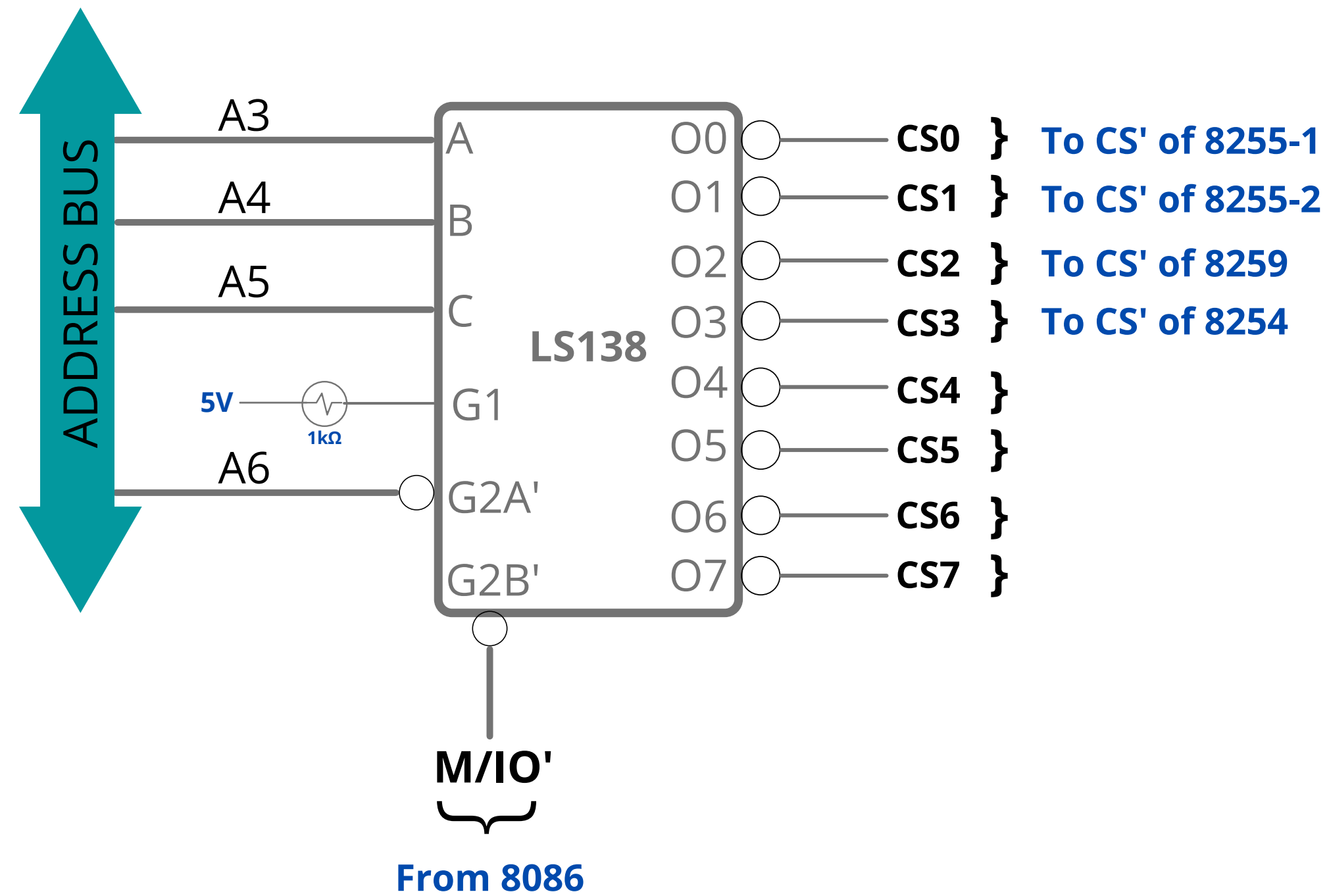
LS138 - 1 : Memory Decoder



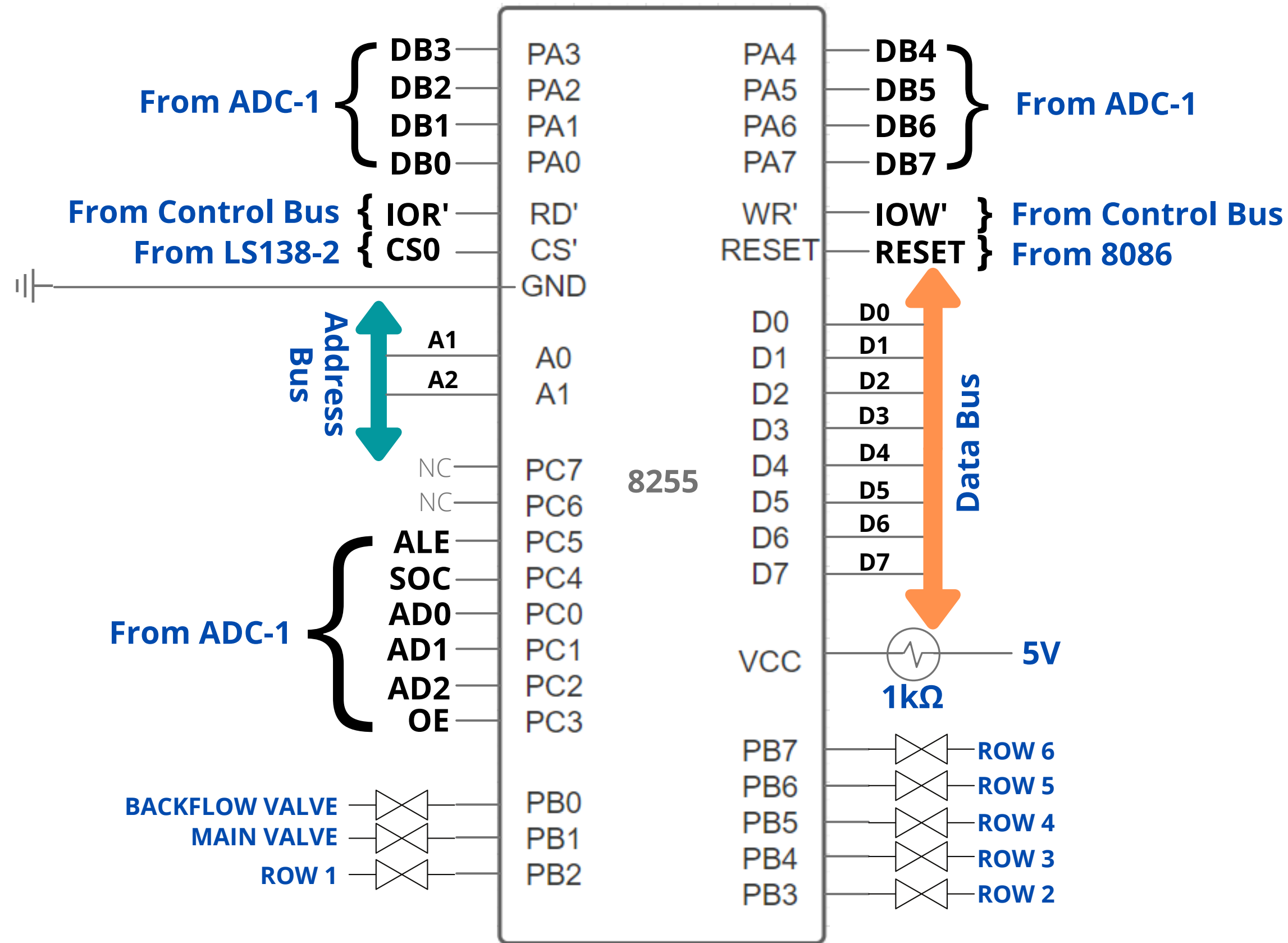
Memory Interfacing



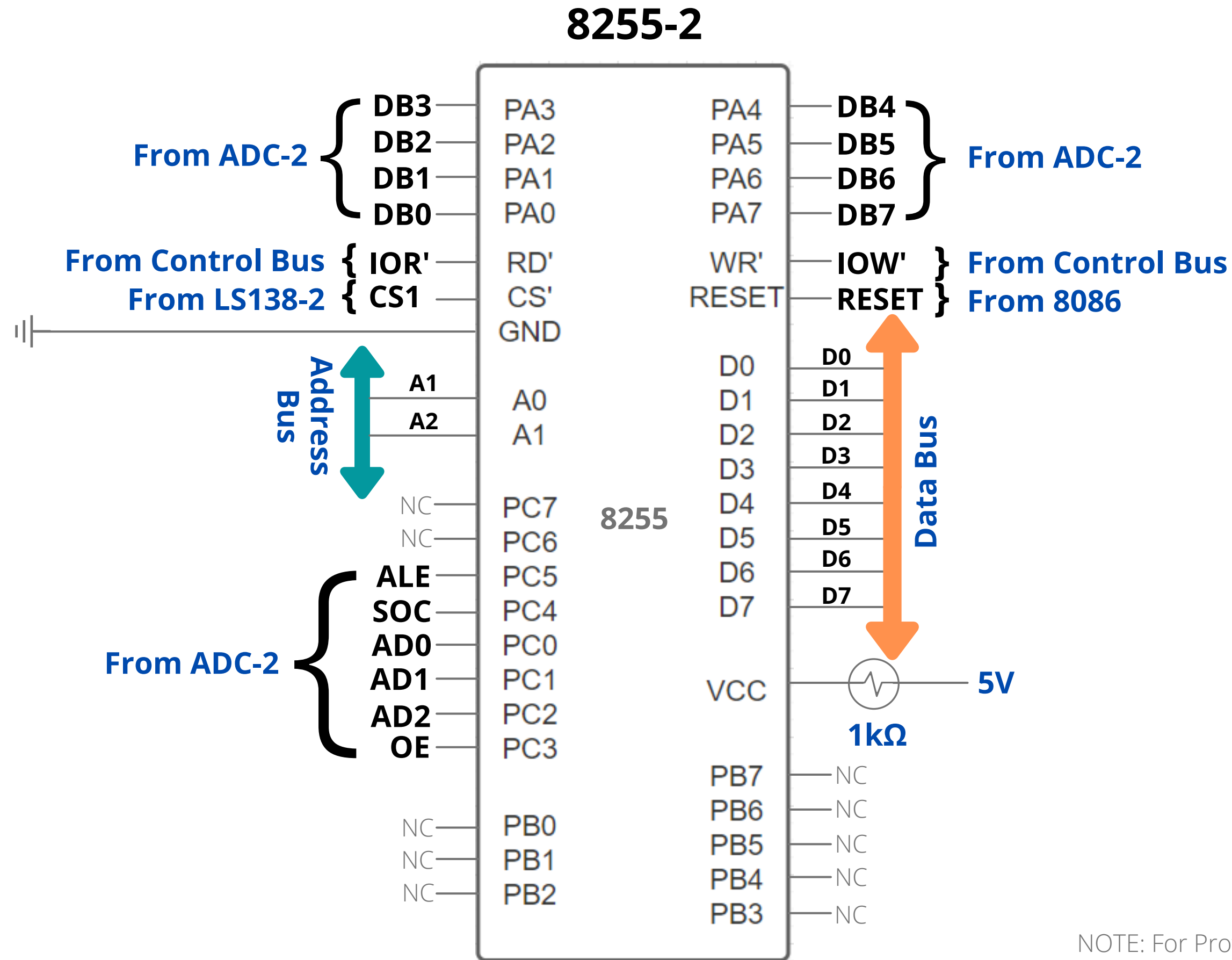
LS138 - 2 : I/O Decoder



8255-1



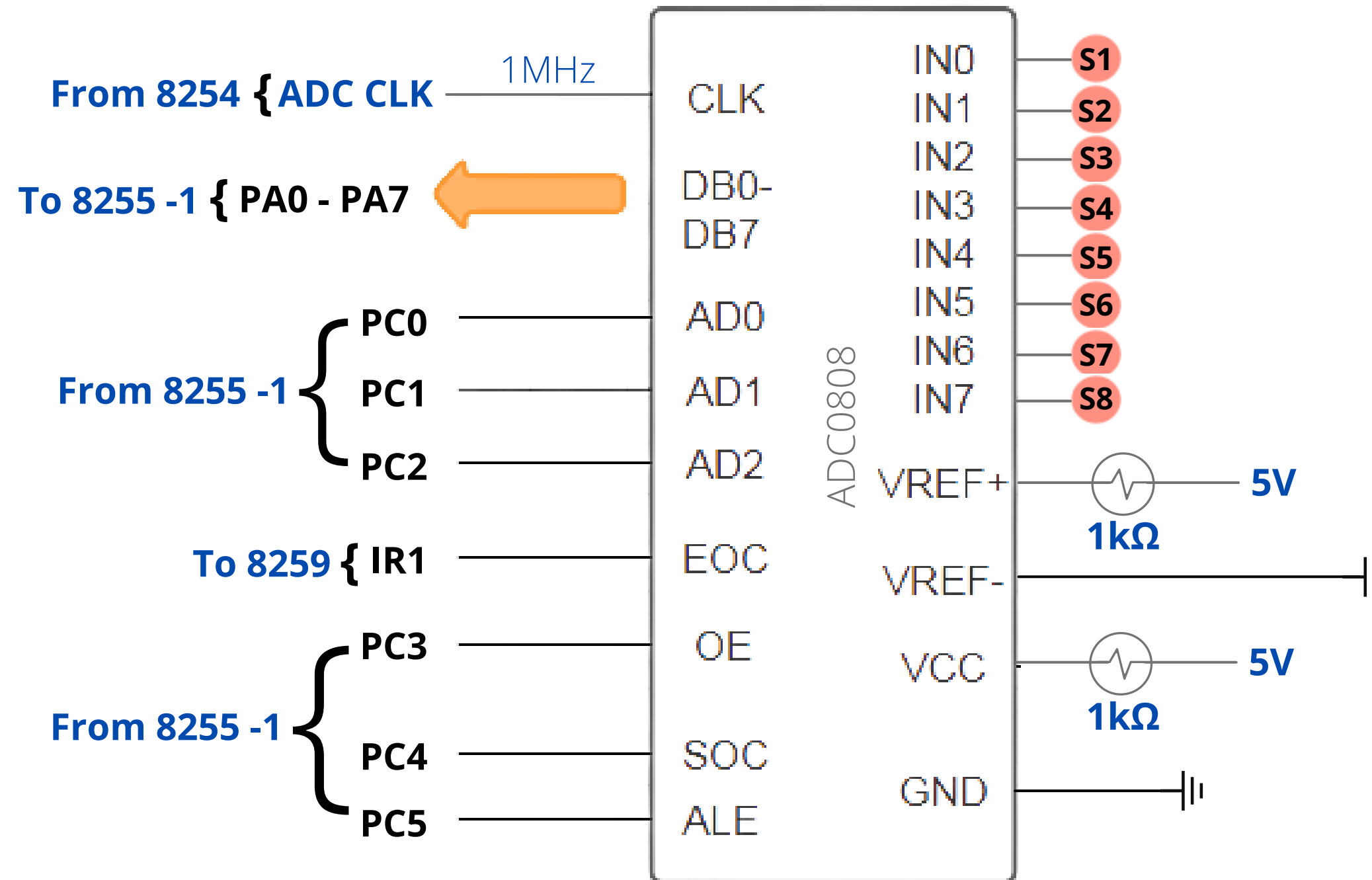
Port A is input
Port B is output
Port C is output



Port A is input
Port B is input
Port C is output

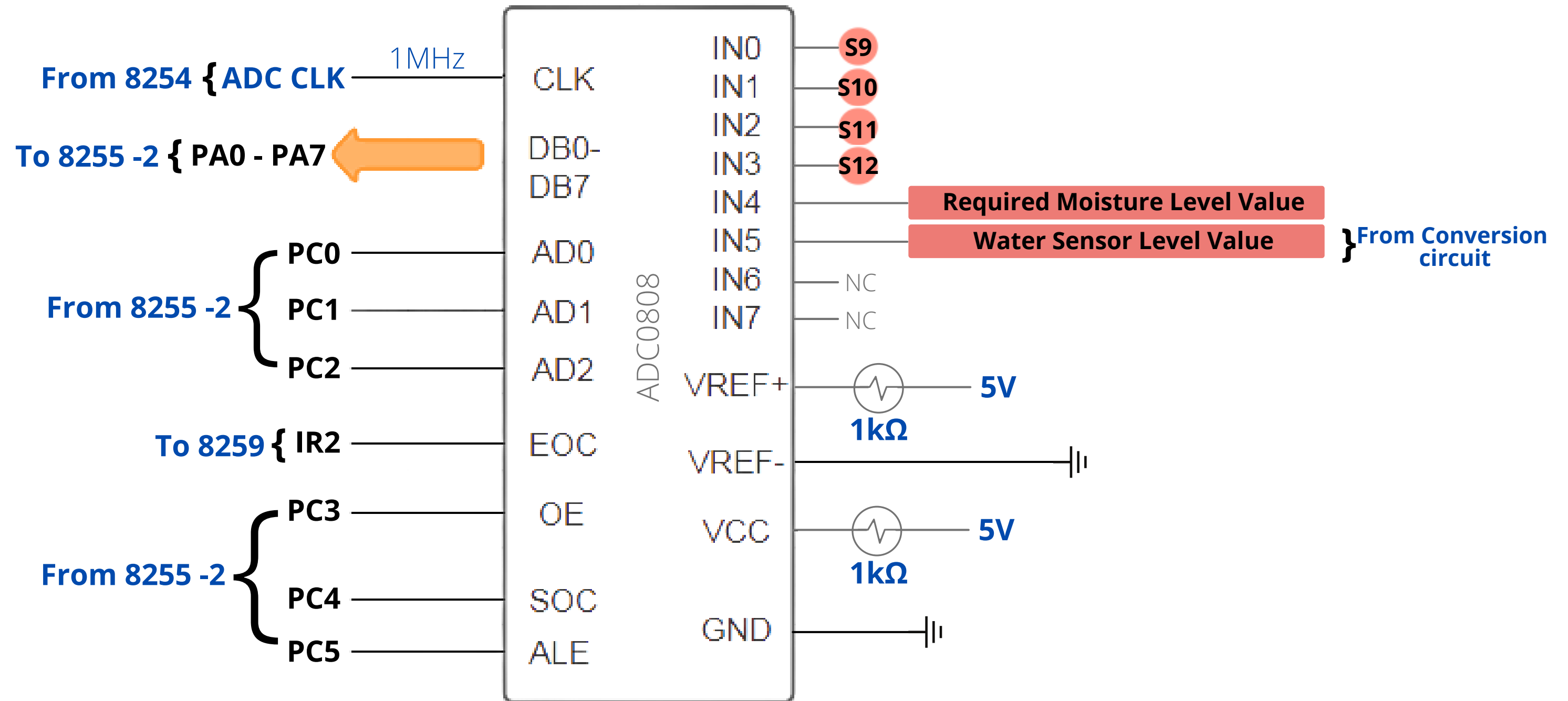
NOTE: For Proteus Simulation,
MASTER SWITCH is connected to PB0 of 8255-2
EOC from ADC-1 is connected to PB1 of 8255-2
EOC from ADC-2 is connected to PB2 of 8255-2

ADC0808 - 1



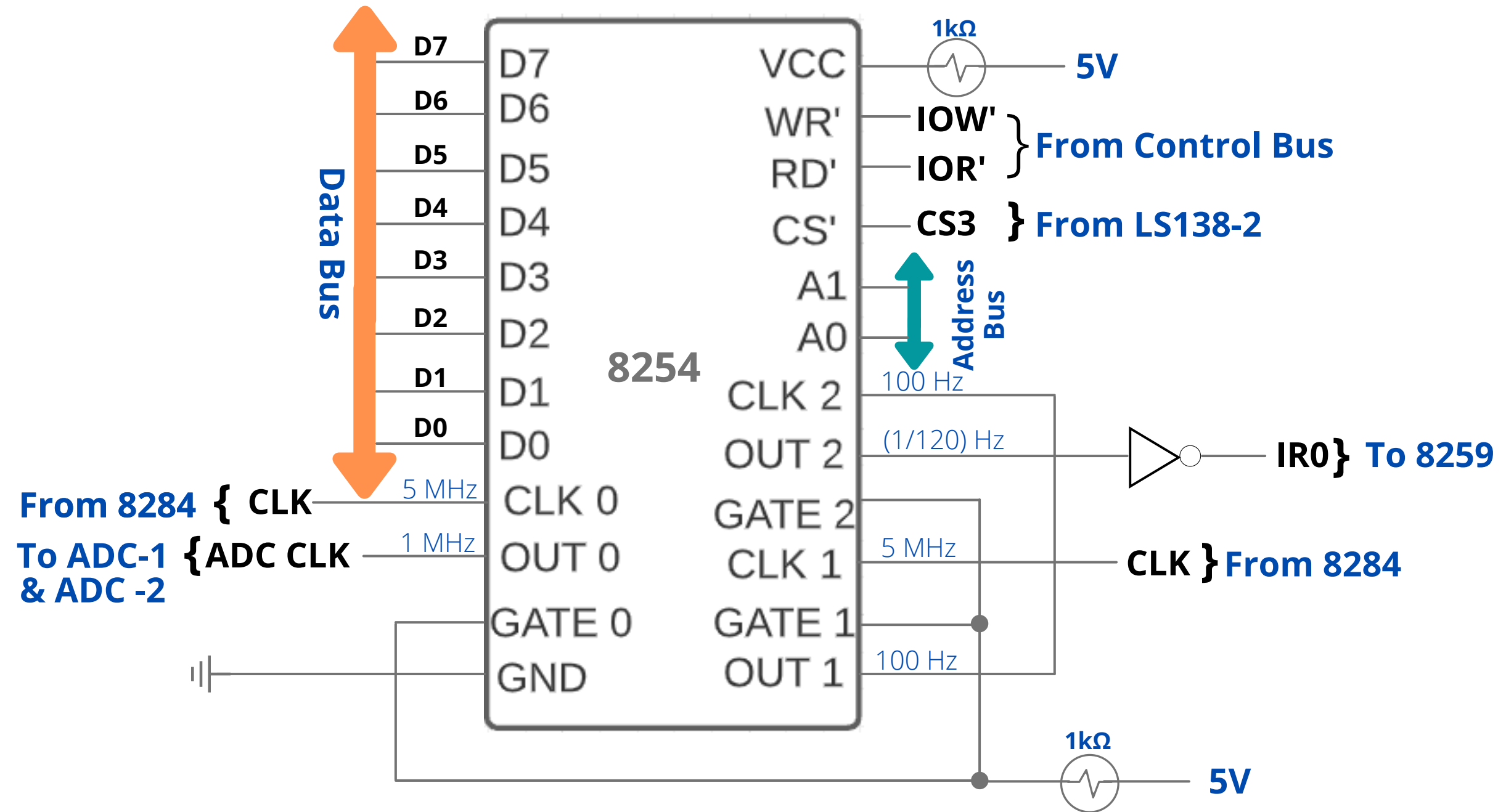
NOTE: For Proteus Simulation,
EOC from ADC1 is connected
to PB1 of 8255-2

ADC0808 - 2

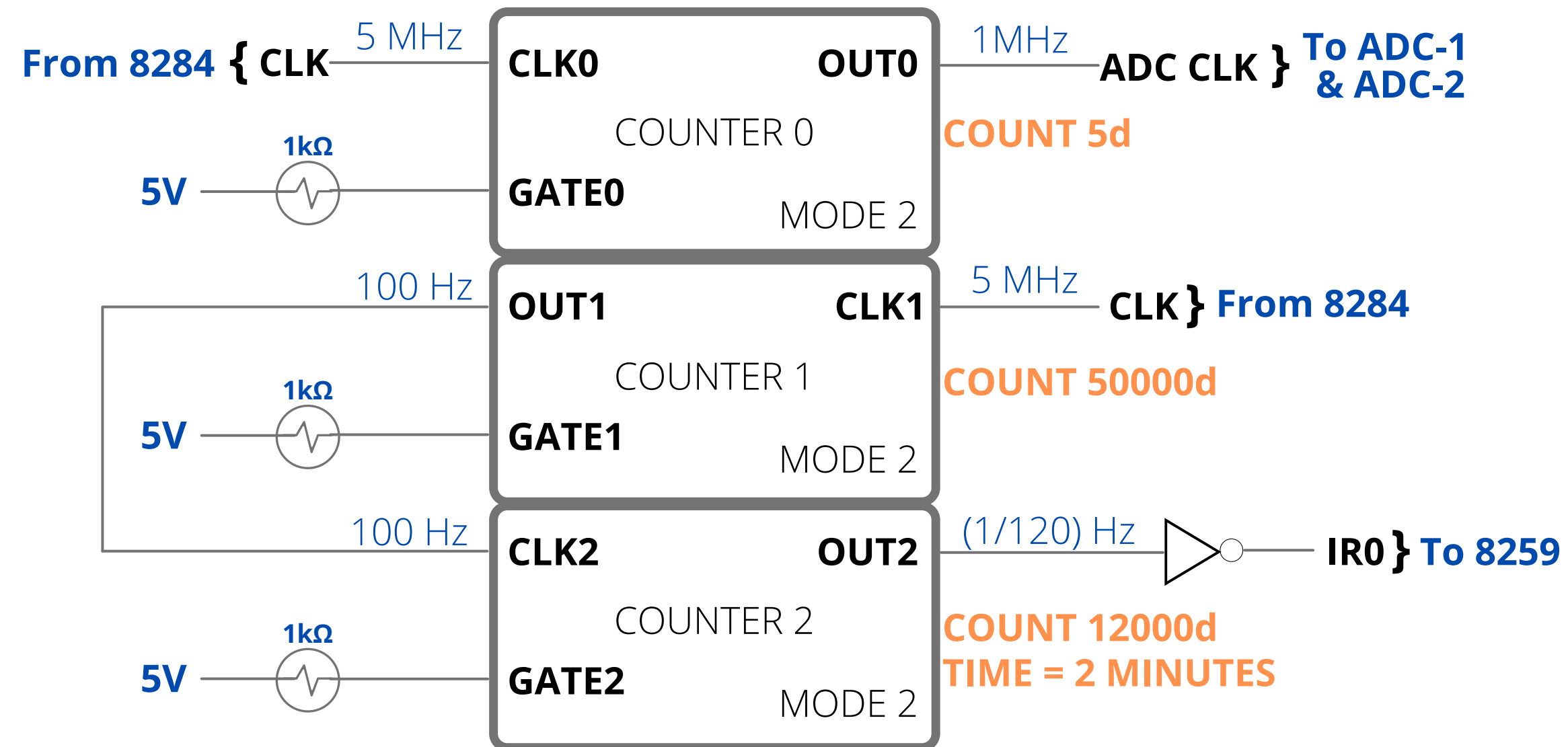


NOTE: For Proteus Simulation,
EOC from ADC2 is connected
to PB2 of 8255-2

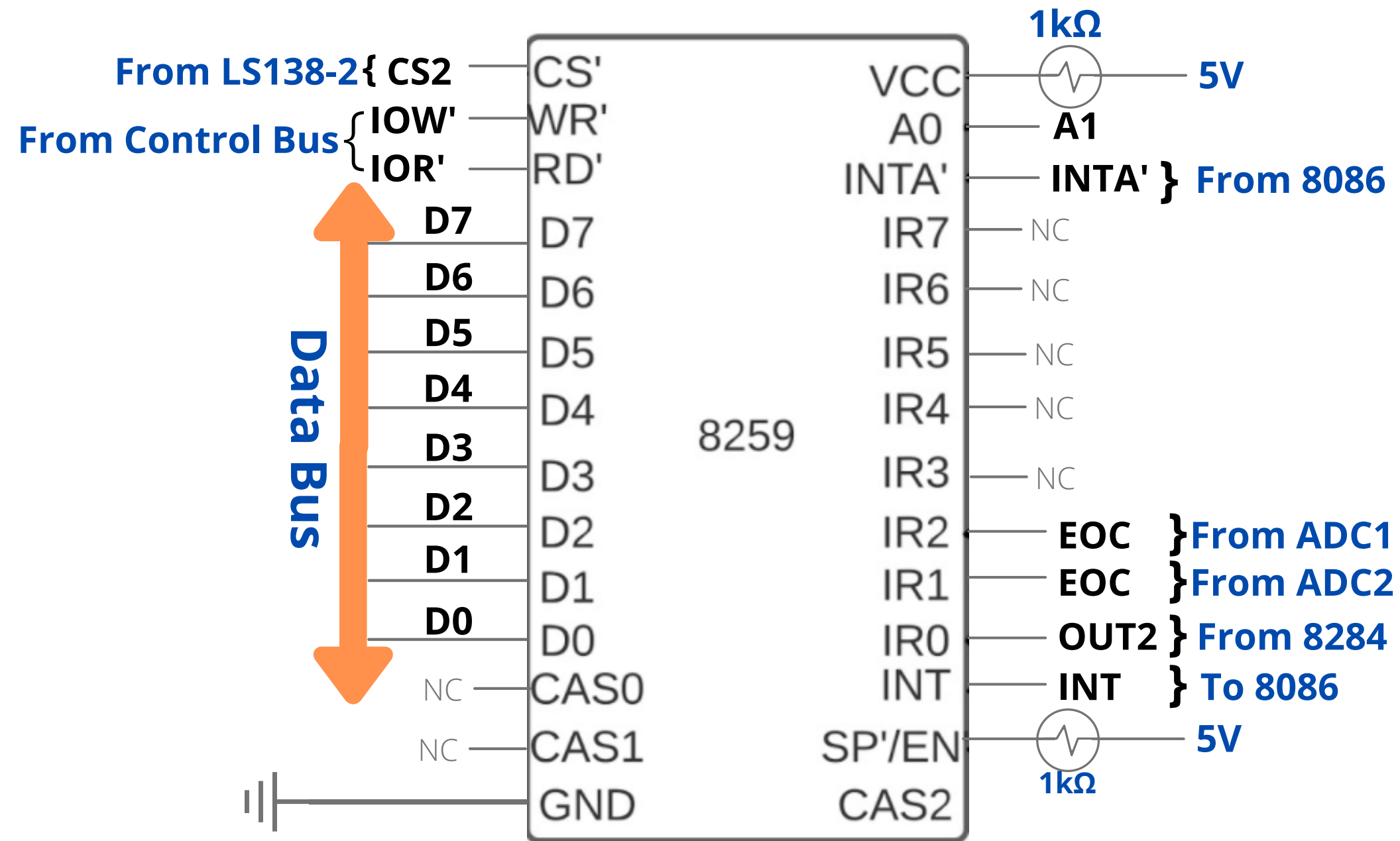
8254



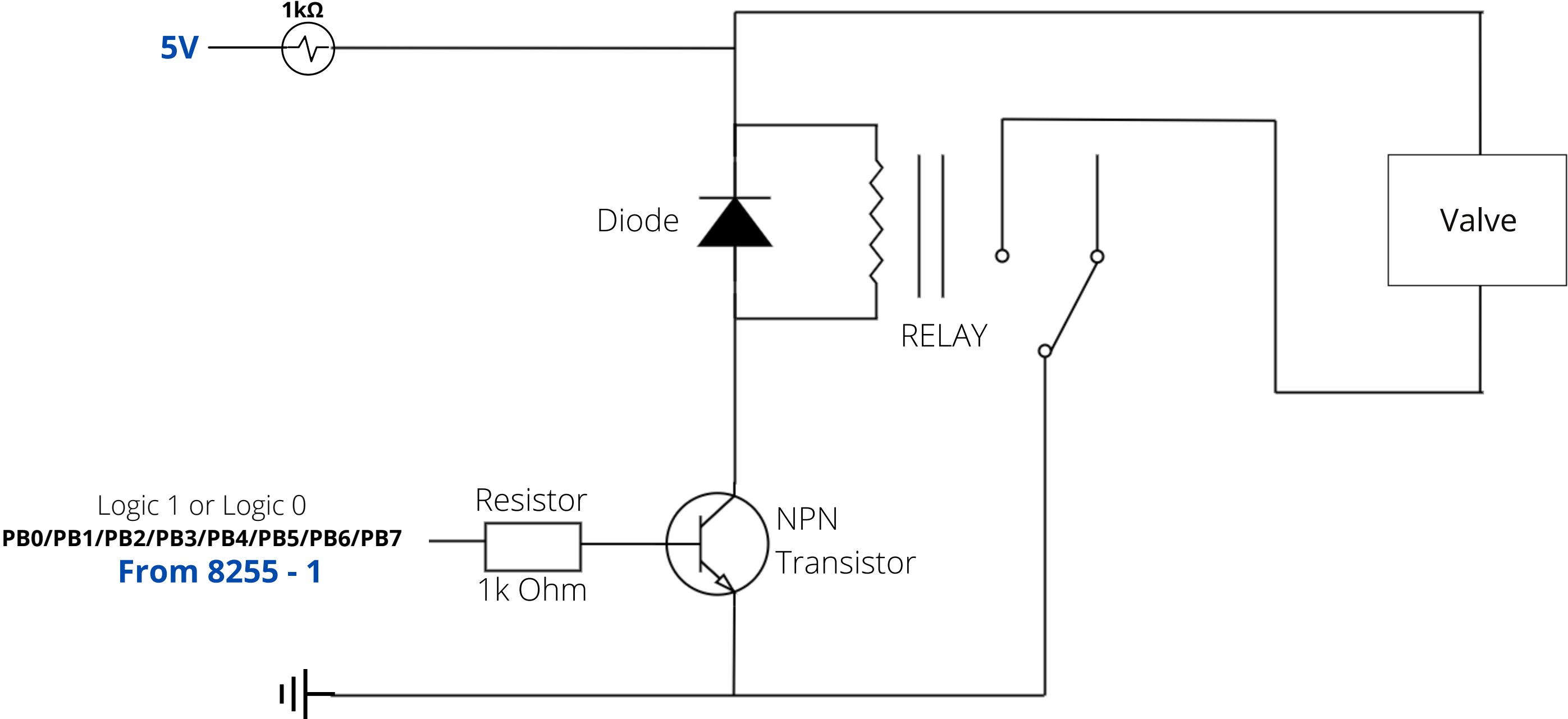
8254 Counters



8259



Relay Mechanism for Valves



Conversion Circuit from 4-20mA to 0-5V

