

18ECC203J – Module 3

8086 Interfacing with Memory and Programmable Devices

S – 1, 2, 3

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S - 1

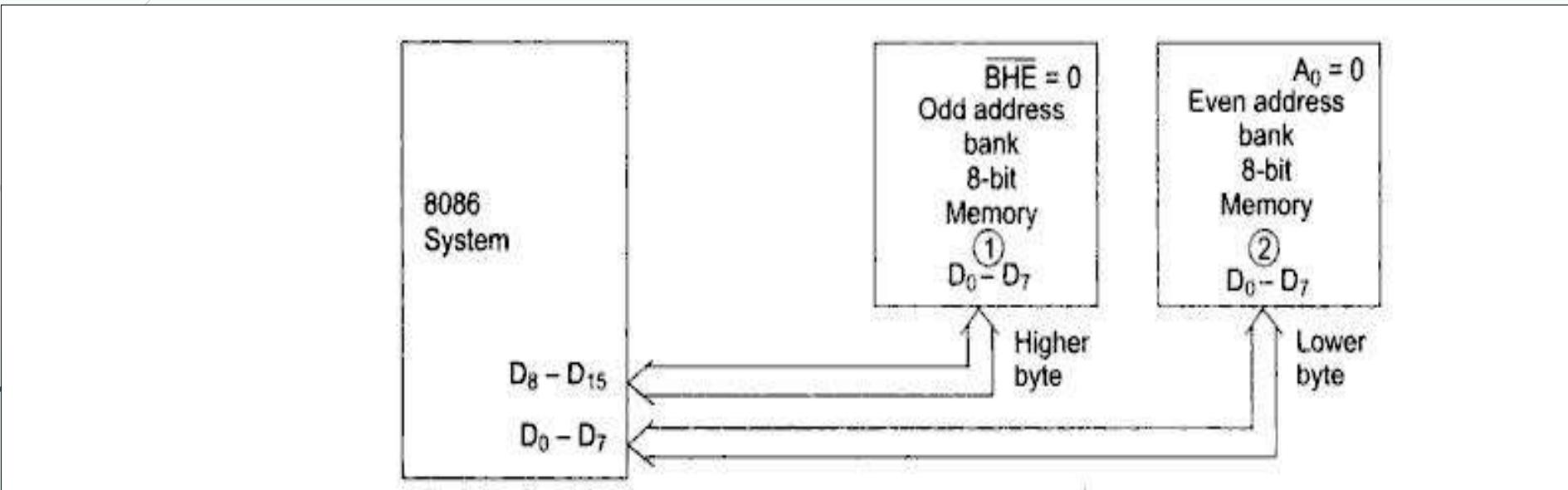
Semiconductor memory interfacing &
Dynamic RAM interfacing

Semiconductor RAM

- ▶ The semiconductor RAM is broadly two types – Static RAM and Dynamic RAM.
- ▶ Semiconductor memory organization
 - Memory is organised as two-dimensional arrays of memory locations.
 - 4K * 8 or 4K byte memory contains 4096 locations. Each location contains 8 bits
 - Only one of the 4096 locations can be selected at a time.
 - Once selected, all bits are available in Data bus.
 - For addressing the 4K bytes of memory, 12 address lines are required.
 - N memory locations means, n address lines required i.e. $n = \log_2 N$.
If the μP has n address lines, then it is able to address at the most N locations of memory, where $2^n = N$. If out of N locations only P memory locations are to be interfaced, then the least significant p address lines out of the n lines of μP are connected to the memory chip while the remaining ($n-p$) higher order address lines are used as inputs to the chip selection logic.
- ▶ The memory address depends upon the hardware circuit used for decoding the chip select (\overline{CS}). The output of the decoding circuit is connected with the \overline{CS} pin of the memory chip.

RECAP:- Physical Memory Organisation

(Module 1, Session 6, Slide No. 12)



- Certain locations in memory are reserved for specific CPU operations. The locations from FFFF0H to FFFFFH are reserved for operations including jump to initialisation programme and I/O-processor initialisation.
- The locations 00000H to 003FFH are reserved for *interrupt vector table*.

Procedure to Interface RAM

1. Arrange the available memory chip so as to obtain 16-bit data bus width. The upper 8-bit bank is called as 'odd address memory bank' and the lower 8-bit bank is called as 'even address memory bank'.
2. Connect available memory address lines of memory chip with those of the μP and also connect the memory \overline{RD} and \overline{WR} inputs to the corresponding processor control signals. Connect the 16-bit data bus of the memory bank with that of the microprocessor 8086.
3. The remaining address lines of the μP , \overline{BHE} and A_0 are used for decoding the required chip select signals for the odd and even memory banks. The \overline{CS} of memory is derived from the o/p of the decoding circuit.

As a good and efficient interfacing practice, the address map of the system should be continuous as far as possible, i.e. there should not be no windows in the map and no fold back space should be allowed.

Example Problem

- **Problem:** Interface two 4K x 8 EPROMS and two 4K x 8 RAM chips with 8086. Select suitable maps.
- **Solution:** We know that, after reset, the IP and CS are initialized to form address FFFF0h. Hence, this address must lie in the EPROM. The address of RAM may be selected anywhere in the 1 MB address space of 8086, but we will select the RAM address such that the address map of the system is continuous.

Memory Map Table

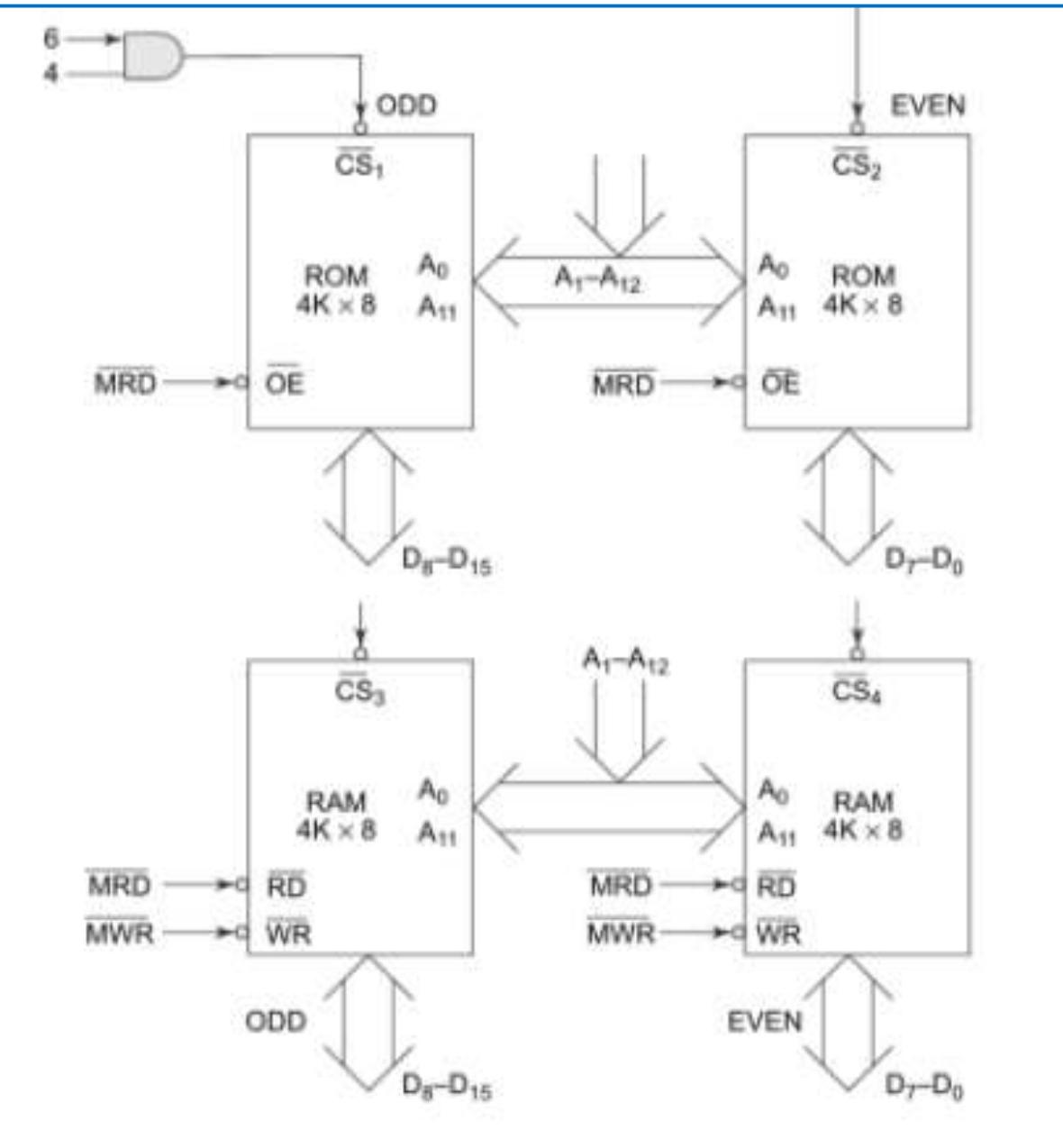
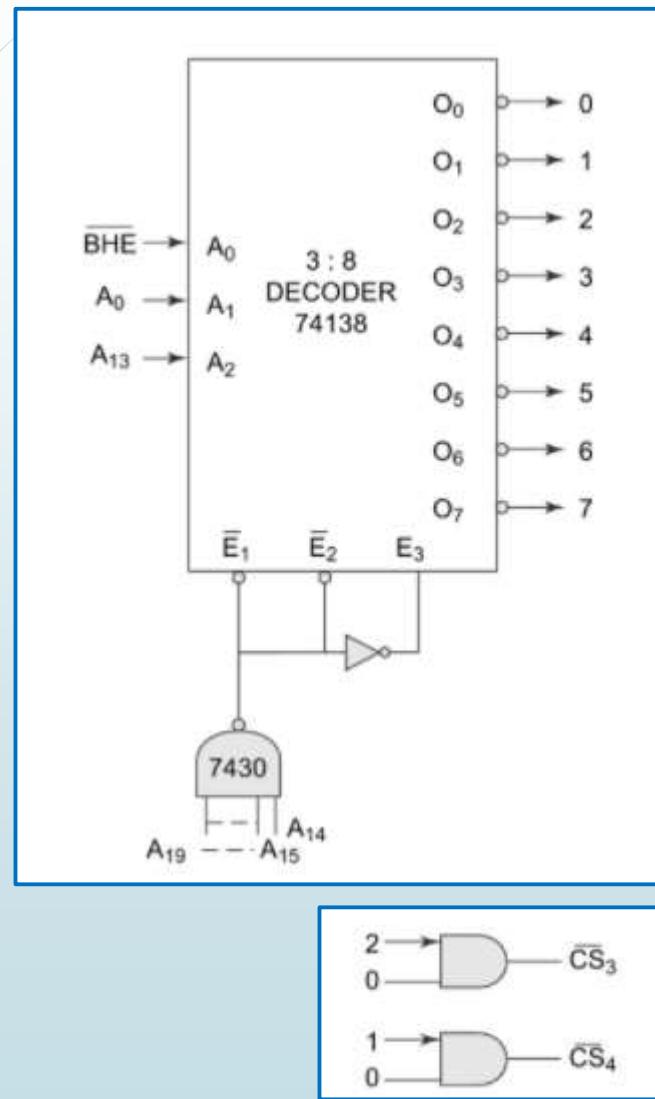
Solution (cont...)

- ▶ Total 8K bytes of EPROM need 13 address lines $A_0 - A_{12}$ (since $2^{13} = 8K$). Address lines $A_{13} - A_{19}$ are used for decoding to generate the chip select. The \overline{BHE} signal goes low when a transfer is at odd address or higher byte of data is to be accessed.
- ▶ The memory system in this example contains in total four $4K \times 8$ memory chips.
- ▶ The two $4K \times 8$ chips of RAM and ROM are arranged in parallel to obtain 16-bit data bus width. If A_0 is 0 is 0, i.e the address is even and is in RAM, then the lower RAM chip is selected indicating 8-bit transfer at an even address.
- ▶ If A_0 is 1, i.e., the address is odd and is in RAM, the \overline{BHE} signal goes low, the upper RAM chip is selected, further indicating that the 8-bit transfer is at an odd address.
- ▶ If A_0 and \overline{BHE} both are at 0, both the RAM and ROM chips are selected i.e. the data transfer is 16 bits.

Address Map

Decoder I/P → Address/ \overline{BHE} →	A_2	A_1	A_0 \overline{BHE}	Selection / Comments
Word transfer on $D_0 - D_{15}$	0	0	0	Even and odd addresses in RAM
Byte transfer on $D_7 - D_0$	0	0	1	Only even address in RAM
Byte transfer on $D_8 - D_{15}$	0	1	0	Only odd address in RAM
Word transfer on $D_0 - D_{15}$	1	0	0	Even and odd addresses in ROM
Byte transfer on $D_7 - D_0$	1	0	1	Only even address in ROM
Byte transfer on $D_8 - D_{15}$	1	1	0	Only odd address in ROM

Diagram



Dynamic RAM

- ▶ Whenever a large capacity memory is required in a microcomputer system, the memory subsystem is generally designed using dynamic RAM (DRAM).
- ▶ Advantages of DRAM over Static RAM
 1. Higher packing density,
 2. lower cost and
 3. less power consumption
- ▶ A static RAM cell has 6 transistors while the dynamic RAM cell has 1 transistor and a capacitor. This leads to higher packaging density and low cost per unit.
- ▶ The function of capacitor is carried out by diode that operates in a reverse bias mode.

Dynamic RAM (Contd...)

- The reverse-biased diode has leakage current that tends to discharge the capacitor giving rise to the possibility of data loss. To avoid this, the stored data in the cell is refreshed in regular intervals. The process is called as **Refresh cycle**.
- The refresh activity is similar to reading the data from each and every cell of memory, independent of the requirement of microprocessor. During this refresh period all other operations related to the memory subsystem are suspended. Hence the refresh activity causes **loss of time**, resulting in **reduce system performance**.
- However keeping in view the advantages of dynamic RAM, like low power consumption, high packaging density and low cost, most of the advanced computing system are designed using dynamic RAM, at the cost of operating speed.
- A dedicated hardware chip called as **dynamic RAM controller** is the most important part of the interfacing circuit.

Refresh Cycle

- The Refresh cycle is different from the memory read cycle in the following aspects.
 1. The memory address is not provided by the CPU address bus, rather it is generated by a refresh mechanism counter called as **refresh counter**.
 2. Unlike memory read cycle, **more than one memory chip** may be enabled at a time so as to reduce the number of total memory refresh cycles.
 3. The **data enable** control of the selected memory chip is deactivated, and data is not allowed to appear on the system data bus during refresh, as more than one memory units are refreshed simultaneously. This is to avoid the data from the different chips to appear on the bus simultaneously.
 4. Memory read is either a **processor initiated** or an external bus master initiated and carried out by the refresh mechanism.

Refresh Cycle (2)

- ▶ Dynamic RAM is available in units of several **kilobits to megabits** of memory. This memory is arranged internally in a 2 – D matrix so that it will have n rows and m columns. The row address n and column address m are important for the **refreshing** operation.
- ▶ A 4 K bit dynamic RAM chip is internally arranged bit array of dimension $64 * 64$, i.e. 64 rows and 64 columns. The row address and column address will require 6 bits each (since $2^6 = 64$). These 6 bits for each row address and column address are generated by the refresh counter, during the refresh cycles.
- ▶ A complete row of 64 cells is refreshed at a time to minimize the refreshing time. Thus the refresh counter generate row addresses only. The row address are multiplexed, over lower order address lines.

Refresh Cycle (3)

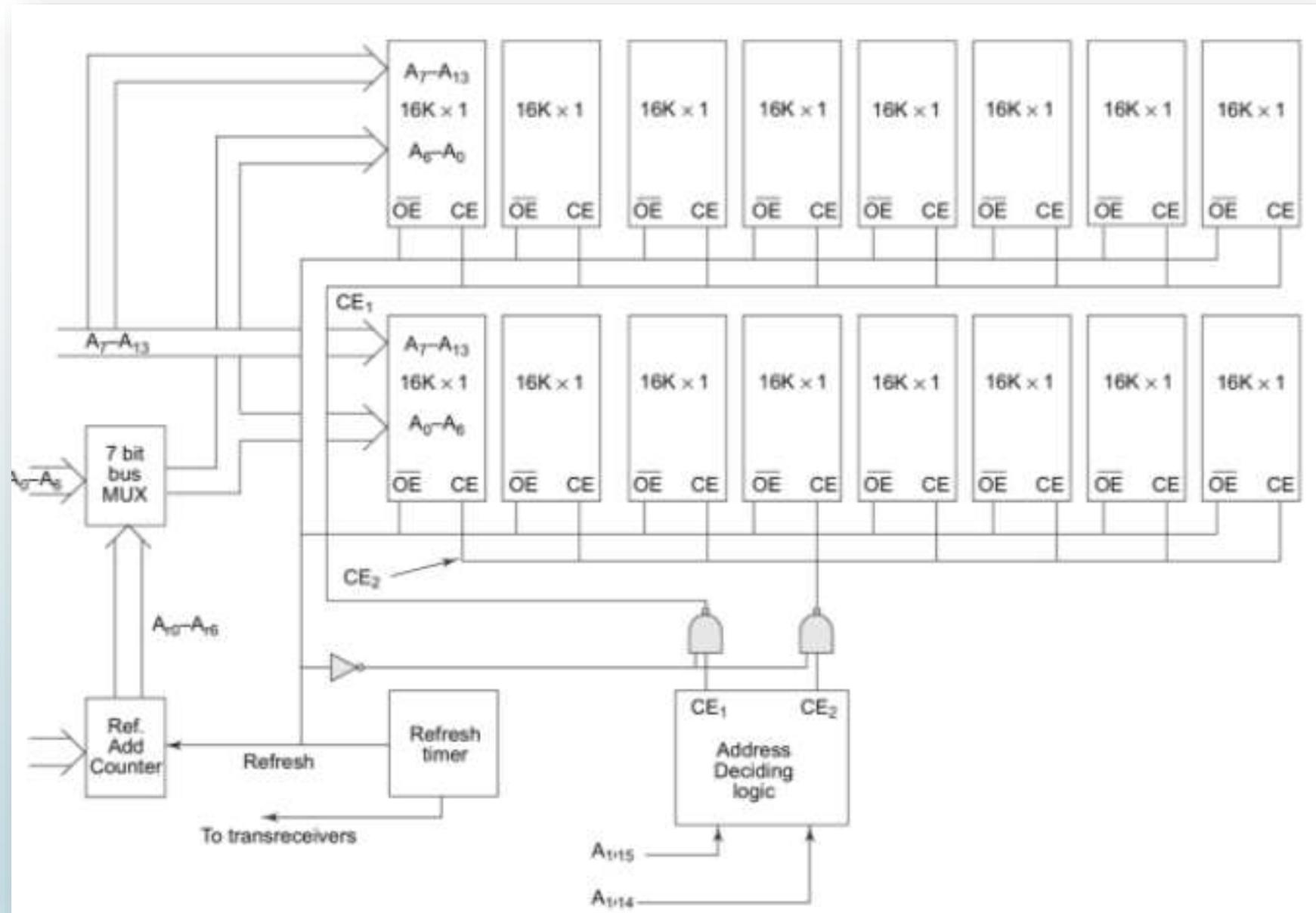
- ▶ During refresh cycle is in process the refresh counter puts the row address over the address bus.
- ▶ During normal processor-initiated activities the address bus of the processor is connected to the address bus of DRAM.
- ▶ A timer, called refresh timer, derives a pulse for refreshing action after each refresh interval.
- ▶ **Refresh interval** can be qualitatively defined as the time for which a dynamic RAM cell can hold data charge level practically constant, i.e. no data loss takes place.
- ▶ If a dynamic RAM chip has 64 rows, then all the 64 rows are to refreshed in a single refresh interval.

Refresh Cycle (4)

- ▶ This refresh interval depends upon the manufacturing technology of the dynamic RAM cell.
- ▶ It may range anywhere from 1 msec to 3 msec.
- ▶ **Example:** Find the frequency of refresh pulses for 4K DRAM arranged in 64 columns x 64 rows. Assume refresh time interval as 2 msec.

$$\text{Refresh Time (per row)} \ t_r = \frac{2 \times 10^{-3}}{64} \quad \dots (1)$$

$$\text{Refresh Frequency } f_r = \frac{64}{2 \times 10^{-3}} \quad \dots (2)$$



Dynamic RAM refresh Logic

Refresh Cycle (5)

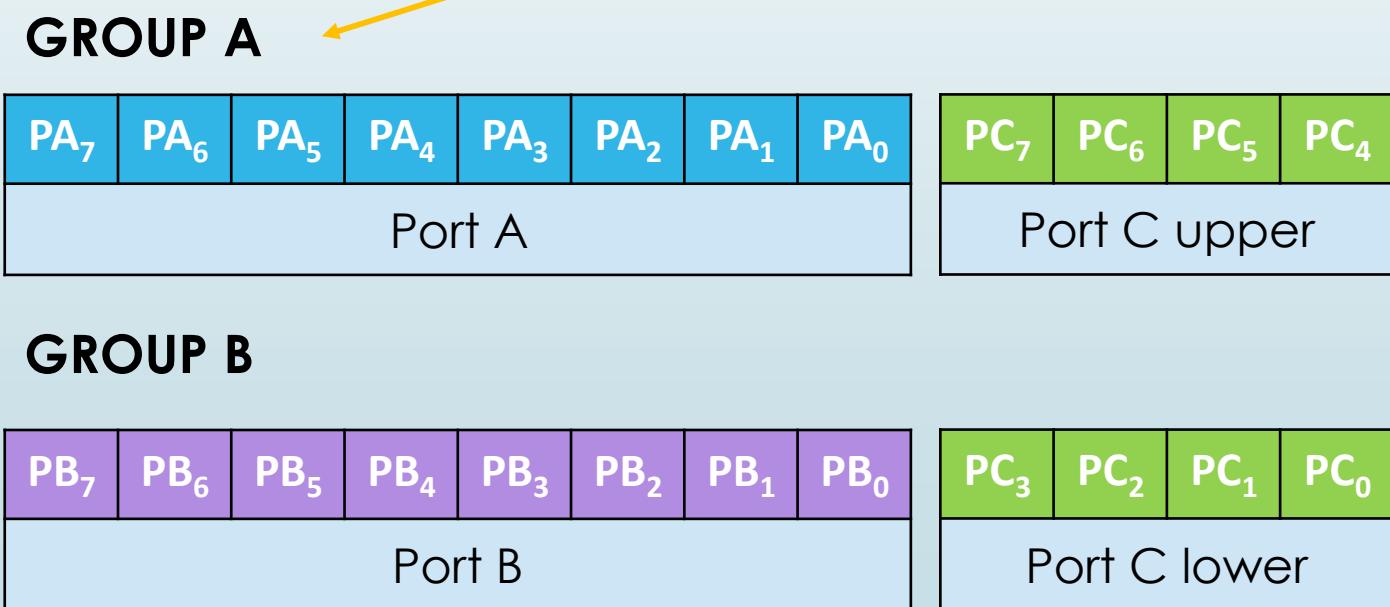
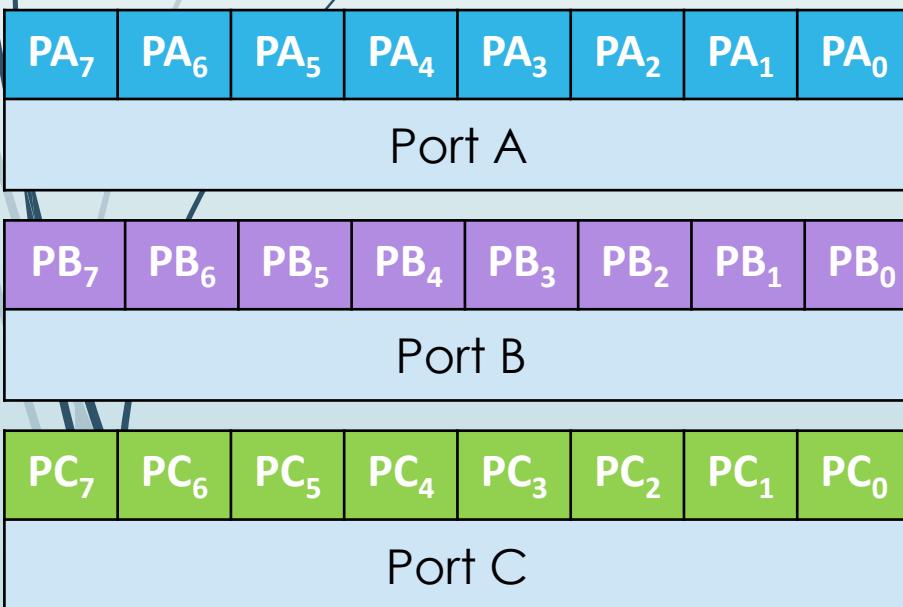
- ▶ Each chip is of 16K * 1-bit dynamic RAM cell array. The system contains two 16K byte dynamic RAM units. All the address and data lines are assumed to be available from an 8086-microprocessor system.
- ▶ The \overline{OE} pin controls output data buffer of the memory chips. The Chip Enable (CE) pins are active high chip select signals.
- ▶ When the refresh cycle starts, \overline{OE} and CE pins tend to go high. The high CE enables the memory chip for refreshing, while high OE prevents the data from appearing on the data bus.
- ▶ The 16K * 1-bit dynamic RAM has an internal array of 128*128 cells, requiring 7 bits for row address. The lower order seven lines A_0-A_6 are multiplexed with the refresh counter output $A_{10}-A_{16}$.

S – 2

Programmable Peripheral Interface 8255 &
Interfacing 8255 with 8086 and programming

8255 – Ports

► The Parallel Input-Output Port chip 8255 is also called as Programmable Peripheral Input-Output Port. The Intel's 8255 is designed for use with Intel's 8-bit, 16-bit and higher capability microprocessors. It has 24 input/output lines which may be individually programmed in two groups of 12 lines each, OR or three groups of eight lines.



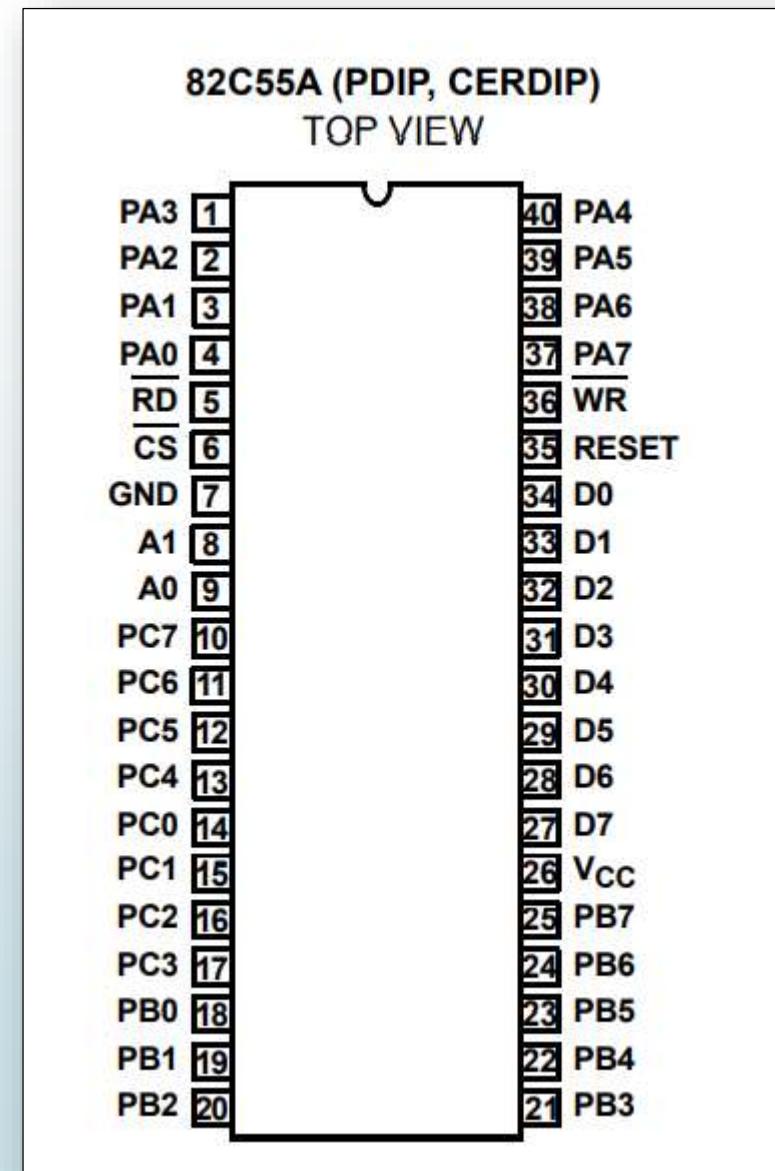
8255 – Ports (2)

- ▶ The two groups of I/O pins are named as Group A and Group B. Each of these two groups contains a subgroup of eight I/O lines called as 8-bit port and another subgroup of four lines or a 4-bit port. Thus, Group A contains an 8-bit port A along with a 4-bit port C upper.
- ▶ The port A lines are identified by symbols PA_0-PA_7 while the port C upper lines are identified as PC_7-PC_4 . Similarly, Group B contains an 8-bit port B, containing lines PB_0-PB_7 and a 4-bit port C with lower bits $PC_0- PC_3$. The port C upper and port C lower can be used in combination as an 8-bit port C. Upper and lower port C are assigned the same address.
- ▶ Either Three 8- bit I/O ports or two 8-bit and two 4-bit C ports from 8255 are possible. All of these ports can function independently either as input or as output ports. This can be achieved by programming the bits of an internal register of 8255 called as Control Word Register (CWR).

8255 – Ports (3)

- ▶ The 8-bit data bus buffer is controlled by the read/write control logic. The read/write control logic manages all of the internal and external transfers of both data and control words.
- ▶ \overline{RD} , \overline{WR} , A_1 , A_0 and RESET are the inputs provided by the microprocessor to the READ/ WRITE control logic of 8255. The 8-bit, 3-state bidirectional buffer is used to interface the 8255 internal data bus with the external system data bus.
- ▶ This buffer receives or transmits data upon the execution of input or output instructions by the microprocessor. The control words or status information is also transferred through the buffer.

Pin Diagram



Pin Diagram of 8255

Signal Description

- ▶ PA₇ – PA₀ : These are eight port A lines that acts as either latched output or buffered input lines depending upon the control word loaded into the CWR.
- ▶ PC₇ – PC₄ : Upper nibble of port C lines. They may act as either output latches or input buffers lines. This port also can be used for generation of handshake lines in mode 1 or mode 2.
- ▶ PC₃ – PC₀ : These are the lower port C lines; other details are the same as PC₇ – PC₄ lines.
- ▶ PB₇ – PB₄ : These are the eight port B lines which are used as latched output lines or buffered input lines in the same way as port A.

Signal Description (2)

- ▶ \overline{RD} : This is the input line driven by the microprocessor and should be low to indicate read operation to 8255.
- ▶ \overline{WR} : This is an input line driven by the microprocessor. A low on this line indicates write operation.
- ▶ \overline{CS} : This is a chip select line. If this line goes low, it enables the 8255 to respond to RD and WR signals, otherwise RD and WR signal are neglected.
- ▶ A_1-A_0 : These are the address input lines and are driven by the μP . These lines A_1-A_0 with \overline{RD} , \overline{WR} and \overline{CS} from the following operations for 8255.
 - These address lines (A_1-A_0) are used for addressing any one of the four registers, i.e. three ports and a Control Word Register (CWR).

8255 – Addressing Ports

A1	A0	\overline{RD}	\overline{WR}	\overline{CS}	INPUT OPERATION (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus → Three-State
X	X	1	1	0	Data Bus → Three-State

Image Courtesy : 8255 data sheet

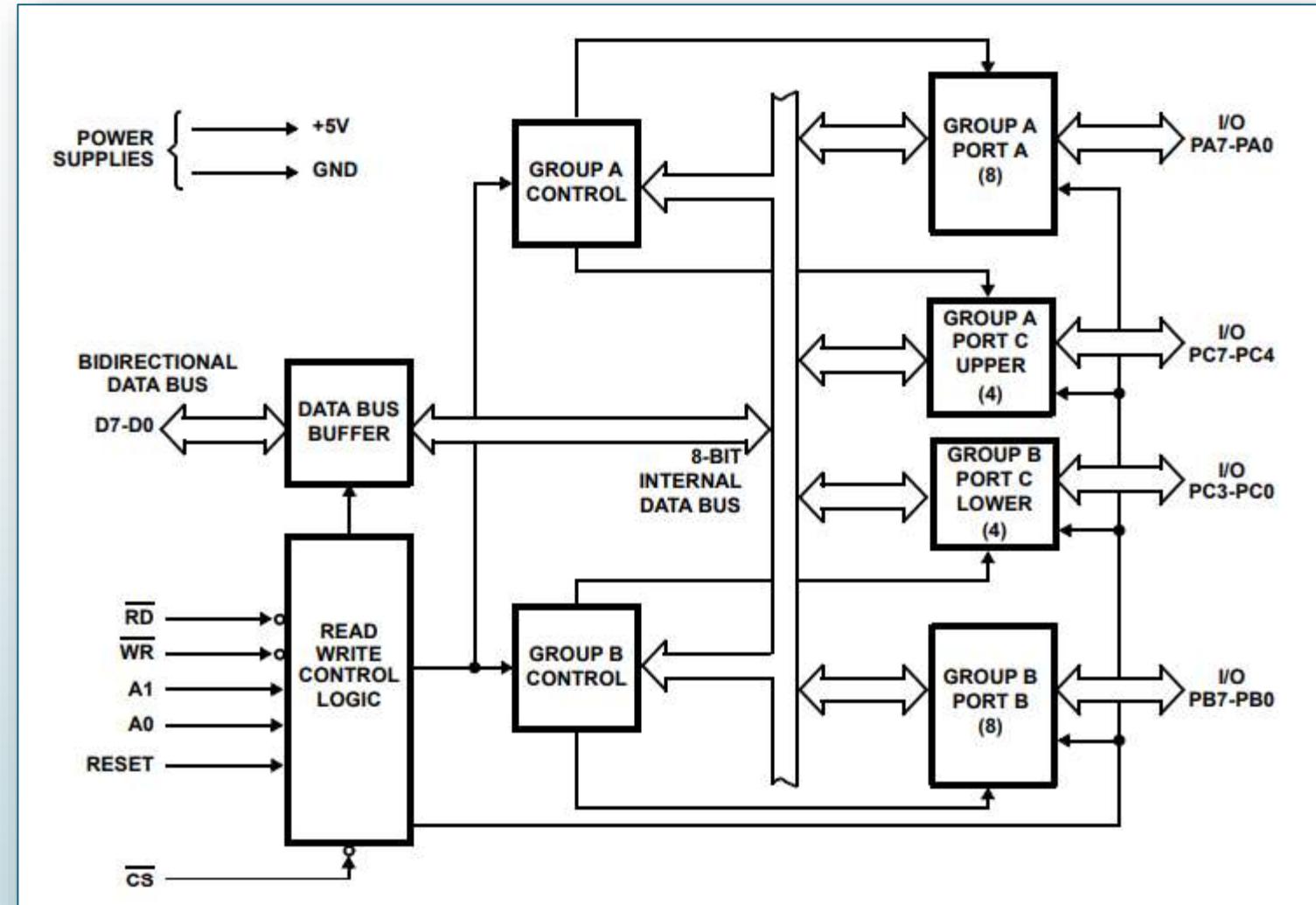
Signal Description (3)

- ▶ In case of 8086 systems, if the 8255 is to be interfaced with lower order data bus, the A₀ and A₁ pins of 8255 are connected with A₁ and A₂ respectively.
- ▶ D₀-D₇: These are the data bus lines those carry data or control word to/from the microprocessor.
- ▶ RESET: A logic high on this line clears the control word register of 8255. All ports are set as input ports by default after reset.
- ▶ It has a 40 pins of 4 groups.

8255 – Internal Architecture

SECTIONS

1. Data bus
2. Read Write control logic
3. Group A and Group B controls
4. Port A, B and C



8255 Internal Architecture

Architecture – Explanation

1. **Data bus buffer:** This is a tristate bidirectional buffer used to interface the 8255 to system data bus. Data is transmitted or received by the buffer on execution of input or output instruction by the CPU.
 - Control word and status information are also transferred through this unit.
2. **Read/Write control logic:** This unit accepts control signals (\overline{RD} , \overline{WR}) and also inputs from address bus and issues commands to individual group of control blocks (Group A, Group B).
3. **Group A and Group B controls:** These block receive control from the CPU and issues commands to their respective ports.
 - Group A - PA and PCU ($PC_7 - PC_4$) Group B - PCL ($PC_3 - PC_0$)
 - CWR can only be written into no read operation of the CWR is allowed.

Architecture – Explanation (2)

4. Port A, B and C

- Port A: This has an 8 bit latched/buffered O/P and 8 bit input latch. It can be programmed in 3 modes – mode 0, mode 1, mode 2
- Port B: This has an 8 bit latched / buffered O/P and 8 bit input latch. It can be programmed in mode 0, mode 1.
- Port C : This has an 8 bit latched input buffer and 8 bit output latched/buffer. This port can be divided into two 4 bit ports and can be used as control signals for port A and port B. it can be programmed in mode 0.

BSR and IO Mode

- ▶ These are two basic modes of operation of 8255.
- ▶ I/O mode and Bit Set-Reset (BSR) mode.
- ▶ In BSR mode only port C (PC_0-PC_7) can be used to set or reset its individual port bits. In I/O mode, the 8255 ports work as **programmable I/O ports**. Under the I/O mode of operation, mode 0, mode 1 and mode 2 is possible
- ▶ **BSR Mode:** In this mode any of the 8-bits of port C can be set or reset depending on D0 of the control word. The bit to be set or reset is selected by bit select flags D3, D2 and D1 of the CWR.

BSR Mode

Port C bits can be SET or RESET

Example

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	1	1	0	1

Port C: 6th bit is SET

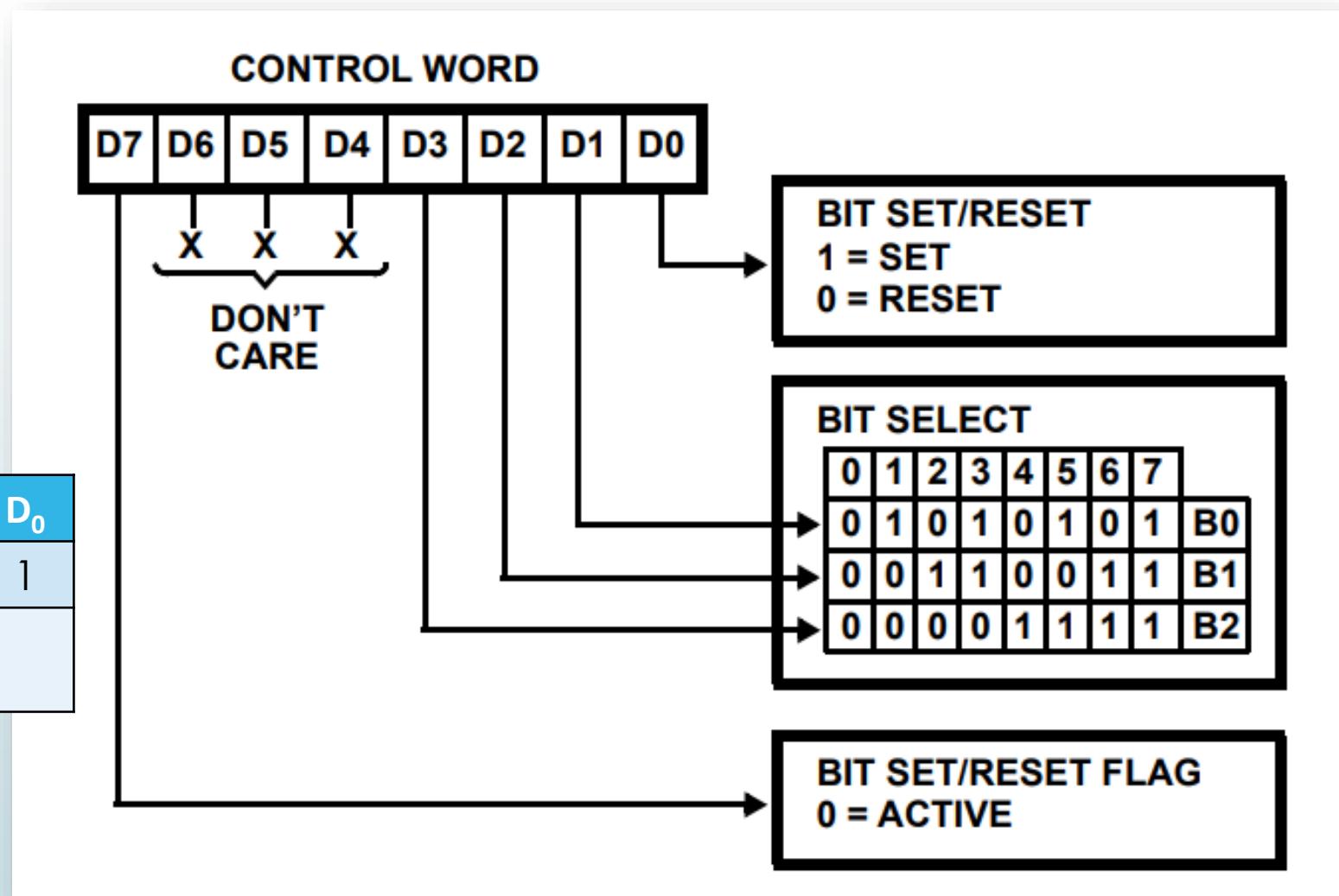


Image Courtesy: 8255 Data sheet

I/O Mode CWR

Example

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	1	0	0	0
IO mode	Mode 0		Port A input	Port C (up) input	Mode 0	Port B output	Port C (low) output

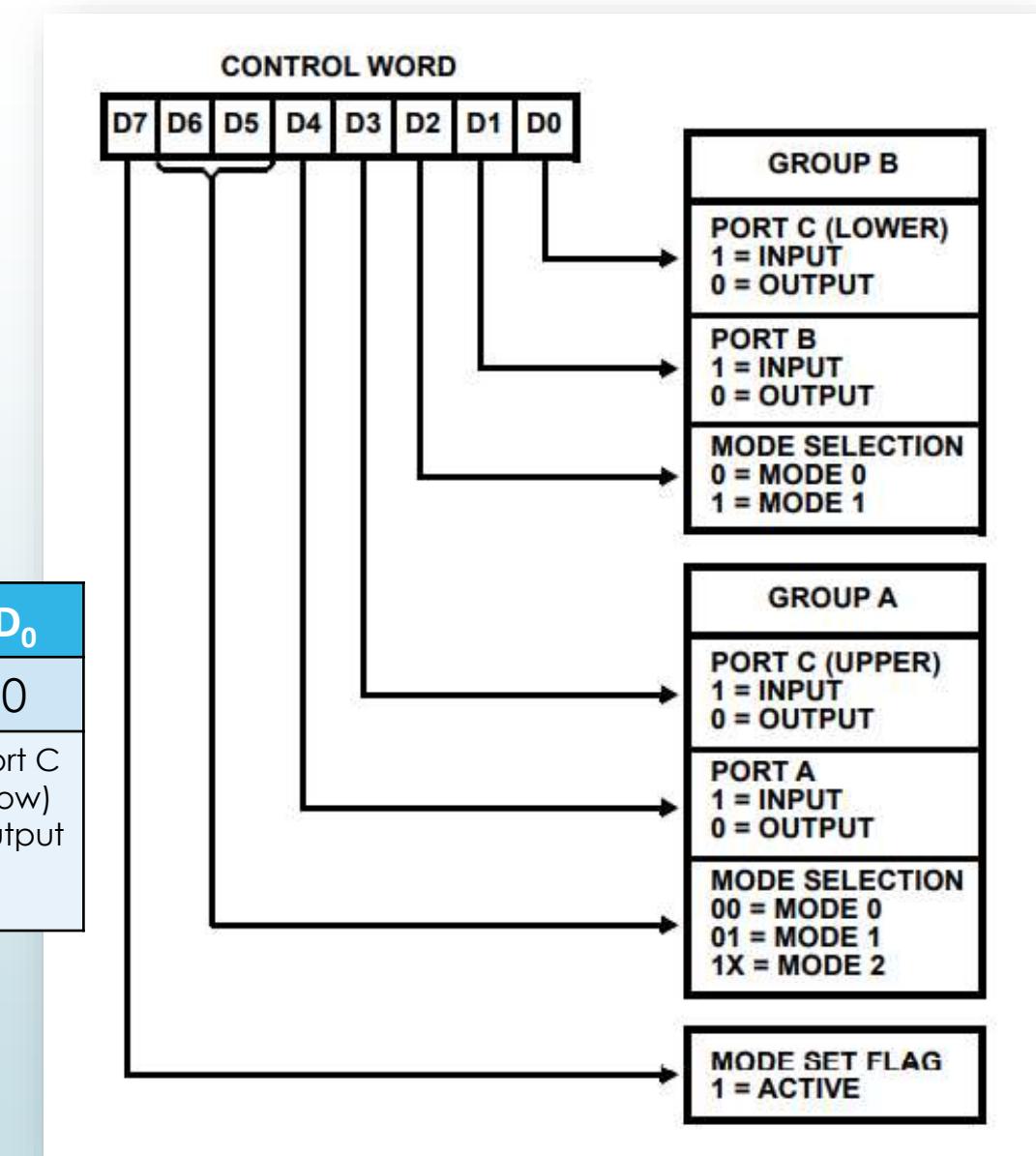


Image Courtesy: 8255 Data sheet

Mode 0 (Basic I/O mode)

- ▶ This mode is also called as basic Input/Output mode. This mode provides simple input and output capabilities using each of the three ports. Data can be simply read from and written to the input and output ports respectively, after appropriate initialisation.
- ▶ **The salient features**
 1. Two 8-bit ports (port A and port B)and two 4-bit ports (port C upper and lower) are available. The two 4-bit ports can be combinedly used as a third 8-bit port.
 2. Any port can be used as an input or output port.
 3. Output ports are latched. Input ports are not latched.
 4. A maximum of 4 ports are available. so, 16 I/O configuration are possible.

Mode 1 (Strobed input/output mode)

- In this mode the **handshaking** control the input and output action of the specified port. Port C lines PC_0-PC_2 , provide strobe or handshake lines for port B. This group which includes port B and PC_0-PC_2 is called as group B for Strobed data input/output. Port C lines PC_3-PC_5 provide strobe lines for port A. This group including port A and PC_3-PC_5 from group A. Thus, port C is utilized for generating handshake signals.
- The salient features of mode 1 are listed as follows:
 1. Two groups – group A and group B are available for strobed data transfer.
 2. Each group contains one 8-bit data I/O port and one 4-bit control/data port.
 3. The 8-bit data port can be either used as input and output port. The inputs and outputs both are latched.
 4. Out of 8-bit port C, PC_0-PC_2 are used to generate control signals for port B and PC_3-PC_5 are used to generate control signals for port A. the lines PC_6 , PC_7 may be used as independent data lines.

Mode 2 (Strobed bidirectional I/O)

- ▶ This mode of operation provides 8255 with additional features for communicating with a peripheral device on an 8-bit data bus. Handshaking signals are provided to maintain proper data flow and synchronization between the data transmitter and receiver. The interrupt generation and other functions are similar to mode 1
- ▶ In this mode, 8255 is a bidirectional 8-bit port with handshake signals. The \overline{RD} and \overline{WR} signals decide whether the 8255 is going to operate as an input port or output port.
- ▶ The Salient features of Mode 2 of 8255 are listed as follows:
 1. The single 8-bit port in group A is available.
 2. The 8-bit port is bidirectional and additionally a 5-bit control port is available.

S – 3

Interfacing ADC with 8086 and programming &
Interfacing DAC with 8086 and programming

Analog-to-Digital Converter (ADC)

- ▶ μP considers ADC as a input device. So, it sends Start of Conversation (SoC) signal (pulse of a specific duration) to ADC.
- ▶ Analog to digital conversion is a **slow** process. So, ADC will send a End of Conversion (EoC) signal to μP, when the conversion is over. Then μP can take the result from the buffer. EoC signal can trigger a interrupt in 8086 or μP can poll the EoC signal.
- ▶ Usually μP will use the IO ports of 8255 to interact with ADC. Like reading EoC signal from ADC and reading digital output of ADC.

Analog-to-Digital Converter (2)

- ▶ The time taken by the ADC from the active edge of SoC pulse till the active edge of EoC signal is called as the **conversion delay** of the ADC.
- ▶ Conversion delay: few μs (fast ADC) to few 100 ms (slow ADC).
- ▶ Most popular conversion techniques in integrated ADC chips
 - Successive Approximation Techniques
 - Dual Slope Integration Techniques

ADC Interfacing – General Algorithm

1. Ensure the stability of analog input, applied to the ADC.
2. Issue SoC pulse to ADC
3. Read EoC signal to mark the end of conversion processes.
4. Read digital data output of the ADC as equivalent digital output.
5. Analog input voltage must be constant at the input of the ADC right from the start of conversion till the end of the conversion to get correct results.
This may be ensured by a **sample and hold circuit (S-H)** which samples the analog signal and holds it constant for a specific time duration. μP issue a hold signal to the S-H circuit.
6. If the applied input changes before the complete conversion process is over, the digital equivalent of the analog input calculated by the ADC may not be correct.

ADC 808 and 809 Characteristics

- The ADC chips 0808 and 0809 are 8-bit CMOS, successive approximation converters. The conversion delay is 100 μ s at a clock frequency of 640 KHz.
- No need of external zero or full scale adjustments. They are inbuilt in the chip.
- These converters internally have a 3:8 analog multiplexer so that at a time 8 different analog conversion can be carried out. Use address lines - ADD A, ADD B, ADD C.
- In multichannel applications – The CPU drive the lines using output port. In single channel applications – the lines are hardwired to select the input.
- There are **unipolar** analog to digital converters, i.e. they are able to convert only positive analog input voltage to their digital equivalent. These chips do no contain any internal sample and hold circuit.

Table

Analog I/P selected	Address lines		
	C	B	A
I/P 0	0	0	0
I/P 1	0	0	1
I/P 2	0	1	0
I/P 3	0	1	1
I/P 4	1	0	0
I/P 5	1	0	1
I/P 6	1	1	0

Address mapping

NOTE

- The signal I/P₀ is referred as IN0 in Pin Diagram
- The signals O₀, O₂, ... O₇ are referred as 2⁻⁸, 2⁻⁷ ... 2⁻¹ in Pin Diagram

Block Diagram

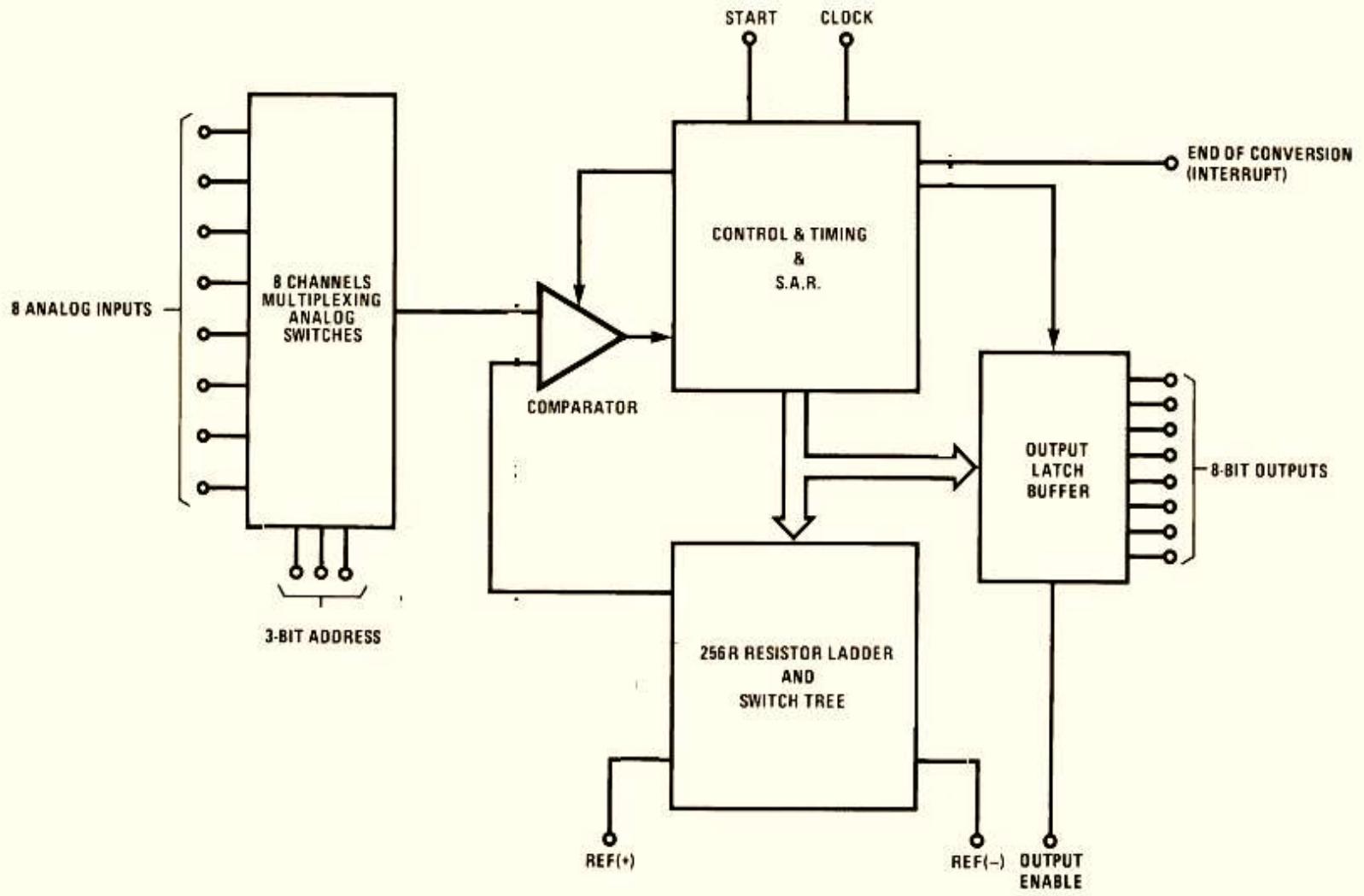


Image Courtesy: 808 IC data sheet

Pin Diagram

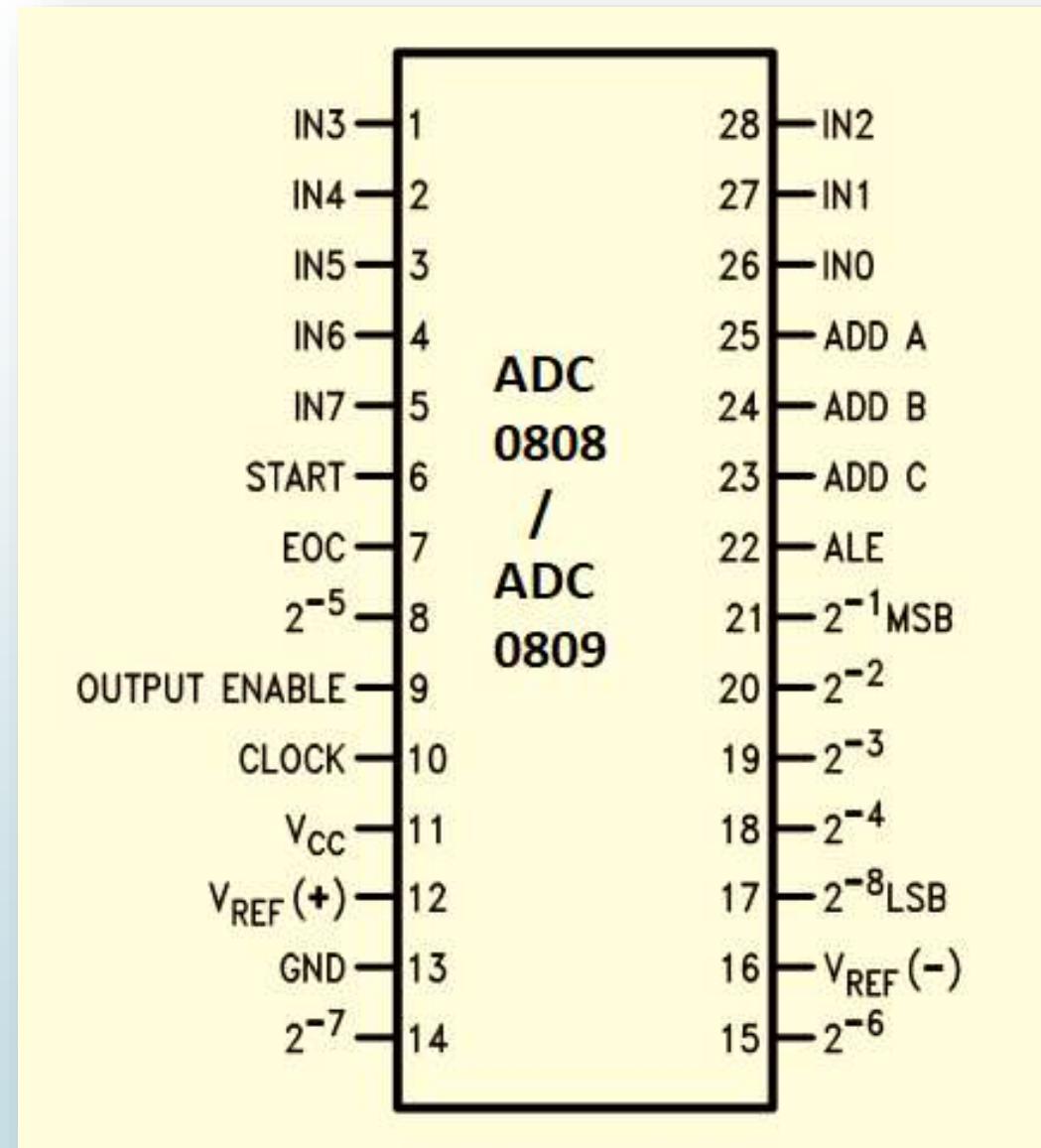


Image Courtesy: ADC 808 Data sheet

Example Interfacing Problem

- ▶ **Example:** Interfacing ADC 0808 with 8086 using 8255 ports. Use port A of 8255 for transferring digital data output of ADC to the CPU and port C for control signals. Assume that an analog input is present at I/P2 of the ADC and a clock input of suitable frequency is available for ADC.
- ▶ **Solution:** The analog input I/P2 is used and therefore address pins A,B,C should be 0,1,0 respectively to select I/P2. The OE and ALE pins are already kept at +5V to select the ADC and enable the outputs.
- ▶ Port C upper receives the EoC signal. Port C lower sends (output) SoC to the ADC.
- ▶ Port A acts as a 8-bit input data port to receive the digital data output from the ADC.

D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
1	0	0	1	1	0	0	0
IO mode	Mode 0		Port A input	Port C (up) input	Mode 0	Port B output	Port C (low) output

CWR is holding a value 98h

Interfacing Diagram

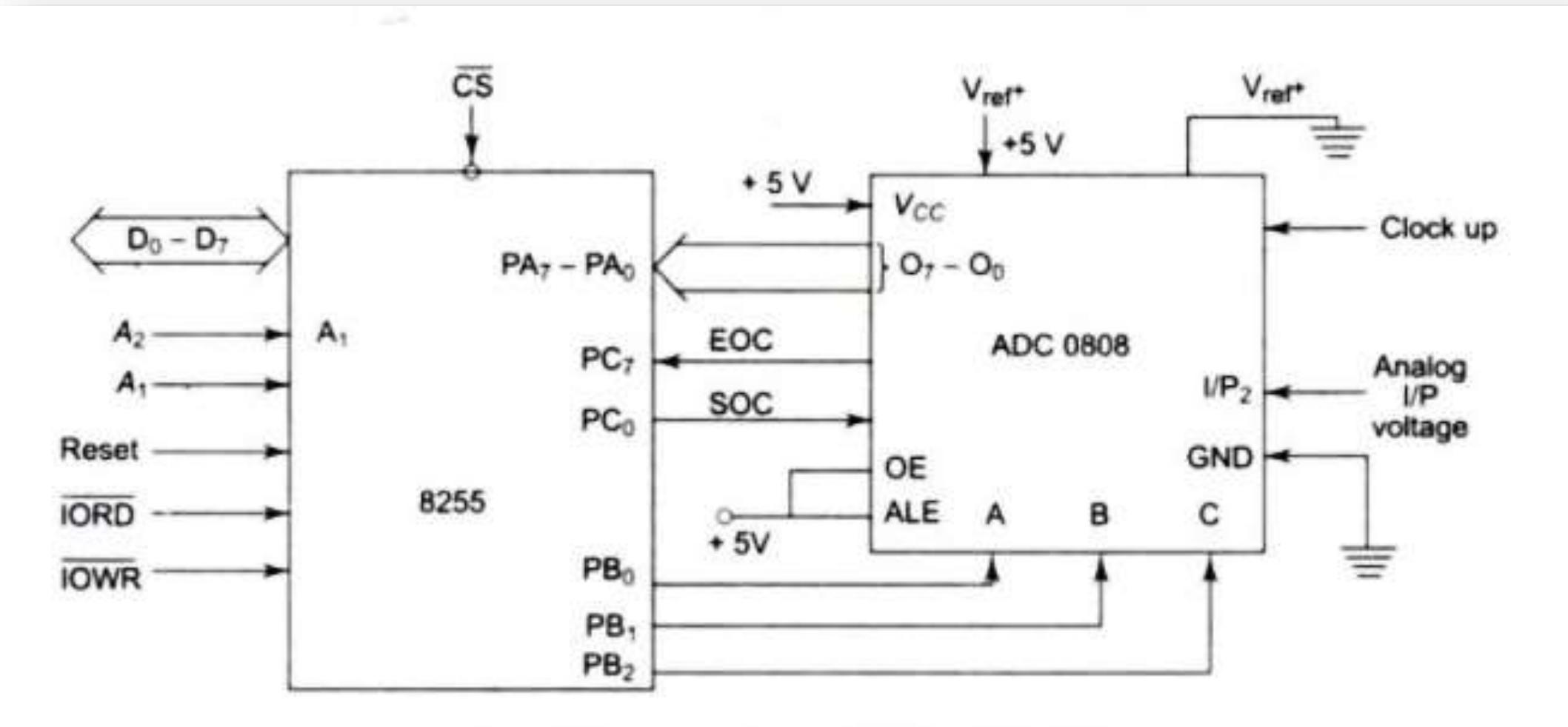


Image Courtesy: A. K. Ray Book

ALP to interface 8086 and 808

```
MOV AL, 98h      ; initialise 8255 as OUT
CWR, AL          ; discussed above.
MOV AL, 02h      ; Select I/P2 as analog input
OUT PortB, AL    ; PortB – Port address
MOV AL, 00h      ; Give SoC pulse to ADC
OUT PortC, AL    ; PortC – Port address
MOV AL, 01h
OUT PortC, AL
MOV AL, 00h
OUT PortC, AL

WAIT: IN AL, PortC
      RCR
      JNC WAIT
      IN AL, PortA
      HLT

; Check for EoC by
; reading port C upper and
; rotating through carry.
; If EoC, read digital equivalent in AL
; Stop.
```

Digital Analog Converters

- The digital to analog converters convert binary number into their equivalent voltages (analog).
- The DAC find applications in areas like digitally controlled gains, motors speed controls, programmable gain amplifiers etc. AD 7523
- 8-bit Multiplying DAC : This is a 16 pin DIP, multiplying digital to analog converter, containing R-2R ladder for D-A conversion along with single pole double thrown NMOS switches to connect the digital inputs to the ladder.

Digital Analog Converters (2)

- ▶ The supply range is from +5V to +15V, while V_{ref} may be anywhere between -10 V to +10 V. The maximum analog output voltage will be anywhere between -10 V to +10 V, when all the digital inputs are at logic high state.
- ▶ Usually a Zener is connected between OUT1 and OUT2 to save the DAC from negative transients. An operational amplifier is used as a current to voltage converter at the output of AD to convert the current output of AD to a proportional output voltage.
- ▶ It also offers additional drive capability to the DAC output.
- ▶ An external feedback resistor acts to control the gain. No need to connect any external feedback resistor, if no gain control is required.

Pin Diagram

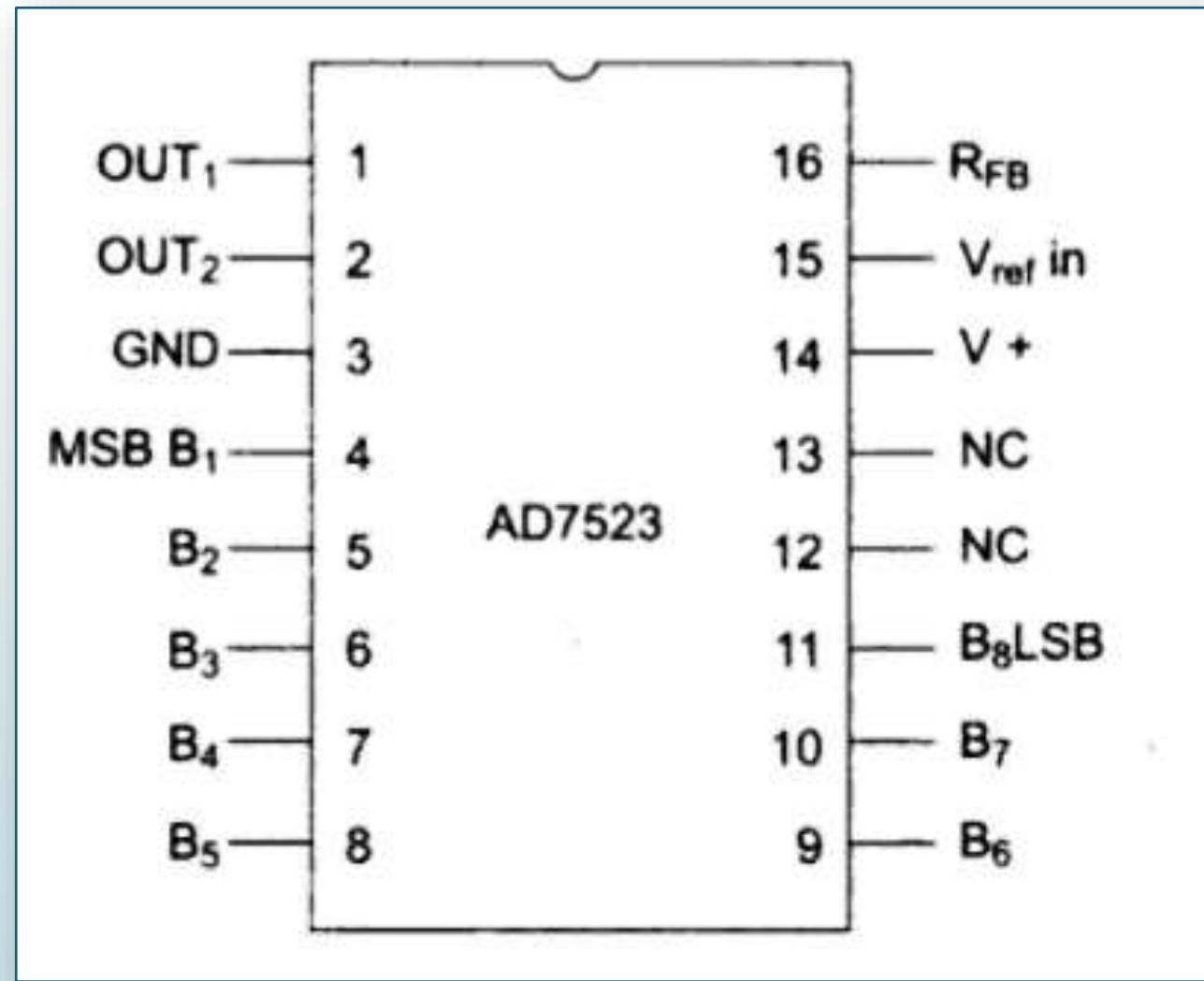
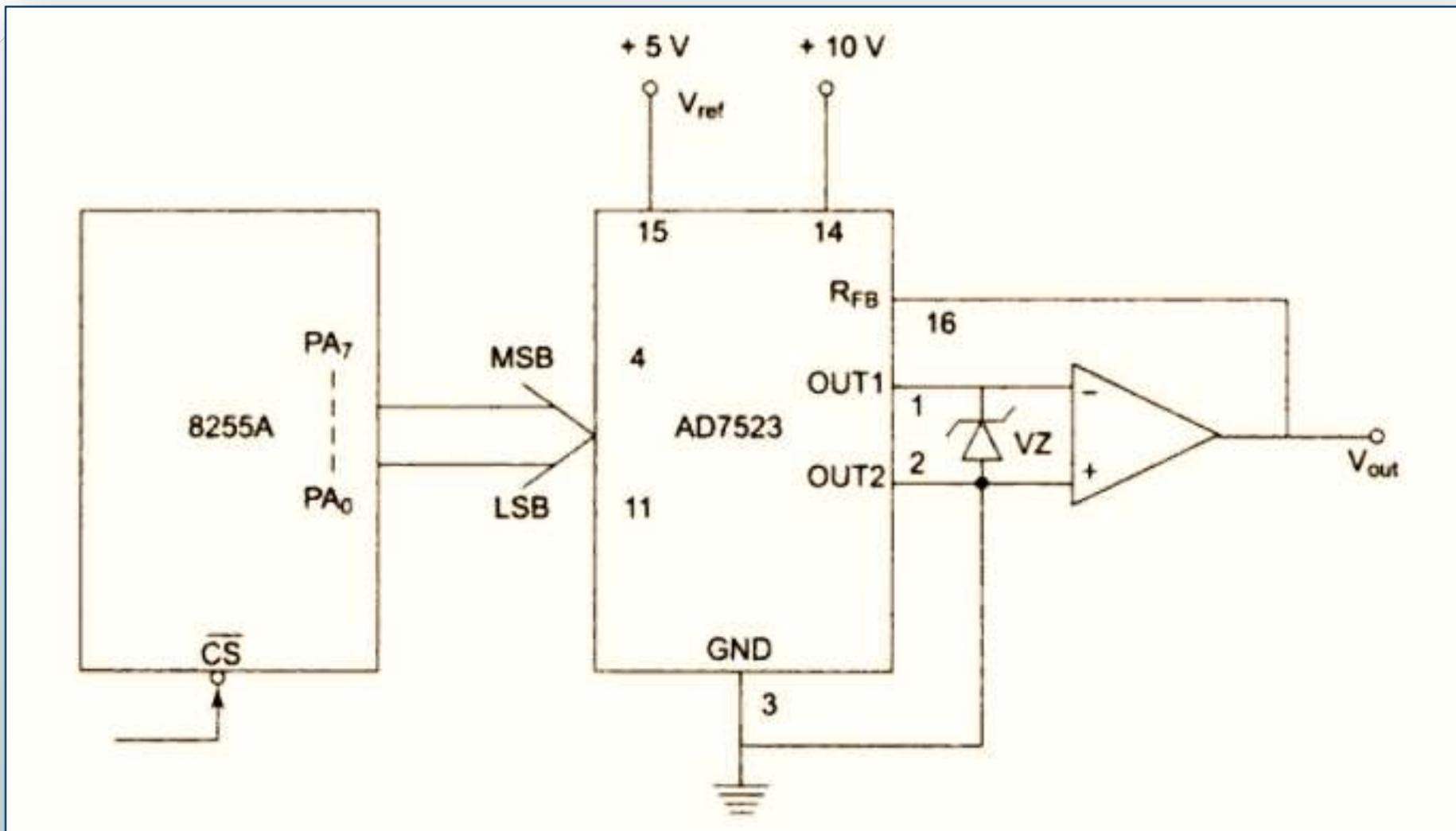


Image Courtesy: A.K. Ray book

8086 – AD7253 Interface Diagram



- EXAMPLE: Interfacing DAC AD7523 with an 8086 CPU running at 8 MHz and write an ALP to generate a sawtooth waveform of period 1 ms with V_{max} 5V.

ASSUME CS: CODE

CODE SEGMENT

START : MOV AL ,80h ;make all ports output
 OUT CWR, AL

AGAIN : MOV AL,00h ;start voltage for ramp

BACK : OUT PA, AL
 INC AL

CMP AL, OFFh

JB BACK

JMP AGAIN

CODE ENDS

END START

D₇	D₆	D₅	D₄	D₃	D₂	D₁	D₀
1	0	0	0	0	0	0	0
IO mode	Mode 0	Port A output	Port C (up) output	Mode 0	Port B output	Port C (low) output	

CWR is holding a value 80h

ALP - Explanation

- ▶ Port A is initialized as the output port for sending the digital data as input to DAC. The ramp starts from the 0 V (analog), hence AL starts with 00H.
- ▶ To increment the ramp, the content of AL is increased during each execution of loop till it reaches F2H.
- ▶ After that the saw tooth wave again starts from 00H, i.e. 0 V (analog) and the procedure is repeated.
- ▶ The ramp period given by this program is precisely 1.000625 msec.
- ▶ Here the count F2H has been calculated by dividing the required delay of 1ms by the time required for the execution of the loop once. The ramp slope can be controlled by calling a controllable delay after the OUT instruction.

Learning Resource

[1] K. M. Bhurchandi and A. K. Ray, "Advanced Microprocessors and Peripherals – with ARM and an Introduction to Microcontrollers and Interfacing", Tata McGraw Hill, 3rd ed., 2015.

Note: Almost all figures and text content taken from the above stated book.



Thank You

18ECC203J – Module 3

8086 Interfacing with Memory and Programmable Devices

S – 6, 7, 8

Prepared by,

Dr. R. Prithiviraj

Dr. Diwakar R. Marur

2

S – 6

Stepper Motor interfacing

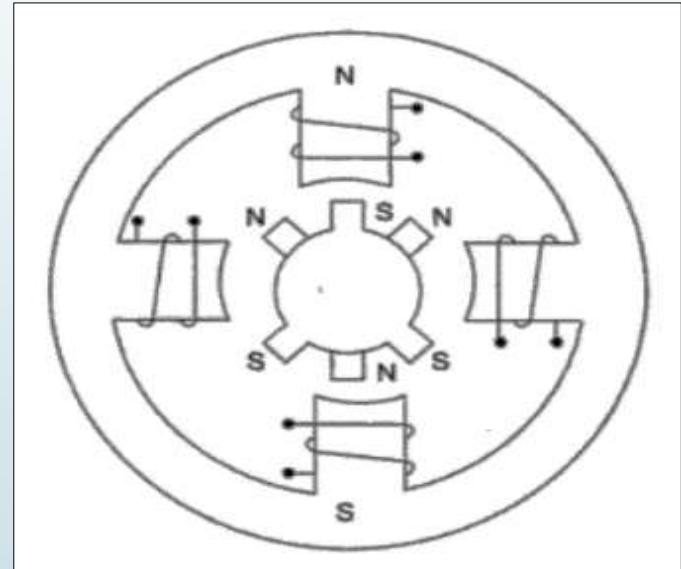
Stepper Motor Interfacing

- ▶ A stepper motor is a device to obtain an accurate position control of rotating shaft. Rotation of shaft takes place in terms of steps unlike AC or DC motors.
- ▶ To rotate the shaft, sequences of pulses are applied to the windings of the stepper motor, in a sequence.
- ▶ No of pulses required for one complete rotation of the shaft of the stepper motor is equivalent to number of teeth on its rotor.
- ▶ When the rotor teeth and stator teeth lock with each other to fix a shaft in a position
- ▶ When a pulse applied to the winding, the rotor rotates by one tooth or an angle x .

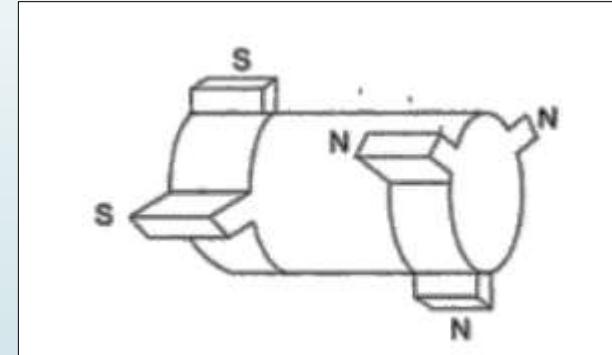
$$x = \frac{360^\circ}{\text{no. of rotor teeth}} \quad \dots \quad (1)$$

Stepper Motor Interfacing (2)

- After rotation of the shaft through angle x , the rotor locks itself with the next tooth in the sequence on the internal surface of stator.



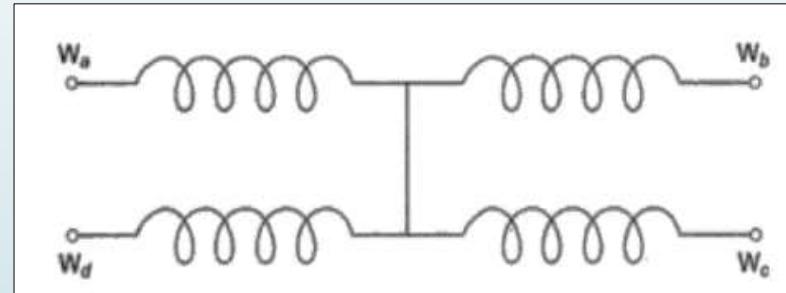
Internal Schematic of a four winding Stepper motor



Schematic of a stepper motor rotor with six teeth on its surface

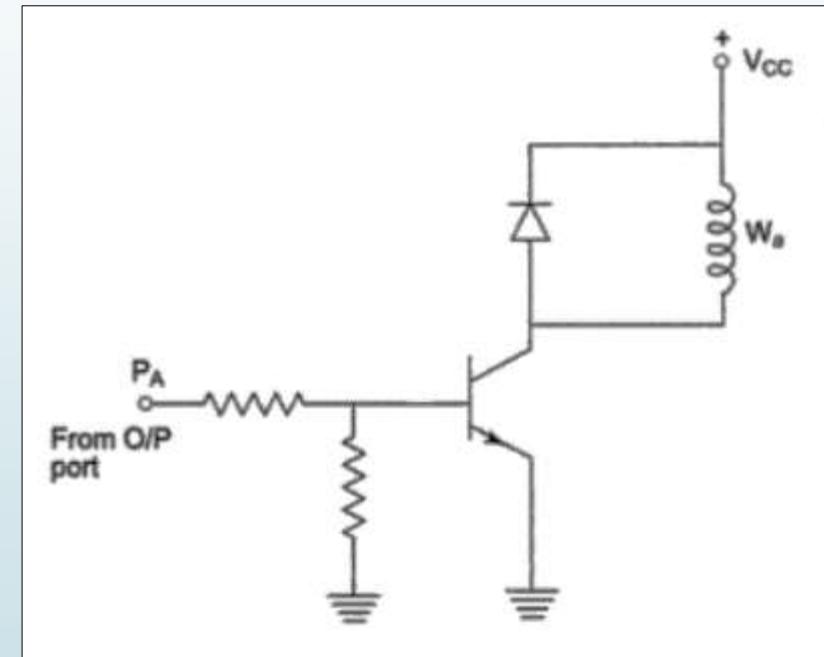
Winding Information

Stepper motors are designed to work with digital circuits. Binary level pulses (0-5 V) are applied to energize the windings.



Winding arrangement of stepper motor

Image Courtesy: Adv. μP by A.K. Ray



Interfacing Stepper Motor Winding W_a
Image Courtesy: Adv. μP by A.K. Ray

Types of Schemes

- ▶ Pulse sequence is decided by the required motion of the shaft.
- ▶ Types of schemes
 - Wave Scheme
 - Full Step Scheme
 - Half Step Scheme
- ▶ **Wave Scheme**
 - A simple scheme to rotate the shaft of stepper motor.
 - Here W_a , W_b , W_c , and W_d are applied with the required voltage pulses, in cyclic fashion. To change the rotation in opposite direction give pulse sequence in reverse direction.
- ▶ **Full Step Scheme**
 - Here consecutive two windings are excited at a time. These are shifted only one position at a time.
- ▶ **Half Step Scheme**
 - Combination of Wave and Full Step scheme. Used for step angle reduction.

Table 1: Wave Winding

Motion	Step	A	B	C	D
Clockwise	1	1	0	0	0
	2	0	1	0	0
	3	0	0	1	0
	4	0	0	0	1
	5	1	0	0	0
Anticlockwise	1	1	0	0	0
	2	0	0	0	1
	3	0	0	1	0
	4	0	1	0	0
	5	1	0	0	0

Table 2: Full Step Winding

Motion	Step	A	B	C	D
Clockwise	1	0	0	1	1
	2	0	1	1	0
	3	1	1	0	0
	4	1	0	0	1
	5	0	0	1	1
Anticlockwise	1	0	0	1	1
	2	1	0	0	1
	3	1	1	0	0
	4	0	1	1	0
	5	0	0	1	1

Operation of Stepper Motor

Stepper motor contains Permanent Magnet (rotor) and electromagnet Stator, with one-phase-on configuration.

In the top left figure, North pole of rotor is attracted by South pole of A+ electromagnet. South pole of rotor is attracted by North pole of A+ electromagnet.

A and B are stator poles.

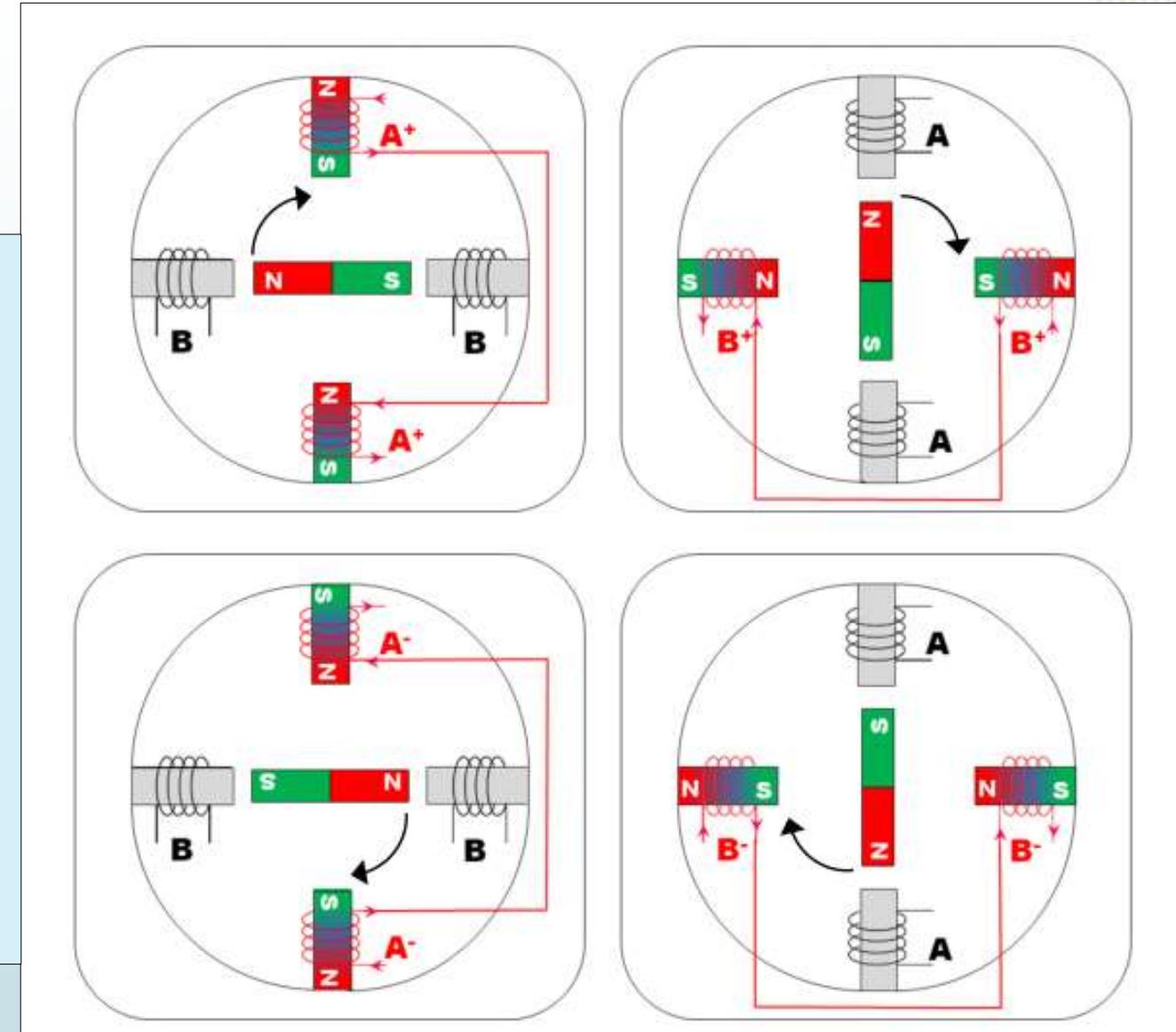
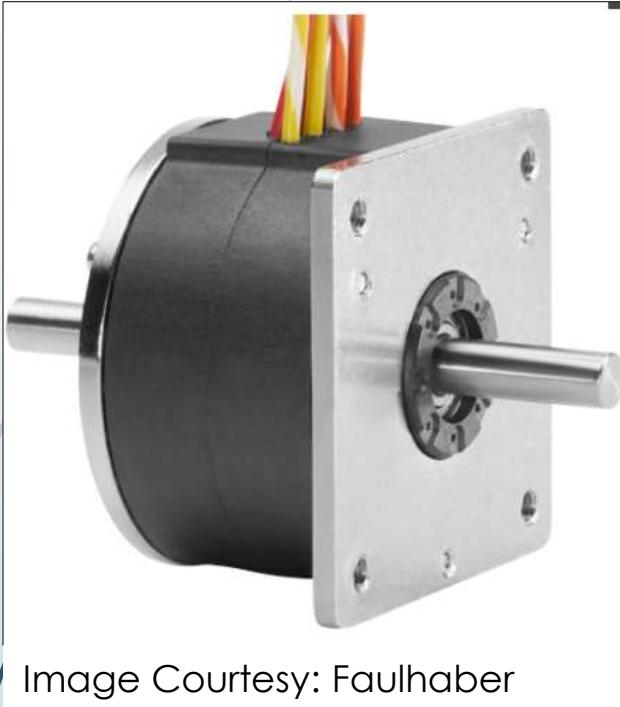


Image Courtesy: Faulhaber Brochure [1]

Typical Stepper Motor



A typical stepper motor may have parameters like torque 3 kg-cm, operating voltage 12 V, current rating 0.2 A and a step angle 1.8°.

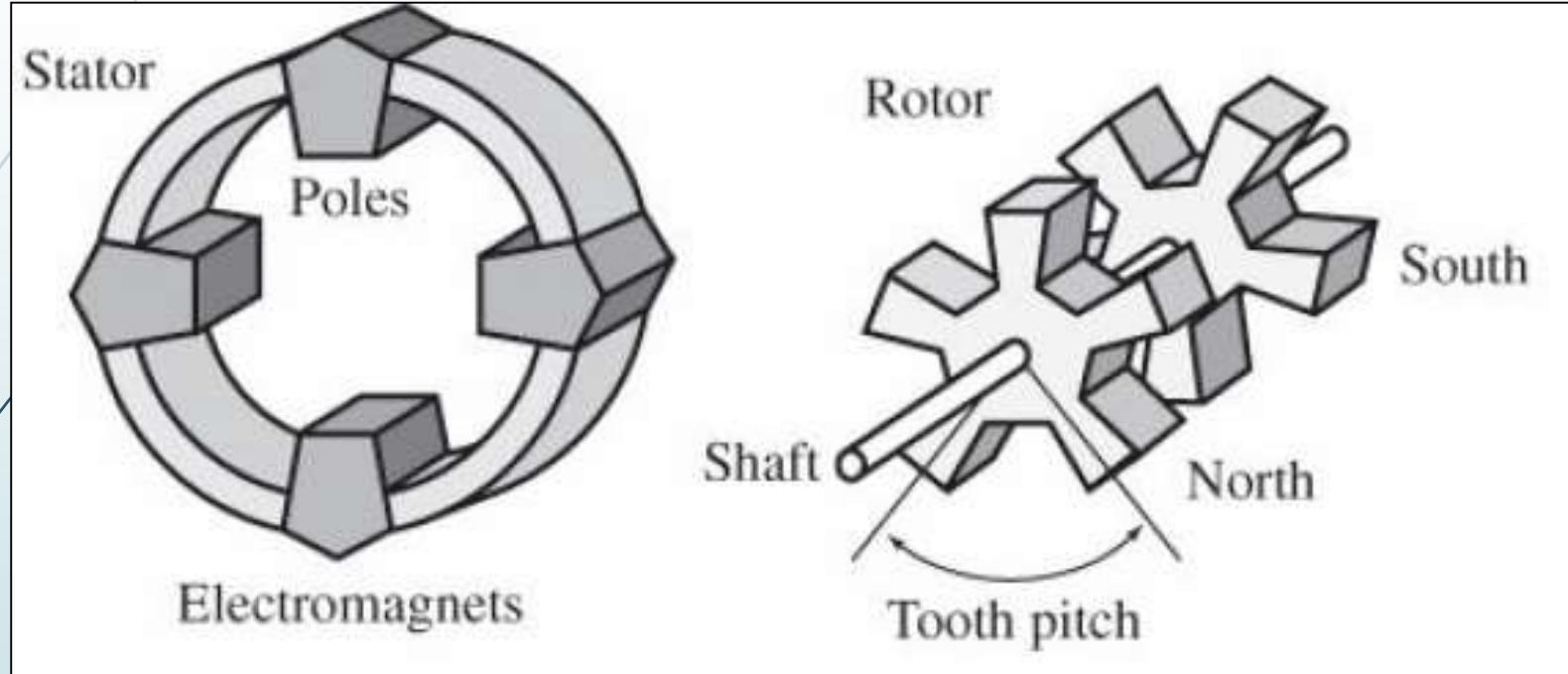
The number of rotor teeth is equal to the count for one rotation, i.e. 360°. For any specified angle θ° the count (C) is calculated as:

$$C = \frac{\text{Number of rotor teeth}}{360^\circ} \times \theta^\circ$$

Reference

- [1] https://www.faulhaber.com/fileadmin/user_upload_global/support/MC_Support/Motors/AppNotes/Faulhaber_AN001_EN.pdf ~ Interesting and well written article

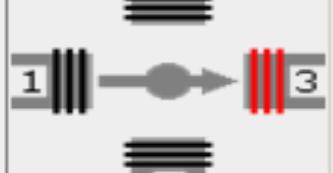
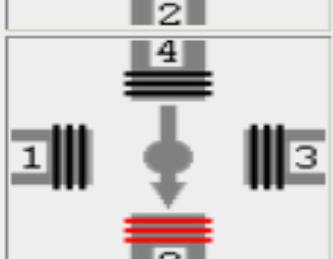
From Other Source (1/5)



Rotors invariably made up of permanent magnet

Image Courtesy: Mrs. Suganthi Brindha G., In turn Google

From Other Source (2/5)

Step	Coil 4	Coil 3	Coil 2	Coil 1	
a.1	on	off	off	off	
a.2	off	on	off	off	
a.3	off	off	on	off	

Single Coil Excitation.

Excited coil is shown in red colour

Image Courtesy: Mrs. Suganthi Brindha G., In turn Google

From Other Source (3/5)

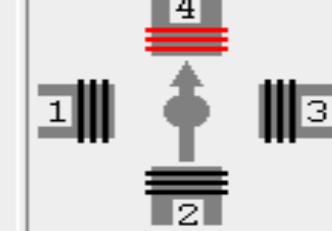
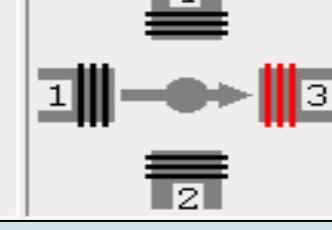
Step	Coil 4	Coil 3	Coil 2	Coil 1	
b.1	on	on	off	off	
b.2	off	on	on	off	
b.3	off	off	on	on	

TWO Coil Excitation.

Each successive pair of adjacent coils is energized in turn.

Image Courtesy: Mrs. Suganthi Brindha G., In turn Google

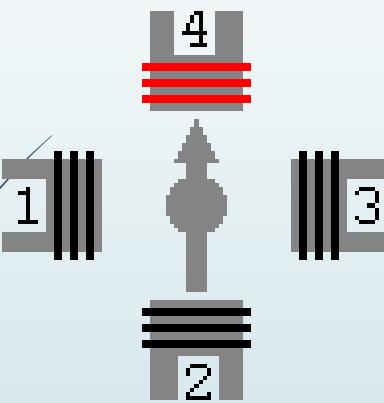
From Other Source (4/5)

Step	Coil 4	Coil 3	Coil 2	Coil 1	
a.1	on	off	off	off	
b.1	on	on	off	off	
a.2	off	on	off	off	

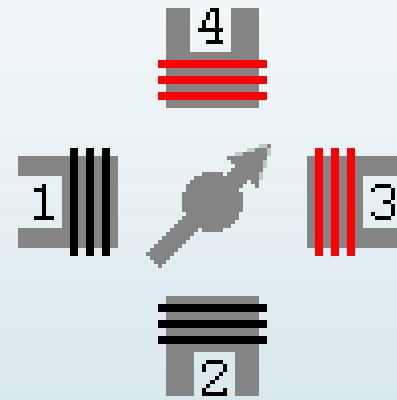
HALF Step Sequence.
 2 sequences interleaved.
 normal (4 step) + wave drive (4 step)
 Total 8 steps.

Image Courtesy: Mrs. Suganthi Brindha G., In turn Google

From Other Source (5/5)

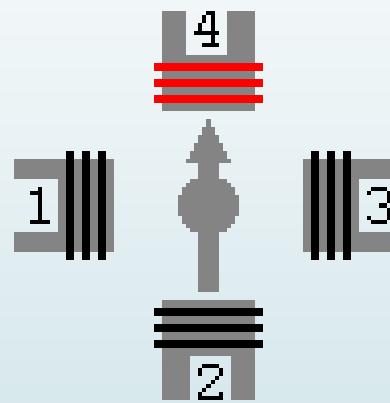


Single-Coil Excitation



Two-Coil Excitation

Interleaved Single- and Two-Coil Excitation



Half-Stepping

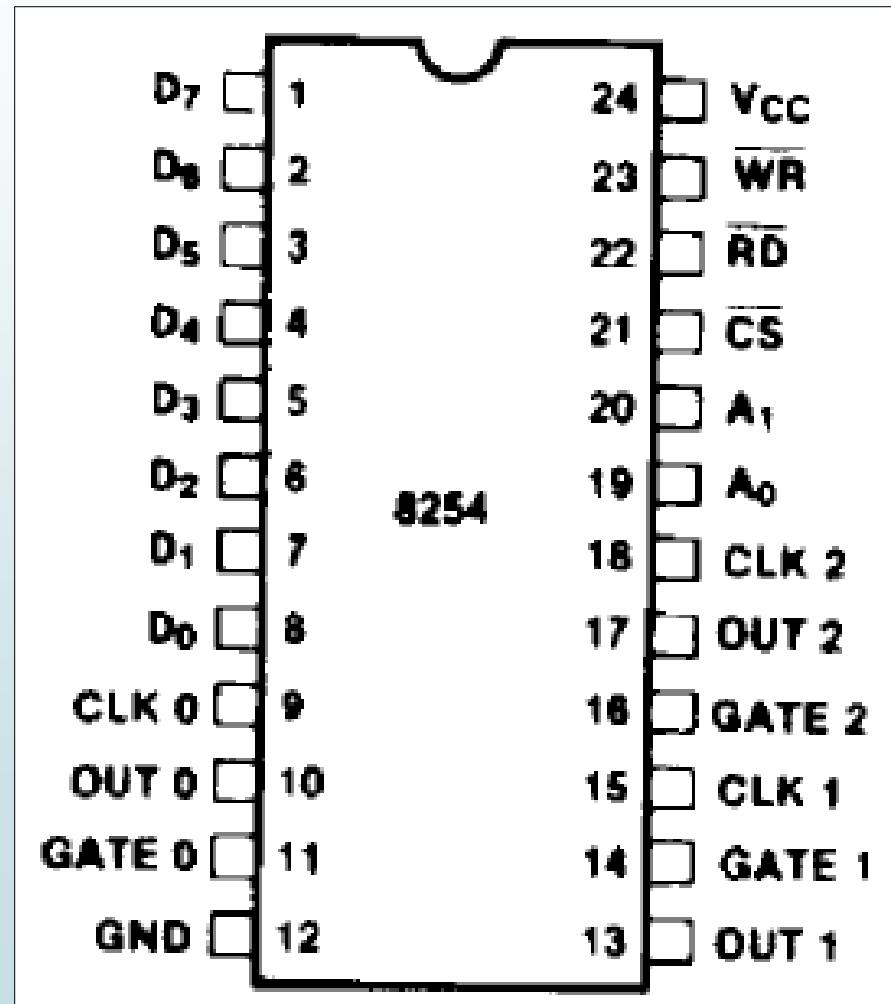
S – 7

Programmable Interval Timer 8254 & Interfacing
8254 with 8086 and programming

Features of 8254

- ▶ Three Independent 16-Bit Counters,
- ▶ Clock input up to 10 MHz,
- ▶ Status Read-Back Command,
- ▶ Six Programmable Counter Modes,
- ▶ Binary or BCD Counting,
- ▶ Single +5V Supply,
- ▶ Superset of PIT-8253.

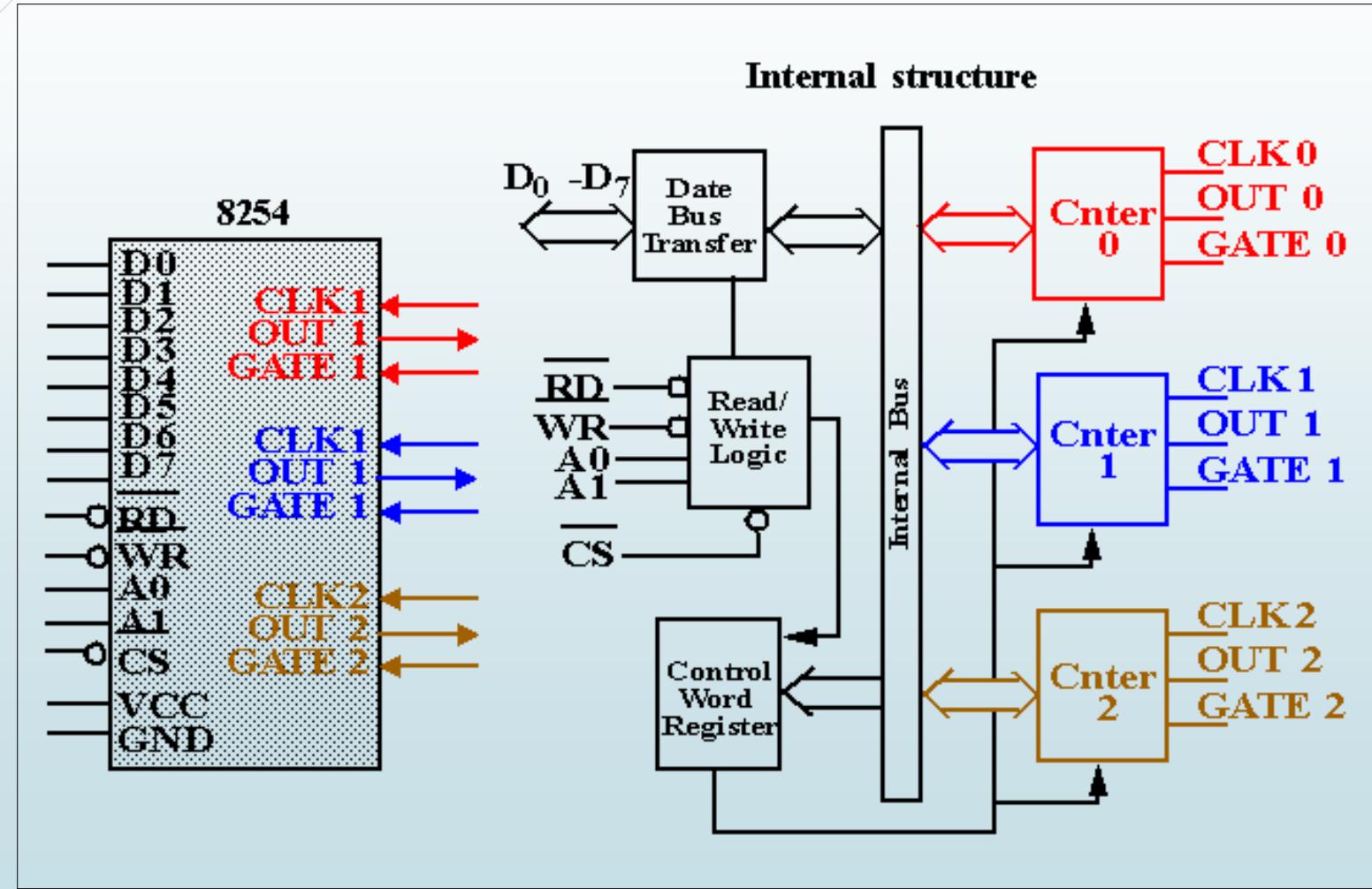
Pin Diagram



Pin Description

Symbol	Pin No.	Type	Name and Function
D ₇ -D ₀	1-8	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.
OUT 0	10	O	OUTPUT 0: Output of Counter 0.
GATE 0	11	I	GATE 0: Gate input of Counter 0.
GND	12		GROUND: Power supply connection.
V _{CC}	24		POWER: + 5V power supply connection.
WR	23	I	WRITE CONTROL: This input is low during CPU write operations.
RD	22	I	READ CONTROL: This input is low during CPU read operations.
CS	21	I	CHIP SELECT: A low on this input enables the 8254 to respond to RD and WR signals. RD and WR are ignored otherwise.
A ₁ , A ₀	20-19	I	ADDRESS: Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.
Selects			
	0	0	Counter 0
	0	1	Counter 1
	1	0	Counter 2
	1	1	Control Word Register
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.
OUT 2	17	O	OUT 2: Output of Counter 2.
GATE 2	16	I	GATE 2: Gate input of Counter 2.
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.
GATE 1	14	I	GATE 1: Gate input of Counter 1.
OUT 1	13	O	OUT 1: Output of Counter 1.

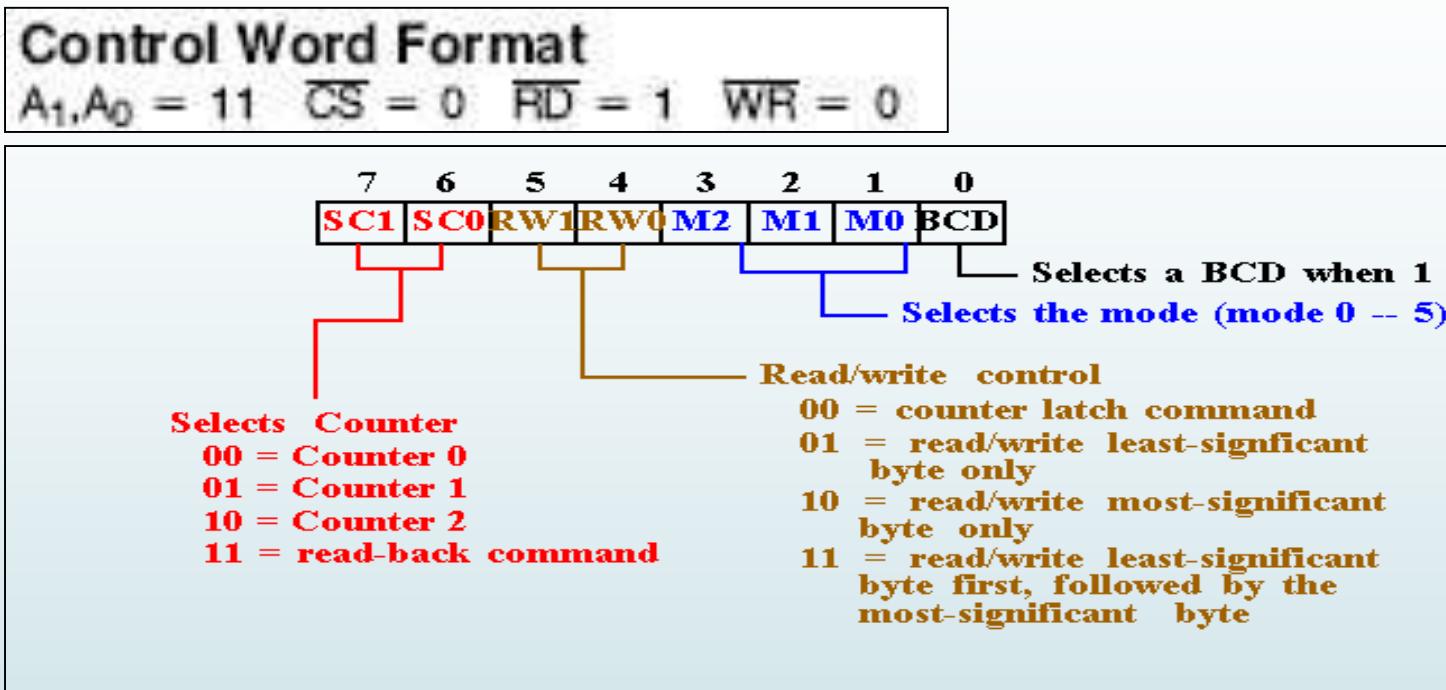
Block Diagram of 8254



Internal Blocks of Counter

- ▶ Count Register (CR) to store count (CRL & CRM),
- ▶ Counting elements (CE) are used for counting,
- ▶ Output Latch (OLL & OLM) to latch the count in CE,
- ▶ The Control Word Register is not part of the Counter itself, but its contents determine how the Counter operates.
- ▶ The status register, when latched, contains the current contents of the Control Word Register and status of the output and null count flag.

Control Word format



8254 Programming

- ▶ Each counter is individually programmed by writing a control word, followed by the initial count.
- ▶ The control word allows the programmer to select the counter, mode of operation, binary or BCD count and type of operation (read/write).

Interleaved Read and Write Operations

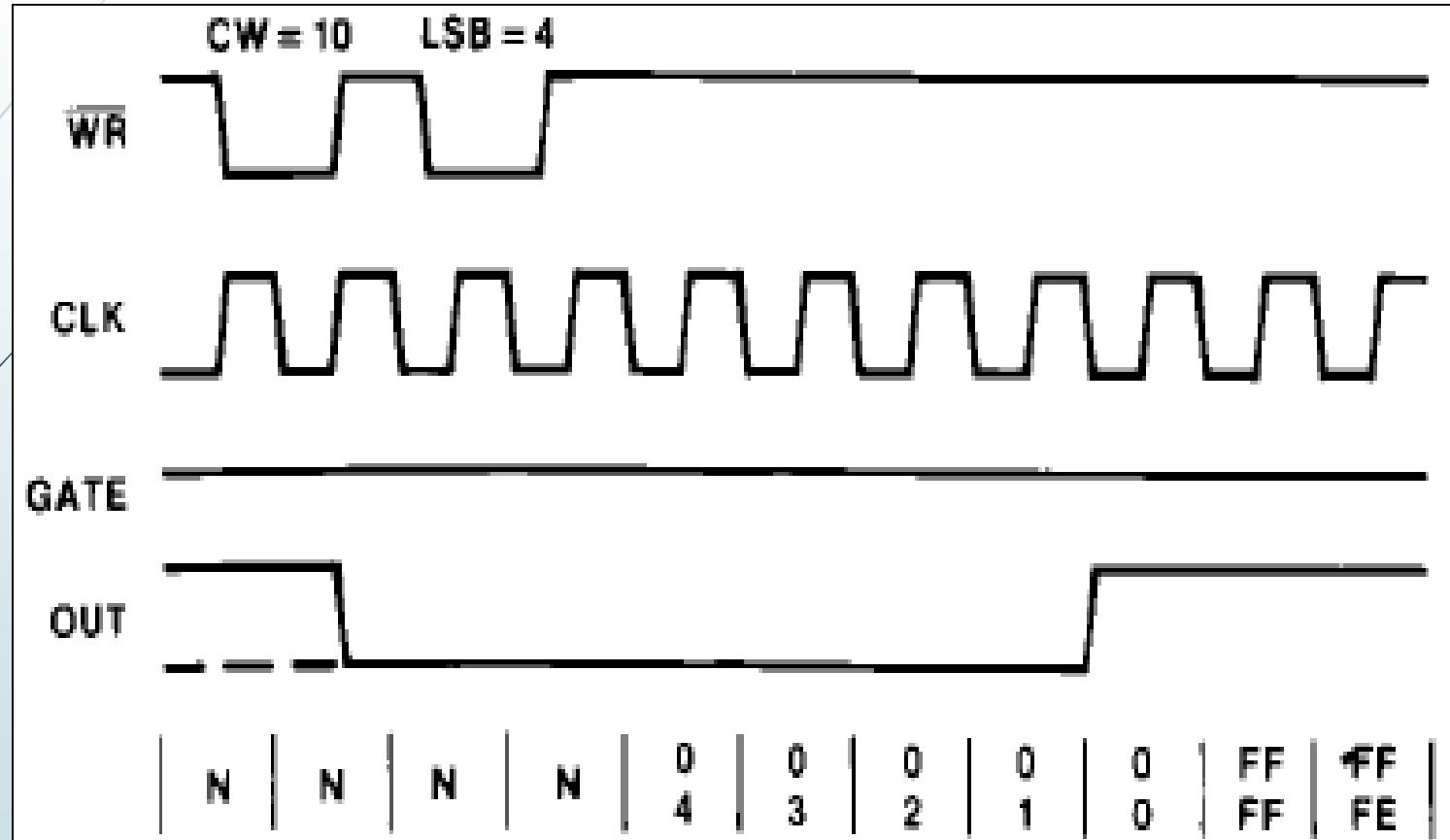
Valid sequence for read and write of the same counter set for two byte count:

1. Read least significant byte,
2. Write new least significant byte,
3. Read most significant byte,
4. Write new most significant byte.

6 Modes of 8254

- ▶ Mode 0: Interrupt On Terminal Count
- ▶ Mode 1: Hardware Retriggerable One-shot
- ▶ Mode 2: Rate Generator
- ▶ Mode 3: Square Wave Mode
- ▶ Mode 4: Software Triggered Strobe
- ▶ Mode 5: Hardware Triggered Strobe (Retriggerable)

MODE 0 – Interrupt on Terminal Count

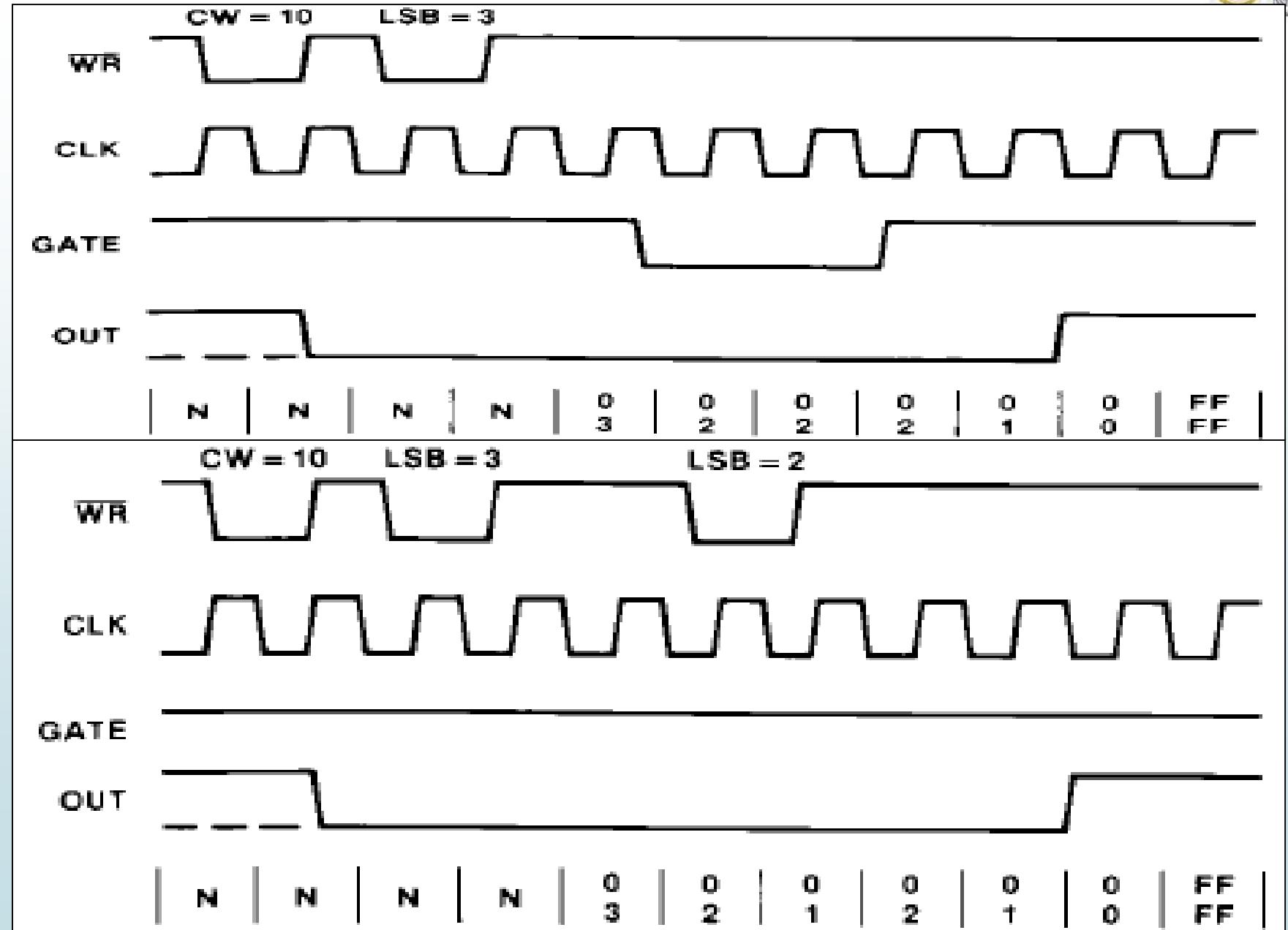


N : Undefined Count

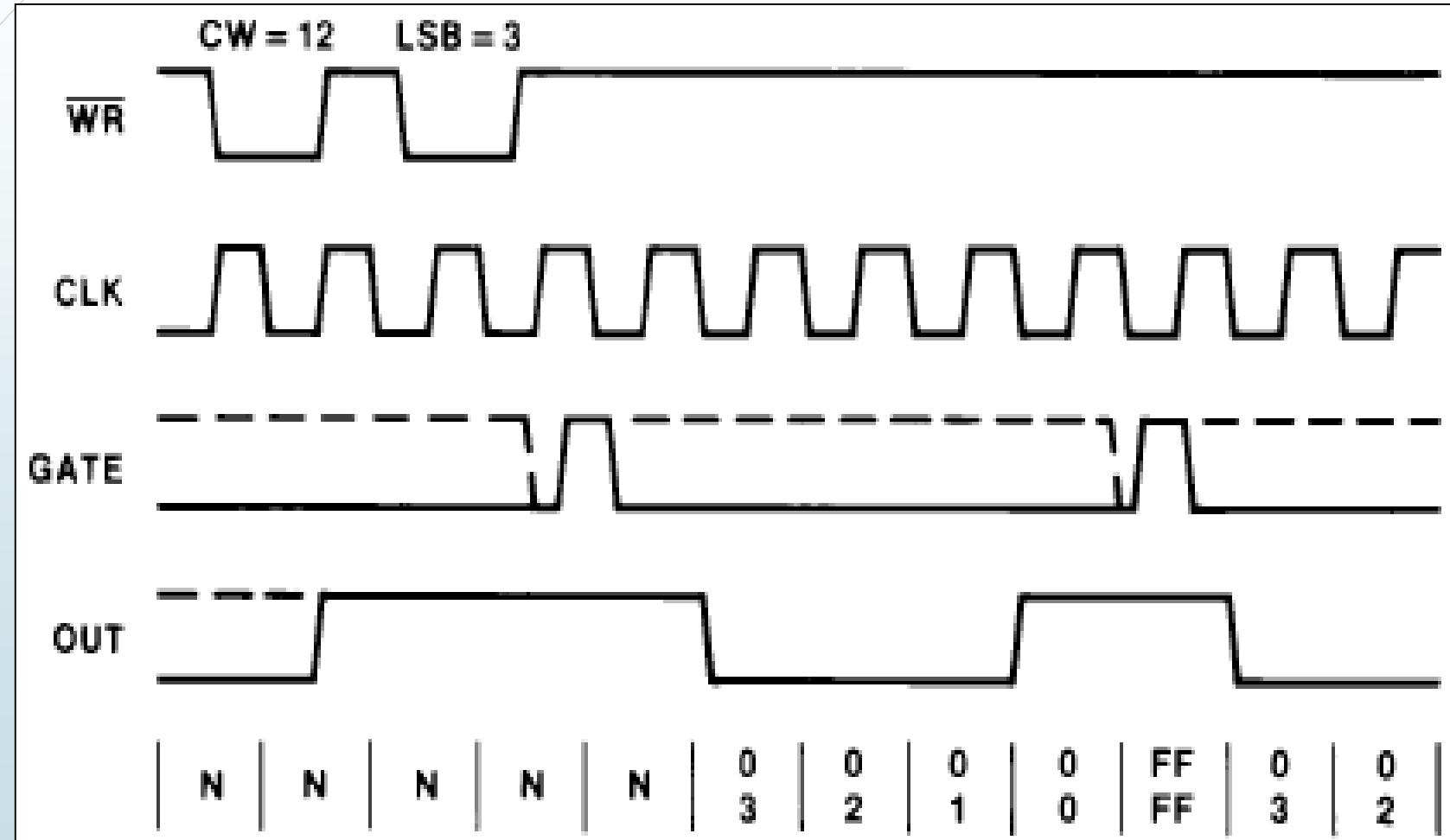
26

MODE 0

contd...

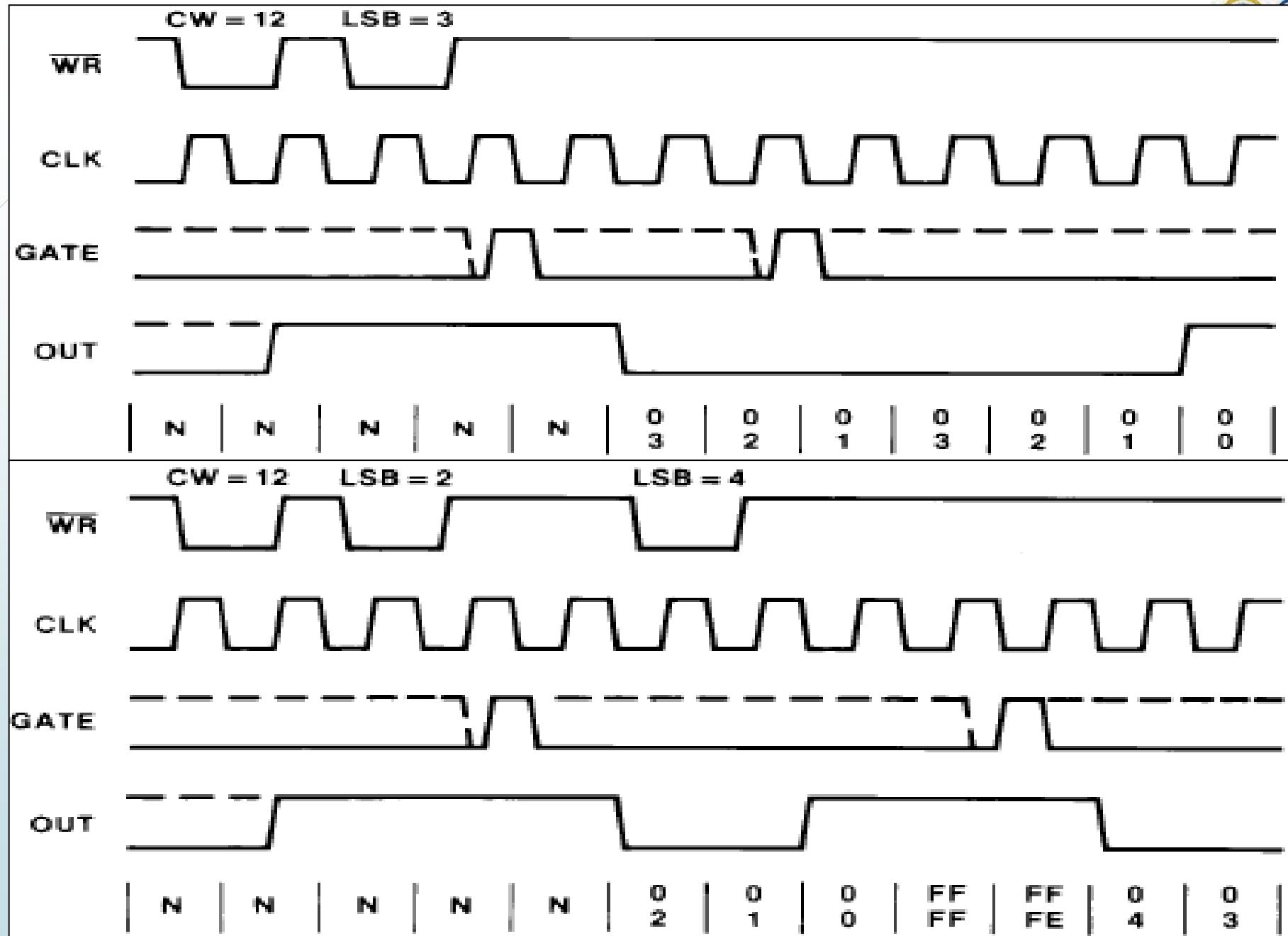


MODE 1: Hardware Retriggerable One Shot.

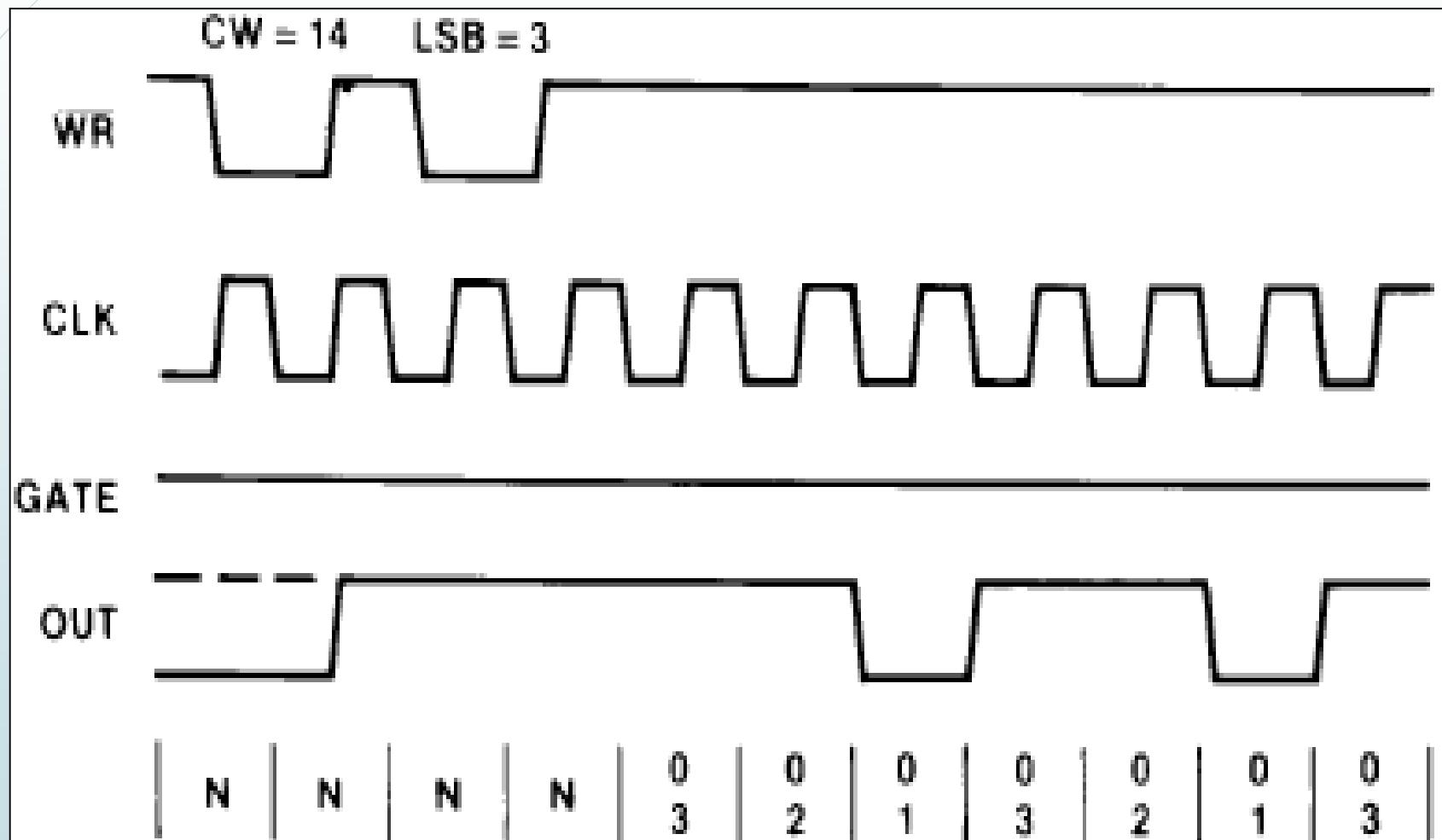


MODE 1

contd...

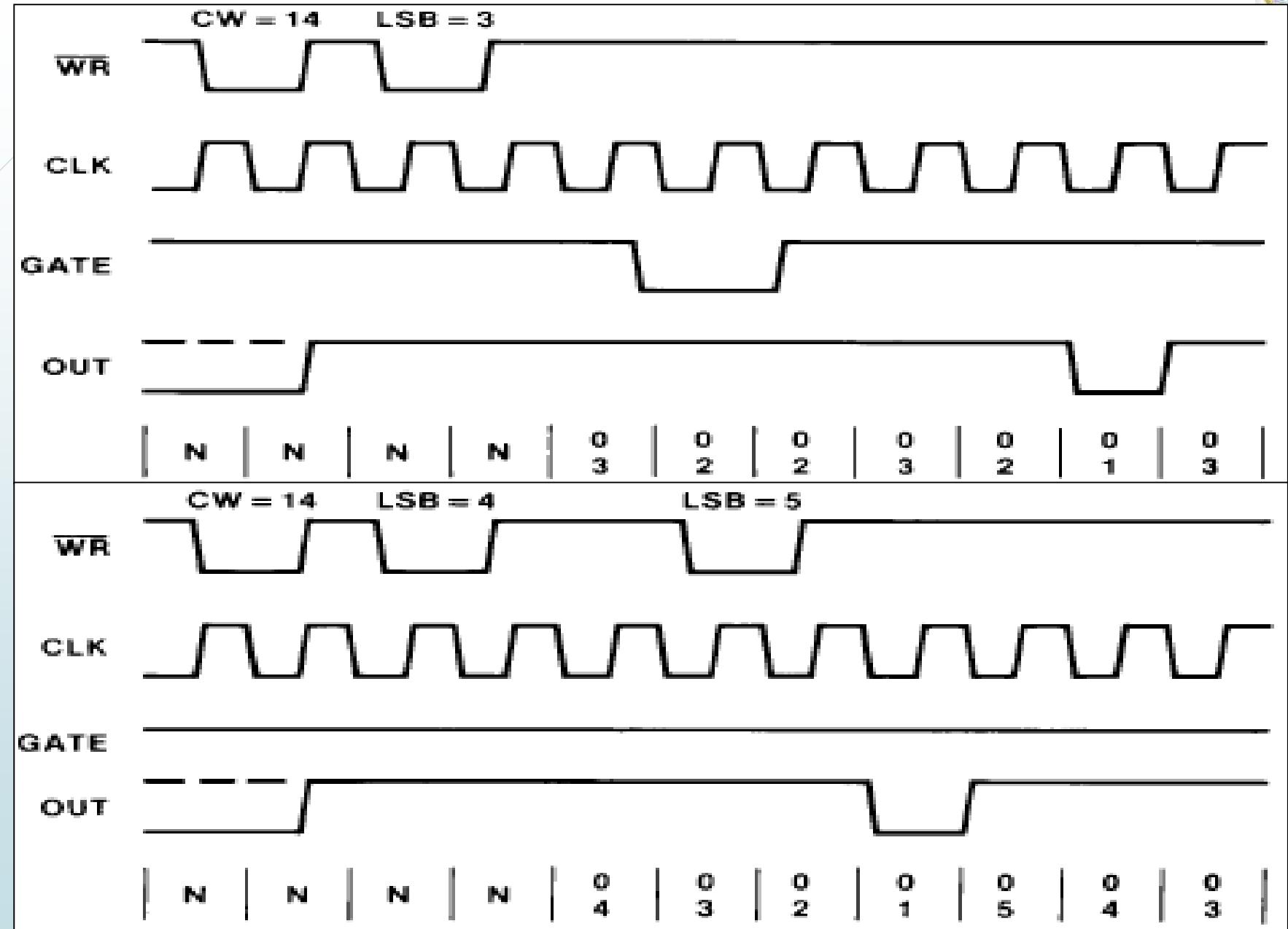


MODE 2: Rate Generator

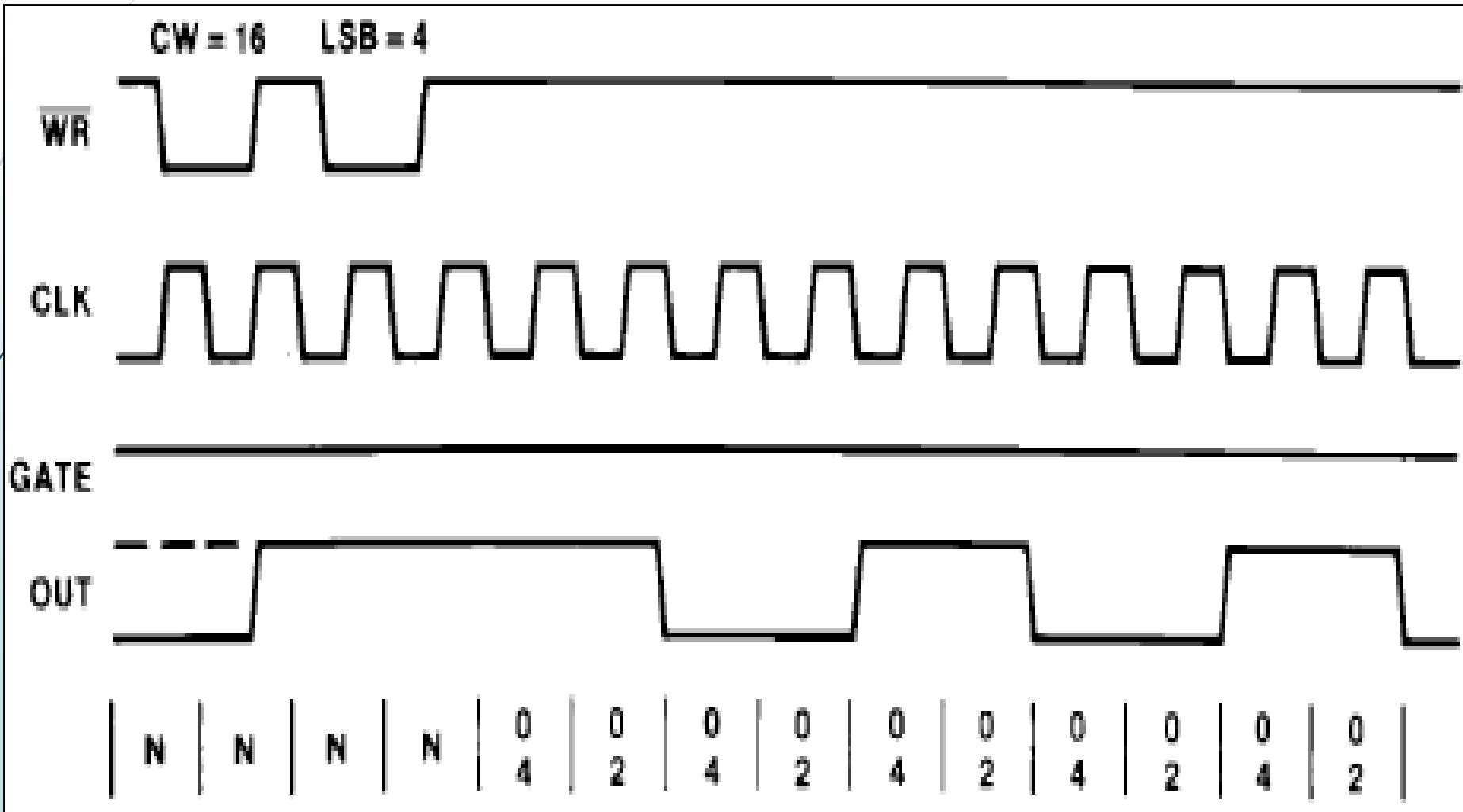


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MODE 2 contd...

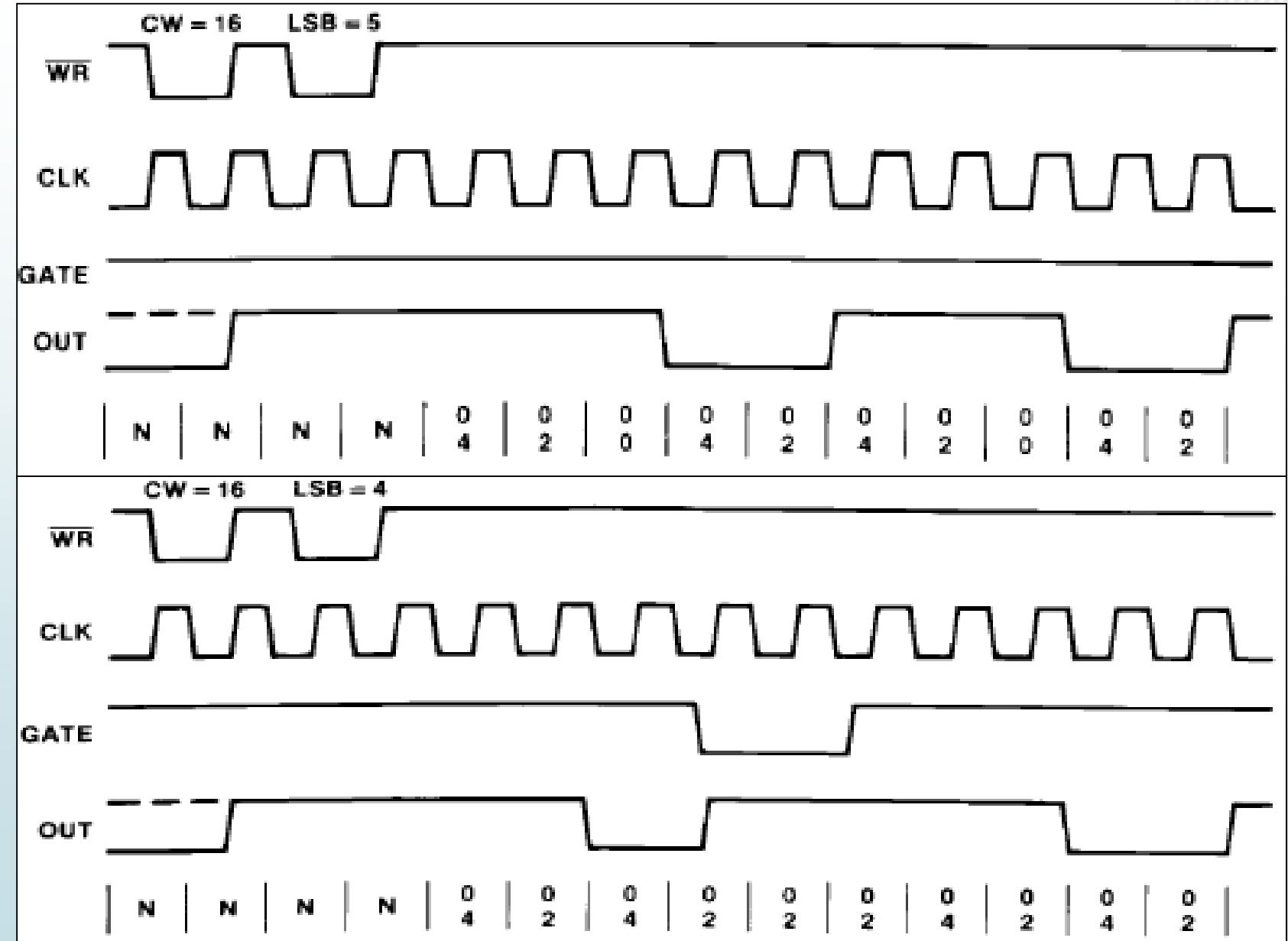


MODE 3: Square Wave Mode

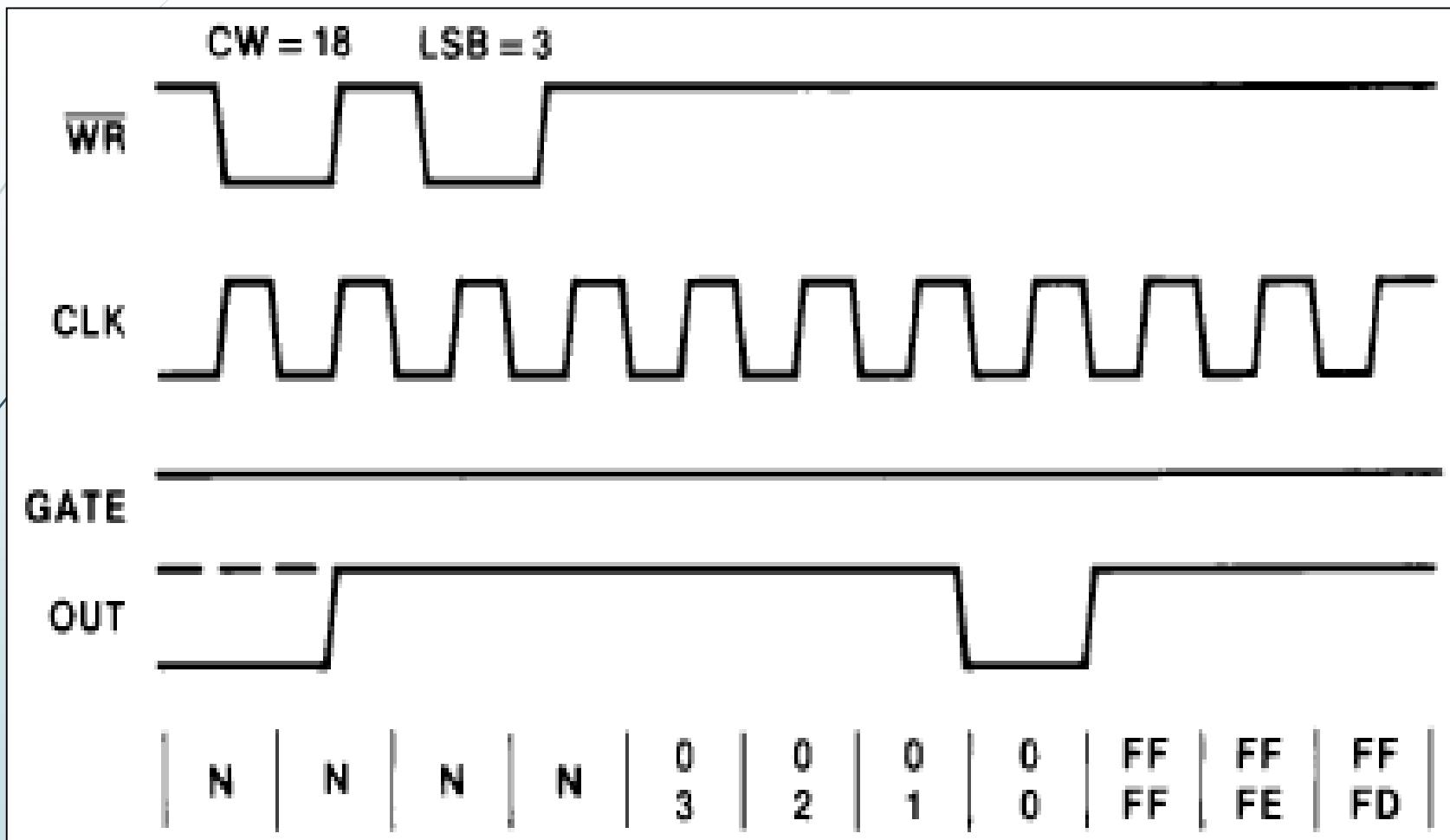


32

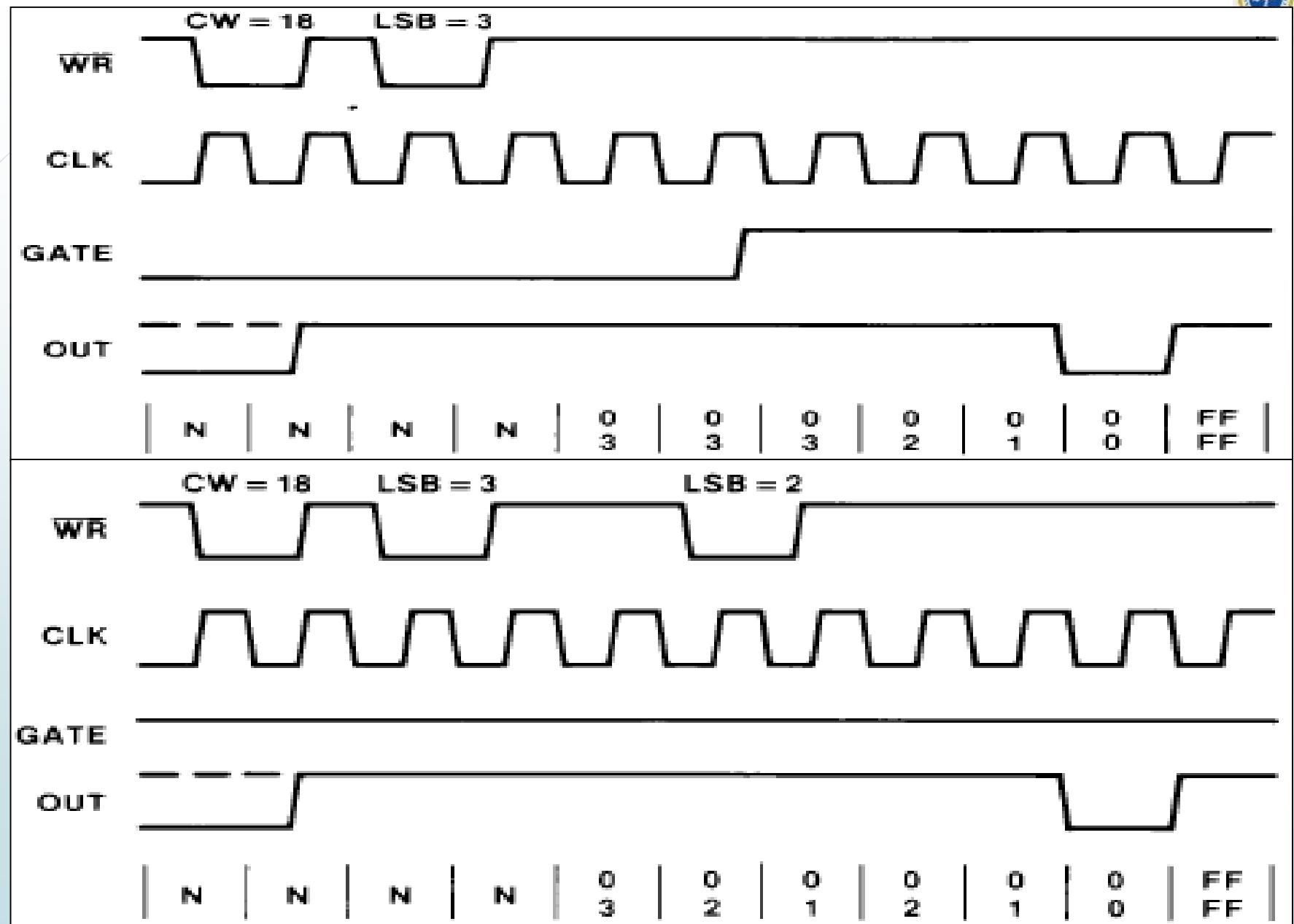
MODE 3 contd...



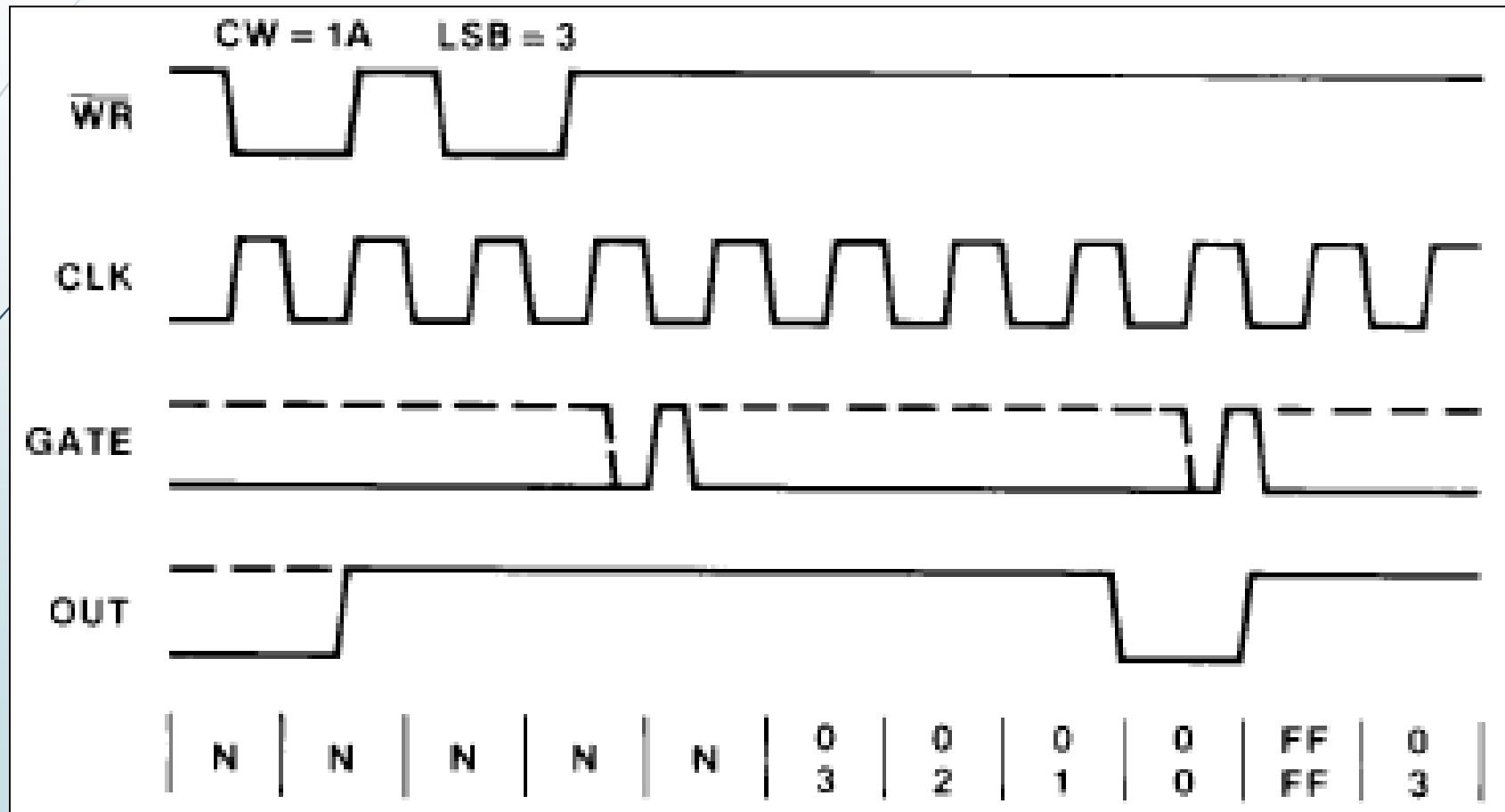
MODE 4: Software Triggered Strobe



MODE 4 contd...

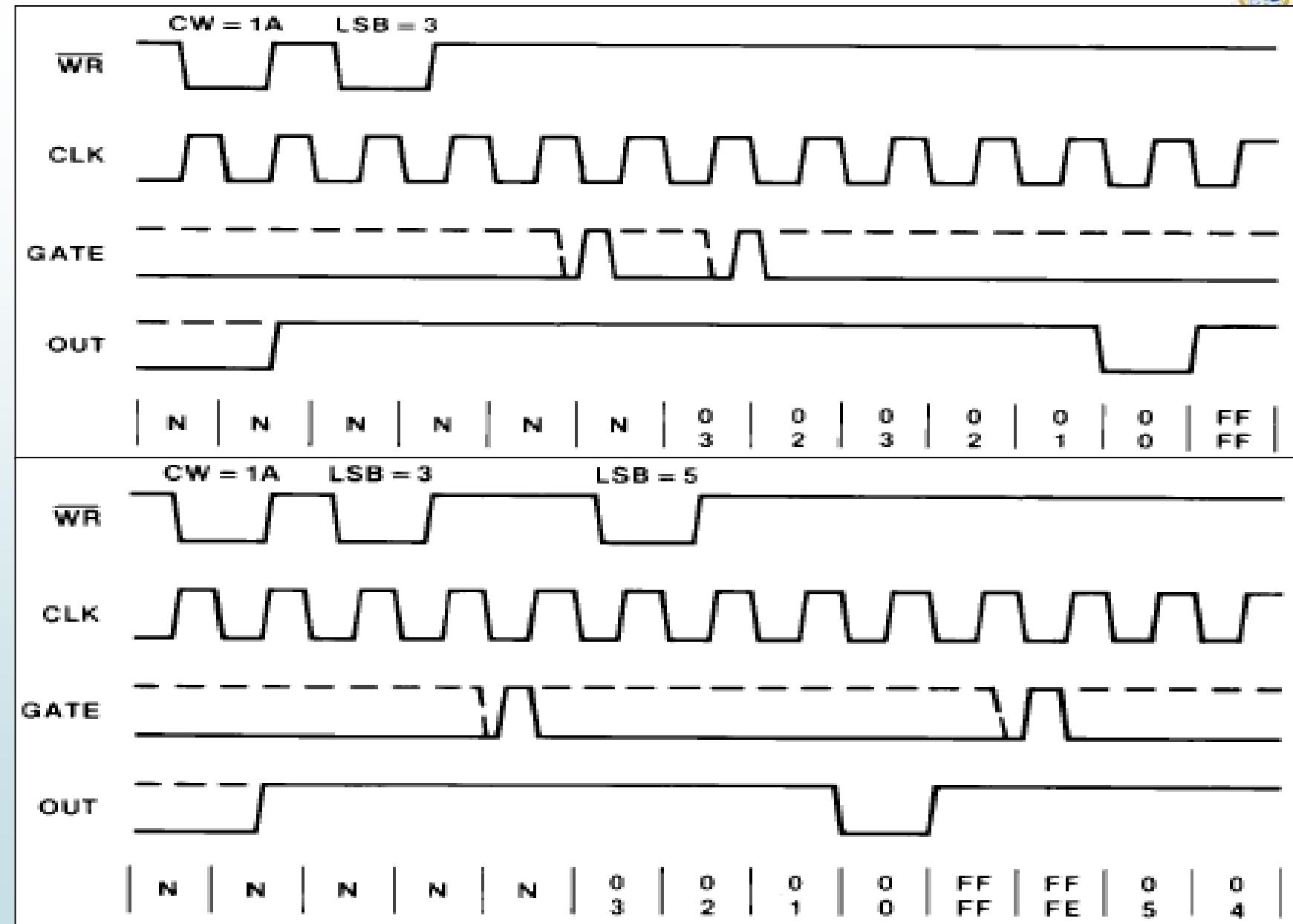


MODE 5 : Hardware Triggered Strobe



MODE 5

contd...



8254

contd...

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables Counting	— —	Enables Counting
1	— —	1) Initiates Counting 2) Resets Output after Next Clock	— —
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	— —	Enables Counting
5	— —	Initiates Counting	— —

Figure 21. Gate Pin Operations Summary

8254

contd...

CS	RD	WR	A ₁	A ₀	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Figure 14. Read/Write Operations Summary

Minimum & Maximum Initial Count

Mode	Min Count	Max Count
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE:

0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Gate Pin Operations Summary

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables Counting	— —	Enables Counting
1	— —	1) Initiates Counting 2) Resets Output after Next Clock	— —
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	— —	Enables Counting
5	— —	Initiates Counting	— —

Applications of 8254

- ▶ Real time clock
- ▶ Event-counter
- ▶ Digital one-shot
- ▶ Programmable rate generator
- ▶ Square wave generator
- ▶ Binary rate multiplier
- ▶ Complex waveform generator
- ▶ Complex motor controller

S – 8

Programmable Interrupt Controller 8259 &
Interfacing 8259 with 8086 and programming

Programmable Interrupt Controller 8259

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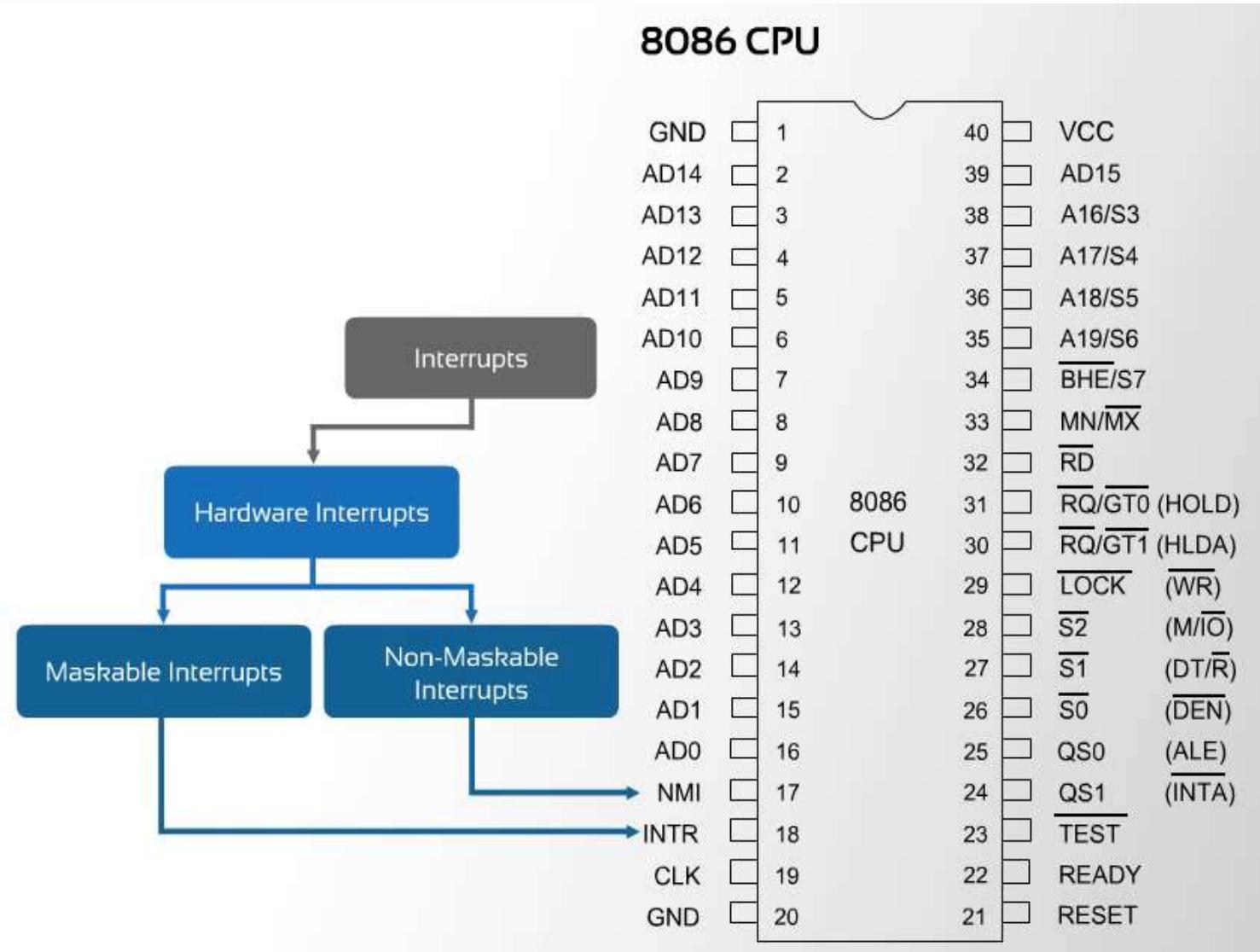


Image Courtesy: Google

8259 Programmable Interrupt Controller (PIC)

1. This IC is designed to simplify the implementation of the interrupt interface in the 8088 and 8086 based microcomputer systems.
2. This device is known as a 'Programmable Interrupt Controller' or PIC.
3. It is manufactured using the NMOS technology and It is available in 28-pin DIP.
4. The operation of the PIC is programmable under software control (Programmable)and it can be configured for a wide variety of applications.
5. 8259A is treated as peripheral in a microcomputer system.
6. 8259A PIC adds eight vectored priority encoded interrupts to the microprocessor.

8259 Programmable Interrupt Controller (PIC) (2)

7. This controller can be expanded without additional hardware to accept up to 64 interrupt request inputs. This expansion required a master 8259A and eight 8259A slaves.
8. Some of its programmable features are:
 - ▶ The ability to accept level-triggered or edge-triggered inputs.
 - ▶ The ability to be easily cascaded to expand from 8 to 64 interrupt-inputs.
 - ▶ Its ability to be configured to implement a wide variety of priority schemes.

Assignment of Signals for 8259

1. $D_7 - D_0$ - Connected to microprocessor data bus ($AD_7 - AD_0$).
2. $IR_7 - IR_0$ - Interrupt Request inputs are used to request an interrupt and to connect to a slave in a system with multiple 8259As.
3. \overline{WR} - the write input connects to write strobe signal of microprocessor.
4. \overline{RD} - the read input connects to the IORC signal.
5. INT - the interrupt output connects to the INTR pin on the microprocessor from the master, and is connected to a master IR pin on a slave.
6. \overline{INTA} - the interrupt acknowledge is an input that connects to the INTA signal on the system. In a system with a master and slaves, only the master INTA signal is connected.

Assignment of Signals for 8259 (2)

1. A_0 - this address input selects different command words within the 8259A.
2. \overline{CS} - chip select enables the 8259A for programming and control.
3. $\overline{PS} / \overline{EN}$ - Slave Program/Enable Buffer is a dual-function pin.
 - ❖ When the 8259A is in buffered mode, this pin is an output that controls the data bus transceivers in a large microprocessor-based system.
 - ❖ When the 8259A is not in buffered mode, this pin programs the device as a master (1) or a slave (0).
4. $CAS_2 - CAS_0$, the cascade lines are used as outputs from the master to the slaves for cascading multiple 8259As in a system.

8259A PIC- Block Diagram

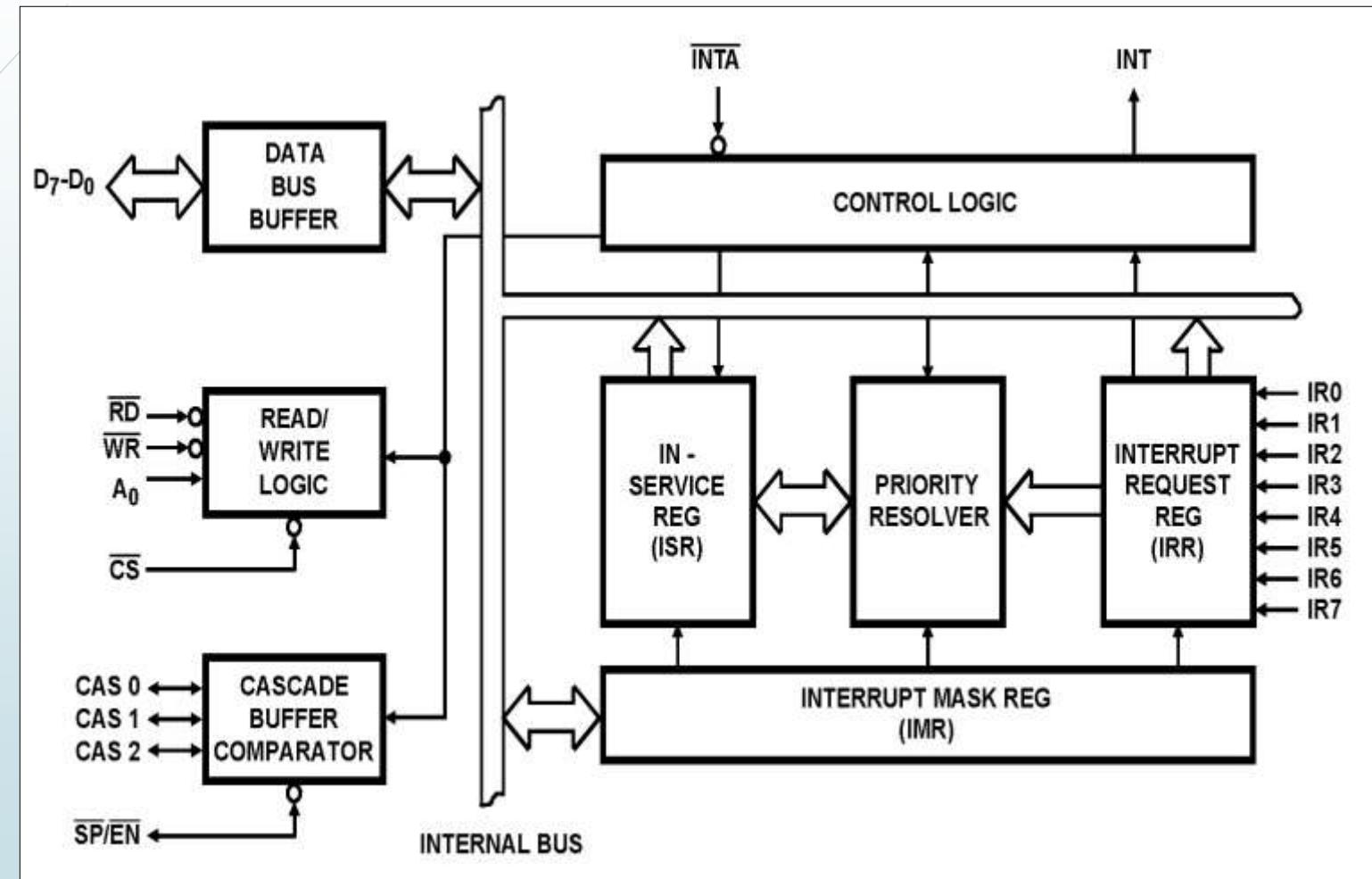


Image Courtesy: Google

8259A - Internals (1/4)

The Internals of 8259

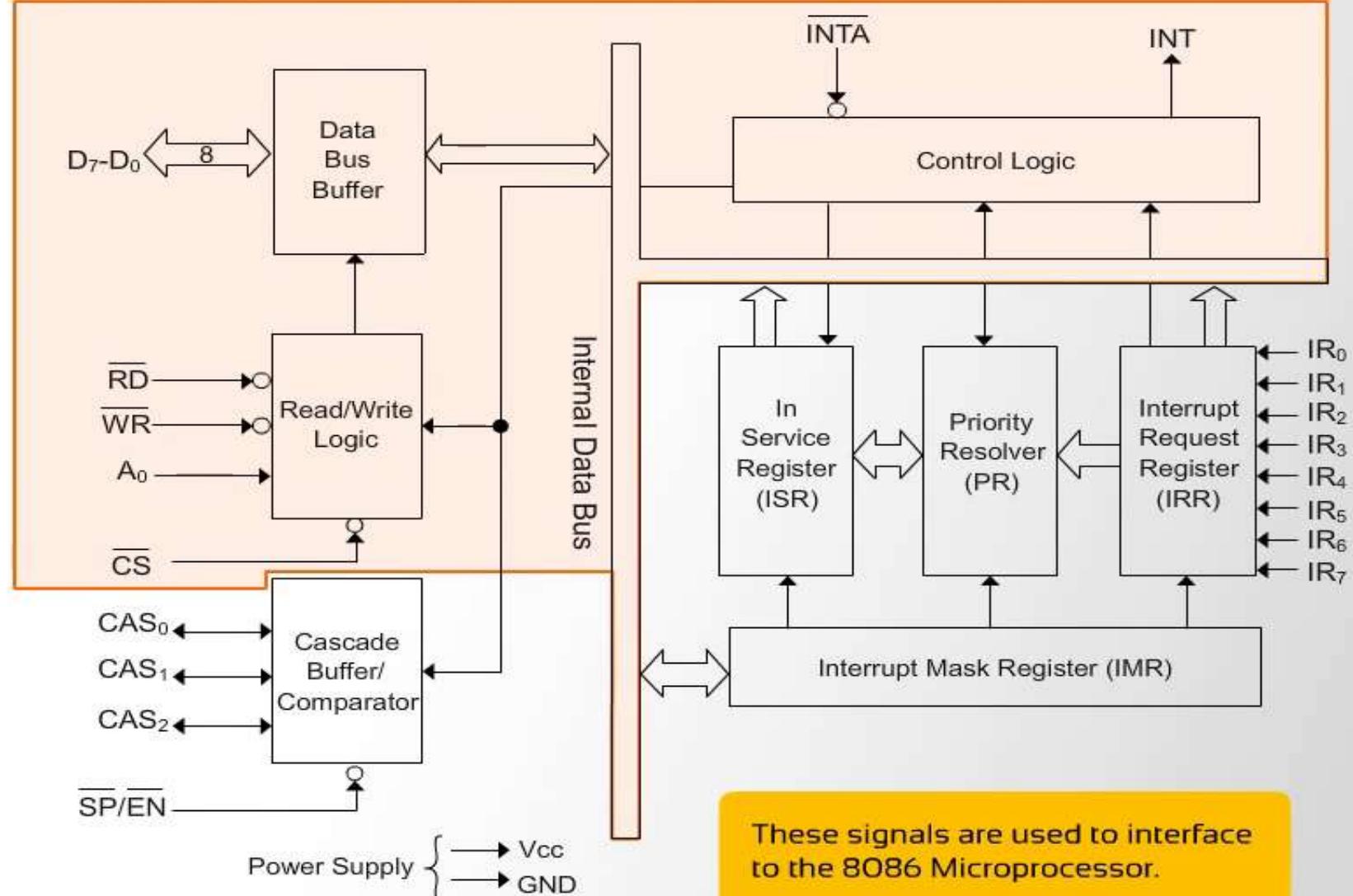
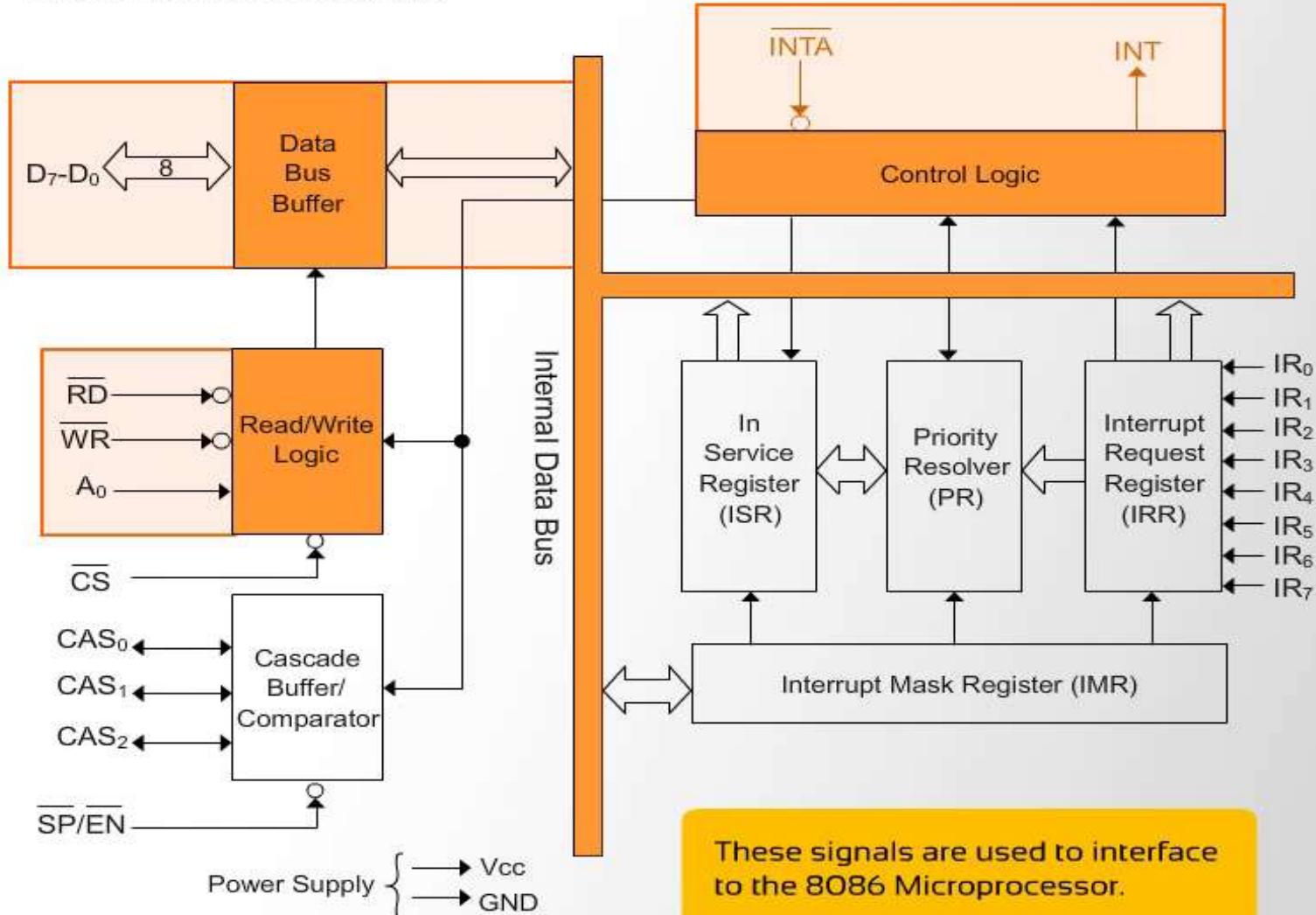


Image Courtesy: Google

8259A - Internals (2/4)

The Internals of 8259



8259A - Internals (3/4)

The Internals of 8259

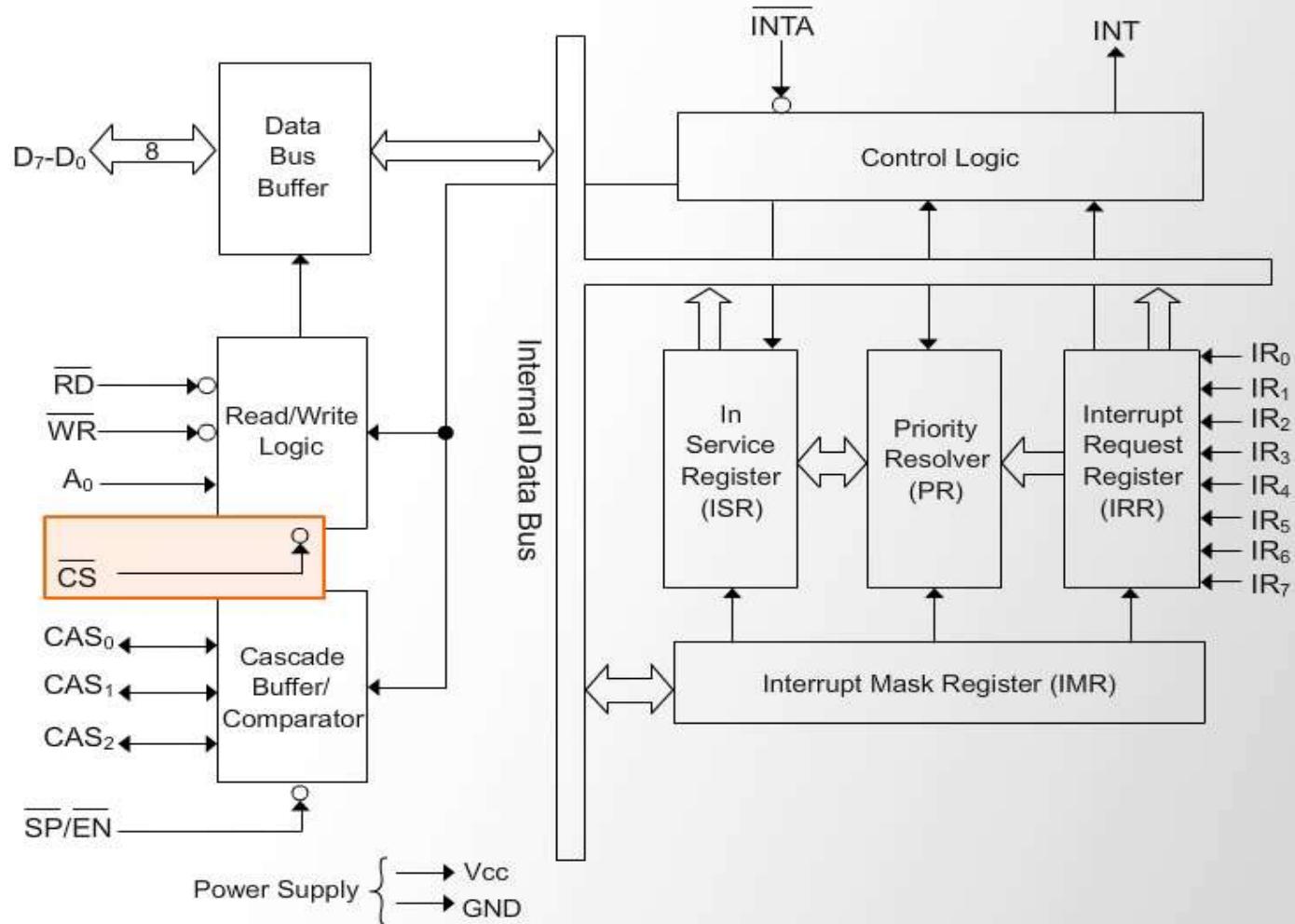
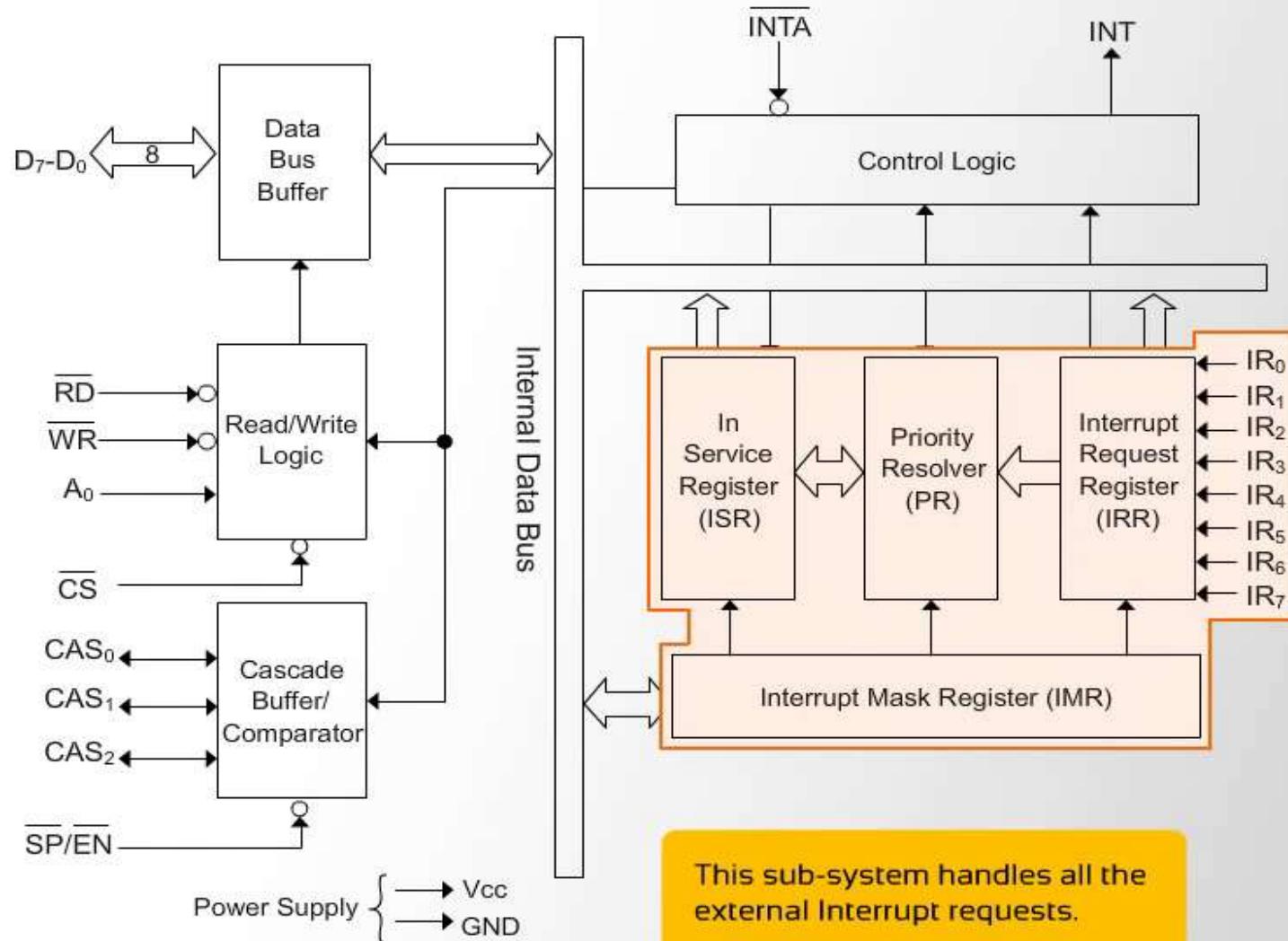


Image Courtesy: Google

8259A - Internals (4/4)

The Internals of 8259



8259A - Internals (IPR)

The Internals of 8259

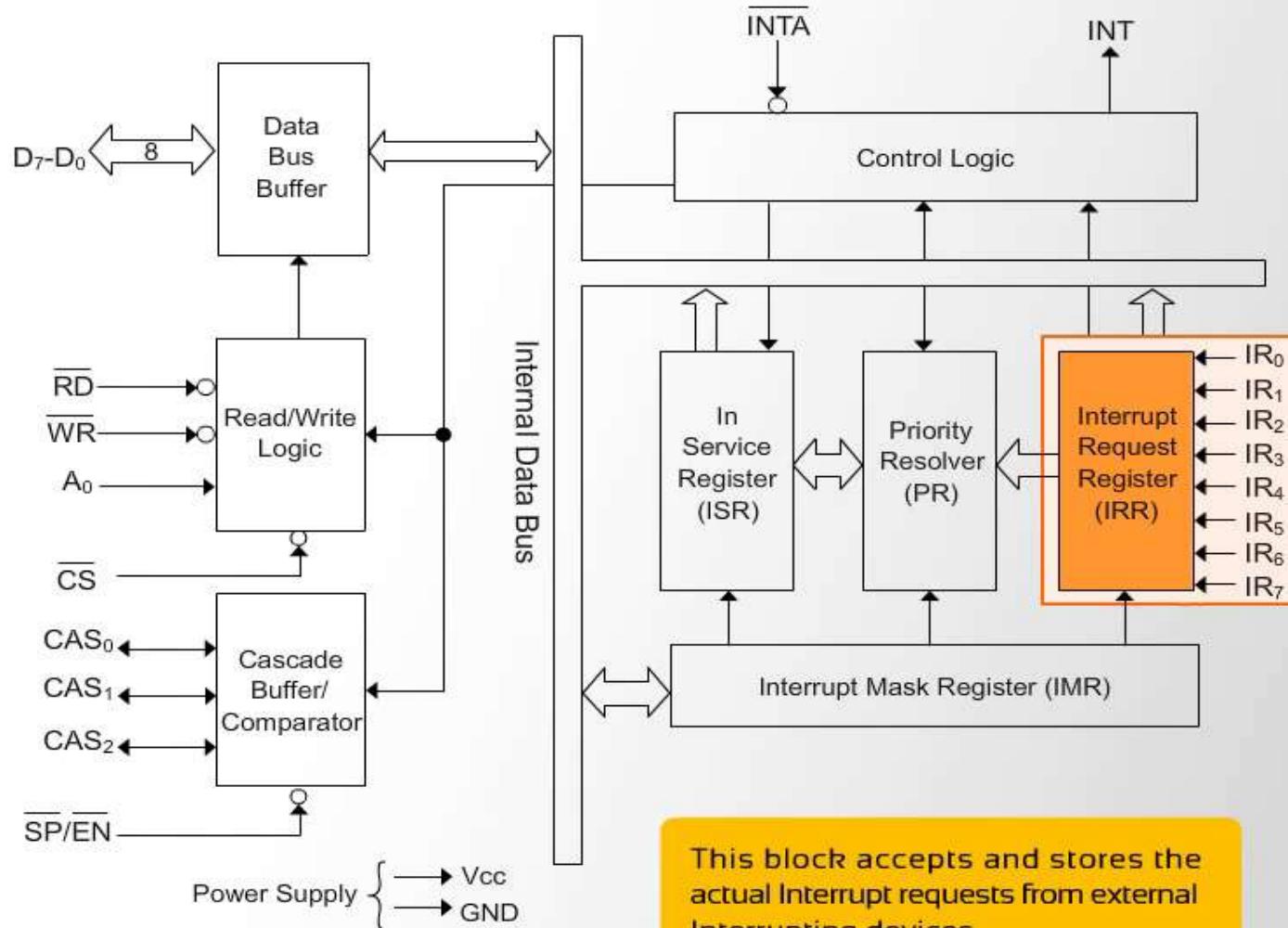


Image Courtesy: Google

8259A - Internals (ISR)

The Internals of 8259

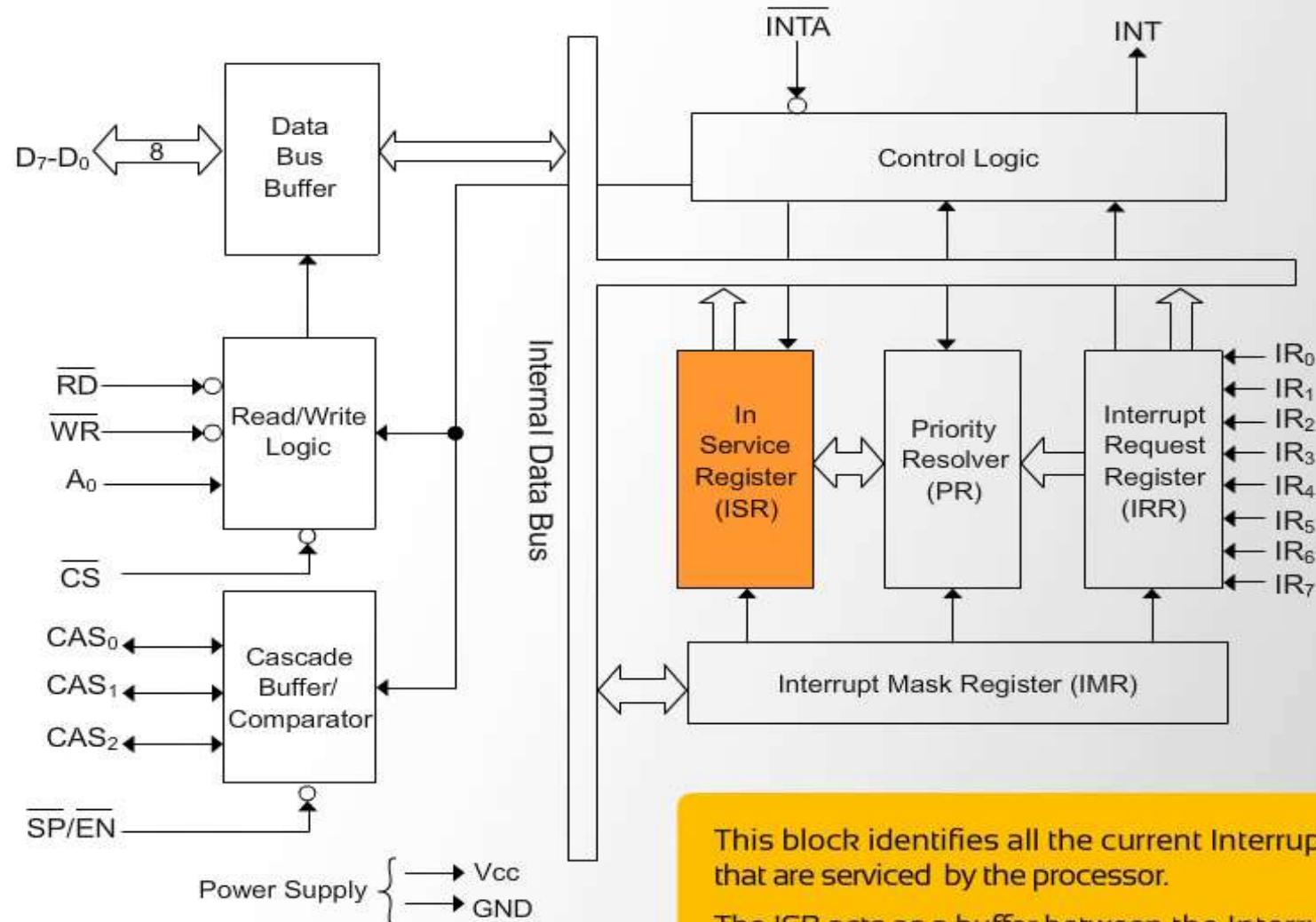
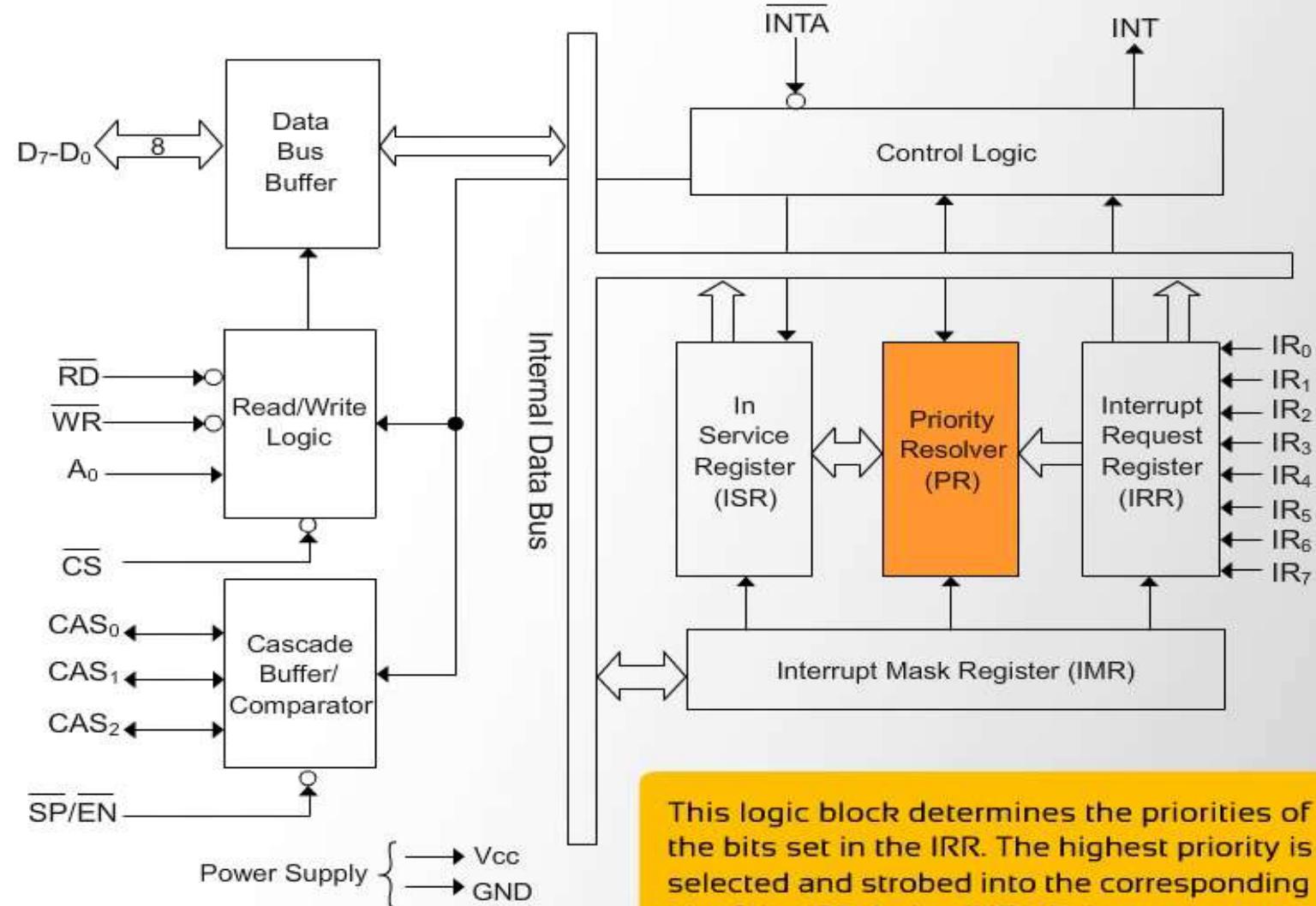


Image Courtesy: Google

8259A - Internals (PR)

The Internals of 8259



8259A - Internals (IMR)

The Internals of 8259

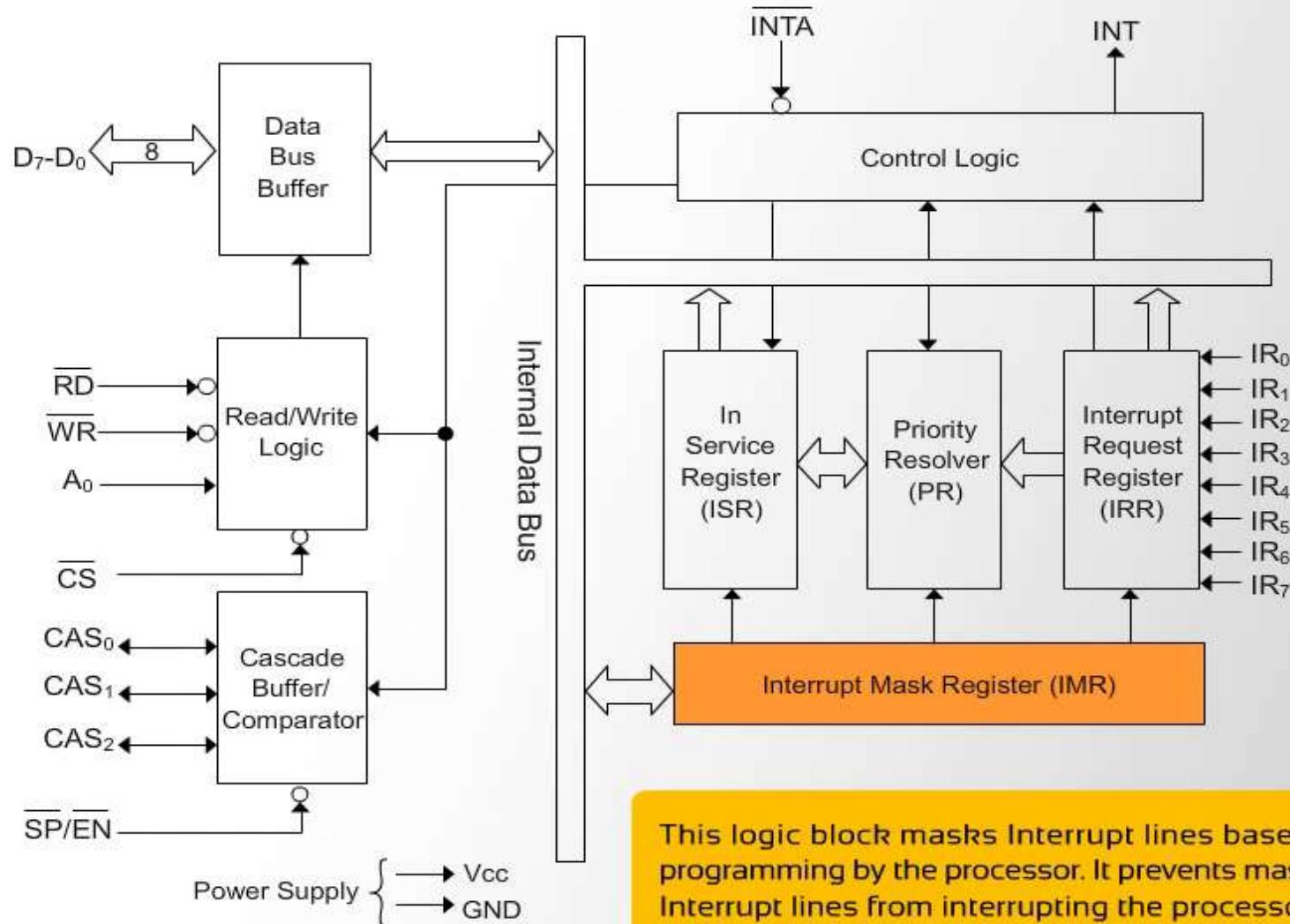


Image Courtesy: Google

8259A - Internals (CAS)

The Internals of 8259

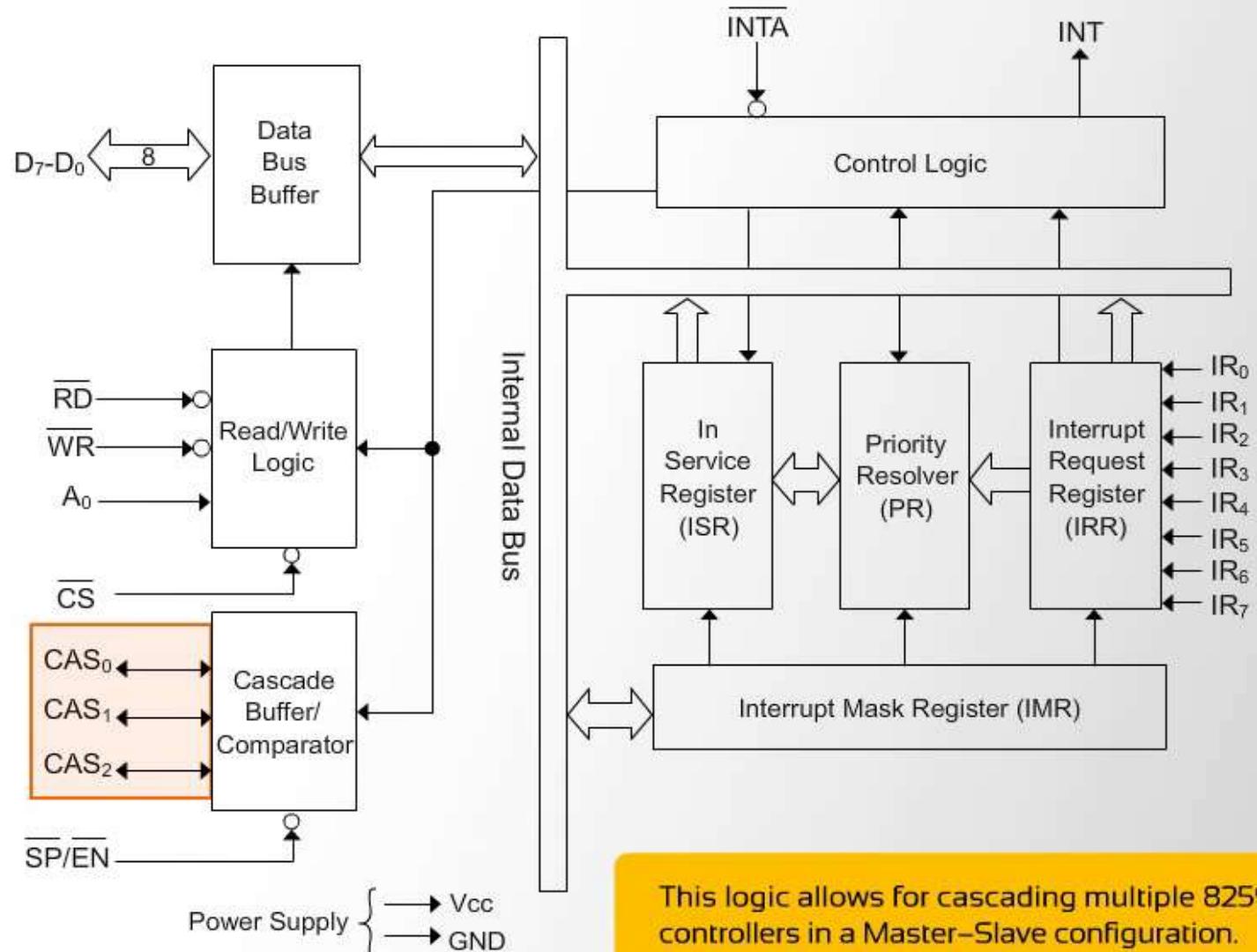
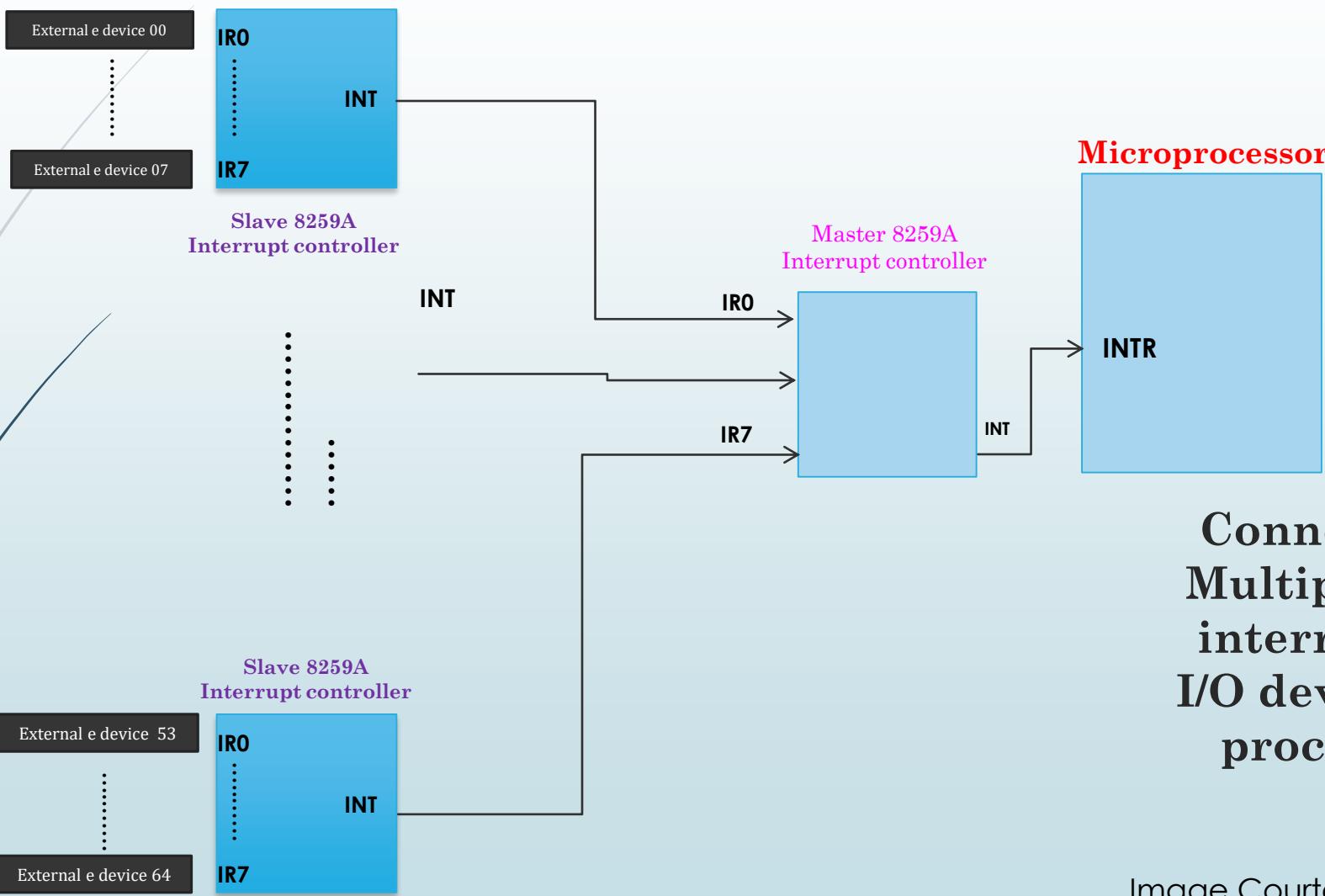


Image Courtesy: Google

Cascading multiple 8259



Connecting
Multiple (64)
interrupted
I/O devices to
processor

Image Courtesy: Google

Learning Resource

[1] K. M. Bhurchandi and A. K. Ray, "Advanced Microprocessors and Peripherals – with ARM and an Introduction to Microcontrollers and Interfacing", Tata McGraw Hill, 3rd ed., 2015.

Note: Almost all figures and text content taken from the above stated book.



Thank You

18ECC203J – Module 3

8086 Interfacing with Memory and Programmable Devices

S – 11, 12, 13

Prepared by,

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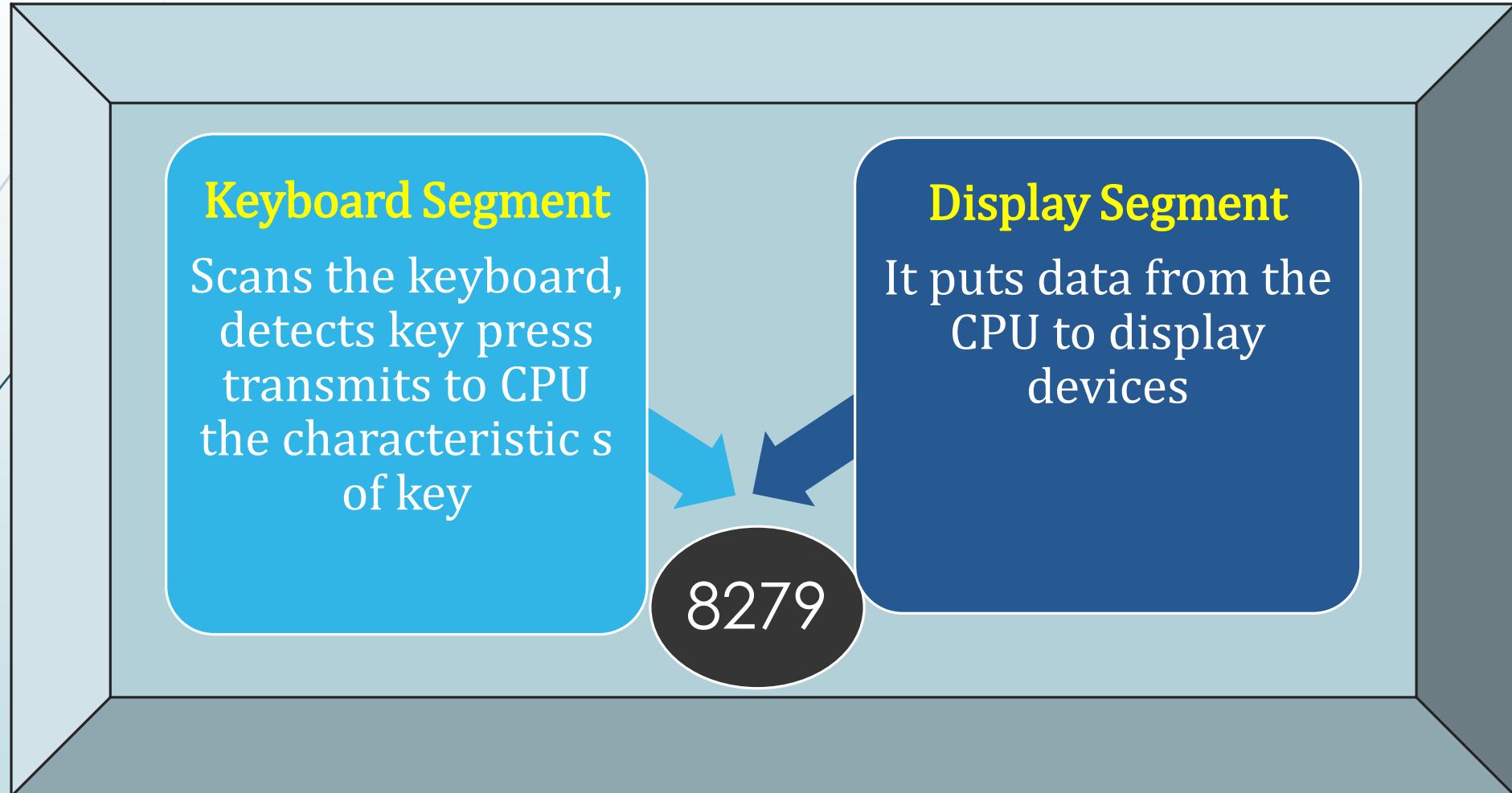
S – 11

Programmable Keyboard / Display Controller
8279 & Interfacing 8279 with 8086 and
programming

Why 8279?

- ▶ Interfacing keyboards and displays can be done using 8255.
- ▶ ISSUE is processor has to refresh the display and check the status of the keyboard periodically using polling technique.
- ▶ DISADVANTAGE: A considerable amount of CPU time is wasted, reducing the system operating speed.
- ▶ Intel's 8279 is a general purpose keyboard display
- ▶ 8279 controller can simultaneously drives the display of a system and interfaces a keyboard with the CPU.
- ▶ ADVANTAGE: CPU left free for its routine task (computing).

Components of 8279

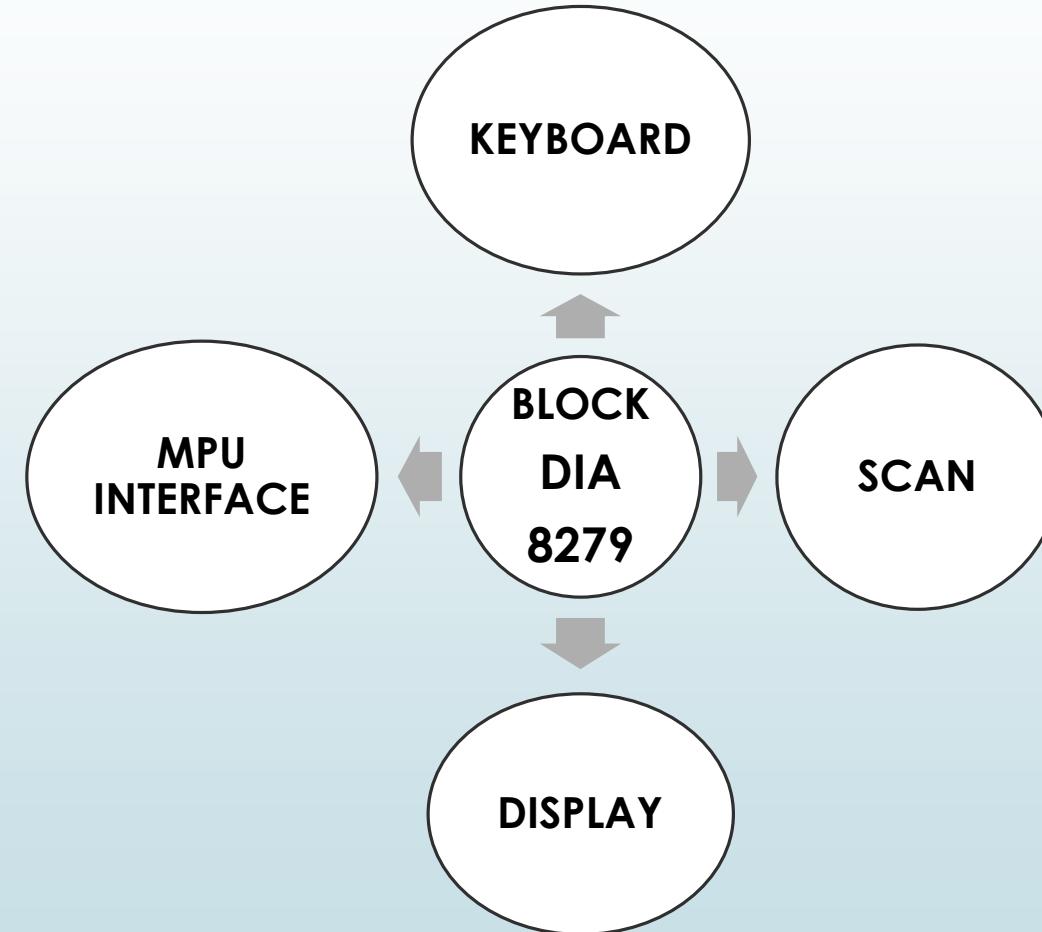


Functions of 8279

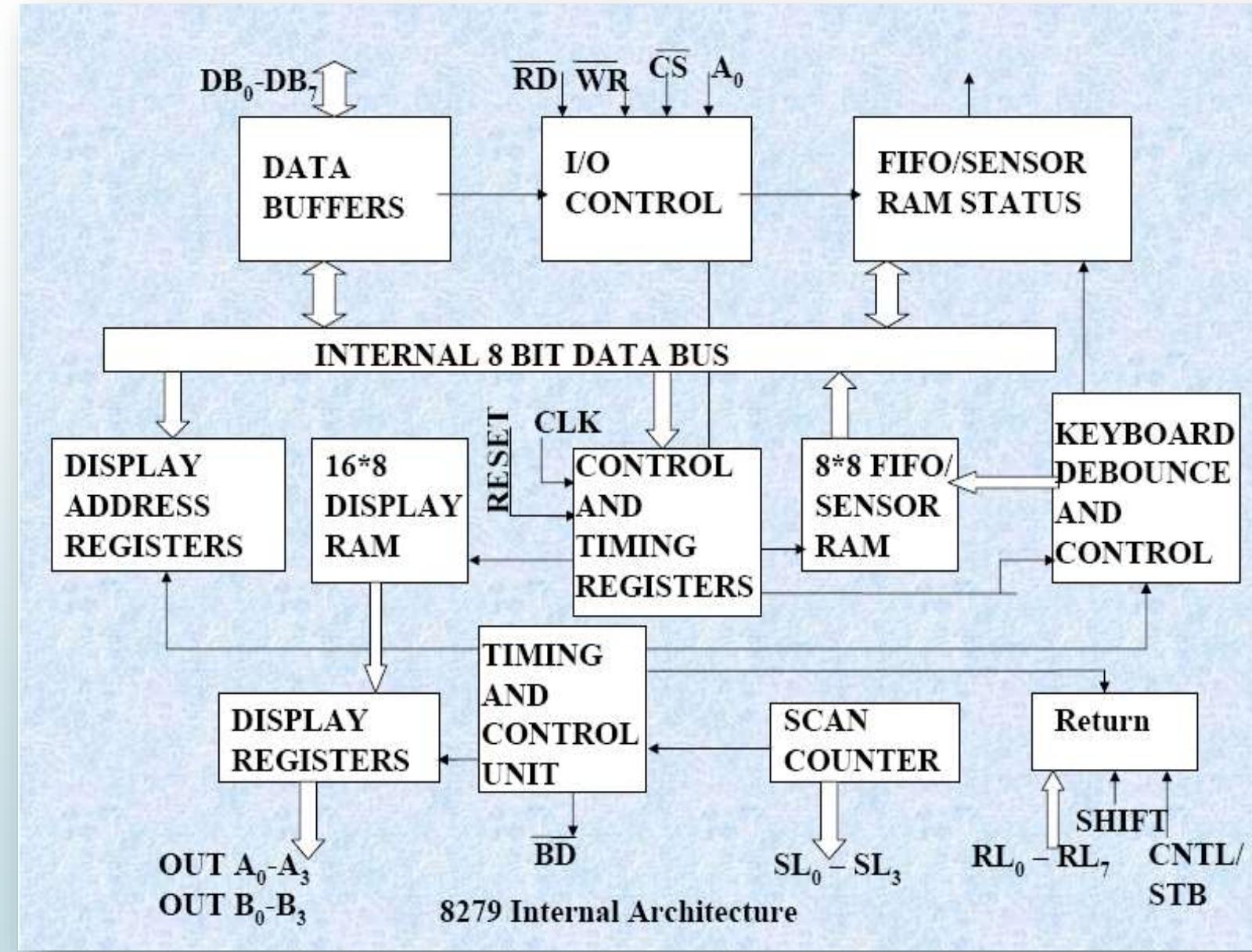


- ↳ Connected to a 64 contact key matrix
 - ↳ Keyboard entries are debounced and stored in FIFO
 - ↳ Interrupt signal is generated with each entry
-
- ↳ 16 character scanned display
 - ↳ 16x8 R/W memory (RAM)
 - ↳ Right entry or left entry

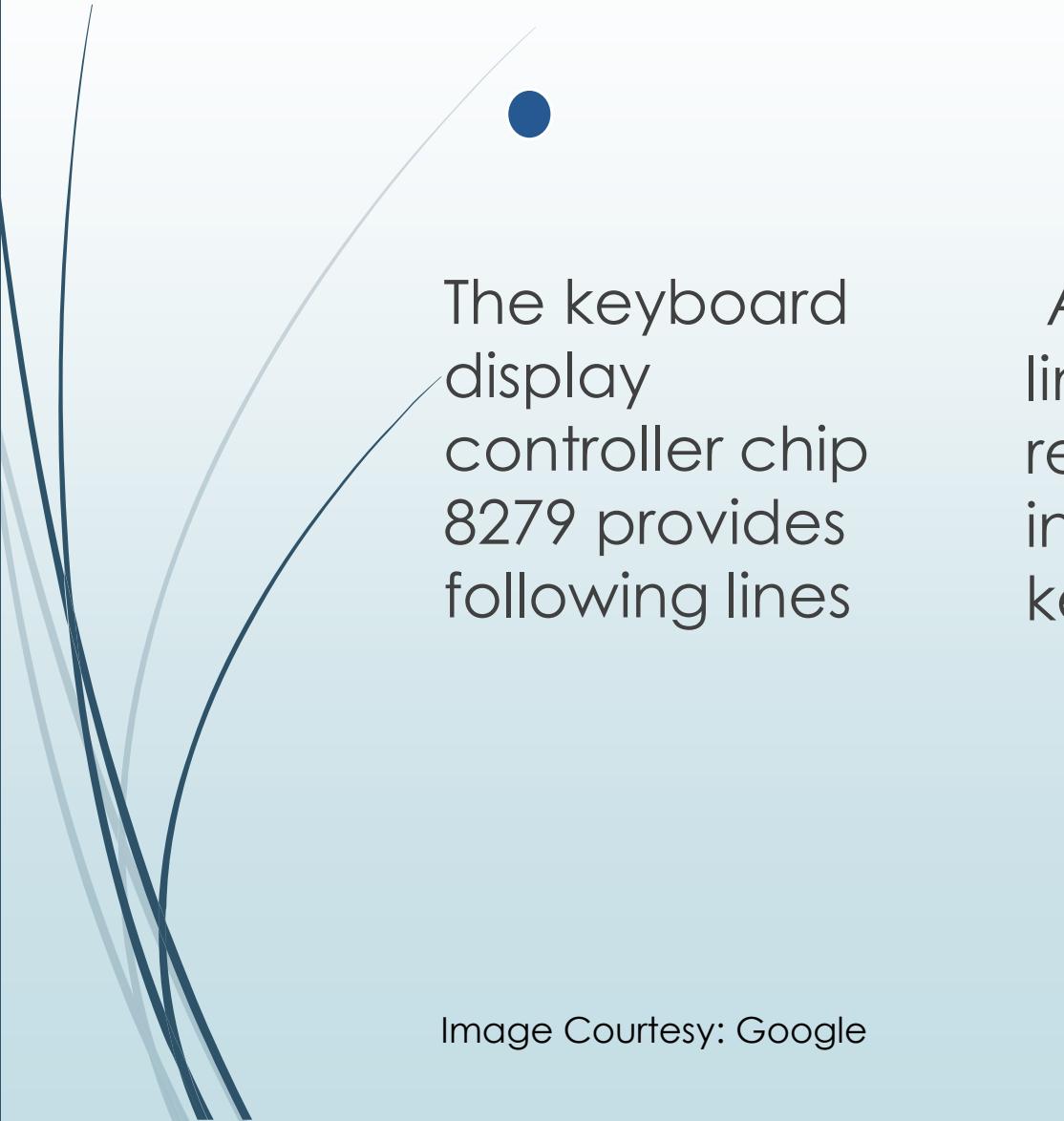
8279 interface



8279 Block Diagram



Architecture of 8279



The keyboard display controller chip 8279 provides following lines

A set of 4 scan lines and 8 return lines for interfacing keyboard



A set of 8 output lines for interfacing display

8279 – Control lines

**I/O
Control
and Data
Buffers**

- ↳ The I/O control section controls the flow of data to/from the 8279
- ↳ The I/O section is enabled only if CS is low.
- ↳ The pins A0, RD and WR select the command, status or data read/write operations carried out by the CPU with 8279.
- ↳ The data buffers interface the external bus of the system with internal bus of 8279.

**Control
and Timing
Register
and Timing
Control :**

- ↳ These registers store the keyboard and display modes and other operating conditions programmed by CPU.
- ↳ The registers are written with A0=1 and WR=0. The Timing and control unit controls the basic timings for the operation of the circuit.
- ↳ Scan counter divide down the operating frequency of 8279 to derive scan keyboard and scan display frequencies.

Scan Counter

- ▶ The scan counter has **two modes** to scan the key matrix and refresh the display.
- ▶ In the **encoded mode**, the counter provides binary count that is to be externally decoded to provide the scan lines for keyboard and display
- ▶ Four externally decoded scan lines may drive upto 16 displays.
- ▶ In the **decode scan mode**, the counter internally decodes the least significant 2 bits and provides a decoded 1 out of 4 scan on SLO-SL3
- ▶ Four internally decoded scan lines may drive upto 4 displays.
- ▶ The keyboard and display both are in the same mode at a time.

Return Buffers and Display RAM

Return Buffers and Keyboard De-bounce and Control:

- ▶ This section scans for a **key closure row wise**. If a key closer is detected, the keyboard debounce unit debounces the key entry (i.e. wait for 10 ms).
- ▶ After the debounce period, if the key continues to be detected, The code of key is directly **transferred to the sensor RAM** along with SHIFT and CONTROL key status.

Display Address Registers and Display RAM :

- ▶ The display address register **holds the address** of the word currently being written or read by the CPU to or from the display RAM.
- ▶ The contents of the registers are **automatically updated** by 8279 to accept the next data entry by CPU.

FIFO/Sensor RAM and Status Logic

In keyboard or strobed input mode, this block acts as 8-byte first-in-first out (FIFO) RAM

- ▶ Each key code of the pressed key is entered in the order of the entry and in the mean time read by the CPU, till the RAM become empty.
- ▶ The status logic generates an interrupt after each FIFO read operation till the FIFO is empty.

In scanned sensor matrix mode, this unit acts as sensor RAM.

- ▶ Each row of the sensor RAM is loaded with the status of the corresponding row of sensors in the matrix.
- ▶ If a sensor changes its state, the IRQ line goes high to interrupt the CPU.

S - 12

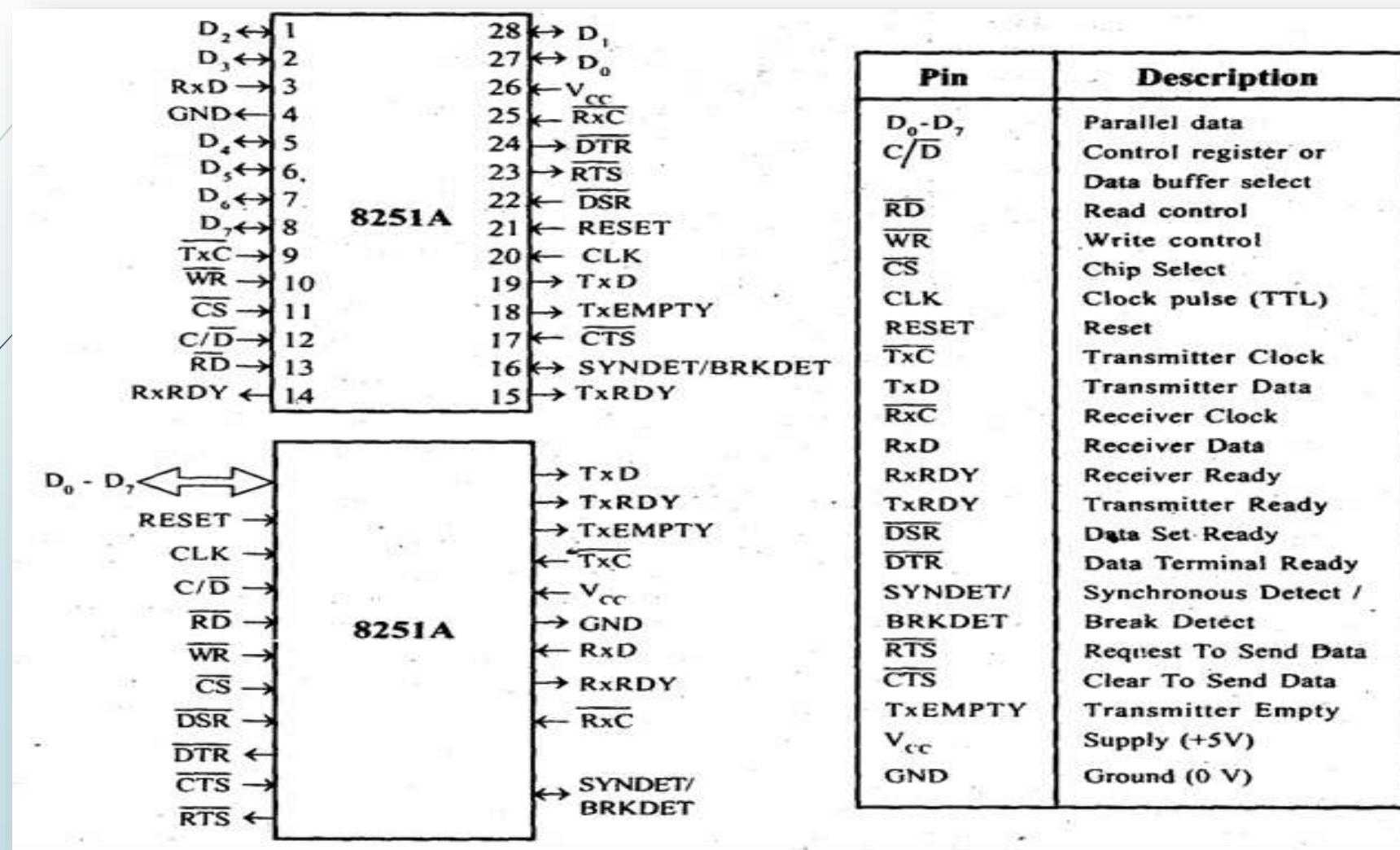
Programmable Communication Interface 8251
USART & Interfacing 8251 with 8086 and
programming

8251

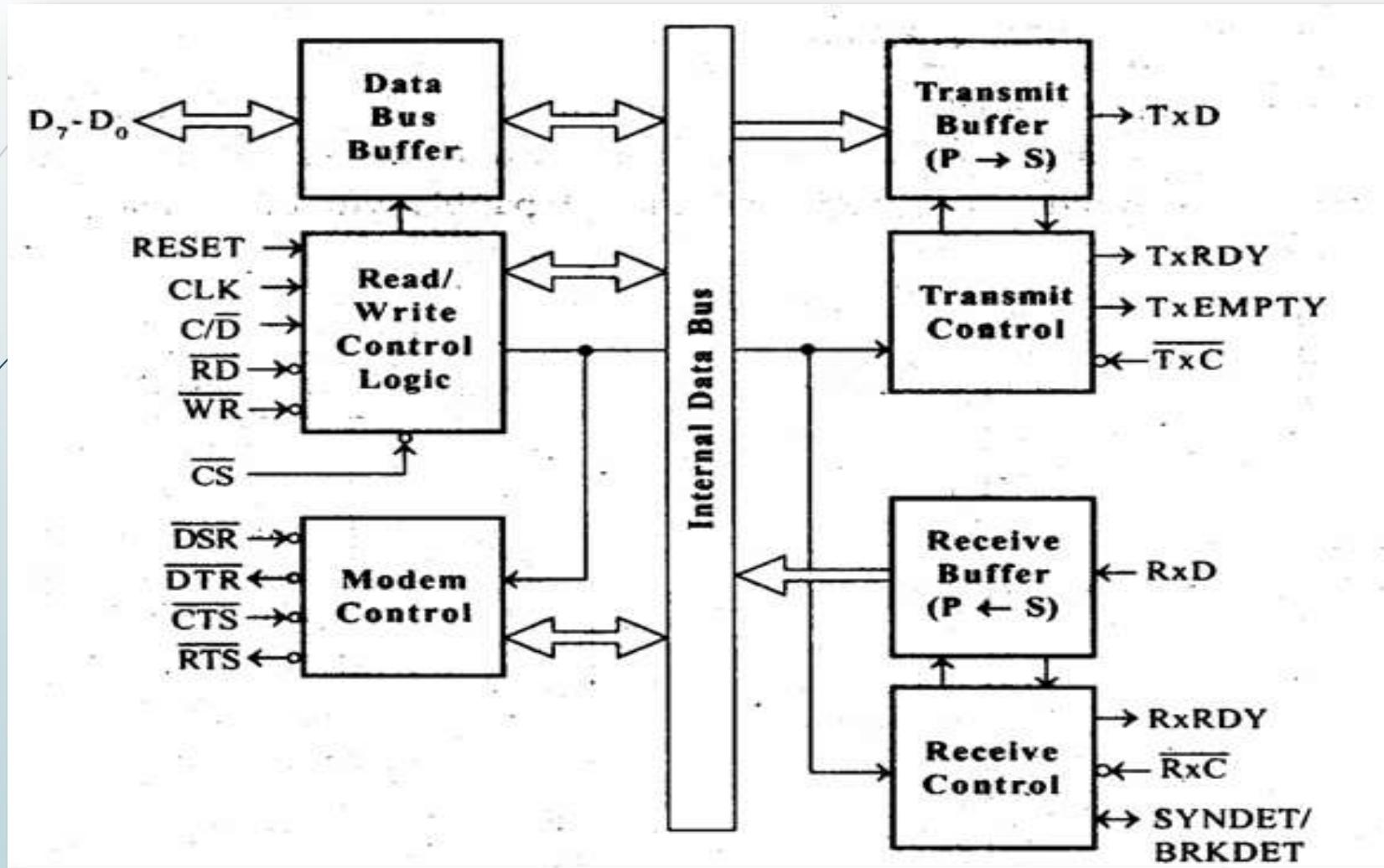
- ▶ The 8251A is a programmable serial communication interface chip designed for synchronous and asynchronous serial data communication.
- ▶ It supports the serial transmission of data.
- ▶ It is packed in a 28 pin DIP.

8251 – Pin Details

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8251 – Architecture



8251 Architecture - Explanation

► The functional block diagram of 8251A consists of five sections.

They are:

- Read/Write control logic
- Transmitter
- Receiver
- Data bus buffer
- Modem control.

Read/Write control logic

- ▶ The Read/Write Control logic interfaces the 8251A with CPU, determines the functions of the 8251A according to the control word written into its control register.
- ▶ It monitors the data flow.
- ▶ This section has three registers and they are control register, status register and data buffer.
- ▶ The active low signals RD, WR, CS and C/D(Low) are used for read/write operations with these three registers.

Read/Write control logic (2)

- ▶ When C/D(low) is high, the control register is selected for writing control word or reading status word.
- ▶ When C/D(low) is low, the data buffer is selected for read/write operation.
- ▶ When the reset is high, it forces 8251A into the idle mode.
- ▶ The clock input is necessary for 8251A for communication with CPU and this clock does not control either the serial transmission or the reception rate.

Transmitter

- ▶ The transmitter section accepts parallel data from CPU and converts them into serial data.
- ▶ The transmitter section is double buffered, i.e., it has a buffer register to hold an 8-bit parallel data and another register called output register to convert the parallel data into serial bits.
- ▶ When output register is empty, the data is transferred from buffer to output register. Now the processor can again load another data in buffer register. If buffer register is empty, then TxRDY goes to high.
- ▶ If output register is empty then TxEMPTY goes to high.
- ▶ The clock signal, TxC (low) controls the rate at which the bits are transmitted by the USART.
- ▶ The clock frequency can be 1,16 or 64 times the baud rate.

Receiver

- ▶ The receiver section accepts serial data and convert them into parallel data
- ▶ The receiver section is double buffered, i.e., it has an input register to receive serial data and convert to parallel, and a buffer register to hold the parallel data.
- ▶ When the RxD line goes low, the control logic assumes it as a START bit, waits for half a bit time and samples the line again.
- ▶ If the line is still low, then the input register accepts the following bits, forms a character and loads it into the buffer register.

Receiver (2)

- ▶ The CPU reads the parallel data from the buffer register.
- ▶ When the input register loads a parallel data to buffer register, the RxRDY line goes high.
- ▶ The clock signal RxC (low) controls the rate at which bits are received by the USART.
- ▶ During asynchronous mode, the signal SYNDET/BRKDET will indicate the break in the data transmission.
- ▶ During synchronous mode, the signal SYNDET/BRKDET will indicate the reception of synchronous character.

Modem Control

- ▶ The MODEM control unit allows to interface a MODEM to 8251A and to establish data communication through MODEM over telephone lines.
- ▶ This unit takes care of handshake signals for MODEM interface.
- ▶ The 8251A can be memory mapped (OR) I/O mapped
- ▶ Using a 3-to-8 decoder generates the chip select signals for I/O mapped devices.
- ▶ The address lines A4, A5 and A6 are decoded to generate eight chip select signals (IOCS-0 to IOCS-7) and in this, the chip select signal IOCS-2 is used to select 8251A.

Modem control (2)

- ▶ The address line A7 and the control signal IO / M(low) are used as enable for decoder.
- ▶ The address line A0 of 8085 is connected to C/D(low) of 8251A to provide the internal addresses.
- ▶ The data lines D0 - D7 are connected to D0 - D7 of the processor to achieve parallel data transfer.
- ▶ The RESET and clock signals are supplied by the processor. Here the processor clock is directly connected to 8251A. This clock controls the parallel data transfer between the processor and 8251A.
- ▶ The output clock signal of 8085 is divided by suitable clock dividers like programmable timer 8254 and then used as clock for serial transmission and reception.

Modem Control (3)

- The TTL logic levels of the serial data lines and the control signals necessary for serial transmission and reception are converted to RS232 logic levels using MAX232 and then terminated on a standard 9-pin D.-type connector.
- In 8251A the transmission and reception baud rates can be different or same.
- The device which requires serial communication with processor can be connected to this 9-pin D-type connector using 9-core cable
- The signals TxEMPTY, TxRDY and RxRDY can be used as interrupt signals to initiate interrupt driven data transfer scheme between processor and 8251

Modem Control (4)

- The CPU reads the parallel data from the buffer register.
- When the input register loads a parallel data to buffer register, the RxRDY line goes high.
- The clock signal RxC (low) controls the rate at which bits are received by the USART.
- During asynchronous mode, the signal SYNDET/BRKDET will indicate the break in the data transmission.
- During synchronous mode, the signal SYNDET/BRKDET will indicate the reception of synchronous character.

S – 13

DMA Controller 8257 & Interfacing 8257 with
8086 and programming

Direct Memory Access (DMA)

- ▶ An I/O technique used for high data transfer
- ▶ Between memory and peripheral
- ▶ MPU releases the control of Buses
- ▶ DMA controller manages data transfer

8257 DMA Controller

- ▶ Programmable DMA controller
- ▶ Primary function: a sequential memory access which allow the peripheral **to read or write data directly to or from memory**
- ▶ Has 4 independent channels each capable of transferring 64 Kbytes of data
- ▶ Must be interfaced with MPU and peripherals
- ▶ HOLD
- ▶ HLDA (Hold Acknowledge)

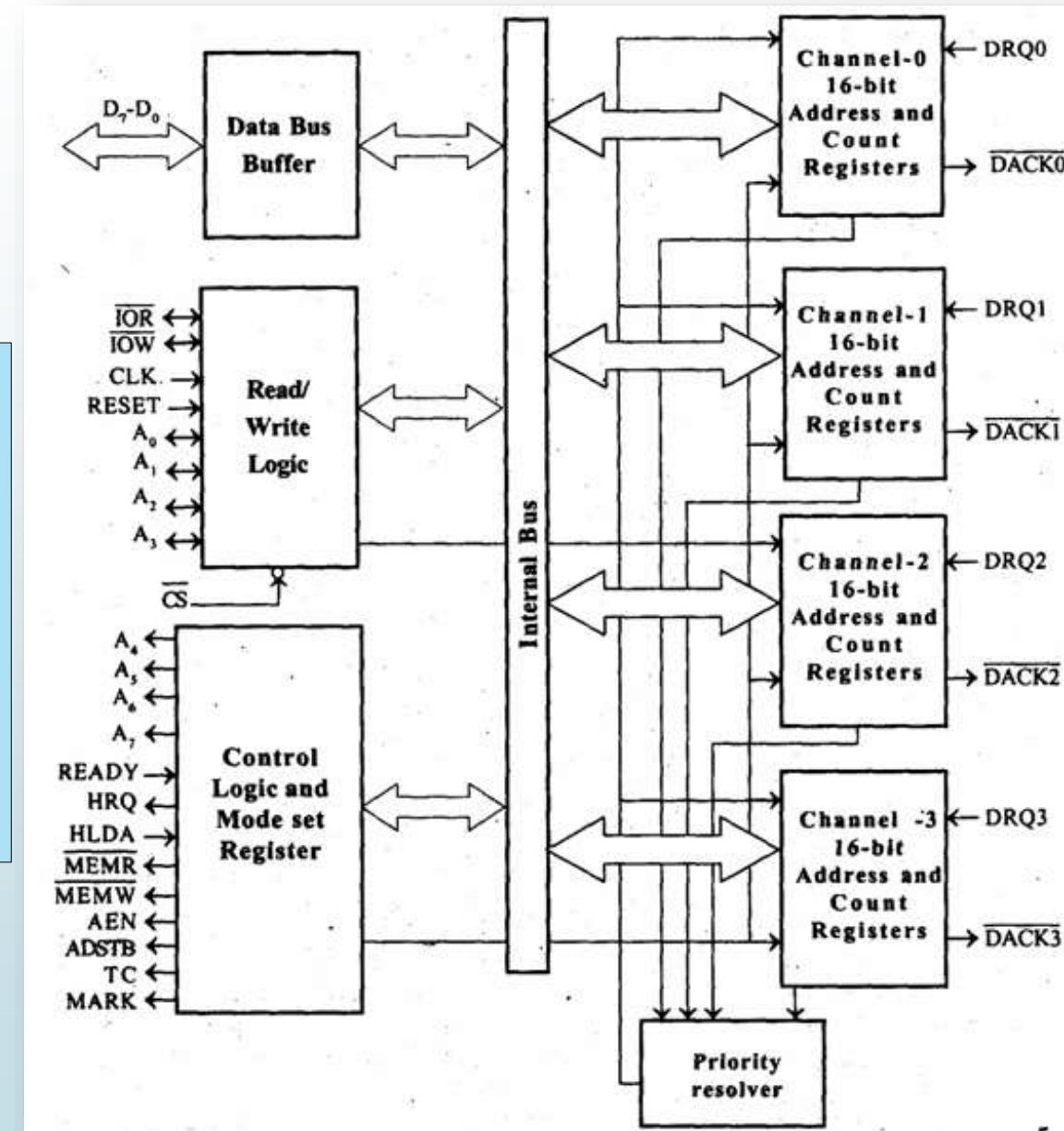
8257 DMA Controller

- ▶ Plays two role:
 - ▶ I/O to Microprocessor (**Slave mode**)
 - ▶ Data transfer processor to peripherals (**Master mode**)
- ▶ Has priority DMA request logic

8257 Architecture

BLOCKS

1. DMA Channels
2. Data Bus Buffer
3. Read/Write Logic
4. Control Logic



1. DMA Channels contd...

- ▶ Four separate DMA channels (CH-0 to CH-3)
- ▶ Each channel includes two 16 bit registers
 1. DMA address register
 2. Terminal count register
- ▶ 14 bit count ($N-1$) is loaded into TC reg
 - ▶ 2 msb's give the type of DMA operation
- ▶ Signals DRQ0 to DRQ3, $\overline{DACK_0}$ to $\overline{DACK_3}$

1. DMA Channels (Types of DMA Operation)

Bit 15	Bit 14	Type of DMA Operation
0	0	Verify DMA Cycle
0	1	Write DMA Cycle
1	0	Read DMA Cycle
1	1	(Illegal)

2. Data Bus Buffer

- ▶ This three-state, bi-directional, eight bit buffer interfaces the 8257 to the system data bus
- ▶ $D_0 - D_7$

3. Read/Write Logic

- A₀ – A₃
 - $\overline{\text{IOR}}$, $\overline{\text{IOW}}$
 - Input signals in slave mode
 - Output signals in master mode
 - RESET
 - CLK
 - $\overline{\text{CS}}$

4. Control Logic

- ADSTB (Address Strobe):
 - This output strobes the most significant byte of the memory address into the 8212 device from the data bus
 - AEN (Address Enable):
 - Used to disable the system buses
 - TC (Terminal Count)
 - MARK (Modulo 128 Mark)

Learning Resource

[1] K. M. Bhurchandi and A. K. Ray, "Advanced Microprocessors and Peripherals – with ARM and an Introduction to Microcontrollers and Interfacing", Tata McGraw Hill, 3rd ed., 2015.

Thank You