

UNIT - II

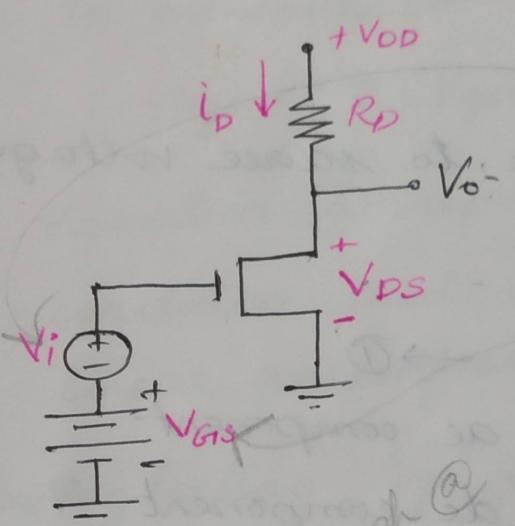
FET Amplifiers.

Overview of FET ckt analysis : MOSFET amplifiers

Although the major use of MOSFET is in digital applications, they are also used in linear amplifiers.

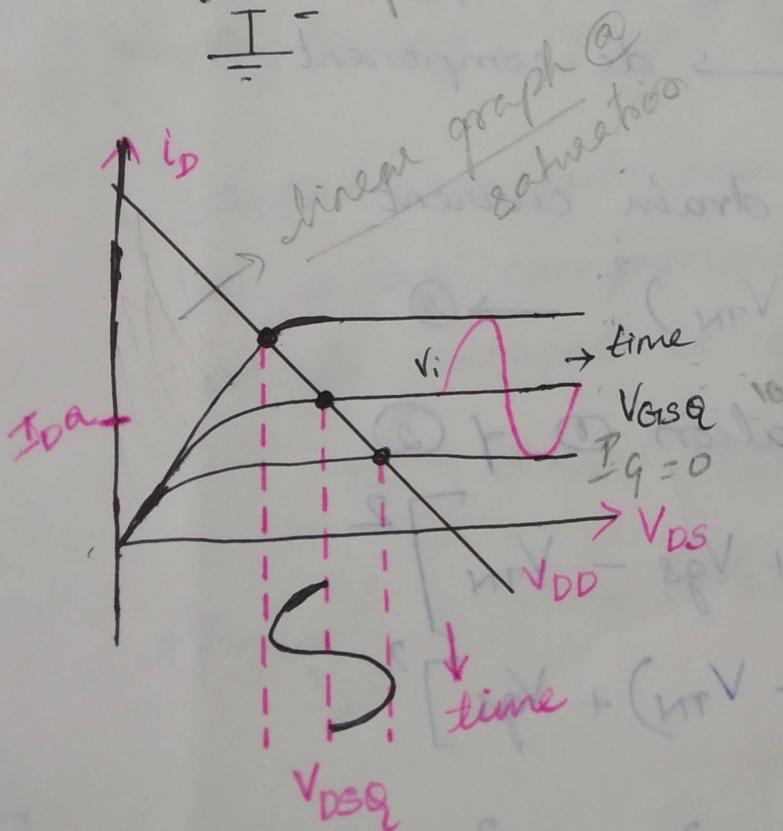
Graphical analysis & load line.

NMOS - common source ckt.



→ shows an NMOS common source circuit with a time varying voltage source in series with dc voltage source

→ assume time varying V_P is sinusoid, and for i_P to be linear function of the V_P voltage, the transistor must be biased in the saturation region. → fet



→ the sinusoidal variations in V_{GS} , i_D & V_{DS} are shown.

$\frac{dI_D}{dV_{GS}} = g_m = \text{constant}$
 $I_D \propto V_{GS} \quad V_{GS} \uparrow \rightarrow I_D \uparrow$
 $V_{DS} \uparrow \rightarrow I_D \downarrow$

- As V_{GS} increases, V_{DS} reduces & I_D increases. If V_i increases in negative, the Q point moves down the load line.
- for FET to operate as a linear amplifier the transistor must be biased in the saturation region, where i_s and V_{DS} must be confined to the saturation region.

Transistor parameters.

- The instantaneous gate to source voltage

is $V_{GS} = V_{GSQ} + V_i$

$$\boxed{V_{GS} = V_{GSQ} + V_{GS}} \rightarrow \textcircled{1}$$

→ ac component

↓ → dc component Q point

- The instantaneous drain current

$$i_D = k_n (V_{GS} - V_{TN})^2 \rightarrow \textcircled{2}$$

- substituting equation $\textcircled{1}$ & $\textcircled{2}$

$$i_D = k_n [V_{GSQ} + V_{GS} - V_{TN}]^2$$

$$= k_n [(V_{GSQ} - V_{TN}) + V_{GS}]^2$$

(QV)

$$\Rightarrow k_n \left[(V_{GSQ} - V_{TN})^2 + (V_{GS})^2 - 2(V_{GSQ} - V_{TN})(V_{GS}) \right]$$

1st

2nd

3rd

- i_{DQ} - is the dc or quiescent drain current.
- i_D - is proportional to the square of signal voltage.
- i_d - time varying drain current component that is linearly related to V_{GS} .

- for sinusoidal $\frac{d}{dt} i_D$ term, squared term produces undesirable harmonics or non-linear distortions in the op voltage.
- To minimize the harmonics, we require

$$V_{GS} \ll 2(V_{GSA} - V_{TN}) \rightarrow ④$$

Equation ④ represents the small signal condition that must be satisfied by all linear amplifiers.

- Neglecting V_{GS}^2 , $i_D = i_{DQ} + i_d$
- total current can be separated into a dc & ac component. The ac component of drain current is given by

$$i_d = 2k_n \underbrace{(V_{GSA} - V_{TN})}_{dc} V_{GS} \quad \text{ac component}$$

$$(g_m) = \frac{i_d}{V_{GS}} = 2k_n (V_{GSA} - V_{TN}) \rightarrow ⑤ \quad \frac{i_d}{V_{GS}} = g_m$$

$\Rightarrow g_m$, transconductance is a transfer co-efficient relating output current to input voltage and can be thought of as the gain of the transistor.

$$g_m = \frac{2D}{V_{GS}} / i_{DS} = V_{GSQ} = \text{constant.}$$

- from ②

$$i_D = k_n (V_{GS} - V_{TN})$$

$$i_{DQ} = k_n (V_{GS} - V_{TN})^2$$

$$\frac{i_{DQ}}{k_n} = (V_{GS} - V_{TN})^2$$

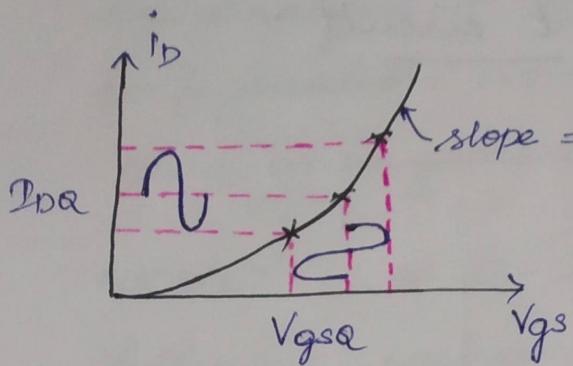
$$\therefore V_{GS} - V_{TN} = \sqrt{\frac{i_{DQ}}{k_n}}$$

substitute the above egn in ⑤

$$g_m = 2k_n \sqrt{\frac{i_{DQ}}{k_n}}$$

$$= 2 \sqrt{i_{DQ} \cdot k_n}$$

$$\boxed{\therefore g_m = 2 \sqrt{k_n \cdot D_{DQ}}}$$

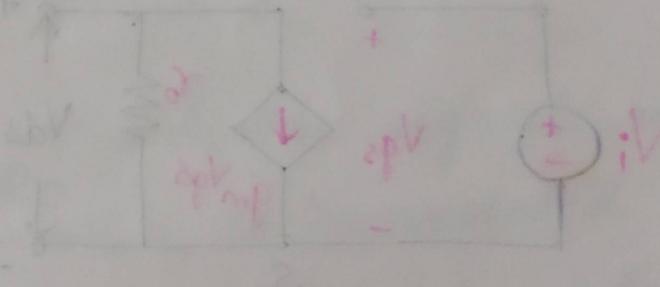


If V_{GS} is small, $g_m = \frac{k}{l}$ constant
with a point in the saturation region, the transistor operates as current sources that is

linearly controlled by V_{GS} .

$g_m \propto k_n$ (function of width to length ratio)
when the width of the transistor increases, the gain increases.

BJT - current controlled source
FET - voltage controlled source



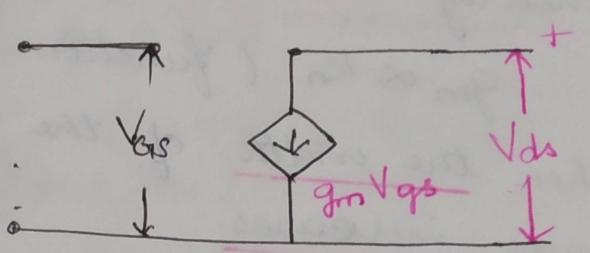
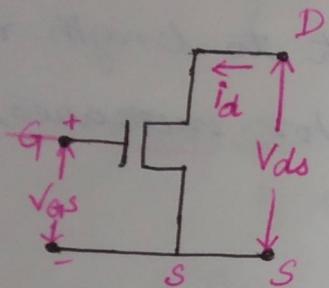
Small signal equivalent circuit ..

$$V_{DS} = V_{DD} - i_D R_o$$

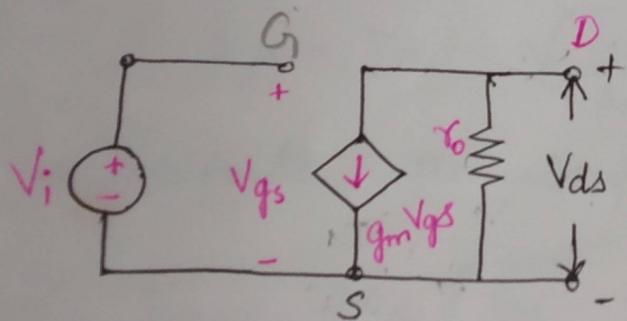
$$V_o = V_{DS} = i_D R_o$$

$$i_D = g_m \cdot V_{GS}$$

$$V_{GS} = V_i$$



↓
Expanded small signal equivalent circuit.



N - channel Mosfet.

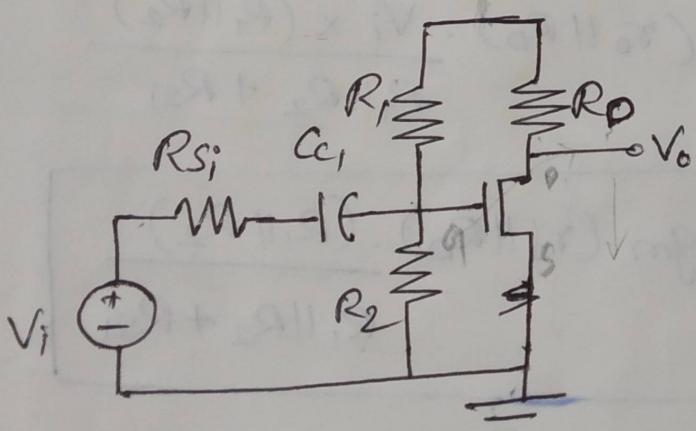
AC analysis of Basic MOSFET Amplifier configuration using classic discrete circuit bias arrangement.

MOSFET is a 3-terminal device. It has the following configurations:

- common source
- common drain
- common gate

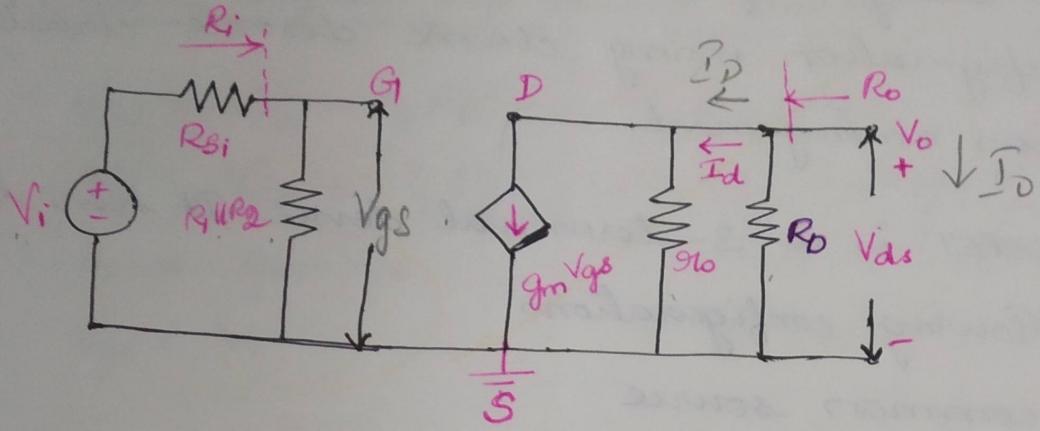
Common Source Amplifier.

Assume that the transistor is biased in the saturation region by $R_1 + R_2$, and signal frequency is sufficiently large for coupling capacitor to act essentially as a short circuit.



- The signal source is represented by the Thevenin's equivalent ckt in which, the signal voltage source V_i , is in series with the equivalent resistor R_s ;

→ R_s should be less than $R_t = R_1 \parallel R_2$ to minimise the loading effect.



Voltage gain (A_V)

$$A_V = \frac{V_o}{V_i}$$

$$V_o = I_o R_o = -I_D R_o$$

$$= -g_m V_{gs} (r_o \parallel R_o)$$

$$V_o = -g_m V_{gs} \times (r_o \parallel R_o)$$

$$V_{gs} = \frac{V_i \times R_1 \parallel R_2}{R_{si} + R_1 \parallel R_2}$$

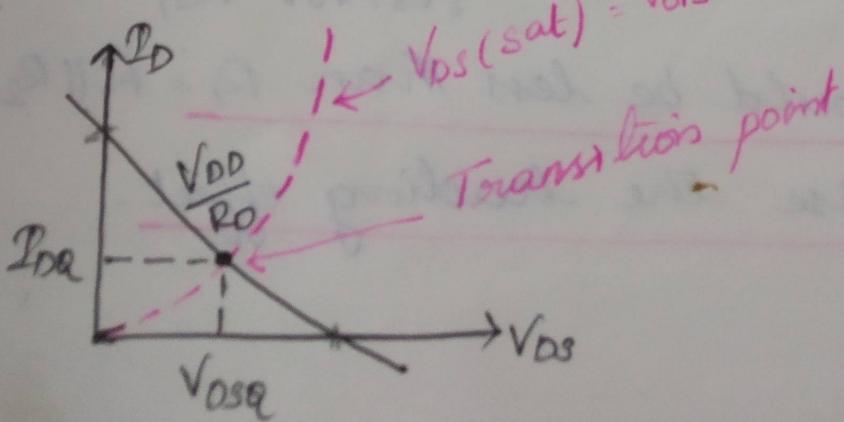
substitute in V_o

$$V_o = -g_m (r_o \parallel R_o) \cdot \frac{V_i \times (R_1 \parallel R_2)}{R_1 \parallel R_2 + R_{si}}$$

$$\boxed{\therefore A_V = \frac{V_o}{V_i} = -g_m (r_o \parallel R_o) \cdot \frac{(R_1 \parallel R_2)}{R_1 \parallel R_2 + R_{si}}}$$

$$\rightarrow V_{ds} = -I_o \cdot R_o$$

$$V_{ds} = V_{GS} - V_{TN}$$



- * transistor should be biased in saturation region and Q point must be near the middle of the saturation region.
- * I/p signal must be small for linear amplification.

Input resistance

$$R_i = R_1 \parallel R_2.$$

low frequency input resistance looking into the gate of MOSFET is ∞ .

Output resistance.

is found by setting $V_i = 0, \Rightarrow V_{gs} = 0$.

$$\therefore R_o = R_D \parallel R_0$$

DC load line.

- 1) Apply KVL at i/p side $\Rightarrow I_G$.
- 2) Apply KVL at o/p " $\Rightarrow y = mx + c$.
 $\Rightarrow I_D + V_{DS}$.

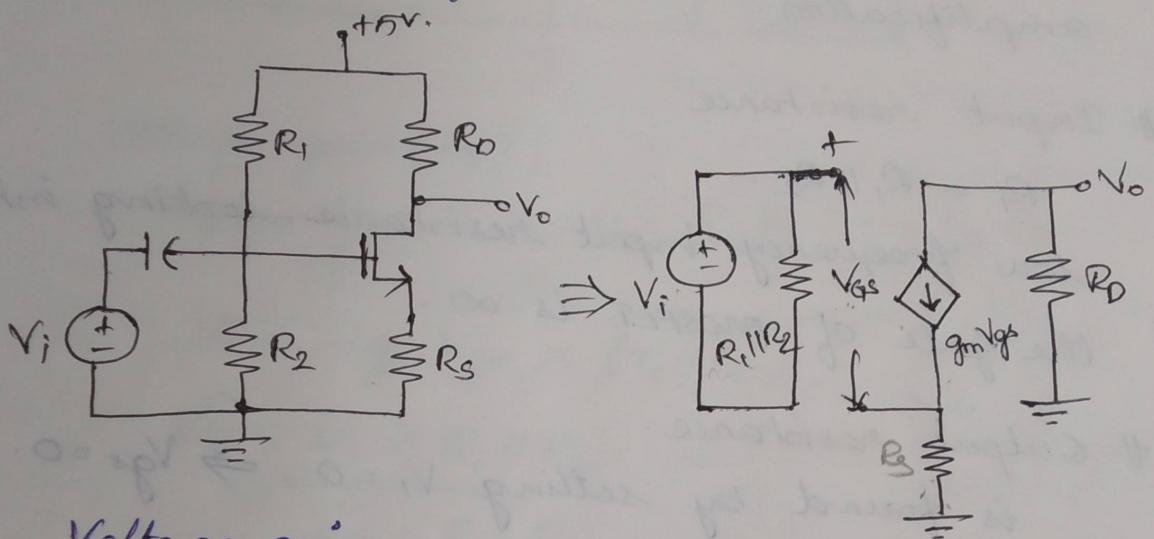
$$(Q_{mp}) \frac{V}{Q_{mp} + 1} = 0V$$

$$\frac{Q_{mp}}{Q_{mp} + 1}$$

$$\frac{Q_{mp}}{Q_{mp} - 1}$$

Common Source Amplifier with source resistor

- R_S tends to stabilise the Q-point against variations in transistor parameters. But it reduces the gain.



Voltage gain

$$A_V = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{gs} \cdot R_D$$

$$\begin{aligned} V_i &= V_{gs} + g_m V_{gs} R_s \\ &= V_{gs} (1 + g_m R_s) \end{aligned}$$

$$V_{gs} = \frac{V_i}{1 + g_m R_s}$$

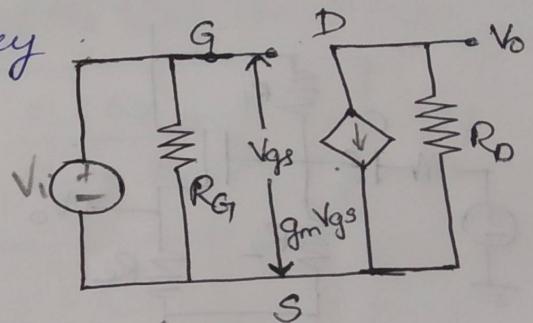
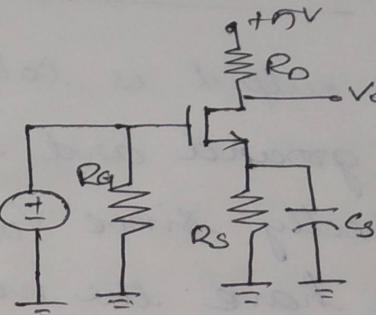
$$V_o = \frac{V_i}{1 + g_m R_s} (-g_m R_D)$$

$$\therefore A_V = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_s}$$

Common Source circuit with source bypass capacitor

A source capacitor added to the common source ckt with a source resistor will minimise the loss in the small signal voltage gain, while maintaining Q-point stability

For analysis, if the frequency is sufficiently large, the bypass capacitor acts as a short circuit.



Voltage Gain Av

$$A_V = \frac{V_o}{V_i} ; \quad V_o = -g_m V_{gs} R_o$$

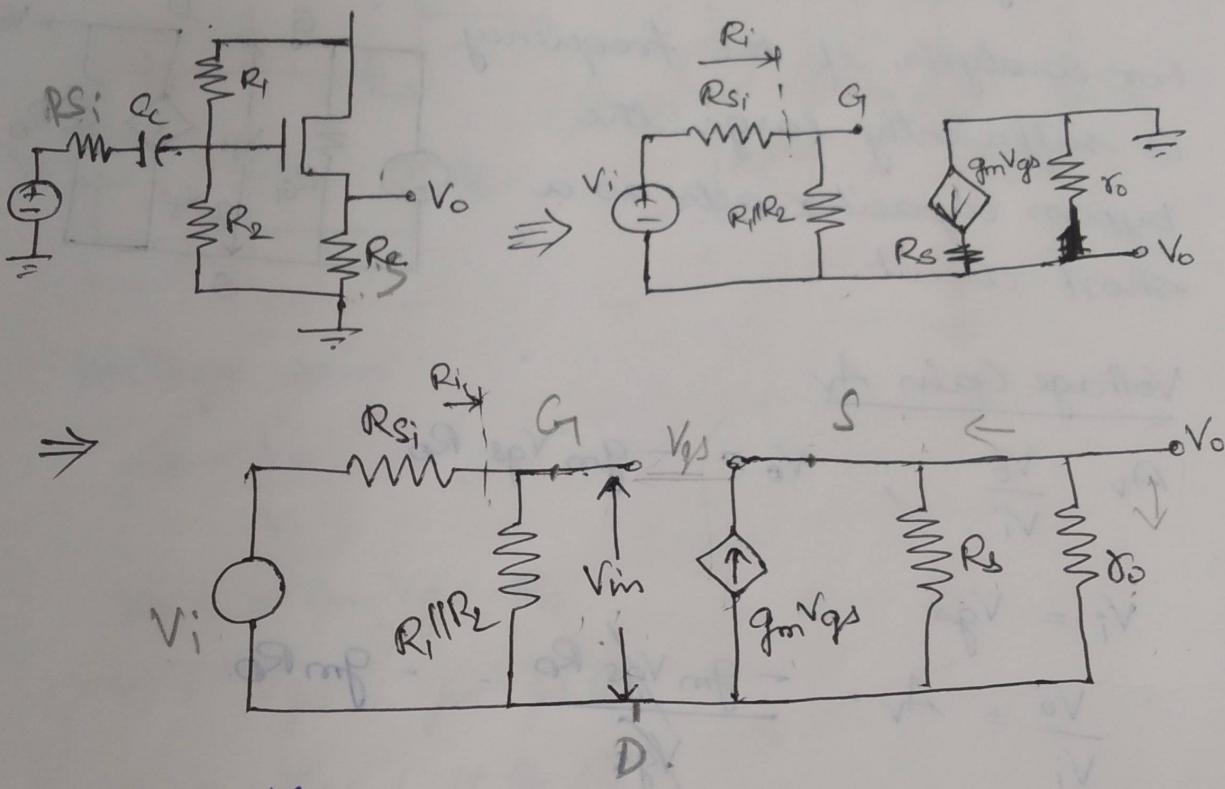
$$V_i = V_{gs}$$

$$\therefore \frac{V_o}{V_i} = A_V = \frac{-g_m V_{gs} R_o}{V_{gs}} = -g_m R_o.$$

$\therefore A_V = -g_m R_o$

Common Drain Circuit : The source follower.

The output is taken off the source with respect to ground and the drain is connected to V_{DD} directly. Since V_{DD} becomes ground in ac analysis we have the name common drain. The more common name is source follower.



$$A_v = \frac{V_o}{V_i}$$

$$V_o = g_m V_{gs} (R_s \parallel r_o)$$

$$V_{in} = \frac{V_i \times R_s \parallel R_2}{R_{si} + R_s \parallel R_2} \rightarrow ①$$

$$\begin{aligned} \text{But, } V_{in} &= V_{gs} + (g_m V_{gs}) (R_s \parallel r_o) \\ &= V_{gs} [1 + g_m (R_s \parallel r_o)] \end{aligned}$$

$$V_{gs} = \frac{V_i}{1 + g_m (R_s \parallel r_o)}$$

sub in V_o ,

$$V_o = \frac{g_m \cdot V_i (R_s \parallel r_o)}{1 + g_m (R_s \parallel r_o)} \rightarrow \textcircled{2}$$

substitute \textcircled{1} in \textcircled{2}

$$V_o = \frac{g_m V_i (R_1 \parallel R_2) (R_s \parallel r_o)}{(R_{si} + R_1 \parallel R_2) (1 + g_m (R_s \parallel r_o))}$$

$$\boxed{A_V = \frac{V_o}{V_i} = \frac{g_m (R_s \parallel r_o)}{1 + g_m (R_s \parallel r_o)} \cdot \frac{R_1 \parallel R_2}{R_{si} + R_1 \parallel R_2}}$$

(or)

$$A_V = \frac{R_s \parallel r_o}{\frac{1}{g_m} + (R_s \parallel r_o)} \cdot \frac{R_1 \parallel R_2}{R_{si} + R_1 \parallel R_2}$$

- magnitude of voltage gain is always less than unity
- op resistance is less than that of common source circuit.

2/p impedance :-

$$R_i = R_1 \parallel R_2 + \frac{r_o}{g_m} = r_{out} - r_o$$

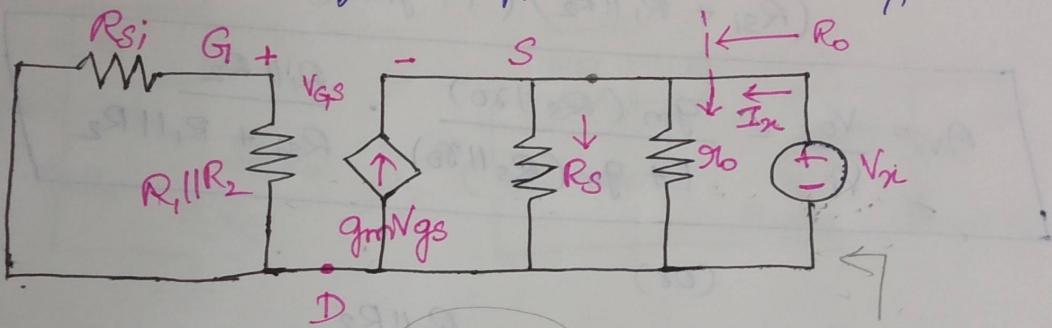
$$r_{out} + \frac{r_o}{g_m} + \frac{r_o}{g_m} = r_o$$

$$[r_{out} + V_o] \sqrt{2} = r_o$$

Output Impedance

A small op resistane is desirable when the circuit is to act as an Ideal voltage source, and drive load circuit without suffering loading effects.

To find the output resistance, let $V_i = 0$, and test voltage is applied to the op



$$- R_o = \frac{V_x}{I_x}; V_x + V_{gs} = 0 \\ \therefore V_x = -V_{gs} \\ V_{gs} = -V_x$$

- apply KCL at the op terminal.

$$I_n + g_m V_{gs} = \frac{V_x}{R_o} + \frac{V_x}{R_s}$$

Subs. $V_{gs} = -V_x$ in the above eqn

$$\therefore I_n - g_m V_x = \frac{V_x}{R_o} + \frac{V_x}{R_s}$$

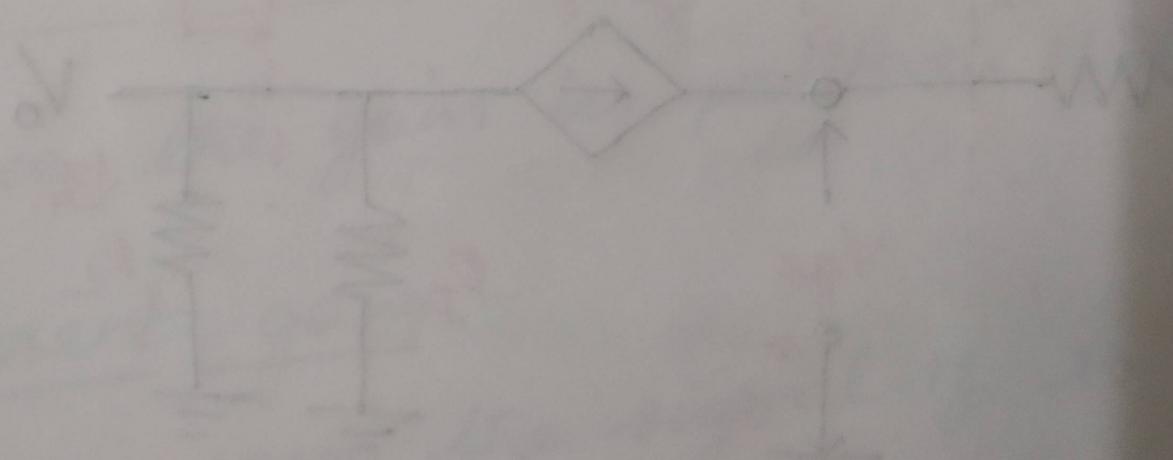
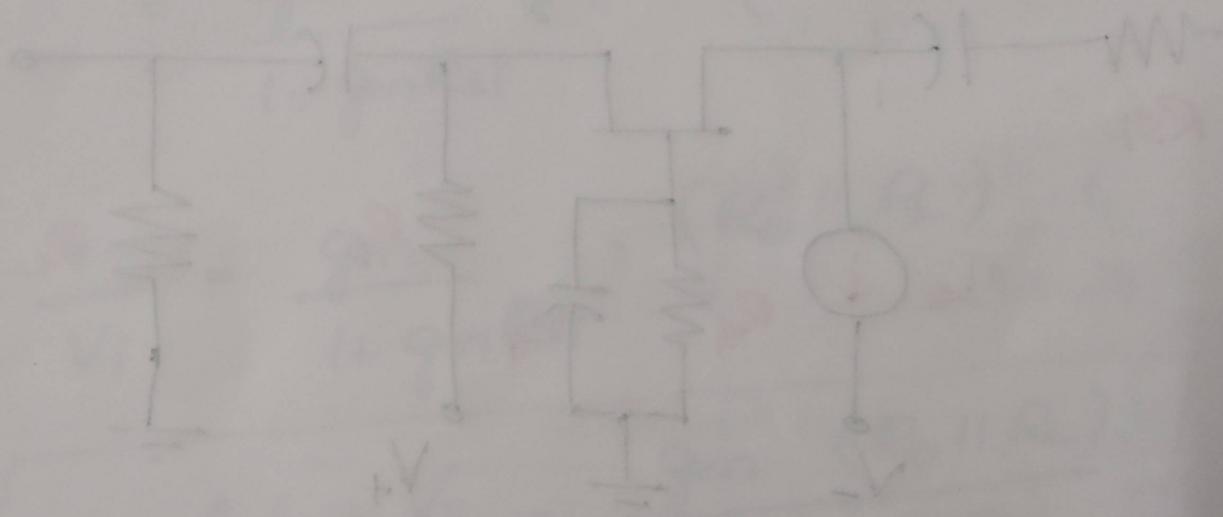
$$\Rightarrow I_n = \frac{V_x}{R_o} + \frac{V_x}{R_s} + g_m V_x$$

$$= V_x \left[\frac{1}{R_o} + \frac{1}{R_s} + g_m \right]$$

$$\therefore V_x = I_n \left(r_o \parallel R_s \parallel \frac{1}{g_m} \right)$$

$$\frac{V_x}{I_n} = r_o \parallel R_s \parallel \frac{1}{g_m}$$

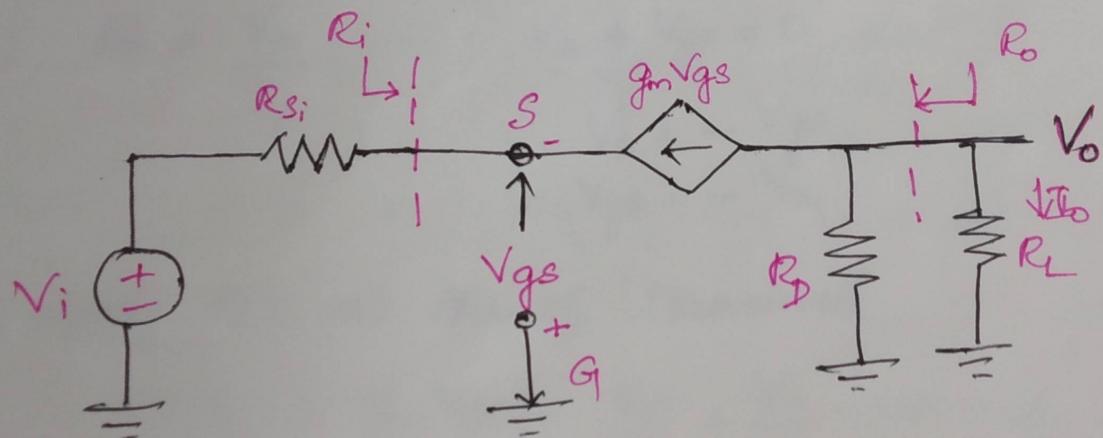
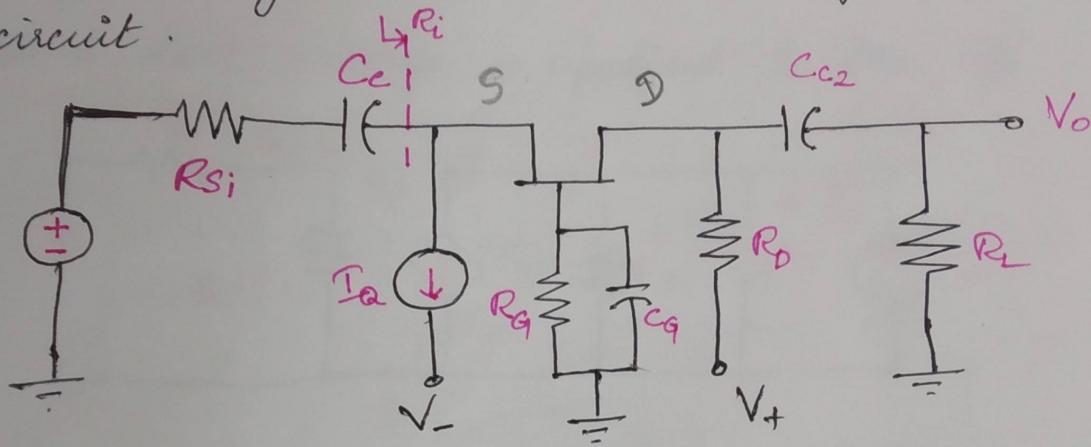
$$\boxed{\therefore R_o = \frac{V_x}{I_n} = r_o \parallel R_s \parallel \frac{1}{g_m}}$$



Common Gate Configurations

- The V_p is applied to the source terminal and the gate is at signal ground.
- Biasing current I_Q .

Circuit diagram and small signal equivalent circuit.



- $A_V = \frac{V_o}{V_i}$; $V_o = g_m V_{gs} (R_D || R_L)$
- $V_i = I_i R_{S1} - V_{gs}$
 $\Rightarrow I_i = -g_m V_{gs}$
- $V_i = -g_m V_{gs} \cdot R_{S1} - V_{gs}$
 $= -V_{gs} [g_m R_{S1} + 1]$

$$V_{gs} = -\frac{V_i}{1 + g_m R_{si}}$$

substitute the above eqn in V_o ,

$$\begin{aligned} V_o &= -g_m \cdot V_{gs} (R_D \parallel R_L) \\ &= -g_m \cdot \frac{-V_i}{1 + g_m R_{si}} \cdot (R_D \parallel R_L) \\ &= \frac{g_m \cdot V_i}{1 + g_m R_{si}} \cdot (R_D \parallel R_L) \end{aligned}$$

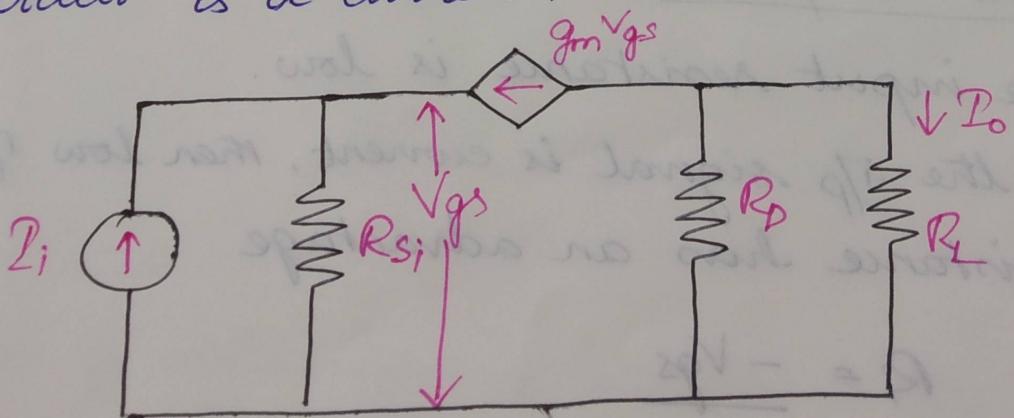
$$\frac{V_o}{V_i} = \frac{g_m}{1 + g_m R_{si}} \cdot (R_D \parallel R_L)$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{g_m \cdot (R_D \parallel R_L)}{1 + g_m R_{si}}$$

since the gain is positive, i_p & ϕ_p are in phase

current gain :-

In many cases the signal i_p to common gate circuit is a current.



$$A_i = \frac{I_o}{I_i} ; \quad I_o = -g_m V_{gs} \times \frac{R_D}{R_L + R_D}$$

Apply KCL to the IP :

$$\Rightarrow I_i + \frac{V_{gs}}{R_{si}} + g_m V_{gs} = 0$$

$$-I_i = V_{gs} \left(\frac{1}{R_{si}} + g_m \right)$$

$$\Rightarrow V_{gs} \left(\frac{1 + g_m R_{si}}{R_{si}} \right) = -I_i$$

$$\Rightarrow V_{gs} = -\frac{I_i \times R_{si}}{1 + g_m R_{si}}$$

$$I_o = \frac{g_m R_D}{R_D + R_L} \cdot \frac{R_{si}}{1 + g_m R_{si}} \cdot I_i$$

$$\Rightarrow A_i = \frac{I_o}{I_i} = \frac{g_m \cdot R_D \cdot R_{si}}{(1 + g_m R_{si})(R_D + R_L)}$$

when $R_D \gg R_L$ &

$$g_m R_{si} \gg 1$$

$A_i \approx 1$ for CG circuit.

Input Impedance

- The input resistance is low.
- If the IP signal is current, then low IP resistance has an advantage

$$R_i = \frac{-V_{gs}}{I_i}$$

$$R_i = -g_m V_{gs}$$

$$\therefore R_i = \frac{-V_{gs}}{-g_m V_{gs}} = Y_{gm}.$$

$$R_i = Y_{gm}$$

O/p Resistance

$$R_o = R_D.$$

$$(R_o + R_D) \frac{dV_{out}}{dI} = -V_{out}$$

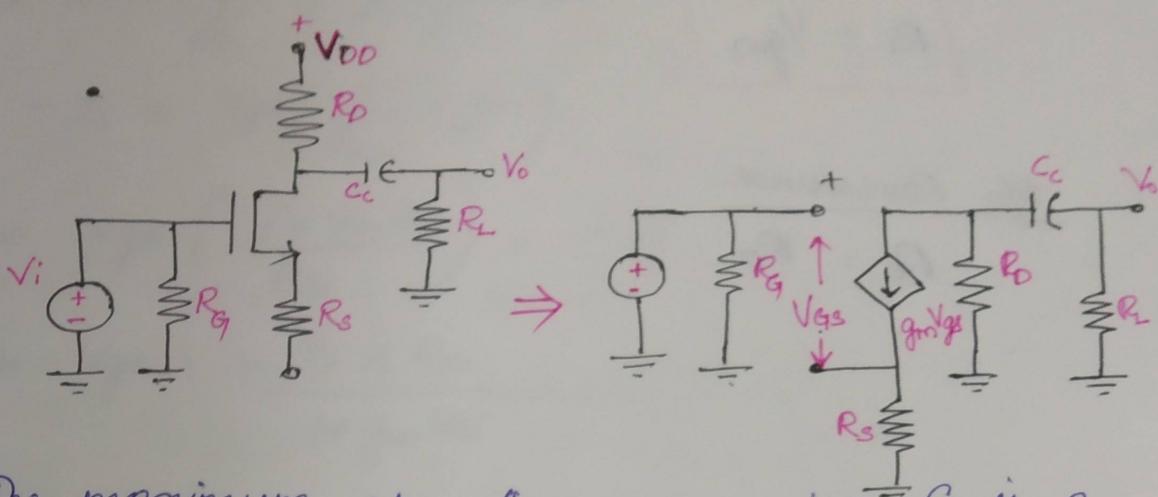
$$2R_o \frac{dV_{out}}{dI} + \frac{dV_{out}}{dI} = -V_{out}$$

$$[2R_o + 1] \frac{dV_{out}}{dI} = -V_{out}$$

$$\frac{V_{out}}{2R_o + 1} = -V_{out}$$

Output coupling capacitor:

Common source circuit.



- The maximum op voltage assuming C_C is a short circuit is,

$$|V_o|_{\max} = g_m V_{gs} (R_D \parallel R_L)$$

$$V_i = V_{gs} + g_m V_{gs} R_s$$

$$= V_{gs} [1 + g_m R_s]$$

$$\Rightarrow V_{gs} = \frac{V_i}{1 + g_m R_s}$$

$$V_o = g_m \cdot \frac{V_i}{1 + g_m R_s} \cdot (R_D \parallel R_L)$$

$$A_V = \frac{V_o}{V_i} = \frac{g_m (R_D \parallel R_L)}{1 + g_m R_s}$$

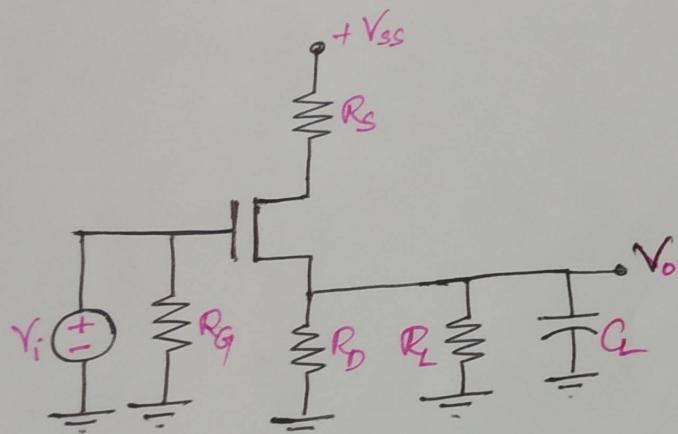
- The time constant is a function of the effective resistance seen by capacitor C_C , which is determined by setting independent source = 0.

$$f_L = \frac{1}{2\pi T_3}$$

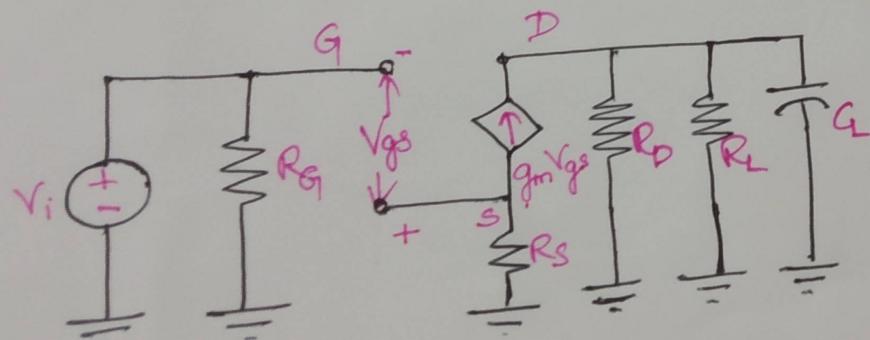
$$V_i = 0, g_m V_{gs} = 0. \text{ Then, } r_g = C_C (R_D + R_L)$$

Load capacitor effects:-

- fig shows a MOSFET common source amplifier with a load resistor R_L & a load capacitor C_L , connected to the op.
- for the ac equivalent circuit r_o is assumed to be ∞
- The circuit is like a low pass filter
- At high frequencies, the impedance of C_L decreases, and acts as a shunt between op and ground, and the op voltage is zero.



- The equivalent resistance seen by load capacitor C_L is $(R_D \parallel R_L)$
- since we set $V_i = 0$, then $g_m V_{gs} = 0$, which means that the dependent current source does not affect the equivalent resistance.



Time constant

$$\tau_p = (R_D \parallel R_L) C_L$$

- The maximum gain with C_L is open circuit, is

$$|A_v|_{\max} = \frac{g_m (R_D \parallel R_L)}{1 + g_m R_S}$$