# VLSI Design Lab

## Experiment - 4

### I Pre-Lab Questions:

1. Write the expression for propagate and generate term in CLA.

Soln. Carry Propagate $P_i = A_i \oplus B_i$

Carry Generate $= A_i B_i$

2. List the efficient method for implementing 64-adder using CLA Technique.

Soln. Use the same design as the 16 bit CLA adder.

### II Post-Lab Questions:

1. Compare the area, delay and power report of Ripple Carry and Carry look-ahead adder in Xilinx ISE. Create a Comparision Chart and justify the results.

Soln.

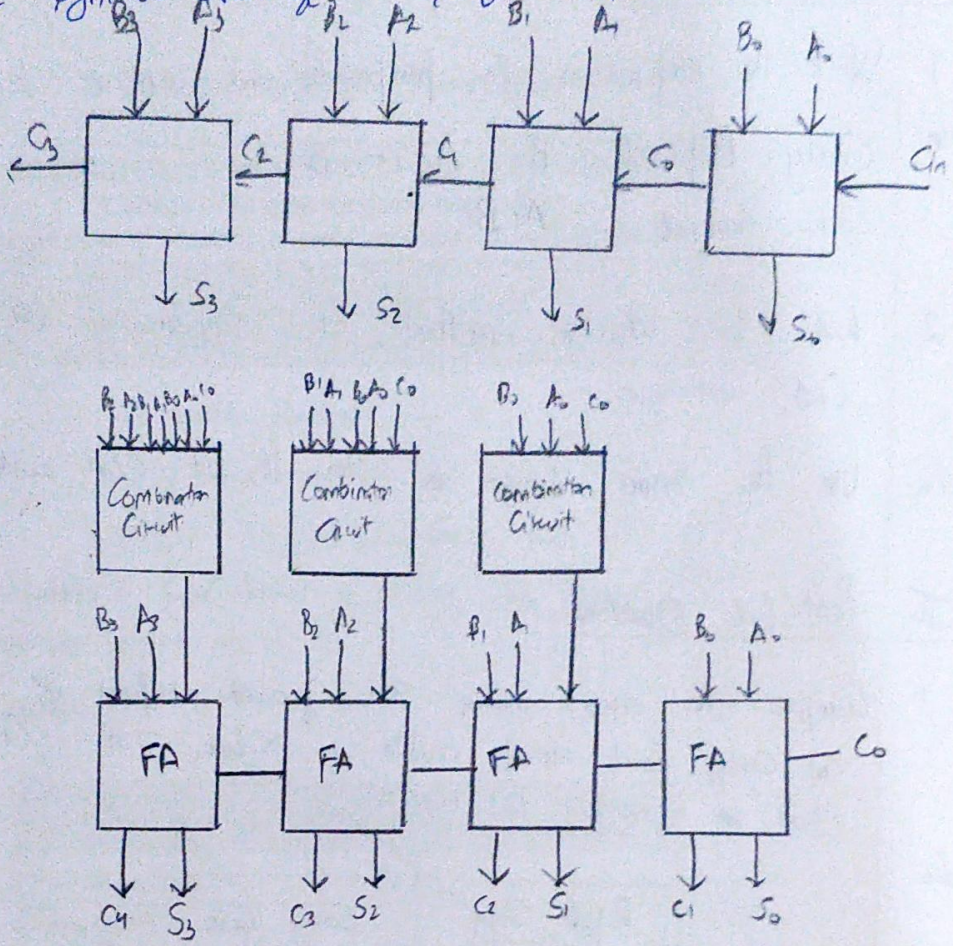
| | Ripple Carry Adder | Carry look ahead adder |
|---|---|---|
| Area | Larger | Smaller |
| Delay | Slower | Faster |
| Power | Lower | Higher |

2. List the application of CLA in VLSI Design.

Soln. A Carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits. If Carry look ahead adder Calculates one of more Carries before the Sum, which reduces the wait time to Calculate the result of the larger value bits of the adder.

3. Prepare the Synthesis Chart of a 4-bit CLA.

Soln.




4. Can retiming mechanism improve the Speed further in CLA architecture?

Soln. Yes. Retiming is a technique used in digital circuit design to optimize the timing of a circuit by moving the flip-flops and combinational logic blocks within the circuit to minimize the critical path delay.

RESULT:

Thus, the design of a 4-bit Carry Look Ahead adder circuit was simulated in Verilog and Synthesized using EDA tool.