

1. P-N DIODE CHARACTERISTICS

1.1 Objective

To study the Volt-Ampere Characteristics of Silicon P-N Junction Diode and to find its cut-in voltage, static and dynamic resistances.

1.2 Hardware Required

S. No	Apparatus	Type	Range	Quantity
01	PN Junction Diode	1N4001		1
02	Resistance		1k ohm, 10% tolerance, 1/2 watt rating	1
03	Regulated power supply		(0 – 30V), 2A Rating	1
04	Ammeter	MC	(0-30)mA, (0-500)µA	1
05	Voltmeter	MC	(0 – 1)V, (0 – 30)V	1
06	Bread board Connecting wires			1 Few

1.3 Introduction

Donor impurities (pentavalent) are introduced into one-side and acceptor impurities into the other side of a single crystal of an intrinsic semiconductor to form a p-n diode with a junction called depletion region . This region gives rise to a barrier potential V_b called **Cut-in Voltage**. This is the voltage across the diode at which it starts conducting. The P-N junction can conduct beyond this Potential.

The P-N junction supports uni-directional current flow. If (+)^{ve} terminal of the input supply is connected to anode (P-side) and (-)^{ve} terminal of the input supply is connected to cathode (N- side), then diode is said to be forward biased. In this condition the height of the potential barrier at the junction is lowered by an amount equal to given forward biasing voltage.

Both the holes from p-side and electrons from n-side cross the junction simultaneously and constitute a forward current (**injected minority current** – due to holes crossing the junction and entering N-side of the diode and current due to electrons crossing the junction and entering P-side of the diode). Assuming current flowing through the diode to be very large, the diode can be approximated as short-circuited switch. If (-)^{ve} terminal of the input supply is connected to anode (p-side) and (+)^{ve} terminal of the input supply is

connected to cathode (n-side) then the diode is said to be reverse biased. In this condition an amount equal to reverse biasing voltage increases the height of the potential barrier at the junction.

Both the holes on p-side and electrons on n-side tend to move away from the junction thereby increasing the depleted region. However the process cannot continue indefinitely, thus a small current called **reverse saturation current** continues to flow in the diode. This small current is due to thermally generated carriers. Assuming current flowing through the diode to be negligible, the diode can be approximated as an open circuited switch.

1.4 Circuit diagram:

1.4.1 Forward Bias

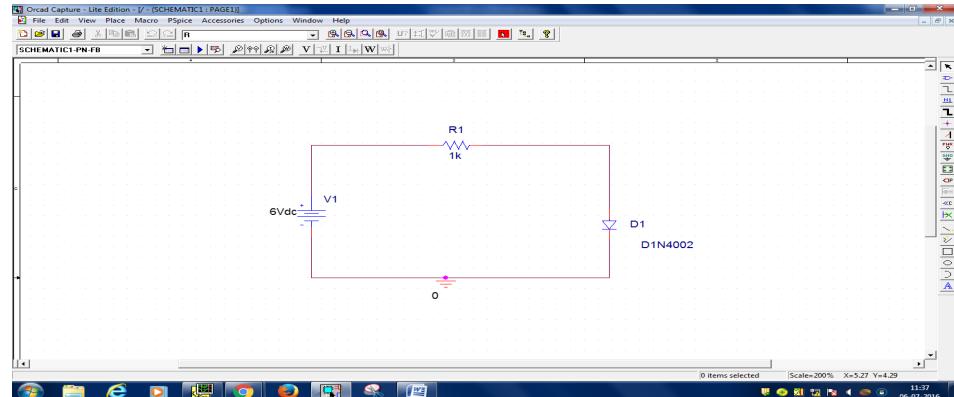
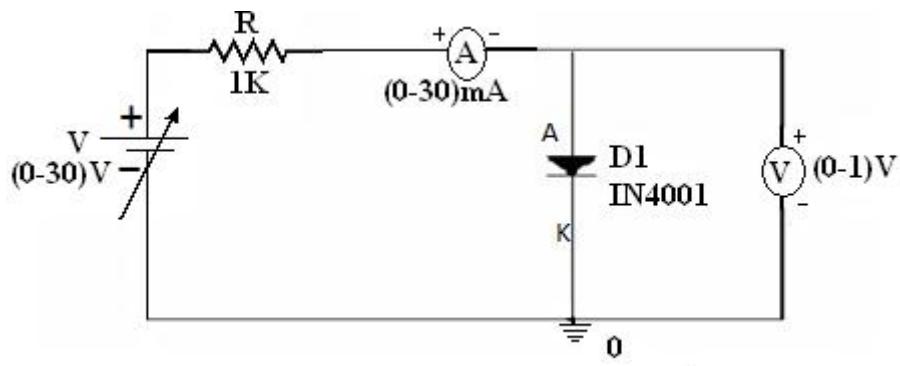
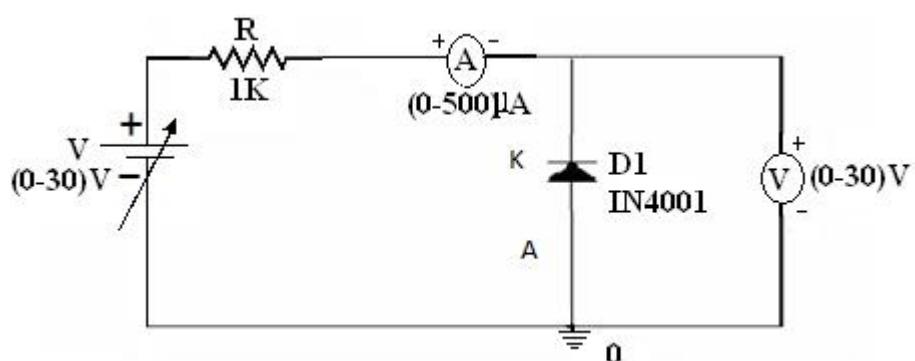


Fig 1.1 Circuit diagram for Forward bias

1.4.2 Reverse Bias



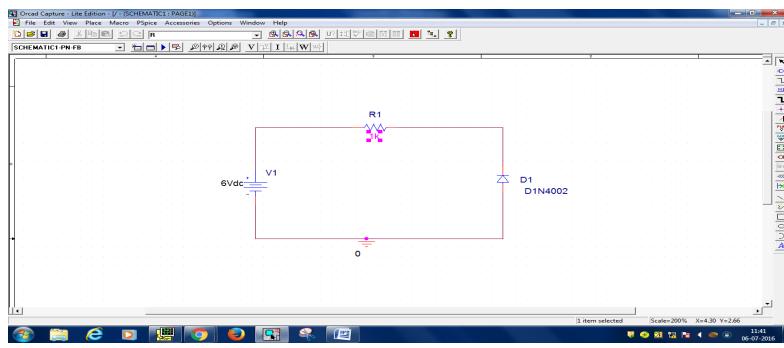


Fig 1.2 Circuit diagram for Reverse bias

1.5 Precautions

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage of the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

1.6 Characteristics of PN junction diode

1. Breakdown voltage can be traded with switching speed. A reduction in recombination lifetime through addition of suitable impurities will increase leakage current. This can be countered by decreasing diode area which however will lead to reduced forward current rating unless doping is increased. This will lead to a reduced breakdown voltage.
2. The breakdown voltage and reverse recovery are also related together in more direct manner. Regions which have higher doping also have a lower recombination lifetime so that a lower breakdown voltage diode is likely to have lower lifetime and better switching speeds. So a **single diode** cannot meet the diverse applications.

1.7 Procedure

1.7.1 Forward Biased Condition

1. Connect the PN Junction diode in forward bias (i.e)anode is connected to positive of the power supply and cathode is connected to negative of the power supply .
2. Use a Regulated power supply of range (0-30) V and a series resistance of $1\text{k}\Omega$.

3. For various values of forward voltage (V_f) note down the corresponding values of forward current (I_f).

1.7.2 Reverse Biased condition

4. Connect the PN Junction diode in Reverse bias i.e; anode is connected to negative of the power supply and cathode is connected to positive of the power supply.
5. For various values of (V_r) note down the corresponding values of reverse current (I_r).

1.8 Tabular column

1.8.1 Forward Bias

S. No	V_f (volts)	I_f (mA)

1.8.2 Reverse Bias

S. No	V_r (volts)	I_r (μ A)

1.9 Model Graph

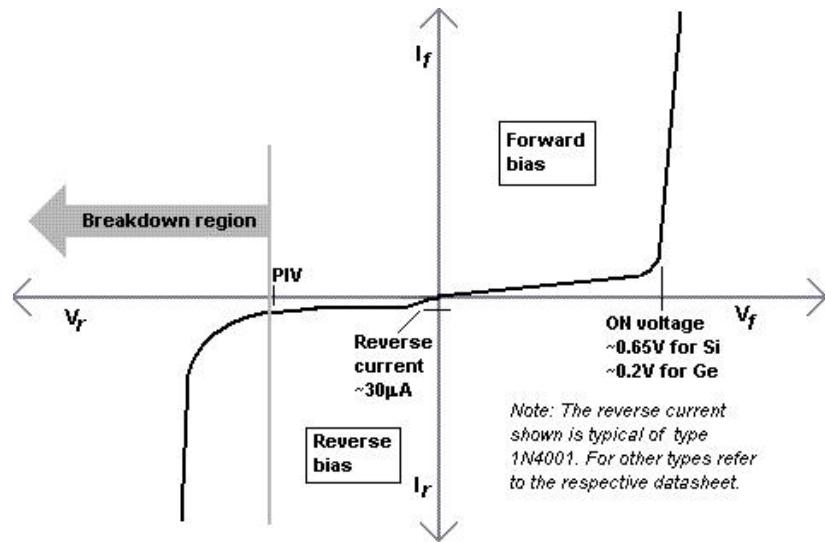


Fig 1.3 Model graph

Forward Bias

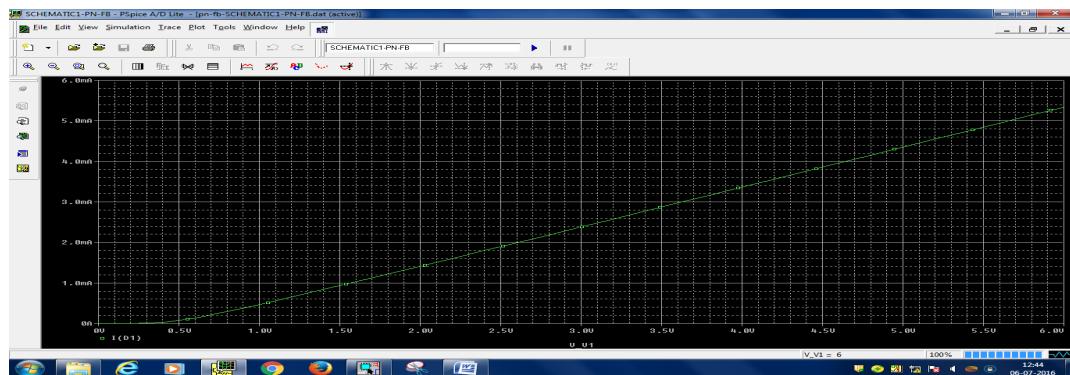


Fig 1.4 PSPICE Simulation output for Forward Bias

Reverse Bias

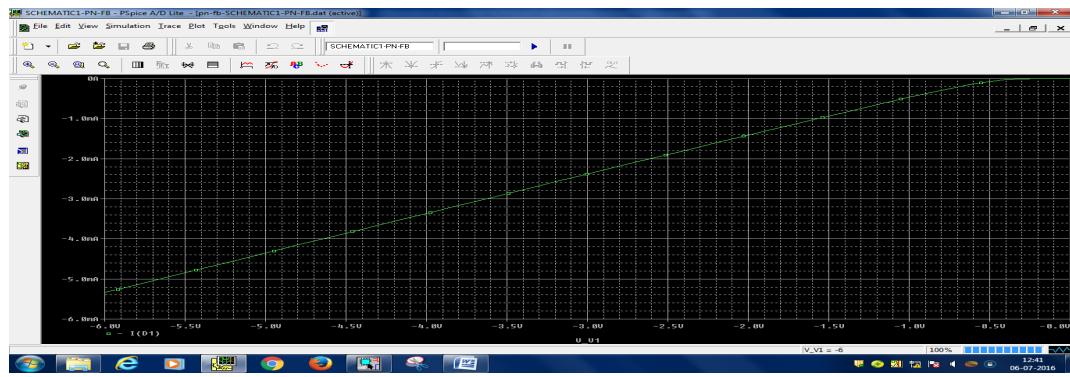


Fig 1.5 PSPICE Simulation output for Reverse Bias

1.10 Result

Thus the VI characteristic of PN junction diode was verified.

- i. Cut in voltage = V
- ii. Static forward Resistance $r_{dc}(V_f/I_f)$ = Ω
- iii. Dynamic forward Resistance $r_{ac}(\Delta V_f/\Delta I_f)$ = Ω
- iv. Static Reverse Resistance $r_{dc}(V_r/I_r)$ = Ω
- v. Dynamic Reverse Resistance $r_{ac}(\Delta V_r/\Delta I_r)$ = Ω

1.11 Pre lab Questions

1. What is the need for doping?
2. How depletion region is formed in the PN junction?
3. What is break down voltage?
4. What is cut-in or knee voltage? Specify its value in case of Ge or Si?
5. What are the differences between Ge and Si diode?
6. What is the relationship between depletion width and the concentration of impurities?

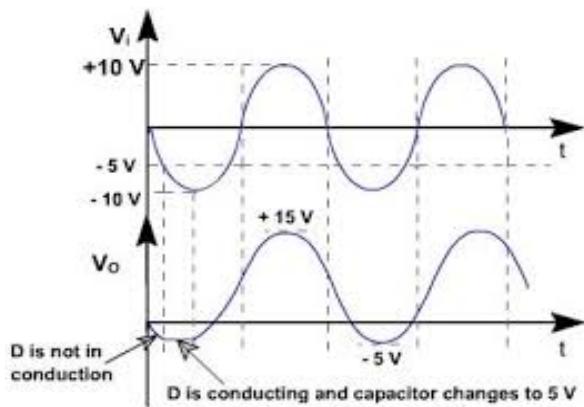
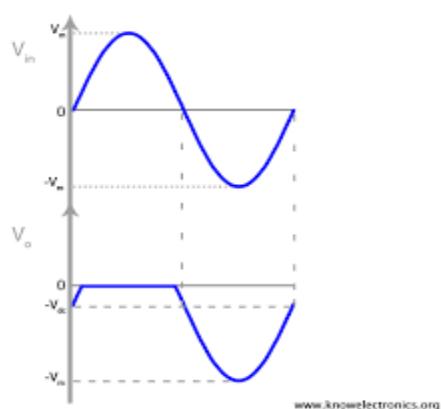
1.12 Post lab Questions

1. How does PN-junction diode acts as a switch?
2. Comment on diode operation under zero biasing condition.
3. For a uniformly doped silicon PN junction diode with an N-type doping of 10^{16} cm^{-3} and a P-type doping of $2 \times 10^{16} \text{ cm}^{-3}$, what fraction of the built-in voltage is dropped in the N-region? Where will most of the built-in voltage be dropped if the P type doping is much larger than the N-type doping?
4. The depletion capacitance/Area measured for a symmetrical Silicon PN junction at different bias voltages is given below:

Bias	Capacitance (F/cm^2)
0.25	3×10^{-8}
0.0	2.44×10^{-8}
-0.5	1.86×10^{-8}
-0.7	1.72×10^{-8}

- (a) Determine the doping of N and P-regions, (b) Determine the built-in voltage
 (c) Determine the depletion width at zero bias

5. Draw the circuits used to get the following outputs.



2. ZENER DIODE CHARACTERISTICS

2.1 Objective

To study the Volt-Ampere characteristics of Zener diode and to measure the Zener break down voltage.

2.2 Hardware Required

S. No	Apparatus	Type	Range	Quantity
01	Zener Diode	IZ 6.2		1
02	Resistance		1k ohm, 10% tolerance, 1/2 watt rating	1
03	Regulated power supply		(0 – 30V), 2A rating	1
04	Ammeter	mC	(0-30)mA	1
05	Voltmeter	mC	(0 – 1)V, (0 – 10)V	1
06	Bread board			1
	Connecting wires			Few

2.3 Introduction

An ideal P-N Junction diode does not conduct in reverse biased condition. A **Zener diode** conducts excellently even in reverse biased condition. These diodes operate at a precise value of voltage called break down voltage. A **Zener diode** when forward biased behaves like an ordinary P-N junction diode. A **Zener diode** when reverse biased can either undergo **avalanche breakdown** or **Zener breakdown**.

Avalanche breakdown:-If both p-side and n-side of the diode are lightly doped, depletion region at the junction widens. Application of a very large electric field at the junction may rupture covalent bonding between electrons. Such rupture leads to the generation of a large number of charge carriers resulting in **avalanche multiplication**.

Zener breakdown:-If both p-side and n-side of the diode are heavily doped, depletion region at the junction reduces. Application of even a small voltage at the junction ruptures covalent bonding and generates large number of charge carriers. Such sudden increase in the number of charge carriers results in **Zener mechanism**.

2.4 Circuit diagram

2.4.1 Forward Bias

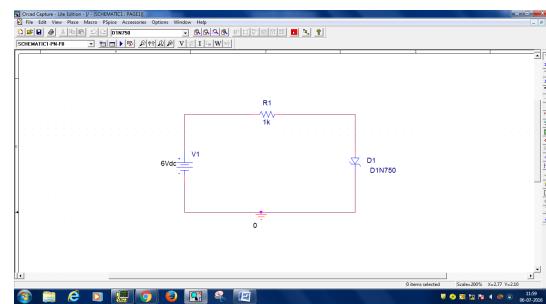
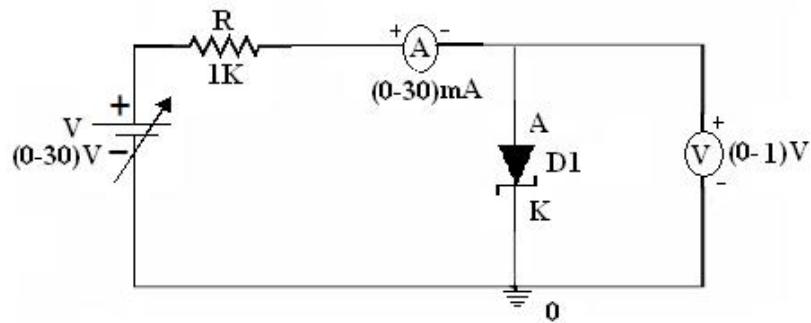


Fig 2.1 Circuit diagram for Forward bias

2.4.2 Reverse Bias

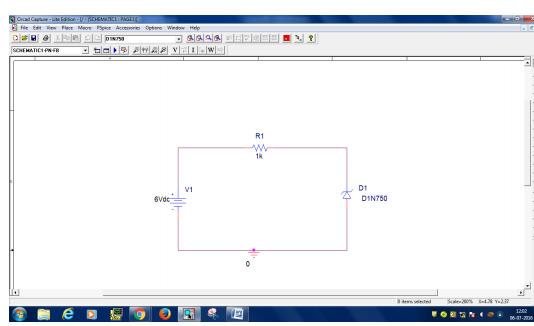
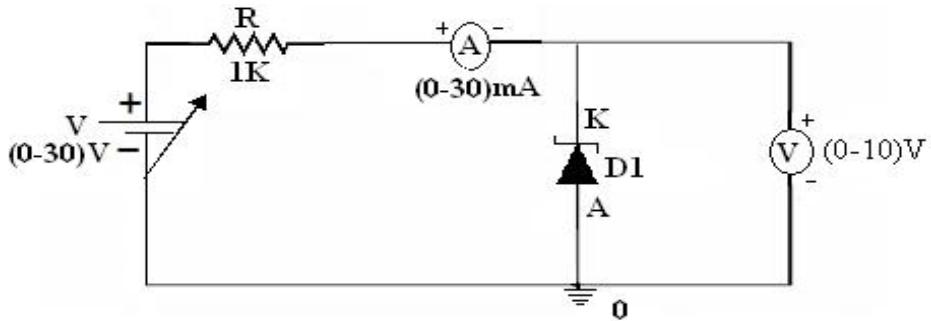
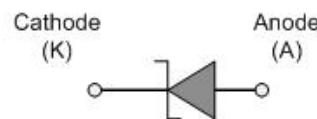


Fig 2.2 Circuit diagram for Reverse bias

2.4.3 Zener Diode Symbol



2.5 Precautions

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage of the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

2.6 Characteristics of Zener Diode

For IZ6.2 Zener diode,

Forward Bias

At a given (constant) diode current, V exhibits an approximately linear shift in the VI -characteristic due to the combined effect of the temperature dependences of both I_s and V_T

Typically, the VI -characteristic shifts approximately $-2 \text{ mV}/^\circ\text{C}$.

Reverse Bias

The temperature dependence of the reverse current is that of I_S alone, which changes exponentially as a function of temperature. Typically, I_S approx. doubles for every 10°C increase in Temperature. These variations may lead to significant changes in the operation of a circuit over a large temperature range and, in many applications, requires compensation strategies to be implemented in the design of some circuits.

2.7 Procedure

2.7.1 Forward Biased Condition

1. Connect the Zener diode in forward bias i.e; anode is connected to positive of the power supply and cathode is connected to negative of the power supply as in circuit
2. Use a Regulated power supply of range (0-30) V and a series resistance of $1\text{k}\Omega$.
3. For various values of forward voltage (V_f) note down the corresponding values of forward Current (I_f).

2.7.2 Reverse biased condition

1. Connect the Zener diode in Reverse bias i.e; anode is connected to negative of the power supply and cathode is connected to positive of the power supply as in circuit.
2. For various values of reverse voltage (V_r) note down the corresponding values of reverse current (I_r).

2.8 Tabular column

2.8.1 Forward Bias

S. No	V_f (volts)	I_f (mA)

2.8.2 Reverse Bias

S. No	V_r (volts)	I_r (mA)

2.9 Model Graph

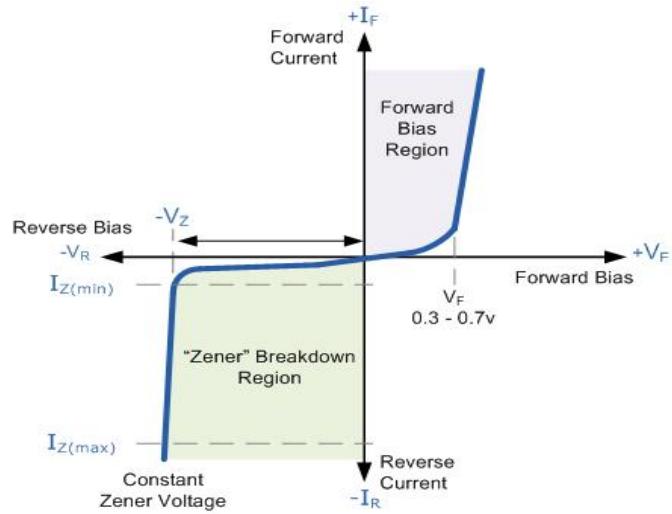


Fig 2.3 Model graph

Forward Bias

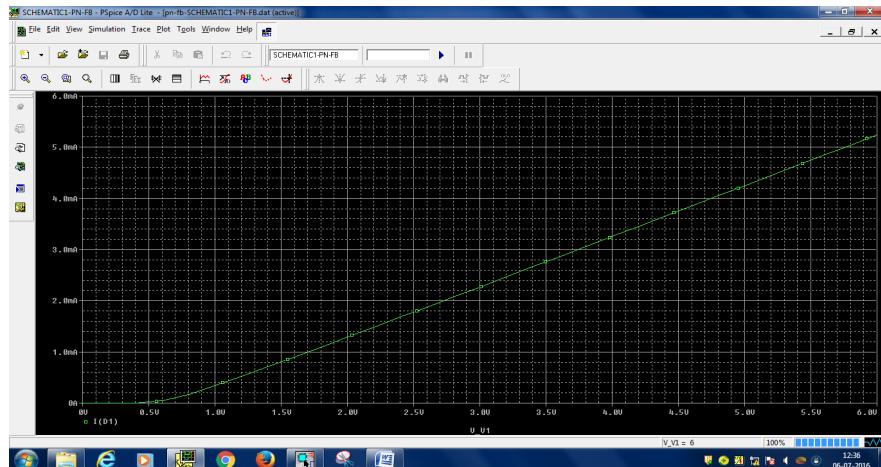


Fig 2.4 PSPICE Simulation output for Forward Bias

Reverse Bias

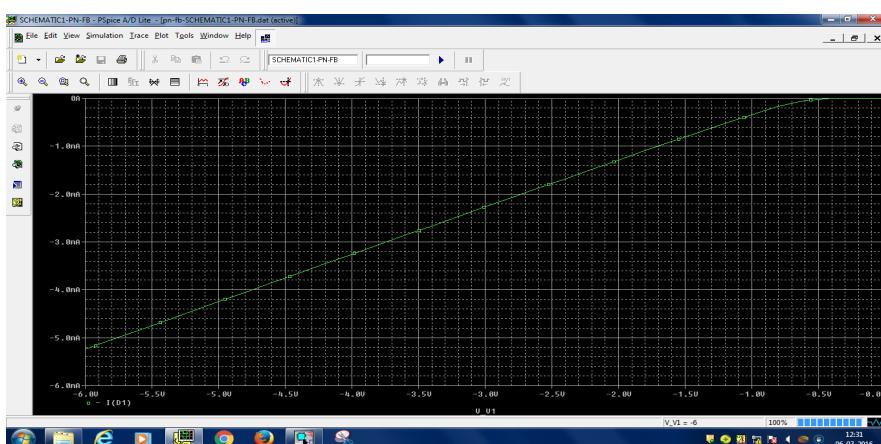


Fig 2.5 PSPICE Simulation output for Reverse Bias

2.10 Result

The Zener diode characteristics have been verified and the following parameters were calculated

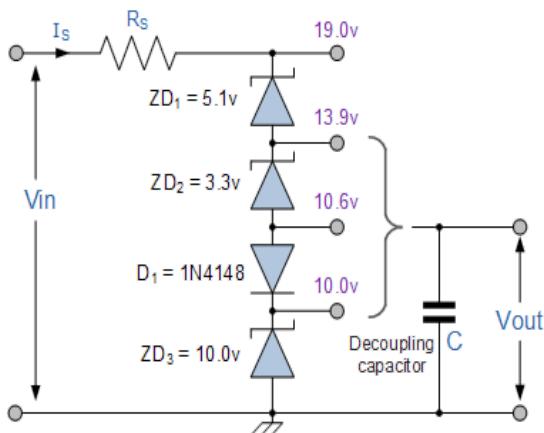
- i) Cut in voltage = V
- ii) Break down voltage = V

2.11 Pre lab Questions

1. Explain the concept of Zener breakdown?
2. How depletion region gets thin by increasing doping level in Zener diode?
3. State the reason why an ordinary diode suffers avalanche breakdown rather than Zener breakdown?
4. Give the reasons why Zener diode acts as a reference element in the voltage regulator circuits.
5. What type of biasing must be used when a Zener diode is used as a regulator?

2.12 Post lab Questions

1. Design a DC power supply network using Zener diode.
2. What happens when the Zener diodes are connected in series?



3. Justify the use of zener diode in a stabilization circuit?
4. How will you differentiate the diodes whether it is Zener or avalanche when you are given two diodes of rating 6.2 v and 24V?
5. How does a zener diode protect meters from excess voltage that is applied accidentally?

3. DIODE RECTIFIER CIRCUITS

3.1 Objective

To design and construct the diode rectifier circuit and analyze the following parameters

- a. To plot Output waveform of the rectifier
- b. To find ripple factor using formulae
- c. To find the efficiency
- d. To stimulate the same using orcad PSPICE capture

3.2 Hardware Required

S. No	Apparatus	Type	Range	Quantity
01	Step down Transformer		(6-0-6)V, 500mA, 1A Rating	1
02	Resistance		470 ohm, 10% tolerance, 1/2 watt rating	1
03	Capacitor		470 μ F	1
04	Diode	IN4001		1
05	Bread board			1
	connecting wires			Few

3.3 Half wave rectifier

A device is capable of converting a sinusoidal input waveform into a unidirectional waveform with non-zero average component is called a rectifier. A practical half wave rectifier with a resistive load is shown in the circuit diagram. In positive half cycle, Diode D is forward biased and conducts. Thus the output voltage is same as the input voltage. In the negative half cycle, Diode D is reverse biased, and therefore output voltage is zero. A smoothing filter is induced between the rectifier and load in order to attenuate the ripple component. The filter is simply a capacitor connected from the rectifier output to ground. The capacitor quickly charges at the beginning of a cycle and slowly discharges through R_L after the positive peak of the input voltage. The variation in the capacitor voltage due to charging and discharging is called ripple voltage. Generally, ripple is undesirable, thus the smaller the ripple, the better the filtering action.

Ripple factor is a measure of effectiveness of a rectifier circuit and defined as a ratio of RMS value of ac component to the dc component in the rectifier output.

Theoretical calculations for Ripple Factor:

Without Filter:

$$V_{rms} = V_m / 2$$

$$V_{dc} = \frac{V_m}{\pi}$$

$$\text{Ripple factor (Theoretical)} = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = 1.21$$

$$\text{Ripple Factor (practical)} \gamma = \frac{V_{ac}}{V_{dc}} \text{ where } V_{ac} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$$

With Filter:

$$\text{Ripple Factor (Theoretical)} r = \frac{1}{2\sqrt{3}fCR}$$

Where $f = 50\text{Hz}$, $R = 1\text{K}\Omega$, $C = 1000\mu\text{F}$

$$V_{ac} = \frac{V_r(p-p)}{2\sqrt{3}}$$

$$V_{dc} = V_m - \frac{V_r(p-p)}{2}$$

$$\text{Ripple Factor (practical)} \gamma = \frac{V_{ac}}{V_{dc}}$$

$$\text{Percentage Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} * 100\%$$

V_{NL} = DC voltage at the load without connecting the load (Minimum current).

V_{FL} = DC voltage at the load with load connected.

$$\text{Efficiency } \eta = \frac{P_{DC}}{P_{AC}}$$

$$P_{AC} = V_{2rms} / R_L$$

$$P_{DC} = V_{dc} / R_L$$

The ripple factor can be lowered by increasing the value of the filter capacitor or increasing the load capacitance.

3.4 Circuit Diagram of Half Wave Rectifier

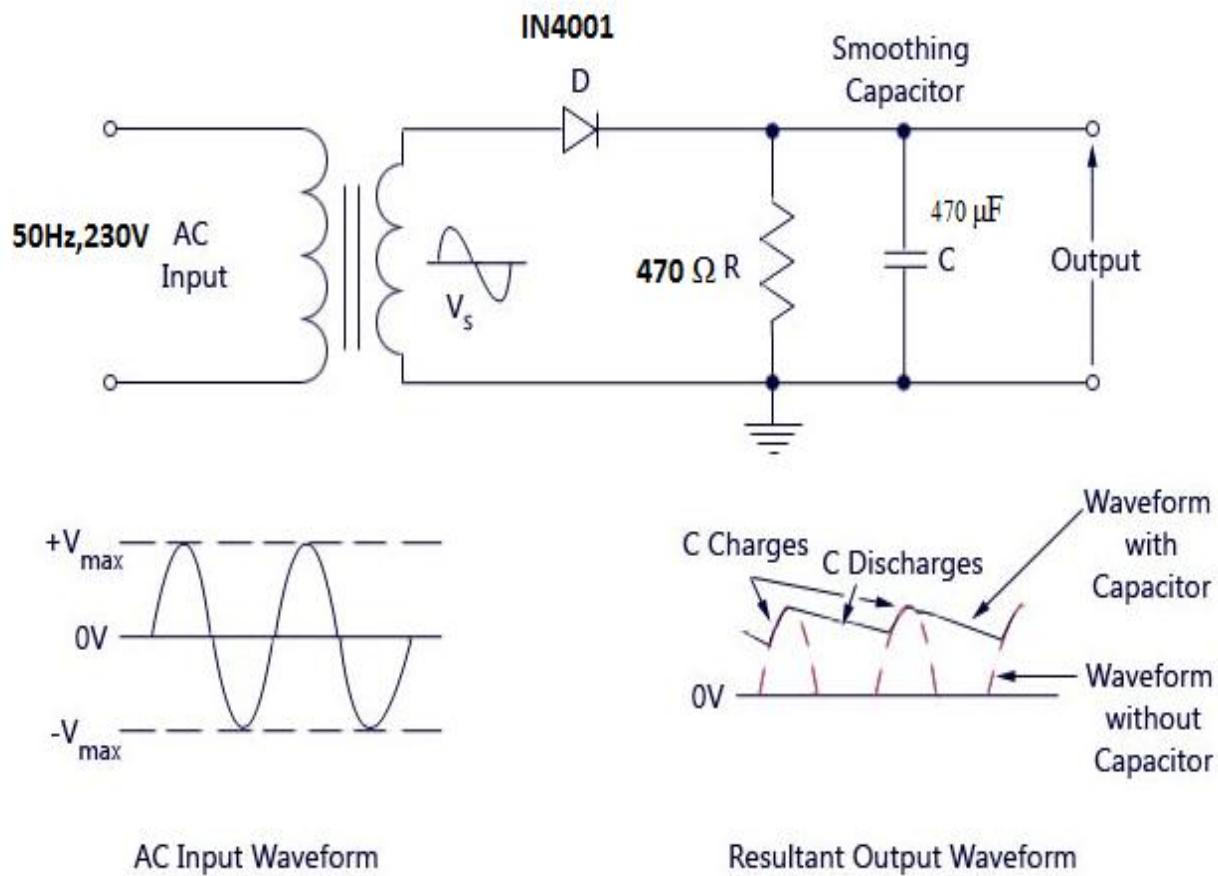


Fig 3.1 Circuit diagram and model graph of half wave rectifier

3.5 Observations

	Input Waveform	Output Waveform (without filter)	Ripple Voltage (with filter)
Amplitude			
Time Period			
Frequency			

3.6 Pspice circuit diagram for Half Wave Rectifier(with out filter)

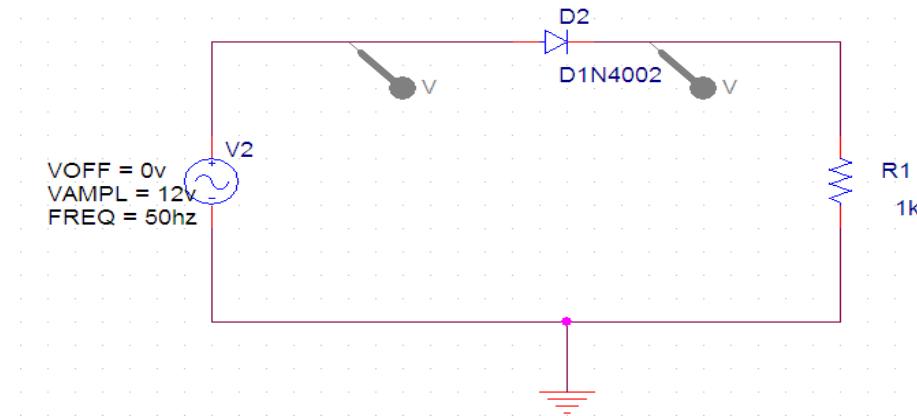


Fig 3.2 PSPICE schematic diagram of half wave rectifier without filter

3.7 Simulation graph for Half wave rectifier without filter

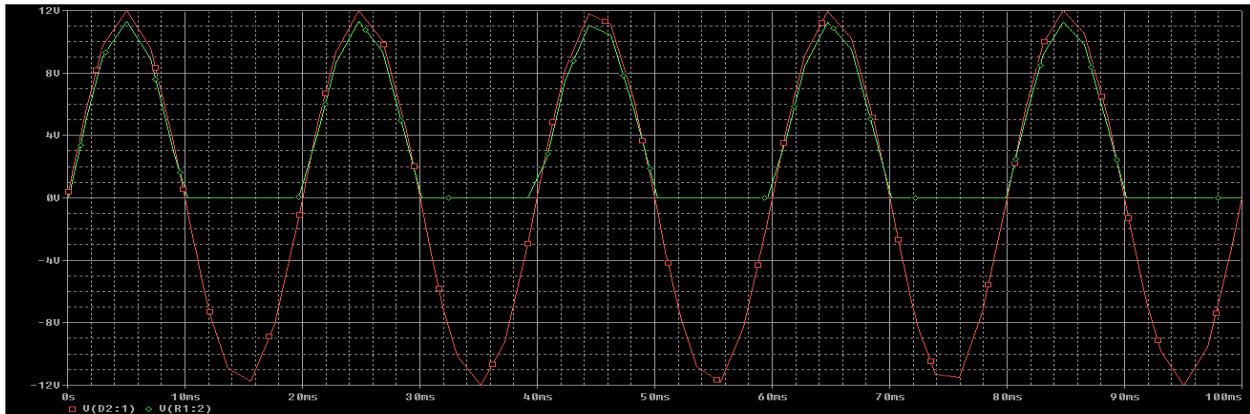


Fig 3.3 PSPICE simulation diagram of half wave rectifier without filter

3.8 Pspice circuit diagram for Half Wave Rectifier(with filter)

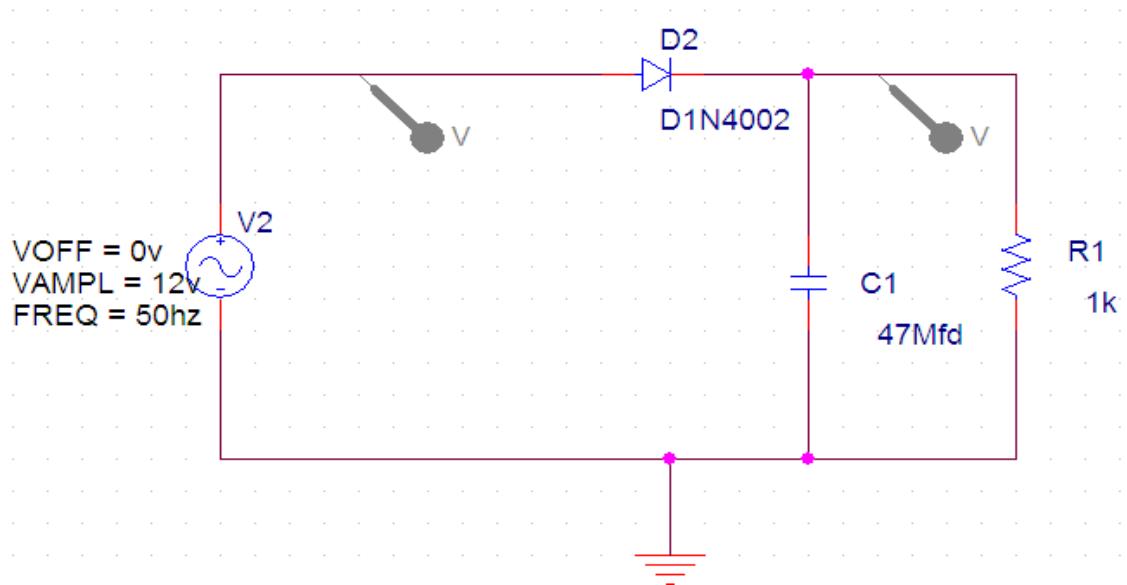


Fig 3.4 PSPICE schematic diagram of half wave rectifier with filter

3.9 Simulation graph for Half wave rectifier with filter

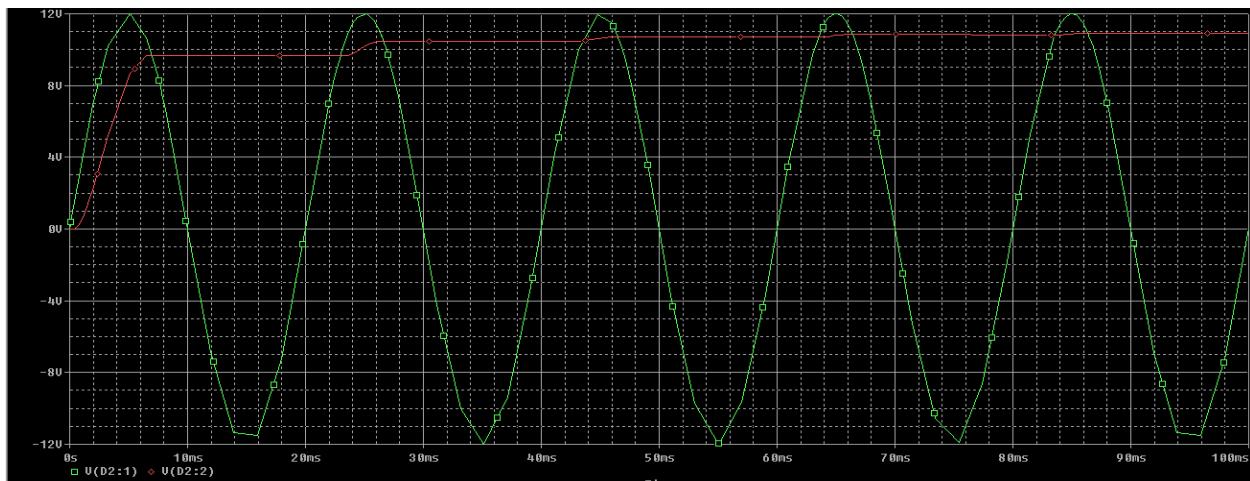


Fig 3.5 PSPICE simulation diagram of half wave rectifier with filter

3.10 Full wave rectifier

A device is capable of converting a sinusoidal input waveform into a unidirectional waveform with non zero average component is called a rectifier.

A practical half wave rectifier with a resistive load is shown in the circuit diagram. It consists of two half wave rectifiers connected to a common load. One rectifies during positive half cycle of the input and the other rectifying the negative half cycle. The transformer supplies the two

diodes (D1 and D2) with sinusoidal input voltages that are equal in magnitude but opposite in phase. During input positive half cycle, diode D1 is ON and diode D2 is OFF. During negative half cycle D1 is OFF and diode D2 is ON. Peak Inverse Voltage (PIV) is the maximum voltage that has to be withstand by a diode when it is reverse biased. Peak inverse voltage for Full Wave Rectifier is $2V_m$ because the entire secondary voltage appears across the non-conducting diode .

The output of the Full Wave Rectifier contains both ac and dc components. A majority of the applications, which cannot tolerate a high value ripple, necessitates further processing of the rectified output. The undesirable ac components i.e. the ripple, can be minimized using filters.

Ripple Factor:

Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol ' γ '.

$$\gamma = \frac{V_{ac}}{V_{dc}}, (\gamma = 0.48)$$

Efficiency:

The ratio of output DC power to input AC power is defined as efficiency.

$$\eta = \frac{(V_{dc})^2}{(V_{ac})^2}$$

$\eta = 81\%$ (if $R \gg R_f$, then R_f can be neglected).

The maximum efficiency of a Full Wave Rectifier is 81.2%.

3.11 Theoretical Calculations:

Without filter:

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$V_{ac} = \sqrt{(V_{rms}^2 - V_{dc}^2)}$$

$$V_{dc} = \frac{2V_m}{\pi}$$

$$\sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = 0.48$$

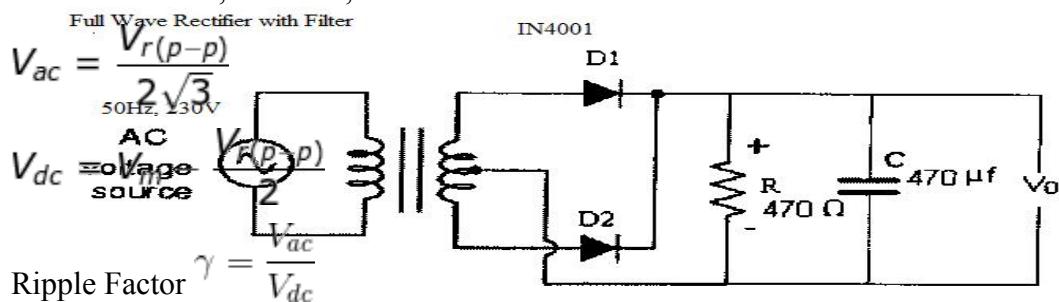
Ripple factor (Theoretical) =

Ripple Factor (Practical) $\gamma = \frac{V_{ac}}{V_{dc}}$

With filter:

Ripple factor (Theoretical) $\gamma = \frac{1}{4\sqrt{3}fCR}$

Where $f = 50\text{Hz}$, $R = 1\text{K}\Omega$, $C = 1000\mu\text{F}$.



Percentage Regulation = $\left(\frac{V_{NL} - V_{FL}}{V_{FL}} \right) * 100 \%$

V_{NL} = DC voltage at the load without connecting the load (Minimum current).

V_{FL} = DC voltage at the load with load connected.

Efficiency $\eta = \frac{P_{DC}}{P_{AC}} \% \text{u200B}$

$P_{AC} = V_{2\text{rms}} / R_L$

$P_{DC} = V_{dc} / R_L$

3.12 Circuit Diagram

Fig 3.6 Circuit diagram of full wave rectifier (Center tapped)

3.13 MODEL GRAPH

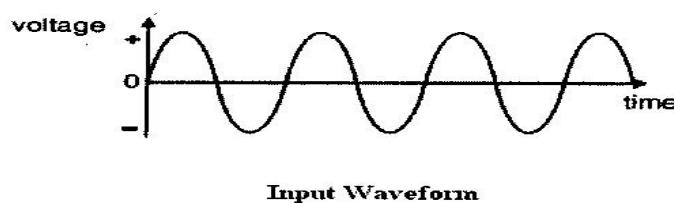


Fig 3.7 Model graph of full wave rectifier

3.14 Observations

	Input Waveform	Output Waveform (without filter)	Ripple Voltage (with filter)
Amplitude			
Time Period			
Frequency			

3.15 Pspice circuit diagram for Full Wave Rectifier(with filter)

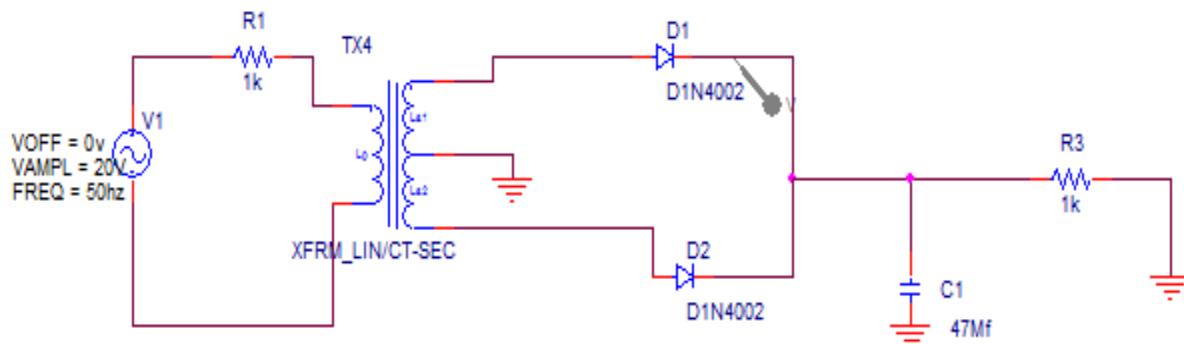


Fig 3.8 PSPICE schematic diagram of full wave rectifier with filter

3.16 Simulation graph for full wave rectifier (with filter)

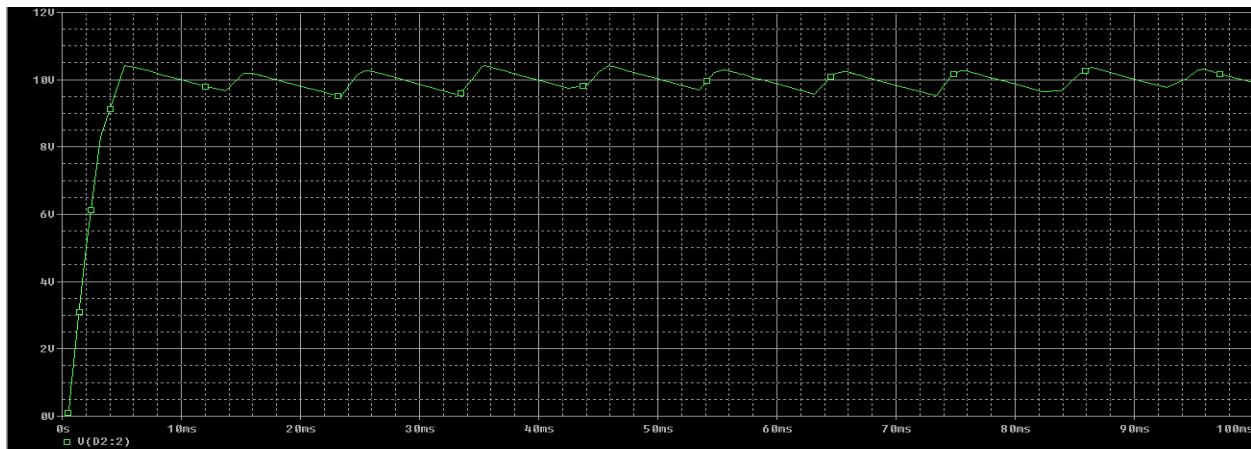


Fig 3.9 PSPICE simulation diagram of full wave rectifier with filter

3.17 Pspice circuit diagram for Full Wave Rectifier(without filter)

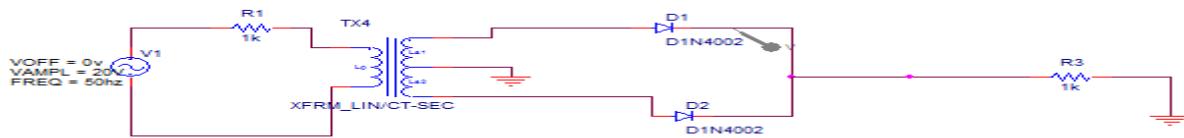


Fig 3.10 PSPICE schematic diagram of full wave rectifier without filter

3.18 Simulation graph for full wave rectifier (without filter)

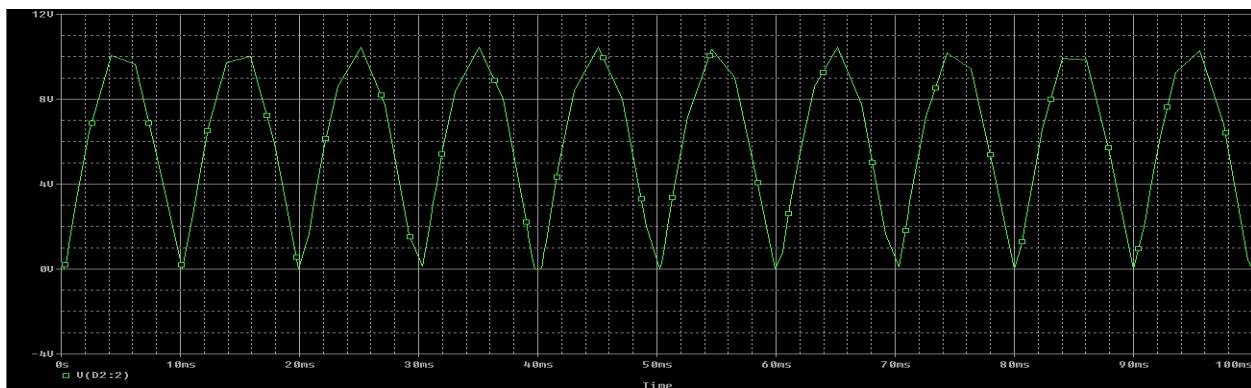


Fig 3.11 PSPICE simulation diagram of full wave rectifier without filter

3.19 Bridge rectifier

A device is capable of converting a sinusoidal input waveform into a unidirectional waveform with non zero average component is called a rectifier. The Bridge rectifier is a circuit, which converts an ac voltage to dc voltage using both half cycles of the input ac voltage. The Bridge rectifier has four diodes connected to form a Bridge. The load resistance is connected between the other two ends of the bridge.

For the positive half cycle of the input ac voltage, diode D1 and D3 conducts whereas diodes D2 and D4 remain in the OFF state. The conducting diodes will be in series with the load resistance RL and hence the load current flows through RL. For the negative half cycle of the input ac voltage, diode D2 and D4 conducts whereas diodes D1 and D3 remain in the OFF state.

The conducting diodes will be in series with the load resistance RL and hence the load current flows through RL in the same direction as in the previous half cycle. Thus a bidirectional wave is converted into a unidirectional wave. Ripple factor is a measure of effectiveness of a rectifier circuit and defined as a ratio of RMS value of ac component to the dc component in the rectifier output.

3.20 Theoretical calculations

Ripple Factor

The ripple factor for a Full Wave Rectifier is given by

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_d}\right)^2 - 1}$$

The average voltage or the DC voltage available across the load resistance is $V_{dc} = 2V_m/\pi$

The RMS value of the voltage at the load resistance is $V_{rms} = V_m / 2$

Ripple factor

$$\therefore \gamma = \sqrt{\left(\frac{V_m/2}{2V_m/\pi}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{8}\right)^2 - 1} = 0.482$$

The ripple factor can be lowered by increasing the value of the filter capacitor or increasing the load capacitance.

Efficiency

Efficiency, η is the ratio of dc output power to ac input power

$$\eta = \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}}$$

$$\frac{V_{dc}^2 / R_L}{V_{rms}^2 / R_L} = \frac{\left[2V_m/\pi\right]^2}{\left[V_m/\sqrt{2}\right]^2} = \frac{8}{\pi^2} = 0.812 = \underline{\underline{81.2\%}}$$

The maximum efficiency of a Full Wave Rectifier is 81.2%

3.21 Circuit Diagram

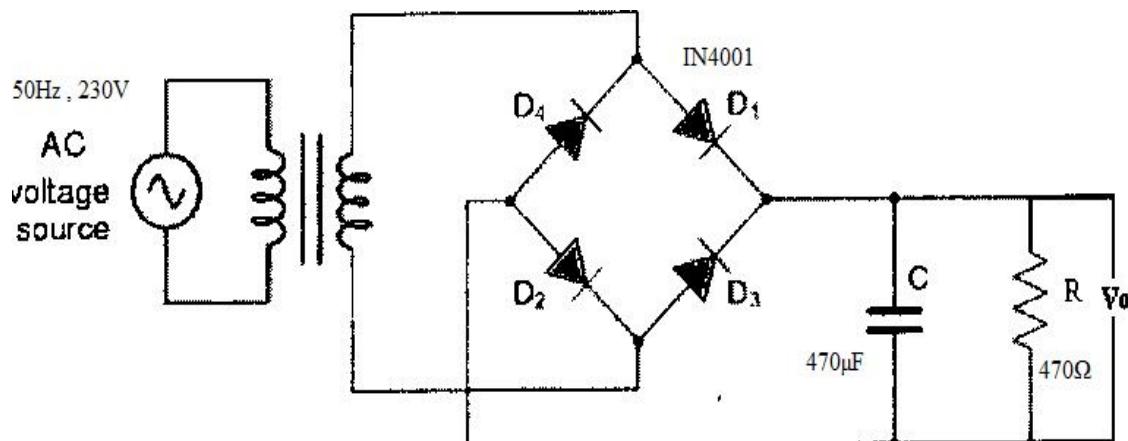


Fig 3.12 Circuit diagram of Full wave bridge rectifier

3.22 Model Graph

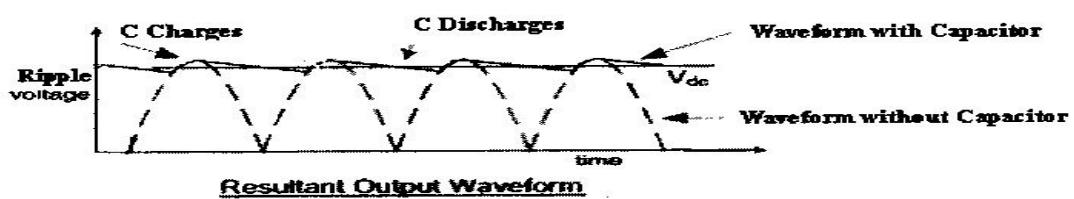
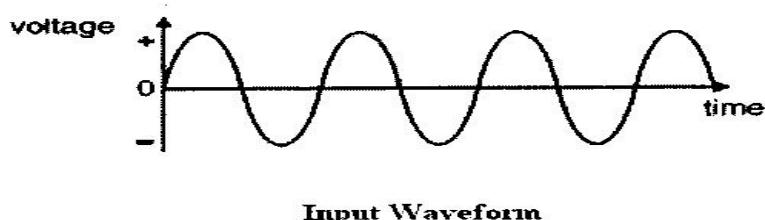


Fig 3.13 Model graph of Full wave bridge rectifier

3.23 Observations

	Input Waveform	Output Waveform (without filter)	Ripple Voltage (with filter)
Amplitude			
Time Period			
Frequency			

3.24 PSPICE circuit diagram for Full Wave Bridge Rectifier(without filter)

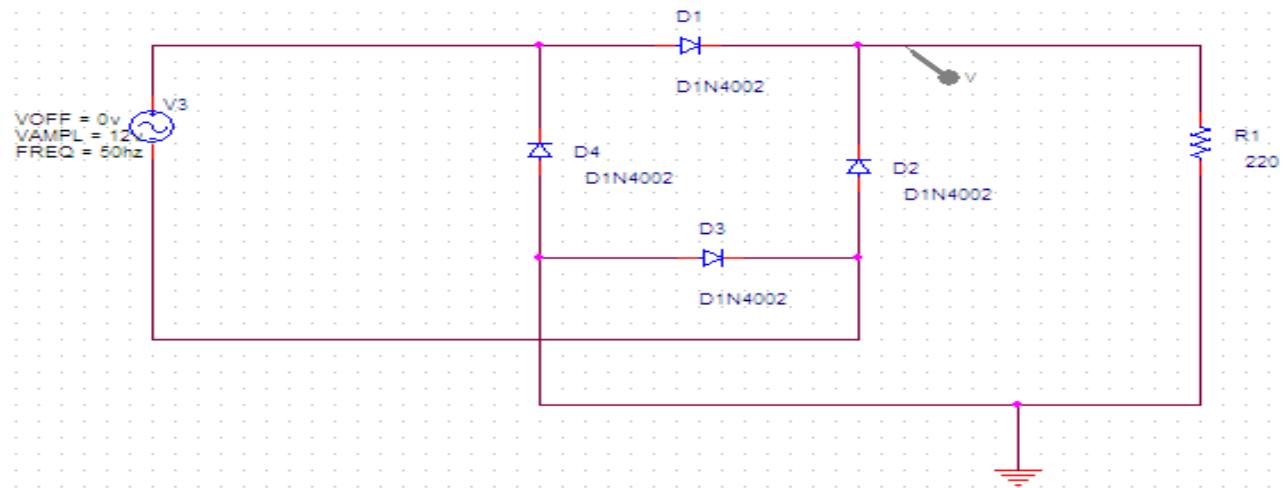


Fig 3.14 PSPICE schematic diagram of full wave bridge rectifier without filter

3.25 Simulation graph for full wave bridge rectifier(without filter)

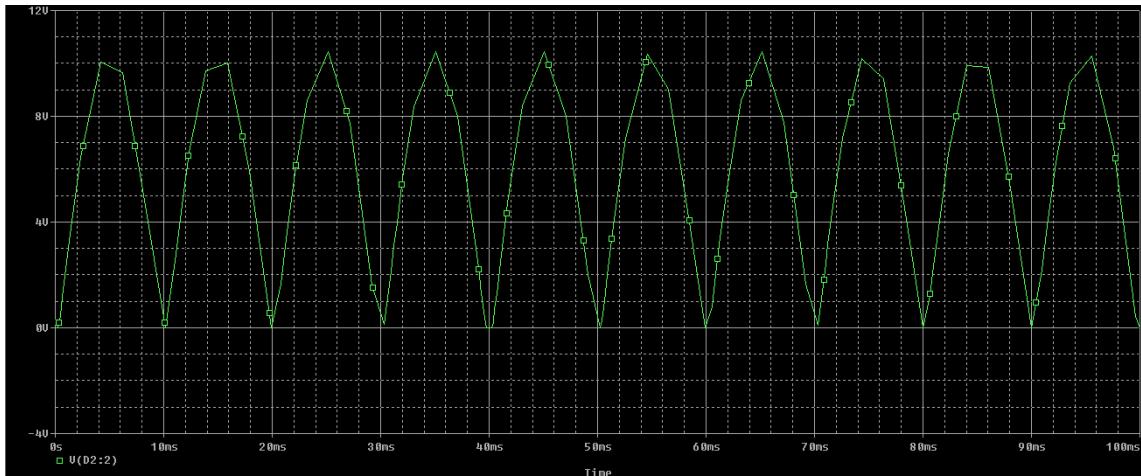


Fig 3.15 PSPICE simulation diagram of full wave bridge rectifier without filter

3.26 pspice circuit diagram for Full Wave Bridge Rectifier(with filter)

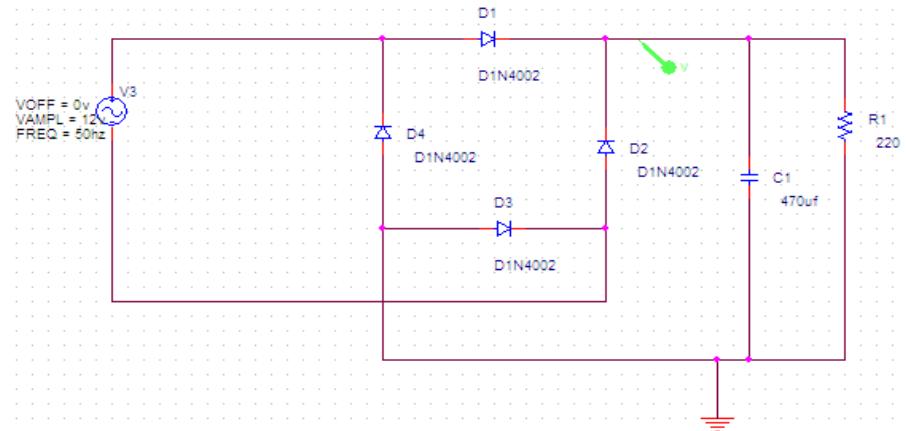


Fig 3.16 PSPICE schematic diagram of full wave bridge rectifier with filter

3.27 Simulation graph for full wave bridge rectifier(withfilter)

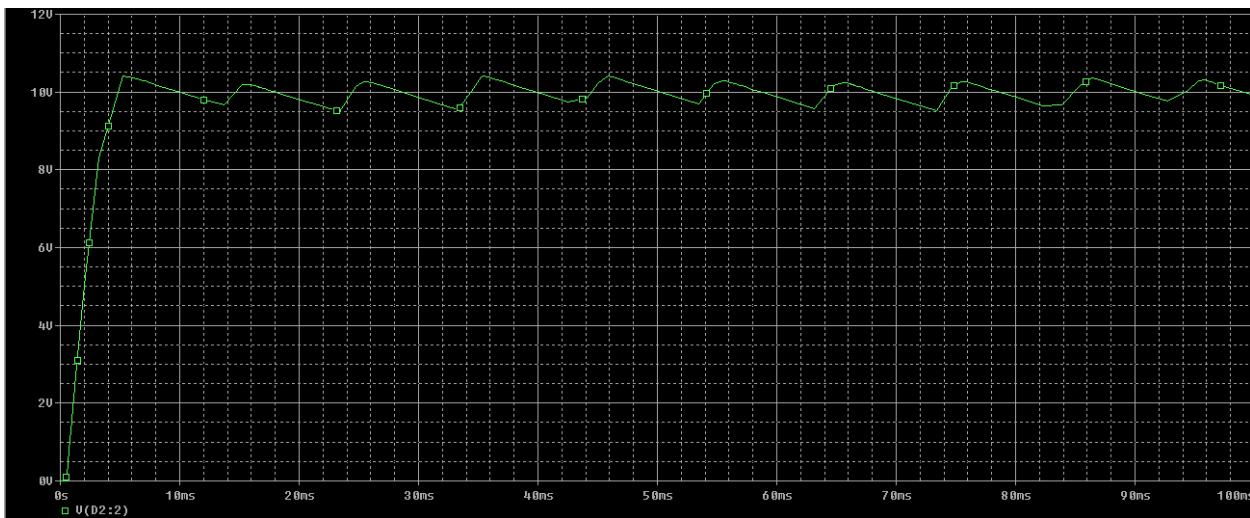


Fig 3.17 PSPICE simulation diagram of full wave bridge rectifier with filter

3.28 Result

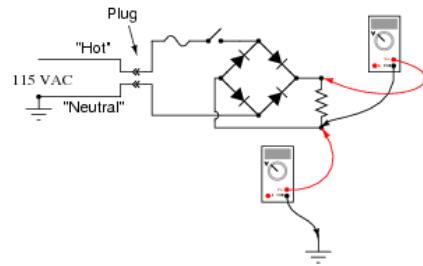
Thus the Rectifier Circuits are constructed and ripple factor, efficiency, $V_p(\text{rect})$, and V_{dc} values for circuits has been analyzed

3.29 Pre lab Questions:

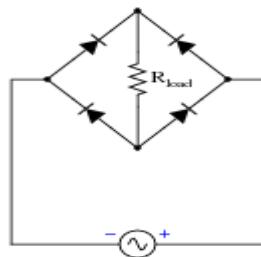
1. What is the PIV of rectifier circuits?
2. A bridge rectifier is preferable to a full-wave rectifier using center-tap transformer as
 - (a) It uses four diodes
 - (b) Its transformer does not require center-tap
 - (c) It requires much smaller transformer for the same output
 - (c) All of these
3. In a full-wave bridge rectifier, the current in each diode flows for
 - (a) Complete cycle of the input signal
 - (b) Half-cycle of the input signal
 - (c) Less than half-cycle of the input signal
 - (d) More than half-cycle of the input signal
4. What is the purpose of a filter in dc power supply?
5. What is TUF? Give the TUF of half wave, full wave-center tapped and bridge rectifier.

3.30 Post lab Questions:

1. When a 50Hz ac signal is fed to a rectifier, the ripple frequency of the output voltage waveform for full bridge rectifier is
 (a) 25 Hz (b) 50 Hz (c) 100 Hz (d) 150 Hz

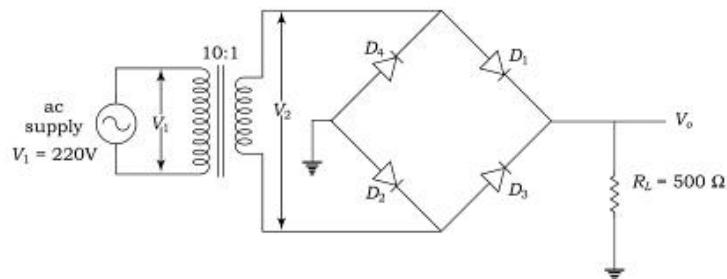


2. Trace the current through this rectifier circuit at a moment in time when the AC source's polarity is positive on right and negative on left as shown. Be sure to designate the convention you use for current direction (conventional or electron flow):



Also, mark the polarity of the voltage drop across R_{load} .

3. For the figure shown below. Determine (a) the DC output voltage, (b) DC load current, (c) the RMS value of the load current, (d) the DC power, (e) the AC power, (f) efficiency of rectifier, (g) peak inverse voltage of each diode, and (h) output frequency. Assume all diodes are ideal.



4. DIODE CLIPPING AND CLAMPING CIRCUITS

4.1 Objective

To study the use of diodes in wave-shaping (clipper) circuits and in level-shifting (clamper) circuits.

4.2 Hardware Required

S. No	Apparatus	Type	Range	Quantity
01	PN Junction Diode	IN4001		1
02	Resistance		1k ohm	1
03	Regulated power supply		(0 – 30V)	1
04	Bread board			1
	Connecting wires			Few

4.3 Introduction

Clippers

It is frequently necessary to modify the shape of various waveforms for use in instrumentation, controls, computation, and communications. Wave shaping is often achieved by relatively simple combinations of diodes, resistors, and voltage sources. Such circuits are called clippers, limiters, amplitude selectors, or slicers. Clipper circuits are primarily used to prevent a waveform from exceeding a particular limit, either positive or negative. For example, one may need to limit a power supply's output voltage so it does not exceed +5 V. The most widely used wave shaping circuit is the rectifier, which you have previously studied.

Figure 4.1 shows a **positive clipper circuit**. As indicated, the output voltage has the entire positive half-cycles clipped off. The circuit works as follows: During the positive half-cycle of the input voltage, the diode turns on. For an ideal diode, the output voltage is zero. For an actual diode the output voltage is equal to V_γ , the cut-in voltage of the diode.

During the negative half-cycle, the diode is reverse-biased and can be approximated by an open circuit. In many clippers, the load resistor, R_L , is much larger than the series resistor, R . In which case, essentially all of the negative half-cycle voltage appears at the output through voltage-divider action. If R_L and R are comparable, then on the negative half-cycle, the output voltage would be given by

$$V_o = V_{p1} = V_p \cdot (R_L / (R_L + R)).$$

Since the first V_γ volts are used to begin conduction in the diode, the output signal is clipped near V_γ , rather than at 0V. If the diode polarity is reversed, the result is a negative clipper that removes the negative half cycle. In this case, the clipping levels occur near $-V_\gamma$.

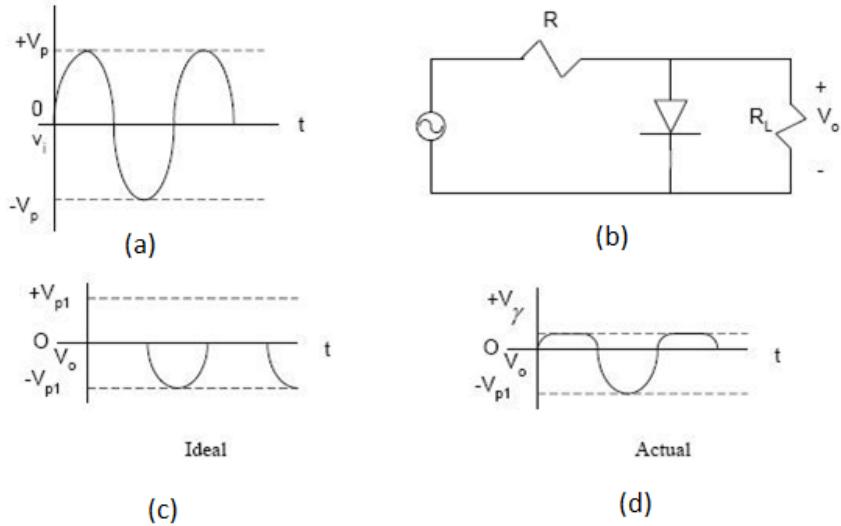


Fig 4.1 A positive clipper circuit: (a) Sinusoidal input to clipper circuit;(b) A positive clipper circuit; (c) Output of ideal positive clipper circuit; and (d) Output of actual positive clipper circuit

If a constant voltage source is placed in series with the diode shown in Figure 4.1(b), the result is a **biased positive clipper**, as shown in Figure 4.2(b). When the input voltage is greater than $V+V_\gamma$, the diode is forward biased and the output voltage is held at $(V+V_\gamma)$ volts (assuming $R_L \gg R$). When the input voltage is less than $V+V_\gamma$, the diode becomes an open circuit and the circuit acts as a voltage divider. R_L is usually much greater than R , in which case, essentially all of the input voltage appears at the output. If both the diode and battery polarities are reversed, a biased negative clipper results, with the output clipped near $-(V+V_\gamma)$ volts.

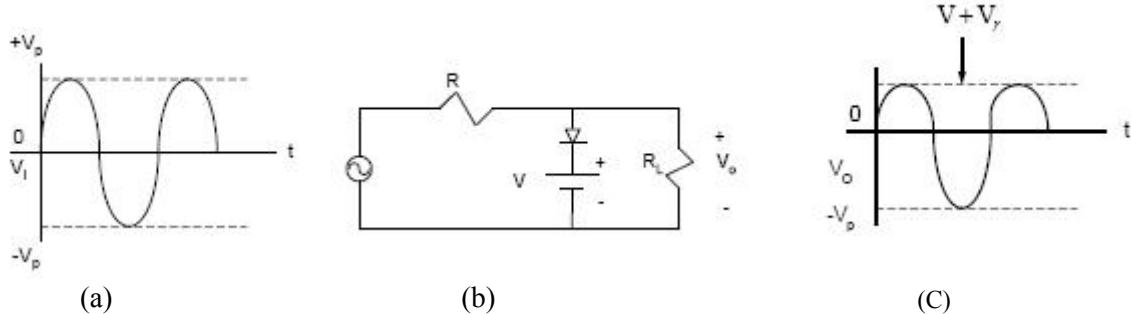


Fig 4.2 Biased positive clipper circuit: (a) Input to clipped circuit; (b) Biased positive clipper circuit; and (c) Output of positive clipper circuit

Clampers

In certain instances, it may be desirable to keep the output waveform essentially unchanged, but modify its dc level to some required value. This can be done by the use of diodes, resistors, capacitors, and voltage sources. Such circuits are known as clampers. For example, if the input voltage signal swings from $-10V$ to $+10V$, a positive dc clumper can produce an output that keeps the signal wave shape intact but swings the voltage from $0V$ to $+20V$. TV receivers use a dc clumper to add a dc voltage to the video signal. Here the dc clumper is usually called a dc restorer.

In Figure 4.3(b) a positive dc clumper is shown. The clumper operates as follows: During the negative half-cycle of the input voltage, the diode turns on as illustrated in Figure 4.4(a). At the negative peak, the capacitor charges up to V_p with the polarity shown and the output voltage is zero. As the voltage grows beyond the negative peak, the diode shuts off as shown in Figure 4.4(b).

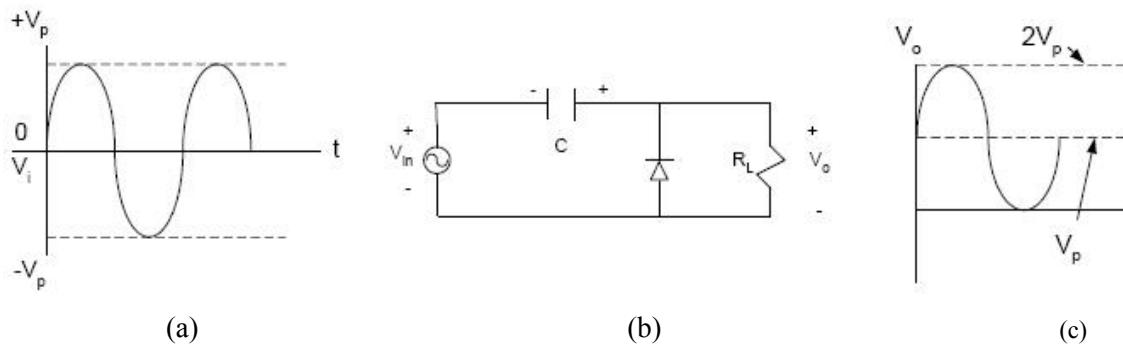
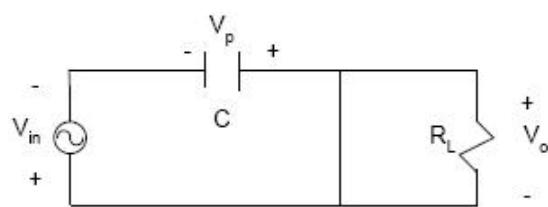


Fig 4.3 Positive dc clumper: (a) Sinusoidal input to positive dc clumper; (b) Positive dc clumper; and (c) Clamped sinusoidal output

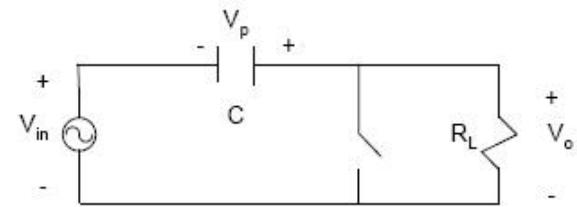
The capacitor retains the voltage for a short time. The $R_L C$ time constant is deliberately made much larger than the period, T , of the input signal. Hence, the capacitor remains almost fully charged during the entire off time of the diode. The capacitor thus acts like a battery of V_p volts and now only passes the ac signal, which rides on top of V_p . The output voltage signal, therefore, consists of the input signal riding on a dc voltage of $+V_p$ volts.

Since the diode drops V_γ volts when conducting, the capacitor voltage does not quite reach $+V_p$ volts. For this reason, the dc clamping is not perfect, and the negative peaks are at $-V_\gamma$ as shown in Figure 4.4(e).

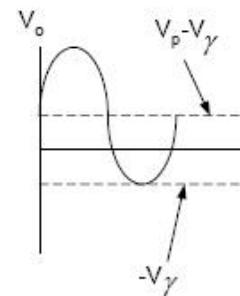
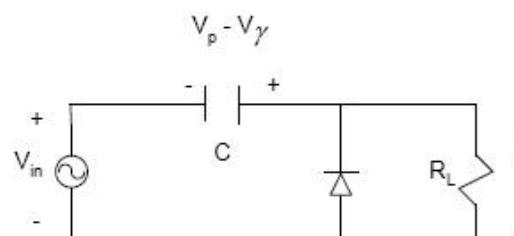
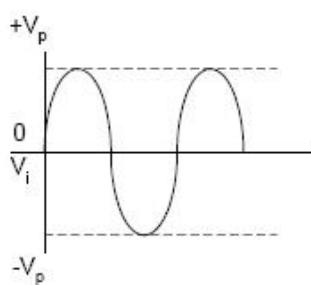
When the polarity of the diode in Figure 4.3(b) is reversed, the polarity of the capacitor voltage reverses also, and the circuit becomes a negative dc clamper. Ideally, the output voltage consists of the input voltage riding on a dc voltage of $-V_p$ volts. If the diode is considered non-ideal, then the output will consist of the input signal riding on a dc voltage of $-(V_p - V_\gamma)$ volts, and the positive peaks will occur at V_γ volts.



(a)



(b)



(c)

(d)

(e)

Fig4.4 Positive clamping circuit operation

From the above discussions, it can be seen that when the diode points upward, a positive dc clamper results. When the diode points downward, the circuit is a negative dc clamer. The clamping value can be modified by putting a voltage source V_B in series with the diode, shifting the peak voltage to $(\pm V_\gamma \pm V_B)$, depending on the sign of V_B and the polarity of the diode.

4.4. EXPERIMENT

4.4.1 IDEAL CLIPPING CIRCUITS

NOTE: Set $V_{in} = 8V_P$ at 1kHz with 0V DC offset and $R = 1k\Omega$ for all circuits.

1. Clipping Circuit 1

- a. Connect the circuit shown in Figure 4.5(a) using the SUPPLY+ power supply as V_B . Set the SUPPLY+ voltage to 0V using the Variable Power Supply.
- b. Measure V_{in} and V_o using the oscilloscope. Make an accurate sketch of the input and output waveforms on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the input voltage at which clipping occurs.
- c. Set V_B (SUPPLY+) = 2V and repeat step b.

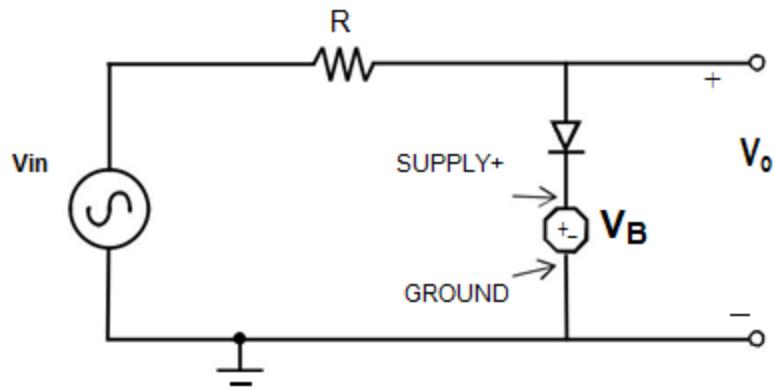


Fig 4.5(a) Clipping Circuit 1

2. Clipping Circuit 2

- Connect the circuit shown in Figure 4.5(b) using the SUPPLY+ power supply as V_B . Set the SUPPLY+ voltage to 0V.
- Measure V_{in} and V_o using the oscilloscope. Make an accurate sketch of the input and output waveforms on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the input voltage at which clipping occurs.
- Set V_B (SUPPLY+) = 2V and repeat step b.

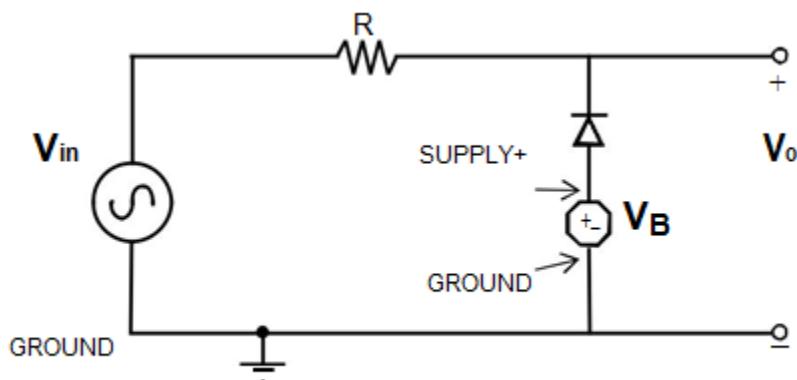


Fig 4.5(b) Clipping Circuit 2

3. Clipping Circuit 3

- a. Connect the circuit shown in Figure 4.5(c) using the SUPPLY– power supply as $-V_B$. Set the SUPPLY– voltage to 0V.
- b. Measure V_{in} and V_o using the oscilloscope. Make an accurate sketch of the input and output waveforms on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the input voltage at which clipping occurs.
- c. Set $V_B = 2V$ (SUPPLY– = -2V) and repeat step b.

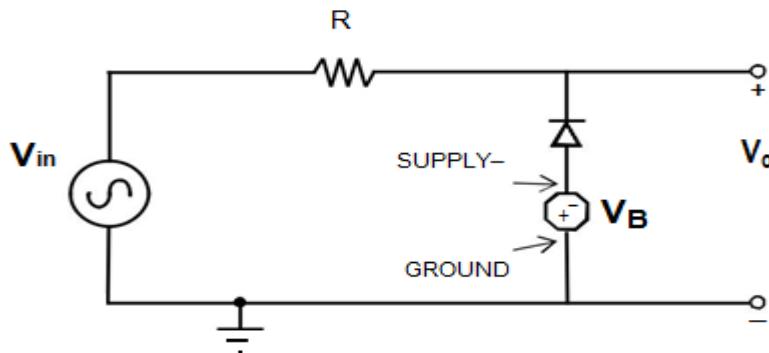


Fig 4.5(c) Clipping Circuit 3

4. Clipping Circuit 4

- a. Connect the circuit shown in Figure 4.5(d) using the SUPPLY– power supply as $-V_B$. Set the SUPPLY– voltage to 0V.
- b. Measure V_{in} and V_o using the oscilloscope. Make an accurate sketch of the input and output waveforms on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the input voltage at which clipping occurs.
- c. Set $V_B = 2V$ (SUPPLY– = -2V) and repeat step b.

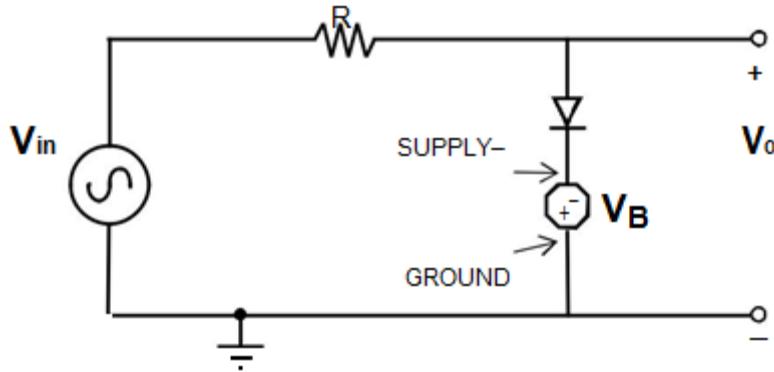


Fig 4.5(d) Clipping Circuit 4

4.4.2 SERIES-BIASED CLIPPING CIRCUITS

NOTE: The Function Generator (FGEN) in the following circuits will provide both the V_{SIN} and V_B voltages. DO NOT USE SUPPLY+ OR SUPPLY- IN THE CIRCUITS.

$R = 1\text{k}\Omega$ for all circuits.

1. Series-Biased Clipping Circuit 1

- Connect the circuit shown in Figure 4.6(a) using the function generator to supply both V_{SIN} and V_B . Set the AMPLITUDE voltage to $8V_p$. Set the frequency to 1kHz. **Set the DC offset to 0V**.
- Measure V_{SIN} and V_o using the oscilloscope using SCOPE CH0 and CH1, respectively. **Set the coupling on CH0 and CH1 to DC**. Click “Autoscale”. Make an accurate sketch of V_{SIN} and V_o on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the value of V_{SIN} at which clipping occurs. Use the cursors as needed.
- Set the DC offset of the function generator to 2V (**which is same as $V_B=2V$**) and repeat step b.

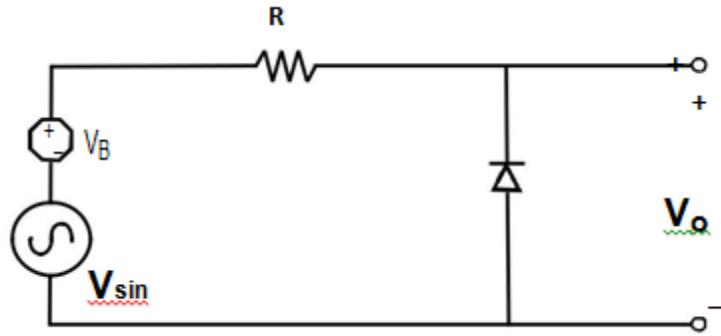


Fig4.6(a) Series-Biased Clipping Circuit 1

2. Series-Biased Clipping Circuit 2

- Connect the circuit shown in Figure 4.6(b) using the function generator to supply both V_{sin} and V_B . Set the AMPLITUDE voltage to $8V_p$. Set the frequency to 1kHz. Set the DC offset to 0V.
- Measure V_{sin} and V_o using the oscilloscope using SCOPE CH0 and CH1, respectively. Set the coupling on CH0 and CH1 to DC. Click “Autoscale”. Make an accurate sketch of V_{sin} and V_o on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the value of V_{sin} at which clipping occurs. Use the cursors as needed.
- Set the DC offset of the function generator to -2V ($V_B=2V$) and repeat step b.

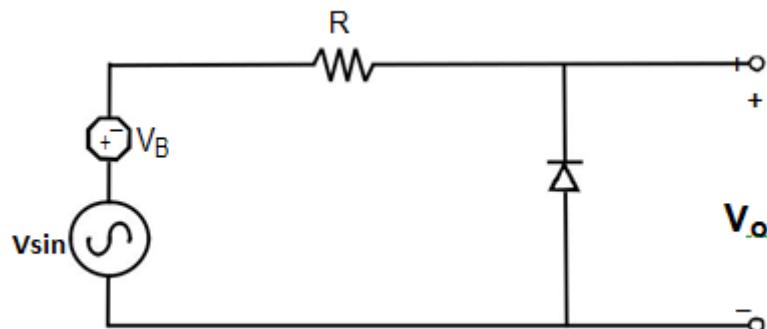


Fig 4.6(b) Series-Biased Clipping Circuit 2

3. Series-Biased Clipping Circuit 3

- a. Connect the circuit shown in Figure 4.6(c) using the function generator to supply both V_{SIN} and V_B . Set the AMPLITUDE voltage to $8V_P$. Set the frequency to 1kHz. Set the DC offset to 0V.
- b. Measure V_{SIN} and V_o using the oscilloscope using SCOPE CH0 and CH1, respectively. Set the coupling on CH0 and CH1 to DC. Click “Autoscale”. Make an accurate sketch of V_{SIN} and V_o on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the value of V_{SIN} at which clipping occurs. Use the cursors as needed.
- c. Set the DC offset of the function generator to 2V ($V_B=2V$) and repeat step b.

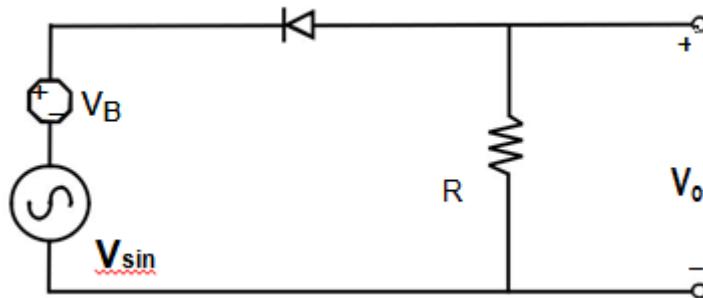


Fig 4.6(c) Series-Biased Clipping Circuit 3

4.4.3 CLAMPERS

Build the circuit shown in Figure 4.8 and make an accurate sketch of the input and output waveforms for a $8V_P$ sine wave input voltage for each of the following conditions. **Each condition should be relative to the circuit as shown in Figure 4.7.** Be sure to record the peakvalues of both waveforms on your sketch. A capacitor larger than $22 \mu\text{F}$ will work in this circuit.

1. Circuit as shown with V_{DC} (or SUPPLY+) = 2 volt.
2. Reverse polarity of diode and of capacitor.

3. Diode as shown with the battery reversed. (**Replace SUPPLY+ with SUPPLY-**)
4. Reverse polarity of diode, of capacitor, and of battery. (**Replace SUPPLY+ with SUPPLY-**)
5. Continuously vary SUPPLY+/SUPPLY- to see how the waveform is shifted in each case.

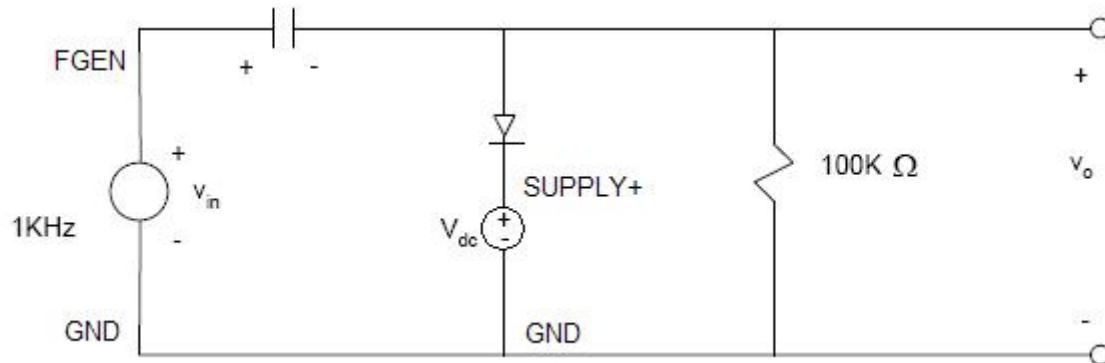


Fig 4.7 Clamping circuit

4.5 Precautions

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage of the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

4.6 Procedure

1. Ideal Clipping Circuits — Build 4 circuits (Figures 4.5 a-d)
 - a. $V_{in} = 8V_p$, $1kHz$, $V_B = 0 \& 2V$.
 - b. Sketch the input and output waveforms.
 - c. Record the voltage at which clipping occurs.

2. Series-Biased Clippers — Build 4 circuits (Figures 4.6 a-c)

- a. $V_{\text{sin}} = 8V_P$, 1 kHz, $V_B = 0$ & $2V$.
 - b. Sketch the input and output waveforms.
 - c. Record the voltage at which clipping occurs.
3. Clamper — Build circuit (Figure 4.7)

- a. $V_{\text{in}} = 8V_P$, 1 kHz, $V_{\text{dc}} = 2V$.
- b. Sketch the input and output waveforms.

4.7 Tabular column

	Amplitude	Time period	Frequency	Clipped Value:
Input Waveform				
Output Waveform				

4.8 IDEAL CLIPPING CIRCUITS

Clipping circuit 1

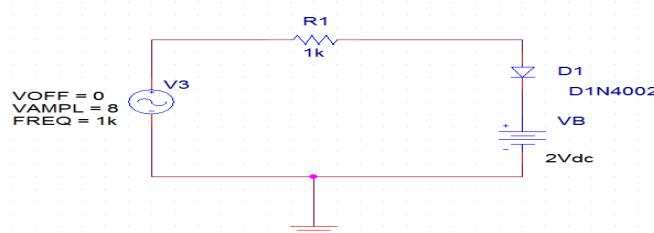


Fig 4.8 Circuit Diagram of Clipping Circuit 1

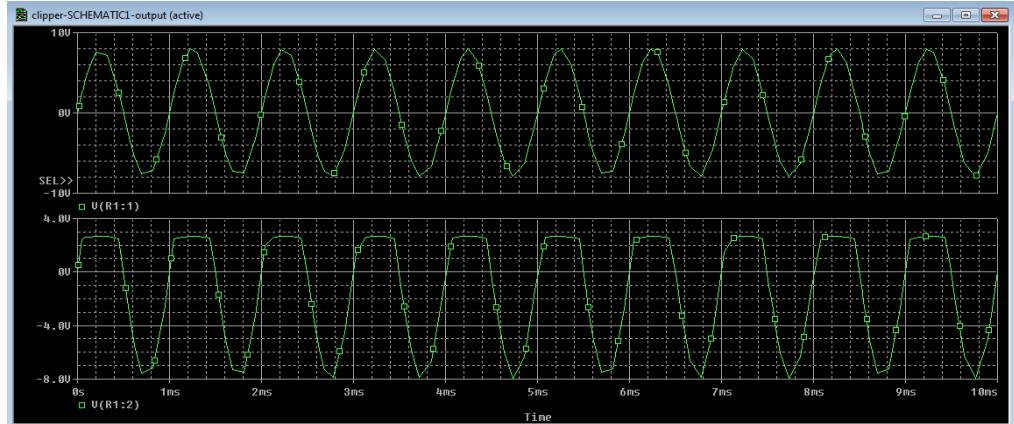


Fig 4.9 Input and Output waveform of Clipping Circuit 1

Clipping Circuit 2

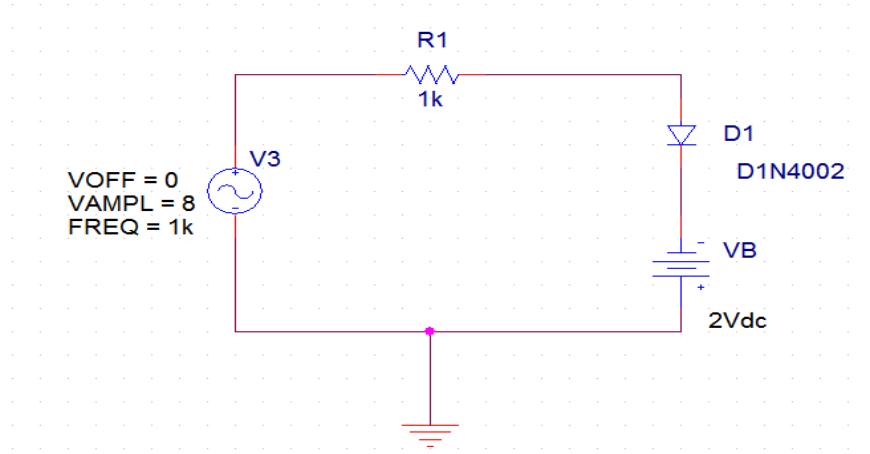


Fig 4.10 Circuit Diagram of Clipping Circuit 2

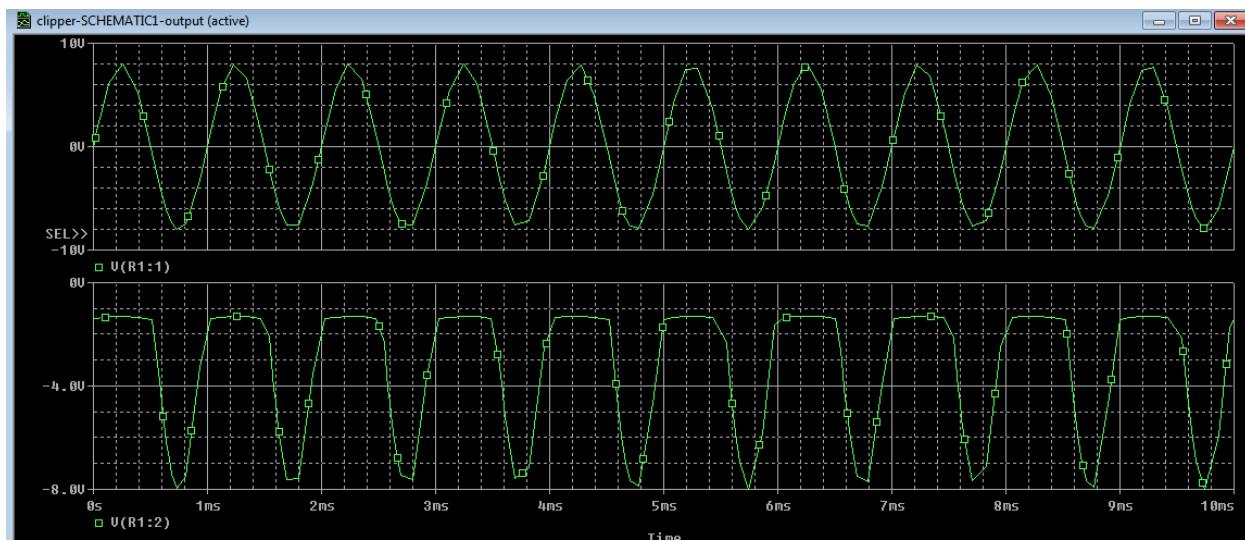


Fig 4.11 Input and Output waveform of Clipping Circuit 2
Clipping Circuit 3

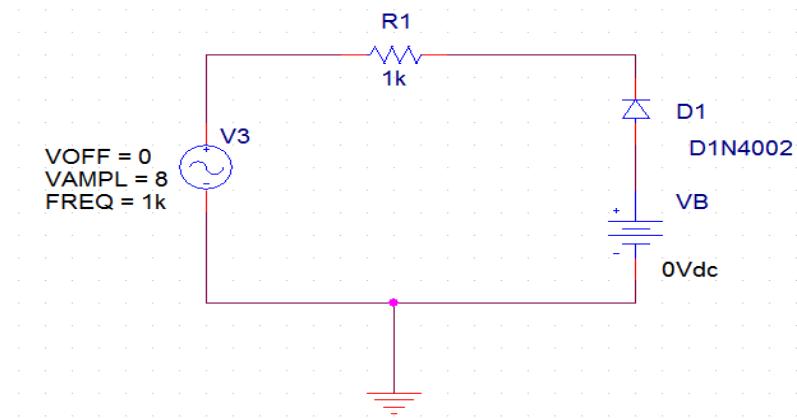


Fig 4.12 Circuit Diagram of Clipping Circuit 3

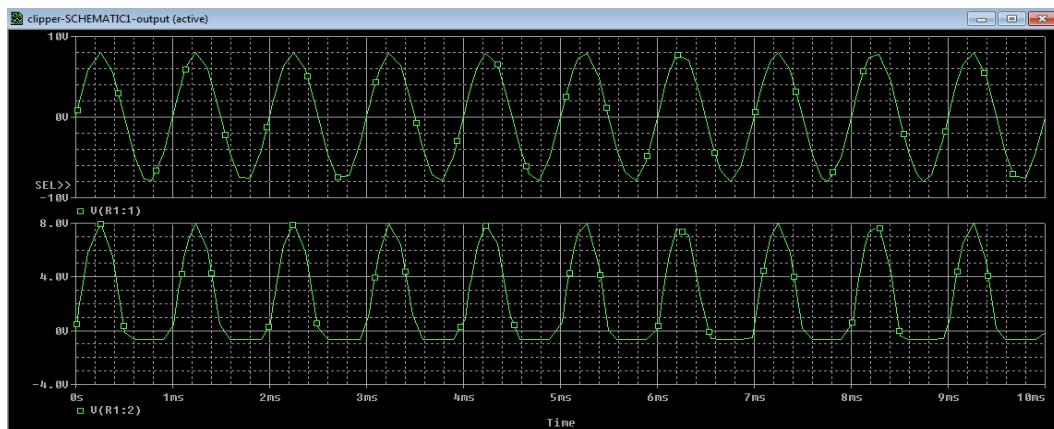


Fig 4.13 Input and Output waveform of Clipping Circuit 3

Clipping Circuit 4

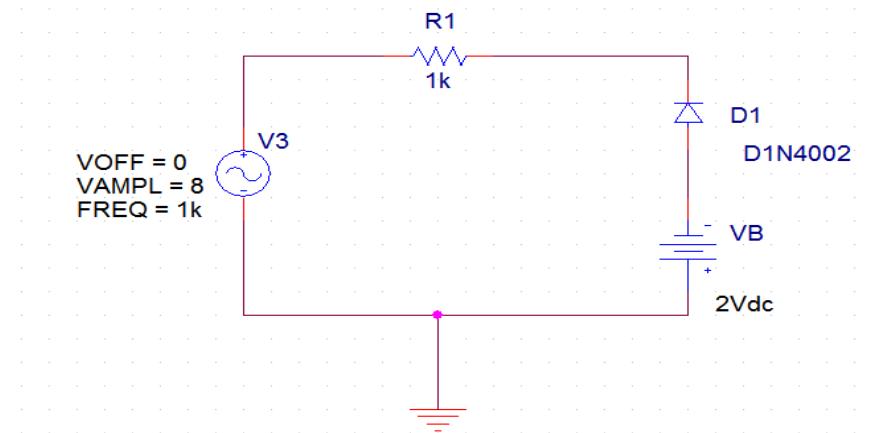


Fig 4.14 Circuit Diagram of Clipping Circuit 4

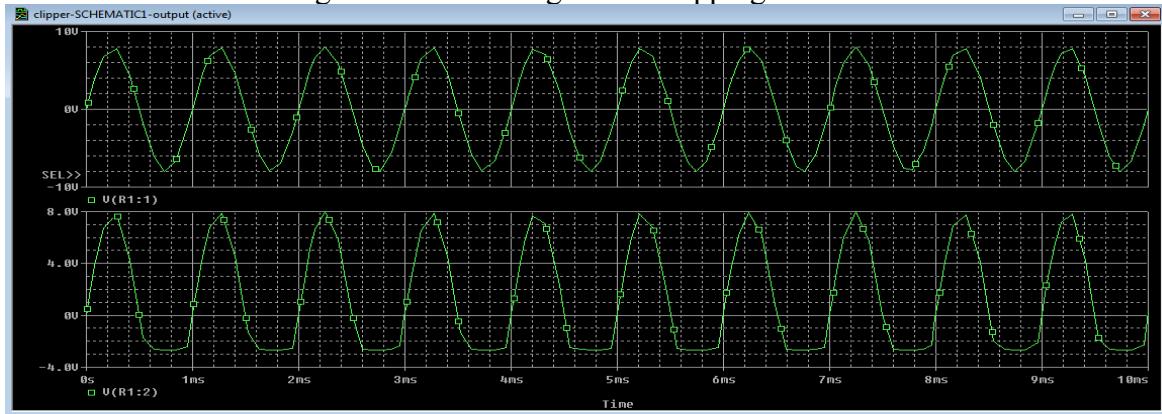


Fig 4.15 Input and Output waveform of Clipping Circuit 4

SERIES-BIASED CLIPPING CIRCUITS

Series Biased Clipping Circuit 1

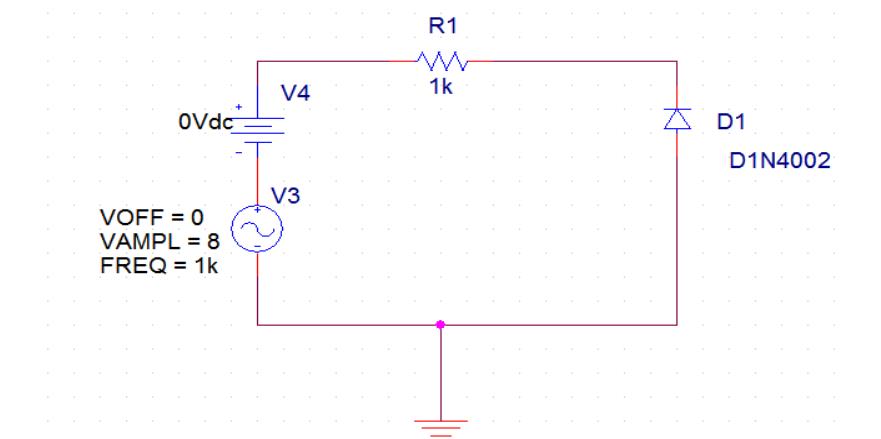


Fig 4.16 Circuit Diagram of Series Biased Clipping Circuit 1

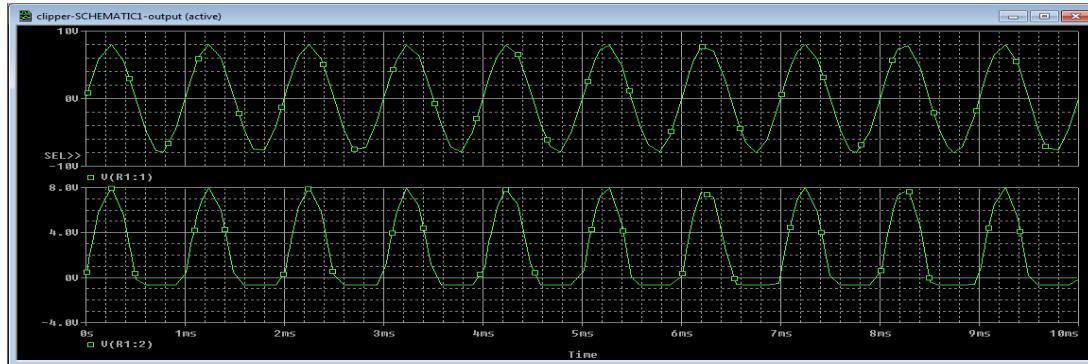


Fig 4.17 Input and output waveform of Series Biased Clipping Circuit 1

Series Biased Clipping Circuit 2

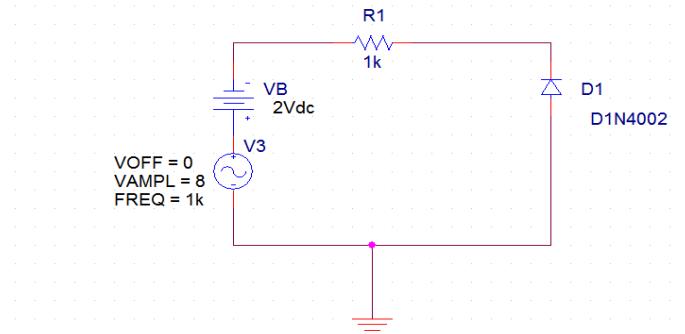


Fig 4.18 Circuit Diagram of Series Biased Clipping Circuit 2

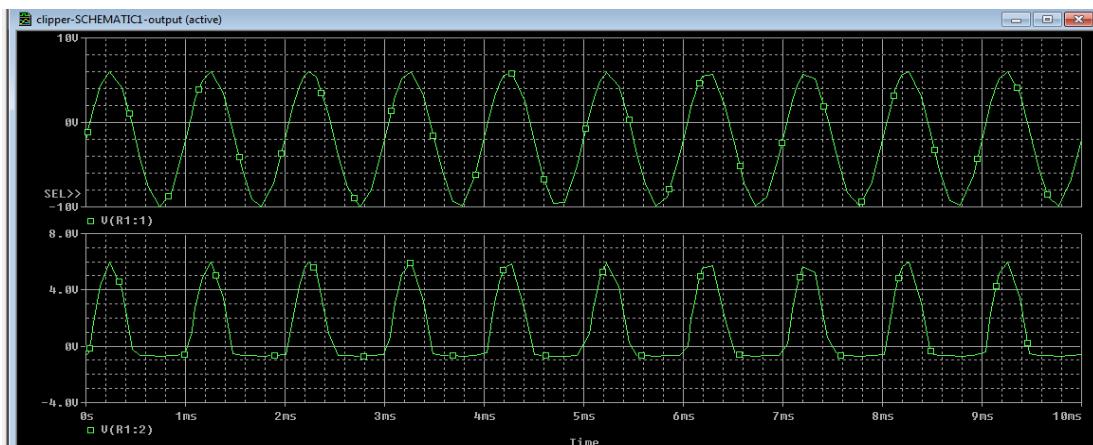


Fig 4.19 Input and output waveform of Series Biased Clipping Circuit 2

Series Biased Clipping Circuit 3

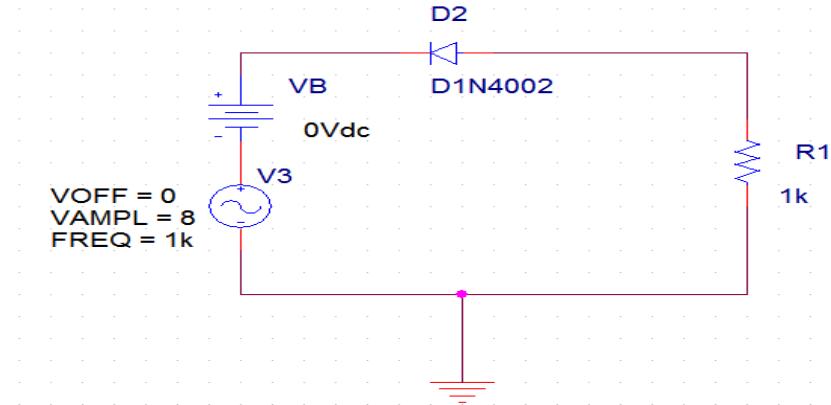


Fig 4.20 Circuit Diagram of Series Biased Clipping Circuit 3

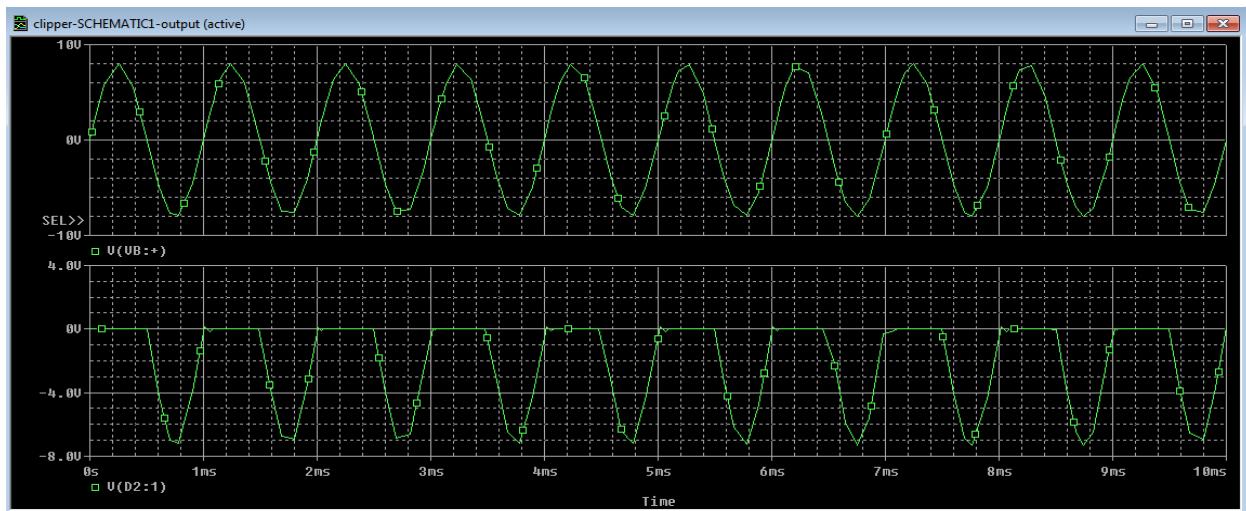


Fig 4.21 Input and output waveform of Series Biased Clipping Circuit 3

CLAMPER

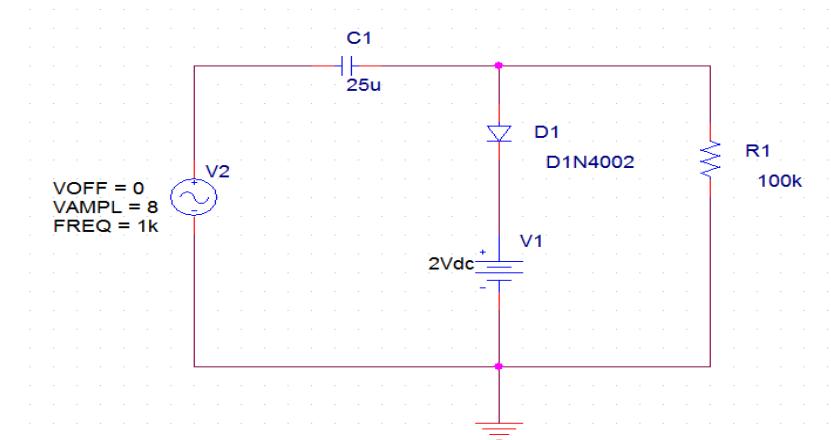


Fig 4.22 Circuit Diagram of Clamper Circuit

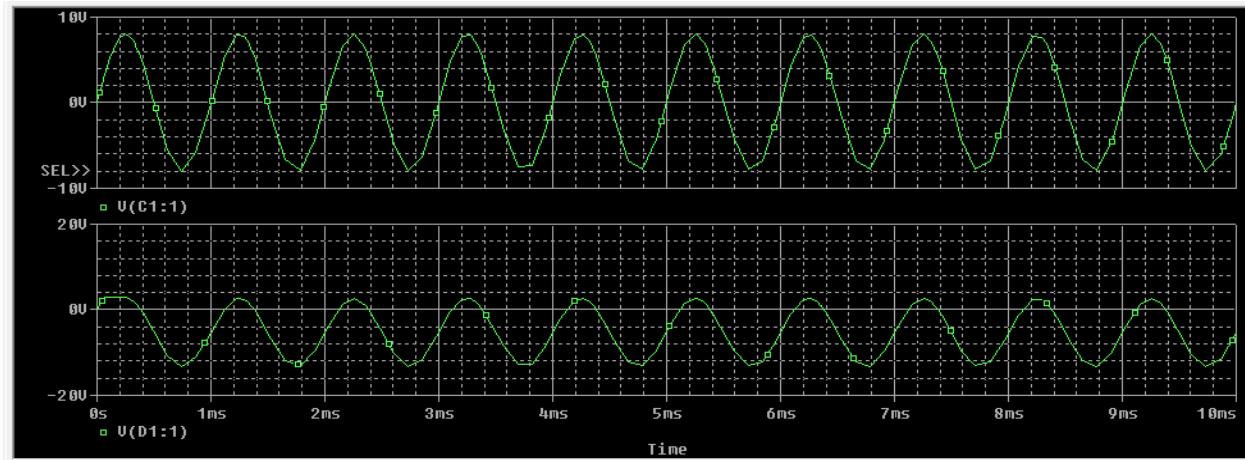


Fig 4.23 Input and output waveform of Clamper Circuit

4.9 Result

Various clipper and clamper circuits are constructed and the input and output waveforms are plotted.

4.10 Prelab Questions

1. What are the different types of clippers?
2. What are the applications of clippers?
3. Design a clipper circuit which limits the output signal to +1V and -1.5V.
4. What are the other names of Clamper?

4.11 Post lab Questions

1. If the diode in the figure 4.6(c) is reversed. What would be the output?
2. If the voltage VB in the figure 4.6(c) is reversed. What would be the output?
3. What is parallel biased clipper?
4. Draw the clipper circuit which clips the waveforms at two different levels.

5. BJT CHARACTERISTICS

5.1 Objective

To study the input and output characteristics of a bipolar junction transistor in Common Emitter configuration and to measure h-parameters

5.2 Hardware Required

S. No	Apparatus	Type	Range	Quantity
01	Transistor	BC147		1
02	Resistance		1k ohm, 10% tolerance, 1/2 watt rating	2
03	Regulated power supply		(0 – 30V), 2A Rating	2
04	Ammeter	MC	(1-30)mA, (0-500) μ A	1
05	Voltmeter	MC	(0 – 1)V, (0 – 30)V	1
06	Bread board			1
	Connecting wires			Few

5.3 Introduction

Bipolar junction transistor (BJT) is a 3 terminal (emitter, base, collector) semiconductor device. There are two types of transistors namely NPN and PNP. It consists of two P-N junctions namely emitter junction and collector junction.

In Common Emitter configuration the input is applied between base and emitter and the output is taken from collector and emitter. Here emitter is common to both input and output and hence the name common emitter configuration.

Input characteristics are obtained between the input current and input voltage taking output voltage as parameter. It is plotted between V_{BE} and I_B at constant V_{CE} in CE configuration.

Output characteristics are obtained between the output voltage and output current taking input current as parameter. It is plotted between V_{CE} and I_C at constant I_B in CE configuration.

5.4 Pin Assignment

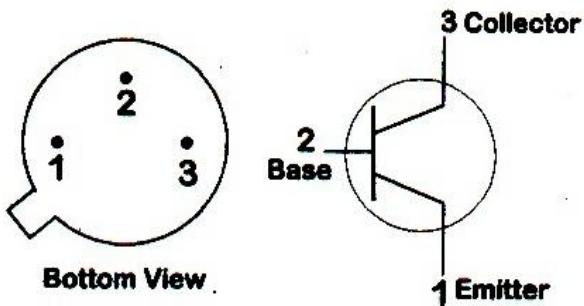


Fig 5.1. BJT Pin

Diagram

5.5 Circuit Diagram

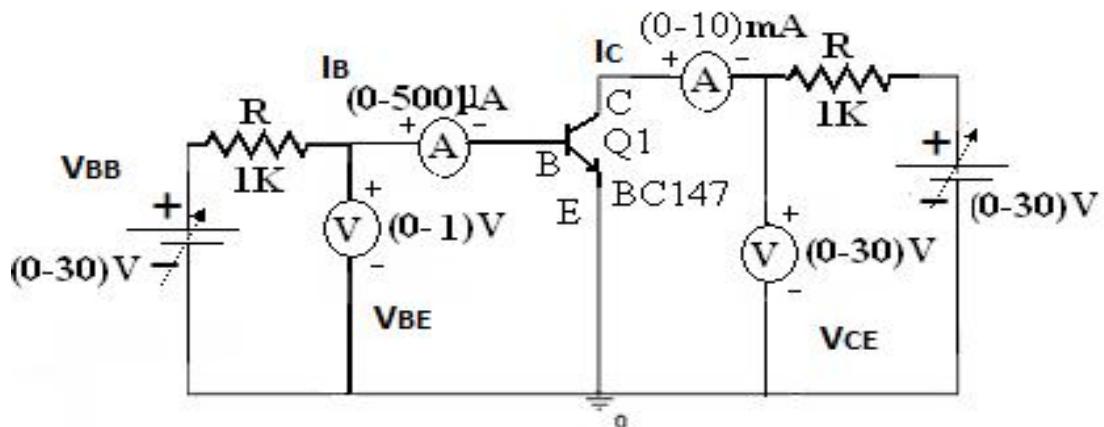


Fig 5.2. Circuit Diagram

5.6 Model Graph

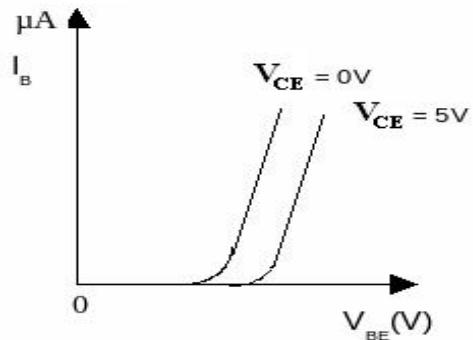


Fig 5.3. Input characteristics

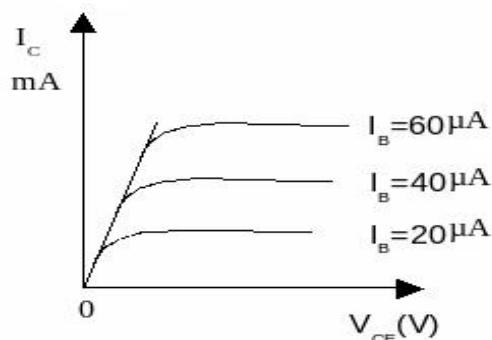


Fig 5.4. Output characteristics

5.7 PSPICE Simulation for Common Emitter Transistor

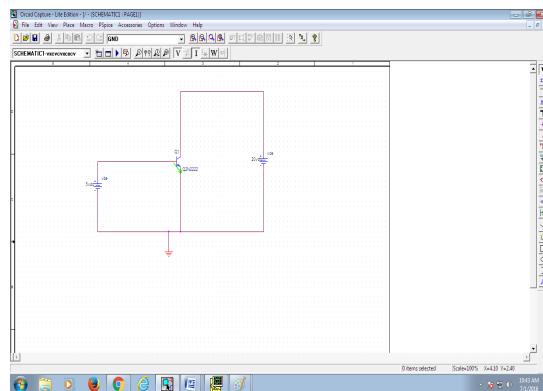


Fig 5.5. PSPICE Simulation

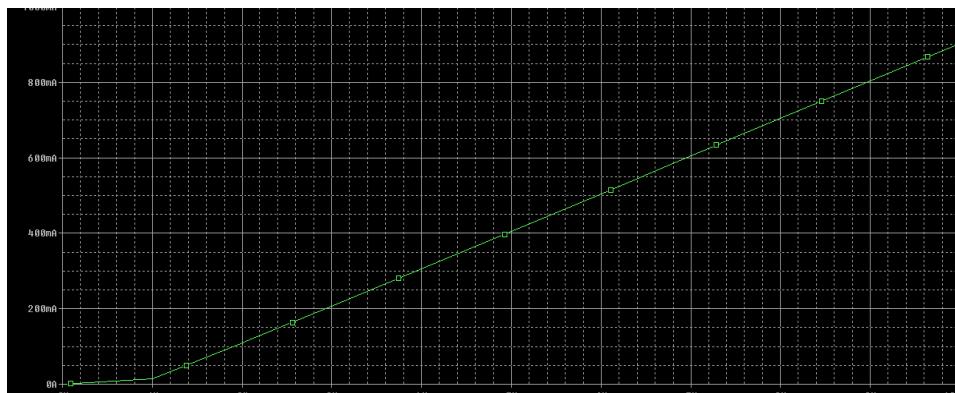


Fig 5.6 Input Characteristics

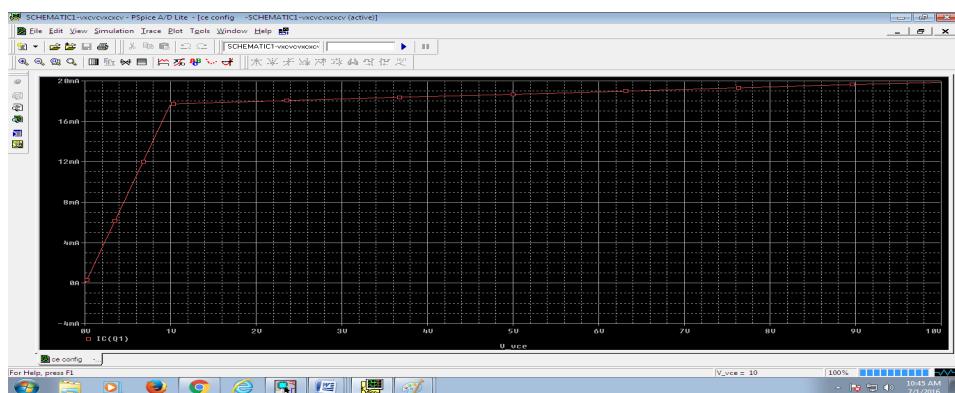


Fig 5.7 Output Characteristics

5.8 Precautions

1. While doing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

5.9 Procedure

5.9.1 Input Characteristics

1. Connect the transistor in CE configuration as per circuit diagram
2. Keep output voltage $V_{CE} = 0V$ by varying V_{CC} .
3. Varying V_{BB} gradually, note down both base current I_B and base - emitter voltage (V_{BE}).
4. Repeat above procedure (step 3) for various values of V_{CE}

5.9.2 Output Characteristics

1. Make the connections as per circuit diagram.
2. By varying V_{BB} keep the base current $I_B = 20\mu A$.
3. Varying V_{CC} gradually, note down the readings of collector-current (I_C) and collector-emitter voltage (V_{CE}).
4. Repeat above procedure (step 3) for different values of I_E

5.10 Tabular Column

5.10.1 Input Characteristics

$V_{CE} = 0 \text{ V}$		$V_{CE} = 4\text{V}$	
V_{BE} (volts)	I_B (mA)	V_{BE} (volts)	I_B (mA)

5.10.2 Output Characteristics

$I_B = 30 \mu\text{A}$		$I_B = 60 \mu\text{A}$	
V_{CE} (volts)	I_C (mA)	V_{CE} (volts)	I_C (mA)

5.11 Result

Thus the input and output characteristics of BJT in CE configuration was verified and the graph was plotted.

- a) Impedance (h_{ie}) = $\Delta V_{BE} / \Delta I_B$, V_{CE} constant. =
- b) Output admittance (h_{oe}) = $\Delta I_C / \Delta V_{EC}$, I_B constant=

5.12 Prelab Questions

- 1. Why is base width small?
- 2. Why is Silicon transistor more commonly used compared to Germanium transistor?
- 3. What is base width modulation?
- 4. The junction capacitance across collector to base junction is much lower than that across base to emitter junction. Why?
- 5. What is the difference between diffusion capacitance and transition capacitance?
- 6. What is the voltage across the collector to emitter terminal when the transistor is in (i) saturation (ii) cut-off (iii) active region?

5.13 Post lab Questions

- 1. From the above observation find forward current gain and reverse voltage gain.
- 2. Explain the switching action of a transistor?
- 3. At what region of the output characteristics, a transistor can act as an amplifier?
- 4. Design an NPN common emitter transistor to work as a current source. It is in which region of the transistor?
- 5. Based on which parameters do we choose a transistor for a particular application

6. BJT BIASING SCHEMES

6.1 Objective

1. To design potential divider bias and fixed bias scheme of a transistor and to understand the operation of the circuit.
2. To analyze the BJT bias circuit and to determine circuit voltage and current levels.

6.2 Hardware Required

S. No	Apparatus	Type	Range	Quantity
01	Transistor	BC107		1
02	Resistance		To be calculated	
03	Regulated power supply		(0 – 30V), 2A Rating	1
04	Ammeter	MC	To be calculated	
05	Voltmeter	MC	To be calculated	
06	Bread board			1
	Connecting wires			Few

6.3 Introduction

Transistor Biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor. A transistors steady state of operation depends a great deal on its base current, collector voltage, and collector current and therefore, if a transistor is to operate as a linear amplifier, it must be properly biased to have a suitable operating point

6.4 Potential Divider Biasing Circuit Operation

The voltage divider is formed using external resistors R_1 and R_2 . The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2 , the operating point of the transistor can be made independent of β . In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with

temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

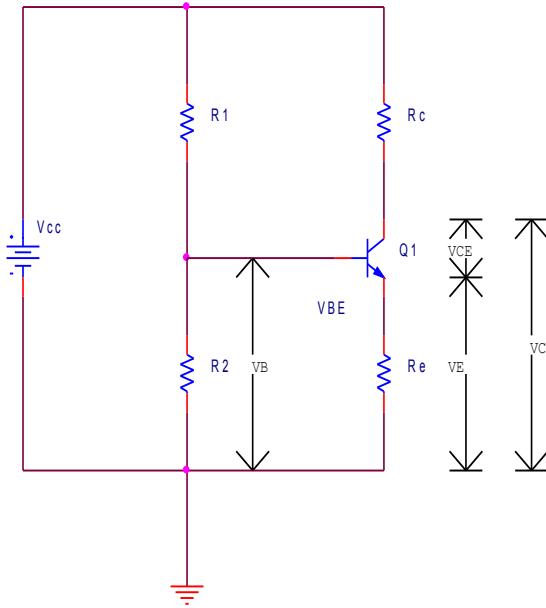


Fig. 6.1 Potential divider bias

6.4.1 Analysis

Referring to fig. 8-1,

$$V_B = V_{CC} \times R_2 / (R_1 + R_2)$$

With V_B constant, the voltage across the emitter resistor is also a constant quantity,

$$V_E = V_B - V_{BE}$$

This means that the emitter current is constant,

$$I_E = (V_B - V_{BE}) / R_E$$

The collector current is approximately equal to the emitter current, so I_C is held at a constant level.

$$I_C \approx I_E$$

The collector – emitter voltage is

$$V_{CE} = V_C - V_E$$

and the transistor collector voltage is

$$V_C = V_{CC} - I_C R_C$$

V_{CE} can also be determined as

$$V_{CE} \approx V_{CC} - I_C (R_C + R_E)$$

Clearly with I_C and I_E constant, the transistor collector – emitter voltage remains at a constant level. It should be noted that the transistor h_{FE} value is not involved in any of the above equations.

6.4.2 Potential divider bias circuit design.

When designing a voltage divider bias circuit the voltage divider current (I_2 in Fig. 8-1) should be selected much larger than the transistor base current I_B . This makes the base voltage V_B a stable quantity largely unaffected by the transistor h_{FE} value. However, a high level of I_2 result in smaller resistance values for R_1 and R_2 , and this gives the circuit undesirable low input impedance.

A rule of thumb approach to selection of I_2 is to use a voltage divider current approximately equal to one – tenth of the transistor collector current.

$$I_2 = I_C / 10$$

This gives reasonably large values for R_1 and R_2 while still keeping I_2 much large than I_B

If V_E is not specified, it should be selected much larger than the transistor V_{BE} ,

$$V_E \gg V_{BE}$$

This is because V_{BE} can vary from transistor to transistor, and it can also change with temperature increase or decrease. Making V_E very much larger than V_{BE} minimizes the effect of V_{BE} changes on the circuit bias conditions. Typically, as another rule of thumb, V_E is selected as 5v regardless of the supply voltage. When V_{CC} is low, V_E can be as low as 3V.

The equations used for calculating each resistor value are:

$$R_1 = (V_{CC} - V_B) / I_2$$

$$R_C = (V_{CC} - V_{CE} - V_E) / I_C$$

$$R_2 = V_B / I_2$$

$$R_E \approx V_E / I_C$$

6.5 Design Problem

Design the voltage divider bias circuit to have $V_{CE} = V_E = 5V$ and $I_C = 5mA$ when the supply voltage is 15V. Assume the transistor h_{fe} is 100.

Design procedure

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{5V}{5mA} = 1K\Omega \quad (\text{Standard value})$$

$$R_C = \frac{(V_{CC} - V_{CE} - V_E)}{I_C} = \frac{15V - 5V - 5V}{5mA} = 1K\Omega \quad (\text{Standard value})$$

$$I_2 = \frac{I_C}{10} = 500\mu A$$

$$V_B = V_E + V_{BE} = 5V + 0.7V = 5.7V$$

$$R_2 = \frac{V_B}{I_2} = \frac{5.7V}{500\mu A} = 11.4K\Omega \quad (\text{Use } 12K\Omega \text{ standard value})$$

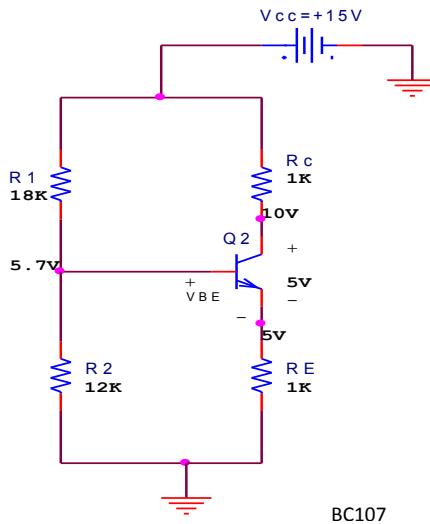
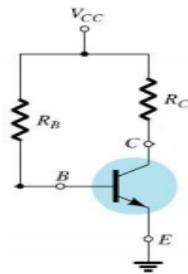


Fig 6.2 Voltage divider bias circuit designed

$$R_1 = \frac{(V_{CC} - V_B)}{I_2} = \frac{15V - 5.7V}{500\mu A} = 18.6K\Omega \quad (\text{use } 18k\Omega \text{ standard value})$$

6.6 Fixed Bias Circuit Operation



BC107

Fig 6.3 Fixed bias circuit

6.7 DC Analysis

Applying KVL to the input loop:

$$V_{cc} = I_B R_B + V_{be}$$

From the above equation, deriving for I_B , we get,

$$I_B = [V_{cc} - V_{be}] / R_B$$

The selection of R_B sets the level of base current for the operating point. Applying KVL for the output loop:

$$V_{cc} = I_C R_C + V_{ce}$$

Thus,

$$V_{ce} = V_{cc} - I_C R_C$$

In circuits where emitter is grounded,

$$V_{ce} = V_E$$

$$V_{be} = V_B$$

6.8 Design Problem

Design the fixed bias circuit to have $V_{CE} = V_E = 5V$ and $I_C = 50mA$ when the supply voltage is 10V. Assume the transistor h_{fe} is 239

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{10V - 5V}{50mA} = 100\Omega$$

$$I_B = \frac{I_C}{\beta} = 50mA / 239 = 209 \mu A$$

$$R_B = \frac{V_{CC}}{I_B} = \frac{10V}{209 \mu A} = 47K\Omega$$

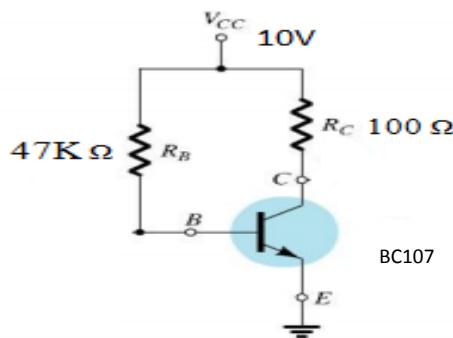


Fig 6.4 Designed Fixed Bias

When the transistor is biased such that I_B is very high so as to make I_C very high such that $I_C R_C$ drop is almost V_{CC} and V_{CE} is almost 0, the transistor is said to be in saturation.

$I_{C\text{ sat}} = V_{CC} / R_C$ in a fixed bias circuit.

6.9 Procedure

- Connect the components as per the circuit diagram.
- Calculate the theoretical value applying KVL in both input and output side.
- Find the practical value of voltages and currents at various point in the circuits,
- Plot the value in the tabular column.

6.10 Tabulation

6.10.1 Fixed Bias

PARAMETER	THEORITICAL VALUE	PRACTICAL VALUE
V_B		
V_C		
V_{BE}		
V_{CE}		
I_B		
I_C		

6.10.2 Voltage Divider Bias

PARAMETER	THEORITICAL VALUE	PRACTICAL VALUE
V_B		
V_C		
V_E		
V_{CE}		
V_{BE}		
I_C		
I_E		

6.11 PSPICE Simulation Procedure

1. Open Capture Lite Edition.
2. Go to the File menu and select New Project. Select Analog or Mixed A/D
3. Create a blank project and then click OK.

4. Select ‘Place’ option from tool bar. Pick and place all the required circuit components by just clicking on the elements.
5. Connect the components as per circuit diagram using ‘place wire’ button that is available in tool bar.
6. Click on each components to give the parameter values as per design. Save the schematic.
7. Create a new simulation profile. Mention the type of analysis and simulate the circuit.
8. Measure the voltages and currents at different points and tabulate the readings

6.12 Pspice Output

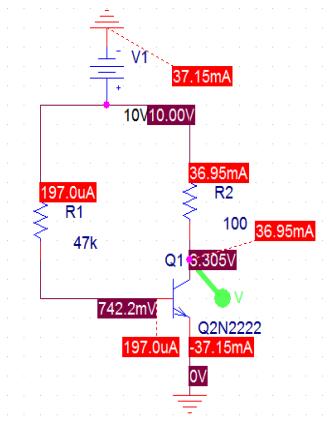


Fig 6.5 Schematic for Self Bias

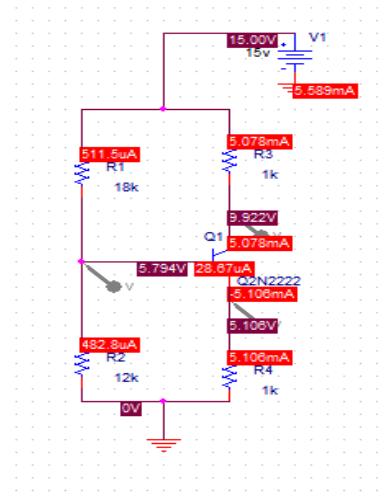


Fig 6.6 Schematic for Voltage Divider Bias

6.13 Result

Potential divider bias and fixed bias scheme of a transistor was constructed and the circuit voltage and current levels are determined.

6.14 Prelab Questions

1. What do you understand by transistor biasing? What is its need?
2. What do you understand by stabilization of Q-point?
3. Define Q-point and explain the concept of dc load line.

6.15 Postlab Questions

1. In the implementation of voltage divider bias (VDB) circuit change the value of R_1 to R_2 and then to $2R_1$ and measure the Q-point in each case. Comment on the changes in the Q-point values.
2. For the voltage divider bias (VDB) circuit implemented in the experiment, answer the following questions.
 - Does V_C increase or decrease if R_1 is increased?
 - Does I_C increase or decrease if $\beta(h_{fe})$ is reduced?
 - Does I_C increase or decrease if V_{CC} is reduced?
 - What happens to V_{CE} if the transistor is replaced one with larger β (h_{fe})?
 - What happens to I_C (sat) if β is increased?
 - What happens to V_{CE} if the ground leg of R_2 opens?
 - What happens to V_{CE} if the transistor EB junction fails by becoming open?
 - What happens to V_{CE} if the transistor EB junction fails by becoming a short
 - How will V_E be affected when replacing the collector resistor with one whose resistance is at the lower end of the tolerance range?
 - If the transistor collector junction becomes open, what will happen to V_E ?
 - Analyze the circuit to investigate the effect of interchanging the voltage divider resistors.

7. SERIES AND SHUNT REGULATORS

7.1 Objective

1. To design a series, shunt voltage regulator
2. To find load regulation
3. To find line regulation

7.2 Hardware Required

S. No	Apparatus	Type	Range	Quantity
1	Power transistor	2N3055		1
2	Transistor		BC147	1
3	Zener diode	1Z6.2, 1Z5.1		1
4	Resistors		1KΩ, 947Ω, 2.48KΩ, 2.2kΩ, 2.75KΩ, 49.6Ω, 10% tolerance, ½ watt	1
5	Voltmeter	MC	(0 – 30)V	1
6	Bread board & wires			
7.	Decade Resistance Box		50Ω	1

7.3 Introduction

The term regulation is the ability of the power supply source to maintain a constant output voltage in spite of line voltage fluctuations and changes in load current

The factors of poor regulation are

1. The line voltage changes which causes a dc output change and the ripple content of the dc input due to inadequate filtering.
2. The load current changes which causes a variable internal drop due to the internal resistance of the regulator and the consequent change in the output voltage and
3. The temperature coefficient of the device parameters which results in a change of the output voltage.

Voltage regulators can be classified by the method of achieving regulation as linear regulators and switching regulators. They are also classified by the way they are connected to the load as series regulators and shunt regulators. Standard regulator contains three basic elements namely a

precision voltage reference, an error amplifier and a power control element.

In series voltage regulator the transistor Q₂ functions both as a voltage comparator and dc amplifier. Any increase in the output voltage V_o either due to the input-voltage variation or change of load results in increase of V_{BE} of the transistor Q₂. Hence the collector current I_{C2} increases. Due to this the total current flowing through R₃ increases. Hence the collector voltage of Q₂ decreases.

Since the base of Q₁ is tied to the collector of T₂, the base voltage of Q₁ with respect to ground decreases thereby decreasing the forward bias of the emitter junction of Q₂. Hence the collector emitter voltage of Q₁ has to increase in order to maintain the same emitter current. If the change in V_{CE} of Q₁ can be made equal to V_i then the output voltage will remain constant. Since V_{CBI} = V_{CEI}. We can assume that if V_i dropped across R₃, then the output voltage will remain constant.

The function of a voltage regulator is to provide a stable dc voltage to electronic circuits and capable of providing substantial output current. Since the element or component used for voltage regulation is connected across the load, it is called as shunt voltage regulator. There are two types of shunt voltage regulator

1. Zener diode shunt voltage regulator
2. Transistor shunt voltage regulator

A zener diode is connected in parallel with the load; a resistance (R₂) is connected in series with the zener to limit the current in the circuit. Hence the resistance is called as series current limiting resistor. The output voltage (V_o) is taken across the load resistance (R₁). Since the reverse bias characteristics of zener diode are used in voltage regulation, the input voltage is always maintained greater than zener voltage (V_z).

5.3.1 Line Regulation

Line regulation is a measure of the ability of the power supply to maintain its output voltage given changes in the input line voltage. Line regulation is expressed as percent of change in the output voltage relative to the change in the input line voltage.

Line regulation = $\frac{(\text{output voltage at High line input voltage} - \text{output voltage at low line input voltage})}{\text{High line input voltage} - \text{low line input voltage}} \times 100$

5.3.2 Load Regulation

Load regulation is a measure of the ability of an output channel to remain constant given changes in the load. Depending on the control mode enabled on the output channel, the load regulation specification can be expressed in one of two ways. In constant voltage mode, variations in the load result in changes in the output current. This variation is expressed as a percentage of range per amp of output load and is synonymous with a series resistance. In constant voltage mode, the load regulation specification defines how close the series resistance of the output is to 0 ohms - the series resistance of an ideal voltage source.

In constant current mode, variations in the load result in changes to the current through the load. This variation is expressed as a percentage of range change in current per volt of change in the output voltage and is synonymous with a resistance in parallel with the output channel terminals. In constant current mode, the load regulation specification defines how close the output shunt resistance

is to infinity—the parallel resistance of an ideal current. In fact, when load regulation is specified in constant current mode, parallel resistance is expressed as 1/load regulation.

Load Regulation can be defined as a percentage by the equation:

$$\text{Percent of regulation} = \frac{(E_{nL} - E_{fL})}{E_{fL}} \times 100$$

Where

- FullLoad (E_{fL}) is the load that draws the greatest current (is the lowest specified load resistance - never short circuit)
- MinimumLoad (E_{nL}) is the load that draws the least current (is the highest specified load resistance - possibly open circuit for some types of linear supplies, usually limited by pass transistor minimum bias levels)

- NominalLoad (E_{IL}) is the typical specified operating load

7.4 Circuit Diagram - Series Voltage Regulator

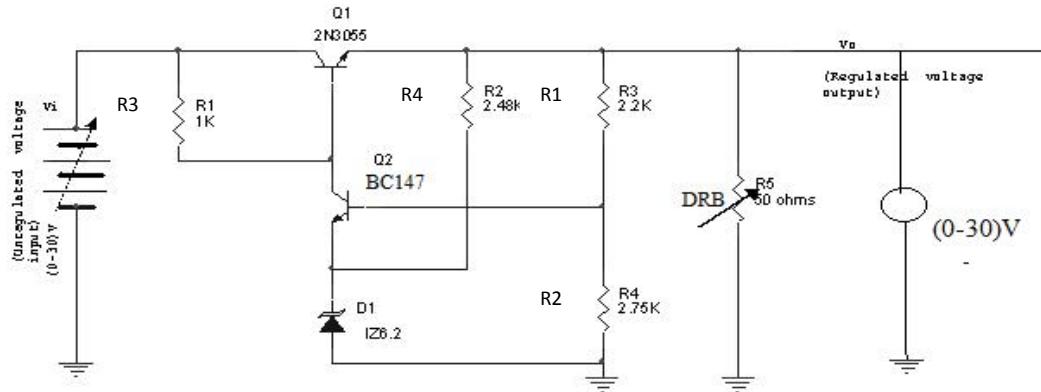


Fig 7.1 Circuit diagram of Series Voltage Regulator

7.5 Model Graph

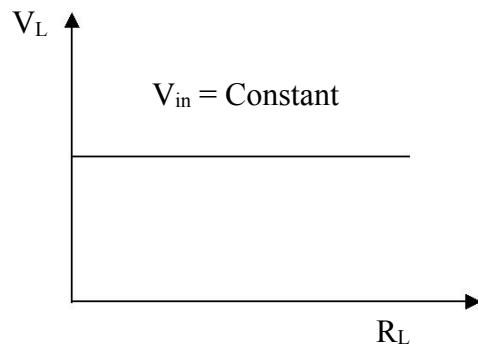


Fig 7.2 LOAD REGULATION

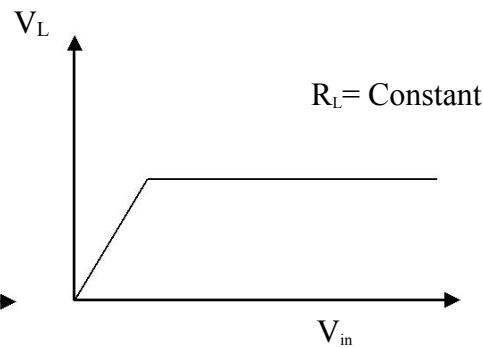


Fig 7.3 LINE REGULATION

7.6 PSPICE Simulation for Series Voltage Regulator

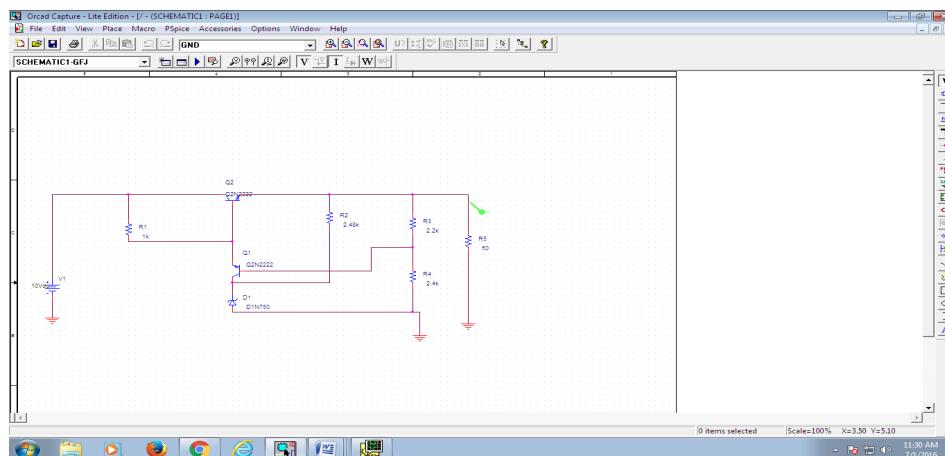


Fig 7.4 PSPICE Simulation of Series Voltage Regulator

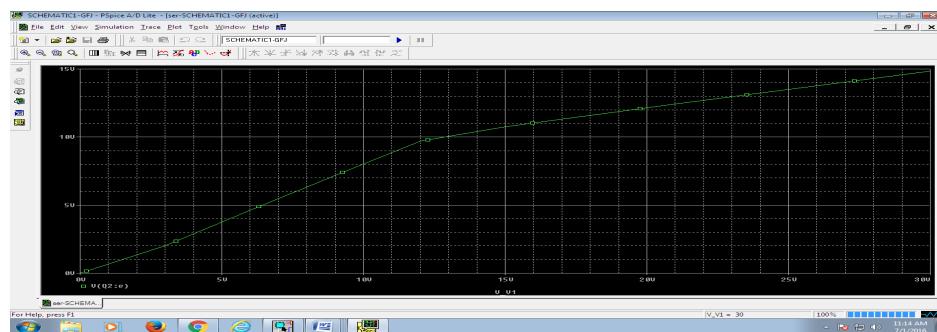


Fig 7.5 Line Regulation

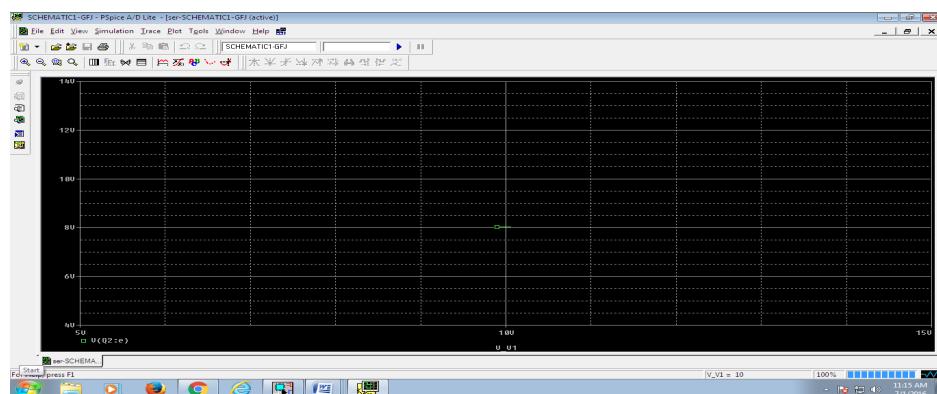


Fig 7.6 Load Regulation

7.7 Circuit Diagram - Shunt Voltage Regulator

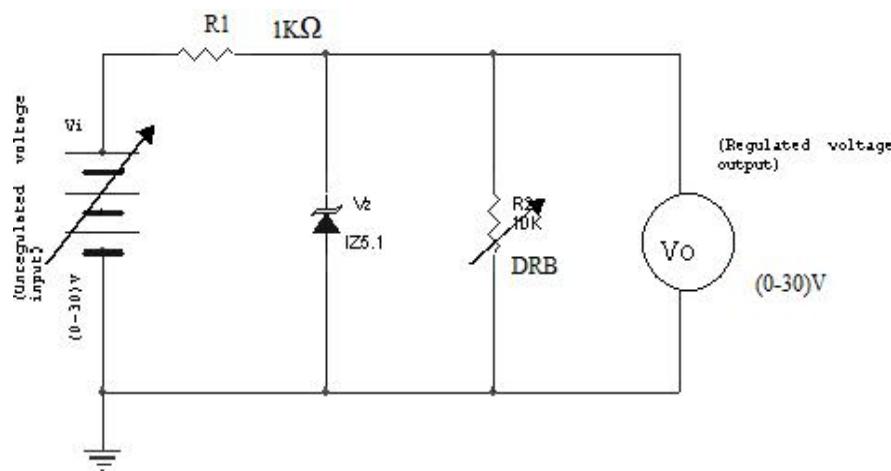


Fig 7.7 Circuit diagram of Shunt Voltage Regulator

7.8 PSPICE Simulation for Shunt voltage Regulator

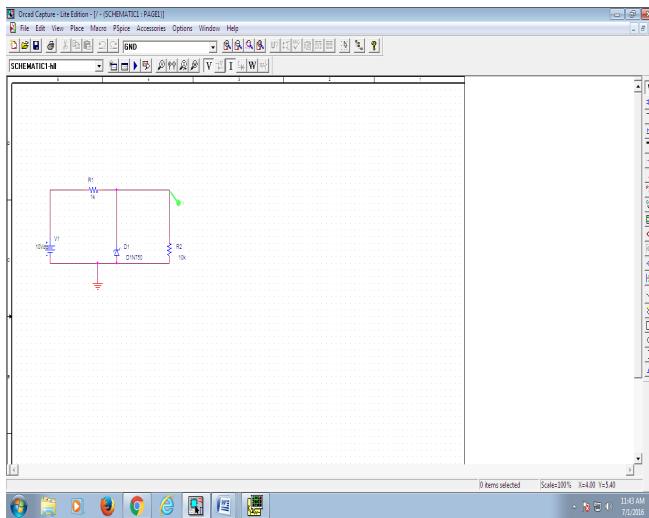


Fig 7.8 PSPICE Simulation of Shunt Voltage Regulator

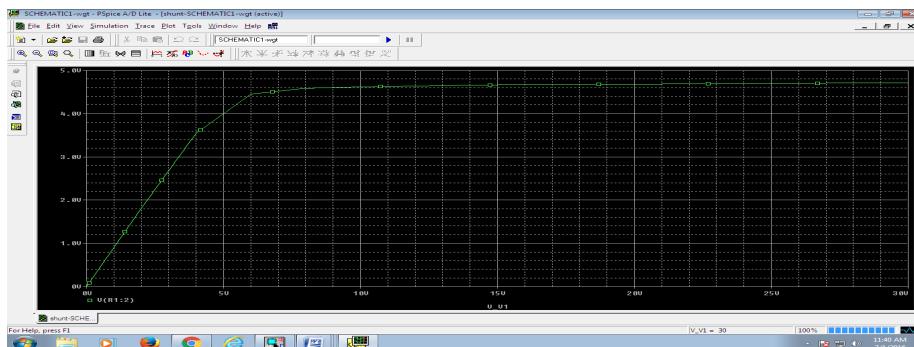


Fig 7.9 Line Regulation

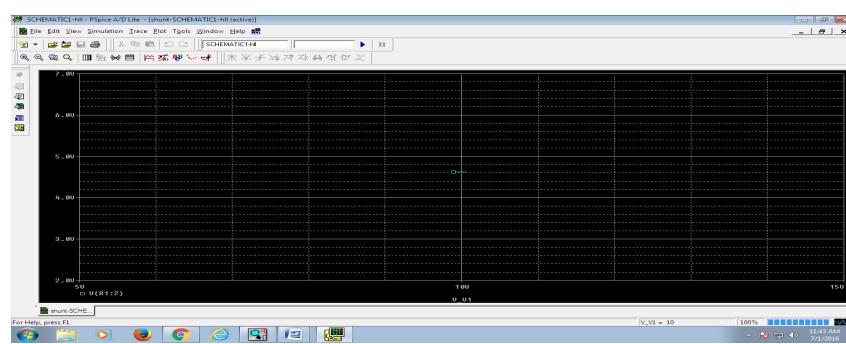


Fig 7.10 Load Regulation

7.9 Characteristics

Series Voltage Regulator

This series voltage regulator is suitable only for low output voltages because of the following reasons

1. With the increase in room temperature, the values of V_{be} and V_{Zener} tend to decrease.

Thus the output voltage cannot be maintained a constant. This will further increase the transistor base emitter voltage and thus the load.

2. There is no option to change the output voltage in the circuit.
3. Due to small amplification process provided by only one transistor(BC147), the circuit cannot provide good regulation at high currents.
4. The power dissipation of a pass transistor is large because it is equal to $V_{cc}I_c$ and almost all variation appears at V_{ce} and the load current is approximately equal to collector current. Thus for heavy load currents pass transistor has to dissipate a lot of power and, therefore, circuit becomes hot. So some heat sink is required.

Shunt Voltage Regulator

The series resistor causes a huge amount of power loss. The circuit may have problems regarding over voltage mishaps.

7.10 Procedure

Connect the circuit as per the circuit diagram.

1. For load regulation characteristics, keep the input voltage constant, find V_L for different values of R_L . Plot the graph by taking R_L in the axis and V_L in the Y axis.
2. For line regulation characteristics, keep R_L constant and for different values of input V_{in} find V_L . Plot the graph by taking V_{in} in x axis and V_L in the y axis

7.11 Tabulation

7.11.1 Series Regulator Line regulation $RL = \text{-----} (\Omega)$

S. No	$V_i (V)$	$V_o (V)$
1.		
2.		
3.		
4.		
5.		
6.		
7.		
8.		

9.		
10		
11		
12		

$$V_i = \text{-----} (V)$$

7.11.2 Load regulation

S.No	$R_L(\Omega)$	$V_o(V)$
1.		
2.		
3.		
4.		
5.		
6.		

7.11.3 Shunt Regulator Line regulation $RL = \text{-----} (\Omega)$

S. No	$V_i (V)$	$V_o (V)$
1.		
2.		
3.		
4.		
5.		
6.		
7.		
8.		
9.		

10		
11		
12		

$$V_i = \text{-----} (V)$$

7.11.4 Load regulation

S.No	$R_L(\Omega)$	$V_o(V)$
1.		
2.		
3.		
4.		
5.		
6.		

7.12 Result

The series and shunt voltage regulator were designed and constructed and the characteristics were plotted.

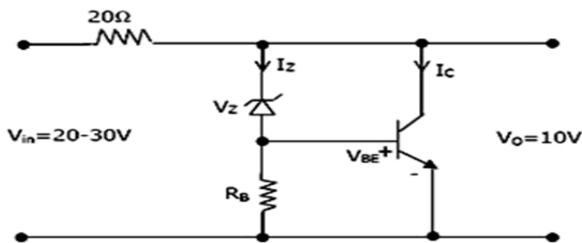
1. The regulated output voltage was found to be -----V
- .2. Line regulation was found to be -----
3. Load regulation was found to be -----

7.13 Prelab Question

1. What are the three basic elements inside a standard voltage regulator?
2. What device is used as a control element? Why?
3. What are the performance measures of the regulator?
4. What is line regulation and Load regulation What is the efficiency of series voltage regulator
5. List the difference between Series and Shunt Voltage Regulator

7.14 Post Lab Question

- With reference to the above circuit (fig 7.4), What will be the output voltage if reference voltage was short circuited?
- The 7812 regulator IC provides _____.
 - 5V
 - 5V
 - 12V
 - 12V
- what will happen if potential divider was open circuited
- The transistor shunt regulator shown in figure has a regulated output voltage of 10 volts, when input varies from 20 volts to 30 volts. The relevant parameters for the zener diode and the transistor are: $V_z = 9.5$ volts, $V_{BE} = 0.3$ volts, $\beta = 99$. Neglect the current through R_B . Then the maximum power dissipated in the zener diode (P_z) and the transistor (P_T) are



- (a) $P_z=75\text{mW}, P_T=7.9\text{W}$
- (b) $P_z=85\text{mW}, P_T=8.9\text{W}$
- (c) $P_z=95\text{mW}, P_T=9.9\text{W}$
- (d) $P_z=115\text{mW}, P_T=11.9\text{W}$

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8.CHARACTERISTICS OF METAL OXIDE SEMICONDUCTOR FIELD

EFFECT TRANSISTORS (MOSFETS) USING PSPICE

8.1 Objective

To simulate drain and transfer characteristics of MOSFET using Pspice Capture Lite Software and to find its drain resistance and transconductance.

8.2. Theory

In a MOSFET, current flows from the drain terminal to the source terminal through a semiconductor channel. The resistance of the channel, and therefore its ability to conduct current, is controlled by a voltage applied to a third terminal denoted as the gate. MOSFETs can be either an n-channel type or a p-channel type. In a n-channel MOSFET a positive voltage is applied to the drain terminal for operation while in a p-channel MOSFET a negative voltage is applied to the drain terminal for operation. An n-channel and p-channel type MOSFET may be one of two modes; enhancement mode or depletion mode. The enhancement mode MOSFET is normally “off” (in cutoff and conducting no current) when no voltage is applied to the gate and is “on” (in saturation and conducting current) when a voltage greater than the gate-to-source threshold is applied to the gate. The depletion mode MOSFET is normally “on” (in saturation and conducting current) when no voltage is applied to the gate and is “off” (in cutoff and not conducting current) when a voltage more negative than the gate-to-source threshold is applied to the gate.

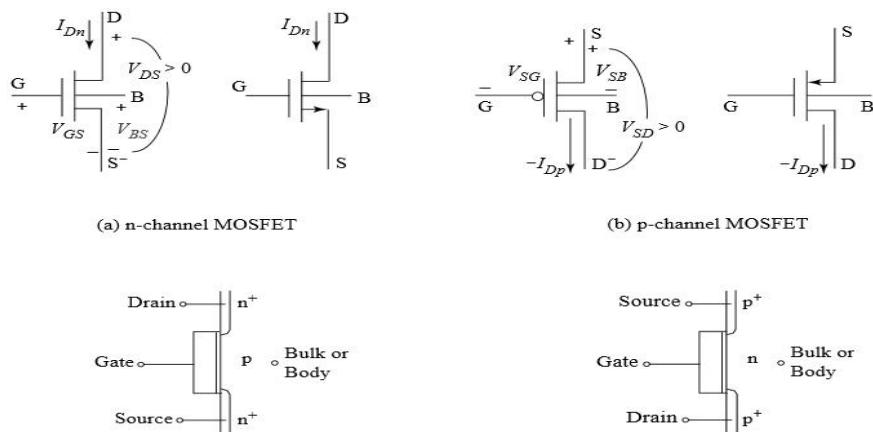


Fig 8.1 Symbol of MOSFET

8.2.1 Transfer Characteristics

In most MOSFET applications, an input signal is the gate voltage V_G and the output is the drain current I_D . The ability of MOSFET to amplify the signal is given by the output/input ratio: the transconductance, $g_m = dI_D/dV_{GS}$ with V_{DS} constant

8.2.2 Drain Characteristics

MOSFET operates in three operation mode, Cut-off when $V_{GS} < V_t$, Linear mode when $V_{GS} > V_t$ and $V_{DS} < (V_{GS} - V_t)$ and Saturation when $V_{GS} > V_t$ and $V_{DS} \geq (V_{GS} - V_t)$. Pinch off occurs when $V_{DS} = V_{Sat} = V_{GS} - V_t$. The drain resistance, $R_d = dV_{DS}/dI_D$ with V_{GS} constant

8.3 Circuit Diagram

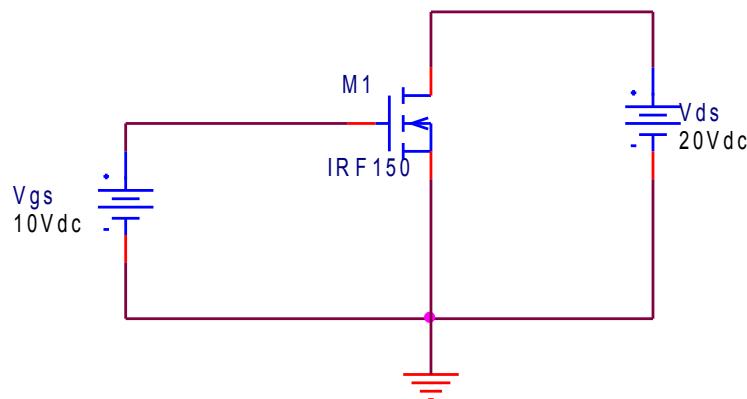
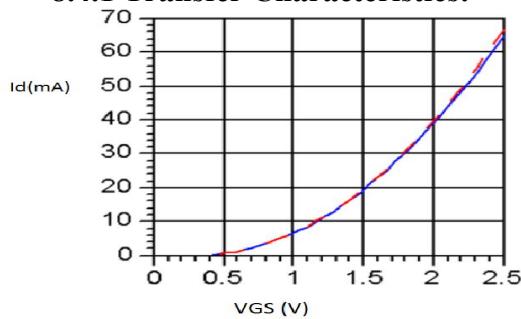


Fig 8.2 MOSFET Characteristics Circuit diagram.

8.4 Model Graph

8.4.1 Transfer Characteristics:



8.4.2 Drain Characteristics:

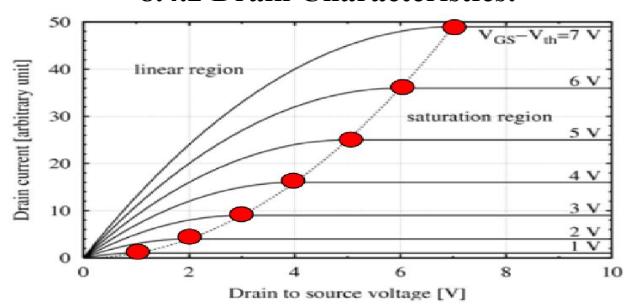


Fig 8.3 Characteristics of MOSFET

8.5 PSPICE Simulation for MOSFET Characteristics

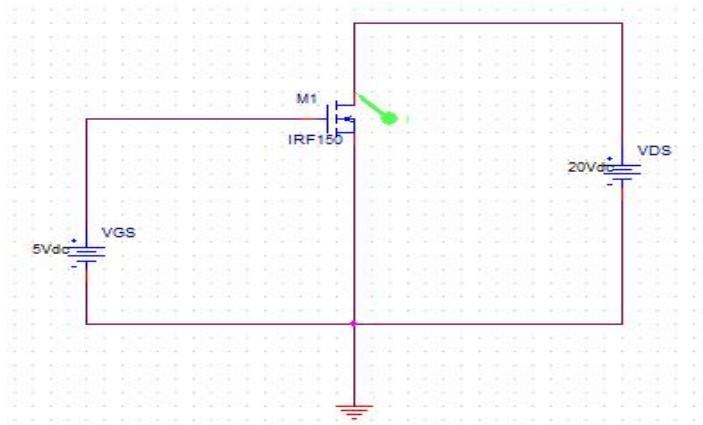


Fig 8.4 PSPICE Simulation

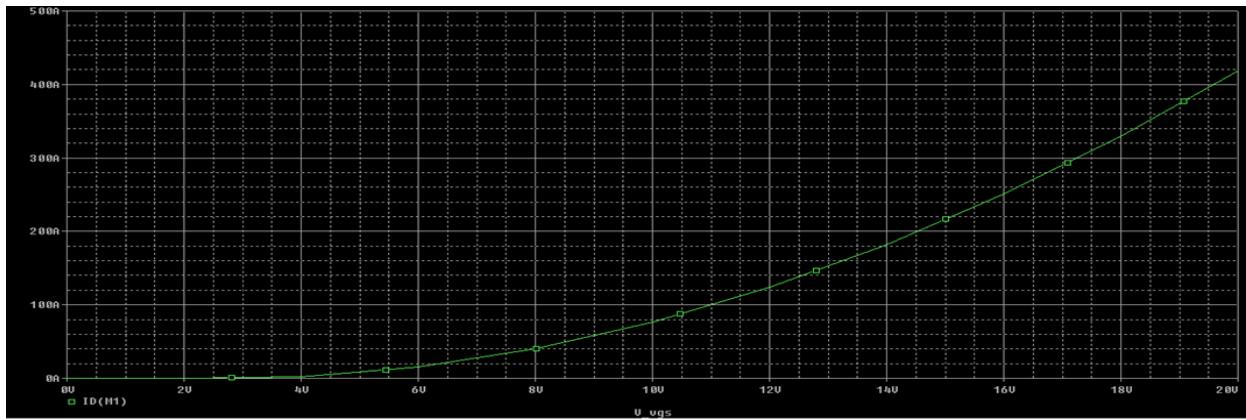


Fig 8.5. MOSFET – Transfer characteristics

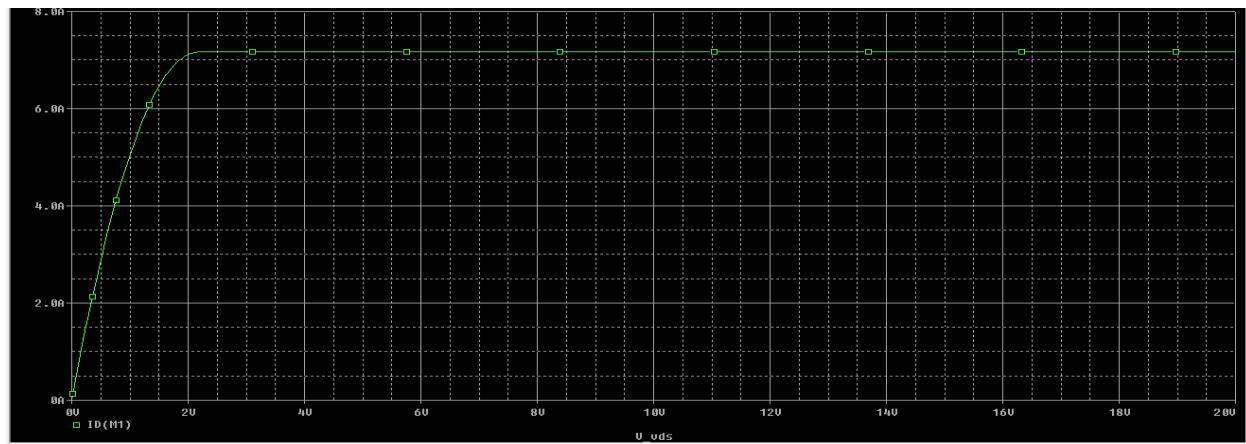


Fig 8.6 MOSFET – Drain characteristics

8.6 Handling Precautions

1. When handling power MOS FETs, the man should be ground. And Power MOS FETs, should be handled by the package, not by the leads.
2. When handling or installing Power MOS FETs into circuits, use metal plates that it grounded on Work Stations.
3. When testing Power MOS FETs, Test Circuit (Curve tracer, etc.) should be grounded.
4. When using soldering irons, soldering irons should be grounded. (It's better to use battery operated soldering irons.)
5. When shipping in circuit boards, they should be placed in antistatic bags, unless the gate and the source are connected by resistors or inductors.
6. Power MOS FETs should be placed not in plastic casesor bags, but in antistatic bags, conductive foam, or aluminum foil.

8.7 Procedure

8.7.1 Transfer characteristics

1. Connect the MOSFET as per the circuit diagram
2. Keep the $V_{GS} = 10 \text{ V}$, $V_{DS} = 20 \text{ V}$
3. Set in the DC sweep primary and secondary values.
4. Place the voltage probe at source of MOSFET and simulate the circuit.

8.7.2 Drain characteristics

1. Connect the MOSFET as per the circuit diagram
2. Keep the $V_{GS} = 10 \text{ V}$, $V_{DS} = 20 \text{ V}$
3. Set in the DC sweep primary and secondary values.
4. Place the voltage probe at source of MOSFET and simulate the circuit

8.8 Result

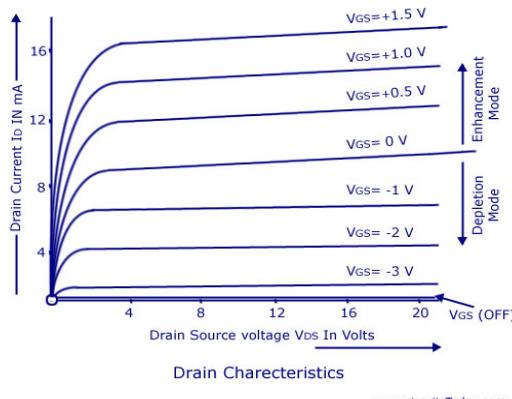
The drain Characteristics and Transfer Characteristics of MOSFET was simulated using Pspice , the transconductance = _____ and drain resistance = ----- was found.

8.9 PreLab Questions

1. With the E-MOSFET, when gate input voltage is zero, what is the drain current?
2. When is a vertical channel E-MOSFET used?
3. Compare the input impedance of MOSFET with that of BJT and FET.
4. In MOSFET devices the N-channel type is better the P-channel type. How?

8.10 Post lab Questions

1. In a MOSFET, the polarity of the inversion layer is the same as that of _____
2. What is the difference between depletion MOSFET and JFET.
3. What are the three regions of operation in MOSFET?
4. Interpret transfer characteristics from the given drain characteristics for MOSFET.



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9. MOSFETS BIASING CIRCUITS

9.1 Objective

To perform biasing of MOSFET using Pspice Capture Lite Software.

9.2. Theory

In a MOSFET, current flows from the drain terminal to the source terminal through a semiconductor channel. The resistance of the channel, and therefore its ability to conduct current, is controlled by a voltage applied to a third terminal denoted as the gate. MOSFETs can be either an n-channel type or a p-channel type. In a n-channel MOSFET a positive voltage is applied to the drain terminal for operation while in a p-channel MOSFET a negative voltage is applied to the drain terminal for operation. An n-channel and p-channel type MOSFET may be one of two modes; enhancement mode or depletion mode. The enhancement mode MOSFET is normally “off” (in cutoff and conducting no current) when no voltage is applied to the gate and is “on” (in saturation and conducting current) when a voltage greater than the gate-to-source threshold is applied to the gate. The depletion mode MOSFET is normally “on” (in saturation and conducting current) when no voltage is applied to the gate and is “off” (in cutoff and not conducting current) when a voltage more negative than the gate-to-source threshold is applied to the gate.

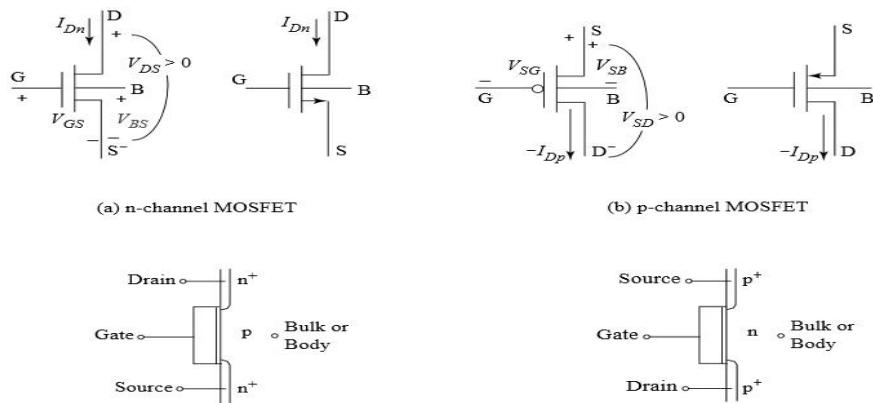


Fig 9.1.symbol of MOSFET

9.2.1 Voltage Divider Bias

Voltage divider bias is used to produce DC gate bias voltage greater than $V_{GS(Th)}$. The value of resistors used in the divider circuit is quite high as E-MOSFET gate draws very little current due to SiO_2 layer.

9.2.2 Drain Feedback Bias

This method is similar to collector feedback bias used with BJT. When MOSFET is conducting, it has drain current of $I_{D(on)}$ and drain voltage $V_{DS(on)}$. Since there is no gate current $V_{GS} = V_{DS(on)}$. If I_D increases, V_{DS} will decrease (since larger voltage drop across R_L)

$$I_D \uparrow \rightarrow V_{DS} \downarrow \rightarrow V_{GS} \downarrow \rightarrow I_D \downarrow$$

E-MOSFET Small Signal Model. We find behavior of the device from its characteristics. In E-MOSFETs we have two characteristics, transfer characteristic and drain characteristic, we will find model from these characteristics. The equivalent is shown in the figure. Note that V_{gs} is the voltage between gate to source open circuit shows that no gate current flows. There is current source between drain and source ie drain current represented by g_m . V_{gs} Same representation for both n and p type MOSFETs .

9.3 Circuit Diagram

9.3.1 Voltage Divider bias

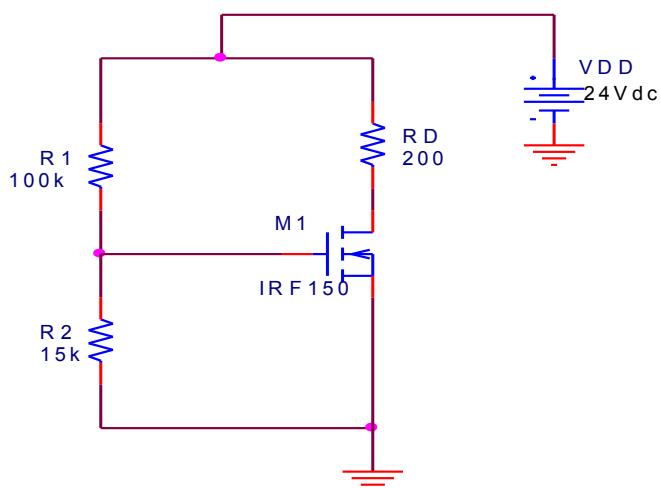


Fig 9.2 MOSFET Voltage divider bias.

9.3.2 Drain Feedback bias

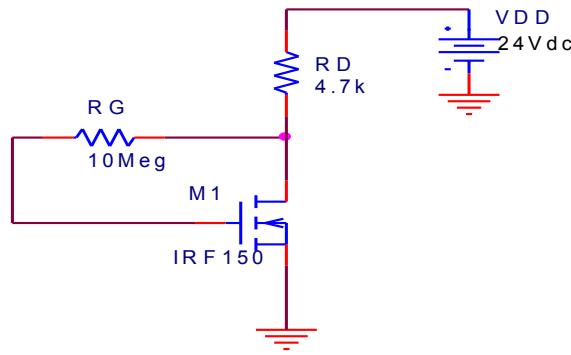


Fig 9.3 MOSFET Drain feedback bias.

9.3.3 Design Specifications voltage divider bias and drain feedback bias

$$V_{gs} = \left[\frac{R_1}{R_1 + R_2} \right] V_{DS}$$

$$V_G = V_{GS} = \left[\frac{R_2}{R_1 + R_2} \right] V_{DD}$$

$$V_{gs} = V_{DD} - V_G$$

$$V_g = \left[\frac{15 \times 10^3}{100 \times 10^3 + 15 \times 10^3} \right] \times 24$$

$$R_1 = 15 \times 10^3 \Omega$$

$$R_2 = 100 \times 10^3 \Omega$$

$$V_{gs} = 24 - 0.6$$

$$V_{gs} = 23.4V$$

$$\begin{aligned} I_D &= K_N (V_{gs} - V_{TN})^2 \\ &= 1(23.4 - 1.5)^2 \\ I_D &= 0.479mA \end{aligned}$$

9.4 PSPICE Simulation for Voltage divider bias and drain feedback of MOSFET

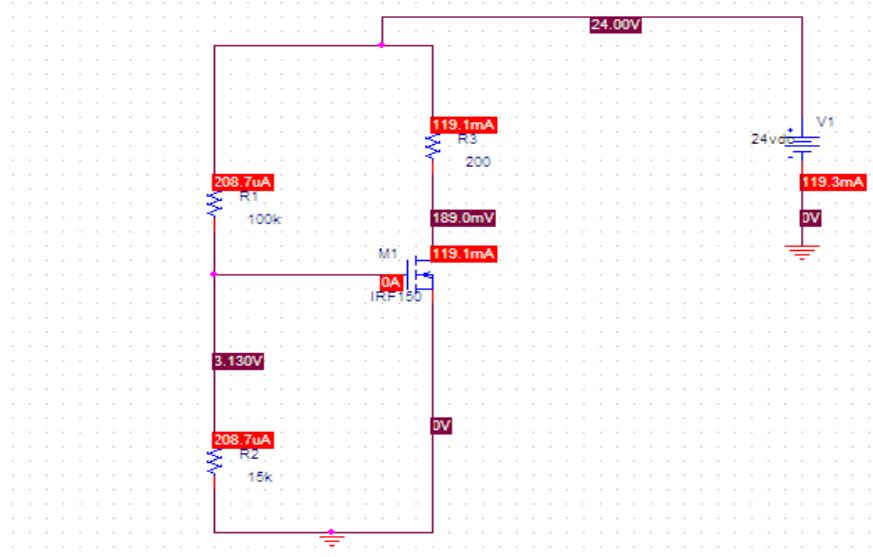


Fig 9.4 PSPICE simulation of Voltage Divider bias for MOSFET

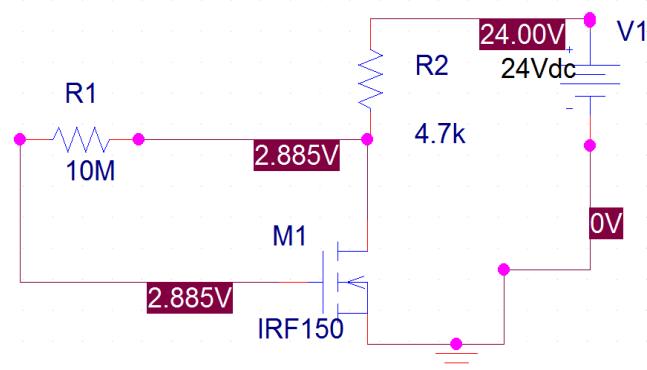


Fig 9.5 PSPICE simulation of Drain feedback bias for MOSFET

9.5 Procedure

9.5.1 Simulation of Voltage Divider bias

1. Connect the MOSFET as per the circuit diagram
2. Keep the VDS = 24 V
3. Set the biasing point.
4. Simulate the circuit voltage divider circuit.

9.5.2 Simulation of Drain feedback bias

1. Connect the MOSFET as per the circuit diagram
2. Keep the VDD = 24 V
3. Set the biasing point.

4. Simulate the circuit drain feedback bias circuit.

9.6 Handling Precautions

1. When handling power MOS FETs, the man should be ground. And Power MOS FETs, should be handled by the package, not by the leads.
2. When handling or installing Power MOS FETs into circuits, use metal plates that it grounded on Work Stations.
3. When testing Power MOS FETs, Test Circuit (Curve tracer, etc.) should be grounded.
4. When using soldering irons, soldering irons should be grounded. (It's better to use battery operated soldering irons.)
5. When shipping in circuit boards, they should be placed in antistatic bags, unless the gate and the source are connected by resistors or inductors.
6. Power MOS FETs should be placed not in plastic casesor bags, but in antistatic bags, conductive foam, or aluminum foil.

9.7 Result

The biasing of MOSFET was simulated using Pspice.

9.8 PreLab Questions

1. What is the meaning of voltage divider bias?
2. What is the concept of drain feedback bias?
3. Compare the biasing of MOSFET with JFET.
4. What is the difference E-MOSFET and D-MOSFET?

9.9 Post lab

1. A very simple bias for a E-MOSFET is called -----
2. What is the different type of biasing in MOSFET?
3. Compare voltage divider bias and drain voltage bias in MOSFET.

10.BJT & MOSFET SWITCHING CIRCUITS

10.a. BJT SWITCHING

10.a.1 Objective

To study the switching characteristics of a bipolar junction transistor in Common Emitter

configuration.

10.a.2 Hardware Required

S. No	Apparatus	Type	Range	Quantity
01	Transistor	BC147		1
02	Resistance		1kΩ & 5kΩ, 10% tolerance, 1/2 watt rating	1
03	Regulated power supply		(0 – 30V), 2A Rating	1
04	Ammeter	MC	(1-30)mA, (0-500)µA	1
05	Voltmeter	MC	(0 – 1)V, (0 – 30)V	1
06	Bread board			1
	Connecting wires			Few

10.a.3 Introduction

Bipolar junction transistor (BJT) is a 3 terminal (emitter, base, collector) semiconductor device. There are two types of transistors namely NPN and PNP. It consists of two P-N junctions namely emitter junction and collector junction.

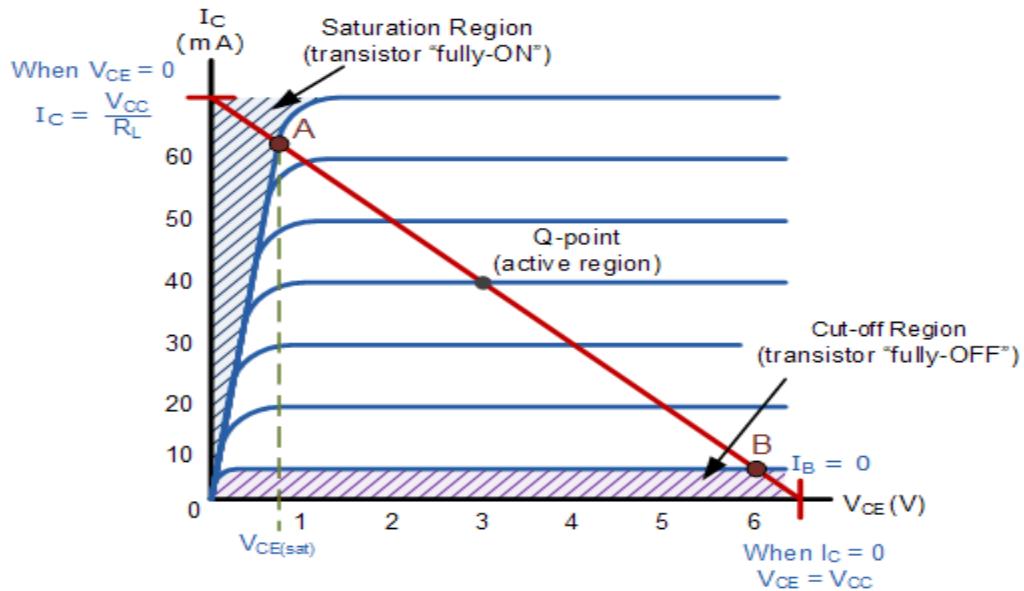
In Common Emitter configuration the input is applied between base and emitter and the output is taken from collector and emitter. Here emitter is common to both input and output and hence the name common emitter configuration.

When BJT used as an AC signal amplifier, the transistors Base biasing voltage is applied in such a way that it always operates within its “active” region, that is the linear part of the output characteristics curves are used. However, both the NPN & PNP type bipolar transistors can be made to operate as “ON/OFF” type solid state switch by biasing the transistors base differently to that of a signal amplifier.

Solid state switches are one of the main applications for the use of transistor to switch a DC output “ON” or “OFF”. Some output devices, such as LED’s only require a few milliamps at logic level DC voltages and can therefore be driven directly by the output of a logic gate. However, high power devices such as motors, solenoids or lamps, often require more power than

that supplied by an ordinary logic gate so transistor switches are used.

The areas of operation for a transistor switch are known as the **Saturation Region** and the **Cut-off Region**. This means then that we can ignore the operating Q-point biasing and voltage divider circuitry required for amplification, and use the transistor as a switch by driving it back and forth between its “fully-OFF” (cut-off) and “fully-ON” (saturation) regions as shown below.



The shaded area at the bottom of the curves represents the “Cut-off” region while the shaded area to the left represents the “Saturation” region of the transistor. Both these transistor regions are defined as:

Cut-off Region

Here the operating conditions of the transistor are zero input base current (I_B), zero output collector current (I_C) and maximum collector voltage (V_{CE}) which results in a large depletion layer and no current flowing through the device. Therefore the transistor is switched “Fully-OFF”. The cut-off characteristics circuit diagram shows

- The input and Base are grounded (0v)
- Base-Emitter voltage $V_{BE} < 0.7V$
- Base-Emitter junction is reverse biased
- Base-Collector junction is reverse biased
- Transistor is “fully-OFF” (Cut-off region)

- No Collector current flows ($I_C = 0$)
- $V_{OUT} = V_{CE}$
- Transistor operates as an “open switch”

Then we can define the “cut-off region” or “OFF mode” when using a bipolar transistor as a switch as being, both junctions reverse biased, $V_B < 0.7V$ and $I_C = 0$. For a PNP transistor, the Emitter potential must be negative with respect to the Base.

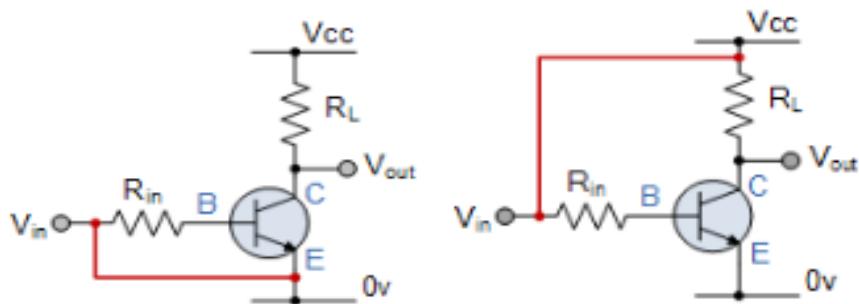
Saturation Region

Here the transistor will be biased so that the maximum amount of base current is applied, resulting in maximum collector current resulting in the minimum collector emitter voltage drop which results in the depletion layer being as small as possible and maximum current flowing through the transistor. Therefore the transistor is switched “Fully-ON”. The saturation characteristics circuit diagram shows

- The input and Base are connected to V_{CC}
- Base-Emitter voltage $V_{BE} > 0.7V$
- Base-Emitter junction is forward biased
- Base-Collector junction is forward biased
- Transistor is “fully-ON” (saturation region)
- Max Collector current flows ($I_C = V_{CC}/R_L$)
- $V_{CE} = 0$ (ideal saturation)
- $V_{OUT} = V_{CE} = 0V$
- Transistor operates as a “closed switch”

Then we can define the “saturation region” or “ON mode” when using a bipolar transistor as a switch as being, both junctions forward biased, $V_B > 0.7V$ and $I_C = \text{Maximum}$. For a PNP transistor, the Emitter potential must be positive with respect to the Base.

10.a.4 Circuit Diagram



$V_{cc} = 10 \text{ V}$; $R_L = 1\text{K}\Omega$; $R_{in} = 5\text{K}\Omega$

Fig 10.1 Cut-off Characteristics

Fig 10.2 Saturation Characteristics

10.a.5 Precautions

1. While doing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

10.a.6 Procedure

Cut-off Characteristics

1. Connect the transistor in CE configuration as per circuit diagram.
2. Connect the input and Emitter to ground.
3. Keep $V_{cc} = 10\text{V}$ by varying Regulated power supply.
4. Measure the voltage across V_{ce} .

Saturation Characteristics

1. Connect the transistor in CE configuration as per circuit diagram.
2. Connect the input and Base to V_{cc} .
3. Keep $V_{cc} = 10\text{V}$ by varying Regulated power supply.
4. Measure the voltage across V_{ce} .

10.a.7 Tabulation

Cutoff Characteristics		Saturation Characteristics	
V_{in} (volts)	V_{out} (volts)	V_{in} (volts)	V_{out} (volts)



10.a.8. Circuit diagram in PSPICE

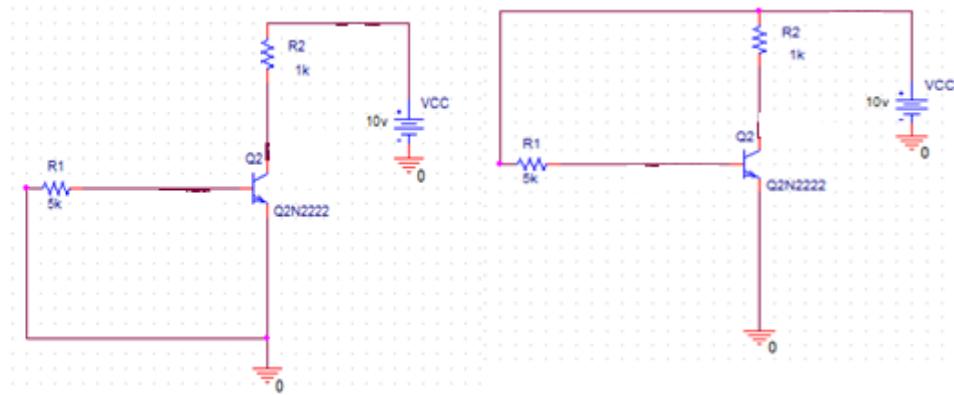


Fig 10.3 Cut-off Characteristics

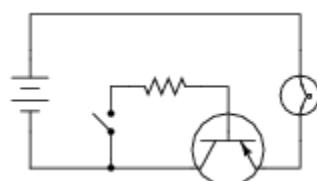
Fig 10.4 Saturation Characteristics

10.a.9. Result

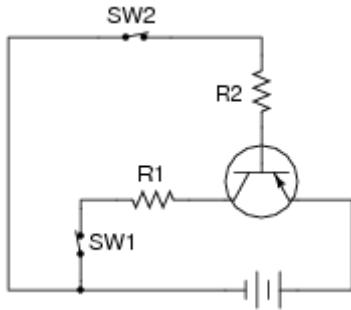
Thus the switching characteristics of BJT in CE configuration was verified.

10.a.10. Pre Lab Question

1. Solid-state switching circuits usually keep their constituent transistors in one of two modes: cutoff or saturation. Explain what each of these terms means?
2. Explain the function of this light-switching circuit, tracing the directions of all currents when the switch closes:



3. Trace the directions of all currents in this circuit, and determine which current is larger: the current through resistor R1 or the current through resistor R2, assuming equal resistor values.

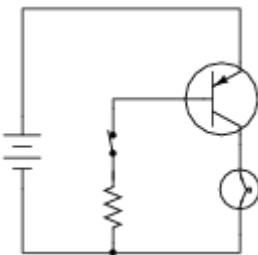


If switch SW2 were opened (and switch SW1 remained closed), what would happen to the currents through R1 and R2?

If switch SW1 were opened (and switch SW2 remained closed), what would happen to the currents through R1 and R2?

10.a.11. Post Lab Questions

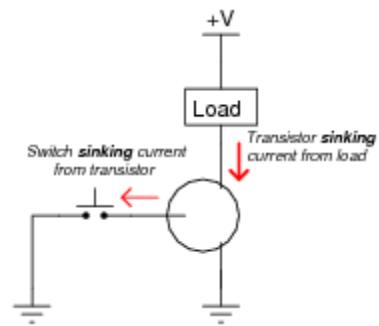
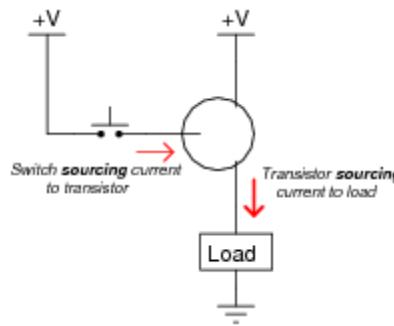
1. Calculate all component voltage drops in this circuit, assuming a supply voltage of 15 volts, an emitter-base forward voltage drop of 0.7 volts, and a (saturated) emitter-collector voltage drop of 0.3 volts:



2. Draw the necessary wire connections so that bridging the two contact points with your finger (creating a high-resistance connection between those points) will turn the light bulb on:



3. Choose the right type of bipolar junction transistor for each of these switching applications, drawing the correct transistor symbol inside each circle:



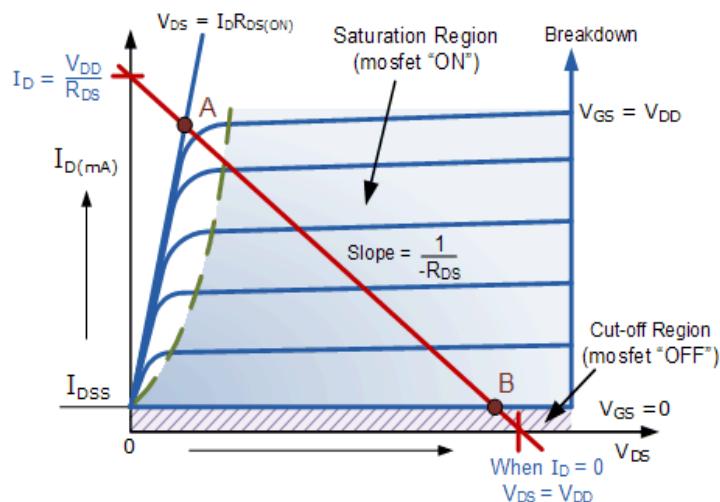
10.b. MOSFET SWITCHING

10.b.1 Objective

To study the switching characteristics of a Metal oxide semiconductor field effect transistor using Pspice.

10.b.2. Theory

We now know that there are two main differences between field effect transistors, depletion-mode only for JFET's and both enhancement-mode and depletion-mode for MOSFETs. In this experiment we will look at using the *Enhancement-mode MOSFET as a Switch* as these transistors require a positive gate voltage to turn “ON” and a zero voltage to turn “OFF” making them easily understood as switches and also easy to interface with logic gates. The operation of the enhancement-mode MOSFET, or e-MOSFET, can best be described using its i-v characteristics curves shown below. When the input voltage, (V_{IN}) to the gate of the transistor is zero, the MOSFET conducts virtually no current and the output voltage (V_{OUT}) is equal to the supply voltage V_{DD} . So the MOSFET is “OFF” operating within its “cut-off” region.



The minimum ON-state gate voltage required to ensure that the MOSFET remains “ON” when carrying the selected drain current can be determined from the v-i transfer curves above. When V_{IN} is HIGH or equal to V_{DD} , the MOSFET Q-point moves to point A along the load line. The drain current I_D increases to its maximum value due to a reduction in the channel resistance. I_D becomes a constant value independent of V_{DD} , and is dependent only on V_{GS} . Therefore, the transistor behaves like a closed switch but the channel ON-resistance does not

reduce fully to zero due to its $R_{DS(on)}$ value, but gets very small.

Likewise, when V_{IN} is LOW or reduced to zero, the MOSFET Q-point moves from point A to point B along the load line. The channel resistance is very high so the transistor acts like an open circuit and no current flows through the channel. So if the gate voltage of the MOSFET toggles between two values, HIGH and LOW the MOSFET will behave as a “single-pole single-throw” (SPST) solid state switch and this action is defined as:

Cut-off Region

Here the operating conditions of the transistor are zero input gate voltage (V_{IN}), zero drain current I_D and output voltage $V_{DS} = V_{DD}$. Therefore for an enhancement type MOSFET the conductive channel is closed and the device is switched “OFF”. The cut-off characteristics circuit diagram shows

- The input and Gate are grounded (0v)
- Gate-source voltage less than threshold voltage $V_{GS} < V_{TH}$
- MOSFET is “OFF” (Cut-off region)
- No Drain current flows ($I_D = 0$)
- $V_{OUT} = V_{DS}$
- MOSFET operates as an “open switch”

Then we can define the cut-off region or “OFF mode” when using an e-MOSFET as a switch as being, gate voltage, $V_{GS} < V_{TH}$ and $I_D = 0$. For a P-channel enhancement MOSFET, the Gate potential must be more positive with respect to the Source.

Saturation Region

In the saturation or linear region, the transistor will be biased so that the maximum amount of gate voltage is applied to the device which results in the channel resistance $R_{DS(on)}$ being as small as possible with maximum drain current flowing through the MOSFET switch. Therefore for the enhancement type MOSFET the conductive channel is open and the device is switched “ON”.

The Saturation characteristics circuit diagram shows

- The input and Gate are connected to V_{DD}
- Gate-source voltage is much greater than threshold voltage $V_{GS} > V_{TH}$
- MOSFET is “ON” (saturation region)
- Max Drain current flows ($I_D = V_{DD} / R_L$)
- $V_{DS} = 0V$ (ideal saturation)

- Min channel resistance $R_{DS(on)} < 0.1\Omega$
- $V_{OUT} = V_{DS} \approx 0.2V$ due to $R_{DS(on)}$
- MOSFET operates as a low resistance “closed switch”

Then we can define the saturation region or “ON mode” when using an e-MOSFET as a switch as gate-source voltage, $V_{GS} > V_{TH}$ and $I_D = \text{Maximum}$. For a P-channel enhancement MOSFET, the Gate potential must be more negative with respect to the Source.

10.b.3. Circuit Diagram

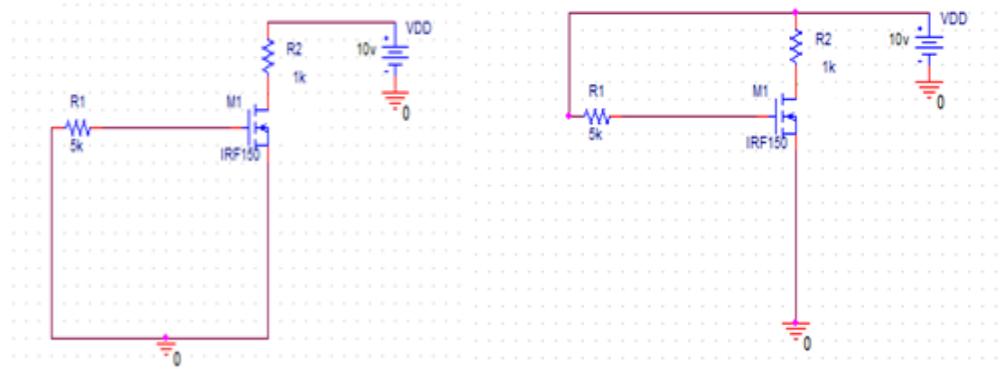


Fig 10.5 Cut-off Characteristics

Fig 10.6 Saturation Characteristics

10.b.4 Result

Thus the switching characteristics of MOSFET using Pspice was verified

10.b.5. Pre Lab Question

1. What is the computational the value of drain current for gate-to-source voltage (V_{GS}) of about 6V in the below drawn schematic diagram of E-MOSFET along with $ID(ON) = 2\text{mA}$ at $V_{GS} & V_{GS(\text{threshold})}$ of about 12V & 4V respectively?

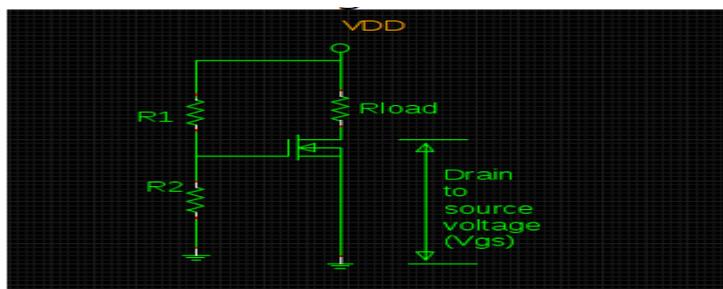


Fig. E-MOSFET Configuration

- a. 1 mA
 - b. 2 mA
 - c. 3 mA
 - d. 4 mA
2. Which mode is produced by a positive swing in gate-to-source voltage by input ac signal with the maximum voltage drop across load resistor in DE-MOSFET amplifier circuit?
- a. Depletion mode with decrease in drain current
 - b. Enhancement mode with decrease in drain current
 - c. Depletion mode with an increase in drain current
 - d. Enhancement mode with an increase in drain current
3. FETs are widely applicable in oscilloscopes and voltmeters as an input amplifier as compared to bipolar transistors due to _____.
- a. ability of minimizing the loading effect with high input resistance
 - b. ability of maximizing the loading effect with high input resistance
 - c. ability of minimizing the loading effect with low input resistance
 - d. ability of maximizing the loading effect with low input resistance

10.b.6. Post Lab Questions

1. How does the FET operate before the pinch-off region with small value of drain-to-source voltage in accordance to the control of drain-to-source resistance by the bias voltage?
2. Compare Depletion and Enhancement MOSFET.
3. The transient time of the current carriers through the channel of the FET decides its _____ characteristics.
4. A D-MOSFET is considered to be a
 - a. Normally off device
 - b. Normally on device
 - c. Current controlled device
 - d. High-power switch

11.a CHARACTERISTICS OF PHOTOCONDUCTIVE CELL, LIGHT EMITTING DIODE

11.a.1 Objective

- To study and verify the characteristics of
- (i) Photoconductive cell (LDR),
 - (ii) Light Emitting Diode (LED).

11.a.2 Hardware Required

S. No	Apparatus	Type	Range	Quantity
1	Resistors		1KΩ, 330Ω	1
2	Regulated power supply		(0-30V), 2A Rating (0-5V)	1
3	LDR			1
4	LED		Red, Green, Yellow	
5	Ammeter	MC	(0-30)mA;(0-100)mA	1
6	Voltmeter	MC	(0-10)V	1
7	Bread board and connecting			1
	Wires			Few

11.a.3 Introduction

11.a.3.1 Photoconductive Cell (LDR)

Photoconductive cells are light-sensitive resistors in which resistance decreases with an increase in light intensity when illuminated. These devices consist of a thin single-crystal or polycrystalline film of compound semiconductor substances. Most commercially available photoconductive cells are manufactured from cadmium sulfide (CdS), which is sensitive to light in the visible spectrum. Other materials that are less commonly used in photoconductive cells include lead sulfide (PbS), lead selenide (PbSe), and lead telluride (PbTe), although they react to infrared light, not the visible spectrum.

CdS photoconductive cells (CdS cells) are often referred to as light dependant resistors (LDR). They function within the same general spectral range as the human eye, and are therefore

widely used in applications where this type of spectral response is required.

When light of suitable frequency falls on the device, the photogeneration of charge carriers reduces the resistance of the device and this property of LDR can be used to control the current flow in a circuit.

11.a.3.2 Light Emitting Diode

A Light emitting diode is essentially a pn junction diode typically made from a direct bandgap semiconductor such as GaAs in which the electron hole pair formation result in the emission of photon. The emitted photon energy is approximately equal to the band gap energy.

In LED, the n side is more heavily doped compared to the p side and a forward bias result in heavy injection of electrons to the p side which are minority carriers on this side. The recombination of injected electrons in the depletion as well as in the neutral p side result in the spontaneous emission of photons. The phenomenon of light emission from EHP recombination as a result of minority carrier injection is called injection electroluminescence.

The photon energy determines the wavelength of the emitted light, and hence its color. Different semiconductor materials with different bandgaps produce different colors of light. The main semiconductor materials used to manufacture LEDs are Indium gallium nitride (InGaN)(blue, green and ultraviolet high-brightness LEDs), Aluminum gallium indium phosphide (AlGaInP-yellow, orange and red high-brightness LEDs) Aluminum gallium arsenide (AlGaAs)-red and infrared LEDs), Gallium phosphide (GaP-yellow and green LEDs) etc.

11.a.4 Circuit diagram:

11.a.4.1 LDR

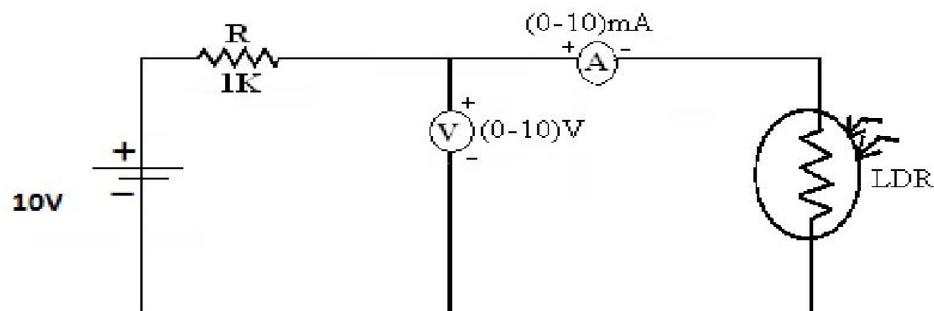


Fig 11a.1 Characteristics of LDR

11.a.4.2 Light Emitting Diode

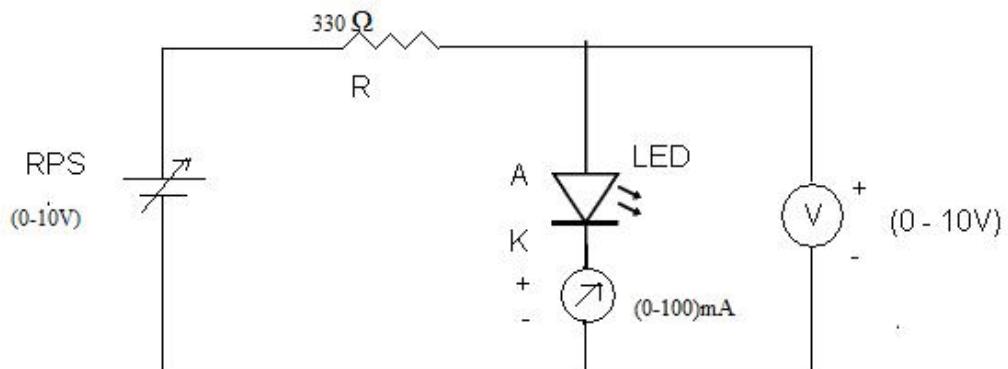


Fig 11a.2 Characteristics of LED

11.a.5 Tabular Column

11.a.5.1 LDR

SI No	Distance (cm)	Voltage (V)	Current (mA)	Resistance(KΩ)

11.a.5.2 LED

Red LED			Yellow LED			Green LED		
SI. No	Voltage(V)	Current(mA)	SI. No	Voltage(V)	Current(mA)	SI. No	Voltage(V)	Current(mA)

11.a.6 Characteristics of LDR, LED

11.a.6.1LDR

- 1.Sensitivity: The sensitivity of LDR varies with the light wavelength.If the wavelength is outside a certain range it will not affect its resistance at all.LDR has a lower light sensitivity compared to photodiodes and phototransistors
- 2.Latency: There is a time latency between changes in illumination and changes in resistance. It usually takes about 10 ms for resistance to drop completely when light is applied after total darkness.
- 3.Photoresistor is a passive component and does not have a PN-junction. The photoresistivity may vary depending on ambient temperature, making them unsuitable for applications requiring precise measurement of sensitivity to light.

11.a.6.2LED

- 1.The actual colour of a light emitting diode is determined by the wavelength of the light emitted, which in turn is determined by the actual semiconductor compound used in forming the PN junction during manufacture.
- 2.The commercially used LED's have a typical voltage drop between 1.5 Volt to 2.5 Volt or current between 10 to 50 milliamperes. An illumination-grade LED containing a single semiconducting element requires the same voltage, but operating currents are much higher, typically several hundred milliamperes.

3.LEDs require a specific electrical polarity. Applying voltage in reverse polarity can destroy them. 5 volts is a typical maximum reverse voltage rating.

4.The forward resistance of the device is very low. Hence LED is always connected with an external series current limiting resistor. Series resistance is determined by the following equation,

11.a.7Precautions

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

11.a.8Procedure

11.a.8.1 LDR

1. Connect circuit as shown in figure 11.a.a.4.1.
2. Keep light source at a distance and switch it ON, so that it falls on the LDR
3. Note down current and voltage in ammeter and voltmeter.
4. Vary the distance of the light source and note the V & I.
5. Sketch graph between R as calculated from observed V and I and distance of light source

11.a.8.2 LED

1. Give the connection as per the figure 11.a.a.4.2.
2. Vary the input voltages at the RPS and note down the corresponding current for the voltages.
3. Repeat the procedure for reverse bias condition and tabulate the corresponding voltages and currents.
4. Plot the graph between voltage and current for forward bias and reverse bias.

11.a.9 Model Graph

LDR

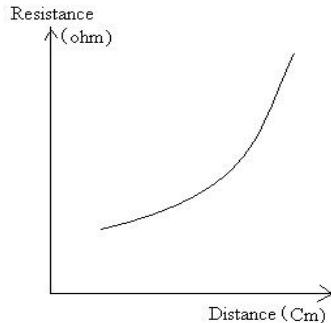


Fig 11a.3 Characteristics of LDR

LED

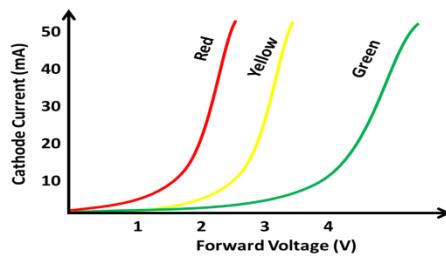


Fig 11a.4 V-I Characteristics of LED

11.a.10 Result

Thus the characteristics of LDR and LED are studied and verified.

11.a.11 Prelab Questions

1. List a few applications of LDR.
2. Give the properties of the materials used for LDR.
3. List a few limitations of LDR.
4. Define the active region in an LED.
5. Give the energy band diagram of an LED.

11.a.12 Post lab Questions

1. Draw the V-I characteristics of LDR as a function of light intensity.
2. Explain why silicon cannot be used to manufacture LED.
3. Give suitable materials for blue LED and compare their efficiencies.
4. Calculate the wavelength of light emitted by a GaAs LE

11.b CHARACTERISTICS OF SOLAR CELL

11b.1 Objective

To study the characteristics of a silicon photovoltaic cell in dark and under illuminance.

11b.2 Hardware Required

Sr. No.	Unit	Description/Rating	Qty
1	Solar Cell	Si cell	1
2	Light Source: Halogen Lamps Black cloth	50W ,230V	2
3	3-1/2 digit Voltmeter	0 to 1.999 V	1
4	Potentiometers	0-10 Ω single turn, 0-100 Ω 10 turn	2
5	3-1/2 digit Ammeter	0 to 1999 mA	1
6	4 Quadrant Supply	0 to +/-10 V, 0 to +/-1 A	1

11b.3 Introduction

A solar cell (or a "photovoltaic" cell) is a device that converts photons from the sun (solar light) into electricity. The conversion involves the photogeneration of charge carriers (electrons and holes) in a light-absorbing material, and separation of the charge carriers to a conductive contact that result in the flow of these photo generated charge carriers through an external load.

The photovoltaic cell has a p-n structure with a narrow n region through which light enters the device. Mostly the photons that are absorbed close to the depletion region result in photogenerated carriers that are separated by the barrier potential across the pn junction and constitute current in the external circuit.

The solar cell efficiency refers to the fraction of incident light energy converted to electrical energy. For a given solar spectrum, this efficiency depends on the semiconductor material properties and device structure. Most solar cells are silicon based and the efficiency

ranges from about 18% for polycrystalline to 22-24% in high efficiency single crystal devices. Under illumination the curve is shifted such that the curve lies in quadrants I, III and IV. where, I_{ph} is the light induced current and depends on the intensity of illumination.

11.b.4 Characteristics of Solar cell

Open circuit voltage: It is measured by measuring voltage across the terminals of the cell when no load is connected to the cell. Normally open circuit voltage of solar cell nearly equal to 0.5 to 0.6 volt. It is normally denoted by V_{oc} .

Short circuit current: The maximum current that a solar cell can deliver without harming its own constriction. It is measured by short circuiting the terminals of the cell at most optimized condition of the cell for producing maximum output. It is normally denoted as I_{sc} .

Maximum Power point: The maximum current that a solar cell can deliver without harming its own constriction. It is measured by short circuiting the terminals of the cell at most optimized condition of the cell for producing maximum output.

Fill factor: The ratio between product of current and voltage at maximum power point to the product of short circuit current and open circuit voltage of the solar cell.

$$Fill\ Factor = \frac{P_m}{I_{sc} \times V_{oc}}$$

Efficiency: It is defined as the ratio of maximum electrical power output to the radiation power input to the cell and it is expressed in percentage.

11b.5 Precautions

4. While doing the experiment do not exceed the ratings of the device. This may lead to damage the device.
5. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
6. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
7. Photovoltaic (PV) modules generate electricity when exposed to light, even when they are not connected in a circuit. Shocks and burns can result from contacts with output wiring

- and module itself.
8. Cover PV module front surfaces completely with an opaque cloth or other opaque material before performing any operation involving the module or electrical connections. Use appropriate safety equipment (insulated tools, insulating gloves, etc.) and procedures.

11b.6 Circuit diagram

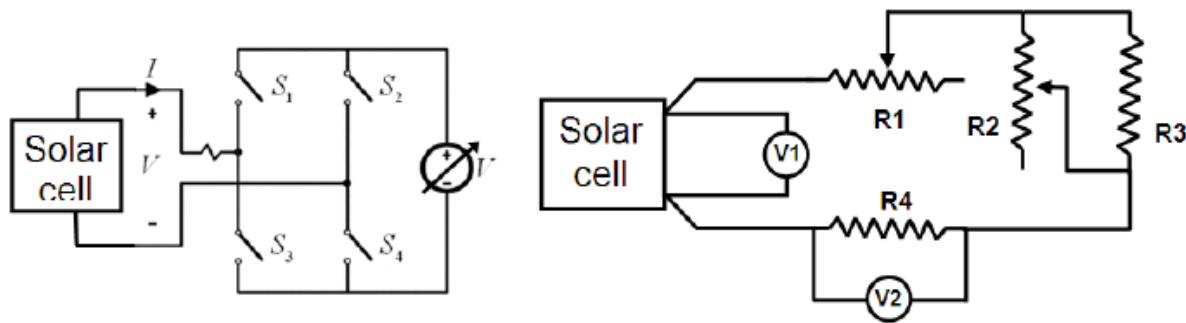


Fig 11b.1. 4 Quadrant power supply schematic with solar cell connected as load, Figure 11b.2 Solar cell as a source of power with a variable load resistor R.

11b.7 Procedure

The solar simulator housing has two cells. In order to use a single cell, connections have to be made as shown.

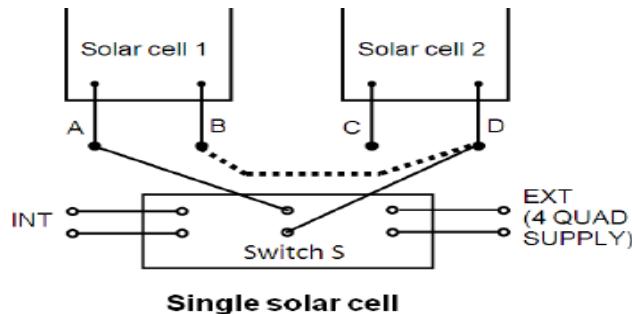


Fig 11b.3 Solar simulator housing connections

This allows to measure the solar cell kept on the left in the housing.

11b.7.1 Measurement using 4 quadrant power supply with solar cell as load

- i) To connect cell to 4-quadrant power supply, keep DPDT switch S in the EXT position.

- ii) Connect the power supply to the leads of the solar cell , brought out on right side of the lamp/ solar cell housing.
 - iii) Cover the solar cells with black cloth for measuring I-V in the dark. Keep the lamps off and shut the door in front of the housing.
 - iv) Measure I-V by gradually turning the bias voltage knob located on the left side of the 4 quadrant supply (the right side knob should be kept in the extreme clockwise position and should not be moved during the experiment).
- The applied bias voltage (in volts) is read on the meter on the left. The meter on the right measures the current in amperes. Measure I-V over bias voltage from -0.7 V to +0.7 V.
- v) Remove the black cloth and take it out of the box. turn on the fan. turn on the two lamp switches l1 and l2.
 - vi) Adjust the bias voltage knob on the 4 quad supply till the current shows zero reading. With this adjustment, the voltmeter reads open circuit voltage V_{oc} . Wait until the reading becomes stable (V_{oc} reading will decrease initially because of rise of cell temperature due to heat from the lamps).

When reading becomes stable, measure I-V characteristics by gradually varying the biasvoltage from -0.7 V to + 0.7 V.

- vii) Turn off the lamps and turn the bias voltage knob till the voltage is zero.

11b.7.2 Measurement using solar cell as power source under illumination

For this measurement, meters on the simulator panel will be used. Change the position the DPDT switch S to INT.

- i) There are two potentiometers. Turn them both clockwise so that resistance is maximum.
- ii) Turn on the fan. Turn on the two lamp switches L1 and L2.
- iii) See the reading on temperature indicator. Wait (a few minutes) till the temperature reading stabilizes.
- iv) Note the readings on current meter and voltmeter. This condition is close to the open circuit condition; voltage will be high and current low.
- v) Reduce resistance by turning 0-100 ohm potentiometer anticlockwise. This is a 10-turn

potentiometer. Take readings of V and I as R is varied.

vi) After the 100 ohm pot reaches the minimum setting (fully anticlockwise), turn 0 – 10 ohm potentiometer gradually anticlockwise and record I-V readings.

vii) 10 ohm pot is single turn. Once it reaches the minimum setting, current will be the highest and voltage is the minimum. This condition is close to short circuit.

After reaching the minimum of the two pots and recording the readings, set the 10 ohm pot to maximum (fully clockwise). Then set the 100 ohm pot also to the maximum (fully clockwise). Check the voltmeter reading. If it is the same as noted in the beginning of the measurement, this checks that the temperature did not change during the above measurements.

11b.8 Result

The characteristics of a silicon solar cell has been studied in dark and under illuminated conditions.

11b.9 Pre- Lab Questions

1. How does a photovoltaic cell differs from a photo detector?
2. Compare the efficiency of amorphous and crystalline Si cells.
3. Define open circuit voltage of a solar cell.
4. Define fill factor.

11b.10 Post Lab Questions

1. Draw the VI characteristics of a solar cell as a function of light intensity.
2. Why a 4 Quadrant power supply is required to measure the characteristics under illumination?
3. Why is it required that in a solar cell most of the photon absorption should take place close to the depletion region?

