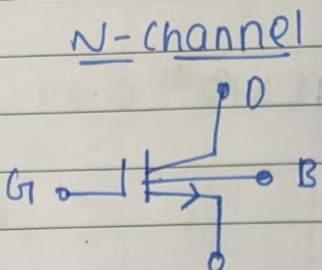
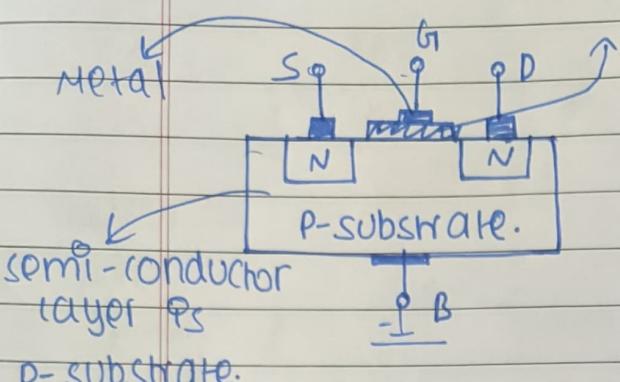
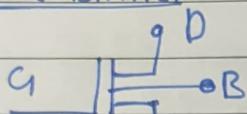


## Unit - II

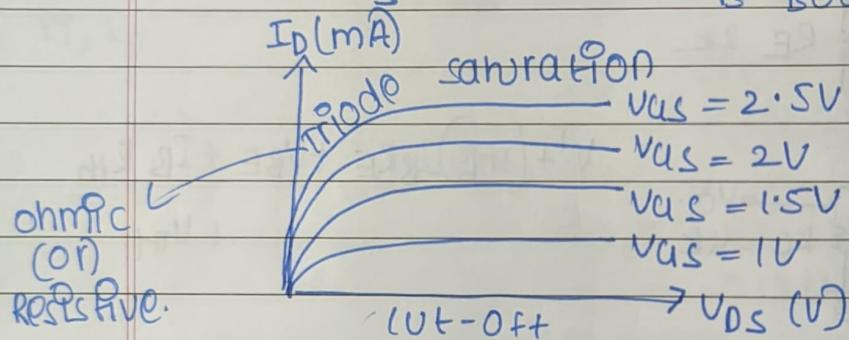
② FET Amplifiers - Enhancement only  
 Si-O<sub>2</sub> layer - Oxide layer



P-channel:



S - Source region  
 D - Drain region.  
 G - Gate  
 B - Body / Bulk.



CUT-OFF Region:

$$i_D = 0.$$

Triode Region:  $\rightarrow$  No need for derivation.

$$i_D = k_n (2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2) \quad \text{for } V_{DS} < V_{GS} - V_{TH}$$

$$k_n = \frac{W H_n C_{Ox}}{2L}$$

Saturation

$$i_D = k_n (V_{GS} - V_{TH})^2 \quad \text{for } V_{DS} \geq V_{GS} - V_{TH}$$

layer

BJT

- 1 Bipolar
- 2 Current controlled device.
- 3 More noisy (Due to Random movement of electrons)
- + only MOSFET will be analysed in this unit.

LOW FREQ

FET → MOSFET

1 Unipolar

2 MOSFET

occupies less

space than BJT for

doing the same

operation.

3 Voltage controlled device application

HIGH FREQ  
used for

4 less noisy.

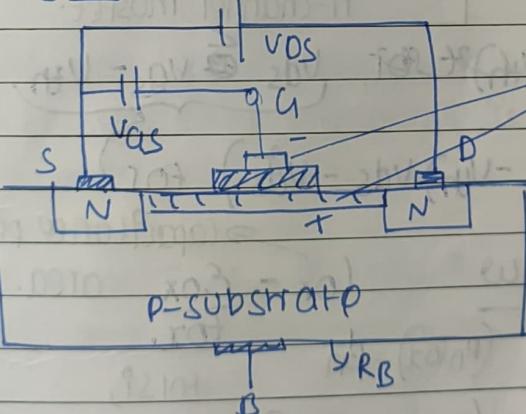
5 I<sub>D</sub>P Imp is more.MOSFET

Depletion type

↓ Normally on

Enhancement Type:

↓ Normally off



when  $V_{GS}$  is supplied  
capacitance effect takes  
place.

→ Enhancement  
MOSFET.

when  $V_{GS}$  is not  
given.

Since no current flows through  $N$  &  $N$  (S) (D)  $q_t$   $p_s$

normally off.

acts like a capacitor with  
dielectric in between

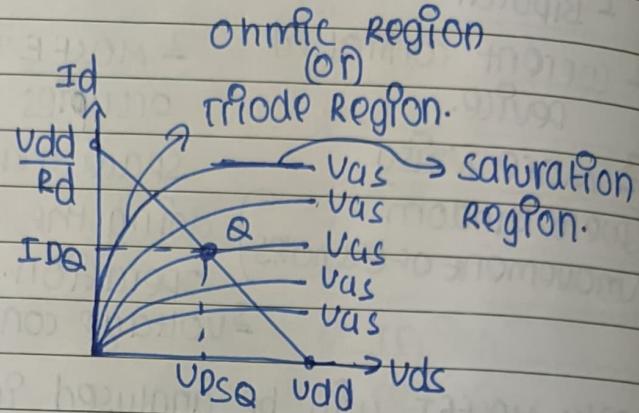
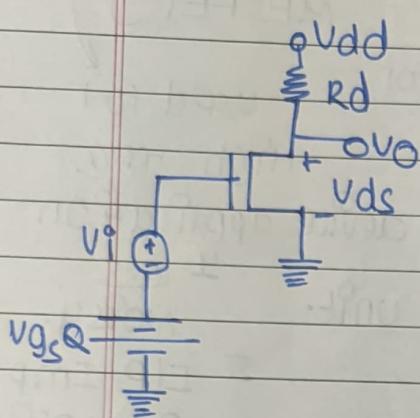
Due to capacitive effect, there will be an  
~~N~~ type layer formed in between S and D  
which with on the MOSFET

-  $V_{TH}$

### V<sub>threshold</sub>:

It is a part of  $V_{GS}$  -

Where channel exist and current starts flowing.



$$(UT\text{OFF} \Rightarrow V_{DS} = V_{DD})$$

In saturation region,  $\rightarrow$  used for derivations

$$[I_D = k_n (V_{GS} - V_{TH})^2] \text{ for } V_{DS} \geq (V_{GS} - V_{TH}) \xrightarrow{V_{DS}(\text{sat})}$$

In triode region,  $[k_n \rightarrow \text{conduction parameter for } n\text{-channel mosfet.}]$

$$I_D = k_n (2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2) \text{ for } V_{DS} \leq V_{GS} - V_{TH}$$

$$I_D = k_n (2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2) \text{ for } \xrightarrow{\text{capacitance per unit area.}}$$

$$k_n = \frac{H_n (C_{ox} W)}{2L} \quad (H_n = \frac{C_{ox}}{t_{ox}}) \quad \text{for } S_i,$$

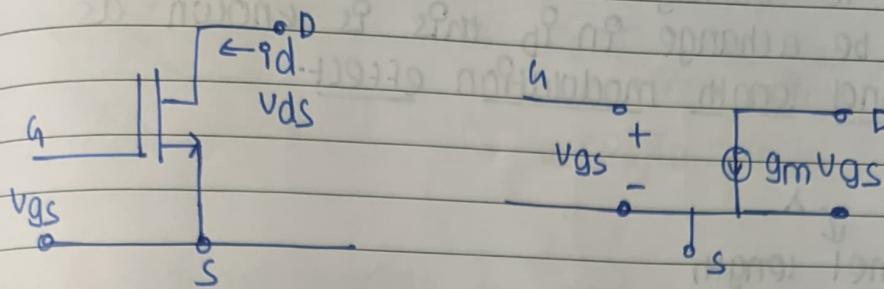
$$g_m = \frac{I_D}{V_{GS}} = 2k_n (V_{GS} - V_{TH}) \quad C_{ox} = (3.9)(8.85 \times 10^{-14}) \text{ F/cm}^2$$

From saturated current expression,

$$(V_{GS} - V_{TH})^2 = I_{DS}/k_n$$

$$V_{GS} - V_{TH} = \sqrt{I_{DS}/k_n}$$

$$g_m = 2k_n \sqrt{\frac{I_{DS}}{k_n}} = 2 \sqrt{k_n I_{DS}}$$

small-signal Equivalent Circuit:

with channel length modulation effect

$$i_D = k_n \left[ (v_{gs} - v_{th})^2 + (1 + \lambda v_{ds}) \right]$$

$$r_0 = \left( \frac{\partial i_D}{\partial v_{ds}} \right)^{-1}$$

$$\therefore r_0 = \underbrace{(\lambda k_n (v_{gs} - v_{th})^2)}_{I_{DQ}}^{-1} = (\lambda I_{DQ})^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}}$$

\* ~~no~~ voltage at which sufficient amount of  $v_{gs}$  is given and the n-channel is formed. It is called  $V_{TH}$ .  $\rightarrow$  (threshold voltage)

\* If the voltage  $v_{GS}$  is ( $-$ ) it will form a p-channel (PMOS). and ( $+v_{GS}$ ) forms an N-MOS.

\* From the loop Qin circuit (on left page).

$$V_{dd} = i_D R_d + U_{ds}$$

At cutoff pt,  $i_D = 0$

$$U_{ds} = V_{dd}$$

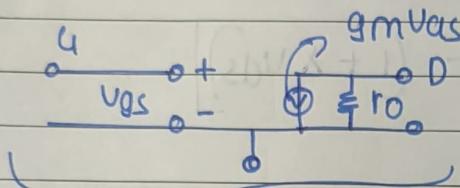
At saturation,  $U_{ds} = 0$

$$i_D = \frac{V_{dd}}{R_d}$$

$R_d$  is analogous to  $R_C$  in BJT.

\* Due to varying of the n-channel region there will be a change in  $I_D$  this is known as channel length modulation effect.

$\lambda$   
channel length  
modulation  
factor



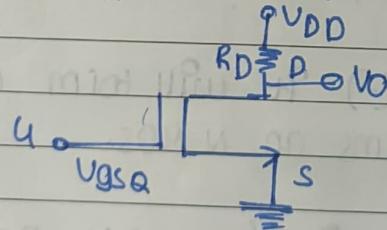
Improvised  
circuit after derivation.

\* Need to find  $r_o$  and  $g_m$  for numericals.

Q) Find the load line and Q-point for a mosfet circuit having  $V_{GSQ} = 2.12V$ ,  $V_{DD} = 5V$ ,  $R_D = 2.5k\Omega$

$$V_{TN} = 1V, k_n = 0.80 \text{ mA/V}^2$$

Ans



$$\bullet V_{DD} = I_D R_D + V_{DS}$$

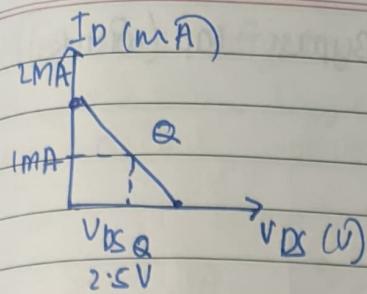
$$\bullet I_D = k_n (V_{GSQ} - V_{TN})^2$$

$$I_D = 0.80 (2.12 - 1)^2$$

$$I_D = 1 \text{ mA}$$

$$V_{DS} = V_{DD} - I_{DQ} R_D = 5 - (1 \times 2.5)$$

$$V_{DSQ} = 2.5 \text{ V}$$



$$V_{DDR} = R_D R_D +$$

at -OFF point,

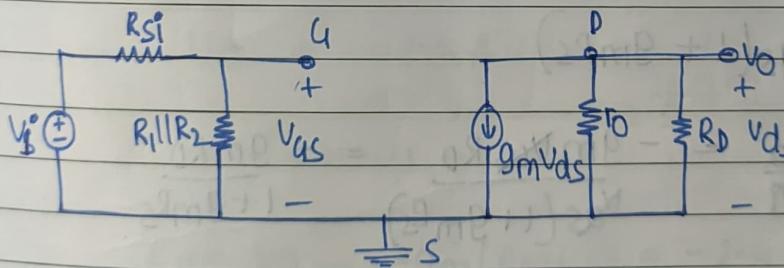
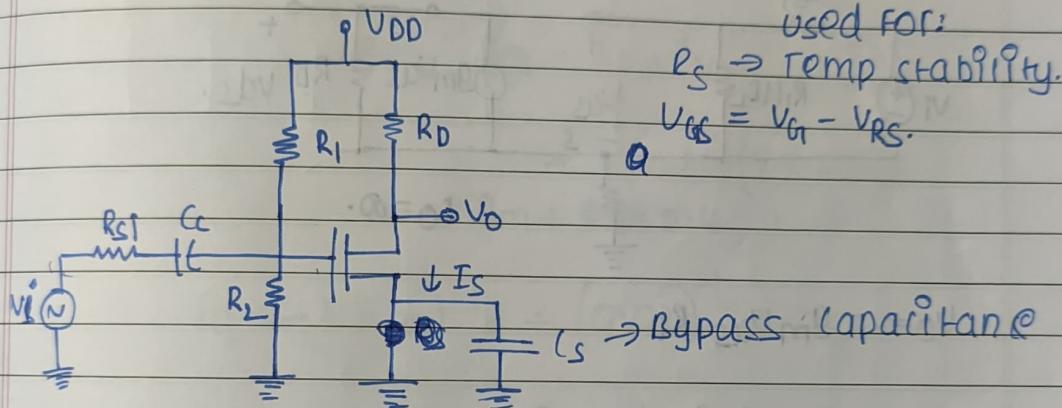
$$I_D = 0 \quad V_{DS} = V_{DD}$$

at saturation point,

$$V_{DS} = 0, I_D = V_{DD}/R_D = 5/2.5 = 2 \text{ mA.}$$

- \* IN p-channel mosfet  $k_p$  and  $V_{TP}$  will be given.

common-source Amplifier: (with bypass capacitance)



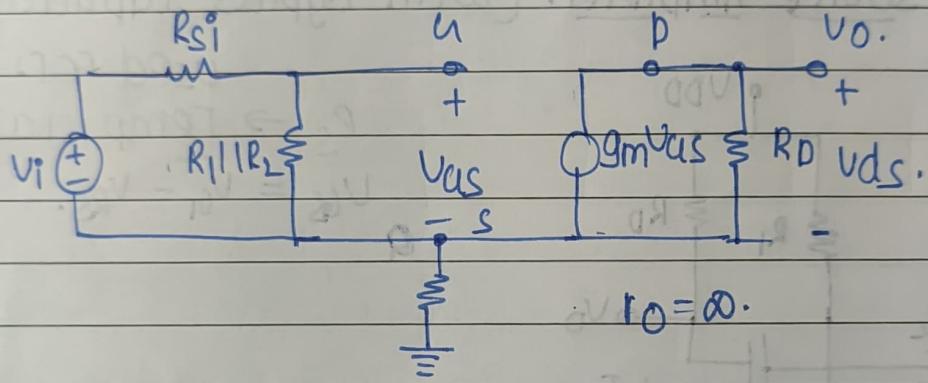
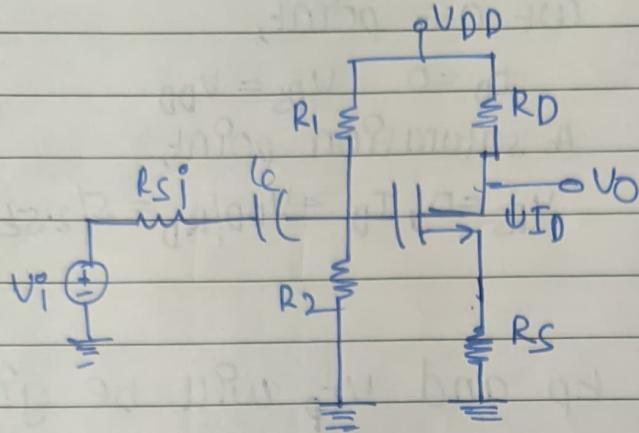
$$V_o = -g_m V_{GS} (r_{o1} || R_D) \quad V_{GS} = V_P \frac{R_1 || R_2}{(R_1 || R_2) + R_{SI}} \quad \boxed{\text{Voltage Divider Rule}}$$

$$A_V = \frac{V_o}{V_P} = -g_m (r_{o1} || R_D) \left( \frac{R_1 || R_2}{R_{SI} + R_1 || R_2} \right) \quad \boxed{[180^\circ \text{ phase shift } P_S \text{ produced}}$$

- \* Question can be asked both with or without bypass capacitance.

Notes

# common-source Amp (with out Bypass (ap (with $R_S$ ))



$$V_o = -g_m V_{dgs} R_D$$

$$V_g = V_{dgs} + g_m V_{dgs} \cdot R_S$$

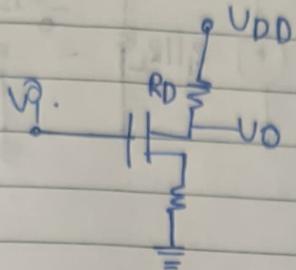
$$V_g = V_{gs} (1 + g_m R_S)$$

$$A_V = \frac{V_o}{V_g} = -\frac{g_m V_{dgs} R_D}{V_{dgs} (1 + g_m R_S)} = -\frac{g_m R_D}{1 + g_m R_S}$$

If  $g_m R_S \gg 1$

$$\text{Then, } A_V = -\frac{R_D}{R_S}$$

Q) Find small signal voltage gain of a mosfet amplifier  
 $V_{GSQ} = 2.12V$ ,  $U_{DD} = 5V$ ,  $R_D = 2.5k\Omega$ ,  $U_{Th} = 1V$ ,  $k_n = 0.80 \text{ mA/V}^2$   
 $\lambda = 0.02 \text{ V}^{-1}$ , operates in saturation.



$$I_{DQ} = 1 \text{ mA} \quad U_{DSQ} = 2.5V$$

$$g_m = 2k_n(U_{GSQ} - U_{Th})$$

$$= 2(0.80)(2.5 - 1)$$

$$g_m = 0.20 \text{ A/V}$$

$$r_o = (\lambda I_{DQ})^{-1} = (0.02)^{-1} = 50k\Omega$$

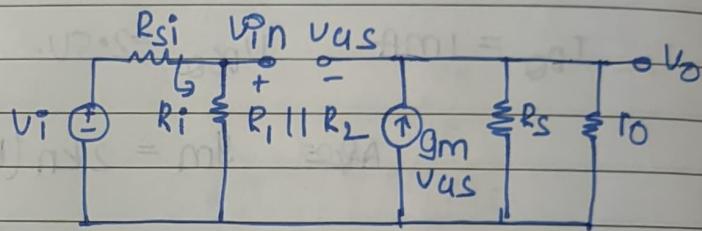
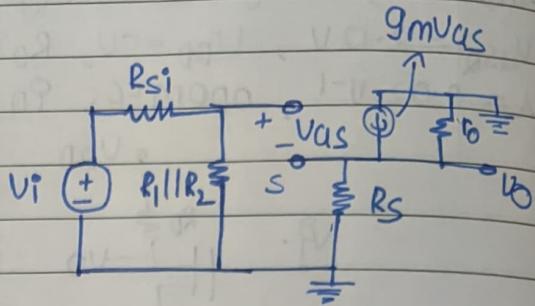
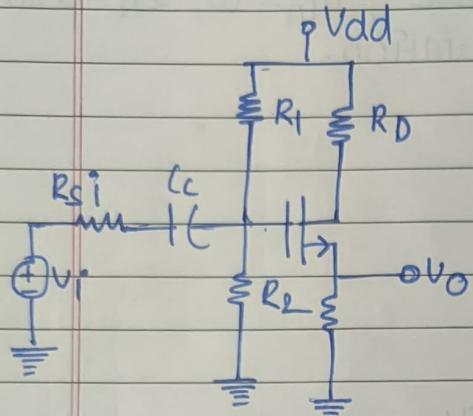
$$V_O = -g_m U_{GS} (R_D || r_o)$$

$$V_O = -2.4 \times 2.12 \times \frac{1}{2.5 + \frac{1}{50}}$$

$$V_O = 12.11$$

$$AV = \frac{V_O}{U_{GS}} = -g_m (R_D || r_o) = -2.4 \times \frac{1}{2.5 + \frac{1}{50}}$$

$$AV = -5.714$$

SOURCE FOLLOWER:

$$V_O = g_m V_{AS} (r_o \parallel R_S)$$

$$\begin{aligned} V_{IN} &= V_{AS} + V_O \\ &= V_{AS} + g_m V_{AS} (r_o \parallel R_S) \end{aligned}$$

$$\therefore V_{AS} = \frac{V_{IN}}{1 + g_m (r_o \parallel R_S)}$$

$$V_{IN} = V_I \cdot \frac{R_i}{R_i + R_{SI}} \quad \therefore R_i = R_1 \parallel R_2$$

$$A_V = \frac{V_O}{V_I} = \frac{g_m V_{AS} (r_o \parallel R_S)}{(R_i + R_{SI}) V_{IN}} \cdot R_i$$

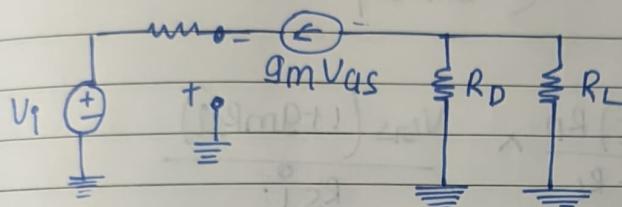
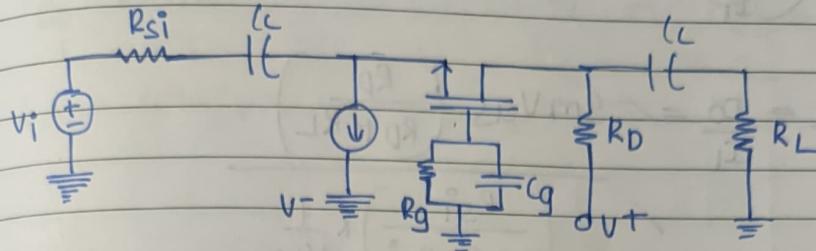
$$g_m (r_o \parallel R_S) \gg 1$$

$$R_{SI} \ll R_i$$

~~$$A_V = \frac{g_m (r_o \parallel R_S)}{(R_i + R_{SI}) \cdot g_m (R_S \parallel r_o)} \cdot \frac{R_i}{R_{SI}}$$~~

$$A_V = \frac{g_m (R_S \parallel r_o)}{g_m (R_S \parallel r_o)} \cdot \frac{R_i}{R_{SI}} \approx 1$$

(common gate):



$$V_D = -g_m V_{AS} \cdot (R_D \parallel R_L)$$

(characteristics)

$$R_i^o = \infty$$

$$R_o^i \uparrow$$

$$A_V = \text{high}$$

$$A_I \approx 1$$

$$\text{Phase Diff} = 0^\circ$$

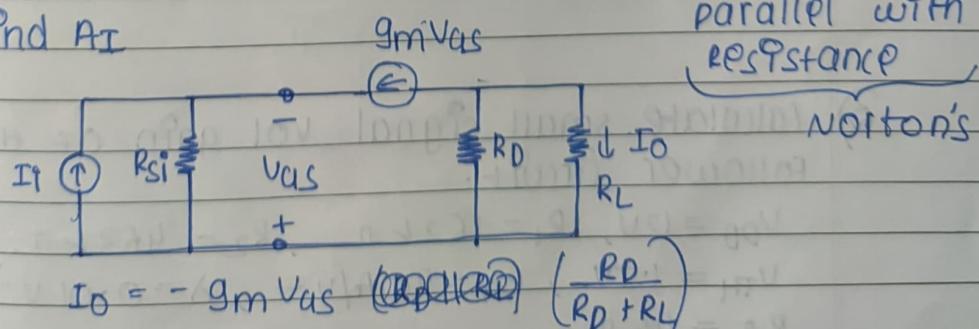
$$V_i = I_i R_{Si} - V_{AS}$$

$$I_i = -g_m V_{AS}$$

$$V_{AS} = \frac{-V_i}{1 + g_m R_{Si}}$$

$$A_V = \frac{V_o}{V_i} = \frac{g_m (R_D \parallel R_L)}{1 + g_m R_{Si}}$$

using norton's equivalent circuit:

To find  $A_I$ 

$$I_o = -g_m V_{AS} \left( \frac{R_D}{R_D + R_L} \right) \left( \frac{R_D}{R_D + R_L} \right)$$

$$\text{At I/P, } I_i + g_m V_{AS} + V_{AS}/R_{Si} = 0$$

$$V_{AS} = -I_i \left( \frac{R_{Si}}{1 + g_m R_{Si}} \right)$$

$$A_I = \frac{I_o}{I_i} =$$

$$A_I = \frac{I_O}{I_I} = g_m V_{AS} (R_D + R_L)$$

$$A_I = \frac{I_O}{I_I} = g_m V_{AS} \left( \frac{R_D}{R_D + R_L} \right) \times \left( \frac{R_S i}{1 + g_m R_S i} \right) \times \frac{1}{V_{AS}}$$

$$A_I = \frac{(g_m V_{AS}) R_D}{R_D + R_L} \times \frac{V_{AS} (1 + g_m R_S i)}{R_S i}$$

$$A_I = \left( \frac{R_D}{R_D + R_L} \right) \left( \frac{g_m R_S i}{1 + g_m R_S i} \right) \approx 1$$

$$= \frac{1}{g_m} \approx 1$$

I/P Imp:

$$R_I^o = -V_{AS}/I_I \quad I_I = -g_m V_{AS}$$

O/P Imp:

$$R_O = R_D$$

Q) calculate small signal vol gain of the source follower circuit.

$$V_{DD} = 12V, R_1 = 162k\Omega, R_2 = 463k\Omega, R_S = 0.7k\Omega$$

$$V_{TH} = 1.5V, k_n = 4mA/V^2, \lambda = 0.01 V^{-1}$$

$$R_S^o = 4k\Omega$$

Ans:

Q) For common gate amp determine o/p  $V_{OL}$   $q_f$

$$I_{DQ} = 0 \text{ mA} \quad V^+ = 5V \quad V^- = -5V \quad R_D = 4k\Omega$$

$$R_L = 10k\Omega, V_{TH} = 1V, R_A = 100k\Omega$$

$$k_n = 1 \text{ mA/V}^2, \lambda = 0, R_S = 50k\Omega \quad I_Q = 100 \sin \omega t \text{ mA}$$

mpli.

so

(21/1/2)

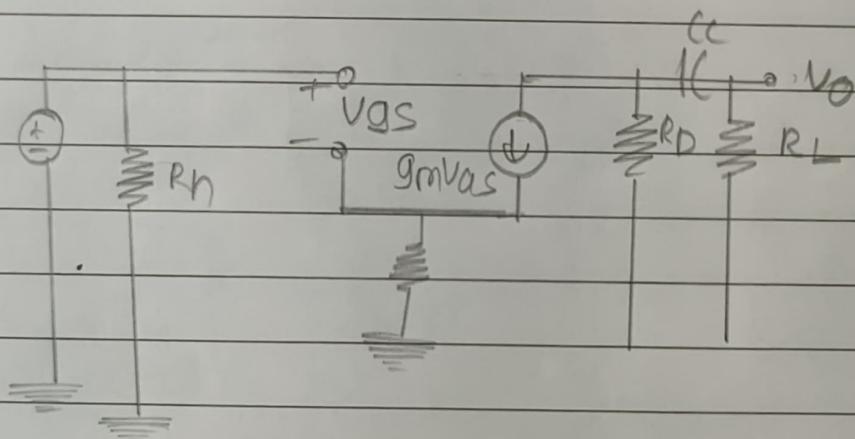
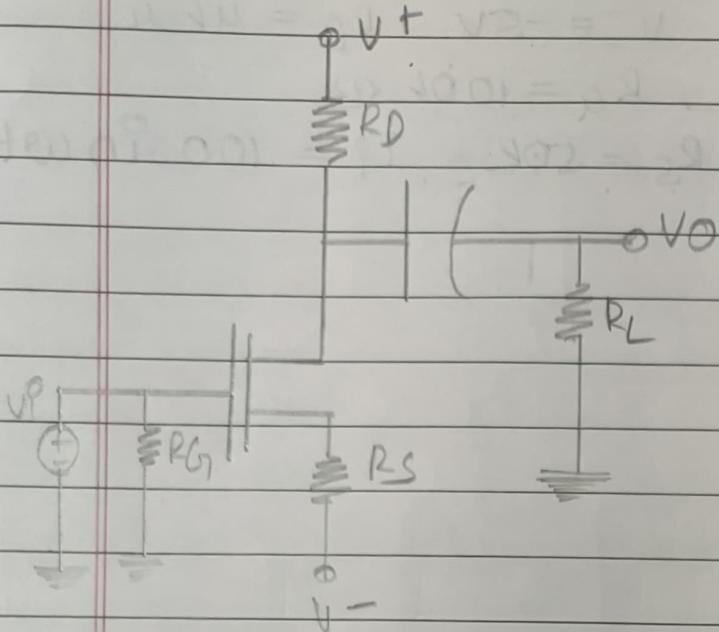
$$20V \text{ mB} + 20V = 40V$$

$$(21/1/2) \text{ mB} = n \text{ mA}$$

$$20 \text{ mB} + 1$$

$$1 + 20 \cdot 2 \cdot (21/1/2) = 23$$

## Frequency Response of CS amp:



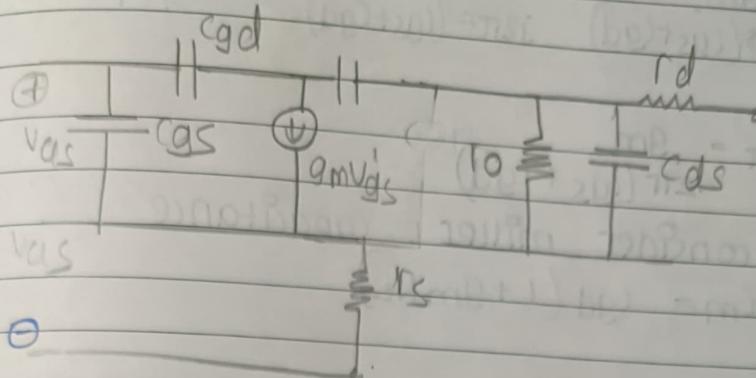
$$|V_O|_{\max} = g_m V_{GS} (R_D \parallel R_L)$$

$$V_i = V_{GS} + g_m V_{GS} R_S$$

$$|A_V|_{\max} = \frac{g_m (R_D \parallel R_L)}{1 + g_m R_S}$$

$$\tau_s = (R_D + R_L) C_C \quad f_L = \frac{1}{2\pi \tau_s}$$

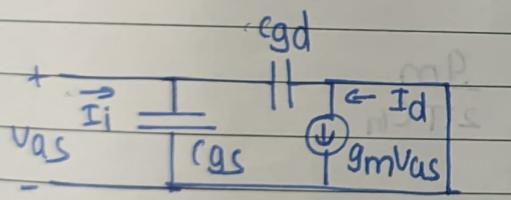
$$\tau_D = (R_D + R_L) C_C$$

High Frequency Response:-

$$I_D = g_m V_{GS}$$

$$V_{DS} = V_{GS}' + (g_m V_{GS}) R_S = (1 + g_m R_S) V_{GS}'$$

$$I_D = \left( \frac{g_m}{1 + g_m R_S} \right) V_{GS} = g_m' V_{GS}$$

short circuit current gain:At I/P node,  $\text{V}_{GS}$ 

$$I_O = \frac{V_{GS}}{\frac{1}{j\omega C_{GS}}} + \frac{V_{DS}}{\frac{1}{j\omega C_{GD}}}$$

$$I_O = V_{GS} \left( j\omega (C_{GS} + C_{GD}) \right)$$

O/P node  $\Rightarrow \text{V}_{DS}$ ,

$$\frac{V_{GS}}{j\omega C_{GD}} + I_D = g_m V_{GS}$$

$$I_D = V_{GS} (g_m - j\omega (C_{GS} + C_{GD}))$$

$$I_O = I_D \frac{(j\omega (C_{GS} + C_{GD}))}{(g_m - j\omega (C_{GS} + C_{GD}))}$$

$$A_I = \frac{I_D}{I_O} = \frac{g_m - j\omega (C_{GD})}{j\omega (C_{GS} + C_{GD})} \quad \omega (C_{GD}) \ll g_m$$

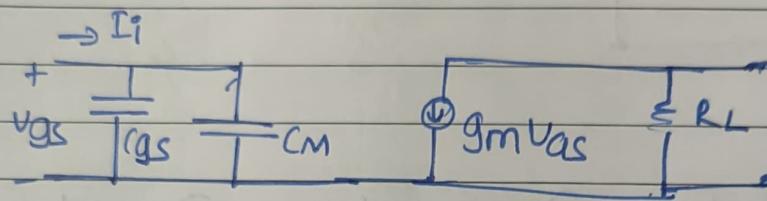
$$\therefore A_I = \frac{g_m}{j\omega(g_s + g_d)} = \frac{g_m}{j2\pi f(g_s + g_d)} = \frac{1}{jf/FT}$$

where,

$$f_T = \frac{g_m}{2\pi(g_s + g_d)}$$

If we consider Miller capacitance

$$C_m = g_d(1 + g_m R_L)$$



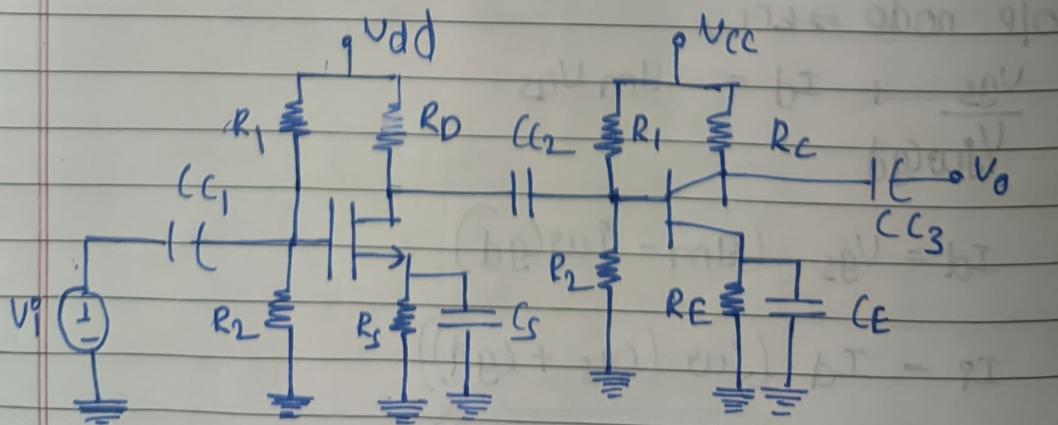
$$I_d = j\omega(g_s + C_m) V_{gs}$$

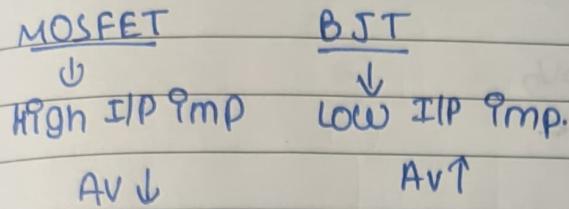
$$I_A = g_m V_{ias}$$

$$A_I = \frac{I_d}{I_A} = \frac{g_m}{2\pi f(g_s + C_m)} = \frac{1}{jf/FT}$$

$$f_T = \frac{g_m}{2\pi(g_s + C_m)} = \frac{g_m}{2\pi C_m}$$

### BiFET Amp





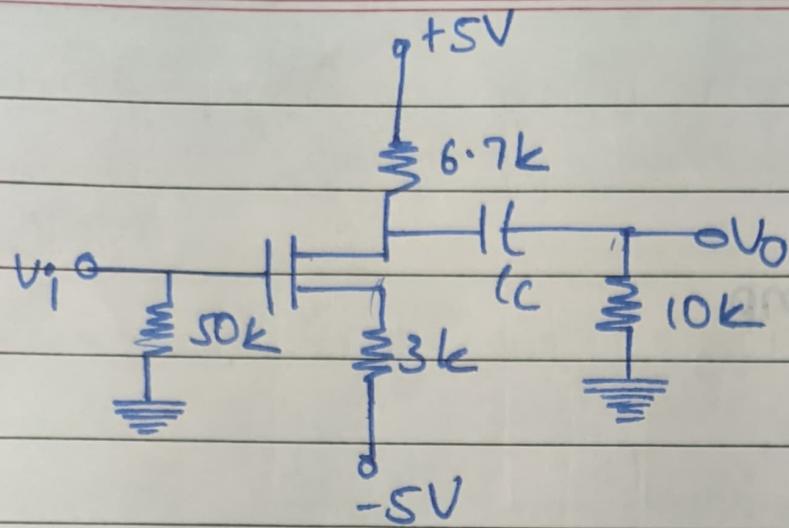
Bifet has ver A<sub>V</sub> than BJT

- \* in order to avoid loading effect an amp should have high I<sub>P</sub> I<sub>mp</sub> impedance.

Reasons for using Bi-FET instead of BJT or FET

- \* BJT occupies more space
- \* very high power consumption
- \* Has more noise.
- \* MOSFET gain is low
- \* MOSFET speed is low
- \* BJT has higher speed.

BiFET combines



Find  $C_C$  if  $f_L = 20\text{kHz}$

$$f_L = \frac{1}{2\pi T_S}$$

$$T_S = (R_D + R_L) C_C$$

$$V_A = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$$

$$V_A = V_{AS} + I_D R_S$$

$$T_d = k_n (V_{GS} -$$