Unit III - MOS Introduction

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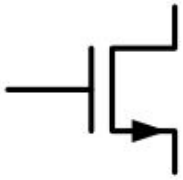
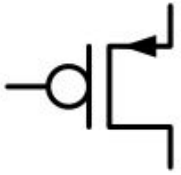
MOS Transistors

- MOS transistors are *extremely* useful devices
  - Almost all of your electronics uses them on the inside
  - Including your phone, laptop, WiFi and Bluetooth, and your Arduino
- Come in two "flavors"
  - nMOS

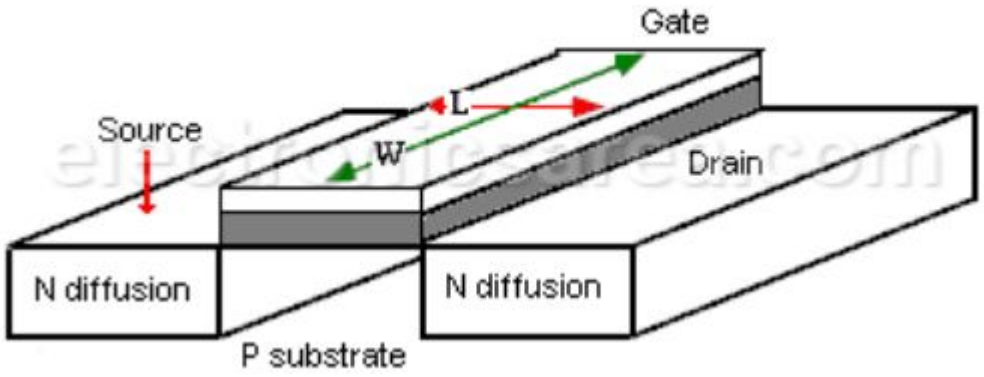


    - It is a switch which connects source to drain
    - If the gate-to-source voltage is greater than V_{th} (around 1 V)
      - Positive gate-to-source voltages turn the device on.
  - pMOS



    - It is a switch which connects source to drain
    - If the gate-to-source voltage is less than V_{th} (around -1 V)
      - Negative gate-to-source voltages turn the device on

MOS Transistor Physical Structure



- The above image shows the **N channel MOSFET transistor** physical structure with its four terminals: Gate, Drain, Source and Substrate. Normally the Source and the substrate are connected together.

- The Gate with W and L dimensions is separated from the substrate by a dielectric (SiO_2), creating a similar structure of the capacitor plates.
- If a **positive voltage is applied to the gate**, **negative charges** are induced (inversion layer) on the substrate surface and they create a **conduction path between the Drain and Source terminals**.
- The minimum voltage needed to create the inversion layer is called **threshold voltage (V_T).** This is a characteristic feature of the transistor.
- If VGS < VT, the drain-source current is zero. Typical values for this voltage are between 0.5 and 3 volts.

Types of MOS Transistors

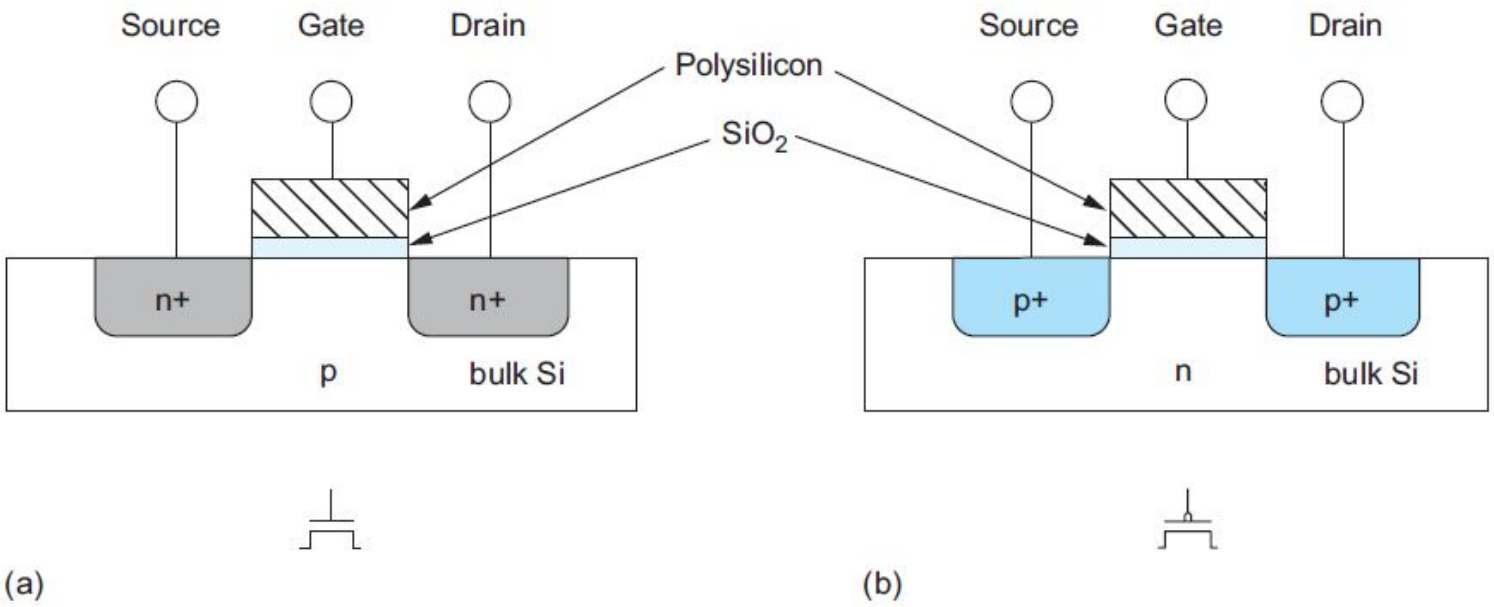


FIGURE : nMOS transistor (a) and pMOS transistor (b)

Types of MOS Transistor

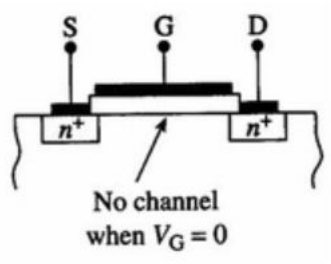
1. **Enhancement mode Transistor -** the **Channel which is NOT existing is Created between Drain and Source** with application of Gate-Source Voltage
   - nMOS Enhancement mode
   - pMOS Enhancement mode

2. **Depletion mode Transistor -** In *depletion mode* the already **existing Channel width between Drain and source is reduced** with application of Gate - Source Voltage
   - nMOS Depletion mode
   - pMOS Depletion mode

Enhancement Mode *vs.* Depletion Mode

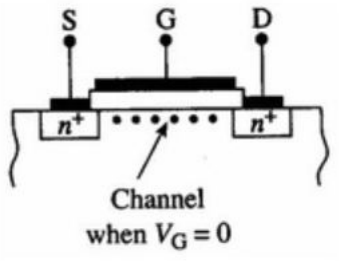
R. F. Pierret, *Semiconductor Device Fundamentals*, Fig. 18.1b

Enhancement Mode



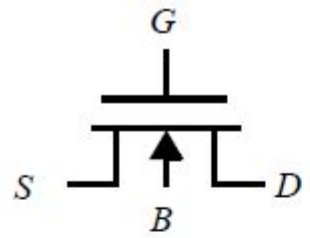
Conduction between source and drain regions is *enhanced* by applying a gate voltage

Depletion Mode

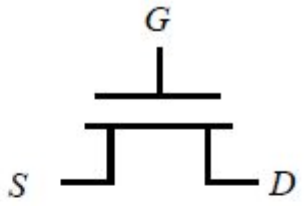


A gate voltage must be applied to *deplete* the channel region in order to turn off the transistor

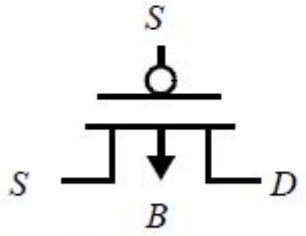
Circuit Symbols for MOS Transistor



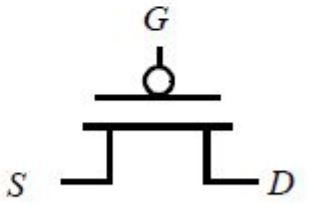
(a) NMOS transistor as 4-terminal device



(b) NMOS transistor as 3-terminal device



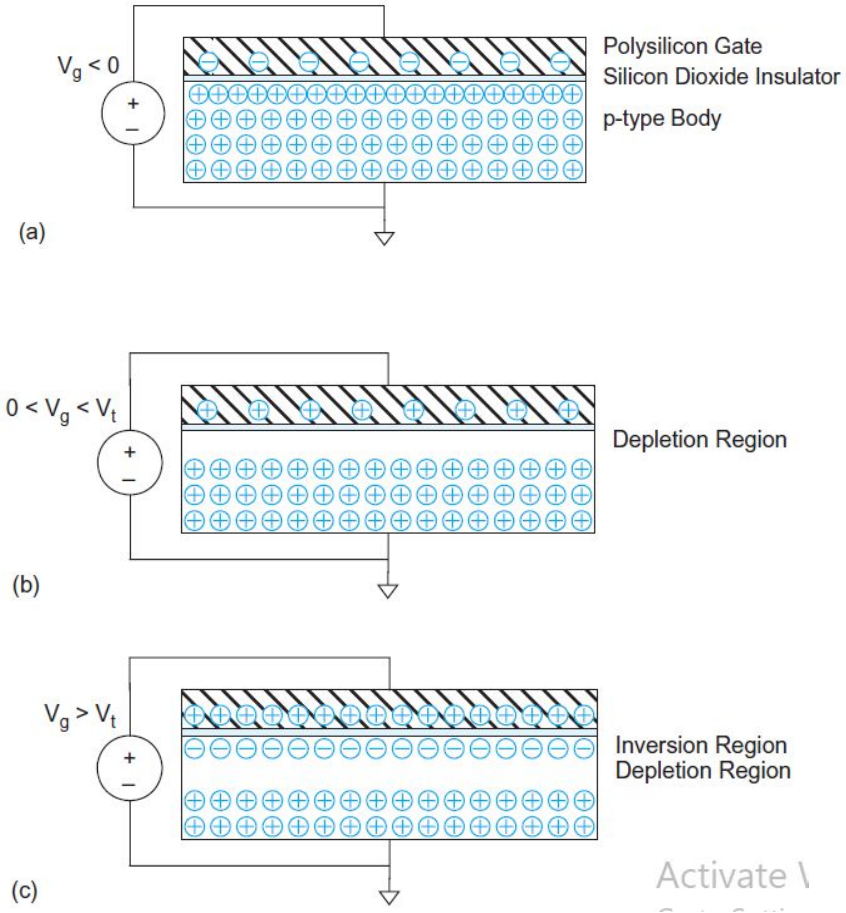
(a) PMOS transistor as 4-terminal device



(d) PMOS transistor as 3-terminal device

If the fourth terminal is not shown, it is assumed that the body is connected to the appropriate supply.

MOS structure demonstrating - Accumulation, Depletion and Inversion



- A negative voltage is applied to the gate, so there is negative charge on the gate.
- The mobile positively charged holes are attracted to the region beneath the gate. This is called **the *accumulation* mode.**

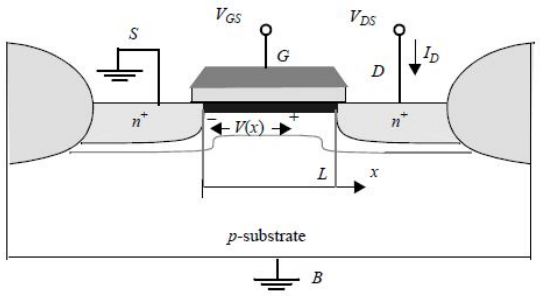
- A small positive voltage is applied to the gate, resulting in some positive charge on the gate.
- The holes in the body are repelled from the region directly beneath the gate, resulting in a ***depletion* region forming below the gate.**

- A higher positive potential exceeding a critical threshold voltage *Vt* is applied, attracting more positive charge to the gate.
- The holes are repelled further and some free electrons in the body are attracted to the region beneath the gate.
- This conductive layer of electrons in the p-type body is called **the *inversion* layer.**

The threshold voltage depends on the number of dopants in the body and the thickness *t*ox of the oxide. It is usually positive,

MOS Transistor Demonstrating – Cut-off Region, Linear Region & Saturation Region

1. Cut-off Region : ($V_{GS} > V_T ; V_{DS} = 0V$)

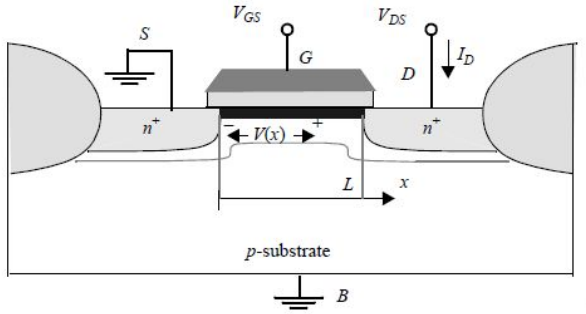


- The transistor consists of the MOS stack between two n-type regions called the *source* and *drain*. **The inversion layer / channel is formed as $V_{GS} > V_T$, *but there is no current flow as* $V_{ds} = 0$V.**
- We say the transistor is OFF, and this mode of operation is called *cutoff*.
- It is often convenient to approximate the current through an OFF transistor as zero, especially incomparison to the current through an ON transistor.
- However, that small amounts of current leaking through OFF transistors can become significant, especially when multiplied by millions or billions of transistors on a chip.

$$I_D = 0$$

2.. Non-saturation Region: ($V_{GS} > V_T$; $0V < V_{DS} < V_{sat}$)

- Assume now that $V_{GS} > V_T$ and that a small voltage, V_{DS}, is applied between drain and source.
- The voltage difference causes a current I_D to flow from drain to source
- Using a simple analysis, a first-order expression of the current as a function of V_{GS} and V_{DS} can be obtained.



- At a point *x* along the channel, the voltage is *V*(*x*), and the gate-to-channel voltage at that point equals $V_{GS} - V(x)$. Under the assumption that this voltage exceeds the threshold voltage all along the channel, the induced channel charge per unit area at point *x* can be computed as $Q_{channel}$.
- The **magnitude of current increases linearly with increasing drain voltage** till a particular drain voltage determined by the following relations :

$$V_{GS} \geq V_{th} \text{ and } V_{DS} < V_{sat} = V_{GS} - V_{th}$$

- The magnitude of current is the charge flowing through the channel and the time taken to drift across the channel.

$$I_{ds} = \frac{Q_{channel}}{t} = \frac{Charge\ flowing\ through\ the\ channel}{time\ taken\ to\ drift\ acorss\ the\ channel} ---(1)$$

2. Non-saturation Region(Cont.)

Time taken to drift acorss the channel

$$t = \frac{L_{channel}}{Velocity\ of\ electron} = \frac{L}{\mu_n E} = \frac{L}{\mu_n \frac{V_{ds}}{L}} = \frac{L^2}{\mu_n V_{ds}} \quad ---(2)$$

Charge flowing through the channel

$$Q_{channel} = C_g V \quad ---(3)$$

$where, C_g - gate\ capacitance, V - applied\ Vds\ for\ the\ current\ flow$

$$Q_{channel} = C_g \left(V_{gs} - V_t - \frac{1}{2} V_{ds} \right) \quad ---(4)$$

$where\ V_{gs} - V_t\ is\ the\ effective\ voltage$

$The\ magnitude\ of\ the\ drain\ current\ in\ non - saturation\ region\ is\ given\ by (1)$

$$I_{ds} = \frac{C_g \left(V_{gs} - V_t - \frac{1}{2} V_{ds} \right)}{\frac{L^2}{\mu_n V_{ds}}} \quad --(5)$$

2. Non-saturation Region(Cont.)

$$In\ equation\ (5)\ where\ C_g = \frac{\varepsilon A^2}{d} = \frac{\varepsilon_{ox} \mathrm{W.L}}{t_{ox}} ---(6)$$

$$Substituting\ (6)\ in\ (5), I_{ds} is\ given\ as$$

$$I_{ds} = \frac{\frac{\varepsilon_{ox} \mathrm{W.L}}{t_{ox}} \left(V_{gs} - V_t - \frac{1}{2} V_{ds} \right)}{\frac{L^2}{\mu_n V_{ds}}} ---(7)$$

$\frac{W}{L}$ *is called as Aspect Ratio*

$k_n = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$ *is called as transconductance parameter*

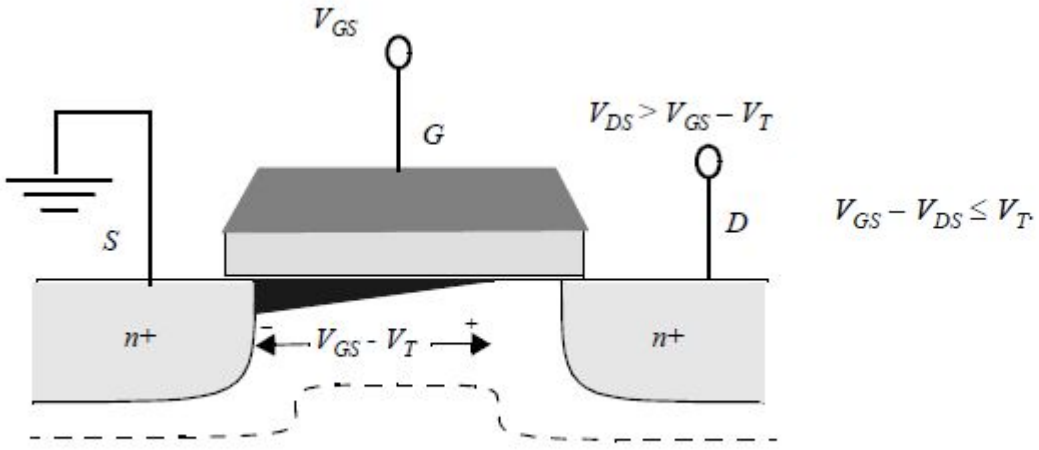
$\beta_n = k_n . \frac{W}{L}$ — *MOS transistor gain factor*

Therefore,

$$I_{ds} = \beta \left(V_{gs} - V_t - \frac{1}{2} V_{ds} \right) V_{ds} ---(8)$$; $V_{GS} \geq V_{th}$ and $V_{DS} < Vsat = V_{GS} - V_{th}$

3.Saturation Region

$$V_{gs} > V_t \; ; \; 0V < V_{ds} \geq V_{gs} - Vt \quad or \quad 0V < V_{ds} = V_{SAT}$$



- As the value of the drain-source voltage is further increased, the assumption that the channel voltage is larger than the threshold all along the channel ceases to hold. This happens when $V_{GS} - V(x) < V_T$.
- At that point, the induced charge is zero, and the conducting channel disappears or is *pinched off*.

Beyond a certain point, the surface concentration is like $\left(\ln \frac{n_s}{n_B}\right)$ *and therefore stop increasing and the surface potential is pinned off when* $n_s \cong N_A$

where, surface potential, $\psi_s = \frac{KT}{q} \ln\left(\frac{n_s}{n_B}\right)$

3.Saturation Region (Cont.)

$$V_{gs} > V_t \; ; \; 0V < V_{ds} \geq V_{gs} - Vt \quad or \quad 0V < V_{ds} = V_{SAT}$$

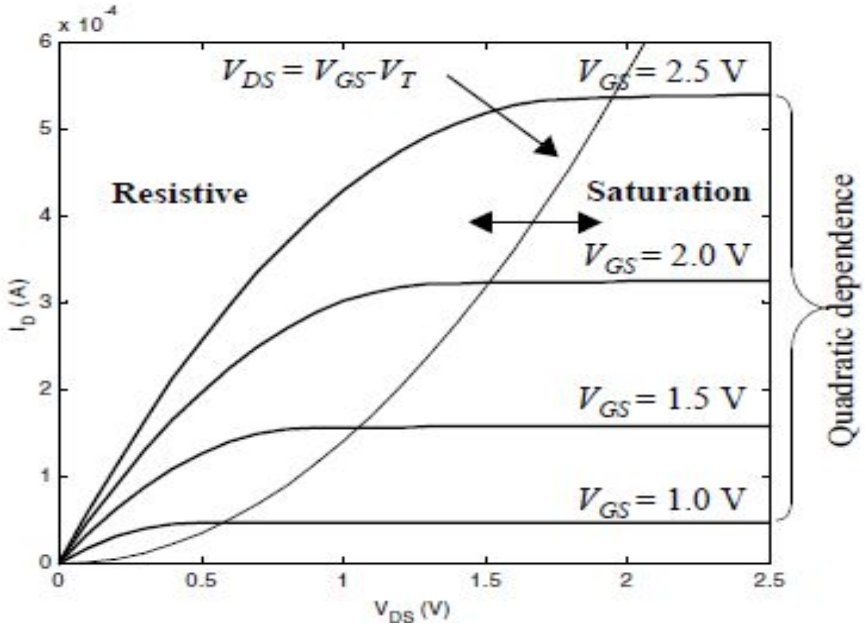
$$Substitute \; V_{ds} = V_{gs} - V_t \; in \; equation \; (8)$$

$$I_{ds} = \beta \left(V_{gs} - V_t - \frac{1}{2}(V_{gs} - V_t) \right) V_{gs} - V_t$$

$$I_{ds} = \beta \left(\frac{[V_{gs} - V_t]^2}{2} \right)$$

$$I_{ds} = \beta \left[\frac{V_{ds}{}^2}{2} \right] \text{--- (9)}$$

MOS Transistor Demonstrating – Cut-off Region, Linear Region & Saturation Region



$I_D = 0$; *Cut − off Region*

$I_D = \mu_n C_{ox} \frac{W}{L}\left(V_{gs} - V_t - \frac{1}{2}V_{ds}\right) V_{ds} = \beta \left(V_{gs} - V_t - \frac{1}{2}V_{ds}\right) V_{ds}$; **Linear Region**

$I_{ds} = I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left[V_{gs} - V_t\right]^2 = \beta \left(\frac{\left[V_{gs}-V_t\right]^2}{2}\right)$; ***Saturation Region***