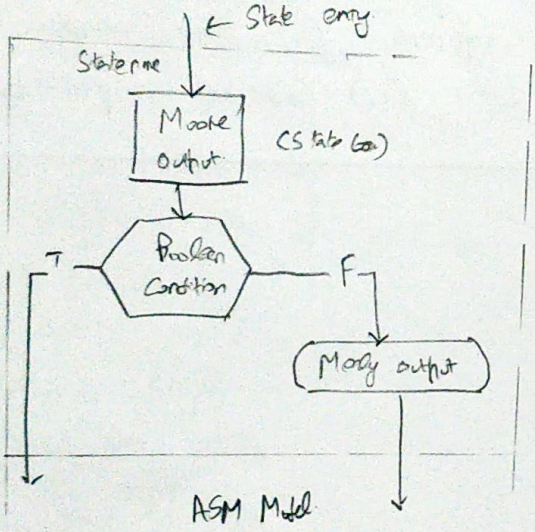
VLSI Design Lab

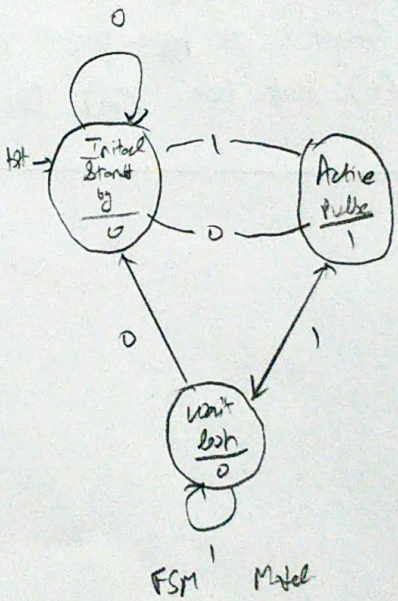
Experiment - 3

I Pre-lab Questions

1. Draw the simple model of FSM and ASM.

Soln.





2. What is the basic algorithm of sequence detector?

Soln

Step 1: Initialize the state of the detector

Step 2: Read the next input symbol or bit

Step 3: Based on the current state / input symbol / bit, determine the next state of the detector

Step 4: Check if the next state represents the complete sequence of input / symbols / bits

Step 5: If a sequence is detected, generate an output signal.

Step 6: Repeat Steps 2-5 for the remaining input symbols / bits

3. What is the difference between Mealy and Moore Model.

Soln. A mealy machine changes its output on the basis of its present state and current input. A moore machine output depends only on the current state. It does not depend on the current input.

4. What is the ASM chart and what are its main components?

Ans: An ASM Chart is a special type of flow chart that is used to describe the sequential operations of a digital circuit. It has four main components: (i) State name, (ii) State box, (iii) Decision box, (iv) Conditional output box

II Post-Lab Questions

1 Write Verilog Code to implement an FSM using Moore Machine

Soln.

```
Module moore_seq (mout, mode, in, test, clk);
output reg [3:0] mode;
output reg mout;
input in, test, clk;
always @(posedge clk, test) begin
if (test)
begin
mode <= 4'b000;
mout <= 0; end
else begin
case (mode) 4'b000 : begin
if (in == 1) mode <= 4'b0001;
             mout <= 0;
end
4'b0011 : begin if (in == 1)
mode <= 4'b0111; else mode <= 4'b000 ; end
4'b0011 : begin if (in == 1)
begin mode <= 4'b1111 , mout <= 1;
end
else begin mode <= 4'b000, mout <= 0;
end end
4'b1111 : begin if (in = 0)
begin mode <= 4'b000,
mout <= 0
end
end
```

endcase
endmodule

RESULT

A Finite State Machine and Algorithmic State Machine were studied and designed using Verilog by simulating and synthesizing using EDA tools.