

# **ELECTRONIC DEVICES AND CIRCUITS**

# About the Authors



**S Salivahanan** is the Principal of SSN College of Engineering, Chennai. He obtained his B.E. degree in Electronics and Communication Engineering from PSG College of Technology, Coimbatore, M.E. degree in Communication Systems from NIT, Trichy and Ph.D. in the area of Microwave Integrated Circuits from Madurai Kamaraj University. He has four decades of teaching, research, administration and industrial experience both in India and abroad. He has taught at NIT, Trichy, A.C. College of Engineering and Technology, Karaikudi, RV College of Engineering, Bangalore, and Mepco Schlenk Engineering College, Sivakasi. He has industrial experience as scientist/engineer at Space Applications Centre, ISRO, Ahmedabad, Telecommunication Engineer at State Organization of Electricity, Iraq and Electronics Engineer at Electric Dar Establishment, Kingdom of Saudi Arabia.

He is the author of 40 popular books which include all-time bestsellers such as *Basic Electrical and Electronics Engineering*, *Electronic Devices and Circuits*, *Linear Integrated Circuits* and *Digital Signal Processing* published by McGraw Hill Education (India), which has also been translated into Mandarin, the Chinese language, outside India by McGraw Hill. He has also authored the books on *Digital Circuits and Design*, *Electromagnetic Field Theory*, *Circuit Theory*, *Network Analysis and Synthesis* and *Control Systems Engineering*. He has published several papers at national and international levels.

Professor Salivahanan is the recipient of Bharatiya Vidya Bhavan National Award for Best Engineering College Principal (2011) from ISTE, and IEEE Outstanding Branch Counsellor and Advisor Award in the Asia-Pacific region for 1996–97. He was the Chairman of IEEE Madras Section from 2008–2009 and Syndicate Member of Anna University.

He is a Senior Member of IEEE, Fellow of IETE, Fellow of Institution of Engineers (India), Life Member of ISTE and Life Member of Society for EMC Engineers. He is also a member of IEEE societies in Microwave Theory and Techniques, Communications, Signal Processing, and Aerospace and Electronics.



**N Suresh Kumar** is the Principal of SNS College of Engineering, Coimbatore. He received his Bachelor's degree in Electronics and Communication Engineering from Thiagarajar College of Engineering, Madurai (Tamil Nadu); M.E. degree in Microwave and Optical Engineering from A.C. College of Engineering Technology, Karaikudi (Tamil Nadu); and Ph.D. in the field of EMI/EMC from Madurai Kamaraj University, Madurai (Tamil Nadu). He has over two and a half decades of teaching, administration and research experience and has authored several blockbuster titles published by McGraw-Hill Education (India).

He has published and presented many research papers in international journals and conferences. His areas of interest include Electromagnetic Interference and Compatibility, Microwave Communication and Optical Communication. He has completed research projects funded by DRDO and DST.

Professor Suresh Kumar is the recipient of Eminent Engineer Award from the Institution of Engineers (India). He is a member of IEEE, fellow of IETE, fellow of Institution of Engineers (India) and, life member in ISTE, Society of EMC Engineers, Institute for Smart Structures and Systems and Broadcast Engineering Society. He was a member of Academic Council of Anna University, Tirunelveli. He is a member of Board of Studies of Anna University, Chennai.

# **ELECTRONIC DEVICES AND CIRCUITS**

**S Salivahanan**

*Principal*

*SSN College of Engineering  
Chennai, Tamil Nadu*

**N Suresh Kumar**

*Principal*

*SNS College of Engineering  
Coimbatore, Tamil Nadu*



**McGraw Hill Education (India) Private Limited**

CHENNAI

---

*McGraw Hill Education Offices*

Chennai New York St Louis San Francisco Auckland Bogotá Caracas  
Kuala Lumpur Lisbon London Madrid Mexico City Milan Montreal  
San Juan Santiago Singapore Sydney Tokyo Toronto



**McGraw Hill Education (India) Private Limited**

Published by McGraw Hill Education (India) Private Limited  
444/1, Sri Ekambara Naicker Industrial Estate, Alapakkam, Porur, Chennai 600 116

### **Electronic Devices and Circuits**

Copyright © 2018, by McGraw Hill Education (India) Private Limited.

No part of this publication may be reproduced or distributed in any form or by any means, electronic, mechanical, photocopying, recording, or otherwise or stored in a database or retrieval system without the prior written permission of the publishers. The program listing (if any) may be entered, stored and executed in a computer system, but they may not be reproduced for publication.

This edition can be exported from India only by the publishers,  
McGraw Hill Education (India) Private Limited.

[1] 2 3 4 5 6 7 8 9 D102739 22 21 20 19 [18]

Printed and bound in India.

ISBN (13): 978-93-5316-093-7

ISBN (10): 93-5316-093-6

Director—Science & Engineering Portfolio: *Vibha Mahajan*

Senior Portfolio Manager—Science & Engineering: *Hemant K Jha*

Associate Portfolio Manager: *Vaishali Thapliyal*

Production Head: *Satinder S Baveja*

Copy Editor: *Taranpreet Kaur*

General Manager—Production: *Rajender P Ghansela*

Manager—Production: *Reji Kumar*

Information contained in this work has been obtained by McGraw Hill Education (India), from sources believed to be reliable. However, neither McGraw Hill Education (India) nor its authors guarantee the accuracy or completeness of any information published herein, and neither McGraw Hill Education (India) nor its authors shall be responsible for any errors, omissions, or damages arising out of use of this information. This work is published with the understanding that McGraw Hill Education (India) and its authors are supplying information but are not attempting to render engineering or other professional services. If such services are required, the assistance of an appropriate professional should be sought.

Typeset at Text-o-Graphics, B-1/56, Aravali Apartment, Sector-34, Noida 201 301, and printed at

Cover Design: APS Compugraphics

Cover Printer:

Visit us at: [www.mheducation.co.in](http://www.mheducation.co.in)

Write to us at: [info.india@mheducation.com](mailto:info.india@mheducation.com)

CIN: U22200TN1970PTC111531

Toll Free Number: 1800 103 5875

# Preface

*Electronic Devices and Circuits* is designed specifically to cater to the needs of second year students of B.Tech. (Electronics and Communication Engineering) JNTU. The book has a perfect blend of focused content and complete coverage. Simple, easy-to-understand and difficult-jargon-free text elucidates the fundamentals of electronics. Several solved examples, circuit diagrams and adequate questions further help students understand and apply the concepts.

The book will also serve the purpose of a text to the engineering students of degree, diploma, AIME and graduate IETE courses and as a useful reference for those preparing for competitive examinations. Additionally, it will meet the pressing needs of interested readers who wish to gain a sound knowledge and understanding of the principles of electronic devices. Practicing engineers will find the content of significant relevance in their day-to-day functioning.

The book contains six chapters. *Chapter 1* discusses Semiconductor Physics, *Chapter 2* explains Junction Diode Characteristics and Special Semiconductor Devices, *Chapter 3* is devoted to Rectifiers and Filters, *Chapter 4* deals with Transistor Characteristics (BJT and FET), *Chapter 5* covers Transistor Biasing and Thermal Stabilization and *Chapter 6* describes Small Signal Low Frequency Transistor Amplifier Models (BJT and FET).

All the topics have been profusely illustrated with diagrams for better understanding. Equal emphasis has been laid on mathematical derivations as well as their physical interpretations. Illustrative examples are discussed to emphasize the concepts and typical applications. Review questions and Objective-type questions have been given at the end of each chapter with a view to help the readers increase their understanding of the subject and to encourage further reading.

We are highly indebted to the management of our institutions for encouraging us from time to time and providing all the necessary facilities. Thanks are due to our colleagues, especially Mr. S. Karthie, Assistant Professor, Department of ECE, SSNCE, for their valuable suggestions and useful comments in the preparation of the manuscript. Our thanks are also due to Mr. R. Gopalakrishnan, Mr. K. Rajan and Mr. S. Sankar Kumar for efficiently word processing the manuscript.

We are also thankful to Prof. G. Sridevi, Aditya Engineering College, Surampalem, Andhra Pradesh, for reviewing draft chapters of the book.

We are thankful to McGraw Hill Education (India) for stimulating interest in this project and bringing out this book in a short span of time.

Further, we would like to extend the warmest thanks to our family members for their enormous patience and cooperation.

Constructive suggestions and corrections for the improvement of the book would be most welcome and highly appreciated.

**S. SALIVAHANAN**  
**N. SURESH KUMAR**

# Contents

<i>Preface</i>	v
<i>Roadmap to the Syllabus</i>	xiii
<b>1. Semiconductor Physics</b>	<b>1.1–1.36</b>
1.1 Introduction 1.1	
1.2 Insulator, Semiconductors and Metals Classification using Energy Band Diagrams 1.1	
1.2.1 Insulator 1.1	
1.2.2 Metal 1.2	
1.3 Classification of Semiconductors 1.3	
1.4 Mobility and Conductivity 1.5	
1.5 Drift and Diffusion Currents 1.8	
1.6 Generation and Recombination of Charges 1.11	
1.7 Hall Effect 1.16	
1.8 Continuity Equation 1.19	
1.9 Law of Junction 1.22	
1.10 Fermi Dirac Function 1.25	
1.11 Fermi Level in Intrinsic and Extrinsic Semiconductors 1.27	
<i>Review Questions</i> 1.32	
<i>Objective-Type Questions</i> 1.34	
<b>2. Junction Diode Characteristics and Special Semiconductor Devices</b>	<b>2.1–2.56</b>
2.1 Introduction 2.1	
2.2 Theory of <i>PN</i> Junction Diode 2.1	
2.2.1 <i>PN</i> Junction Diode in Equilibrium with no Applied Voltage 2.1	
2.2.2 Under Forward-bias Condition 2.5	
2.2.3 Under Reverse-bias Condition 2.6	
2.2.4 <i>PN</i> Junction as a Diode 2.7	
2.2.5 <i>PN</i> Junction Diode as a Rectifier 2.8	
2.2.6 Diode Ratings or Limiting Values of <i>PN</i> Junction Diode 2.8	
2.3 Current Components in <i>PN</i> Junction Diode 2.8	
2.4 Diode Equation 2.11	

2.5	Temperature Dependence on $V-I$ Characteristics	2.14
2.5.1	Effect of Temperature on Reverse Saturation Current	2.16
2.5.2	Temperature Dependence of $V-I$ Characteristics	2.17
2.6	Diode Resistance (Static and Dynamic)	2.18
2.7	Diode Capacitance	2.22
2.7.1	Transition or Space Charge (or Depletion Region) Capacitance ( $C_T$ )	2.22
2.7.2	Diffusion Capacitance ( $C_D$ )	2.25
2.8	Energy-Band Diagram of $PN$ Junction Diode	2.26
2.9	Zener Diode	2.29
2.10	Avalanche and Zener Breakdown Mechanism	2.29
2.11	Zener Diode Applications	2.30
2.12	Tunnel Diode	2.30
2.12.1	Equivalent Circuit	2.32
2.13	Light Emitting Diode (LED)	2.33
2.14	Photodiode	2.34
2.15	$PNPN$ Diode (Shockley Diode)	2.35
2.16	SCR (Silicon-Controlled Rectifier)	2.36
2.16.1	Thyristor Ratings	2.38
2.16.2	Rectifier Circuits using SCR	2.39
2.16.3	LASCR (Light-Activated SCR)	2.43
2.17	TRIAC (Triode AC Switch)	2.44
2.18	DIAC (Diode AC Switch)	2.45
2.19	UJT (Unijunction Transistor) Relaxation Oscillator	2.46
	<i>Review Questions</i>	2.50
	<i>Objective-Type Questions</i>	2.52

### 3. Rectifiers and Filters 3.1–3.34

3.1	Introduction	3.1
3.2	Rectifiers	3.1
3.2.1	Half-wave Rectifier	3.1
3.2.2	Full-wave Rectifier	3.10
3.2.3	Bridge Rectifier	3.15
3.3	Harmonic Components in a Rectifier Circuit	3.18
3.4	Filters	3.19
3.5	Inductor Filter	3.20
3.6	Capacitor Filter	3.22
3.7	L-section Filter (LC Filter)	3.25
3.8	$\pi$ -section Filter	3.28
3.9	Multiple L-section and Multiple $\pi$ -section Filter	3.29
3.9.1	Multiple L-section Filter	3.29
3.9.1	Multiple $\pi$ -section Filter	3.30
3.10	Comparison of Various Filter Circuits	3.32
	<i>Review Questions</i>	3.32
	<i>Objective-Type Questions</i>	3.33

<b>4. Transistor Characteristics (BJT and FET)</b>	<b>4.1–4.54</b>
4.1 Introduction 4.1	
4.2 Bipolar Junction Transistor 4.1	
4.2.1 Construction 4.1	
4.2.2 Transistor Biasing 4.2	
4.2.3 Operation of an <i>NPN</i> Transistor 4.2	
4.2.4 Operation of a <i>PNP</i> Transistor 4.3	
4.3 Transistor Current Components 4.3	
4.3.1 Current Amplification Factor 4.3	
4.3.2 Relationship between $\alpha$ and $\beta$ 4.3	
4.3.3 Relation among $\alpha$ , $\beta$ , and $\gamma$ 4.4	
4.3.4 Large-signal Current Gain ( $\alpha$ ) 4.4	
4.3.5 General Transistor Equation 4.5	
4.3.6 Relation among $I_C$ , $I_B$ , and $I_{CBO}$ 4.5	
4.3.7 Relation among $I_C$ , $I_B$ , and $I_{CEO}$ 4.5	
4.3.8 Relation between $I_{CBO}$ and $I_{CEO}$ 4.6	
4.3.9 dc Current Gain ( $\beta_{dc}$ or $h_{FE}$ ) 4.6	
4.4 Transistor Configurations (CE, CB and CC Characteristics) 4.7	
4.4.1 CB Configuration 4.7	
4.4.2 CE Configuration 4.10	
4.4.3 CC Configuration 4.13	
4.4.4 Comparison of Different Configurations 4.14	
4.5 Transistor as an Amplifier 4.14	
4.6 Large Signal, dc and Small-Signal CE Values of Current Gain 4.16	
4.7 Ebers–Moll Model of a Transistor 4.25	
4.8 Punch-through or Reach-through 4.27	
4.9 Phototransistor 4.27	
4.10 Typical Transistor Junction Voltage Values 4.28	
4.11 Types of FET 4.31	
4.12 FET Construction 4.31	
4.13 Operation and Characteristics of FET 4.31	
4.14 JFET Parameters 4.33	
4.14.1 Expression for Saturation Drain Current 4.37	
4.14.2 Slope of the Transfer Characteristic at $I_{DSS}$ 4.38	
4.14.3 Biasing for Zero Current Drift 4.38	
4.14.4 Comparison of JFET and BJT 4.41	
4.14.5 Applications of JFET 4.41	
4.15 MOSFET – Types and Construction 4.42	
4.15.1 Types of MOSFET 4.42	
4.15.2 Construction 4.42	
4.16 Operation and Characteristics of MOSFET 4.43	
4.16.1 Operation of MOSFET 4.43	
4.16.2 Depletion MOSFET 4.43	
4.17 Comparison of MOSFET with JFET 4.49	
<i>Review Questions</i> 4.49	
<i>Objective-Type Questions</i> 4.51	

<b>5. Transistor Biasing and Thermal Stabilization</b>	<b>5.1–5.52</b>
5.1 Introduction 5.1	
5.2 Need for Biasing 5.1	
5.3 Load Line Analysis 5.2	
5.3.1 dc Load Line 5.2	
5.3.2 ac Load Line 5.3	
5.4 BJT Biasing – Methods and Basic Stability 5.8	
5.4.1 Fixed Bias or Base Resistor Method 5.8	
5.4.2 Emitter-Feedback Bias 5.10	
5.4.3 Collector-to-Base Bias or Collector-Feedback Bias 5.13	
5.4.4 Collector-Emitter Feedback Bias 5.16	
5.4.5 Voltage-Divider Bias, Self-Bias, or Emitter Bias 5.16	
5.4.6 Common Base Stability 5.17	
5.5 Stabilization Factors 5.18	
5.6 Bias Compensation 5.30	
5.6.1 Thermistor and Sensistor Compensations 5.30	
5.6.2 Compensation Against Variation in $V_{BE}$ and $I_{CO}$ 5.31	
5.7 Thermal Runaway 5.33	
5.8 Thermal Stability 5.33	
5.9 FET Biasing – Methods and Stabilization 5.36	
5.9.1 Fixing the $Q$ -point 5.36	
5.9.2 Self-bias 5.37	
5.9.3 Voltage-Divider Bias 5.37	
5.9.4 Fixed Bias 5.38	
5.10 Biasing the MOSFET 5.39	
5.10.1 Biasing of Enhancement MOSFET 5.39	
5.10.2 Biasing of Depletion MOSFET 5.40	
<i>Review Questions</i> 5.49	
<i>Objective-Type Questions</i> 5.51	

<b>6. Small Signal Low Frequency Transistor Amplifier Models (BJT and FET)</b>	<b>6.1–6.56</b>
6.1 Introduction 6.1	
6.2 BJT as a Two Port Network 6.1	
6.2.1 Z-Parameters or Impedance Parameters 6.2	
6.2.2 Y-Parameters or Admittance Parameters 6.2	
6.2.3 Hybrid Parameters or $h$ -Parameters 6.3	
6.2.4 Notations used in Transistor Circuits 6.3	
6.3 Transistor Hybrid Model 6.4	
6.4 Determination of $h$ -parameters 6.4	
6.5 Conversion of $h$ -parameters 6.7	
6.6 Generalized Analysis of Transistor Amplifier Model using $h$ -parameters 6.7	
6.6.1 Current Gain or Current Amplification, $A_I$ 6.8	
6.6.2 Input Impedance, $Z_i$ 6.8	
6.6.3 Voltage Gain or Voltage Amplification Factor, $A_V$ 6.9	

6.6.4	Output Admittance, $Y_O$	6.9
6.6.5	Voltage Amplification ( $A_{Vs}$ ) taking into account the Source Resistance ( $R_s$ )	6.10
6.6.6	Current Amplification ( $A_{Is}$ ) taking into account the Source Resistance ( $R_s$ )	6.11
6.6.7	Operating Power Gain, $A_P$	6.11
6.7	Comparison of Transistor Amplifiers	6.13
6.8	Approximate Hybrid Model	6.15
6.9	Analysis of CE using Approximate Analysis	6.17
6.10	Analysis of CC using Approximate Analysis	6.19
6.11	Analysis of CB using Approximate Analysis	6.22
6.12	BJT Amplifiers	6.25
6.13	Single-Stage Amplifiers	6.25
6.13.1	Common-Emitter (CE) Amplifier	6.26
6.13.2	Common-Collector (CC) Amplifier	6.27
6.13.3	Common-Base (CB) Amplifier	6.29
6.14	Small-signal Analysis of Single-stage BJT Amplifiers	6.29
6.14.1	CE Amplifier with Fixed Bias	6.29
6.14.2	Common-Emitter Amplifier with Emitter Resistor	6.32
6.14.3	CE Amplifier with Unbypassed Emitter Resistor	6.34
6.14.4	CE Amplifier with Voltage-Divider Bias	6.37
6.14.5	CB Amplifier	6.42
6.14.6	CC Amplifier or Emitter Follower	6.43
6.15	Generalized Analysis of FET Small Signal Model	6.45
6.16	Analysis of CS Amplifier	6.46
6.17	Analysis of CD Amplifier	6.48
6.18	Analysis of CG Amplifier	6.49
6.19	Comparison of FET Model with BJT Model	6.52
<i>Review Questions</i>		6.52
<i>Objective-Type Questions</i>		6.54

<b>Appendix A: Probable Values of General Physical Constants</b>	<b>A.1</b>
<b>Appendix B: Conversion Factors and Prefixes</b>	<b>B.1</b>
<b>Previous Years' Solved JNTU Examination Questions</b>	<b>S.1–S.4</b>



# Roadmap to the Syllabus

JNTU Kakinada

## ELECTRONIC DEVICES AND CIRCUITS

### Unit-I

**Semiconductor Physics:** Insulators, semiconductors, and metals classification using energy band diagrams; Mobility and conductivity; Electrons and holes in intrinsic and extrinsic semiconductors; Drift and diffusion; Charge densities in semiconductors; Hall effect; continuity equation, law of junction, Fermi dirac function; Fermi level in intrinsic and extrinsic semiconductors

GO TO

**Chapter 1: Semiconductor Physics**

### Unit-II

**Junction Diode Characteristics:** Open circuited  $P-N$  junction; Biased  $P-N$  junction,  $P-N$  junction diode; Current components in  $PN$  junction diode; Diode equation;  $V-I$  characteristics; Temperature dependence on  $V-I$  characteristics; Diode resistance; Diode capacitance; Energy band diagram of  $PN$  junction diode

**Special Semiconductor Diodes:** Zener diode; Breakdown mechanisms; Zener diode applications; LED; Photodiode; Tunnel diode; SCR; UJT; Construction, operation and characteristics of all the diodes

GO TO

**Chapter 2: Junction Diode Characteristics and Special Semiconductor Devices**

### Unit-III

**Rectifiers and Filters:** Basic rectifier setup; Half-wave rectifier, Full-wave rectifier; Bridge rectifier; Derivations of characteristics of rectifiers; Rectifier circuits-operation; Input and output waveforms; Filters; Inductor filter; Capacitor filter; Comparison of various filter circuits in terms of ripple factors

GO TO

**Chapter 3: Rectifiers and Filters**

**Unit-IV****Transistor Characteristics**

**BJT:** Junction transistor; Transistor current components; Transistor equation; Transistor configurations; Transistor as an amplifier; Characteristics of transistor in common-base, common-emitter and common-collector configurations; Ebers-Moll model of a transistor; Punch-through and reach-through; Photo transistor; Typical transistor junction voltage values

**FET:** FET – types, construction, operation, characteristics, parameters; MOSFET – types, construction, operation, characteristics; Comparison between JFET and MOSFET

GO TO


**Chapter 4: Transistor Characteristics (BJT and FET)**
**Unit-V**

**Transistor Biasing and Thermal Stabilization:** Need for biasing; Operating point; Load line analysis; BJT biasing – methods, basic stability, fixed bias, collector to base bias, self bias; Stabilization against variations in  $V_{BE} > I_C$ , and  $\beta$ ; Stability factors, (S, S, S); Bias compensation; Thermal runaway; Thermal stability

FET biasing – methods and stabilization

GO TO


**Chapter 5: Transistor Biasing and Thermal Stabilization**
**Unit-VI****Small Signal Low Frequency Transistor Amplifier Models**

**BJT:** Two port network; Transistor hybrid model; Determination of  $h$ -parameters; Conversion of  $h$ -parameters; Generalized analysis of transistor amplifier model using  $h$ -parameters; Analysis of CB, CE and CC amplifiers using exact and approximate analysis; Comparison of transistor amplifiers

**FET:** Generalized analysis of small signal model; Analysis of CG, CS and CD amplifiers; Comparison of FET amplifiers

GO TO


**Chapter 6: Small Signal Low Frequency Transistor Amplifier Models (BJT and FET)**

# Semiconductor Physics

---

## 1.1 INTRODUCTION

---

Electronics is the branch of science and engineering which relates to the conduction of electricity either through vacuum by electrons or through gases by electrons and ions. Basically, it is a study of electronic devices and their utilization. An electron device is that in which electrons flow through a vacuum or gas or semiconductor. In the beginning of 20th century, electrons began to take technological shape and it has enjoyed an explosive development in the last few decades.

Electronics has a wide range of applications, such as rectification, amplification, power generation, industrial control, photo-electricity, communications and so on. The electronic industry turns out a variety of items in the range of consumer electronics, control and industrial electronics, communication and broadcasting equipments, biomedical equipments, calculators, computers, microprocessors, aerospace and defence equipments and components.

A semiconductor is a material that has a resistivity value in between that of a conductor and an insulator. The conductivity of a semiconductor material can be varied under an external electric field. Devices made from semiconductor materials are the foundation of modern electronics which includes radio, computers, telephones, and many other devices. Semiconductor devices include the transistor, many kinds of diodes including the light emitting diode, the silicon controlled rectifier, and digital and analog integrated circuits.

This chapter deals with the classification of semiconductors based on energy band diagram. It also discusses the doping in semiconductors, Hall effect and Fermi level in semiconductors.

---

## 1.2 INSULATOR, SEMICONDUCTORS AND METALS CLASSIFICATION USING ENERGY BAND DIAGRAMS

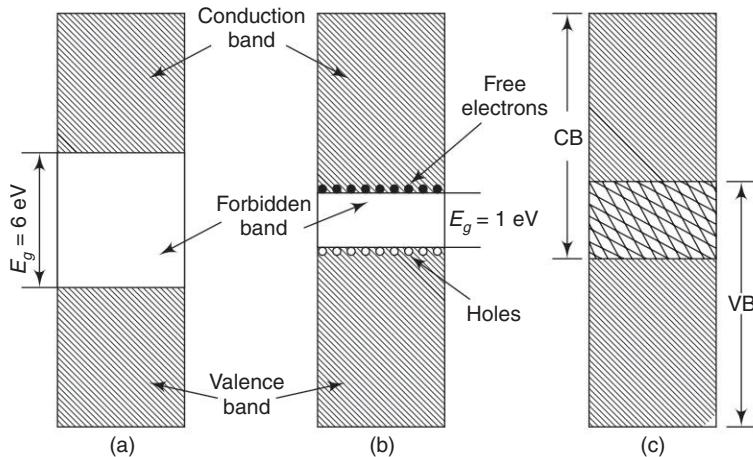
---

A very poor conductor of electricity is called an insulator; an excellent conductor is a metal; and a material whose conductivity lies between these two extremes is a semiconductor. A material may be classified as one of these three depending upon its energy-band structure.

### 1.2.1 Insulator

An insulator is a material having extremely poor electrical conductivity. The energy-band structure at the normal lattice spacing is indicated schematically in Fig. 1.1(a). The forbidden energy gap is large; for diamond, the energy gap is about 6 eV. If additional energy is given to an electron in the upper level of valence band, this electron attempts to cross the forbidden energy gap and enter the conduction band. However, in

an insulator, the additional energy which may ordinarily be given to an electron is, in general, much smaller than this high value of forbidden energy gap. Hence, no electrical conduction is possible. The number of free electrons in an insulator is very small, roughly about  $10^7$  electrons/m<sup>3</sup>.



**Fig. 1.1** Energy-band gap in (a) insulators, (b) semiconductors, and (c) metals

### 1.2.2 Metal

Conduction in metals is only due to the electrons. A metal has overlapping valence and conduction bands. The valence band is only partially filled and the conduction band extends beyond the upper end of filled valence band. The outer electrons of an atom are as much associated with one ion as with another, so that the electron attachment to any individual atom is almost zero. The band occupied by the valence electrons may not be completely filled and that there are no forbidden levels at higher energies. Depending upon the metal, at least one, and sometimes two or three, electrons per atom are free to move throughout the interior of the metal under the action of applied fields. When an electric field is applied, few electrons may acquire enough additional energy and move to higher energy level within the conduction band. Thus, the electrons become mobile. Since the additional energy required for transfer of electrons from valence band to conduction band is extremely small, the conductivity of a metal is excellent.

In *electron-gas theory* description of a metal, the metal is visualized as a region containing a periodic three-dimensional array of heavy, tightly bound ions permeated with a swarm of electrons that may move about quite freely. According to this theory, the electrons in a metal are continuously moving and the direction of motion changes whenever the electron collides with other electrons. The average distance travelled by an electron between successive collisions is called *mean-free-path* of an electron. In the absence of any applied potential, the average current in a metal is zero because the number of electrons passing through unit area in any direction is almost same as the number of electrons passing through the same unit area in the opposite direction. This can be attributed to the random nature of motion of electrons.

When a constant electric field  $E$  (volt per metre) is applied to a metal, the electrons would be accelerated and its velocity would increase indefinitely with time. However, because of collision of electrons, electrons lose energy and a steady-state condition is reached where a finite value of drift velocity  $v_d$  is attained. The drift velocity,  $v_d$  is in the direction opposite to that of the electric field and its magnitude is proportional to  $E$ .

Thus,

$$v_d = \mu E \quad (1.1)$$

where  $\mu$  = mobility of the electron,  $\text{m}^2/\text{volt-second}$ . Due to the applied field, a steady-state drift velocity has been superimposed upon the random thermal motion of the electrons. Such a directed flow of electrons constitutes a current. If the concentration of free electrons is  $n$  (electrons per cubic meter), the current density  $J$  (ampere per square metre) is

$$J = nqv_d = nq\mu E = \sigma E \quad (1.2)$$

where

$$\sigma = nq\mu \quad (1.3)$$

$\sigma$  is the *conductivity* of the metal in  $(\text{ohm-metre})^{-1}$ . For a good conductor,  $n$  is very large, approximately,  $10^{28}$  electrons/ $\text{m}^3$ . Equation (1.2) can be recognized as Ohm's law which states that the conduction current density is proportional to the applied electric field. The energy acquired by the electrons from the applied field is given to the lattice ions as a result of collisions. Hence, power is dissipated within the metal by the electrons, and the power density (joule heat) is given by

$$JE = \sigma E^2 \text{ watt/metre}^3 \quad (1.4)$$

### 1.3 CLASSIFICATION OF SEMICONDUCTORS

Semiconductors are classified as (i) intrinsic (pure), and (ii) extrinsic (impure) types. The extrinsic semiconductors are of *N-type* and *P-type*.

**Intrinsic Semiconductor** A pure semiconductor is called an intrinsic semiconductor. As already explained in the first chapter, even at room temperature, some of the valence electrons may acquire sufficient energy to enter the conduction band to form free electrons. Under the influence of an electric field, these electrons constitute electric current. A missing electron in the valence band leaves a vacant space, which is known as *hole*, as shown in Fig. 1.2. Holes also contribute to electric current.

In an intrinsic semiconductor, even at room temperature, electron-hole pairs are created. When an electric field is applied across an intrinsic semiconductor, the current conduction takes place due to free electrons and holes. Under the influence of an electric field, the total current through the semiconductor is the sum of currents due to free electrons and holes.

Though the total current inside the semiconductor is due to free electrons and holes, the current in the external wire is only by electrons. In Fig. 1.3, holes being positively charged move towards the negative terminal of the battery. As the holes reach the negative terminal of the battery, electrons enter the semiconductor near

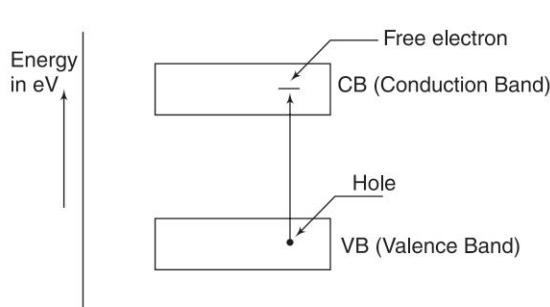


Fig. 1.2 Creation of electron-hole pair in a semiconductor

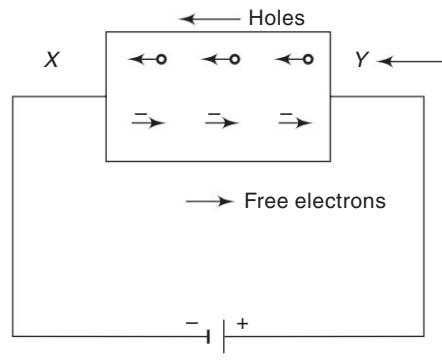


Fig. 1.3 Current conduction in semiconductor

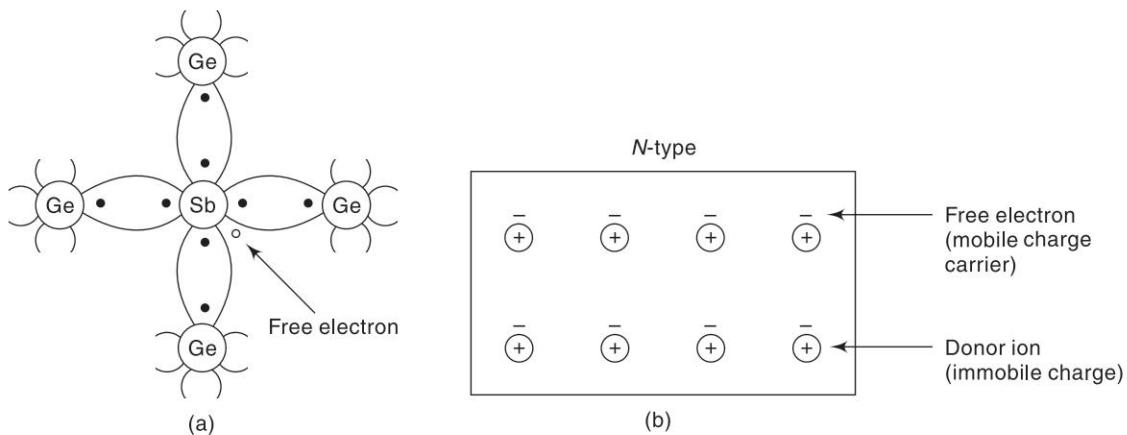
the terminal ( $X$ ) and combine with the holes. At the same time, the loosely held electrons near the positive terminal ( $Y$ ) are attracted towards the positive terminal. This creates new holes near the positive terminal which again drift towards the negative terminal.

**Extrinsic Semiconductor** Due to the poor conduction at room temperature, the intrinsic semiconductor as such, is not useful in the electronic devices. Hence, the current conduction capability of the intrinsic semiconductor should be increased. This can be achieved by adding a small amount of impurity to the intrinsic semiconductor, so that it becomes impure or extrinsic semiconductor. This process of adding impurity is known as *doping*.

The amount of impurity added is extremely small, say 1 to 2 atoms of impurity in  $10^6$  intrinsic atoms.

**N-type Semiconductor** A small amount of pentavalent impurity such as arsenic, antimony, or phosphorus is added to the pure semiconductor (germanium or silicon crystal) to get an *N*-type semiconductor.

The germanium atom has four valence electrons and antimony has five valence electrons. As shown in Fig. 1.4, each antimony atom forms a covalent bond with surrounding four germanium atoms. Thus, four valence electrons of the antimony atom form a covalent bond with four valence electrons of an individual germanium atom and the fifth valence electron is left free which is loosely bound to the antimony atom.

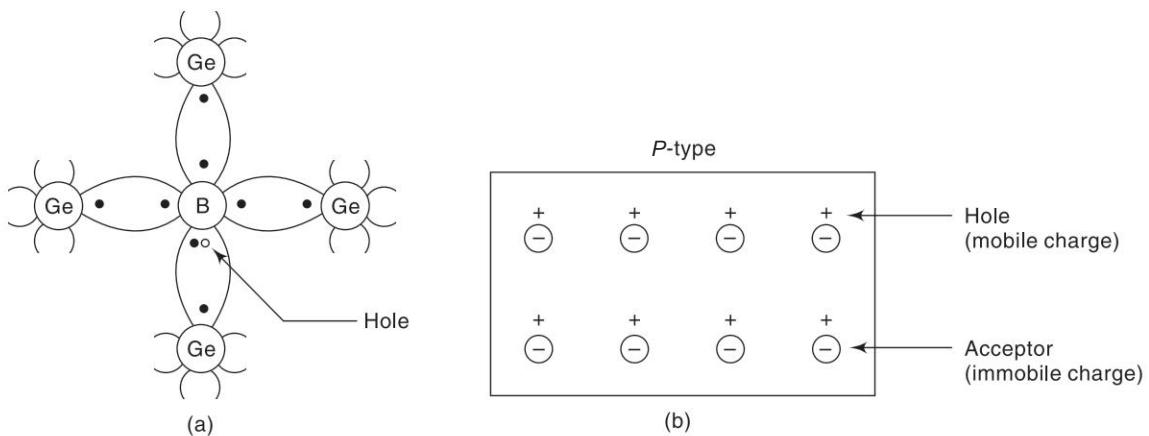


**Fig. 1.4** N-type semiconductor: (a) Formation of covalent bonds (b) Charged carriers

This loosely bound electron can be easily excited from the valence band to the conduction band by the application of electric field or increasing the thermal energy. Thus, every antimony atom contributes one conduction electron without creating a hole. Such a pentavalent impurity is called a donor impurity because it donates one electron for conduction. On giving an electron for conduction, the donor atom becomes a positively charged ion because it loses one electron. But it cannot take part in conduction because it is firmly fixed in the crystal lattice.

Thus, the addition of a pentavalent impurity (antimony) increases the number of electrons in the conduction band, thereby increasing the conductivity of an *N*-type semiconductor. As a result of doping, the number of free electrons far exceeds the number of holes in an *N*-type semiconductor. So electrons are called majority carriers and holes are called minority carriers.

**P-type Semiconductor** A small amount of trivalent impurity such as aluminium or boron is added to the pure semiconductor to get the P-type semiconductor. The germanium (Ge) atom has four valence electrons and boron has three valence electrons as shown in Fig. 1.5. Three valence electrons in boron form a covalent bond with four surrounding atoms of Ge leaving one bond incomplete which gives rise to a hole. Thus, the trivalent impurity (boron) when added to the intrinsic semiconductor (germanium) introduces a large number of holes in the valence band. These positively charged holes increase the conductivity of the P-type semiconductor. A trivalent impurity such as boron is called *acceptor impurity* because it accepts free electrons in the place of holes. As each boron atom donates a hole for conduction, it becomes a negatively charged ion. As the number of holes is very much greater than the number of free electrons in a P-type material, holes are termed *majority carriers* and electrons *minority carriers*.



**Fig. 1.5** P-type semiconductor: (a) Formation of covalent bonds (b) Charged carriers

## 1.4 MOBILITY AND CONDUCTIVITY

The conductivity of a material is proportional to the concentration of free electrons. The number of free electrons in a semiconductor lies between  $10^7$  and  $10^{28}$  electrons/m<sup>3</sup>. Thus, a semiconductor has conductivity much greater than that of an insulator but much smaller than that of a metal. Typically, a semiconductor has a forbidden energy gap of about 1 eV. The most important practical semiconductor materials are germanium and silicon, which have values of  $E_g$  of 0.785 and 1.21 eV, respectively, at 0 degree Kelvin. Energies of this magnitude normally cannot be acquired from an applied field. At low temperatures the valence band remains full, the conduction band empty, and these materials are insulators at low temperatures. The conductivity of these materials increases with temperature and hence, these materials are called as intrinsic semiconductors. As the temperature is increased, some of the electrons in the valence band acquire thermal energy greater than the gap energy and move into the conduction band. These electrons are now free to move about under the influence of even a small applied field. These free electrons, also called *conduction electrons*, constitute for conduction and the material becomes slightly conducting. The current density due to the motion of electrons is given by

$$J_n = n\mu_n qE = \sigma_n E \quad (1.5)$$

where,  $\mu_n$  is the electron mobility, and the suffix ‘ $n$ ’ represents that the respective terms are due to motion of electrons. The absence of an electron in the valence band is represented by a small circle and is called a hole. The hole may serve as a carrier of electricity whose effectiveness is comparable with the free electron. The hole conduction current density is given by

$$J_p = p\mu_p qE = \sigma_p E \quad (1.6)$$

where  $\mu_p$  is the hole mobility and  $p$  is the hole concentration.

Hence, the total current density  $J$  in a semiconductor is given by

$$J = (n\mu_n + p\mu_p)qE = \sigma E \quad (1.7)$$

where  $\sigma = (n\mu_n + p\mu_p)q$  is the total conductivity of a semiconductor. For a pure semiconductor (intrinsic semiconductor), the number of free electrons is exactly same as the number of holes. Thus, the total current density is

$$J = n_i(\mu_n + \mu_p) qE \quad (1.8)$$

where  $n_i = n = p$  is the intrinsic concentration of a semiconductor.

The conductivity of an intrinsic semiconductor can be increased by introducing certain impurity atoms into the crystal. This results in allowable energy states which lie in the forbidden energy gap and these impurity levels also contribute to the conduction. Such a semiconductor material is called an extrinsic semiconductor.

**Effective Mass** An electron travelling through a crystal under the influence of an externally applied field hardly notices the electrostatic field of the ions making up the lattice, i.e., it behaves as if the applied field were the only one present. This is the basis of the electron-gas approximation and the assumption will now be looked at a little more closely. If the electrons were to experience only the applied field,  $E$ , then immediately after a collision it would accelerate in the direction of the field with an acceleration  $a$ , proportional to the applied force, i.e.,

$$qE = ma \quad (1.9)$$

where the constant of proportionality is the electron mass,  $m$ . When quantum theory is applied to the problem of an electron moving through a crystal lattice, it predicts that under the action of an applied field, the electron acceleration will indeed be proportional to the field, but that the constant of proportionality will be different from the normal mass of an electron:

$$qE = m_n a \quad (1.10)$$

The field due to the lattice ions can, therefore, be ignored providing we treat the electrons inside the crystal as if they had a slightly different mass to the real electron mass or, to put it another way, the effect of the lattice ions on an electron is to make it behave as if it had a different mass. This new mass is called the effective mass of the electron,  $m_n$ , and the effective mass of a hole,  $m_p$ , can be similarly defined. In general,  $m_n$  and  $m_p$  are not the same. Usually,  $m_n$  is of the same order as  $m$ ; in germanium, for instance,  $m_n = 0.2$  m and in silicon,  $m_n = 0.4$  m.

The value of effective mass is an important parameter for any semiconductor, especially from the device point of view. Certain semiconductors, for instance, have low electron effective mass and hence, high electron mobility. This makes them very suitable for high-frequency devices. The III-V semiconductor GaAs comes into this category and some of the best microwave transistors are made from this material.

In a pure semiconductor, the number of holes is equal to the number of electrons. Thermal agitation continues to produce new electron-hole pairs and the electron-hole pair disappears because of recombination. With each electron-hole pair created, two charge-carrying particles are formed. One is negative which is the free electron with mobility  $\mu_n$ . The other is positive, i.e., the hole with mobility  $\mu_p$ . The electrons and holes move in opposite directions in an electric field  $E$ , but since they are of opposite sign, the current due to each is in the same direction. Hence, the total current density  $J$  within the intrinsic semiconductor is given by

$$\begin{aligned} J &= J_n + J_p \\ &= qn \mu_n E + qp \mu_p E \\ &= (n\mu_n + p\mu_p)qE \\ &= \sigma E \end{aligned} \quad (1.11)$$

where  $J_n$  = electron-drift current density

$J_p$  = hole-drift current density

$n$  = number of electrons per unit volume, i.e., magnitude of free-electron (negative) concentration

$p$  = number of holes per unit volume, i.e., magnitude of hole (positive) concentration

$E$  = applied electric field strength, V/m

$q$  = charge of electron or hole, coulomb

Hence,  $\sigma$  is the conductivity of a semiconductor which is equal to  $(n\mu_n + p\mu_p)q$ . The resistivity ( $\rho$ ) of a semiconductor is the reciprocal of conductivity, i.e.,  $\rho = \frac{1}{\sigma}$ .

It is evident from the above equation that current density within a semiconductor is directly proportional to the applied electric field.

For a pure (intrinsic) semiconductor,  $n = p = n_i$ , where  $n_i$  is the intrinsic carrier concentration.

Therefore,

$$J = n_i (\mu_n + \mu_p) qE$$

and conductivity of an intrinsic semiconductor is  $\sigma_i = qn_i(\mu_n + \mu_p)$ . Hence, it is clear that conductivity of an intrinsic semiconductor depends upon its intrinsic concentration ( $n_i$ ) and the mobility of electrons ( $\mu_n$ ) and holes ( $\mu_p$ ). The intrinsic conductivity of germanium and silicon increase by approximately 5 percent per °C and 7 percent per °C rise in temperature respectively due to the influence of  $n_i$ .

**Conductivities of N- and P-type Semiconductors** The conductivity of an intrinsic semiconductor,

$$\sigma_i = q \cdot n_i (\mu_n + \mu_p) = q \cdot (n \mu_n + p \mu_p) \quad (1.12)$$

For an *N*-type semiconductor, as  $n \gg p$ , then the conductivity,  $\sigma = q \cdot n \cdot \mu_n$ .

For a *P*-type semiconductor, as  $p \gg n$ , the conductivity,  $\sigma = q \cdot p \cdot \mu_p$ .

### EXAMPLE 1.1

The mobility of free electrons and holes in pure germanium are 3,800 and 1,800 cm<sup>2</sup>/V-s, respectively. The corresponding values for pure silicon are 1,300 and 500 cm<sup>2</sup>/V-s, respectively. Determine the values of intrinsic conductivity for both germanium and silicon. Assume  $n_i = 2.5 \times 10^{13} \text{ cm}^{-3}$  for germanium and  $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$  for silicon at room temperature.

**Solution**

The intrinsic conductivity for germanium,

$$\begin{aligned}\sigma_i &= qn_i(\mu_n + \mu_p) \\ &= (1.602 \times 10^{-19}) (2.5 \times 10^{13}) (3800 + 1800) \\ &= 0.0224 \text{ S/cm}\end{aligned}$$

The intrinsic conductivity for silicon,

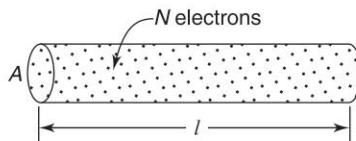
$$\begin{aligned}\sigma_i &= qn_i(\mu_n + \mu_p) \\ &= (1.602 \times 10^{-19}) (1.5 \times 10^{10}) (1300 + 500) \\ &= 4.32 \times 10^{-6} \text{ S/cm}\end{aligned}$$

## 1.5 DRIFT AND DIFFUSION CURRENTS

The flow of charge, i.e., current, through a semiconductor material is of two types, namely, drift and diffusion. The net current that flows through a *PN* junction diode also has two components, viz., (i) drift current, and (ii) diffusion current.

**Drift Current** When an electric field is applied across the semiconductor material, the charge carriers attain a certain drift velocity  $v_d$ , which is equal to the product of the mobility of the charge carriers and the applied electric field intensity,  $E$ . The holes move towards the negative terminal of the battery and electrons move towards the positive terminal. This combined effect of movement of the charge carriers constitutes a current known as *drift current*. Thus, drift current is defined as the flow of electric current due to the motion of the charge carriers under the influence of an external electric field.

▪ **Drift current density** Figure 1.6 shows that a conducting wire of length  $l$  cm contains  $N$  electrons. If an electron travels a distance of  $l$  cm in the conductor in time  $T$  sec, the total number of electrons passing through any cross section of wire per second is  $\frac{N}{T}$ .



**Fig. 1.6** Conducting wire to determine drift current density

The total current flowing through the wire with area of cross-section  $A$  is given by

$$I = \frac{Nq}{T} = \frac{Nqv_d}{l}$$

where  $v_d$  is the drift velocity and time  $T = \frac{l}{v_d}$ . The drift current density  $J$  is defined as the current per unit area of the conducting medium.

i.e.,

$$J = \frac{I}{A} = \frac{Nqv_d}{lA} \text{ A/cm}^2$$

Here,  $lA$  is the volume containing  $N$  electrons and the electron concentration,  $n = \frac{N}{lA}$ .

Therefore,

$$J = nqv_d = \rho v_d$$

where  $\rho = nq$  is the charge density, in coulomb per cubic centimeter. Generally, the above current density can also be written as

$$J = nqv_d = nq\mu E = \sigma E$$

where  $E$  is the applied electric field intensity in V/cm,  $\mu$  is the mobility of electrons in  $\text{cm}^2/\text{V}\cdot\text{s}$ , the drift velocity,  $v_d = \mu E$  in cm/s, and the conductivity,  $\sigma = nq\mu$  in  $\text{S}\cdot\text{m}^{-1}$ . The equation  $J = \sigma E$  is also called Ohm's law.

The drift current density due to the charge carriers such as free electrons and holes are the current passing through a square centimeter perpendicular to the direction of flow. The equation for the drift current density,  $J_n$ , due to free electrons is given by

$$J_n = qn\mu_n E \text{ A/cm}^2$$

and the drift current density,  $J_p$ , due to holes is given by

$$J_p = qp\mu_p E \text{ A/cm}^2$$

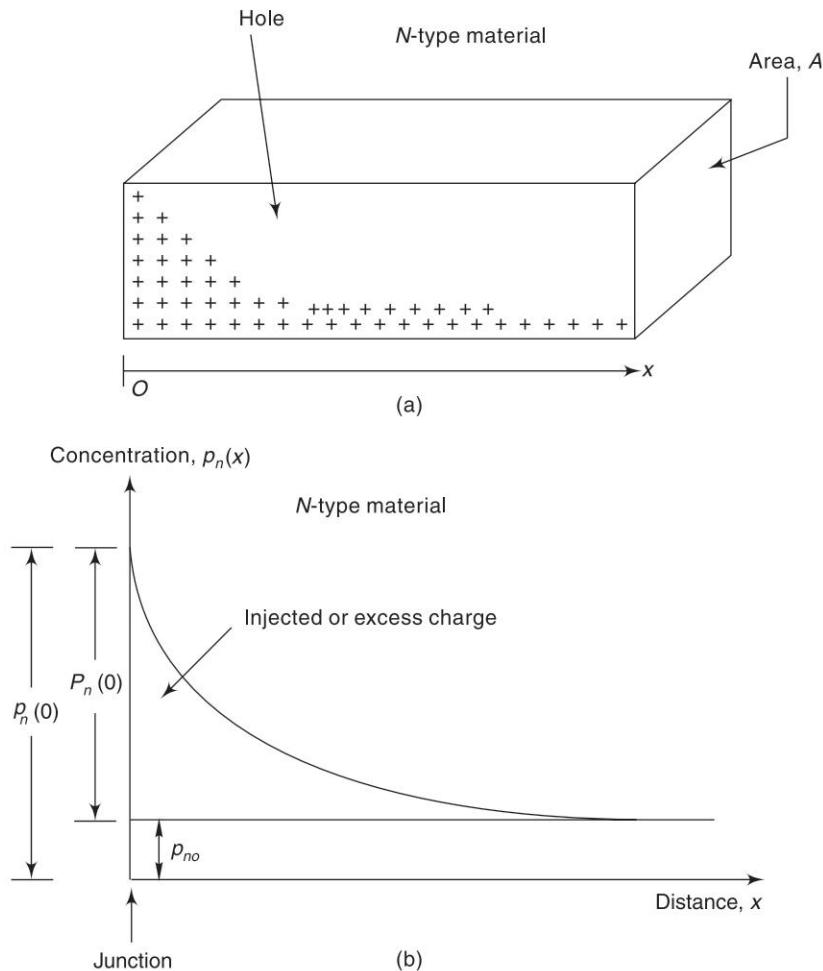
where  $n$  = number of free electrons per cubic centimetre  
 $p$  = number of holes per cubic centimetre  
 $\mu_n$  = mobility of electrons in  $\text{cm}^2/\text{V}\cdot\text{s}$   
 $\mu_p$  = mobility of holes in  $\text{cm}^2/\text{V}\cdot\text{s}$   
 $E$  = applied electric field intensity in V/cm  
 $q$  = charge of an electron =  $1.602 \times 10^{-19}$  coulomb

**Diffusion Current** It is possible for an electric current to flow in a semiconductor even in the absence of the applied voltage, provided a concentration gradient exists in the material. A concentration gradient exists if the number of either electrons or holes is greater in one region of a semiconductor as compared to the rest of the region. In a semiconductor material, the charge carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers. Thus, the movement of charge carriers takes place resulting in a current called *diffusion current*. The diffusion current depends on the material of the semiconductor, type of charge carriers, and the concentration gradient.

As indicated in Fig. 1.7(a), the hole concentration  $p(x)$  in a semiconductor bar varies from a high value to a low value along the  $x$ -axis and is constant in the  $y$ - and  $z$ -directions.

Diffusion current density due to holes,  $J_p$ , is given by

$$J_p = -qD_p \frac{dp}{dx} \text{ A/cm}^2 \quad (1.13)$$



**Fig. 1.7** (a) Excess hole concentration varying along the axis in an N-type semiconductor bar  
 (b) The resulting diffusion current

Since the hole density  $p(x)$  decreases with increasing  $x$  as shown in Fig. 1.7(b),  $dp/dx$  is negative and the minus sign in the above equation is needed in order that  $J_p$  has a positive sign in the positive  $x$ -direction.

Diffusion current density due to the free electrons,  $J_n$ , is given by

$$J_n = qD_n \frac{dn}{dx} \text{ A/cm}^2$$

where  $dn/dx$  and  $dp/dx$  are the concentration gradients for electrons and holes respectively, in the  $x$ -direction, and  $D_n$  and  $D_p$  are the diffusion coefficients expressed in  $\text{cm}^2/\text{s}$  for electrons and holes, respectively.

**Total Current** The total current in a semiconductor is the sum of drift current and diffusion current. Therefore, for a P-type semiconductor, the total current per unit area, i.e., the total current density is given by

$$J_p = qp\mu_p E - qD_p \frac{dp}{dx}$$

Similarly, the total current density for an *N*-type semiconductor is given by

$$J_n = qn\mu_n E + qD_n \frac{dn}{dx}$$

### Einstein Relationship for a Semiconductor

There exists a definite relationship between the mobility and diffusion coefficient of a particular type of charge carrier in the same semiconductor. The higher the value of mobility of a charge carrier, the greater will be its tendency to diffuse. The equation which relates the mobility  $\mu$  and the diffusion coefficient  $D$  is known as the *Einstein relationship*. The Einstein relationship is expressed as

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = \frac{kT}{q} = V_T \quad (1.14)$$

The importance of the Einstein relationship is that it can be used to determine  $D_p$  (or  $D_n$ ), if the mobility of holes (or electrons) is measured experimentally. For an intrinsic silicon,  $D_p = 13 \text{ cm}^2/\text{s}$  and  $D_n = 34 \text{ cm}^2/\text{s}$ . For an intrinsic germanium,  $D_p = 47 \text{ cm}^2/\text{s}$  and  $D_n = 99 \text{ cm}^2/\text{s}$ .

**Diffusion Length ( $L$ )** As shown in Fig. 1.6, the excess hole or electron densities fall off exponentially with distance as a result of the recombination of these excess minority carriers with the majority carriers of the semiconductor. Here, the excess charge carriers have a finite lifetime,  $\tau$ , before they are totally destroyed by recombination. The average distance that an excess charge carrier can diffuse during its lifetime is called the diffusion length  $L$ , which is given by

$$L = \sqrt{D\tau}$$

where  $D$  is the diffusion coefficient that may be related to the drift mobility,  $\mu$ , through the Einstein relation as

$$D = \mu \frac{kT}{q}$$

If the transverse length of the semiconductor is greater than the diffusion length  $L$  then the terminal currents are the recombination currents arising out of the recombination, as every electron lost by recombination is supplanted by the terminal electrode to maintain the charge neutrality.

## 1.6 GENERATION AND RECOMBINATION OF CHARGES

If a pure semiconductor is doped with *N*-type impurities, the number of electrons in the conduction band increases above a level and the number of holes in the valence band decreases below a level, which would be available in the intrinsic (pure) semiconductor. Similarly, the addition of *P*-type impurities to a pure semiconductor increases the number of holes in the valence band above a level and decreases the number of electrons in the conduction band below a level, which would have been available in the intrinsic semiconductor. This is because the rate of recombination increases due to the presence of large number of free electrons (or holes).

Further, the experimental results state that under thermal equilibrium for any semiconductor, the product of the number of holes and the number of electrons is constant and is independent of the amount of donor and acceptor impurity doping. This relation is known as *mass-action law* and is given by

$$n \cdot p = n_i^2 \quad (1.15)$$

where  $n$  is the number of free electrons per unit volume,  $p$  is the number of holes per unit volume, and  $n_i$  is the intrinsic concentration.

While considering the conductivity of the doped semiconductors, only the dominant majority charge carriers have to be considered.

**Charge Densities in N-type and P-type Semiconductors** The law of mass-action provides the relationship between free-electron concentration and hole concentration. These concentrations are further related by the *law of electrical neutrality* as given below.

Let  $N_D$  be the concentration of donor atoms in an *N*-type semiconductor. In order to maintain the electric neutrality of the crystal, we have

$$\begin{aligned} n_N &= N_D + p_N \\ &\approx N_D \end{aligned}$$

where  $n_N$  and  $p_N$  are the electron and hole concentrations in the *N*-type semiconductor. The value of  $p_N$  is obtained from the relations of mass-action law as

$$\begin{aligned} p_N &= \frac{n_i^2}{n_N} \\ &\approx \frac{n_i^2}{N_D}, \text{ which is } \ll n_N \text{ or } N_D \end{aligned}$$

Similarly, in a *P*-type semiconductor, we have

$$\begin{aligned} p_P &= N_A + n_P \\ &\approx N_A \end{aligned}$$

where  $N_A$ ,  $p_P$ , and  $n_P$  are the concentrations of acceptor impurities, holes, and electrons respectively in a *P*-type semiconductor.

$$\text{From the mass-action law, } n_P = \frac{n_i^2}{p_P}$$

$$\text{Therefore, } n_P = \frac{n_i^2}{N_A}, \text{ which is } \ll p_P \text{ or } N_A$$

**Extrinsic Conductivity** The conductivity of an *N*-type semiconductor is given by

$$\sigma_N = qn_N \mu_n \approx qN_D \mu_n, \text{ since } n_N \approx N_D$$

The conductivity of a *P*-type semiconductor is given by

$$\sigma_P = qp_P \mu_P \approx qN_A \mu_P, \text{ since } p_P \approx N_A$$

The doping of intrinsic semiconductor considerably increases its conductivity.

If the concentration of donor atoms added to a *P*-type semiconductor exceeds the concentration of acceptor atoms, i.e.,  $N_D \gg N_A$ , then the semiconductor is converted from *P*-type to *N*-type. Similarly, a large number of acceptor atoms added to an *N*-type semiconductor can convert it to a *P*-type semiconductor if  $N_A \gg N_D$ . This concept is precisely used in the fabrication of a *PN* junction, which is an essential part of semiconductor devices and integrated circuits.

### EXAMPLE 1.2

Consider a silicon *PN* junction at  $T = 300$  K so that  $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$ . The *N* type doping is  $1 \times 10^{10} \text{ cm}^{-3}$  and a forward bias of 0.6 V is applied to the *PN* junction. Calculate the minority hole concentration at the edge of the space charge region.

**Solution** Given  $T = 300$  K,  $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$ ,  $n = 1 \times 10^{10} \text{ cm}^{-3}$  and  $V_F = 0.6$  V

From mass action law,

$$n \cdot p = n_i^2$$

Therefore, the concentration of holes is

$$p = \frac{n_i^2}{n} = \frac{(1.5 \times 10^{10})^2}{1 \times 10^{10}} = 2.25 \times 10^{10} \text{ cm}^{-3}$$

### EXAMPLE 1.3

Find the conductivity of silicon (a) in intrinsic condition at a room temperature of 300 K, (b) with donor impurity of 1 in  $10^8$ , (c) with acceptor impurity of 1 in  $5 \times 10^7$ , and (d) with both the above impurities present simultaneously. Given that  $n_i$  for silicon at 300 K is  $1.5 \times 10^{10} \text{ cm}^{-3}$ ,  $\mu_n = 1300 \text{ cm}^2/\text{V-s}$ ,  $\mu_p = 500 \text{ cm}^2/\text{V-s}$ , number of Si atoms per  $\text{cm}^3 = 5 \times 10^{22}$ .

**Solution**

(a) In intrinsic condition,  $n = p = n_i$

Hence,

$$\begin{aligned}\sigma_i &= qn_i(\mu_n + \mu_p) \\ &= (1.602 \times 10^{-19})(1.5 \times 10^{10})(1300 + 500) \\ &= 4.32 \times 10^{-6} \text{ S/cm}\end{aligned}$$

(b) Number of silicon atoms/ $\text{cm}^3 = 5 \times 10^{22}$

Hence,

$$N_D = \frac{5 \times 10^{22}}{10^8} = 5 \times 10^{14} \text{ cm}^{-3}$$

Further,

$$n \approx N_D$$

Therefore,

$$p = \frac{n_i^2}{n} \approx \frac{n_i^2}{N_D} = \frac{(1.5 \times 10^{10})^2}{5 \times 10^{14}} = 0.46 \times 10^6 \text{ cm}^{-3}$$

Thus,  $p \ll n$ . Hence,  $p$  may be neglected while calculating the conductivity.

Hence,

$$\begin{aligned}\sigma &= nq\mu_n = N_D q\mu_n \\ &= (5 \times 10^{14})(1.602 \times 10^{-19})(1300) = 0.104 \text{ S/cm.}\end{aligned}$$

$$(c) \quad N_A = \frac{5 \times 10^{22}}{5 \times 10^7} = 10^{15} \text{ cm}^{-3}$$

Further,

$$p \approx N_A$$

$$\text{Hence, } n = \frac{n_i^2}{p} \approx \frac{n_i^2}{N_A} = \frac{(1.5 \times 10^{10})^2}{10^{15}} = 2.25 \times 10^5 \text{ cm}^{-3}$$

Thus,  $p >> n$ . Hence,  $n$  may be neglected while calculating the conductivity.

$$\begin{aligned} \text{Hence, } \sigma &= pq\mu_p = N_A q \mu_p \\ &= (10^{15} \times 1.602 \times 10^{-19} \times 500) = 0.08 \text{ S/cm.} \end{aligned}$$

- (d) With both types of impurities present simultaneously, the net acceptor impurity density is,

$$N'_A = N_A - N_D = 10^{15} - 5 \times 10^{14} = 5 \times 10^{14} \text{ cm}^{-3}$$

Hence,

$$\begin{aligned} \sigma &= N'_A q \mu_p \\ &= (5 \times 10^{14}) (1.602 \times 10^{-19}) (500) = 0.04 \text{ S/cm.} \end{aligned}$$

### EXAMPLE 1.4

Determine the resistivity of germanium (a) in intrinsic condition at 300 K, (b) with donor impurity of 1 in  $10^7$ , (c) with acceptor impurity of 1 in  $10^8$ , and (d) with both the above impurities simultaneously. Given that for germanium at room temperature,  $n_i = 2.5 \times 10^{13}/\text{cm}^3$ ,  $\mu_n = 3,800 \text{ cm}^2/\text{V-Vs}$ ,  $\mu_p = 1800 \text{ cm}^2/\text{V-Vs}$ , and number of germanium atoms/ $\text{cm}^3 = 4.4 \times 10^{22}$ .

#### Solution

$$(a) \quad n = p = n_i = 2.5 \times 10^{13} \text{ cm}^{-3}$$

$$\begin{aligned} \text{Therefore, conductivity, } \sigma &= qn_i(\mu_n + \mu_p) \\ &= (1.602 \times 10^{-19})(2.5 \times 10^{13})(3800 + 1800) \\ &= 0.0224 \text{ S/cm} \end{aligned}$$

$$\text{Hence, resistivity, } \rho = \frac{1}{\sigma} = \frac{1}{0.0224} = 44.64 \Omega\text{-cm}$$

$$(b) \quad N_D = \frac{4.4 \times 10^{22}}{10^7} = 4.4 \times 10^{15} \text{ cm}^{-3}$$

Also,

$$n = N_D$$

$$\text{Therefore, } p = \frac{n_i^2}{n} = \frac{n_i^2}{N_D} = \frac{(2.5 \times 10^{13})^2}{4.4 \times 10^{15}} = 1.42 \times 10^{11} \text{ holes/cm}^3$$

Here, as  $n >> p$ ,  $p$  can be neglected.

$$\begin{aligned} \text{Therefore, conductivity, } \sigma &= nq\mu_n = N_D q \mu_n \\ &= (4.4 \times 10^{15}) (1.602 \times 10^{-19}) (3800) = 2.675 \text{ S/cm} \end{aligned}$$

$$\text{Hence, resistivity, } \rho = \frac{1}{\sigma} = \frac{1}{2.675} = 0.374 \Omega\text{-cm}$$

$$(c) \quad N_A = \frac{4.4 \times 10^{22}}{10^8} = 4.4 \times 10^{14} \text{ cm}^{-3}$$

Also,

$$p = N_A$$

$$\text{Therefore, } n = \frac{n_i^2}{p} = \frac{n_i^2}{N_A} = \frac{(2.5 \times 10^{13})^2}{4.4 \times 10^{14}} = 1.42 \times 10^{12} \text{ electron/cm}^3$$

Here, as  $p \gg n$ ,  $n$  may be neglected. Then

$$\begin{aligned} \text{Conductivity, } \sigma &= p q \mu_p = N_A q \mu_p \\ &= (4.4 \times 10^{14}) (1.602 \times 10^{-19}) (1800) = 0.1267 \text{ S/cm} \end{aligned}$$

$$\text{Hence, resistivity, } \rho = \frac{1}{\sigma} = \frac{1}{0.1267} = 7.89 \Omega\text{-cm}$$

(d) With both  $P$ - and  $N$ -type impurities present,

$$N_D = 4.4 \times 10^{15} \text{ cm}^{-3} \text{ and } N_A = 4.4 \times 10^{14} \text{ cm}^{-3}$$

Therefore, the net donor density  $N'_D$  is

$$N'_D = (N_D - N_A) = (4.4 \times 10^{15} - 4.4 \times 10^{14}) = 3.96 \times 10^{15} \text{ cm}^{-3}$$

Therefore, effective  $n = N'_D = 3.96 \times 10^{15} \text{ cm}^{-3}$

$$p = \frac{n_i^2}{N'_D} = \frac{(2.5 \times 10^{13})^2}{3.96 \times 10^{15}} = 1.578 \times 10^{11} \text{ cm}^{-3}$$

Here again,  $p \left( = \frac{n_i^2}{N'_D} \right)$  is very small compared with  $N'_D$  and may be neglected in calculating the effective conductivity.

$$\text{Therefore, } \sigma = N'_D q \mu_n = (3.96 \times 10^{15}) (1.6 \times 10^{-19}) (3800) = 2.408 \text{ S/cm}$$

$$\text{Hence, resistivity } \rho = \frac{1}{\sigma} = \frac{1}{2.408} = 0.415 \Omega\text{-cm}$$

### EXAMPLE 1.5

A sample of silicon at a given temperature  $T$  in intrinsic condition has a resistivity of  $25 \times 10^4 \Omega\text{-cm}$ . The sample is now doped to the extent of  $4 \times 10^{10}$  donor atoms/cm<sup>3</sup> and  $10^{10}$  acceptor atoms/cm<sup>3</sup>. Find the total conduction current density if an electric field of 4 V/cm is applied across the sample. Given that  $\mu_n = 1,250 \text{ cm}^2/\text{V-s}$ ,  $\mu_p = 475 \text{ cm}^2/\text{V-s}$  at the given temperature.

#### Solution

$$\sigma_i = q n_i (\mu_n + \mu_p) = \frac{1}{25 \times 10^4} \text{ S/cm}$$

$$\text{Therefore, } n_i = \frac{\sigma_i}{q(\mu_n + \mu_p)} = \frac{1}{(25 \times 10^4)(1.602 \times 10^{-19})(1250 + 475)} = 1.45 \times 10^{10} \text{ cm}^{-3}$$

$$\text{Net donor density } N_D (= n) = (4 \times 10^{10} - 10^{10}) = 3 \times 10^{10} \text{ cm}^{-3}$$

$$\text{Hence, } p = \frac{n_i^2}{N_D} = \frac{(1.45 \times 10^{10})^2}{3 \times 10^{10}} = 0.7 \times 10^{10} \text{ cm}^{-3}$$

Hence,

$$\begin{aligned}\sigma &= q(n\mu_n + p\mu_p) \\ &= (1.602 \times 10^{-19})(3 \times 10^{10} \times 1250 + 0.7 \times 10^{10} \times 475) \\ &= 6.532 \times 10^{-6} \text{ S/cm}\end{aligned}$$

Therefore, total conduction current density,

$$J = \sigma E = 6.532 \times 10^{-6} \times 4 = 26.128 \times 10^{-6} \text{ A/cm}^2$$

### EXAMPLE 1.6

Find the concentration (densities) of holes and electrons in *N*-type silicon at 300 K, if the conductivity is 300 S/cm. Also find these values for *P*-type silicon. Given that for silicon at 300 K,  $n_i = 1.5 \times 10^{10}/\text{cm}^3$ ,  $\mu_n = 1,300 \text{ cm}^2/\text{V-s}$  and  $\mu_p = 500 \text{ cm}^2/\text{V-s}$ .

#### Solution

##### (a) Concentration in *N*-type silicon

The conductivity of *N*-type silicon is  $\sigma = qn\mu_n$

$$\text{Concentration of electrons, } n = \frac{\sigma}{q\mu_n} = \frac{300}{(1.602 \times 10^{-19})(1300)} = 1.442 \times 10^{18} \text{ cm}^{-3}$$

$$\text{Hence, concentration of holes, } p = \frac{n_i^2}{n} = \frac{(1.5 \times 10^{10})^2}{1.442 \times 10^{18}} = 1.56 \times 10^2 \text{ cm}^{-3}$$

##### (b) Concentration in *P*-type silicon

The conductivity of *P*-type silicon is  $\sigma = qp\mu_p$

$$\text{Hence, concentration of holes } p = \frac{\sigma}{q\mu_p} = \frac{300}{(1.602 \times 10^{-19})(500)} = 3.75 \times 10^{18} \text{ cm}^{-3}$$

$$\text{and concentration of electrons, } n = \frac{n_i^2}{p} = \frac{(1.5 \times 10^{10})^2}{3.75 \times 10^{18}} = 0.6 \times 10^2 \text{ cm}^{-3}$$

## 1.7 HALL EFFECT

When a transverse magnetic field  $B$  is applied to a specimen (thin strip of metal or semiconductor) carrying current  $I$ , an electric field  $E$  is induced in the direction perpendicular to both  $I$  and  $B$ . This phenomenon is known as the *Hall effect*.

A Hall-effect measurement experimentally confirms the validity of the concept that it is possible for two independent types of charge carriers, electrons and holes, to exist in a semiconductor.

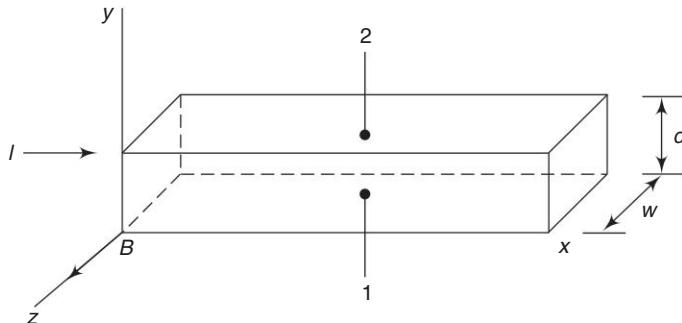
The schematic arrangement of the semiconductor, the magnetic field and the current flow pertaining to the Hall effect are shown in Fig. 1.8. Under the equilibrium condition, the electric field intensity,  $E$ , due to the Hall effect must exert a force on the carrier of charge,  $q$ , which just balances the magnetic force, i.e.,

$$qE = Bqv_d$$

where  $v_d$  is the drift velocity. Also, the electric field intensity due to Hall effect is

$$E = \frac{V_H}{d}$$

where  $d$  is the distance between surfaces 1 and 2, and  $V_H$  is the Hall voltage appearing between surfaces 1 and 2. In an  $N$ -type semiconductor, the current is carried by electrons and these electrons will be forced downward towards side 1 which becomes negatively charged with respect to side 2.



**Fig. 1.8** Schematic arrangement to observe the Hall effect

The current density ( $J$ ) is related to charge density ( $\rho$ ) by

$$J = \rho v_d$$

Further, the current density ( $J$ ) is related to current ( $I$ ) by

$$J = \frac{I}{\text{Area}} = \frac{I}{wd}$$

where  $w$  is the width of the specimen in the direction of magnetic field ( $B$ ).

Combining the above relations, we get

$$V_H = Ed = B v_d d = \frac{BJd}{\rho} = \frac{BI}{\rho w}$$

The Hall coefficient,  $R_H$ , is defined by

$$R_H = \frac{1}{\rho}$$

so that  $V_H = \frac{R_H}{w} BI$ . A measurement of the Hall coefficient  $R_H$  determines not only the sign of the charge carriers but also their concentration. The Hall coefficient for a  $P$ -type semiconductor is positive, whereas it is a negative for an  $N$ -type semiconductor. This is true because the Hall voltage in a  $P$ -type semiconductor is of opposite polarity to that in an  $N$ -type semiconductor.

The advantage of Hall-effect transducers is that they are non-contact devices with high resolution and small size.

**Applications** The Hall effect is used to find whether a semiconductor is  $N$ - or  $P$ -type and to determine the carrier concentration. If the terminal 2 becomes positively charged with respect to terminal 1, the semiconductor must be  $N$ -type and  $\rho = nq$ , where  $n$  is the electron concentration. On the other hand, if the polarity of  $V_H$  is positive at terminal 1 with respect to terminal 2, the semiconductor must be  $P$ -type and  $\rho = pq$ , where  $p$  is the hole concentration.

The mobility ( $\mu$ ) can also be calculated with simultaneous measurement of the conductivity ( $\sigma$ ). The conductivity and the mobility are related by the equation  $\sigma = \rho\mu$  or  $\mu = \sigma R_H$ .

Therefore, the conductivity for  $N$ -type semiconductor is  $\sigma = nq\mu_n$  and for  $P$ -type semiconductor,  $\sigma = pq\mu_p$ , where  $\mu_n$  is the electron mobility and  $\mu_p$  is the hole mobility.

Thus, if the conductivity of a semiconductor is measured along with  $R_H$ , then mobility can be determined from the following relations.

$$\text{For } N\text{-type semiconductor, } \mu_n = \frac{\sigma}{nq} = \sigma R_H$$

$$\text{and for } P\text{-type semiconductor, } \mu_p = \frac{\sigma}{pq} = \sigma R_H$$

Since  $V_H$  is proportional to  $B$  for a given current  $I$ , Hall effect can be used to measure the ac power and the strength of magnetic field and sense the angular position of static magnetic fields in a magnetic field meter. It is also used in an instrument called Hall-effect multiplier which gives the output proportional to the product of two input signals. If  $I$  is made proportional to one of the inputs and  $B$  is made proportional to the second signal, then from the equation,  $V_H = \frac{BI}{\rho w}$ ,  $V_H$  will be proportional to the product of two inputs. Hall devices

for such applications are made from a thin wafer or film of indium antimonide (InSb) or indium arsenide. As the material has a very high electron mobility, it has high Hall coefficient and high sensitivity.

An electrical current can be controlled by a magnetic field because the magnetic field changes the resistances of some elements with which it comes in contact. In the magnetic bubble memory, while read-out, the Hall effect element is passed over the bubble. Hence, a change in current of the circuit will create, say, a *one*. If there is no bubble, there will be a *zero* and there will be no current change in the output circuit. The read-in device would have an opposite effect, wherein the Hall device creates a magnetic field when supplied with a pulse of current. This, in turn, creates a little domain and then a magnetic bubble is created.

Some of the other applications are in measurement of velocity, rpm, sorting, limit sensing, and non-contact current measurements.

### EXAMPLE 1.7

An  $N$ -type semiconductor has a Hall coefficient of  $200 \text{ cm}^3/\text{C}$  and its conductivity is  $10 \text{ S/m}$ . Find its electron mobility.

**Solution** Given  $R_H = 200 \text{ cm}^3/\text{C}$  and  $\sigma = 10 \text{ S/m}$ .

Therefore, the electron mobility,  $\mu_n = \sigma R_H = 10 \times 200 = 2000 \text{ cm}^2/\text{V-s}$

### EXAMPLE 1.8

The conductivity of an  $N$ -type semiconductor is  $10 \text{ S/m}$  and its electron mobility is  $50 \times 10^{-4} \text{ m}^2/\text{V-s}$ . Determine the electron concentration.

**Solution** Given  $\sigma = 10 \text{ s/m}$  and  $\mu_n = 50 \times 10^{-4} \text{ m}^2/\text{V-s}$ .

We know that the electron mobility,  $\mu_n = \frac{\sigma}{nq}$

Therefore, the electron concentration,

$$n = \frac{\sigma}{\mu q} = \frac{10}{50 \times 10^{-4} \times 1.6 \times 10^{-19}} = 12.5 \times 10^{21} \text{ m}^{-3}$$

### EXAMPLE 1.9

A current of 20 A is passed through a thin metal strip, which is subjected to a magnetic flux density of 1.2 Wb/m<sup>2</sup>. The magnetic field is directed perpendicular to the current. The thickness of the strip in the direction of the magnetic field is 0.5 mm. The Hall voltage is 60 V. Find the electron density.

**Solution** Given:  $I = 20 \text{ A}$ ,  $B = 1.2 \text{ Wb/m}^2$ ,  $V_H = 60 \text{ V}$  and  $w = 0.5 \text{ mm}$

We know that the number of conduction electrons, i.e., electron density,

$$n = \frac{BI}{V_H q w} = \frac{1.2 \times 20}{60 \times 1.6 \times 10^{-19} \times 0.5 \times 10^{-3}} = 5 \times 10^{21} \text{ m}^{-3}$$

## 1.8 CONTINUITY EQUATION

The fundamental law governing the flow of charge is called the *continuity equation*. The continuity equation as applied to semiconductors describes how the carrier concentration in a given elemental volume of the crystal varies with time and distance. The variation in density is attributable to two basic causes, viz., (i) the rate of generation and loss by recombination of carriers within the element, and (ii) drift of carriers into or out of the element. The continuity equations enable us to calculate the excess density of electrons or holes in time and space.

As shown Fig. 1.9, consider an infinitesimal N-type semiconductor bar of volume of area  $A$  and length  $dx$  and the average minority carrier (hole) concentration  $p$ , which is very small compared to the density of majority carriers. At time  $t$ , if minority carriers (holes) are injected, the minority current entering the volume at  $x$  is  $I_p$  and leaving at  $x + dx$  is  $I_p + dI_p$  which is predominantly due to diffusion. The minority carrier concentration injected into one end of the semiconductor bar decreases exponentially, with distance into the specimen, as a result of diffusion and recombination. Here,  $dI_p$  is the decrease in number of coulomb per second within the volume.

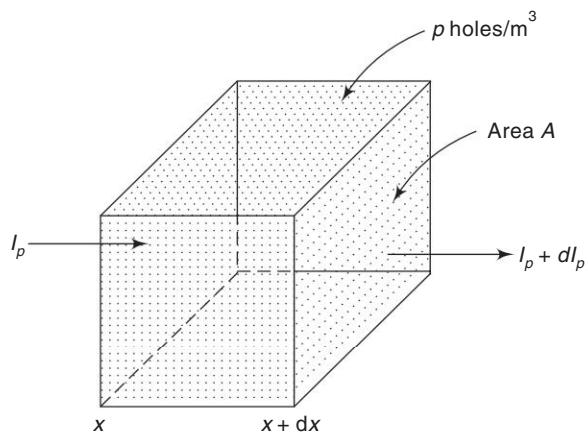


Fig. 1.9 Relating to continuity equation

Since the magnitude of the carrier charge is  $q$ , then  $\frac{dI_p}{p}$  equals the decrease in the number of holes per second within the elemental volume  $A \propto x$ . As the current density  $J_p = \frac{I_p}{A}$ , we have

$$\frac{1}{Aq} \cdot \frac{dI_p}{dx} = \frac{1}{q} \cdot \frac{dJ_p}{dx} = \text{decrease in hole concentration per second, due to current } I_p$$

We know that an increase in number of holes per unit volume per second is given by  $G = p_o/\tau_p$  due to thermal generation. Further, there is a decrease of holes per unit volume per second given by  $R = p/\tau_p$  due to recombination but charge can neither be created nor destroyed. Hence, increase in holes per unit volume per second,  $dp/dt$ , must equal the algebraic sum of all the increases in hole concentration. Thus,

$$\frac{\partial p}{\partial t} = -\frac{p - p_o}{\tau_p} - \frac{1}{q} \frac{\partial J_p}{\partial x}$$

where

$$J_p = -qD_p \frac{dp}{dx} + qp\mu_p E$$

Therefore,

$$\frac{\partial p}{\partial t} = -\frac{p - p_o}{\tau_p} + D_p \frac{d^2 p}{dx^2} - \mu_p \frac{d(pE)}{dx}$$

This is the *continuity equation* or *equation of conservation of charge* for holes stating the condition of dynamic equilibrium for the density of mobile carrier holes. Here, partial derivatives have been used since both  $p$  and  $J_p$  are functions of both  $t$  and  $x$ .

Similarly, the continuity equation for electrons states the condition of dynamic equilibrium for the density of mobile carrier electrons and is given by

$$\frac{\partial n}{\partial t} = \frac{n_o - n}{\tau_n} - \frac{1}{q} \frac{\partial J_n}{\partial x}$$

where

$$J_n = -qD_n \frac{dn}{dx} + qn\mu_n E$$

Therefore,

$$\frac{\partial n}{\partial t} = -\frac{n - n_o}{\tau_n} + D_n \frac{d^2 n}{dx^2} - \mu_n \frac{d(nE)}{dx}$$

We now consider three special cases of the continuity equation.

**Concentration Independent of Distance with Zero Electric Field** For this special case, the continuity equation can be changed into

$$\frac{\partial p}{\partial t} = -\frac{p - p_0}{\tau_p}$$

Solving the above equation, we get

$$p - p_o = A_1 e^{-t/\tau_p} \text{ where } A \text{ is a constant}$$

**Concentration Independent of Time with Zero Electric Field** For this special case, the continuity equation can be changed into

$$0 = -\frac{p - p_o}{\tau_p} + D_p \frac{d^2 p}{dx^2}$$

$$\frac{d^2 p}{dx^2} = \frac{p - p_o}{\tau_p D_p}$$

Solving this equation, we get

$$p - p_o = A_1 e^{-x/L_p} + A_2 e^{x/L_p}$$

where  $A_1$  and  $A_2$  are constants.

$$L_p = \sqrt{D_p \tau_p} = \text{diffusion length for holes}$$

### **Concentration varies Sinusoidally with Time and with Zero Electric Field**

Let

$$P(x, t) = P(x) e^{j\omega t}$$

For this special case, the continuity equation can be changed into

$$j\omega P(x) = -\frac{P(x)}{\tau_p} + D_p \frac{d^2 P(x)}{dx^2}$$

$$\frac{d^2 p}{dx^2} = \frac{(1 + j\omega\tau_p)}{L_p^2} P$$

$$\text{At } \omega = 0, \quad \frac{d^2 p}{dx^2} = \frac{P}{L_p^2}$$

The above equation is the same as that of the second special case.

**Minority Carrier Injection in Homogeneous Semiconductors** Consider the semiconductor bar shown in Fig. 1.7(a). This bar is uniformly doped with donor atoms so that the charge concentration  $n = N_D$  is uniform throughout the bar on which radiation falls on one end of the bar at  $x = 0$ . Near the illuminated surface, the bound electrons in the covalent bonds capture some of the photons. This energy transfer results in breaking of covalent bonds and generation of hole-electron pairs.

The minority carrier (hole) concentration  $P$  is very small compared with the doping level, i.e.,  $P \ll n$ . The condition  $p = P + p_o \ll n$  which states that the minority concentration is much smaller than the majority concentration is called the low-level injection. The controlling differential equation for  $p$  is

$$\frac{d^2 p}{dx^2} = \frac{p - p_0}{D_p \tau_p}$$

The diffusion length for holes  $L_p$  is given by

$$L_p = \sqrt{D_p \tau_p}$$

The differential equation for the injected concentration  $P = p - p_0$  becomes

$$\frac{d^2 p}{dx^2} = \frac{P}{L_p^2}$$

The solution of the equation is

$$P(x) = A_1 e^{-x/AL_p} + A_2 e^{x/AL_p}$$

when  $x \rightarrow \infty$ ,  $A_2 = 0$ . At  $x = 0$ , the injected concentration  $P(0)$  to satisfy this boundary condition,  $A_1 = P(0)$ .

Therefore,

$$P(x) = P(0) e^{-x/L_p} = p(x) - p_o$$

Here, the hole concentration decreases exponentially with distance as shown in Fig. 1.7(b).

**Diffusion Current** The minority (hole) diffusion current is  $I_p = AJ_p$ , where  $A$  is the area of cross section of the bar. Therefore,

$$I_p(x) = \frac{Aq D_p P(0)}{L_p} e^{-x/L_p} = \frac{Aq D_p}{L_p} (p(0) - p_o) e^{-x/L_p}$$

This current decreases exponentially with distance  $x$  as that of minority carrier concentration.

The majority (electron) diffusion current is

$$Aq D_n \frac{dn}{dx} = Aq D_n \frac{dp}{dx} = -\frac{D_n}{D_p} I_p$$

where  $I_p = -Aq D_n \frac{dp}{dx}$ . The magnitude of ratio of majority to minority diffusion current is  $D_n/D_p \approx 3$  for Si and 2 for Ge.

**Drift Current** For an open-circuit semiconductor bar, the sum of the hole and electron currents should be zero everywhere. Therefore, a majority (electron) drift current  $I_{nd}$  exists such that

$$I_p + \left( I_{nd} - \frac{D_n I_p}{D_p} \right) = 0$$

$$\text{Therefore, } I_{nd} = \left( \frac{D_n}{D_p} - 1 \right) I_p$$

The hole drift current  $I_{pd}$  is given by

$$I_{pd} = Aqp \mu_p E = \frac{p}{n} \frac{\mu_p}{\mu_n} \left( \frac{D_n}{D_p} - 1 \right) I_p$$

$$\text{where the electric field, } E = \frac{1}{Aqn \mu_n} \left( \frac{D_n}{D_p} - 1 \right) I_p$$

Here as  $p \ll n$ , we have  $I_{pd} \ll I_p$ , i.e., the hole-drift current is negligible compared to the hole-diffusion current.

## 1.9 LAW OF JUNCTION

Let us now derive the expression for the total current as a function of applied voltage assuming that the width of the depletion region is zero. When a forward bias is applied to a diode, holes are injected from the  $P$ -side into the  $N$ -side. Due to this, the concentration of holes in the  $N$ -side ( $p_n$ ) is increased from its thermal equilibrium value ( $p_{n0}$ ) and injected hole concentration [ $P_n(x)$ ] decreases exponentially with respect to the distance ( $x$ ).

$$P_n(x) = p_n - p_{n0} = P_n(0) e^{-x/L_p}$$

where  $L_p$  is the diffusion length for holes in the  $N$ -material.

$$p_n(x) = p_{n0} + P_n(0)e^{-x/L_p} \quad (1.16)$$

Injected hole concentration at  $x = 0$  is

$$P_n(0) = p_n(0) - p_{n0} \quad (1.17)$$

The several components of hole concentration in the  $N$ -side of a forward-biased diode are shown in Fig. 1.6, in which the density  $p_n(x)$  decreases exponentially with the distance ( $x$ ).

Let  $p_p$  and  $p_n$  be the hole concentrations at the edges of the space charge in the  $P$ - and  $N$ -sides, respectively. Let  $V_B$  ( $= V_0 - V$ ) be the effective barrier potential across the depletion layer. Then

$$p_p = P_n e^{V_B/V_T} \quad (1.18)$$

where  $V_T$  is the volt-equivalent of temperature.

This is the Boltzmann's relation of kinetic gas theory. This equation is valid as long as the hole current is small compared to diffusion or drift currents. This condition is called *low-level-injection*.

Under open-circuit condition (i.e.,  $V = 0$ ),  $p_p = p_{p0}$ ,  $p_n = p_{n0}$  and  $V_B = V_0$ . Equation (1.18) can be changed into

$$p_{p0} = p_{n0} e^{V_0/V_T} \quad (1.19)$$

Under forward-bias condition, let  $V$  be the applied voltage; then the effective barrier voltage

$$V_B = V_0 - V$$

The hole concentration throughout the  $P$ -side is constant and equal to the thermal equilibrium value ( $p_p = p_{p0}$ ). The hole concentration varies exponentially with distance into the  $N$ -side.

At  $x = 0$ ,  $p_n = p_n(0)$

Equation (1.18) can be changed into

$$p_{p0} = p_n(0) e^{(V_0-V)/V_T} \quad (1.20)$$

Comparing Eqs (1.19) and (1.20),

$$p_n(0) = p_{n0} e^{V/V_T}$$

This boundary condition is called the *law of the junction*. Substituting this into Eq. (1.17), we get

$$P_n(0) = p_{n0} (e^{V/V_T} - 1) \quad (1.21)$$

The diffusion-hole current in the  $N$ -side is

$$\begin{aligned} I_{pn}(x) &= -Aq D_p \frac{dp_n(x)}{dx} \\ &= -Aq D_p \frac{d}{dx} \left[ p_{n0} + P_n(0) e^{-x/L_p} \right] \\ &= \frac{Aq D_p P_n(0)}{L_p} e^{-x/L_p} \end{aligned}$$

From this equation, it is evident that the injected hole current decreases exponentially with distance.

**Forward Currents** The hole current crossing the junction into the *N*-side with  $x = 0$  is

$$I_{pn}(0) = \frac{AqD_p P_n(0)}{L_p} = \frac{AqD_p p_{n0}}{L_p} (e^{V/V_T} - 1)$$

The electron current crossing the junction into the *P*-side with  $x = 0$  is

$$I_{np}(0) = \frac{AqD_n N_p(0)}{L_n} = \frac{AqD_n n_{p0}}{L_n} (e^{V/V_T} - 1)$$

The total diode current,

$$I = I_{pn}(0) + I_{np}(0) = I_o (e^{V/V_T} - 1)$$

where  $I_o = \frac{AqD_p p_{n0}}{L_p} + \frac{AqD_n n_{p0}}{L_n}$  = reverse saturation current.

If we consider carrier generation and recombination in the space-charge region, the general equation of the diode current is approximately given by

$$I = I_o [e^{(V/\eta V_T)} - 1]$$

where  $V$  = external voltage applied to the diode and  $\eta$  = a constant, 1 for germanium and 2 for silicon.

**Reverse Saturation Current** We know that  $p_n = \frac{n_i^2}{N_D}$  and  $n_p = \frac{n_i^2}{N_A}$ . Applying these relationships in

the above equation of reverse saturation current,  $I_o$ , we get

$$I_o = Aq \left[ \frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right] n_i^2$$

where  $n_i^2 = A_o T^3 e^{-E_{Go}/kT} = A_o T^3 e^{-V_{Go}/V_T}$ , where  $V_{Go}$  is a voltage which is numerically equal to the forbidden-gap energy  $E_{Go}$  in electronvolt.

For a germanium diode, the diffusion constants  $D_p$  and  $D_n$  vary approximately inversely proportional to  $T$ . Hence, the temperature dependence of  $I_o$  is

$$I_o = K_1 T^2 e^{\frac{-V_{Go}}{V_T}}$$

where  $K_1$  is a constant independent of temperature.

For a silicon diode,  $I_o$  is proportional to  $n_i$  instead of  $n_i^2$ . Hence,

$$I_o = K_2 T^{\frac{3}{2}} e^{\frac{-V_{Go}}{2V_T}}$$

where  $K_2$  is a constant independent of temperature.

## 1.10 FERMI DIRAC FUNCTION

An electron inside the metal must possess an energy level that is at least greater than the surface barrier energy  $E_B$ , so as to escape to a higher level. It is, therefore, important to know about the energies possessed by the electrons in a metal. This is given by the energy-distribution function.

**Energy Density** The distribution in energy of the free electrons in a metal is given by

$$dn = \rho dE$$

where  $dn$  is the number of electrons per cubic metre whose energies lie in the energy interval  $dE$ , and  $\rho$  is the density of electrons in a given energy interval.

It is assumed that there are no potential variations within the metal, since only free electrons are considered. Hence, there must be the same number of electrons in each cubic metre of the metal. That is, the density in space (electrons per cubic metre) is a constant. However, there will be electrons having all possible energies within each unit volume of the metal. This distribution in energy is expressed by

$$\rho = f(E) N(E)$$

where  $N(E)$  is the density of states in the conductance band, and  $f(E)$  is the probability that a quantum state with energy ' $E$ ' is occupied by an electron. Therefore,

$$N(E) = \gamma E^{\frac{1}{2}}$$

Here,  $\gamma$  is a constant defined by

$$\gamma = \frac{4\pi}{h^3} \left(2m\right)^{\frac{3}{2}} \left(1.602 \times 10^{-19}\right)^{\frac{3}{2}} = 6.82 \times 10^{27}$$

where the dimensions of  $\gamma$  are  $(m^{-3}) (eV)^{-\frac{3}{2}}$ ,  $m$  is the mass of the electron in kg, and  $h$  is the Planck's constant in joule-second.

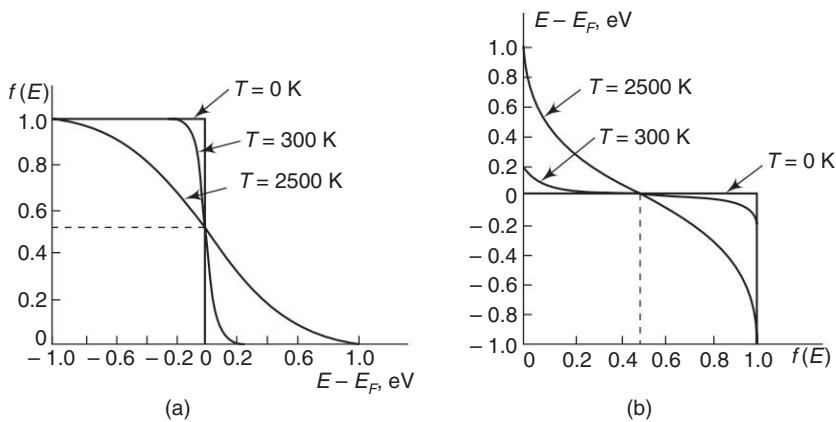
**Fermi-Dirac Function** The Fermi-Dirac probability function  $f(E)$  specifies the fraction of all states at energy  $E$  (in eV) occupied under conditions of thermal equilibrium. From quantum physics,

$$f(E) = \frac{1}{1 + e^{(E - E_F)/kT}}$$

where  $k$  is the Boltzmann constant in eV/K,  $T$  is the temperature in K, and  $E_F$  is the Fermi level or characteristic energy for the crystal in eV.

The Fermi level represents the energy state with 50 percent probability of being filled if no forbidden band exists. That is, if  $E = E_F$  then  $f(E) = \frac{1}{2}$  for any value of temperature.

The plots of  $f(E)$  vs  $(E - E_F)$  and  $(E - E_F)$  vs  $f(E)$  are shown in Fig. 1.10(a) and (b) respectively for  $T = 0$  K and larger values of temperature.



**Fig. 1.10** Fermi-Dirac distribution function  $f(E)$  gives the probability that a state of energy  $E$  is occupied

At  $T = 0$  K, the following conditions exist:

- If  $E > E_F$ , the exponential term becomes infinite and  $f(E) = 0$ . Consequently, there is no probability of finding an occupied quantum state of energy greater than  $E_F$  at absolute zero temperature.
- If  $E < E_F$ , the exponential becomes zero and  $f(E) = 1$ . All quantum levels with energies less than  $E_F$  will be occupied at  $T = 0$  K.

From these equations, we get at absolute zero temperature,

$$\rho = \begin{cases} \gamma E^{\frac{1}{2}}; & \text{for } E < E_F \\ 0 & \text{for } E > E_F \end{cases}$$

It implies that there are no electrons at 0 K which have energies in excess of  $E_F$ . Therefore, the Fermi energy is the maximum energy that any electron may possess at absolute zero temperature.

The relationship given by the above equation is called the *completely degenerate energy distribution function*. In fact, all particles should have zero energy at 0 K. Based on Pauli's exclusion principle, it is also to be mentioned that since no two electrons have the same set of quantum numbers, not all the electrons can have the same energy even at 0 K.

**Fermi Level** An expression for  $E_F$  may be obtained on the basis of the completely degenerate function. The total number of free electrons is given by

$$n = \int_0^{E_F} \gamma E^{\frac{1}{2}} dE = \frac{2}{3} \gamma E_F^{\frac{3}{2}}$$

i.e., 
$$E_F = \left( \frac{3n}{2\gamma} \right)^{\frac{2}{3}}, \text{ where } \gamma = 6.82 \times 10^{27}$$

Therefore, 
$$E_F = 3.64 \times 10^{-19} n^{\frac{2}{3}}$$

Since the density of free electrons,  $n$ , varies from metal to metal,  $E_F$  will also vary among metals. Generally, the numerical value of  $E_F$  is less than 10 eV.

## 1.11 FERMI LEVEL IN INTRINSIC AND EXTRINSIC SEMICONDUCTORS

To calculate the conductivity of a semiconductor, the concentration of free electrons  $n$  and the concentration of free holes  $p$  must be known.

$$dn = N(E) f(E) dE$$

where  $dn$  represents the number of conduction electrons per cubic metre whose energies lie between  $E$  and  $E + dE$ , and  $N(E)$  is the density of states. In a semiconductor, the lowest energy in the conduction band is  $E_C$  and hence,

$$N(E) = \gamma(E - E_C)^{1/2}$$

The Fermi–Dirac probability function  $f(E)$  is given by

$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}}$$

where  $E_F$  is the Fermi level or characteristic energy for the crystal in eV.

The concentration of electrons in the conduction band is,

$$n = \int_{E_C}^{\infty} N(E) f(E) dE$$

For  $E \geq E_C$ ,  $E - E_F \gg kT$ ,

$$f(E) = e^{-(E-E_F)/kT}$$

$$\text{and } n = \int_{E_C}^{\infty} \gamma(E - E_C)^{1/2} e^{-(E-E_F)/kT} dE$$

Substitute  $(E - E_C) = x^2$ , i.e.,  $E = x^2 + E_C$  and  $dE = 2xdx$

At  $x = 0$ ,  $E = E_c$ ,

At  $x = \infty$ ,  $E = \infty$

$$\text{Therefore, } n = \int_0^{\infty} \gamma x e^{\left(-\frac{x^2+E_C-E_F}{kT}\right)} [2xdx]$$

$$= 2\gamma e^{\left(\frac{E_C-E_F}{kT}\right)} \int_0^{\infty} x^2 e^{-\frac{x^2}{kT}} dx$$

$$\text{We know that, } \int_0^{\infty} x^{2n} e^{-x^2/a^2} dx = \sqrt{\pi} \frac{2n!}{n!} \left(\frac{a}{2}\right)^{2n+1}$$

Here,  $n = 1$  and  $a = \sqrt{kT}$

Therefore,

$$n = 2\gamma e^{-\left(\frac{E_C - E_F}{kT}\right)} \times 2\sqrt{\pi} \left(\frac{\sqrt{kT}}{2}\right)^3$$

Substituting  $\gamma = \frac{4\pi}{h^3} (2m_n)^{\frac{3}{2}} (1.602 \times 10^{-19})^{\frac{3}{2}}$ , we have

$$\begin{aligned} n &= 2 \times \frac{4\pi}{h^3} (2m_n)^{\frac{3}{2}} (1.602 \times 10^{-19})^{\frac{3}{2}} \times \frac{\sqrt{\pi} (kT)^{\frac{3}{2}}}{4} \times e^{-\left(\frac{E_C - E_F}{kT}\right)} \\ &= 2 \left( \frac{2m_n \pi k T}{h^2} \right)^{\frac{3}{2}} \times (1.602 \times 10^{-19})^{\frac{3}{2}} e^{-\left(\frac{E_C - E_F}{kT}\right)} = N_C e^{-\left(\frac{E_C - E_F}{kT}\right)} \end{aligned}$$

where  $N_C = 2 \left( \frac{2\pi m_n k t}{h^2} \right)^{\frac{3}{2}} (1.602 \times 10^{-19})^{\frac{3}{2}}$ , where  $m_n$  is the effective mass of an electron.

When the maximum energy in the valence band is  $E_V$ , the density of states is given by

$$N(E) = \gamma(E_V - E)^{1/2}$$

The Fermi function of a hole is  $[1 - f(E)]$  and is given by

$$1 - f(E) = \frac{e^{(E - E_F)/kT}}{1 + e^{(E - E_F)/kT}} = e^{-(E_F - E)/kT}$$

where  $E_F - E \gg kT$  for  $E \leq E_V$ .

The concentration of holes in the valence band is,

$$p = \int_{-\infty}^{E_V} \gamma(E_V - E)^{1/2} e^{-(E_F - E)/kT} dE$$

This integral evaluates to

$$p = N_V e^{-(E_F - E_V)/kT}$$

where  $N_V = 2 \left( \frac{2\pi m_p k T}{h^2} \right)^{3/2} (1.602 \times 10^{-19})^{3/2}$ , where  $m_p$  is the effective mass of a hole.

**Fermi Level in an Intrinsic Semiconductor** In the case of an intrinsic material, the crystal must be electrically neutral.

$$n_i = p_i$$

Therefore,  $N_C e^{-(E_C - E_F)/kT} = N_V e^{-(E_F - E_V)/kT}$

Taking logarithm on both sides,

$$\ln \frac{N_C}{N_V} = \frac{E_C + E_V - 2E_F}{kT}$$

$$E_F = \frac{E_C + E_V}{2} - \frac{kT}{2} \ln \frac{N_C}{N_V}$$

If the effective masses of a free electron and hole are the same,

$$N_C = N_V$$

Then,  $E_F = \frac{E_C + E_V}{2}$

From the above equation, Fermi level is present at the centre of the forbidden energy band.

**Donor and Acceptor Impurities** If a pentavalent substance (antimony, phosphorous, or arsenic) is added as an impurity to pure germanium, four of the five valence electrons of the impurity atoms will occupy covalent bonds and the fifth electron will be available as a carrier of current. These impurities donate excess electron carriers and are, hence, called *donor* or *N-type* impurities.

If a trivalent impurity (boron, gallium, or indium) is added to an intrinsic semiconductor, only three covalent bonds are filled, and the vacancy in the fourth bond constitutes a hole. These impurities are known as *acceptor* or *P-type* impurities.

**Fermi Level in a Semiconductor having Impurities** The Fermi level in an *N*-type material is given by

$$E_F = E_C - kT \ln \frac{N_C}{N_D}$$

where  $N_D = N_C e^{-(E_C - E_F)/kT}$ , the concentration of donor atoms.

The Fermi level in a *P*-type material is given by

$$E_F = E_V + kT \ln \frac{N_V}{N_A}$$

where  $N_A = N_V e^{-(E_F - E_V)/kT}$ , the concentration of acceptor atoms. The change in the position of Fermi level in *N*- and *P*-type semiconductors is shown in Fig. 1.11.

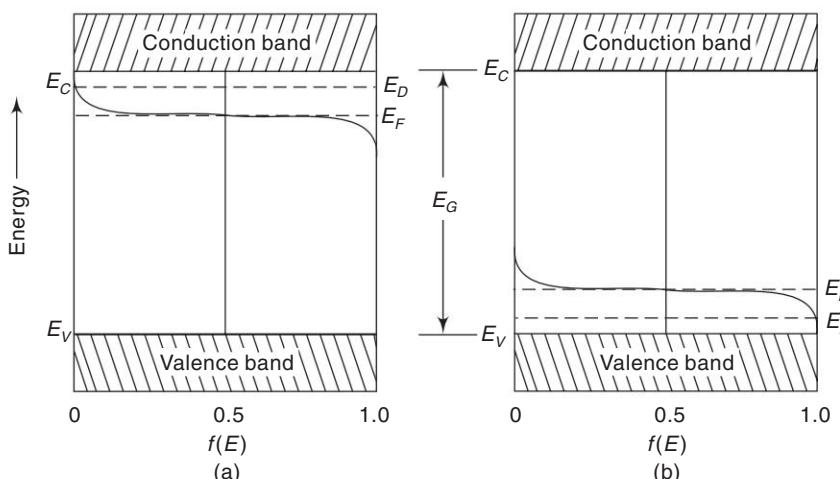


Fig. 1.11 Positions of Fermi level in (a) *N*-type, and (b) *P*-type semiconductors

**Movement of  $E_F$  with Temperature** In an  $N$ -type semiconductor, as the temperature  $T$  increases, more electron-hole pairs are formed. At a very high temperature  $T$ , the concentration of thermally generated electrons in the conduction band will be far greater than the concentration of donor electrons. In such a case, as concentration of electrons and holes become equal, the semiconductor becomes essentially intrinsic and  $E_F$  returns to the middle of the forbidden energy gap. Hence, it is concluded that as the temperature of the  $P$ -type and  $N$ -type semiconductor increases,  $E_F$  progressively moves towards the middle of the forbidden energy gap.

### EXAMPLE 1.10

In an  $N$ -type semiconductor, the Fermi level is 0.3 eV below the conduction level at a room temperature of 300 K. If the temperature is increased to 360 K, determine the new position of the Fermi level.

**Solution** The Fermi level in an  $N$ -type material is given by

$$E_F = E_C - kT \ln \frac{N_C}{N_D}$$

Therefore,  $(E_C - E_F) = kT \ln \frac{N_C}{N_D}$

At  $T = 300$  K,  $0.3 = 300k \ln \frac{N_C}{N_D}$  (1)

Similarly,  $E_C - E_{F1} = 360k \ln \frac{N_C}{N_D}$  (2)

Equation (2) divided by Eq. (1) gives

$$\frac{E_C - E_{F1}}{0.3} = \frac{360}{300}$$

Therefore,  $E_C - E_{F1} = \frac{360}{300} \times 0.3 = 0.36$  eV

Hence, the new position of the Fermi level lies 0.36 eV below the conduction level.

### EXAMPLE 1.11

In a  $P$ -type semiconductor, the Fermi level is 0.3 eV above the valence band at a room temperature of 300 K. Determine the new position of the Fermi level for temperatures of (a) 350 K, and (b) 400 K.

**Solution** The Fermi level in a  $P$ -type material is given by

$$E_F = E_V + kT \ln \frac{N_V}{N_A}$$

Therefore,  $(E_F - E_V) = kT \ln \frac{N_V}{N_A}$

At  $T = 300$  K,  $0.3 = 300k \ln \frac{N_V}{N_A}$

(a) At  $T = 350$  K,  $(E_{F1} - E_V) = 350 k \ln \frac{N_V}{N_A}$

Hence, from the above equation

$$\frac{E_{F1} - E_V}{0.3} = \frac{350}{300}$$

Therefore,  $E_{F1} - E_V = \frac{350}{300} \times 0.3 = 0.35$  eV

(b) At  $T = 400$  K,  $(E_{F2} - E_V) = 400 k \ln \frac{N_V}{N_A}$

Hence, from the above equation,

$$\frac{E_{F2} - E_V}{0.3} = \frac{400}{300}$$

Therefore,  $E_{F2} - E_V = \frac{400}{300} \times 0.3 = 0.4$  eV

### EXAMPLE 1.12

In an  $N$ -type semiconductor, the Fermi level lies 0.2 eV below the conduction band. Find the new position of the Fermi level if the concentration of donor atoms is increased by a factor of (a) 4, and (b) 8. Assume  $kT = 0.025$  eV.

**Solution** In an  $N$ -type material, the concentration of donor atoms is given by

$$N_D = N_C e^{-(E_C - E_F)/kT}$$

Let initially,  $N_D = N_{DO}$ ,  $E_F = E_{FO}$  and  $E_C - E_{FO} = 0.2$  eV

Therefore,  $N_{DO} = N_C e^{-0.2/0.025} = N_C e^{-8}$

(a) When  $N_D = 4N_{DO}$  and  $E_F = E_{F1}$  then

$$4N_{DO} = N_C e^{-(E_C - E_{F1})/0.025} = N_C e^{-40(E_C - E_{F1})}$$

Therefore,  $4 \times N_C e^{-8} = N_C e^{-40(E_C - E_{F1})}$

Therefore,  $4 = e^{-40(E_C - E_{F1}) + 8}$

Taking natural logarithm on both sides, we get

$$\ln 4 = -40(E_C - E_{F1}) + 8$$

$$1.386 = -40(E_C - E_{F1}) + 8$$

Therefore,  $E_C - E_{F1} = 0.165$  eV

(b) When  $N_D = 8N_{DO}$  and  $E_F = E_{F2}$  then

$$\ln 8 = -40(E_C - E_{F2}) + 8$$

$$2.08 = -40(E_C - E_{F2}) + 8$$

Therefore,  $E_C - E_{F2} = 0.148$  eV

**EXAMPLE 1.13**

In a *P*-type semiconductor, the Fermi level lies 0.4 eV above the valence band. Determine the new position of the Fermi level if the concentration of acceptor atoms is multiplied by a factor of (a) 0.5, and (b). Assume  $kT = 0.025$  eV.

**Solution** In a *P*-type material, the concentration of acceptor atoms is given by

$$N_A = N_V e^{-(E_F - E_V)/kT}$$

Let initially,  $N_A = N_{AO}$ ,  $E_F = E_{FO}$  and  $E_{FO} - E_V = 0.4$  eV

Therefore,  $N_{AO} = N_V e^{-0.4/0.025} = N_V e^{-16}$

(a) When  $N_A = 0.5$ ,  $N_{AO}$  and  $E_F = E_{F1}$  then

$$0.5N_{AO} = N_V e^{-(E_{F1} - E_V)/0.025} = N_V e^{-40(E_{F1} - E_V)}$$

Therefore,  $0.5 \times N_V e^{-16} = N_V e^{-40(E_{F1} - E_V)}$

Therefore,  $0.5 = e^{-40(E_{F1} + E_V) + 16}$

Taking natural logarithm on both sides, we get

$$\ln(0.5) = -40(E_{F1} - E_V) + 16$$

Therefore,  $E_{F1} - E_V = 0.417$  eV

(b) When  $N_A = 4N_{AO}$  and  $E_F = E_{F2}$  then

$$\ln 4 = -40(E_{F2} - E_V) + 16$$

Therefore,  $E_{F2} - E_V = 0.365$  eV

**REVIEW QUESTIONS**

1. Describe the energy-band structures of an insulator, a metal, and a semiconductor.
2. What are the three commonly used semiconductors?
3. What is meant by intrinsic semiconductor?
4. Explain the differences between intrinsic and extrinsic semiconductors.
5. What is meant by a hole? How do the holes move in an intrinsic semiconductor?
6. What is meant by doping in a semiconductor?
7. Discuss the following with respect to semiconductor: (i) doping (ii) dopant (iii) donor (iv) acceptor.
8. Explain “majority and minority carriers” in a semiconductor.
9. What is meant by *N*-type impurity in a semiconductor?
10. What is meant by *P*-type impurity in a semiconductor?
11. Define the terms *conductivity* and *mobility* in a semiconductor.
12. Derive the conductivity equation for *N*-type and *P*-type semiconductors.
13. Prove that the conductivity of a semiconductor is given by,  $\sigma = q(P\mu_p + n\mu_n)$ .
14. Describe the phenomenon of diffusion of charge carriers in semiconductors.
15. In an *N*-type semiconductor, the Fermi level lies 0.4 eV below the conduction band at 300 K. Determine the new position of the Fermi level if (i) the temperature is increased to 400 K, and (ii) the concentration of donor atoms is increased by a factor of 6. Assume  $kT = 0.03$  eV.

[Ans.: (i) 0.533 eV (ii) 0.3463 eV below the conduction band]

16. In a *P*-type semiconductor, the Fermi level lies 0.4 eV above the valence band at 300 K. Determine the new position of the Fermi level (i) at 450 K, and (ii) if the concentration of acceptor atoms is multiplied by a factor of 2. Assume  $kT = 0.03$  eV.  
 [Ans.: (i) 0.6 eV and (ii) 0.38 eV above the valence band]
17. The mobilities of electrons and holes in a sample of intrinsic germanium at room temperature are  $0.36 \text{ m}^2/\text{V-s}$  and  $0.17 \text{ m}^2/\text{V-s}$ , respectively. If the electron and hole densities are each equal to  $2.5 \times 10^{19}/\text{m}^3$ , calculate the conductivity.  
 [Ans.:  $\sigma_i = 2.12 \text{ S/m}$ ]
18. Compute the conductivity of a silicon semiconductor which is doped with acceptor impurity to a density of  $10^{22} \text{ atoms/m}^3$ . Given that  $n_i = 1.4 \times 10^{16}/\text{m}^3$ ,  $\mu_n = 0.145 \text{ m}^2/\text{V-s}$  and  $\mu_p = 0.05 \text{ m}^2/\text{V-s}$ .  
 [Ans.: 80 S/m]
19. The conductivity of pure silicon at room temperature is  $5 \times 10^{-4} \text{ S/m}$ . How many aluminium atoms per  $\text{m}^3$  are required so that a saturation conductivity of  $200 \text{ S/m}$  could be achieved in silicon using aluminium as an impurity? Given that the mobility of holes in silicon is  $0.05 \text{ m}^2/\text{V-s}$  and the mobility of electrons is  $0.13 \text{ m}^2/\text{V-s}$ .  
 [Ans.:  $2.5 \times 10^{22}/\text{m}^3$ ]
20. Calculate the conductivity of pure silicon at room temperature of 300 K. Given that  $n_i = 1.5 \times 10^{16}/\text{m}^3$ ,  $\mu_n = 0.13 \text{ m}^2/\text{V-s}$ ,  $\mu_p = 0.05 \text{ m}^2/\text{V-s}$  and  $q = 1.602 \times 10^{-19} \text{ C}$ . Now the silicon is doped 2 in  $10^8$  of a donor impurity. Calculate its conductivity if there are  $5 \times 10^{28} \text{ silicon atoms/m}^3$ . By what factor has the conductivity increased?  
 [Ans.:  $4.32 \times 10^{-4} \text{ S/m}$ ;  $20.8 \text{ S/m}$ ;  $\approx 48,000$ ]
21. The mobilities of free electrons and holes in pure silicon are  $0.13$  and  $0.05 \text{ m}^2/\text{V-s}$  and the corresponding values for pure germanium are  $0.38$  and  $0.18 \text{ m}^2/\text{V-s}$  respectively. Determine the values of intrinsic conductivity for both silicon and germanium. Given that  $n_i = 2.5 \times 10^{19}/\text{m}^3$  for germanium and  $n_i = 1.5 \times 10^{16}/\text{m}^3$  for silicon at room temperature.  
 [Ans.: 0.43 S/m; 2.24 S/m].
22. (i) A crystal of pure germanium has sufficient antimony (*N*-type or donor impurities) added to produce  $1.5 \times 10^{22}$  antimony atoms/ $\text{m}^3$ . The electron and hole mobility are  $0.38 \text{ m}^2/\text{V-s}$  and  $0.18 \text{ m}^2/\text{V-s}$  respectively, and the intrinsic charge carrier density is  $2.5 \times 10^{19}/\text{m}^3$ . Calculate (a) the density of electrons and holes in the crystal, and (b) the conductivity.  
 (ii) A second germanium crystal is produced which is doped with  $2.5 \times 10^{22}$  indium (*P*-types or acceptor impurities) atoms/ $\text{m}^3$ . Repeat the calculations listed in part (i).  
 (iii) A *PN* junction is made by joining the two crystals described above. Calculate its barrier voltage at 300 K.  
 [Ans.: (i)  $n = 1.5 \times 10^{22}/\text{m}^3$ ,  $p = 4.167 \times 10^{16}/\text{m}^3$ ,  $\sigma = 912/\Omega\text{-m}$   
 (ii)  $n = 2.5 \times 10^{16}/\text{m}^3$ ,  $p = 2.5 \times 10^{22}/\text{m}^3$ ,  $\sigma = 720/\Omega\text{-m}$  (iii) 0.335 V]
23. Explain the drift and diffusion currents for a semiconductor.
24. State and explain mass-action law.
25. What is Einstein relationship in a *PN* junction?
26. Derive the continuity equation from the first principle.
27. Show that in an intrinsic semiconductor, the Fermi level is located at the middle of the unallowable energy gap.
28. Explain Hall effect. How can Hall effect be used to determine some of the properties of a semiconductor?
29. Describe the applications of Hall effect.
30. A sample of *N*-type semiconductor has a Hall coefficient of  $150 \text{ cm}^3/\text{coulomb}$ . If its resistivity is  $0.15 \Omega\text{-cm}$ , estimate the electron mobility in the sample.  
 [Ans:  $1000 \text{ cm}^2/\text{V-s}$ ]
31. The conductivity of a pure silicon bar is  $5 \times 10^{-4}/\Omega\text{-m}$ . The magnetic flux density is  $0.1 \text{ Wb/m}^2$  and the thickness of the bar in the direction of the magnetic field is 3 mm. The measured values of Hall voltage and current are 50 mV and  $10 \mu\text{A}$ , respectively. Find the hole mobility.  
 [Ans:  $0.075 \text{ m}^2/\text{V-s}$ ]

**OBJECTIVE-TYPE QUESTIONS**

1. One of the following is not a semiconductor:  
 (a) Gallium arsenide (b) Indium (c) Germanium (d) Silicon
2. Referring to energy-level diagram of semiconductor materials, the width of the forbidden band-gap is about  
 (a) 10 eV (b) 100 eV (c) 1 eV (d) 0.1 eV
3. The electron mobility of the following semiconductor material is higher:  
 (a) Germanium (b) Silicon (c) Gallium arsenide (d) Indium
4. The energy required for relecting an electron from the valence bond for germanium is  
 (a) 0.66 eV (b) 1.08 eV (c) 1.58 eV (d) 1.88 eV
5. The unit of mobility is  
 (a)  $\text{m}^2\text{V}^{-1}\text{s}^{-1}$  (b)  $\text{mV}^{-1}\text{s}^{-1}$  (c)  $\text{Vsm}^{-1}$  (d)  $\text{Vms}^{-1}$
6. The conductivity of a semiconductor crystal due to any current carrier is NOT proportional to  
 (a) mobility of the carrier (b) effective density of state in conduction band  
 (c) electronic charge (d) surface states in the semiconductor
7. A long specimen of *P*-type semiconductor  
 (a) is positively charged (b) is electrically neutral  
 (c) has an electric field along its length (d) acts as a dipole
8. With increasing temperature, the resistivity of an intrinsic semiconductor decreases. This is because, with the increase of temperature,  
 (a) both the carrier concentration and mobility of carriers decrease  
 (b) the carrier concentration increases but the mobility of carriers decreases  
 (c) the carrier concentration decreases but the mobility of carriers increases  
 (d) the carrier concentration remains the same but the mobility of carriers decreases
9. If an intrinsic semiconductor is doped with a very small amount of boron, then in the extrinsic semiconductor so formed, the number of electrons and holes will  
 (a) decrease. (b) increase and decrease  
 (c) increase (d) decrease and increase
10. In an *N*-type semiconductor, the concentration of minority carriers mainly depends upon the  
 (a) doping technique (b) temperature of material  
 (c) number of donor atoms (d) quality of the intrinsic semiconductor material
11. Consider the following statements for an *N*-type semiconductor:  
  1.  $E_F$  lies below  $E_D$  at a room temperature ( $T$ )
  2.  $E_F$  lies above  $E_D$  at  $T \rightarrow 0$
  3.  $E_F = E_D$  at some intermediate temperature
  4.  $E_F$  is invariant with temperature
 where  $E_F$  is Fermi energy and  $E_D$  is donor level energy.  
 Which of these statement is/are correct?  
 (a) 1 and 2 (b) 2 and 3 (c) 4 only (d) 1, 2 and 3
12. The intrinsic carrier concentration of a silicon sample at 300 K is  $1.5 \times 10^{11}/\text{m}^3$ . If after doping, the number of majority carriers is  $5 \times 10^{20}/\text{m}^3$ , the minority carrier density is  
 (a)  $4.50 \times 10^{11}/\text{m}^3$  (b)  $3.33 \times 10^4/\text{m}^3$   
 (c)  $5.00 \times 10^{20}/\text{m}^3$  (d)  $3.00 \times 10^{-5}/\text{m}^3$
13. For intrinsic GaAs, the room-temperature electrical conductivity is  $10^{-6}(\text{ohm-m})^{-1}$ , the electron and hole mobilities are, respectively, 0.85 and  $0.04 \text{ m}^2/\text{V-s}$ . What is the intrinsic carrier concentration  $n_i$  at the room temperature?  
 (a)  $10^{-21} \text{ m}^{-3}$  (b)  $10^{-20} \text{ m}^{-3}$  (c)  $7.0 \times 10^{12} \text{ m}^{-3}$  (d)  $7.0 \times 10^{-20} \text{ m}^{-3}$

14. Drift current in semiconductors depends upon
- only the electric field
  - only the carrier concentration gradient
  - both the electric field and the carrier concentration
  - both electric field and the carrier concentration gradient
15. Diffusion current of holes in a semiconductor is proportional to (with  $p$  = concentration of holes/unit volume)
- |                       |                         |
|-----------------------|-------------------------|
| (a) $\frac{dp}{dx^2}$ | (b) $\frac{dp}{dx}$     |
| (c) $\frac{dp}{dt}$   | (d) $\frac{d^2p}{dx^2}$ |
16. Consider two energy levels;  $E_1$ ,  $E$  eV above the Fermi level and  $E_2$ ,  $E$  eV below the Fermi level.  $P_1$  and  $P_2$  are respectively the probabilities of  $E_1$  being occupied by an electron and  $E_2$  being empty. Then
- $P_1 > P_2$
  - $P_1 = P_2$
  - $P_1 < P_2$
  - $P_1$  and  $P_2$  depend on number of free electrons
17. In an intrinsic semiconductor, the free electron concentration depends on
- effective mass of electrons only
  - effective mass of holes only
  - temperature of the semiconductor
  - width of the forbidden energy band of the semiconductor
18. Which of the following quantities cannot be measured/determined using Hall effect?
- Type of semiconductor ( $P$  or  $N$ )
  - Mobility of charge carriers
  - Diffusion constant
  - Carrier concentration
19. What does a Hall-effect sensor sense?
- |                     |              |
|---------------------|--------------|
| (a) Temperature     | (b) Moisture |
| (c) Magnetic fields | (d) Pressure |
20. A current of 20 A is passed through a thin metal strip which is subjected to a magnetic flux density of  $1.2 \text{ Wb/m}^2$ . The magnetic field is directed perpendicular to the current. The thickness of the strip in the direction of the magnetic field is 0.5 mm. The Hall voltage is 60 V. Find the electron density.
- $0.5 \times 10^{21} \text{ m}^3$
  - $5 \times 10^{21} \text{ m}^3$
  - $0.05 \times 10^{21} \text{ m}^3$
  - $5.5 \times 10^{21} \text{ m}^3$
21. The current density as per Hall effect is \_\_\_\_\_ to charge density.
- directly proportional
  - inversely proportional
  - not proportional
  - none of the above
22. In an extrinsic semiconductor, the Hall coefficient  $R_H$
- increases with increase of temperature
  - decreases with increase of temperature
  - is independent of the change of temperature
  - changes with the change of magnetic field



# Junction Diode Characteristics and Special Semiconductor Devices

## **2.1 INTRODUCTION**

---

The *PN* junction diode is one of the semiconductor devices with two semiconductor materials in physical contact, one with excess of holes (*P*-type) and other with excess of electrons (*N*-type). A *PN* junction diode may be formed from a single crystal intrinsic semiconductor by doping part of it with acceptor impurities and the remaining with donors. Such junctions can form the basis of very efficient rectifiers. The most important characteristic of a *PN* junction is its ability to allow the flow of current in only one direction. In the opposite direction, it offers very high resistance. The high vacuum diode has largely been replaced by silicon and selenium rectifiers. Semiconductor diodes find wide applications in all phases of electronics, viz. radio and TV, optoelectronics, power supplies, industrial electronics, instrumentation, computers, etc. The chapter deals with the working of *PN* junction diode and its characteristics.

In addition to the *PN* junction diode, other types of diodes like Zener diode and tunnel diode are also discussed in this chapter and they are manufactured for specific applications. These special diodes are two terminal devices with their doping levels carefully selected to give the desired characteristics.

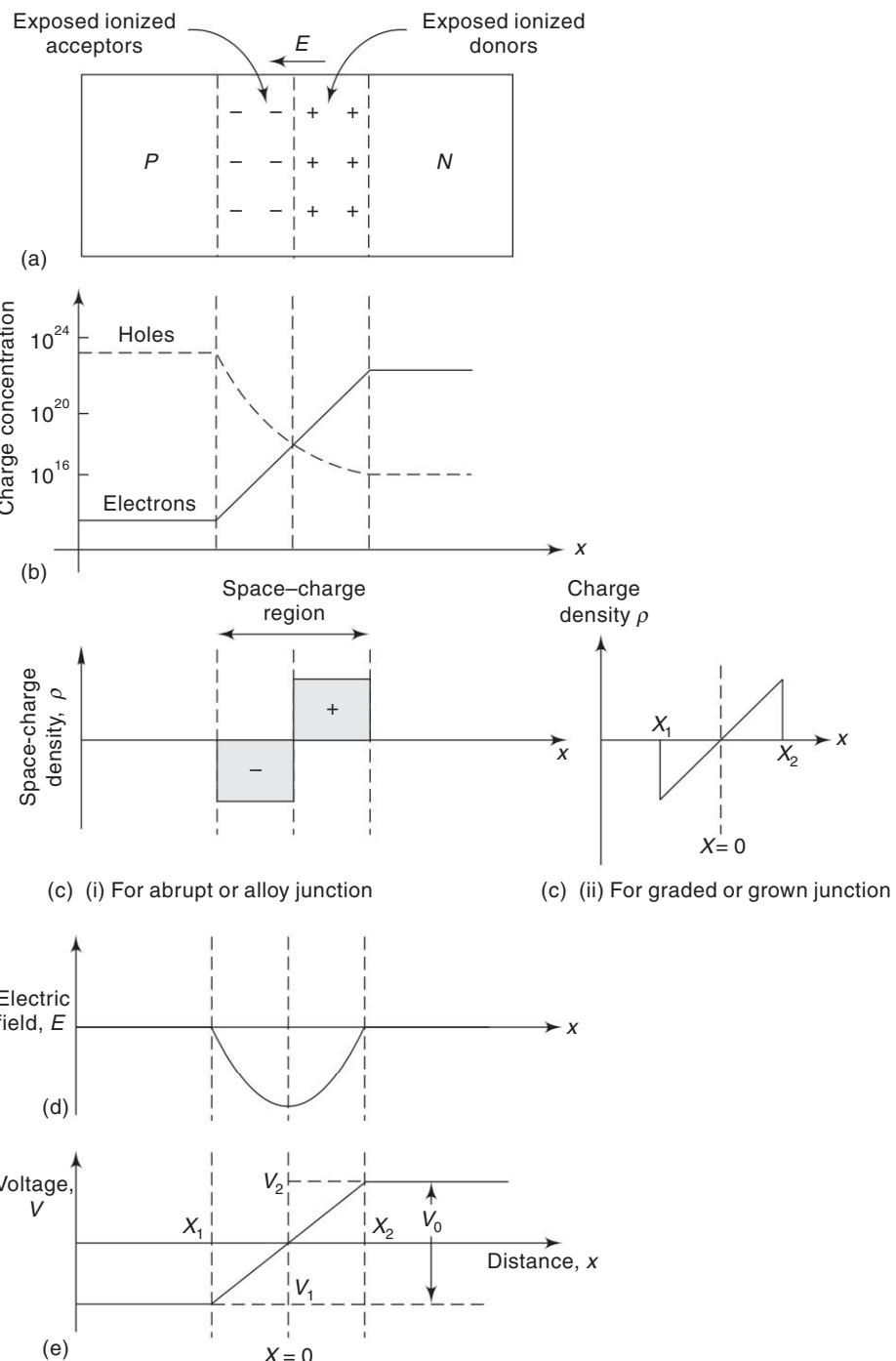
Thyristor, in general, is a semiconductor device having three or more junctions. Such a device acts as a switch without any bias and can be fabricated to have voltage ratings of several hundred volts and current ratings from a few amperes to almost thousand amperes. The family of thyristors consists of PNPN diode (Shockley diode), SCR, TRIAC, DIAC, etc. which are discussed here. This chapter also discusses the operation and characteristics of special semiconductor devices like LED, photo diode and UJT.

## **2.2 THEORY OF *PN* JUNCTION DIODE**

---

### **2.2.1 *PN* Junction Diode in Equilibrium with no Applied Voltage**

In a piece of semiconductor material, if one half is doped by *P*-type impurity and the other half is doped by *N*-type impurity, a *PN* junction is formed. The plane dividing the two halves or zones is called the *PN* junction. As shown in Fig. 2.1, the *N*-type material has high concentration of free electrons, while the *P*-type material has high concentration of holes. Therefore, at the junction there is a tendency for the free electrons to diffuse over to the *P*-side and holes to the *N*-side. This process is called *diffusion*. As the free electrons move across



**Fig. 2.1** Formation of PN junction

the junction from *N*-type to *P*-type, the donor ions become positively charged. Hence, a positive charge is built on the *N*-side of the junction. The free electrons that cross the junction uncover the negative acceptor ions by filling in the holes. Therefore, a net negative charge is established on the *P*-side of the junction. This net negative charge on the *P*-side prevents further diffusion of electrons into the *P*-side. Similarly, the net positive charge on the *N*-side repels the hole crossing from *P*-side to *N*-side. Thus, a barrier is set up near the junction which prevents further movement of charge carriers, i.e., electrons and holes. As a consequence of the induced electric field across the depletion layer, an electrostatic potential difference is established between *P*- and *N*-regions, which is called the potential barrier, junction barrier, diffusion potential, or contact potential,  $V_o$ . The magnitude of the contact potential  $V_o$  varies with doping levels and temperature.  $V_o$  is 0.3 V for germanium and 0.72 V for silicon.

The electrostatic field across the junction caused by the positively charged *N*-type region tends to drive the holes away from the junction and negatively charged *P*-type region tends to drive the electrons away from the junction. The majority holes diffusing out of the *P*-region leave behind negatively charged acceptor atoms bound to the lattice, thus exposing negative space charge in a previously neutral region. Similarly, electrons diffusing from the *N*-region expose positively ionized donor atoms, and a double-space-charge layer builds up at the junction as shown in Figs 2.1(a) and (c).

It is noticed that the space-charge layers are of opposite sign to the majority carriers diffusing into them, which tends to reduce the diffusion rate. Thus, the double space of the layer causes an electric field to be set up across the junction directed from *N*- to *P*-regions, which is in such a direction to inhibit diffusion of majority electrons and holes, as illustrated in Figs 2.1(a) and (d). The shape of the charge density,  $\rho$ , depends upon how the diode is doped. Thus, the junction region is depleted of mobile charge carriers. Hence, it is called the depletion region (layer), the space-charge region, or the transition region. The depletion region is of order 0.5  $\mu\text{m}$  thick. There are no mobile carriers in this very narrow depletion layer. Hence, no current flows across the junction and the system is in equilibrium. To the left of this depletion layer, the carrier concentration is  $p \approx N_A$ , and to its right, it is  $n \approx N_D$ .

**Calculation of Depletion Width** Let us now consider the width of the depletion region in the junction of Fig. 2.1. The region contains space charge due to the fact that donors on the *N*-side and acceptors on the *P*-side have lost their accompanying electrons and holes. Hence, an electric field is established which, in turn, causes a difference in potential energy,  $qV_o$ , between the two parts of the specimen. Thus, a potential is built up across the junction and Fig. 2.1(e) represents the variation in potential. Here, the *P*-side of the junction is at a lower potential than the *N*-side which means that the electrons on the *P*-side have a great potential energy.

In this analysis, let us consider an *alloy junction* in which there is an abrupt change from acceptor ions on *P*-side to donor ions on *N*-side. Assume that the concentration of electrons and holes in the depletion region is negligible and that all of the donors and acceptors are ionized. Hence, the regions of space charge may be described as

$$\begin{aligned}\rho &= -qN_A, 0 > x > X_1 \\ \rho &= +qN_D, X_2 > x > 0 \\ \rho &= 0, \text{ elsewhere}\end{aligned}$$

where  $\rho$  is the space-charge density, as indicated in Fig. 2.1(c)(i). The axes have been chosen in Fig. 2.1(e) in such a way that  $V_1$  and  $X_1$  have negative values. The potential variation in the space-charge region can be calculated by using Poisson's equation, which is given by

$$\nabla^2 V = -\frac{\rho(x, y, z)}{\epsilon_0 \epsilon_r}$$

where  $\epsilon_r$  is the relative permittivity. The relevant equation for the required one-dimensional problem is

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon_0 \epsilon_r}$$

Applying the above equation to the *P*-side of the junction, we get

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\epsilon_0 \epsilon_r}$$

Integrating twice, we get

$$V = \frac{qN_A x^2}{2\epsilon_0 \epsilon_r} + Cx + D$$

where  $C$  and  $D$  are the constants of integration.

From Fig. 2.1(e), we have  $V = 0$  at  $x = 0$ , and, hence,  $D = 0$ . When  $x < X_1$  on the *P*-side, the potential is constant, so that  $\frac{dV}{dx} = 0$  at  $x = X_1$ . Hence,

$$C = -\frac{qN_A}{\epsilon_0 \epsilon_r} \cdot X_1$$

Therefore, 
$$V = \frac{qN_A x^2}{2\epsilon_0 \epsilon_r} - \frac{qN_A}{\epsilon_0 \epsilon_r} \cdot X_1 \cdot x$$

i.e., 
$$V = \frac{qN_A}{\epsilon_0 \epsilon_r} \left( \frac{x^2}{2} - X_1 \cdot x \right)$$

As  $V = V_1$  at  $x = X_1$ , we have

$$V_1 = -\frac{qN_A}{2\epsilon_0 \epsilon_r} \cdot X_1^2$$

If we apply the same procedure to the *N*-side, we get

$$V_2 = \frac{qN_D}{2\epsilon_0 \epsilon_r} \cdot X_2^2$$

Therefore, the total built-in potential or the contact potential is  $V_o$ , where

$$V_o = V_2 - V_1 = \frac{q}{2\epsilon_0 \epsilon_r} (N_A X_1^2 + N_D X_2^2)$$

We know the fact that the positive charge on the *N*-side must be equal in magnitude to the negative charge on the *P*-side for the neutral specimen. Hence,

$$N_A X_1 = -N_D X_2$$

and substituting this relationship in the above equation and using the fact that  $X_1$  is a negative quantity, we get

$$X_1 = -\left[ \frac{2\epsilon_0 \epsilon_r V_o}{qN_A \left( 1 + \frac{N_A}{N_D} \right)} \right]^{1/2}$$

Similarly,

$$X_2 = \left[ \frac{2\epsilon_o \epsilon_r V_o}{qN_D \left( 1 + \frac{N_D}{N_A} \right)} \right]^{1/2}$$

The total depletion width,  $W = X_2 - X_1$  and, hence,  $W^2 = X_1^2 + X_2^2 - 2X_1 X_2$ , and then substituting for  $X_1$  and  $X_2$  from the above equations, we find

$$W = \left[ \frac{2\epsilon_o \epsilon_r V_o}{q} \left( \frac{N_A + N_D}{N_A N_D} \right) \right]^{1/2}$$

Here, in an *alloy junction*, the depletion width  $W$  is proportional to  $(V_o)^{1/2}$ .

In a *grown junction*, the charge density ( $\rho$ ) varies linearly with distance ( $x$ ) as shown in Fig. 2.1(c)(ii). If a similar analysis is carried for this junction, it is found that  $W$  varies as  $(V_o)^{1/3}$  instead of  $(V_o)^{1/2}$ .

## 2.2.2 Under Forward-Bias Condition

When the positive terminal of the battery is connected to the *P*-type and negative terminal to the *N*-type of the *PN* junction diode, the bias applied is known as forward bias.

**Operation** As shown in Fig. 2.2, the applied potential with external battery acts in opposition to the internal potential barrier and disturbs the equilibrium. As soon as equilibrium is disturbed by the application of an external voltage, the Fermi level is no longer continuous across the junction. Under the forward-bias condition, the applied positive potential repels the holes in the *P*-type region so that the holes move towards the junction and the applied negative potential repels the electrons in the *N*-type region and the electrons move towards the junction. Eventually, when the applied potential is more than the internal barrier potential, the depletion region and internal potential barrier disappear.

**V-I Characteristics of a Diode under Forward Bias** Under forward-bias condition, the *V-I* characteristics of a *PN* junction diode are shown in Fig. 2.3. As the forward voltage ( $V_F$ ) is increased, for  $V_F < V_O$ , the forward current  $I_F$  is almost zero (region *OA*) because the potential barrier prevents the holes from *P*-region and electrons from *N*-region to flow across the depletion region in the opposite direction.

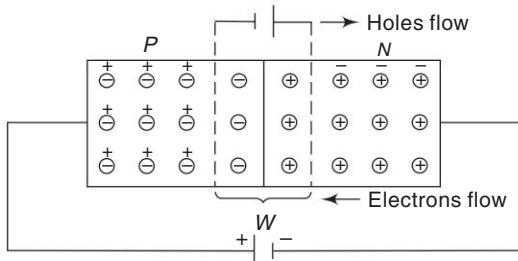


Fig. 2.2 PN junction under forward bias

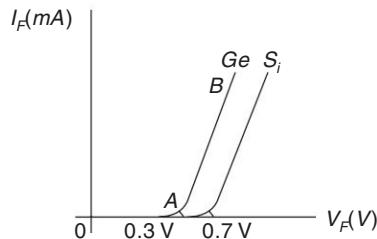


Fig. 2.3 V-I characteristics of a diode under forward-bias condition

For  $V_F > V_O$ , the potential barrier at the junction completely disappears and, hence, the holes cross the junction from *P*-type to *N*-type and the electrons cross the junction in the opposite direction, resulting in relatively large current flow in the external circuit.

A feature worth to be noted in the forward characteristics shown in Fig. 2.3 is the cut in or threshold voltage ( $V_t$ ) below which the current is very small. It is 0.3 V and 0.7 V for germanium and silicon, respectively. At the cut-in voltage, the potential barrier is overcome and the current through the junction starts to increase rapidly.

### 2.2.3 Under Reverse-Bias Condition

When the negative terminal of the battery is connected to the *P*-type and positive terminal of the battery is connected to the *N*-type of the *PN* junction, the bias applied is known as reverse bias.

**Operation** Under applied reverse bias as shown in Fig. 2.4, holes which form the majority carriers of the *P*-side move towards the negative terminal of the battery and electrons which form the majority carrier of the *N*-side are attracted towards the positive terminal of the battery. Hence, the width of the depletion region which is depleted of mobile charge carriers increases. Thus, the electric field produced by applied reverse bias, is in the same direction as the electric field of the potential barrier. Hence, the resultant potential barrier is increased which prevents the flow of majority carriers in both directions; the depletion width,  $W$ , is proportional to  $\sqrt{V_o}$  under reverse bias. Therefore, theoretically, no current should flow in the external circuit. But in practice, a very small current of the order of a few microampere flows under reverse bias as shown in Fig. 2.5. Electrons forming covalent bonds of the semiconductor atoms in the *P*- and *N*-type regions may absorb sufficient energy from heat and light to cause breaking of some covalent bonds. Hence, electron-hole pairs are continually produced in both the regions. Under the reverse-bias condition, the thermally generated holes in the *P*-region are attracted towards the negative terminal of the battery and the electrons in the *N*-region are attracted towards the positive terminal of the battery. Consequently, the minority carriers, electrons in the *P*-region and holes in the *N*-region, wander over to the junction and flow towards their majority carrier side giving rise to a small reverse current. This current is known as *reverse saturation current*,  $I_o$ . The magnitude of the reverse saturation current mainly depends upon junction temperature because the major source of minority carriers is thermally broken covalent bonds.

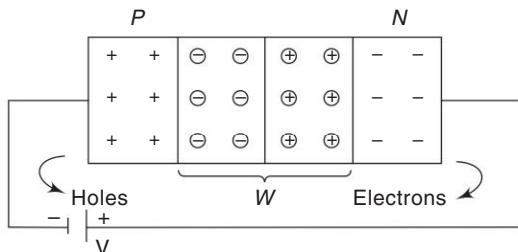


Fig. 2.4 *PN* junction under reverse bias

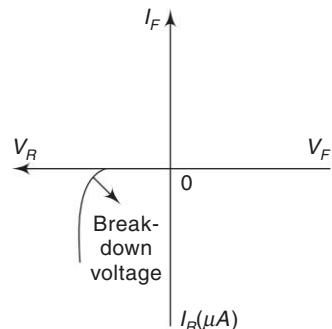


Fig. 2.5 *V-I* characteristics under reverse bias

For large applied reverse bias, the free electrons from the *N*-type moving towards the positive terminal of the battery acquire sufficient energy to move with high velocity to dislodge valence electrons from semiconductor atoms in the crystal. These newly liberated electrons, in turn, acquire sufficient energy to dislodge other parent electrons. Thus, a large number of free electrons are formed which is commonly called an avalanche

of free electrons. This leads to the breakdown of the junction leading to very large reverse current. The reverse voltage at which the junction breakdown occurs is known as *breakdown voltage*,  $V_{BD}$ .

#### 2.2.4 PN Junction as a Diode

Figure 2.6 shows the current-voltage characteristics of *PN* junction. The characteristics of the *PN* junction vary enormously depending upon the polarity of the applied voltage. For a forward-bias voltage, the current increases exponentially with the increase of voltage. A small change in the forward-bias voltage increases the corresponding forward-bias current by orders of magnitude and, hence, the forward-bias *PN* junction will have a very small resistance. The level of current flowing across a forward-biased *PN* junction largely depends upon the junction area. In the reverse-bias direction, the current remains small, i.e., almost zero, irrespective of the magnitude of the applied voltage and hence the reverse-bias *PN* junction will have a high resistance. The reverse-bias current depends on the area, temperature and type of semiconductor material.

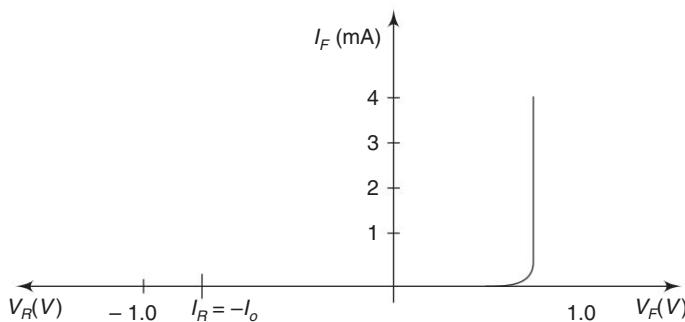


Fig. 2.6 Ideal I–V characteristics of a *PN* junction diode

The semiconductor device that displays these *I–V* characteristics is called a *PN* junction diode. Figure 2.7 shows the *PN* junction diode with forward-bias and reverse-bias and their circuit symbols. The metal contacts are indicated with which the homogeneous *P*-type and *N*-type materials are provided. Thus, two metal-semiconductor junctions, one at each end of the diode, are introduced. The contact potential across these junctions is approximately independent of the direction and magnitude of the current. A contact of this type is called an *ohmic contact*, which has low resistance. In the forward bias, a relatively large current is produced by a fairly small applied voltage. In the reverse bias, only a very small current, ranging from nanoamps to microamps is produced. The diode can be used as a voltage controlled switch, i.e., OFF for a reverse-bias voltage and ON for a forward-bias voltage.

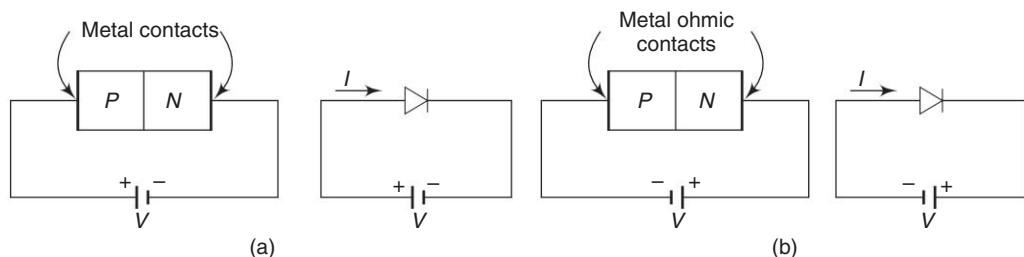


Fig. 2.7 (a) Forward-biased *PN* junction diode and its circuit symbol  
(b) Reverse-biased *PN* junction diode and its circuit symbol

When a diode is reverse-biased by at least 0.1 V, the diode current is  $I_R = -I_o$ . As the current is in the reverse direction and is a constant, it is called the diode *reverse saturation current*. Real diodes exhibit reverse-bias current that are considerably larger than  $I_o$ . This additional current is called a *generation current* which is due to electrons and holes being generated within the space-charge region. A typical value of  $I_0$  may be  $10^{-14}$  A and a typical value of reverse-bias current may be  $10^{-9}$  A.

### 2.2.5 PN Junction Diode as a Rectifier

A *PN* junction diode is a two-terminal device that is polarity sensitive. When the diode is forward biased, the diode conducts and allows current to flow through it without any resistance, i.e., the diode is ON. When the diode is reverse biased, the diode does not conduct and no current flows through it, i.e., the diode is OFF, or providing a blocking function. Thus, an ideal diode acts as a switch, either open or closed, depending upon the polarity of the voltage placed across it. The ideal diode has zero resistance under forward bias and infinite resistance under reverse bias.

### 2.2.6 Diode Ratings or Limiting Values of PN Junction Diode

The *PN* junction diode will perform satisfactorily only if it is operated within certain limiting values. They are the following:

- **Maximum Forward Current** It is the highest instantaneous current under forward-bias condition that can flow through the junction.
- **Peak Inverse Voltage (PIV)** It is the maximum reverse voltage that can be applied to the *PN* junction. If the voltage across the junction exceeds PIV under reverse-bias condition, the junction gets damaged.
- **Maximum Power Rating** It is the maximum power that can be dissipated at the junction without damaging the junction. Power dissipation is the product of voltage across the junction and current through the junction.
- **Maximum Average Forward Current** It is given at a special temperature, usually 25°C, (77°F) and refers to the maximum amount of average current that can be permitted to flow in the forward direction. If this rating exceeds its limit then the structure breakdown can occur.
- **Repetitive Peak Forward Current** It is the maximum peak current that can be permitted to flow in the forward direction in the form of recurring pulses. The limiting value of this current is 450 mA.
- **Maximum Surge Current** It is the maximum current permitted to flow in the forward direction in the form of non-recurring pulses. The current should not equal this value for more than a few milliseconds.

The above diode ratings are subject to change with temperature variations. If the operating temperature is more than that stated for the rating then the ratings must be decreased.

## 2.3 CURRENT COMPONENTS IN PN JUNCTION DIODE

---

Let us now derive the expression for the total current as a function of applied voltage assuming that the width of the depletion region is zero. When a forward bias is applied to a diode, holes are injected from the *P*-side into the *N*-side. Due to this, the concentration of holes in the *N*-side ( $p_n$ ) is increased from its thermal equilibrium value ( $p_{n0}$ ) and injected hole concentration [ $P_n(x)$ ] decreases exponentially with respect to the distance ( $x$ ).

$$P_n(x) = p_n - p_{n0} = P_n(0)e^{-x/L_p}$$

where  $L_p$  is the diffusion length for holes in the  $N$ -material.

$$p_n(x) = p_{n0} + P_n(0)e^{-x/L_p} \quad (2.1)$$

Injected hole concentration at  $x = 0$  is

$$P_n(0) = p_n(0) - p_{n0} \quad (2.2)$$

Let  $p_p$  and  $p_n$  be the hole concentrations at the edges of the space charge in the  $P$ - and  $N$ -sides, respectively. Let  $V_B (= V_0 - V)$  be the effective barrier potential across the depletion layer. Then

$$p_p = P_n e^{V_B/V_T} \quad (2.3)$$

where  $V_T$  is the volt-equivalent of temperature.

This is the Boltzmann's relation of kinetic gas theory. This equation is valid as long as the hole current is small compared with diffusion or drift currents. This condition is called *low-level-injection*.

Under open-circuit condition (i.e.,  $V = 0$ ),  $p_p = p_{p0}$ ,  $p_n = p_{n0}$  and  $V_B = V_0$ . Equation (2.3) can be changed into

$$p_{p0} = p_{n0} e^{V_0/V_T} \quad (2.4)$$

Under forward-bias condition, let  $V$  be the applied voltage; then the effective barrier voltage

$$V_B = V_0 - V$$

The hole concentration throughout the  $P$ -side is constant and equal to the thermal equilibrium value ( $p_p = p_{p0}$ ). The hole concentration varies exponentially with distance into the  $N$ -side.

At  $x = 0$ ,  $p_n = p_n(0)$

Equation (2.3) can be changed into

$$p_{p0} = p_n(0) e^{(V_0 - V)/V_T} \quad (2.5)$$

Comparing Eqs (2.4) and (2.5),

$$p_n(0) = p_{n0} e^{V/V_T}$$

This boundary condition is called the *law of the junction*. Substituting this into Eq. (2.2), we get

$$P_n(0) = p_{n0} (e^{V/V_T} - 1) \quad (2.6)$$

The diffusion-hole current in the  $N$ -side is

$$\begin{aligned} I_{pn}(x) &= -Aq D_p \frac{dp_n(x)}{dx} \\ &= -Aq D_p \frac{d}{dx} \left[ p_{n0} + P_n(0) e^{-x/L_p} \right] \\ &= \frac{Aq D_p P_n(0)}{L_p} e^{-x/L_p} \end{aligned}$$

From this equation, it is evident that the injected hole current decreases exponentially with distance.

**Forward Currents** The hole current crossing the junction into the *N*-side with  $x = 0$  is

$$I_{pn}(0) = \frac{AqD_p P_n(0)}{L_p} = \frac{AqD_p p_{n0}}{L_p} (e^{V/V_T} - 1)$$

The electron current crossing the junction into the *P*-side with  $x = 0$  is

$$I_{np}(0) = \frac{AqD_n N_p(0)}{L_n} = \frac{AqD_n n_{p0}}{L_n} (e^{V/V_T} - 1)$$

The total diode current,

$$I = I_{pn}(0) + I_{np}(0) = I_o (e^{V/V_T} - 1)$$

where  $I_o = \frac{AqD_p p_{n0}}{L_p} + \frac{AqD_n n_{p0}}{L_n}$  = reverse saturation current.

If we consider carrier generation and recombination in the space-charge region, the general equation of the diode current is approximately given by

$$I = I_o [e^{(V/\eta V_T)} - 1]$$

where  $V$  = external voltage applied to the diode and  $\eta$  = a constant, 1 for germanium and 2 for silicon.

**Reverse Saturation Current** We know that  $p_n = \frac{n_i^2}{N_D}$  and  $n_p = \frac{n_i^2}{N_A}$ . Applying these relationships in

the above equation of reverse saturation current,  $I_o$ , we get

$$I_o = Aq \left[ \frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right] n_i^2$$

where  $n_i^2 = A_o T^3 e^{-E_{Go}/kT} = A_o T^3 e^{-V_{Go}/V_T}$ , where  $V_{Go}$  is a voltage which is numerically equal to the forbidden-gap energy  $E_{Go}$  in electronvolt.

For a germanium diode, the diffusion constants  $D_p$  and  $D_n$  vary approximately inversely proportional to  $T$ . Hence, the temperature dependence of  $I_o$  is

$$I_o = K_1 T^2 e^{\frac{-V_{Go}}{V_T}}$$

where  $K_1$  is a constant independent of temperature.

For a silicon diode,  $I_o$  is proportional to  $n_i$  instead of  $n_i^2$ . Hence,

$$I_o = K_2 T^{\frac{3}{2}} e^{\frac{-V_{Go}}{2V_T}}$$

where  $K_2$  is a constant independent of temperature.

## 2.4 DIODE EQUATION

---

The diode-current equation relating the voltage  $V$  and current  $I$  is given by

$$I = I_o [e^{(V/\eta V_T)} - 1]$$

where  $I$  = diode current

$I_o$  = diode reverse saturation current at room temperature

$V$  = external voltage applied to the diode

$\eta$  = a constant, 1 for germanium and 2 for silicon

Now,  $V_T = kT/q = T/11600$ , volt-equivalent of temperature, i.e., thermal voltage,

where  $k$  = Boltzmann's constant ( $1.38 \times 10^{-23}$  J/K)

$q$  = charge of the electron ( $1.602 \times 10^{-19}$  C)

$T$  = temperature of the diode junction (K) = ( $^{\circ}\text{C} + 273$ )

At room temperature ( $T = 300$  K),  $V_T = 26$  mV. Substituting this value in the current equation, we get

$$I = I_o [e^{(40 V/\eta)} - 1]$$

Therefore, for a germanium diode,  $I = I_o [e^{40V} - 1]$ , since  $\eta = 1$  for germanium. For a silicon diode,  $I = I_o [e^{20V} - 1]$ , since  $\eta = 2$  for silicon.

If the value of applied voltage is greater than unity then the equation of diode current for germanium,

$$I = I_o (e^{40V})$$

and for silicon,  $I = I_o (e^{20V})$

When the diode is reverse biased, its current equation may be obtained by changing the sign of the applied voltage  $V$ . Thus, the diode current with reverse bias is

$$I = I_o [e^{(-V/\eta V_T)} - 1]$$

If  $V \gg V_T$  then the term  $e^{(-V/\eta V_T)} \ll 1$ ; therefore,  $I \approx -I_o$ , termed as reverse saturation current, which is valid as long as the external voltage is below the breakdown value.

### EXAMPLE 2.1

When a reverse bias is applied to a germanium  $PN$  junction diode, the reverse saturation current at room temperature is  $0.3 \mu\text{A}$ . Determine the current flowing in the diode when  $0.15$  V forward bias is applied at room temperature.

**Solution** Given  $I_o = 0.3 \times 10^{-6}$  A and  $V_F = 0.15$  V

The current flowing through the  $PN$  diode under forward bias is

$$\begin{aligned} I &= I_o (e^{40V_F} - 1) \\ &= 0.3 \times 10^{-6} (e^{40 \times 0.15} - 1) \\ &= 120.73 \mu\text{A} \end{aligned}$$

**EXAMPLE 2.2**

The reverse saturation current of a silicon  $PN$  junction diode is  $10 \mu\text{A}$ . Calculate the diode current for the forward-bias voltage of  $0.6 \text{ V}$  at  $25^\circ\text{C}$ .

**Solution** Given  $V_F = 0.6 \text{ V}$ ,  $T = 273 + 25 = 298 \text{ K}$   
 $I_o = 10 \mu\text{A} = 1 \times 10^{-5} \text{ A}$  and  $\eta = 2$  for silicon

The volt-equivalent of the temperature ( $T$ ) is

$$V_T = \frac{T}{11,600} = \frac{298}{11,600} = 25.7 \times 10^{-3} \text{ V}$$

Therefore, the diode current,

$$\begin{aligned} I &= I_o \left( e^{\frac{V_F}{\eta V_T} - 1} \right) \\ &= 10^{-5} \left( e^{\frac{0.6}{2 \times 25.7 \times 10^{-3}}} - 1 \right) = 1.174 \text{ A} \end{aligned}$$

**EXAMPLE 2.3**

The diode current is  $0.6 \text{ mA}$  when the applied voltage is  $400 \text{ mV}$ , and  $20 \text{ mA}$  when the applied voltage is  $500 \text{ mV}$ . Determine  $\eta$ . Assume  $\frac{kT}{q} = 25 \text{ mV}$ .

**Solution**

The diode current,  $I = I_o \left( e^{\frac{qV}{\eta kT}} - 1 \right)$

$$\begin{aligned} \text{Therefore, } 0.6 \times 10^{-3} &= I_o \left( e^{\frac{qV}{\eta kT}} - 1 \right) = I_o e^{\frac{qV}{\eta kT}} \\ &= I_o \cdot e^{\frac{400}{25\eta}} = I_o \cdot e^{\frac{16}{\eta}} \end{aligned} \quad (1)$$

$$\text{Also, } 20 \times 10^{-3} = I_o \cdot e^{\frac{500}{25\eta}} = I_o \cdot e^{\frac{20}{\eta}} \quad (2)$$

Dividing Eq. (2) by Eq. (1), we get

$$\frac{20 \times 10^{-3}}{0.6 \times 10^{-3}} = \frac{I_o \cdot e^{\frac{20}{\eta}}}{I_o \cdot e^{\frac{16}{\eta}}}$$

$$\text{Therefore, } \frac{100}{3} = e^{\frac{4}{\eta}}$$

Taking natural logarithms on both sides, we get

$$\log_e \frac{100}{3} = \frac{4}{\eta}$$

$$3.507 = \frac{4}{\eta}$$

Therefore,

$$\eta = \frac{4}{3.507} = 1.14$$

### EXAMPLE 2.4

Find the voltage at which the reverse current in a germanium *PN* junction diode attains a value of 90% of its saturation value at room temperature.

**Solution** We know that the current of a *PN* junction diode is

$$I = I_o \left( e^{\frac{V}{V_T}} - 1 \right)$$

Therefore,  $-0.90 I_o = I_o \left( e^{\frac{V}{V_T}} - 1 \right)$

where  $V_T = \frac{T}{11,600} = 26 \text{ mV}$

$$-0.9 = \left( e^{\frac{V}{0.026}} - 1 \right)$$

$$0.1 = e^{\frac{V}{0.026}}$$

Therefore,  $V = -0.06 \text{ V}$

### EXAMPLE 2.5

Determine the ideal reverse saturation current density in a silicon *PN* junction at  $T = 300 \text{ K}$ . Consider the following parameters in the silicon *PN* junction:

$N_A = N_D = 10^{16} \text{ cm}^{-3}$ ,  $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$ ,  $D_n = 25 \text{ cm}^2/\text{s}$ ,  $T_{po} = T_{no} = 5 \times 10^{-7} \text{ s}$ ,  $D_p = 10 \text{ cm}^2/\text{s}$ ,  $\varepsilon_r = 11.7$ . Comment on the result.

**Solution** Given,  $T = 300 \text{ K}$ ,  $N_A = N_D = 10^{16} \text{ cm}^{-3}$ ,  $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$ ,  $D_n = 25 \text{ cm}^2/\text{s}$ ,

$$T_{po} = T_{no} = 5 \times 10^{-7} \text{ s}$$

The reverse saturation current is given by

$$I_o = Aq \left[ \frac{D_p}{L_p \cdot N_D} + \frac{D_n}{L_n \cdot N_A} \right] n_i^2$$

We know that,  $J_o = \frac{I_o}{A}$

Therefore, reverse saturation current density is,

$$J_o = q \left[ \frac{D_p}{L_p \cdot N_D} + \frac{D_n}{L_n \cdot N_A} \right] n_i^2$$

where  $L_p = \sqrt{D_p \cdot T_{po}} = \sqrt{10 \times 10^{-4} \times 5 \times 10^{-7}} = 2.236 \times 10^{-5}$

and  $L_n = \sqrt{D_n \cdot T_{no}} = \sqrt{25 \times 10^{-4} \times 5 \times 10^{-7}} = 3.535 \times 10^{-5}$

Hence,

$$J_o = 1.602 \times 10^{-19} \left[ \frac{10 \times 10^{-4}}{2.236 \times 10^{-5} \times 10^{22}} + \frac{25 \times 10^{-4}}{3.535 \times 10^{-5} \times 10^{22}} \right] (1.5 \times 10^{-16})^2$$

$$= 0.416 \mu\text{A/s}$$

## 2.5 TEMPERATURE DEPENDENCE ON V-I CHARACTERISTICS

The reverse saturation current  $I_o$  is temperature dependent while voltage equivalent of temperature  $V_T$  is also temperature dependent. Hence, the diode current involving  $I_o$  and  $V_T$  is temperature dependent. Therefore, the overall diode characteristics depend on the temperature.

The dependence of  $I_o$  on temperature  $T$  is given by

$$I_o = K T^m e^{-V_{Go}/\eta V_T} \quad (2.7)$$

where  $K$  = constant independent of temperature (not the Boltzmann's constant)

$m$  = 2 for Ge and 1.5 for Si

and  $V_{Go}$  = forbidden energy gap = 0.785 V for Ge and 1.21 V for Si.

As temperature increases, the value of  $I_o$  increases and, hence, the diode current increases. To keep diode current constant, it is necessary to reduce the applied voltage  $V$  of the diode.

Let us calculate, the rate of change of the applied voltage to keep the diode current constant. For a constant diode current,  $\frac{dI}{dT} = 0$ . Hence, the change in voltage has to be calculated.

A diode current equation is given by

$$I = I_o (e^{V/\eta V_T} - 1)$$

Since  $I \gg I_o$  for a forward characteristics, we have

$$I = I_o e^{V/\eta V_T} \quad (2.8)$$

Substituting Eq. (2.7) into Eq. (2.8), we get

$$I = K T^m e^{-V_{Go}/\eta V_T} \cdot e^{V/\eta V_T}$$

$$= K T^m e^{(V-V_{Go})/\eta V_T} \quad (2.9)$$

Since  $V_T = kT$ , where  $k$  is Boltzmann's constant,

$$I = K T^m e^{(V-V_{Go})/\eta k_T}$$

For a constant diode current,  $dI/dT = 0$ . Hence, differentiating this equation with respect to  $T$ , we get

$$\begin{aligned}\frac{dI}{dT} &= K \left[ mT^{m-1} e^{(V-V_{Go})/\eta k_T} + T^m e^{(V-V_{Go})/\eta k_T} \cdot \frac{d}{dT} \left( \frac{V - V_{Go}}{\eta k_T} \right) \right] \\ &= K e^{(V-V_{Go})/\eta k_T} \left[ mT^{m-1} + \frac{T^m}{\eta^k} \left( \frac{T \frac{dV}{dT} - (V - V_{Go}) \times 1}{T^2} \right) \right] \\ &= K e^{(V-V_{Go})/\eta k_T} \left[ \frac{mT^m}{T} + \frac{T^m}{\eta k T^2} \left( T \frac{dV}{dT} - (V - V_{Go}) \right) \right]\end{aligned}$$

Note that  $V_{Go}$  is forbidden energy gap at 0 K and, hence, it is a constant from differentiation point of view. Taking  $T^m$  outside and rearranging the above equation, we get

$$\begin{aligned}\frac{dI}{dT} &= K e^{(V-V_{Go})/\eta k_T} \times T^m \left[ \frac{m\eta k T + \left( T \frac{dV}{dT} - (V - V_{Go}) \right)}{\eta k T} \right] \\ &= K e^{(V-V_{Go})/\eta k_T} \times \frac{T^m}{\eta k T^2} \left[ m\eta k T + \left( T \frac{dV}{dT} - (V - V_{Go}) \right) \right]\end{aligned}$$

Replacing  $kT$  with  $V_T$ , we get

$$\frac{dI}{dT} = K e^{(V-V_{Go})/\eta k_T} \times \frac{T^{m-1}}{\eta V_T} \left[ m\eta V_T + \left( T \frac{dV}{dT} - (V - V_{Go}) \right) \right]$$

Now,  $\frac{dI}{dT} = 0$  for constant diode current. Hence, equating the above equation to zero, we get

$$m\eta V_T + T \frac{dV}{dT} - (V - V_{Go}) = 0$$

$$T \frac{dV}{dT} = V - V_{Go} - m\eta V_T$$

$$\frac{dV}{dT} = \frac{V - (V_{Go} - m\eta V_T)}{T}$$

This is the required change in voltage necessary to keep diode current constant.

Hence, for germanium, at cut-in voltage,  $V = V_\gamma = 0.2$  V and with  $m = 2$ ,  $\eta = 1$ ,  $T = 30$  K, and  $V_{Go} = 0.785$  V in the above equation, we get

$$\frac{dV}{dT} = \frac{0.2 - (0.785 + 2 \times 1 \times 26 \times 10^{-3})}{300} = -2.12 \text{ mV/}^\circ\text{C for Ge}$$

The negative sign indicates that the voltage must be reduced at a rate of 2.12 mV per degree change in temperature to keep diode current constant.

Similarly,  $\frac{dV}{dT} = -2.3 \text{ mV/}^\circ\text{C}$  for Si.

Practically, the value of  $\frac{dV}{dT}$  is assumed to be  $-2.5 \text{ mV}/\text{°C}$  for either Ge or Si at room temperature.

$$\text{Thus, } \frac{dV}{dT} = -2.5 \text{ mV}/\text{°C} \quad (2.10)$$

The negative sign indicates that  $dV/dT$  decreases with increase in temperature.

### 2.5.1 Effect of Temperature on Reverse Saturation Current

To study by what rate  $I_o$  changes with respect to temperature, consider Eq. (2.7) again. That is,

$$I_o = KT^m e^{-V_{Go}/\eta V_T}$$

Taking logarithm on both sides, we get

$$\begin{aligned} \ln(I_o) &= \ln(KT^m e^{-V_{Go}/\eta V_T}) \\ &= \ln K + \ln T^m - \frac{V_{Go}}{\eta V_T} \\ &= \ln K + m \ln T - \frac{V_{Go}}{\eta V_T} \end{aligned}$$

Substituting  $V_T = kT$ , we get

$$\ln(I_o) = \ln K + m \ln T - \frac{V_{Go}}{\eta kT}$$

Differentiating this equation with respect to  $T$ , we get

$$\frac{d \ln(I_o)}{dT} = 0 + \frac{m}{T} - \frac{V_{Go}}{\eta k} \cdot \left( \frac{-1}{T^2} \right) = \frac{m}{T} + \frac{V_{Go}}{\eta k T^2}$$

Replacing  $kT$  with  $V_T$  we have

$$\frac{d[\ln I_o]}{dT} = \frac{m}{T} + \frac{V_{Go}}{\eta T V_T}$$

For germanium, substituting the values of various terms at room temperature, we get

$$\frac{d[\ln I_o]}{dT} = \frac{2}{300} + \frac{0.785}{1 \times 300 \times 26 \times 10^{-3}} = 0.11 \text{ per } \text{°C}$$

This indicates that  $I_o$  increases by 11% per degree rise in temperature. For silicon, we get

$$\frac{d[\ln I_o]}{dT} = 0.08 \text{ per } \text{°C}$$

This indicates that  $I_o$  increases by 8% per degree rise in temperature.

Practically, it is found that the reverse saturation current  $I_o$  increases by 7% per  $\text{°C}$  change in temperature for both silicon and germanium diodes. If at  $T^\circ\text{C}$  is  $1 \mu\text{A}$  then at  $(T + 1)^\circ\text{C}$ , it becomes  $1.07 \mu\text{A}$ , and so on. From this, it can be concluded that reverse saturation current approximately doubles, i.e.,  $1.07^{10}$  for every  $10^\circ\text{C}$  rise in temperature.

The above result can be mathematically represented as,

$$I_{02} = \left( 2^{\frac{T_2 - T_1}{10}} \right) I_{01} = \left( 2^{\frac{\Delta T}{10}} \right) I_{01}$$

where  $I_{02}$  is the reverse saturation current at  $T_2$  and  $I_{01}$  is the reverse saturation current at  $T_1$ .

### 2.5.2 Temperature Dependence of V-I Characteristics

The rise in temperature increases the generation of electron-hole pairs in semiconductors and increases their conductivity. As a result, the current through the  $PN$  junction diode increases with temperature as given by the diode-current equation,

$$I = I_o [e^{(V/\eta VT)} - 1]$$

The reverse saturation current  $I_o$  of the diode increases approximately 7 percent/ $^{\circ}\text{C}$  for both germanium and silicon. Since  $(1.07)^{10} \approx 2$ , reverse saturation current approximately doubles for every  $10^{\circ}\text{C}$  rise in temperature. Hence, if the temperature is increased at fixed voltage, the current  $I$  increases. To bring the current  $I$  to its original value, the voltage  $V$  has to be reduced. It is found that at room temperature, for either germanium or silicon,  $\frac{dV}{dT} \approx -2.5 \text{ mV}/^{\circ}\text{C}$  in order to maintain the current  $I$  to a constant value.

At room temperature, i.e., at 300 K, the value of barrier voltage or cut-in voltage is about 0.3 V for germanium and 0.7 V for silicon. The barrier voltage is temperature dependent and it decreases by 2 mV/ $^{\circ}\text{C}$  for both germanium and silicon. This fact may be expressed in mathematical form, which is given by

$$I_{02} = I_{01} \times 2^{(T_2 - T_1)/10}$$

where  $I_{01}$  = saturation current of the diode at the temperature ( $T_1$ ), and  $I_{02}$  = saturation current of the diode at the temperature ( $T_2$ ).

Figure 2.8 shows the effect of increased temperature on the characteristic curve of a  $PN$  junction diode. A germanium diode can be used up to a maximum of  $75^{\circ}\text{C}$  and a silicon diode, to a maximum of  $175^{\circ}\text{C}$ .

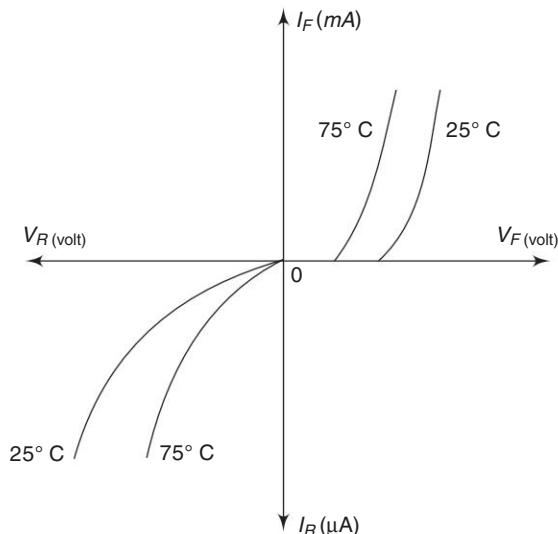


Fig. 2.8 Effect of temperature on diode characteristics

#### EXAMPLE 2.6

The voltage across a silicon diode at room temperature (300 K) is 0.7 volt when 2 mA current flows through it. If the voltage increases to 0.75 V, calculate the diode current (assume  $V_T = 26 \text{ mV}$ ).

**Solution**

Given data

Room temperature = 300 K

Voltage across a silicon diode,  $V_{D1} = 0.7 \text{ V}$

Current through the diode,  $I_{D1} = 2 \text{ mA}$

When the voltage increases to 0.75 V,  $V_{D2}$  then

$$\frac{I_{D2}}{I_{D1}} = \frac{I_o(e^{V_{D2}/V_T\eta} - 1)}{I_o(e^{V_{D1}/V_T\eta} - 1)} = \frac{e^{0.75/26 \times 10^{-3} \times 2} - 1}{e^{0.7/26 \times 10^{-3} \times 2} - 1} = 2.615$$

Therefore,

$$I_{D2} = 2.615 \times I_{D1} = 2.615 \times 2 \times 10^{-3} = 5.23 \text{ mA}$$

### EXAMPLE 2.7

A silicon diode has a saturation current of  $7.5 \mu\text{A}$  at room temperature of 300 K. Calculate the saturation current at 400 K.

**Solution** Given  $I_{o1} = 7.5 \times 10^{-6} \text{ A}$  at  $T_1 = 300 \text{ K} = 27^\circ\text{C}$  and  $T_2 = 400 \text{ K} = 127^\circ\text{C}$

Therefore, the saturation current at 400 K is

$$\begin{aligned} I_{o2} &= I_{o1} \times 2^{(T_2-T_1)/10} \\ &= 7.5 \times 10^{-6} \times 2^{(127-27)/10} \\ &= 7.5 \times 10^{-6} \times 2^{10} = 7.68 \text{ mA} \end{aligned}$$

### EXAMPLE 2.8

The reverse saturation current of the Ge transistor is  $2 \mu\text{A}$  at room temperature of  $25^\circ\text{C}$  and increases by a factor of 2 for each temperature increase of  $10^\circ\text{C}$ . Find the reverse saturation current of the transistor at a temperature of  $75^\circ\text{C}$ .

**Solution** Given  $I_{o1} = 2 \mu\text{A}$  at  $T_1 = 25^\circ\text{C}$ ,  $T_2 = 75^\circ\text{C}$

Therefore, the reverse saturation current of the transistor at  $T_2 = 75^\circ\text{C}$  is

$$\begin{aligned} I_{o2} &= I_{o1} \times 2^{(T_2-T_1)/10} = 2 \times 10^{-6} \times 2^{\left(\frac{75-25}{10}\right)} \\ &= 2 \times 10^{-6} \times 2^5 = 64 \mu\text{A} \end{aligned}$$

## 2.6 DIODE RESISTANCE (STATIC AND DYNAMIC)

An ideal diode should offer zero resistance in forward bias and infinite resistance in the reverse bias. But in practice, no diode can act as an ideal diode, i.e., an actual diode does not behave as a perfect conductor when forward biased and as a perfect insulator when reverse biased. Let us consider four resistances of the diode (i) dc or static resistance, (ii) ac or dynamic resistance, (iii) average ac resistance, and (iv) reverse resistance.

**dc or Static Resistance ( $R_F$ )** It is defined as the ratio of the voltage to the current,  $V/I$ , in the forward-bias characteristics of the  $PN$  junction diode. In the forward-bias characteristics of the diode as shown in Fig. 2.9, the dc or static resistance ( $R_F$ ) at the operating point can be determined by using the corresponding

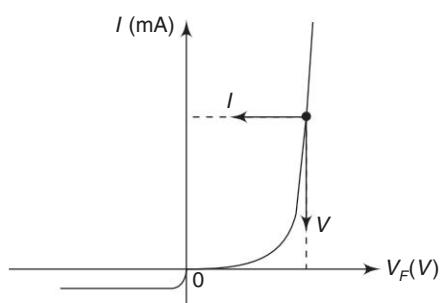


Fig. 2.9 Forward biasing of a diode

levels of the voltage  $V$  and current  $I$ , i.e.,  $R_F = \frac{V}{I}$ . Here, the dc resistance is independent of the shape of the characteristics in the region surrounding the point of interest. The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the characteristics above the knee. Hence, the dc resistance will be low when the diode current is high. As the static resistance varies widely with  $V$  and  $I$ , it is not a useful parameter.

**ac or Dynamic Resistance ( $r_f$ )** It is defined as the reciprocal of the slope of the volt-ampere characteristics.

$$r_f = \frac{\text{change in voltage}}{\text{resulting change in current}} = \frac{\Delta V}{\Delta I}$$

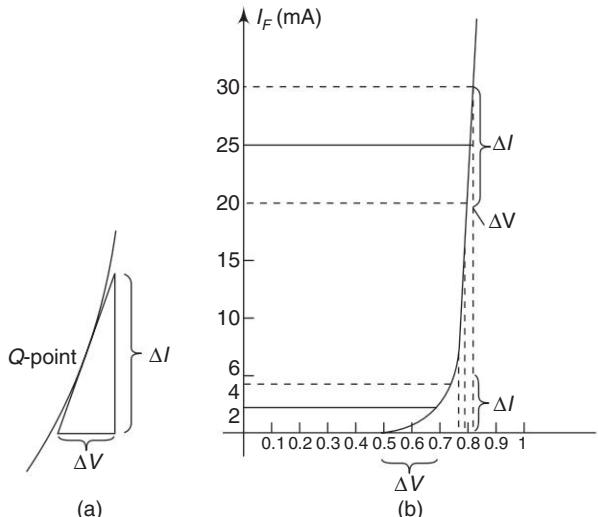
A straight line drawn tangent to the curve through the quiescent point ( $Q$ -point) as shown in Fig. 2.10(a) will define a specific change in voltage and current which may be used to determine the ac or dynamic resistance for this region of the diode characteristics. As shown in Fig. 2.10(b), for a small change in voltage, there will be a corresponding change in current, which is equidistant to either side of the  $Q$ -point. Hence, the ac or dynamic resistance is determined as  $r_f = \frac{\Delta V}{\Delta I}$ .

The derivative of a function at a point is equal to the slope of the tangent line drawn at the point. The Shockley's equation for the forward and reverse-bias regions is defined by

$$I = I_o (e^{V/\eta V_T} - 1)$$

Taking the derivative of the above equation w.r.t. the applied voltage,  $V$ , we get

$$\begin{aligned} \frac{dI}{dV} &= \frac{d}{dV} [I_o (e^{V/\eta V_T} - 1)] \\ &= I_o \left[ \frac{1}{\eta V_T} \cdot e^{V/\eta V_T} \right] \\ &= \frac{I_o e^{V/\eta V_T}}{\eta V_T} \\ &= \frac{I + I_o}{\eta V_T} \end{aligned}$$



**Fig. 2.10** Dynamic resistance

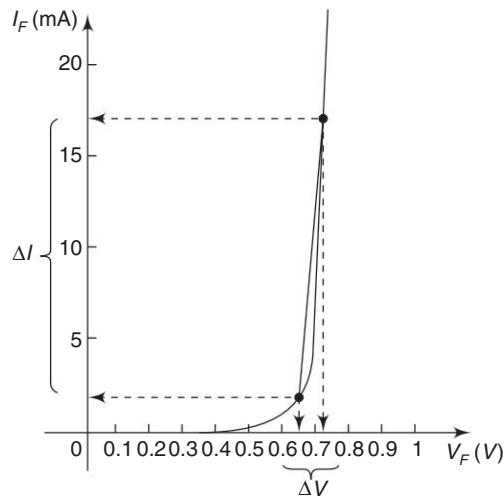
Generally,  $I \gg I_o$  in the vertical-slope section of the characteristics. Therefore,

$$\frac{dI}{dV} \cong \frac{I}{\eta V_T}$$

Therefore,  $\frac{dV}{dI} = r_f = \frac{\eta V_T}{I}$

The dynamic resistance varies inversely with current, i.e.,  $r_f = \frac{\eta V_T}{I}$ , where  $V_T = T/1600$ , the volt equivalent of temperature ( $T$ ) of the diode junction ( $K$ ) and  $\eta$  is a constant whose value is equal to 1 for germanium and 2 for silicon diodes. At room temperature  $V_T = 26$  mV.

The ac resistance of a diode is the sum of bulk resistance  $r_b$  and junction resistance  $r_j$ . Bulk resistance ( $r_b$ ) is the sum of ohmic resistance of the  $P$ - and  $N$ -type semiconductors.



**Fig. 2.11** Average ac resistance

**Average ac Resistance** It is the resistance associated with the device for the region if the input signal is sufficiently large to produce a wide range of the characteristics as shown in Fig. 2.11. Therefore,

$$r_{av} = \left. \frac{\Delta V}{\Delta I} \right|_{\text{point to point}}$$

As with the dc and ac resistance levels, the lower the level of currents used to determine the average, the higher is the resistance level.

**Reverse Resistance** It is the resistance offered by the  $PN$  junction diode under reverse-bias condition. It is very large compared to the forward resistance, which is in the range of several  $M\Omega$ .

### EXAMPLE 2.9

Determine the forward resistance of a  $PN$  junction diode when the forward current is 5 mA at  $T = 300$  K. Assume silicon diode.

**Solution** Given, for a silicon diode, the forward current,  $I = 5$  mA,  $T = 300$  K

Forward resistance of a  $PN$  junction diode,  $r_f = \frac{\eta V_T}{I}$ , where  $V_T = \frac{T}{11,600}$  and  $\eta = 2$  for silicon

$$\text{Therefore, } r_f = \frac{2 \times \frac{T}{11,600}}{5 \times 10^{-3}} = \frac{2 \times 300}{11,600 \times 5 \times 10^{-3}} = 10.34 \Omega$$

### EXAMPLE 2.10

Find the value of dc resistance and ac resistance of a germanium junction diode at  $25^\circ\text{C}$  with  $I_o = 25$   $\mu\text{A}$  and at an applied voltage of 0.2 V across the diode.

**Solution** Given  $I_o = 25$   $\mu\text{A}$ ,  $T = 25^\circ\text{C} = 298$  K and  $V = 0.2$  volt

$$I = I_o \left( \frac{V}{e^{\eta V_T} - 1} \right) = 25 \times 10^{-6} \left( \frac{0.2}{e^{26 \times 10^{-3}} - 1} \right) = 54.79 \text{ mA}$$

dc resistance  $R_F = \frac{V}{I} = \frac{0.2}{54.79 \times 10^{-3}} = 3.65 \Omega$

For germanium,  $\eta = 1, V_T = \frac{KT}{q} = 25.71 \text{ mV}$

ac resistance  $r_f = \frac{\eta V_T}{I} = \frac{25.71 \times 10^{-3}}{54.79 \times 10^{-3}} = 0.47 \Omega$

### EXAMPLE 2.11

Calculate the dynamic forward and reverse resistances of a *PN* junction diode when the applied voltage is 0.25 V at  $T = 300 \text{ K}$  given  $I_o = 2 \mu\text{A}$ .

**Solution** Given  $V = 0.25 \text{ V}, T = 300 \text{ K}, I_o = 2 \mu\text{A}$

At  $T = 300 \text{ K}$ ,  $V_T = 26 \text{ mV}$ .

Assuming it to be a silicon diode,  $\eta = 2$

Therefore,  $I = I_o \left( e^{\frac{V}{\eta V_T}} - 1 \right) = 2 \times 10^{-6} \left( e^{\frac{0.25}{2 \times 26 \times 10^{-3}}} - 1 \right) = 0.24 \text{ mA}$

$$r_f = \frac{\eta V_T}{I} = \frac{2 \times 26 \times 10^{-3}}{0.24 \times 10^{-3}} = 216.67 \Omega$$

For a germanium diode,  $\eta = 1$

$$I = I_o \left( e^{\frac{V}{\eta V_T}} - 1 \right) = 2 \times 10^{-6} \left( e^{\frac{0.25}{26 \times 10^{-3}}} - 1 \right) = 0.03 \text{ A}$$

$$r_f = \frac{\eta V_T}{I} = \frac{26 \times 10^{-3}}{0.03} = 0.867 \Omega$$

Reverse resistance,  $\frac{V}{I_o} = \frac{0.25}{2 \times 10^{-6}} = 125 \text{ k}\Omega$

### EXAMPLE 2.12

A *PN* junction diode has a reverse saturation current of  $30 \mu\text{A}$  at a temperature, of  $125^\circ\text{C}$ . At the same temperature, find the dynamic resistance for 0.2 V bias in forward and reverse directions.

**Solution** Given the reverse saturation current,  $I_o = 30 \times 10^{-6} \text{ A}$  and  $V = 0.2 \text{ V}$

We know that, the dynamic resistance,  $r_f = \frac{\eta V_T}{I_o e^{V/\eta V_T}}$

Here,  $\eta = 1$  for germanium and  $V_T = \frac{T}{11,600} = \frac{125 + 273}{11,600} = 34.3 \text{ mV}$

Therefore, forward dynamic resistance,  $r_f = \frac{34.3 \times 10^{-3}}{30 \times 10^{-6} (e^{0.2/34.3 \times 10^{-3}})} = 3.356 \Omega$

$$\text{Reverse dynamic resistance, } r_r = \frac{\eta V_T}{I_o e^{-V/\eta V_T}} = \frac{34.3 \times 10^{-3}}{30 \times 10^{-6} (e^{-0.2/34.3 \times 10^{-3}})} = 389.5 \text{ k}\Omega$$

**EXAMPLE 2.13**

If two similar germanium diodes are connected back to back and the voltage  $V$  is impressed upon, calculate the voltage across each diode and current through each diode. Assume similar value of  $I_o = 1 \mu\text{A}$  for both the diodes and  $\eta = 1$ .

**Solution** The arrangement is shown in Fig. 2.12.

As  $D_1$  is reverse biased, the total current flowing in the circuit is  $I_o = 1 \mu\text{A}$ . The diode  $D_2$  is forward biased and its forward current is equal to the reverse current  $I_o = 1 \mu\text{A}$ , which can flow as  $D_1$  is reverse biased.

For the diode  $D_2$ ,  $I = I_o = 1 \mu\text{A}$  and voltage across  $D_2$  is  $V_{D_2}$ .

Therefore,  $I = I_o [e^{V/\eta V_T} - 1]$

or  $I = I_o [e^{V_{D_2}/\eta V_T} - 1]$

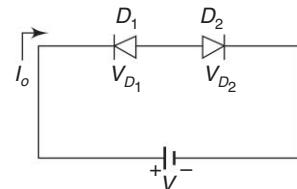
Hence,  $e^{V_{D_2}/\eta V_T} = 1 + 1 = 2$

$$\frac{V_{D_2}}{\eta V_T} = \ln 2$$

$$V_{D_2} = \eta V_T \times \ln 2 = 1 \times 26 \times 10^{-3} \times 0.6931 = 0.01802 \text{ V}$$

Therefore,  $V_{D_1} = V - V_{D_2} = V - 0.01802 \text{ V}$

The current through the diodes  $D_1$  and  $D_2$  is  $I = I_0 = 1 \mu\text{A}$

**Fig. 2.12****EXAMPLE 2.14**

Determine the forward resistance of a  $PN$  junction diode, when the forward current is  $5 \text{ mA}$  at  $T = 300 \text{ K}$ . Assume silicon diode.

**Solution** Given, for a silicon diode, the forward current,  $I = 5 \text{ mA}$ .  $T = 300 \text{ K}$

Forward resistance of a  $PN$  junction diode,  $r_f = \frac{\eta V_T}{I}$  where  $V_T = \frac{T}{11,600}$  and  $\eta = 2$  for silicon

$$\text{Therefore, } r_f = \frac{2 \times \frac{T}{11,600}}{5 \times 10^{-3}} = \frac{2 \times 300}{11,600 \times 5 \times 10^{-3}} = 10.34 \Omega$$

**2.7 DIODE CAPACITANCE****2.7.1 Transition or Space Charge (or Depletion Region) Capacitance ( $C_T$ )**

Under reverse-bias condition, the majority carriers move away from the junction, thereby uncovering more immobile charges. Hence, the width of the space-charge layer at the junction increases with reverse voltage. This increase in uncovered charge with applied voltage may be considered a capacitive effect. The parallel

layers of oppositely charged immobile ions on the two sides of the junction form the capacitance,  $C_T$ , which is expressed as

$$C_T = \left| \frac{dQ}{dV} \right|$$

where  $dQ$  is the increase in charge caused by a change in voltage  $dV$ . A change in voltage  $dV$  in a time  $dt$  will result in a current  $I = dQ/dt$  given by

$$I = C_T \frac{dV}{dt}$$

Therefore,  $C_T$  is important while considering a diode or a transistor as a circuit element. The quantity  $C_T$  is called the transition, space-charge, barrier or depletion region capacitance.

### Step-graded Junction

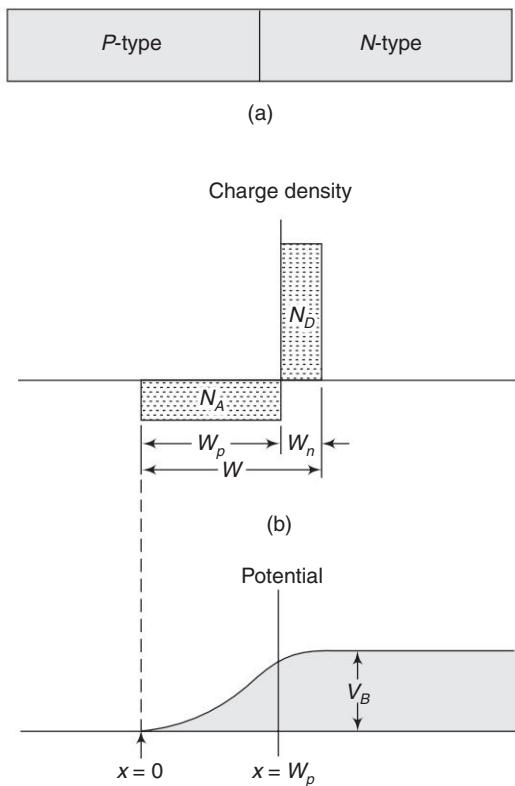
A  $PN$  junction is formed from a single-crystal intrinsic semiconductor by doping part of it with acceptor impurities and the remaining with donors. A junction between  $P$ -type and  $N$ -type materials may be fabricated in a variety of ways.

The change in impurity concentration from  $P$  to  $N$ -type semiconductor occurs in a very short length, typically much less than  $1\text{ }\mu\text{m}$ . In an abrupt  $PN$  junction, there is a sudden step change from acceptor ions on one side to donor ions on the other side. Such a junction is fabricated by placing trivalent indium against  $N$ -type germanium and heating the combination to a high temperature for a short time. Since some of the indium dissolves into the germanium, the  $N$ -type germanium is changed into  $P$ -type at the junction. Such a step-graded junction is called an *alloy*, or *fusion junction*. A step-graded junction is also formed between the emitter and base of an integrated transistor.

A diffused junction is graded in which case the donor and acceptor concentrations are functions of distance across the junction. Then the acceptor density,  $N_A$ , gradually decreases and the donor density,  $N_D$ , gradually increases till  $N_A = N_D$  is reached. Therefore,  $N_D$  increases and  $N_A$  decreases to zero.

It is not necessary for the abrupt junction to be symmetrical, that is, the doping concentrations at either side of the junction are dissimilar.

As shown in Fig. 2.13, consider a  $PN$  diode which is asymmetrically doped at the junction. Since the net charge is zero then  $qN_A W_p = qN_D W_n$ .



**Fig. 2.13** Charge density and potential variation at an alloy  $PN$  junction

If  $N_A \gg N_D$  then  $W_p \ll W_n \approx W$ . The relationship between potential and charge density is given by the Poisson's equation,  $\frac{d^2V}{dx^2} = \frac{qN_A}{\epsilon}$

Integrating the above equation twice,

$$\iint d^2V = \iint \frac{qN_A}{\epsilon} dx^2$$

Therefore,  $V = \frac{qN_A x^2}{2\epsilon}$

At  $x = W_p \approx W$ ,  $V = V_B$ , the barrier potential that appears across the uncovered acceptor ions. Thus,

$$V_B = \frac{qN_A W^2}{2\epsilon} \quad (2.11)$$

Here,  $V_B = V_0 - V$ , where  $V$  is a negative number for an applied reverse bias and  $V_0$  is the contact potential. Hence, the width of the depletion layer increases with applied reverse voltage, i.e.,  $V_B \propto W^2$ . Therefore,  $W \propto \sqrt{V_B}$ .

The total charge density of a *P*-type material with area of the junction  $A$  is given by

$$Q = qN_A WA$$

Differentiating the above equation w.r.t.  $V$ , we get

$$C_T = \left| \frac{dQ}{dV} \right| = AqN_A \left| \frac{dW}{dV} \right| \quad (2.12)$$

Differentiating Eq. (2.11) w.r.t.  $V$ , we get

$$1 = \frac{qN_A 2W}{2\epsilon} \left| \frac{dW}{dV} \right|$$

Therefore,  $\left| \frac{dW}{dV} \right| = \frac{\epsilon}{qN_A W} \quad (2.13)$

Substituting Eq. (2.13) in Eq. (2.12), we get

$$C_T = \left| \frac{dQ}{dV} \right| = AqN_A \frac{\epsilon}{qN_A W}$$

Therefore,  $C_T = \frac{\epsilon A}{W}$

Here,  $\epsilon$  is the permittivity of the material,  $A$  the cross-sectional area of the junction and  $W$  is the width of the depletion layer over which the ions are uncovered. The depletion width,  $W$ , is given by

$$W = \left[ \frac{2\epsilon_r \epsilon (V_o - V)}{q} \left( \frac{N_A + N_D}{N_A N_D} \right) \right]^{1/2}$$

where  $V$  is the applied voltage and  $V_o$  is the barrier potential, or the contact potential.

When no external voltage is applied, i.e.,  $V = 0$ , the width of the depletion region of a  $PN$  junction diode is of the order of 0.5 microns. The movement of majority carriers across the junction causes opposite charges to be stored at this distance  $W$  apart. This depletion region acts as a dielectric between the two conducting  $P$ - and  $N$ -regions. Therefore, these regions act as a parallel-plate capacitor whose transition capacitance  $C_T$  is approximately 20 pF with no external bias.

When a forward bias of  $+V$  is applied, the effective barrier potential,  $V_B = [V_o - (+V)]$ , is lowered and hence, the width of the depletion region  $W$  decreases and  $C_T$  increases. Under reverse-bias condition, the majority carriers move away from the junction, thereby uncovering more immobile charges. Now the effective barrier potential,  $V_B = [V_o - (-V)]$ , is increased and, hence,  $W$  increases with reverse voltage and  $C_T$  decreases correspondingly. The values of  $C_T$  range from 5 to 200 pF, the larger values being for the high-power diodes. This property of voltage variable capacitance with the reverse bias appears in varactors, vari-caps or volta-caps.

### 2.7.2 Diffusion Capacitance ( $C_D$ )

The capacitance that exists in a forward-biased junction is called a diffusion or storage capacitance ( $C_D$ ), whose value is usually much larger than  $C_T$ , which exists in a reverse-biased junction. This is also defined as

the rate of change of injected charge with applied voltage, i.e.,  $C_D = \frac{dQ}{dV}$ , where  $dQ$  represents the change

in the number of minority carriers stored outside the depletion region when a change in voltage across the diode,  $dV$ , is applied.

**Calculation of  $C_D$**  Let us assume that the  $P$ -material in one side of the diode is heavily doped in comparison with the  $N$ -side. Since the holes move from the  $P$ - to the  $N$ -side, the hole current  $I \approx I_{pn}(0)$ .

The excess minority charge  $Q$  existing on the  $N$ -side is given by

$$Q = \int_0^{\infty} AqP_n(0)e^{-x/L_p} dx = \left[ \frac{AqP_n(0)e^{-x/L_p}}{-1/L_p} \right]_0^{\infty} = L_p AqP_n(0)$$

Differentiating the above equation, we get

$$C_D = \frac{dQ}{dV} = AqL_p \frac{d[P_n(0)]}{dV} \quad (2.14)$$

We know that the diffusion hole current in the  $N$ -side is  $I_{pn}(x) = AqD_p P_n(0)/L_p e^{-x/L_p}$ . The hole current crossing

the junction into the  $N$ -side with  $x = 0$  is  $I_{pn}(0) = \frac{AqD_p P_n(0)}{L_p}$ .

Therefore, 
$$I = \frac{AqD_p P_n(0)}{L_p}$$

$$P_n(0) = \frac{IL_p}{AqD_p}$$

Differentiating the above equation w.r.t.  $V$ , we get

$$\frac{d[P_n(0)]}{dV} = \frac{dI}{dV} \frac{L_p}{AqD_p}$$

Upon substituting in Eq. (2.14), we have

$$C_D = \frac{dQ}{dV} = \frac{dI L_p^2}{dV D_p}$$

Therefore,  $C_D = g\tau$ , where  $g = \frac{dI}{dV}$  is the diode conductance and  $\tau = \frac{L_p^2}{D_p}$  is the mean lifetime of holes in the  $N$ -region.

From the diode-current equation,  $g = \frac{I}{\eta V_T}$

Therefore,  $C_D = \frac{\tau I}{\eta V_T}$

where  $\tau$  is the mean lifetime for holes and electrons.

Diffusion capacitance  $C_D$  increases exponentially with forward bias or, alternatively, that it is proportional to diode forward current,  $I$ . The values of  $C_D$  range from 10 to 1000 pF, the larger values being associated with the diode carrying a larger anode current,  $I$ .

The effect of  $C_D$  is negligible for a reverse-biased  $PN$  junction. As the value of  $C_D$  is inversely proportional to frequency, it is high at low frequencies and it decreases with the increase in frequency.

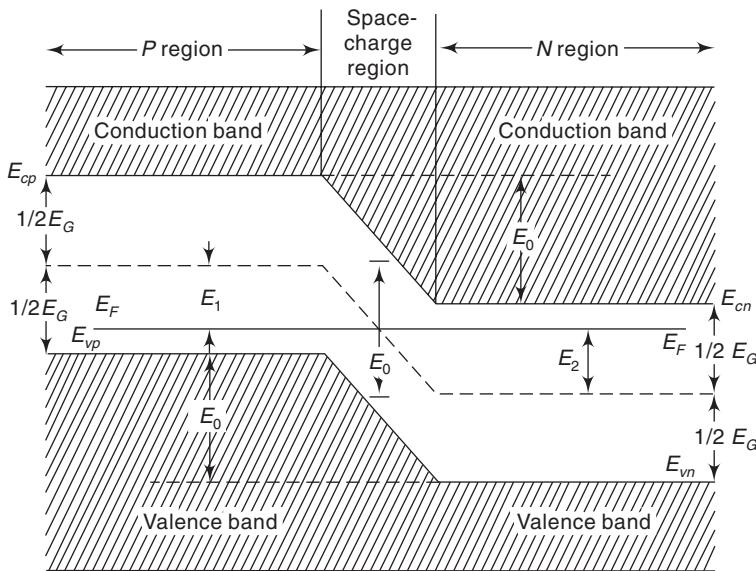
## 2.8 ENERGY-BAND DIAGRAM OF $PN$ JUNCTION DIODE

Consider that a  $PN$  junction has  $P$ -type and  $N$ -type materials in close physical contact at the junction on an atomic scale. Hence, the energy-band diagrams of these two regions undergo relative shift to equalise the Fermi level. The Fermi level  $E_F$  should be constant throughout the specimen at equilibrium. The distribution of electrons or holes in allowed energy states is dependent on the position of the Fermi level. If this is not so, electrons on one side of the junction would have an average energy higher than those on the other side, and this causes transfer of electrons and energy until the Fermi levels on the two sides get equalized. However, such a shift does not disturb the relative position of the conduction band, valence band, and Fermi level in any region. Equalization of Fermi levels in the  $P$  and  $N$  materials of a  $PN$  junction is similar to equalization of levels of water in two containers on being joined together.

The energy-band diagram for a  $PN$  junction is shown in Fig. 2.14, where the Fermi level  $E_F$  is closer to the conduction-band edge  $E_{cn}$  in the  $N$ -type material while it is closer to the valence-band edge  $E_{vp}$  in the  $P$ -type material. It is clear that the conduction-band edge  $E_{cp}$  in the  $P$ -type material is higher than the conduction band edge  $E_{cn}$  in the  $N$ -type material. Similarly, the valence-band edge  $E_{vp}$  in the  $P$ -type material is higher than the valence-band edge  $E_{vn}$  in the  $N$ -type material. As illustrated in Fig. 2.14,  $E_1$  and  $E_2$  indicate the shifts in the Fermi level from the intrinsic conditions in the  $P$  and  $N$  materials respectively. Then the total shift in the energy level  $E_0$  is given by

$$E_0 = E_1 + E_2 = E_{cp} - E_{cn} = E_{vp} - E_{vn}$$

This energy  $E_0$  (in eV) is the potential energy of the electrons at the  $PN$  junction, and is equal to  $qV_0$ , where  $V_0$  is the contact potential (in volt) or contact difference of potential or the barrier potential.



**Fig. 2.14 Energy-band structure**

**Contact Difference of Potential** A contact difference of potential exists across an open-circuited *PN* junction. We now proceed to obtain an expression for  $E_0$ . From Fig. 2.14, we find that

$$E_F - E_{vp} = \frac{1}{2} E_G - E_1 \quad (2.15)$$

$$E_{cn} - E_F = \frac{1}{2} E_G - E_2 \quad (2.16)$$

Combining Eqs (2.15) and (2.16), we get

$$E_0 = E_1 + E_2 = E_G - (E_{cn} - E_F) - (E_F - E_{vp}) \quad (2.17)$$

We know that

$$np = N_C N_V e^{-E_G/kT}$$

and

$$np = n_i^2 \text{ (Mass-action law)}$$

From the above equations, we get

$$E_G = kT \ln \frac{N_C N_V}{n_i^2} \quad (2.18)$$

We know that for an *N*-type material,  $E_F = E_C - kT \ln \frac{N_C}{N_D}$ . Therefore, from this equation, we get

$$E_{cn} - E_F = kT \ln \frac{N_C}{n_n} = kT \ln \frac{N_C}{N_D} \quad (2.19)$$

Similarly, for a *P*-type material,  $E_F = E_V + kT \ln \frac{N_V}{N_A}$ . Therefore, from this equation, we get

$$E_F - E_{vp} = kT \ln \frac{N_V}{p_p} = kT \ln \frac{N_V}{N_A} \quad (2.20)$$

Substituting from Eqs (2.18), (2.19), and (2.20) into Eq. (2.17), we get

$$\begin{aligned} E_0 &= kT \left[ \ln \frac{N_C N_V}{n_i^2} - \ln \frac{N_C}{N_D} - \ln \frac{N_V}{N_A} \right] \\ &= kT \ln \left[ \frac{N_C N_V}{n_i^2} \times \frac{N_D}{N_C} \times \frac{N_A}{N_V} \right] \\ &= kT \ln \frac{N_D N_A}{n_i^2} \end{aligned} \quad (2.21)$$

As  $E_0 = qV_0$ , the contact difference of potential or barrier voltage is given by

$$V_0 = \frac{kT}{q} \ln \frac{N_D N_A}{n_i^2}$$

In the above equations,  $E$  is in electronvolt and  $k$  is in electronvolt per degree Kelvin. The contact difference of potential  $V_0$  is expressed in volt and is numerically equal to  $E_0$ . From Eq. (2.21), we note that  $E_0$  (hence,  $V_0$ ) depends upon the equilibrium concentrations and not on the charge density in the transition region.

An alternative expression for  $E_0$  may be obtained by substituting the equations of  $n_n \approx N_D$ ,  $p_n = \frac{n_i^2}{N_D}$ ,

$n_n p_p = n_i^2$ ,  $p_p \approx N_A$  and  $n_p = \frac{n_i^2}{N_A}$  into Eq. (2.21). Then we get

$$E_0 = kT \ln \frac{p_{p0}}{p_{n0}} = kT \ln \frac{n_{n0}}{n_{p0}} \quad (2.22)$$

where the subscript 0 represents the thermal equilibrium condition.

### EXAMPLE 2.14

The resistivities of the *P*-region and *N*-region of a germanium diode are  $6 \Omega\text{-cm}$  and  $4 \Omega\text{-cm}$ , respectively.

(a) Calculate the contact potential  $V_0$  and potential energy barrier  $E_0$ . (b) If the doping densities of both *P* and *N*-regions are doubled, determine  $V_0$  and  $E_0$ . Given that  $q = 1.602 \times 10^{-19} \text{ C}$ ,  $n_i = 2.5 \times 10^{13}/\text{cm}^3$ ,  $\mu_p = 1800 \text{ cm}^2/\text{V}\cdot\text{s}$ ,  $\mu_n = 3800 \text{ cm}^2/\text{V}\cdot\text{s}$ , and  $V_T = 0.026 \text{ V}$  at  $300 \text{ K}$ .

#### Solution

$$(a) \text{ Resistivity, } \rho = \frac{1}{\sigma} = \frac{1}{N_A q \mu_p} = 6 \Omega\text{-cm}$$

Therefore,

$$N_A = \frac{1}{6q\mu_p} = \frac{1}{6 \times 1.602 \times 10^{-19} \times 1800} = 0.579 \times 10^{15}/\text{cm}^3$$

Similarly,

$$N_D = \frac{1}{4q\mu_n} = \frac{1}{4 \times 1.602 \times 10^{-19} \times 3800} = 0.411 \times 10^{15} / \text{cm}^3$$

Therefore,

$$V_0 = V_T \ln \frac{N_D N_A}{n_i^2} = 0.026 \ln \frac{0.579 \times 0.411 \times 10^{30}}{(2.5 \times 10^{13})^2} = 0.1545 \text{ V}$$

Hence,

$$E_0 = 0.1545 \text{ eV}$$

(b)

$$V_0 = 0.026 \ln \frac{2 \times 0.579 \times 10^{15} \times 2 \times 0.411 \times 10^{15}}{(2.5 \times 10^{13})^2} = 0.1906 \text{ V}$$

Therefore,

$$E_0 = 0.1906 \text{ eV}$$

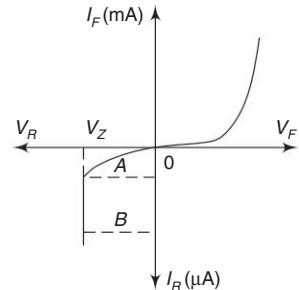
## 2.9 ZENER DIODE

When the reverse voltage reaches breakdown voltage in a normal *PN* junction diode, the current through the junction and the power dissipated at the junction will be high. Such an operation is destructive and the diode gets damaged. Whereas diodes can be designed with adequate power dissipation capabilities to operate in the breakdown region. One such diode is known as the Zener diode. The Zener diode is heavily doped than the ordinary diode.

From the *V-I* characteristics of the Zener diode, shown in Fig. 2.15, it is found that the operation of the Zener diode is same as that of an ordinary *PN* diode under forward-biased condition. Whereas under reverse-biased condition, breakdown of the junction occurs. The breakdown voltage depends upon the amount of doping. If the diode is heavily doped, the depletion layer will be thin and, consequently, breakdown occurs at lower reverse voltage and further, the breakdown voltage is sharp. Whereas a lightly doped diode has a higher breakdown voltage. Thus, breakdown voltage can be selected with the amount of doping.

The sharp increasing currents under breakdown conditions are due to the following two mechanisms.

1. Avalanche breakdown
2. Zener breakdown



**Fig. 2.15** *V-I* characteristics of a Zener diode

## 2.10 AVALANCHE AND ZENER BREAKDOWN MECHANISM

### Avalanche breakdown

As the applied reverse bias increases, the field across the junction increases correspondingly. Thermally generated carriers, while traversing the junction, acquire a large amount of kinetic energy from this field. As a result, the velocity of these carriers increases. These electrons disrupt covalent bond by colliding with immobile ions and create new electron-hole pairs. These new carriers again acquire sufficient energy from the field and collide with other immobile ions thereby generating further electron-hole pairs. This process is cumulative in nature and results in generation of avalanche of charge carriers within a short time. This mechanism of carrier generation is known as *avalanche multiplication*. This process results in flow of large amount of current at the same value of reverse bias.

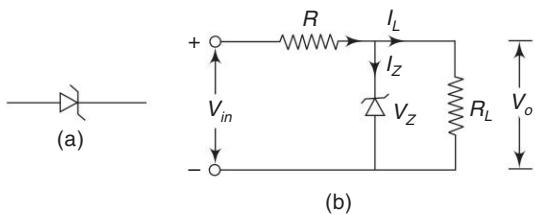
### Zener Breakdown

When the *P*- and *N*-regions are heavily doped, direct rupture of covalent bonds takes place because of the strong electric fields, at the junction of the *PN* diode. The new electron-hole pairs so created increase the reverse current in a reverse-biased *PN* diode. The increase in current takes place at a constant value of reverse bias typically below 6 V for heavily doped diodes. As a result of heavy doping of *P*- and *N*-regions, the depletion-region width becomes very small and for an applied voltage of 6 V or less, the field across the depletion region becomes very high, of the order of  $10^7$  V/m, making conditions suitable for Zener breakdown. For lightly doped diodes, Zener breakdown voltage becomes high and breakdown is then predominantly by avalanche multiplication. Though Zener breakdown occurs for lower breakdown voltage and avalanche breakdown occurs for higher breakdown voltage, such diodes are normally called Zener diodes.

## 2.11 ZENER DIODE APPLICATIONS

From the Zener characteristics shown in Fig. 2.15, under the reverse-bias condition, the voltage across the diode remains almost constant although the current through the diode increases as shown in region *AB*. Thus, the voltage across the Zener diode serves as a reference voltage. Hence, the diode can be used as a voltage regulator.

In Fig. 2.16, it is required to provide constant voltage across load resistance  $R_L$ , whereas the input voltage may be varying over a range. As shown, Zener diode is reverse biased and as long as the input voltage does not fall below  $V_Z$  (Zener breakdown voltage), the voltage across the diode will be constant and hence the load voltage will also be constant.



**Fig. 2.16** Zener diode: (a) Circuit symbol  
(b) As a voltage regulator

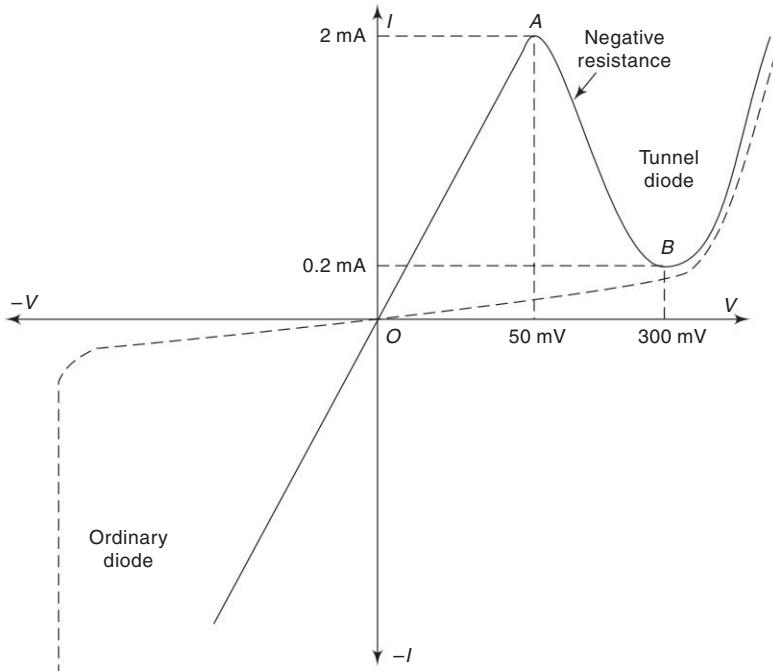
## 2.12 TUNNEL DIODE

The tunnel diode, or Esaki diode, is a thin-junction diode which exhibits negative resistance under low forward-bias conditions.

An ordinary *PN* junction diode has an impurity concentration of about 1 part in  $10^8$ . With this amount of doping, the width of the depletion layer is of the order of 5 microns. This potential barrier restrains the flow of carriers from the majority carrier side to the minority carrier side. If the concentration of impurity atoms is greatly increased to the level of 1 part in  $10^3$ , the device characteristics are completely changed. The width of the junction barrier varies inversely as the square root of the impurity concentration and, therefore, is reduced from 5 microns to less than 100 Å ( $10^{-8}$  m). This thickness is only about 1/50th of the wavelength of visible light. For such thin potential-energy barriers, the electrons will penetrate through the junction rather than surmounting them. This quantum mechanical behavior is referred to as tunneling and hence, these high-impurity-density *PN* junction devices are called tunnel diodes.

The  $V$ - $I$  characteristic for a typical germanium tunnel diode is shown in Fig. 2.17. It is seen that at first forward current rises sharply as applied voltage is increased, where it would have risen slowly for an ordinary *PN* junction diode (which is shown as dashed line for comparison). Also, reverse current is much larger for comparable back bias than in other diodes due to the thinness of the junction. The interesting portion of the characteristic starts at the point *A* on the curve, i.e., the peak voltage. As the forward bias is increased beyond

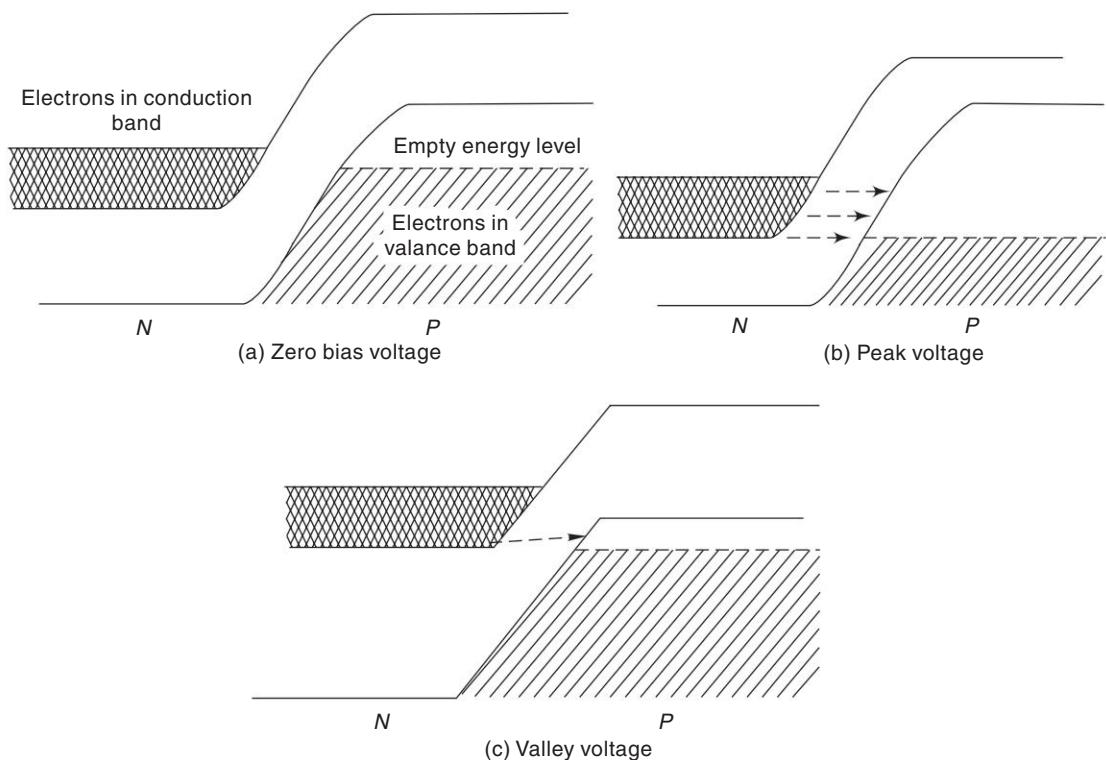
this point, the forward current drops and continues to drop until point *B* is reached. This is the valley voltage. At *B*, the current starts to increase once again and does so very rapidly as bias is increased further. Beyond this point, the characteristic resembles that of an ordinary diode. Apart from the peak voltage and valley voltage, the other two parameters normally used to specify the diode behaviour are the peak current and the peak-to-valley current ratio, which are 2 mA and 10 respectively, as shown.



**Fig. 2.17** *V*–*I* characteristic of a tunnel diode

The *V*–*I* characteristic of the tunnel diode illustrates that it exhibits dynamic resistance between *A* and *B*. Figure 2.18 shows energy level diagrams of the tunnel diode for three interesting bias levels. The shaded areas show the energy states occupied by electrons in the valence band, whereas the cross hatched regions represent energy states in the conduction band occupied by the electrons. The levels to which the energy states are occupied by electrons on either side of the junctions are shown by dotted lines. When the bias is zero, these lines are at the same height. Unless energy is imparted to the electrons from some external source, the energy possessed by the electrons on the *N*-side of the junction is insufficient to permit them to climb over the junction barrier to reach the *P*-side. However, quantum mechanics show that there is a finite probability for the electrons to tunnel through the junction to reach the other side, provided there are allowed empty energy states in the *P*-side of the junction at the same energy level. Hence, the forward current is zero.

When a small forward bias is applied to the junction, the energy level of the *P*-side is lower as compared with the *N*-side. As shown in Fig. 2.18(b), electrons in the conduction band of the *N*-side see an empty energy level on the *P*-side. Hence, tunnelling from *N*-side to *P*-side takes place. Tunnelling in other directions is not possible because the valence band electrons on the *P*-side are now opposite to the forbidden energy gap on the *N*-side. The energy band diagram shown in Fig. 2.18(b), is for the peak of the diode characteristic.



**Fig. 2.18** Energy level diagrams of tunnel diode

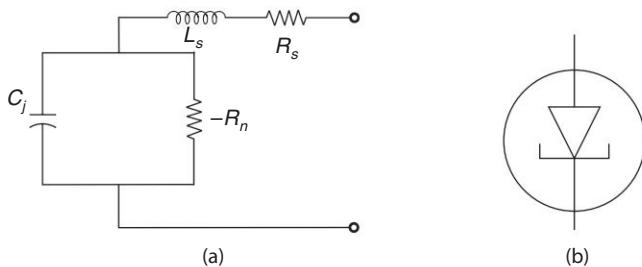
When the forward bias is raised beyond this point, tunnelling will decrease as shown in Fig. 2.18(c). The energy of the *P*-side is now depressed further, with the result that fewer conduction band electrons on the *N*-side are opposite to the unoccupied *P*-side energy levels. As the bias is raised, forward current drops. This corresponds to the negative resistance region of the diode characteristic. As forward bias is raised still further, tunnelling stops altogether and it behaves as a normal *PN* junction diode.

### 2.12.1 Equivalent Circuit

The equivalent circuit of the tunnel diode, when biased in the negative resistance region, is as shown in Fig. 2.19(a). In the circuit,  $R_s$  is the series resistance and  $L_s$  is the series inductance which may be ignored except at highest frequencies. The resulting diode equivalent circuit is thus reduced to parallel combination of the junction capacitance  $C_j$  and the negative resistance  $-R_n$ . Typical values of the circuit components are  $R_s = 6 \Omega$ ,  $L_s = 0.1 \text{ nH}$ ,  $C_j = 0.6 \text{ pF}$  and  $R_n = 75 \Omega$ .

**Applications** Tunnel diode is used as

1. An ultra-high speed switch with switching speed of the order of *ns* or *ps*
2. Logic memory storage device
3. Microwave oscillator
4. A relaxation oscillator circuit
5. An amplifier



**Fig. 2.19** (a) Equivalent circuit of a tunnel diode (b) Symbol of a tunnel diode

### Advantages

1. Low noise
2. Ease of operation
3. High speed
4. Low power

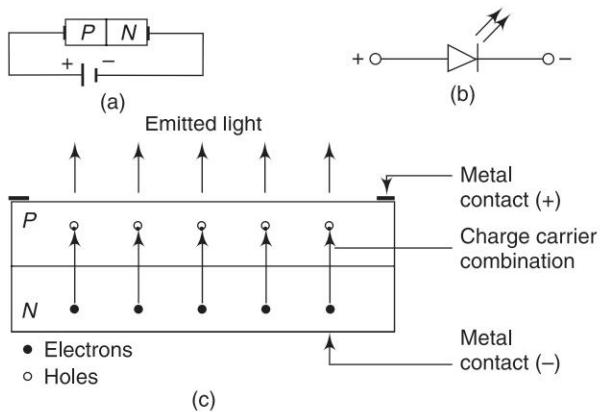
### Disadvantages

1. Voltage range over which it can be operated is 1 V or less.
2. Being a two-terminal device, there is no isolation between the input and output circuits.

## 2.13 LIGHT EMITTING DIODE (LED)

The Light Emitting Diode (LED) is a *PN* junction device which emits light when forward biased, by a phenomenon called electroluminescence. In all semiconductor *PN* junctions, some of the energy will be radiated as heat and some in the form of photons. In silicon and germanium, greater percentage of energy is given out in the form of heat and the emitted light is insignificant. In other materials such as gallium phosphide (GaP) or gallium arsenide phosphide (GaAsP), the number of photons of light energy emitted is sufficient to create a visible light source. Here, the charge carrier recombination takes place when electrons from the *N*-side cross the junction and recombine with the holes on the *P*-side.

LED under forward bias and its symbol are shown in Figs 2.20(a) and (b), respectively. When an LED is forward biased, the electrons and holes move towards the junction and recombination takes place. As a result of recombination, the electrons lying in the conduction bands of *N*-region fall into the holes lying in the valence band of a *P*-region. The difference of energy between the conduction band and the valence band is radiated in the form of light energy. Each recombination causes radiation of light energy. Light is generated by recombination of electrons



**Fig. 2.20** LED (a) LED under forward bias (b) Symbol (c) Recombinations and emission of light

and holes whereby their excess energy is transferred to an emitted photon. The brightness of the emitted light is directly proportional to the forward-bias current.

Figure 2.20(c) shows the basic structure of an LED showing recombination of carriers and emission of light. Here, an *N*-type layer is grown on a substrate and a *P*-type is deposited on it by diffusion. Since carrier recombination takes place in the *P*-layer, it is kept uppermost. The metal anode connections are made at the outer edges of the *P*-layer so as to allow more central surface area for the light to escape. LEDs are manufactured with domed lenses in order to reduce the reabsorption problem. A metal (gold) film is applied to the bottom of the substrate for reflecting as much light as possible to the surface of the device and also to provide cathode connection. LEDs are always encased to protect their delicate wires.

The efficiency of generation of light increases with the increases in injected current and with a decrease in temperature. The light is concentrated near the junction as the carriers are available within a diffusion length of the junction.

LEDs radiate different colours such as red, green, yellow, orange, blue and white. Some of the LEDs emit infrared (invisible) light also. The wavelength of emitted light depends on the energy gap of the material. Hence, the colour of the emitted light depends on the type of material used is given as follows.

Gallium arsenide (GaAs) – infrared radiation (invisible)

Gallium phosphide (GaP) – red or green

Gallium arsenide phosphide (GaAsP) – red or yellow

In order to protect LEDs, resistance of  $1\text{ k}\Omega$  or  $1.5\text{ k}\Omega$  must be connected in series with the LED. LEDs emit no light when reverse biased. LEDs operate at voltage levels from 1.5 to 3.3 V, with the current of some tens of milliamperes. The power requirement is typically from 10 to 150 mW with a lifetime of 1,00,000 + hours. LEDs can be switched ON and OFF at a very fast speed of 1 ns.

They are used in burglar alarm systems, picture phones, multimeters, calculators, digital meters, microprocessors, digital computers, electronic telephone exchange, intercoms, electronic panels, digital watches, solid state video displays, and optical communication systems. Also, there are two-lead LED lamps which contain two LEDs, so that a reversal in biasing will change the colour from green to red, or vice-versa.

When the emitted light is coherent, i.e., essentially monocromatic, then such a diode is referred to as an Injection Laser Diode (ILD). The LED and ILD are the two main types used as optical sources. ILD has a shorter rise time than LED, which makes the ILD more suitable for wide-bandwidth and high-data-rate applications. In addition, more optical power can be coupled into a fibre with an ILD, which is important for long distance transmission. A disadvantage of the ILD is the strong temperature dependence of the output characteristic curve.

## 2.14 PHOTODIODE

Silicon photodiode is a light-sensitive device, also called photodetector, which converts light into electrical signals. The construction and symbol of a photodiode are shown in Fig. 2.21. The diode is made of a semiconductor PN junction kept in a sealed plastic or glass casing. The cover is so designed that the light rays are allowed to fall on one surface across the junction. The remaining sides of the casing are painted to restrict the penetration of light rays. A lens permits light to fall on the junction. When light falls on the reverse-biased PN photodiode junction, hole-electron pairs are created. The movement of these hole-electron pairs in a

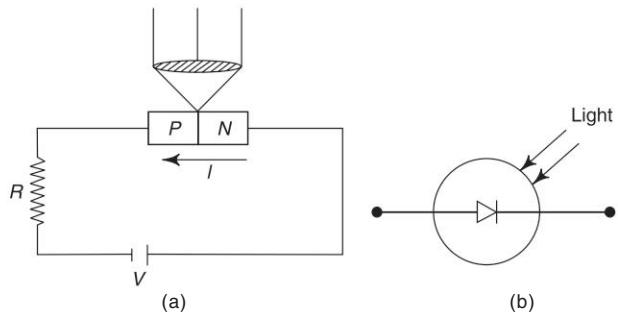
properly connected circuit results in current flow. The magnitude of the photocurrent depends on the number of charge carriers generated and hence, on the illumination of the diode element. This current is also affected by the frequency of the light falling on the junction of the photodiode. The magnitude of the current under large reverse bias is given by

$$I = I_S + I_o(1 - e^{V/\eta V_T})$$

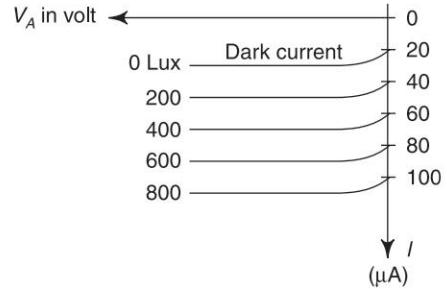
where  $I_o$  = reverse saturation current  
 $I_S$  = short-circuit current which is proportional to the light intensity  
 $V$  = voltage across the diode  
 $V_T$  = volt equivalent of temperature  
 $\eta$  = parameter, 1 for Ge and 2 for Si.

The characteristics of a photodiode are shown in Fig. 2.22. The reverse current increases in direct proportion to the level of illumination. Even when no light is applied, there is a minimum reverse leakage current called *dark current*, flowing through the device. Germanium has a higher dark current than silicon, but it also has a higher level of reverse current.

Photodiodes are used as light detectors, demodulators and encoders. They are also used in optical communication system, high-speed counting and switching circuits. Further, they are used in computer card punching and tapes, light operated switches, sound track films and electronic control circuits.



**Fig. 2.21** Photodiode (a) Construction, and (b) Symbol

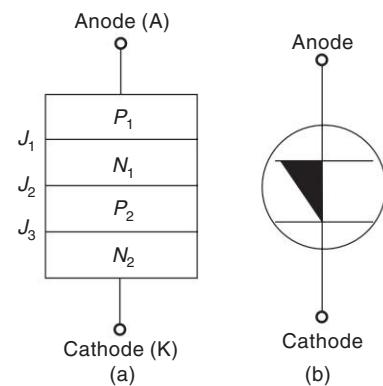


**Fig. 2.22** Classification of photodiode

## 2.15 PNPN DIODE (SHOCKLEY DIODE)

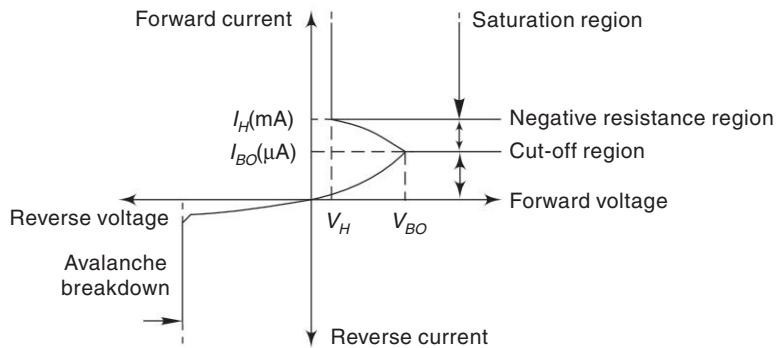
As shown in Fig. 2.23, it is a four-layer *PNPN* silicon device with two terminals. When an external voltage is applied to the device in such a way that anode is positive with respect to cathode, junctions  $J_1$  and  $J_3$  are forward biased and  $J_2$  is reverse biased. Then the applied voltage appears across the reverse biased junction  $J_2$ . Now, the current flowing through the device is only reverse saturation current.

However, as this applied voltage is increased, the current increases slowly until the so called firing or breakover voltage ( $V_{BO}$ ) is reached. Once firing takes place, the current increases abruptly and the voltage drop across the device decreases sharply. At this point, the diode switches over from 'OFF' to 'ON' state. Once the device is fired into conduction, a minimum amount of current known as *holding current*,  $I_H$ , is required to keep the device in the ON state. To turn the device OFF from ON state, the current has to be reduced below  $I_H$  by reducing the applied voltage close to



**Fig. 2.23** PNPN diode: (a) Basic structure and (b) Circuit symbol

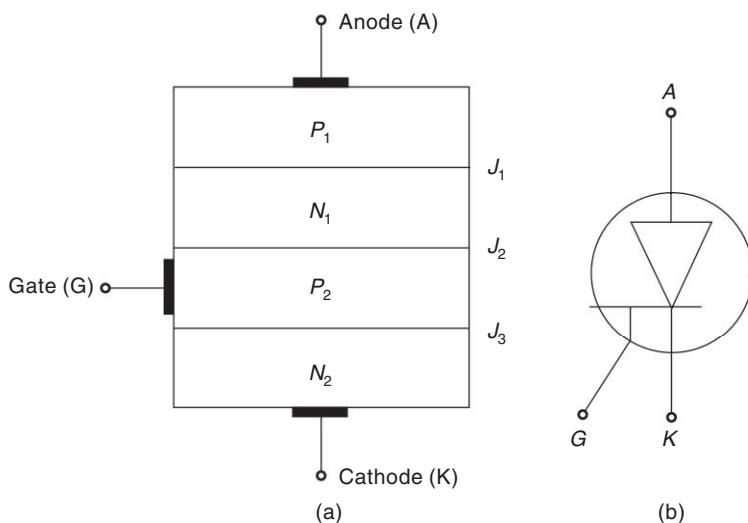
zero, i.e., below *holding voltage*,  $V_H$ . Thus, the diode acts as a switch during forward bias condition. The characteristic curve of a *PNPN* diode is shown in Fig. 2.24.



**Fig. 2.24** Characteristic curve of *PNPN* diode

## 2.16 SCR (SILICON-CONTROLLED RECTIFIER)

The basic structure and circuit symbol of an SCR is shown in Fig. 2.25. It is a four-layer three-terminal device in which the end *P*-layer acts as anode, the end *N*-layer acts as cathode, and the *P*-layer nearer to cathode acts as gate. As leakage current in silicon is very small compared to germanium, SCRs are made of silicon and not germanium.



**Fig. 2.25** SCR (a) Basic Structure and (b) Circuit symbol

**Characteristics of SCR** The characteristics of the SCR are shown in Fig. 2.26. SCR acts as a switch when it is forward biased. When the gate terminal is kept open, i.e., gate current  $I_G = 0$ , operation of SCR is similar to the *PNP* diode. When  $I_G < 0$ , the amount of reverse bias applied to  $J_2$  is increased. So the breakdown voltage  $V_{BO}$  is increased. When  $I_G > 0$ , the amount of reverse bias applied to  $J_2$  is decreased, thereby decreasing the breakdown voltage. With very large positive gate current, breakdown may occur at a very low voltage such that the characteristics of SCR is similar to that of the ordinary *PN* diode. As the voltage at which the SCR is switched 'ON' can be controlled by varying the gate current  $I_G$ , it is commonly called as controlled switch. Once the SCR is turned ON, the gate loses control, i.e., the gate cannot be used to switch the device OFF. One way to turn the device OFF is by lowering the anode current below the holding current  $I_H$  by reducing the supply voltage below the holding voltage  $V_H$ , keeping the gate open.

The SCR is used in relay control, motor control, phase control, heater control, battery chargers, inverters, regulated power supplies, and as static switches.

**Two-transistor Version of SCR** The operation of an SCR can be explained in a very simple way by considering it in terms of two transistors, called the two-transistor version of SCR. As shown in Fig. 2.27, an SCR can be split into two parts and displaced mechanically from one another but connected electrically. Thus, the device may be considered to be constituted by two transistors  $T_1$  (PNP) and  $T_2$  (NPN) connected back to back.

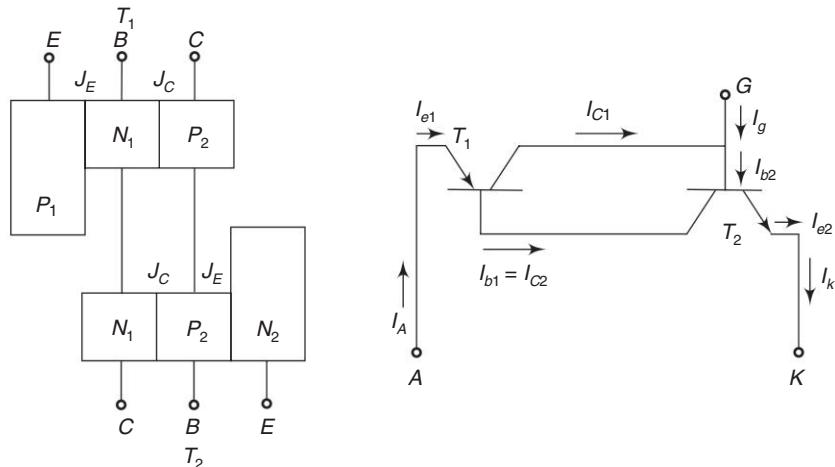


Fig. 2.27 Two-transistor version of SCR

Assuming the leakage current of  $T_1$  to be negligibly small, we obtain

$$I_{b1} = I_A - I_{c1} = I_A - \alpha_1 I_A = (1 - \alpha_1) I_A \quad (2.23)$$

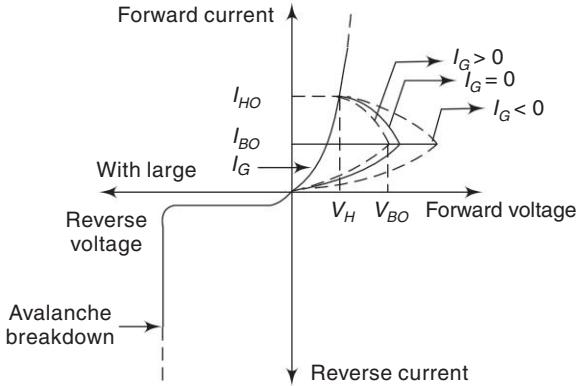


Fig. 2.26 Characteristics of SCR

Also, from Fig. 2.27, it is clear that

$$I_{b1} = I_{C2} \quad (2.24)$$

and

$$I_{C2} = \alpha_2 I_K \quad (2.25)$$

Substituting the values given in Eqs (2.24) and (2.25) in Eq. (2.23), we get

$$(1 - \alpha_1) I_A = \alpha_2 I_K \quad (2.26)$$

We know that

$$I_K = I_A + I_g \quad (2.27)$$

Substituting Eq. (2.27) in Eq. (2.26), we obtain

$$(1 - \alpha_1) I_A = \alpha_2 (I_A + I_g)$$

i.e.,

$$(1 - \alpha_1 - \alpha_2) I_A = \alpha_2 I_g$$

i.e.,

$$I_A = \left[ \frac{\alpha_2 I_g}{1 - (\alpha_1 + \alpha_2)} \right] \quad (2.28)$$

Equation (2.28) indicates that if  $(\alpha_1 + \alpha_2) = 1$ , then  $I_A = \infty$ , i.e., the anode current  $I_A$  suddenly reaches a very high value approaching infinity. Therefore, the device suddenly triggers into ON state from the original OFF state. This characteristic of the device is known as its *regenerative action*.

The value of  $(\alpha_1 + \alpha_2)$  can be made almost equal to unity by giving a proper value of positive current  $I_g$  for a short duration. This signal  $I_g$  applied at the gate which is the base of  $T_2$  will cause a flow of collector current  $I_{C2}$  by transferring  $T_2$  to its ON state. As  $I_{C2} = I_{b1}$ , the transistor  $T_1$  will also be switched ON. Now, the action is regenerative since each of the transistors would supply base current to the other. At this point even if the gate signal is removed, the device keeps on conducting, till the current level is maintained to a minimum value of holding current.

### 2.16.1 Thyristor Ratings

**Latching Current ( $I_L$ )** Latching current is the minimum current required to latch or trigger the device from its OFF-state to its ON-state.

**Holding Current ( $I_H$ )** Holding current is the minimum value of current to hold the device in the ON-state. For turning the device OFF, the anode current should be lowered below  $I_H$  by increasing the external circuit resistance.

**Gate Current ( $I_g$ )** Gate current is the current applied to the gate of the device for control purposes. The minimum gate current is the minimum value of current required at the gate for triggering the device. The maximum gate current is the maximum value of current applied to the device without damaging the gate. More the gate current, earlier is the triggering of the device and vice versa.

**Voltage Safety Factor ( $V_f$ )** Voltage safety factor  $V_f$  is a ratio which is related to the PIV, the RMS value of the normal operating voltage as,

$$V_f = \frac{\text{peak inverse voltage (PIV)}}{\sqrt{2} \times \text{rms value of the operating voltage}}$$

The value of  $V_f$  normally lies between 2 and 2.7. For a safe operation, the normal working voltage of the device is much below its PIV.

### 2.16.2 Rectifier Circuits using SCR

SCRs are much superior in performance than ordinary diode rectifiers. They find their main applications as rectifiers. Some of the rectifier circuits have been explained in the following sections.

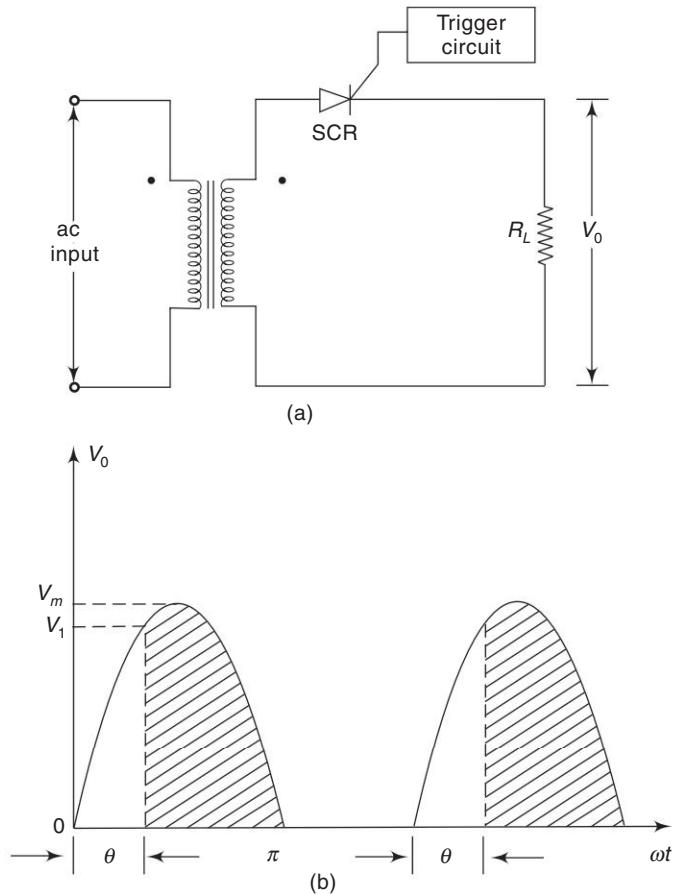
**SCR Half-Wave Rectifier** Though the SCR is basically a switch, it can be used in linear applications like rectification. Figure 2.28 shows the circuit of an SCR half-wave rectifier.

During the negative half-cycle, the SCR does not conduct irrespective of the gate current, as the anode is negative with respect to cathode and also PIV is less than the reverse breakdown voltage.

During the positive half-cycle of ac voltage appearing across secondary, the SCR will conduct provided proper gate current is made to flow. The greater the gate current, the lesser the supply voltage at which the SCR is triggered ON. Referring to Fig. 2.28(b), the gate current is adjusted to such a value that the SCR is turned ON at a positive voltage  $V_1$  of ac secondary voltage which is less than the peak voltage  $V_m$ . Beyond this, the SCR will be conducting till the applied voltage becomes zero. The angle at which the SCR starts conducting during the positive half-cycle is called firing angle  $\theta$ . Therefore, the conduction angle is  $(180^\circ - \theta)$ .

The SCR will block not only the negative part of the applied sinusoidal voltage, but also the part of the positive waveform up to a point SCR is triggered ON. If the angle  $\theta$  is zero, this will be an ordinary half-wave rectification. Therefore, by proper adjustment of gate current, the SCR can be made to conduct full or part of a positive half-cycle, thereby controlling the power fed to the load.

**Analysis** Let  $V = V_m \sin \omega t$  be alternating voltage that appears across the secondary of the transformer. In an SCR half-wave rectifier,  $\theta$  is the firing angle and the rectifier conducts from  $\theta$  to  $180^\circ$  ( $\pi$  radians) during the positive half-cycle.



**Fig. 2.28** SCR half-wave rectifier (a) Circuit diagram and (b) Conduction characteristics

$$\text{Therefore, average or dc output, } V_{av} = \frac{1}{2\pi} \int_{\theta}^{\pi} V_m \sin \omega t \, d\omega t \\ = \frac{1}{2\pi} [-V_m \cos \omega t]_{\theta}^{\pi} = \frac{V_m}{2\pi} (1 + \cos \theta)$$

For  $\theta = 0^\circ$ ,  $V_{av} = \frac{V_m}{\pi}$ . Here, the full positive half-cycle will appear across the load. This is the value of average voltage for ordinary half-wave rectifier.

When  $\theta = 90^\circ$ ,  $V_{av} = \frac{V_m}{2\pi}$ . This shows that greater the firing angle  $\theta$ , the smaller is the average voltage and vice versa.

$$\text{Similarly, } V_{rms} = \sqrt{\frac{1}{2\pi} \int_{\theta}^{\pi} (V_m \sin \omega t)^2 \, d\omega t} = \sqrt{\frac{V_m^2}{4\pi} \int_{\theta}^{\pi} (1 - \cos 2\omega t) \, d\omega t} \\ = \sqrt{\frac{V_m^2}{4\pi} \left[ \omega t - \frac{\sin 2\omega t}{2} \right]_{\theta}^{\pi}} = \frac{V_m}{2} \left[ \frac{1}{\pi} (\pi - \theta + \frac{\sin 2\theta}{2}) \right]^{\frac{1}{2}}$$

$$\text{If } \theta = 0, \text{ then } V_{rms} = \frac{V_m}{2}$$

### EXAMPLE 2.15

In an SCR half-wave rectifier, the forward breakdown voltage of SCR is 110 V for a gate current of 1 mA. If a 50 Hz sinusoidal voltage of 220 V peak is applied, find firing angle, conduction angle, average voltage, average current, power output, and the time during which the SCR remains OFF. Assume load resistance is  $100 \Omega$  and the holding current to be zero.

**Solution** We know that,  $V_1 = V_m \sin \theta$

$$110 = 220 \sin \theta, \text{ i.e., } \sin \theta = 0.5$$

$$\text{Therefore, firing angle, } \theta = \sin^{-1}(0.5) = 30^\circ$$

$$\text{Conduction angle} = 180^\circ - \theta = 180^\circ - 30^\circ = 150^\circ$$

$$\text{Average voltage, } V_{av} = \frac{V_m}{2\pi} (1 + \cos \theta) \\ = \frac{220}{2\pi} (1 + \cos 30^\circ) = 65.37 \text{ V}$$

$$\text{Average current, } I_{av} = V_{av}/R_L = 65.37/100 = 0.6537 \text{ A}$$

$$\text{Power output, } = V_{av} I_{av} = (65.37) (0.6537) = 42.7326 \text{ W}$$

$$\text{As } V_1 = V_m \sin \theta = V_m \sin \omega t$$

$$\omega t = \theta = 30^\circ = \frac{\pi}{6}$$

$$2\pi \times 50t = \frac{\pi}{6}$$

Therefore, the time during which the SCR remains OFF is

$$t = 1/(2 \times 6 \times 50) = 1/600 = 1.667 \text{ ms}$$

**SCR Full-Wave Rectifier** The SCR full-wave rectifier is shown in Fig. 2.29. It is exactly similar to an ordinary full wave rectifier except that the two diodes have been replaced by two SCRs. The angle of conduction can be changed by adjusting the gate currents.

During the positive half-cycle of the input signal, anode of SCR1 becomes positive and at the same time, the anode of SCR2 becomes negative. When the input voltage reaches  $V_1$  as shown in Fig. 2.29(b), SCR1 starts conducting and therefore only the shaded portion of positive half-cycle will pass through the load.

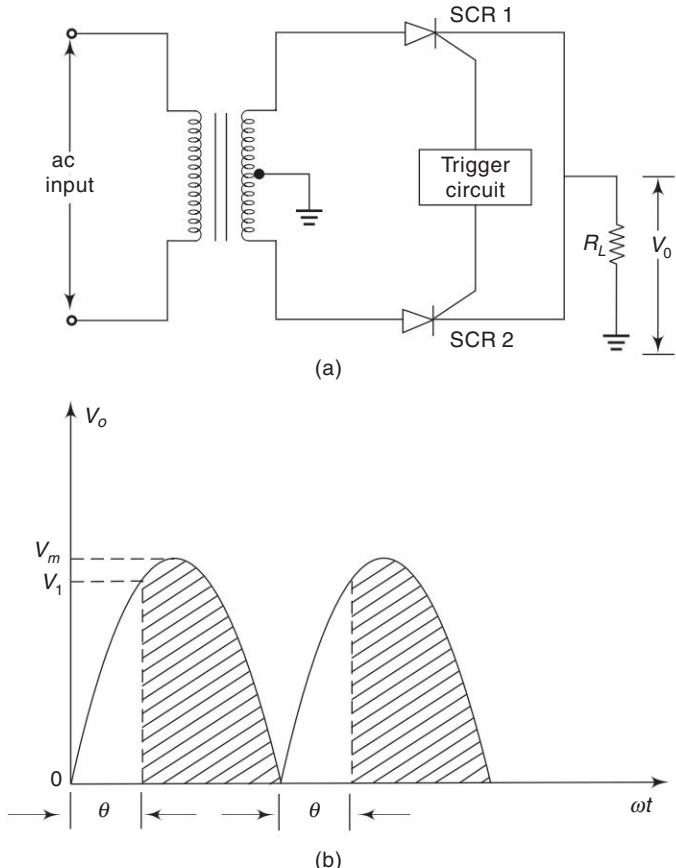
During the negative half-cycle of the input, the anode of SCR1 becomes negative and the anode of SCR2 becomes positive. Hence, SCR1 does not conduct and SCR2 conducts when the input voltage becomes  $V_1$ .

The main advantage of this circuit over an ordinary full-wave rectifier circuit is that any voltage can be made available at the output by simply changing the firing angle of the SCRs.

**Analysis** Referring to Fig. 2.29, let  $V = V_m \sin \omega t$  be the alternating voltage that appears between center tap and either end of secondary and  $\theta$  be the firing angle.

$$V_{av} = \frac{1}{\pi} \int_{\theta}^{\pi} V_m \sin \omega t d\omega t = \frac{V_m}{\pi} [-\cos \omega t]_{\theta}^{\pi} = \frac{V_m}{\pi} [1 + \cos \theta]$$

This is double that of a half-wave rectifier, as negative half-cycle is also rectified.



**Fig. 2.29** SCR full-wave rectifier (a) Circuit diagram and (b) Conduction characteristics

**EXAMPLE 2.16**

A full wave controlled rectifier employs 2 SCRs and 2 diodes in bridge configuration to rectify 230 V, 50 Hz ac mains and give an output of 150 V to a resistive load of  $10\ \Omega$ . Find the firing angle, the time during which the SCR remains OFF, and the load current.

**Solution** For an SCR full-wave rectifier,

$$V_{dc} = \frac{V_m}{\pi} (1 + \cos \theta)$$

$$150 = \frac{230 \times \sqrt{2}}{\pi} (1 + \cos \theta)$$

Therefore,  $\theta = 63.33^\circ$

For 50 Hz,  $T = 20$  ms for  $360^\circ$

$$\text{Therefore, } t = \frac{20}{360^\circ} \times 63.33^\circ = 3.52 \text{ ms}$$

$$\text{Load current, } I_{av} = \frac{V_{av}}{R_L} = \frac{150}{10} = 15 \text{ A}$$

**EXAMPLE 2.17**

When an SCR full-wave rectifier is connected across a sinusoidal voltage of  $400 \sin 314t$ , the rms value of the current flowing through the device is 20 A. Find the power rating of the SCR.

**Solution** As the supply voltage is  $400 \sin 314t$ ,  $V_m = 400$  V

$$\text{Peak inverse voltage (PIV)} = \sqrt{3} V_m = \sqrt{3} \times 400 = 692.8 \text{ V}$$

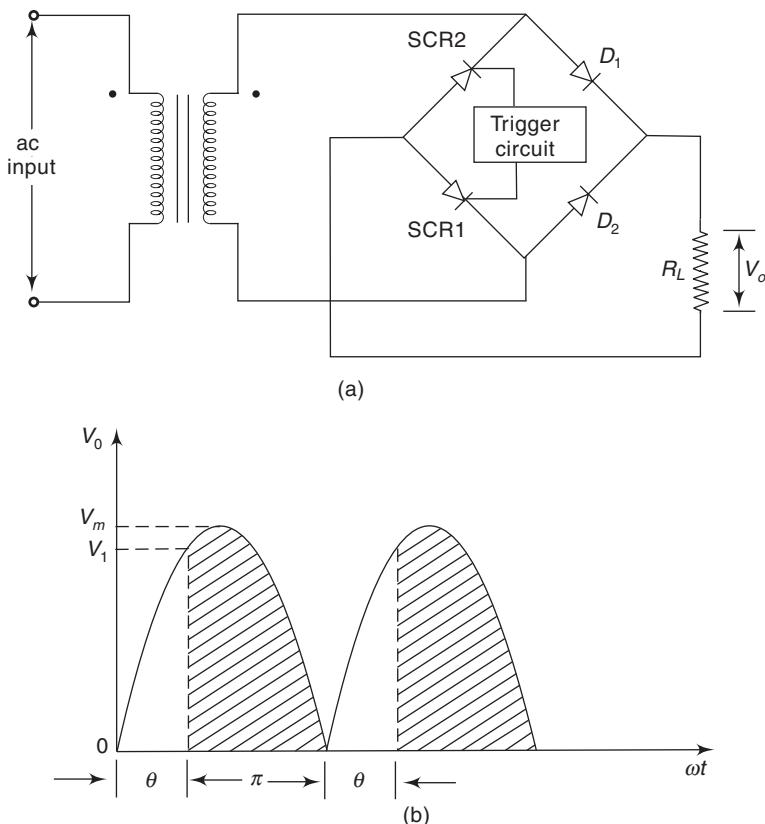
$$\text{rms value of current} = 20 \text{ A}$$

$$\text{Average value of current, } I_{av} = \text{rms value/form factor} = 20/1.11 = 18 \text{ A}$$

$$\text{Power rating of the SCR} = \text{PIV} \times I_{av} = 692.8 \times 18 = 12.47 \text{ kW}$$

**SCR Bridge Rectifier** The SCR bridge rectifier is shown in Fig. 2.30(a). During the positive half-cycle of the input ac voltage, SCR1 and diode  $D_1$  conduct whereas SCR2 and diode  $D_2$  do not conduct. During the negative half-cycle, SCR2 and diode  $D_2$  conduct. As shown in Fig. 2.30(b), the conduction angle and hence, the output voltage can be changed by adjusting the gate currents of SCR1 and SCR2. Here, the dc output

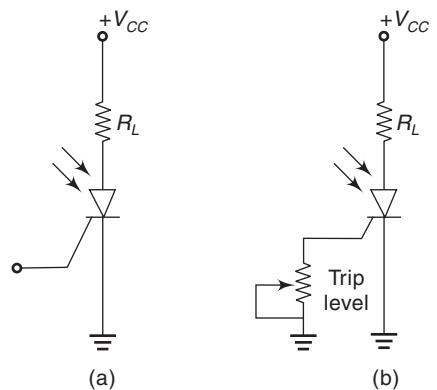
voltage,  $V_{av} = \frac{V_m}{\pi} [1 + \cos \theta]$ , which is equal to that of the SCR full-wave rectifier. If the current is lowered below  $I_H$  by increasing the external circuit resistance, the SCR will switch OFF.



**Fig. 2.30** SCR bridge rectifier (a) Circuit diagram and (b) Conduction characteristics

### 2.16.3 LASCR (Light-Activated SCR)

The LASCR shown in Fig. 2.31 is triggered by irradiating it with light. The arrows represent incoming light that passes through a window and falls on the depletion layer closer to the middle junction  $J_2$  of SCR. The incident light generates electron-hole pairs in the device thus increasing the number of charge carriers. This leads to the instantaneous flow of current within the device and the device turns ON. For light triggering to occur, the device must have high value of rate of change of voltage with time,  $dV/dt$ .

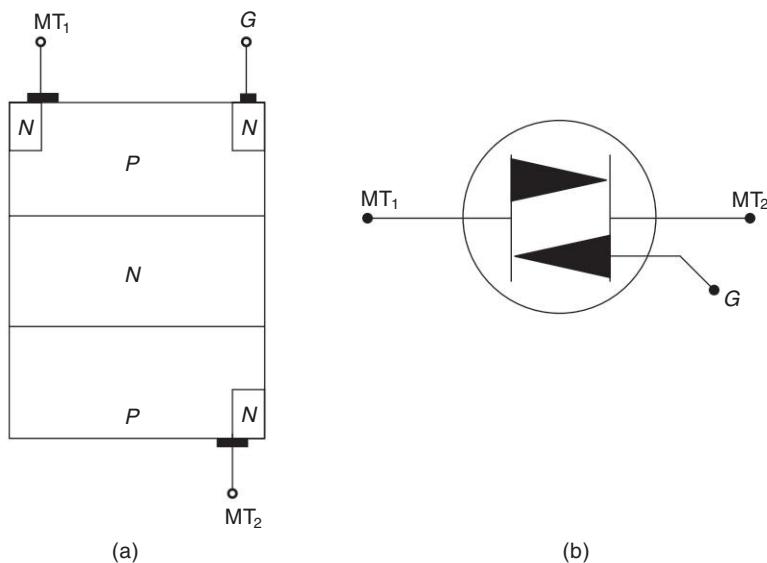


**Fig. 2.31** Light-activated SCR

## 2.17 TRIAC (TRIODE AC SWITCH)

The TRIAC is a three-terminal semiconductor switching device which can control alternating current in a load. Its three terminals are MT<sub>1</sub>, MT<sub>2</sub>, and the gate (G). The basic structure and circuit symbol of a TRIAC are shown in Fig. 2.32. The TRIAC is equivalent to two SCRs connected in parallel but in the reverse direction as shown in Fig. 2.33. So, a TRIAC will act as a switch for both directions. The characteristics of a TRIAC are shown in Fig. 2.34.

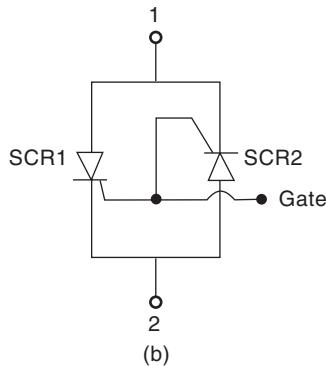
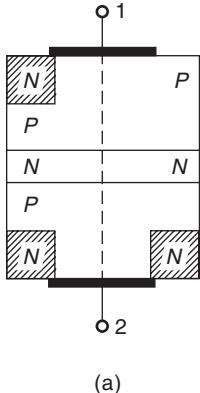
Like an SCR, a TRIAC also starts conducting only when the breakdown voltage is reached. Earlier to that, the leakage current which is very small in magnitude flows through the device and therefore remains in the OFF state. The device, when starts conducting, allows very heavy amount of current to flow through it. The high inrush of current must be limited using external resistance, or it may otherwise damage the device.



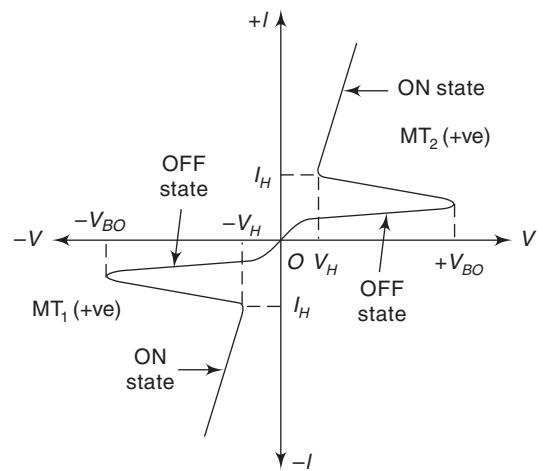
**Fig. 2.32** TRIAC: (a) Basic structure and (b) Circuit symbol

During the positive half-cycle, MT<sub>1</sub> is positive with respect to MT<sub>2</sub>, whereas MT<sub>2</sub> is positive with respect to MT<sub>1</sub> during the negative half-cycle. A TRIAC is a bidirectional device and can be triggered either by a positive or by a negative gate signal. By applying proper signal at the gate, the breakdown voltage, i.e., firing angle of the device can be changed; thus phase control process can be achieved.

A TRIAC is used for illumination control, temperature control, liquid-level control, motor-speed control, and as static switch to turn ac power ON and OFF. Nowadays, the DIAC-TRIAC pairs are increasingly being replaced by a single component unit known as QUADRAC. Its main limitation in comparison to SCR is its low power-handling capacity.



**Fig. 2.33** Two SCR version of TRIAC: (a) Basic structure and (b) Equivalent circuit

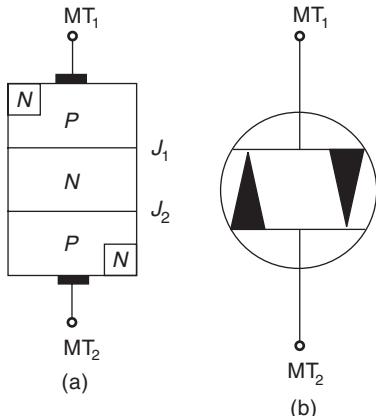


**Fig. 2.34** Characteristics of TRIAC

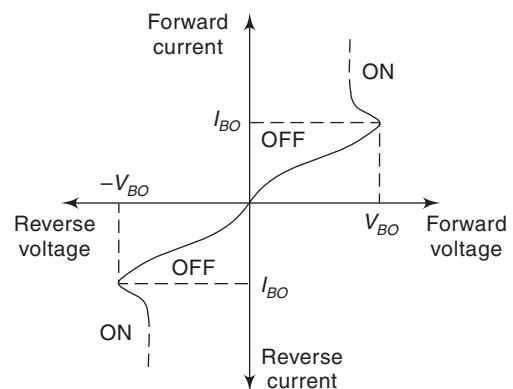
## 2.18 DIAC (DIODE AC SWITCH)

The construction and symbol of DIAC are shown in Fig. 2.35. DIAC is a three-layer, two-terminal semiconductor device. MT<sub>1</sub> and MT<sub>2</sub> are the two main terminals which are interchangeable. It acts as a bidirectional avalanche diode. It does not have any control terminal. It has two junctions J<sub>1</sub> and J<sub>2</sub>. Though the DIAC resembles a bipolar transistor, the central layer is free from any connection with the terminals.

From the characteristic of a DIAC shown in Fig. 2.36, it acts as a switch in both directions. As the doping level at the two ends of the device is the same, the DIAC has identical characteristics for both positive and negative half of an ac cycle. During the positive half-cycle, MT<sub>1</sub> is positive with respect to MT<sub>2</sub> whereas



**Fig. 2.35** DIAC: (a) Basic structure and (b) Circuit symbol



**Fig. 2.36** Characteristic of DIAC

$MT_2$  is positive with respect to  $MT_1$  in the negative half-cycle. At voltage less than the breakdown voltage, a very small amount of current, called the *leakage current*, flows through the device and the device remains in OFF state. When the voltage level reaches the breakdown voltage, the device starts conducting and it exhibits negative resistance characteristics, i.e., the current flowing in the device starts increasing and the voltage across it starts decreasing.

The DIAC is not a control device. It is used as triggering device in TRIAC phase-control circuits used for light dimming, motor speed control, and heater control.

## 2.19 UJT (UNIJUNCTION TRANSISTOR) RELAXATION OSCILLATOR

UJT is a three-terminal semiconductor switching device. As it has only one *PN* junction and three leads, it is commonly called unijunction transistor.

The basic structure of a UJT is shown in Fig. 2.37(a). It consists of a lightly doped *N*-type silicon bar with a heavily doped *P*-type material alloyed to its one side closer to  $B_2$  for producing a single *PN* junction. The circuit symbol of UJT is shown in Fig. 2.37(b). Here, the emitter leg is drawn at an angle to the vertical and the arrow indicates the direction of the conventional current.

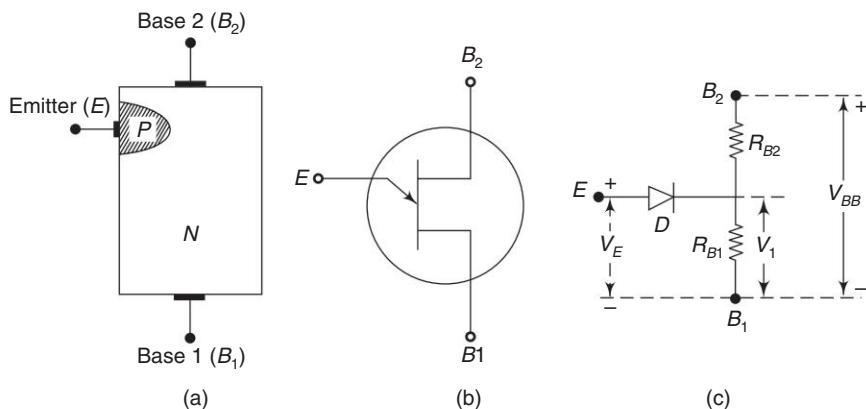


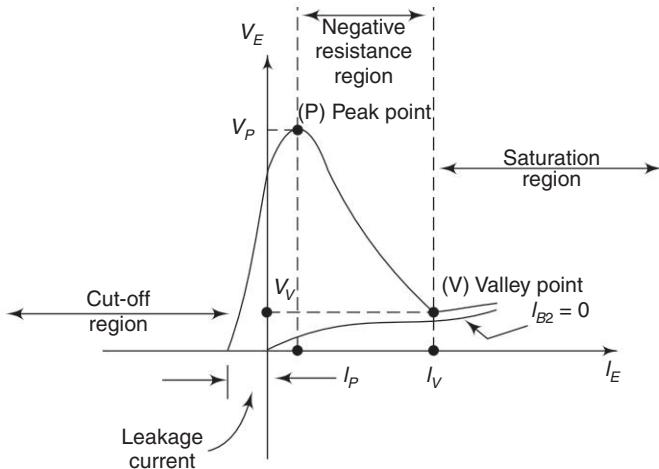
Fig. 2.37 UJT: (a) Basic structure (b) Circuit symbol and (c) Equivalent circuit

**Characteristics of UJT** Referring to Fig. 2.37(c), the interbase resistance between  $B_2$  and  $B_1$  of the silicon bar is  $R_{BB} = R_{B1} + R_{B2}$ . With the emitter terminal open, if voltage  $V_{BB}$  is applied between the two bases, a voltage gradient is established along the *N*-type bar. The voltage drop across  $R_{B1}$  is given by  $V_1 = \eta V_{BB}$ , where the *intrinsic stand-off ratio*  $\eta = R_{B1}/(R_{B1} + R_{B2})$ . The typical value of  $\eta$  ranges from 0.56 to 0.75. This voltage  $V_1$  reverse biases the *PN* junction and emitter current is cut-off. But a small leakage current flows from  $B_2$  to emitter due to minority carriers. If a positive voltage  $V_E$  is applied to the emitter, the *PN* junction will remain reverse biased so long as  $V_E$  is less than  $V_1$ . If  $V_E$  exceeds  $V_1$  by the cut-in voltage  $V_\gamma$ , the diode becomes forward biased. Under this condition, holes are injected into *N*-type bar. These holes are repelled by the terminal  $B_2$  and are attracted by the terminal  $B_1$ . Accumulation of holes in  $E$  to  $B_1$  region reduces the resistance in this section and hence, emitter current  $I_E$  is increased and is limited by  $V_E$ . The device is now in the 'ON' state.

If a negative voltage is applied to the emitter,  $PN$  junction remains reverse biased and the emitter current is cut-off. The device is now in the 'OFF' state.

Figure 2.38 shows a family of input characteristics of UJT. Here, up to the peak point  $P$ , the diode is reverse biased and hence, the region to the left of the peak point is called *cut-off region*. The UJT has a stable firing voltage  $V_P$  which depends linearly on  $V_{BB}$  and a small firing current  $I_P$  ( $\approx 25 \mu\text{A}$ ). At  $P$ , the peak voltage  $V_P = \eta V_{BB} + V_r$ , the diode starts conducting and holes are injected into  $N$ -layer. Hence, resistance decreases thereby decreasing  $V_E$  for the increase in  $I_E$ . So, there is a *negative resistance region* from the peak point  $P$  to the valley point  $V$ . After the valley point, the device is driven into saturation and behaves like a conventional forward biased  $PN$  junction diode. The region to the right of the valley point is called *saturation region*. In the valley point, the resistance changes from negative to positive. The resistance remains positive in the saturation region. For very large  $I_E$ , the characteristic asymptotically approaches the curve for  $I_{B2} = 0$ .

A unique characteristic of UJT is, when it is triggered, the emitter current increases regeneratively until it is limited by emitter power supply. Due to this negative resistance property, a UJT can be employed in a variety of applications, viz., sawtooth wave generator, pulse generator, switching, timing and phase control circuits.



**Fig. 2.38** Input characteristics of UJT

**UJT Relaxation Oscillator** The relaxation oscillator using UJT which is meant for generating sawtooth waveform is shown in Fig. 2.39. It consists of a UJT and a capacitor  $C_E$  which is charged through  $R_E$  as the supply voltage  $V_{BB}$  is switched ON.

The voltage across the capacitor increases exponentially and when the capacitor voltage reaches the peak point voltage  $V_P$ , the UJT starts conducting and the capacitor voltage is discharged rapidly through  $EB_1$  and  $R_1$ . After the peak point voltage of UJT is reached, it provides negative resistance to the discharge path which is useful in the working of the relaxation oscillator. As the capacitor voltage reaches zero, the device then cuts off and capacitor  $C_E$  starts to charge again. This cycle is repeated continuously generating a *sawtooth waveform* across  $C_E$ .

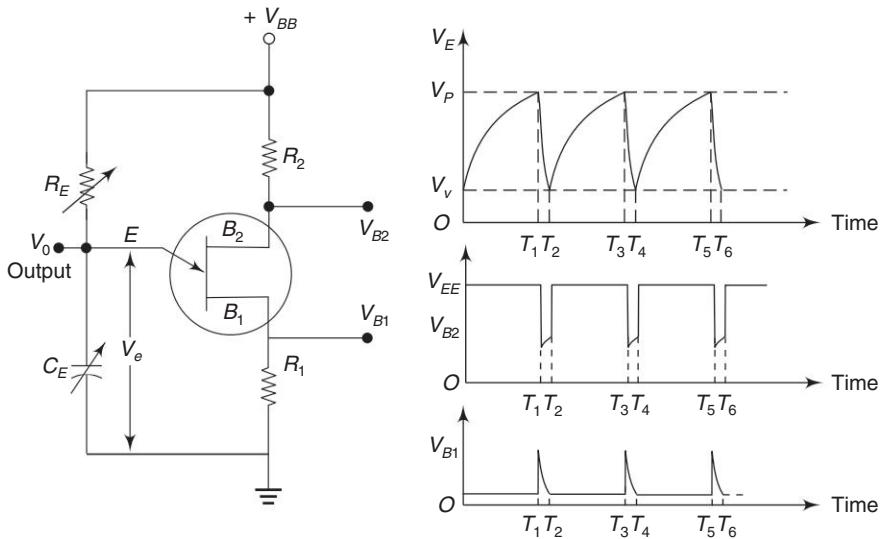


Fig. 2.39 UJT relaxation oscillator

The inclusion of external resistors  $R_2$  and  $R_1$  in series with  $B_2$  and  $B_1$  provides spike waveforms. When the UJT fires, the sudden surge of current through  $B_1$  causes drop across  $R_1$ , which provides positive going spikes. Also, at the time of firing, fall of  $V_{EBI}$  causes  $I_2$  to increase rapidly which generates negative going spikes across  $R_2$ .

By changing the values of capacitance  $C_E$  or resistance  $R_E$ , frequency of the output waveform can be changed as desired, since these values control the time constant  $R_E C_E$  of the capacitor charging circuit.

**Frequency of Oscillation** The time period and hence, the frequency of the sawtooth wave can be calculated as follows. Assuming that the capacitor is initially uncharged, the voltage  $V_C$  across the capacitor prior to breakdown is given by

$$V_C = V_{BB} (1 - e^{-t/R_E C_E})$$

where  $R_E C_E$  = charging time constant of resistor-capacitor circuit, and  $t$  = time from the commencement of the waveform.

The discharge of the capacitor occurs when  $V_C$  is equal to the peak-point voltage  $V_P$ , i.e.,

$$V_P = \eta V_{BB} = V_{BB} (1 - e^{-t/R_E C_E})$$

$$\eta = 1 - e^{-t/R_E C_E}$$

$$e^{-t/R_E C_E} = (1 - \eta)$$

Therefore,

$$t = R_E C_E \log_e \frac{1}{(1 - \eta)}$$

$$= 2.303 R_E C_E \log_{10} \frac{1}{(1 - \eta)}$$

If the discharge time of the capacitor is neglected, then  $t = T$  is the period of the wave.

Therefore, frequency of oscillation of sawtooth wave,

$$f_o = \frac{1}{T} = \frac{1}{2.303 R_E C_E \log_{10} \frac{1}{(1-\eta)}}$$

### EXAMPLE 2.18

Design a UJT relaxation oscillator to generate a sawtooth waveform at a frequency of 500 Hz. Assume the supply voltage  $V_{BB} = 20$  V,  $V_P = 2.9$  V,  $V_V = 1.118$  V,  $I_P = 1.6$  mA and  $I_V = 3.5$  mA.

#### Solution

We know that

$$f_o = \frac{1}{2.303 R_E C_E \log_{10} \frac{1}{(1-\eta)}}$$

We know that  $\eta_{\min} = 0.56$

For determining  $R_E$ , we have

$$R_E < \frac{V_{BB} - V_P}{I_P}, \text{ i.e., } R_E < \frac{20 - 2.9}{1.6 \times 10^{-3}} = 10.7 \text{ k}\Omega$$

$$R_E > \frac{V_{BB} - V_V}{I_V}, \text{ i.e., } R_E > \frac{20 - 1.118}{3.5 \times 10^{-3}} = 5.36 \text{ k}\Omega$$

Therefore,  $R_E$  is selected as 10 k $\Omega$ .

$$\frac{1}{500} = 2.303 \times 10 \times 10^3 C_E \log_{10} \left( \frac{1}{1 - 0.56} \right)$$

$$\text{Therefore, } C_E = \frac{1}{500 \times 2.303 \times 10^4 \times 0.36} = 0.24 \mu\text{F}$$

So,  $C_E$  is selected as 0.22  $\mu\text{F}$ .

Let the required pulse voltage at  $B_1 = 5$  V

Let the peak pulse current,  $I_E = 250$  mA.

$$\text{Therefore, } R_1 = \frac{V_{R1}}{I_E} = \frac{5}{250 \times 10^{-3}} = 20 \Omega$$

So,  $R_1$  is selected to be 22  $\Omega$ .

We select the voltage characteristics for  $V_{B1B2} = 4$  V.

Therefore,  $V_{R2} = 20 - (4 + 5) = 11$  V

$$R_2 = \frac{11}{250} \times 10^3 = 44 \Omega$$

So,  $R_2$  is selected as 100  $\Omega$ .

**EXAMPLE 2.19**

A UJT has a firing potential of 20 V. It is connected across the capacitor of a series  $RC$  circuit with  $R = 100 \text{ k}\Omega$  and  $C = 1000 \text{ pF}$  supplied by a source of 40 V dc. Calculate the time period of the sawtooth waveform generated.

**Solution** Given  $R_E = 100 \text{ k}\Omega$  and  $C_E = 1000 \text{ pF}$

$$V_{BB} = 40 \text{ V}, V_P = 20 \text{ V}$$

$$V_P = V_{BB} \left( 1 - e^{\frac{-t}{R_E C_E}} \right)$$

$$20 = 40 \left( 1 - e^{\frac{-t}{R_E C_E}} \right)$$

$$e^{-t/R_E C_E} = \frac{1}{2}$$

$$\frac{-t}{R_E C_E} = \ln \frac{1}{2}$$

$$\frac{t}{R_E C_E} = \ln 2$$

$$t = \ln 2 \times R_E C_E$$

Therefore,  $t = 0.693 \times 100 \times 10^3 \times 1000 \times 10^{-12} = 0.693 \times 10^{-4} = 69.3 \mu\text{s}$

**REVIEW QUESTIONS**

- What is a  $PN$  junction? How is it formed?
- Explain the formation of depletion region in a  $PN$  junction.
- Draw the energy-band diagram of a  $PN$  junction and explain the working of a diode.
- Sketch the conduction and valence bands before and after diffusion of carriers in a  $PN$  junction.
- Explain how a barrier potential is developed at the  $PN$  junction.
- Describe the action of  $PN$  junction diode under forward bias and reverse bias.
- Show that the  $PN$  diode works as a rectifier.
- Explain how unidirectional current flow is possible through a  $PN$  junction diode.
- Explain  $V-I$  characteristics of a  $PN$  junction diode.
- Indicate the differences between the characteristics of silicon and germanium diodes and state approximately their cut-in voltages.
- Explain the following terms in a  $PN$  junction diode:
  - Maximum forward current
  - Peak inverse voltage
  - Maximum power rating
- Explain the terms (i) static resistance, (ii) dynamic resistance, (iii) junction resistance, and (iv) reverse resistance of a diode.
- Write the volt–ampere equation for a  $PN$  diode. Give the meaning of each symbol.
- What are the factors governing the reverse saturation current in a  $PN$  junction diode?

15. Determine the forward-bias voltage applied to a silicon diode to cause a forward current of 10 mA and reverse saturation current,  $I_o = 25 \times 10^{-7}$  A at room temperature. [Ans.: 0.4 V]
16. The reverse saturation current  $I_o$  in a germanium diode is 6  $\mu$ A. Calculate the current flowing through the diode when the applied forward bias voltages are 0.2, 0.3 and 0.4 V at room temperature. [Ans.: 13.15 mA, 21.5 mA, 28.8 mA]
17. Define the term *transition capacitance*  $C_T$  of a *PN* diode.
18. Explain the term *diffusion capacitance*  $C_D$  of a forward biased diode.
19. Explain the effect of temperature of a diode.
20. Distinguish between avalanche and Zener mechanisms.
21. Can an ordinary rectifier diode be used as a Zener diode? Explain.
22. Mention the applications of *PN* junction diodes.
23. Explain avalanche breakdown and Zener breakdown.
24. Draw the  $V-I$  characteristic of Zener diode and explain its operation.
25. Show that the Zener diode can be used as a voltage regulator.
26. What is tunnelling?
27. From the energy-band diagram, explain the  $V-I$  characteristic of a tunnel diode.
28. Draw the equivalent circuit of a tunnel diode and explain it.
29. List the applications of tunnel diode and mention its advantages and disadvantages.
30. Explain the principle and working of photodiode.
31. Write the equation for the volt-ampere characteristics of a photodiode. Define each term in the equation.
32. Explain the volt-ampere characteristics of a semiconductor photodiode.
33. List the applications of a photodiode.
34. Describe with the help of a relevant diagram, the construction of an LED and explain its working.
35. List the applications of an LED.
36. Compare the working principle of LED with solar cell.
37. In what respect is an LED different from an ordinary *PN* junction diode?
38. What is a thyristor? Mention some of them.
39. Describe the operation of a Shockley diode.
40. Describe the working principle of an SCR with  $V-I$  characteristics
41. Draw the two-transistor model of an SCR and explain its breakdown operation.
42. Explain why an SCR is operated only in the forward-biased condition.
43. Explain how triggering of an SCR can be controlled by the gate signal supplied.
44. Explain the terms (i) firing angle, and (ii) conduction angle of an SCR.
45. Once the SCR is triggered, the gate loses its control. Explain.
46. Explain the two transistor analogy of an SCR.
47. A half wave rectifier circuit employing an SCR is adjusted to have a gate current of 1 mA and its forward breakdown voltage is 150 V. If a sinusoidal voltage of 400 V peak is applied, determine (i) firing angle, (ii) average output voltage, (iii) average current for a load resistance of  $200\ \Omega$ , and (iv) power output. [Ans: (i)  $22^\circ$  (ii) 122.6 V (iii) 0.613 A (iv) 75.15 W]
48. A sinusoidal voltage  $V_1 = 200 \sin 314t$  is applied to an SCR whose forward breakdown voltage is 150 V. Determine the time during which SCR remains OFF. [Ans. 2.7 ms]
49. An SCR full-wave rectifier is connected to 230 V, 50 Hz mains to supply ac voltage to a resistive load of  $10\ \Omega$  for firing angle of  $90^\circ$ . Find the dc output voltage and load current. [Ans. 103.53 V, 10.353 A]
50. The brightness of a 100 W, 110 V lamp is to be varied by controlling firing angle of SCR full-wave circuit. The RMS value of ac voltage appearing across each SCR is 110 V. Find the rms voltage and current in the lamp and firing angle of  $60^\circ$ . [Ans. 98.9 V, 0.82 A]
51. What is a TRIAC? Sketch its characteristics and describe its operation.

52. DIAC is a bidirectional device. Explain.
53. Draw the  $V-I$  characteristics of a DIAC and explain its working principle.
54. What is the advantage of TRIAC over SCR?
55. Draw the equivalent circuit of UJT and explain its operation with the help of emitter characteristics.
56. Explain the  $V-I$  characteristics of a UJT.
57. Define intrinsic stand-off ratio of a UJT.
58. Explain the terms (a) peak point voltage  $V_p$ , and (b) valley point voltage  $V_v$  of a UJT.
59. Mention some of the applications of UJT.
60. Explain the difference between UJT and a conventional bipolar transistor.
61. Explain with the help of a circuit diagram the working of a UJT relaxation oscillator.
62. A silicon UJT has an interbase resistance  $R_{BB} = 10 \text{ k}\Omega$  and  $R_{B1} = 6 \text{ k}\Omega$  with  $I_E = 0$ . If  $V_{BB} = 20 \text{ V}$  and  $V_E < V_p$ , find UJT current,  $\eta$  and  $V_p$ . [Ans. 2 mA, 0.6, 12.7 V]
63. A UJT has  $R_{BB} = 10 \Omega$  and  $R_{B2} = 3.5 \text{ k}\Omega$ . Find its intrinsic stand-off ratio. [Ans. 0.65]
64. Design a UJT relaxation oscillator to generate a sawtooth waveform at a frequency of 600 Hz. Assume the supply voltage  $V_{BB} = 18 \text{ V}$ ;  $V_p = 2.9 \text{ V}$ ,  $V_v = 1.118 \text{ V}$ .
65. The base one of a UJT has resistance of  $4.7 \text{ k}\Omega$  and the value of intrinsic stand-off ratio of the device is 0.58. If an inter-base voltage of 10 V is applied across the two bases, calculate the value of  $I_B$ . [Ans. 1.23 mA]

### OBJECTIVE-TYPE QUESTIONS

- In a  $PN$  junction, the barrier potential offers opposition to only
  - holes in  $P$ -region
  - free electrons in  $N$ -region
  - majority carriers in both regions
  - minority carriers in both regions
- In a forward-biased  $PN$  junction diode, the sequence of events that best describes the mechanism of current flow is
  - injection and subsequent diffusion and recombination of minority carriers
  - injection and subsequent drift and generation of minority carriers.
  - extraction and subsequent diffusion and generation of minority carriers.
  - extraction and subsequent drift and recombination of minority carriers
- Which of the following is not associated with a  $PN$  junction?
  - Junction capacitance
  - Charge storage capacitance.
  - Depletion
  - Channel-length modulation
- The diffusion capacitance of a  $PN$  junction
  - decreases with increasing current and increasing temperature
  - decreases with decreasing current and increasing temperature
  - increases with increasing current and increasing temperature
  - does not depend on current and temperature
- In an abrupt  $PN$  junction, the doping concentrations on the  $P$ -side and  $N$ -side are  $N_A = 9 \times 10^{16} / \text{cm}^3$  and  $N_D = 1 \times 10^{16} / \text{cm}^3$  respectively. The  $PN$  junction is reverse biased and the total depletion width is  $3 \mu\text{m}$ . The depletion width on the  $P$ -side is
  - $2.7 \mu\text{m}$
  - $0.3 \mu\text{m}$
  - $2.25 \mu\text{m}$
  - $0.75 \mu\text{m}$
- A  $PN$  junction has a built-in potential of 0.8 V. The depletion layer width at a reverse bias of 1.2 V is  $2 \mu\text{m}$ . For a reverse bias of 7.2 V, the depletion layer width will be
  - $4 \mu\text{m}$
  - $4.9 \mu\text{m}$
  - $8 \mu\text{m}$
  - $12 \mu\text{m}$
- A tunnel diode is
  - a high resistivity  $PN$  junction diode
  - a slow switching device
  - an amplifying device
  - a very heavily doped  $PN$  junction diode

8. Consider a Ge diode operation at 27°C and just beyond the threshold voltage of Ge. What is the value of  $dv/dt$ ?  
 (a) -1.9 mV/°C      (b) -2.0 mV/°C      (c) -2.1 mV/°C      (d) -2.3 mV/°C
9. For a *PN* junction, match the type of breakdown with phenomenon  
 1. Avalanche breakdown  
 2. Zener breakdown  
 3. Collision of carriers with crystal ions  
 A. Collision of carriers with crystal ions  
 B. Early effect  
 C. Rupture of covalent bond due to strong electric field  
 (a) 1-B, 2-A, 3-C      (b) 1-c, 2-A, 3-B      (c) 1-A, 2-B, 3-C      (d) 1-A, 2-C, 3-B
10. Avalanche breakdown is observed in Zener diodes having  $V_z$  more than  
 (a) 5 V      (b) 8 V      (c) 50 V      (d) 100 V
11. For a Zener diode having maximum Zener current of 50 mA and  $V_z = 10$  V, the maximum power dissipation is  
 (a) 1 W      (b) 5 mW      (c) 50 mW      (d) 0.5 W
12. Zener breakdown occurs  
 (a) due to normally generated minority carriers      (b) in lightly doped junctions  
 (c) due to rupture of covalent bonds      (d) mostly in germanium junctions
13. Zener diode is usually operated  
 (a) in forward-bias mode      (b) in reverse-bias mode  
 (c) near cut-in voltage      (d) in forward linear region
14. For highly doped diode,  
 (a) Zener breakdown is likely to take place      (b) avalanche breakdown is likely to take place  
 (c) either (a) or (b) will take place      (d) neither (a) or (b) will take place
15. In avalanche multiplication, pick up the correct answer:  
 (a) Disruption of covalent bond occur by collision  
 (b) Direct rupture  
 (c) Both (a) and (b)  
 (d) None of the above
16. A Zener diode works on the principle of  
 (a) tunnelling of charge carriers across the junction  
 (b) thermionic emission  
 (c) diffusion of charge carriers across the junction  
 (d) doping of charge carriers across the junction
17. Zener diodes have breakdown voltage which  
 (a) has positive temperature coefficient      (b) has negative temperature coefficient  
 (c) is independent of temperature      (d) none of these
18. In a tunnel diode, impurity concentration is of the order of  
 (a)  $1 \text{ in } 10^3$       (b)  $1 \text{ in } 10^5$       (c)  $1 \text{ in } 10^7$       (d)  $1 \text{ in } 10^9$
19. In a Zener diode,  
 (a) only the *P*-region is heavily doped      (b) only the *N*-region is heavily doped  
 (c) both *P*- and *N*-regions are heavily doped      (d) both *P*- and *N*-regions are lightly doped
20. A Zener diode, when used in voltage stabilization circuits, is biased in  
 (a) reverse-bias region below the breakdown voltage  
 (b) reverse breakdown region  
 (c) forward-bias region  
 (d) forward-bias constant current mode
21. In a tunnel diode, the width of the depletion layer is of the order of  
 (a) 0.1 micron      (b) 1.0 micron  
 (c) 0.1 armstrong      (d) 100 armstrong

22. The light emitting diode (LED) emits light of a particular colour because  
 (a) it is fabricated from a fluorescent material  
 (b) transition between energy levels of the carriers takes place while crossing the *p-n* junction  
 (c) heat generated in the diode is converted into light  
 (d) the bandgap of the semiconductor material used in the fabrication of the diode is equal to the energy  $h_v$  of the light photon
23. The photoconductive cell most popularly used for visible light spectrum uses  
 (a) Ge (b) Si (c) GaAs (d) cadmium sulphide
24. The colour of the emitted light while using gallium phosphide GaP in a light emitting diode is  
 (a) invisible (b) red or green (c) red or yellow (d) green or yellow
25. LEDs operate at voltage levels from  
 (a) 10 to 150 V (b) 1 to 15 V (c) 1.5 to 3.3 V (d) 15 to 33 V
26. The charge on the dielectric in the plasma display channels which allows the cell to refire on the next transition of the applied voltage is called  
 (a) wall voltage (b) cut-off voltage (c) pinch-off voltage (d) none of the above
27. The isolation provided by the optoisolator is due to  
 (a) coupling wires (b) capacitors (c) transformers (d) none of the above
28. The refractive index profile which gives the variation of the refractive index with distance along the cross section of the fibre may be defined as  
 (a)  $n(r) = n_1; r < a$  (core) (b)  $n(r) = n_2; r \geq a$  (cladding)  
 (c) both (a) and (b) (d) none of the above
29. In the forward blocking region of a silicon-controlled rectifier, the SCR is  
 (a) in the OFF-state (b) in the ON-state  
 (c) reverse biased (d) at the point of breakdown
30. In the fabrication of *NPN* transistor in an IC, the buried layer on the *P*-type substrate is  
 (a)  $P^+$  doped (b)  $N^+$  doped  
 (c) used to reduce the parasitic capacitance (d) located in the emitter region
31. The  $di/dt$  protection for an SCR is achieved through the use of  
 (a)  $R$  in series with SCR (b)  $RL$  in series with SCR  
 (c)  $RL$  across SCR (d)  $L$  in series with SCR
32. What are the different methods followed to take *PNPN* device from its conducting state to the non-conducting state?  
 (1) reducing the anode current below the holding value  
 (2) reducing the gate current to zero  
 (3) reducing the gate voltage to zero  
 (4) reducing anode voltage below the holding value
- Select the correct answer using the codes given below:  
 (a) 1 and 2 (b) 2 and 3 (c) 1 and 4 (d) 3 and 4
33. A *PNPN* diode is a  
 (a) negative resistance device (b) current controllable device  
 (c) controlled rectifier (d) current controlled negative resistance device
34. The *PNPN* diode  
 (a) is unilateral device  
 (b) is a bilateral device  
 (c) may function either as a unilateral or as a bilateral device  
 (d) functions as a bilateral device depending on the ambient temperature

- 35.** In a *PNP* diode, breakdown takes place when  
 (a)  $(\alpha_1 + \alpha_2) = 0.5$       (b)  $(\alpha_1 + \alpha_2) = 0.9$   
 (c)  $(\alpha_1 + \alpha_2) = 1$       (d)  $\alpha_1 = \alpha_2$   
 where  $\alpha_1$  and  $\alpha_2$  refer to the constituent transistors
- 36.** After firing an SCR, if the gate pulse is removed, the SCR current  
 (a) remains the same      (b) reduces to zero  
 (c) rises up      (d) rises a little and then falls to zero
- 37.** An SCS is  
 (a) a *PNP* diode with three terminals      (b) a *PNP* diode with one gate  
 (c) a *PNP* diode with two gates      (d) a *PNP* diode made of germanium
- 38.** TRIAC is a  
 (a) 2-terminal bidirectional switch      (b) 3-terminal bidirectional switch  
 (c) 2-terminal unilateral switch      (d) 3-terminal unilateral switch
- 39.** DIAC is a  
 (a) 2-terminal bidirectional switch      (b) 2-terminal unilateral switch  
 (c) 3-terminal bidirectional switch      (d) 3-terminal unilateral switch
- 40.** DIAC is a silicon device with  
 (a) 3 layers and one gate      (b) 3 layers and no gate  
 (c) 4 layers and one gate      (d) 4 layers and no gate
- 41.** A TRIAC can be triggered with  
 (a) positive pulse      (b) negative pulse  
 (c) both positive and negative pulses      (d) light
- 42.** A DIAC is a  
 (a) four-layer, three-junction device      (b) five-layer, four-junction device  
 (c) three-layer, two-junction device      (d) none of the above
- 43.** Which of the following is not an application of UJT?  
 (a) Relaxation oscillator      (b) Speed control circuit  
 (c) Differentiate a pulse      (d) Phase control circuit
- 44.** Pick the odd one out in terms of  $V$ - $I$  behaviour.  
 (a) BJT      (b) MOSFET      (c) UJT      (d)  $PN$  junction diode
- 45.** A UJT relaxation oscillator circuit produces a sawtooth waveform  
 (a) at the  $B_1$  terminal      (b) at the  $B_2$  terminal  
 (c) across the capacitor  $C_E$       (d) none of the above
- 46.** Intrinsic stand-off ratio  $\eta$  is given by  
 (a)  $\frac{R_{B2}}{R_{B1} + R_{B2}}$       (b)  $\frac{R_{B1} + R_{B2}}{R_{B2}}$       (c)  $\frac{R_{B1} + R_{B2}}{R_{B1}}$       (d)  $\frac{R_{B1}}{R_{B1} + R_{B2}}$
- 47.** Frequency of oscillation of a sawtooth waveform using UJT is given by  
 (a)  $f_o = \frac{1}{2.303 R_E C_E \log_{10}(1-\eta)}$       (b)  $f_0 = \frac{1}{2.303 R_E C_E \log_{10}\left(\frac{1}{1-\eta}\right)}$   
 (c)  $f_o = \frac{1}{1.289 R_E C_E \log_{10}(1-\eta)}$       (d)  $f_0 = \frac{1}{1.289 R_E C_E \log_{10}\left(\frac{1}{1-\eta}\right)}$



# Rectifiers and Filters

---

## 3.1 INTRODUCTION

---

All electronic circuits need dc power supply either from battery or power-pack units. Transformers, rectifiers and filters form the basic building blocks of a linear power supply. A transformer supplies ac voltage at the required level. This bidirectional ac voltage is converted into a unidirectional pulsating dc using a rectifier. The unwanted ripple contents of this pulsating dc are removed by a filter to get pure dc voltage. The output of the filter is fed to a regulator which gives a steady dc output independent of load variations and input supply fluctuations. This chapter mainly discusses the operation and characteristics of different types of rectifiers and filters.

---

## 3.2 RECTIFIERS

---

Rectifier is defined as an electronic circuit used for converting ac voltage into unidirectional voltage. A rectifier utilizes unidirectional conduction device like a vacuum diode or *PN* junction diode. Rectifiers are classified depending upon the period of conduction as half-wave rectifier and full-wave rectifier.

### 3.2.1 Half-wave Rectifier

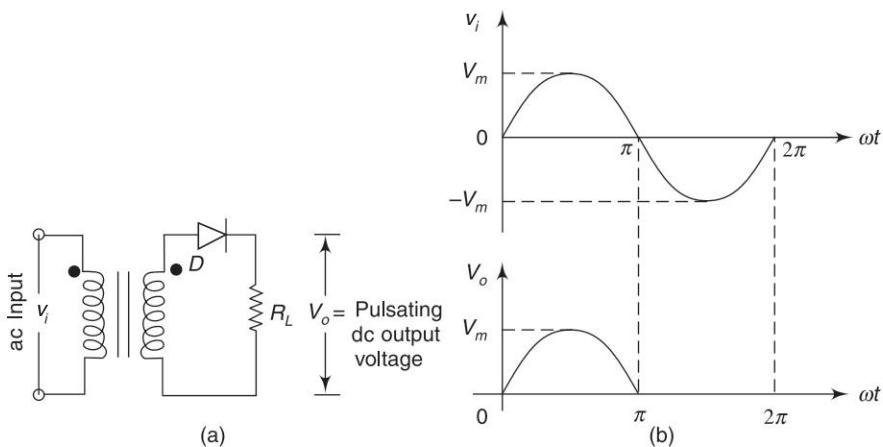
It converts an ac voltage into a pulsating dc voltage using only one half of the applied ac voltage. The rectifying diode conducts only during one half of the ac cycle. Figure 3.1 shows the basic circuit and waveforms of a half-wave rectifier (HWR).

Let  $v_i$  be the voltage applied to the primary of the transformer and given by the equation

$$v_i = V_m \sin \omega t; V_m \gg V_\gamma$$

where  $V_\gamma$  is the cut-in voltage of the diode. During the positive half cycle of the input signal, the anode of the diode becomes more positive with respect to the cathode and hence, the diode  $D$  conducts. For an ideal diode, the forward voltage drop is zero. So, the whole input voltage will appear across the load resistance,  $R_L$ .

During negative half cycle of the input signal, the anode of the diode becomes negative with respect to the cathode and hence, diode  $D$  does not conduct. For an ideal diode, the impedance offered by the diode is infinity. So the whole input voltage appears across diode  $D$ . Hence, the voltage drop across  $R_L$  is zero.



**Fig. 3.1** (a) Basic structure of a half-wave rectifier (b) Input output waveforms of half-wave rectifier

**Ripple Factor (\$\Gamma\$)** The ratio of rms value of ac component to the dc component in the output is known as ripple factor (\$\Gamma\$).

$$\Gamma = \frac{\text{rms value of ac component}}{\text{dc value of component}} = \frac{V_{r,\text{rms}}}{V_{dc}}$$

where \$V\_{r,\text{rms}} = \sqrt{V\_{\text{rms}}^2 - V\_{dc}^2}\$.

$$\text{Therefore, } \Gamma = \sqrt{\left(\frac{V_{\text{rms}}}{V_{dc}}\right)^2 - 1}$$

The rms value of a continuous-time periodic waveform is the square root of the ratio of the square of that waveform function to the time period \$T\$, as given by

$$\begin{aligned} V_{\text{rms}} &= \sqrt{\frac{\text{Square of the area under the curve for one cycle}}{\text{Time period}}} \\ &= \sqrt{\frac{1}{T} \int_0^T [x(t)]^2 dt} \end{aligned}$$

The average or the dc content of the voltage across the load is given by

$$\begin{aligned} V_{av} &= V_{dc} = \frac{1}{2\pi} \left[ \int_0^\pi V_m \sin \omega t d(\omega t) + \int_\pi^{2\pi} 0.d(\omega t) \right] \\ &= \frac{V_m}{2\pi} [-\cos \omega t]_0^\pi = \frac{V_m}{\pi} \end{aligned}$$

$$\text{Therefore, } I_{dc} = \frac{V_{dc}}{R_L} = \frac{V_m}{\pi R_L} = \frac{I_m}{\pi}$$

If the values of diode forward resistance ( $r_f$ ) and the transformer secondary winding resistance ( $r_s$ ) are also taken into account, then

$$V_{dc} = \frac{V_m}{\pi} - I_{dc} (r_s + r_f)$$

$$I_{dc} = \frac{V_{dc}}{(r_s + r_f) + R_L} = \frac{V_m}{\pi(r_s + r_f + R_L)}$$

The rms voltage at the load resistance can be calculated as

$$V_{rms} = \left[ \frac{1}{2\pi} \int_0^{\pi} V_m^2 \sin^2 \omega t d(\omega t) \right]^{\frac{1}{2}}$$

$$= V_m \left[ \frac{1}{4\pi} \int_0^{\pi} (1 - \cos 2\omega t) d\omega t \right]^{\frac{1}{2}} = \frac{V_m}{2}$$

$$\text{Therefore, } \Gamma = \sqrt{\left[ \frac{V_m/2}{V_m/\pi} \right]^2 - 1} = \sqrt{\left( \frac{\pi}{2} \right)^2 - 1} = 1.21$$

From this expression, it is clear that the amount of ac present in the output is 121% of the dc voltage. So the half-wave rectifier is not practically useful in converting ac into dc.

**Efficiency ( $\eta$ )** The ratio of dc output power to ac input power is known as rectifier efficiency ( $\eta$ ).

$$\eta = \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{\frac{(V_{dc})^2}{R_L}}{\frac{(V_{rms})^2}{R_L}} = \frac{\left( \frac{V_m}{\pi} \right)^2}{\left( \frac{V_m}{2} \right)^2} = \frac{4}{\pi^2} = 0.406 = 40.6\%$$

The maximum efficiency of a half-wave rectifier is 40.6%.

**Peak Inverse Voltage (PIV)** It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half cycle. For half-wave rectifier, PIV is  $V_m$ .

**Transformer Utilization Factor (TUF)** In the design of any power supply, the rating of the transformer should be determined. This can be done with a knowledge of the dc power delivered to the load and the type of rectifying circuit used.

$$\text{TUF} = \frac{\text{dc power delivered to the load}}{\text{ac rating of the transformer secondary}}$$

$$= \frac{P_{dc}}{P_{ac \text{ rated}}}$$

In the half-wave rectifying circuit, the rated voltage of the transformer secondary is  $V_m/\sqrt{2}$ , but the actual rms current flowing through the winding is only  $\frac{I_m}{2}$ , not  $I_m/\sqrt{2}$ .

$$\text{TUF} = \frac{\frac{I_m^2}{\pi^2} R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{2}} = \frac{\frac{V_m^2}{\pi^2} \frac{1}{R_L}}{\frac{V_m}{\sqrt{2}} \frac{V_m}{2R_L}} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

The TUF for a half-wave rectifier is 0.287.

- **Form Factor**

$$\text{Form factor} = \frac{\text{rms value}}{\text{average value}} = \frac{V_m/2}{V_m/\pi} = \frac{\pi}{2} = 1.57$$

- **Peak Factor**

$$\text{Peak factor} = \frac{\text{peak value}}{\text{rms value}} = \frac{V_m}{V_m/2} = 2$$

### EXAMPLE 3.1

A half-wave rectifier, having a resistive load of  $1000\Omega$ , rectifies an alternating voltage of 325 V peak value and the diode has a forward resistance of  $100\Omega$ . Calculate (a) peak, average and rms values of current (b) dc power output (c) ac input power and (d) efficiency of the rectifier.

#### Solution

$$(a) \text{ Peak value of current, } I_m = \frac{V_m}{r_f + R_L} = \frac{325}{100 + 1000} = 295.45 \text{ mA}$$

$$\text{Average current, } I_{dc} = \frac{I_m}{\pi} = \frac{295.45}{\pi} \text{ mA} = 94.046 \text{ mA}$$

$$\text{RMS value of current, } I_{rms} = \frac{I_m}{2} = \frac{295.45}{2} = 147.725 \text{ mA}$$

$$(b) \text{ The dc power output, } P_{dc} = I_{dc}^2 \times R_L \\ = (94.046 \times 10^{-3})^2 \times 1000 = 8.845 \text{ W}$$

$$(c) \text{ The ac input power, } P_{ac} = (I_{rms})^2 \times (r_f + R_L) \\ = (147.725 \times 10^{-3})^2 (1100) = 24 \text{ W}$$

$$(d) \text{ Efficiency of rectification, } \eta = \frac{P_{dc}}{P_{ac}} = \frac{8.845}{24} = 36.85\%.$$

### EXAMPLE 3.2

A half-wave rectifier is used to supply 24 V dc to a resistive load of  $500\Omega$  and the diode has a forward resistance of  $50\Omega$ . Calculate the maximum value of the ac voltage required at the input.

**Solution** Average value of load current,

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{24}{500} = 48 \text{ mA}$$

Maximum value of load current,  $I_m = \pi \times I_{dc} = \pi \times 48 \text{ mA} = 150.8 \text{ mA}$

Therefore, maximum ac voltage required at the input,

$$V_m = I_m \times (r_f + R_L) = 150.8 \times 10^{-3} \times 550 = 82.94 \text{ V}$$

### EXAMPLE 3.3

An ac supply of 230 V is applied to a half-wave rectifier circuit through transformer of turns ratio 5:1. Assume the diode is an ideal one. The load resistance is  $300 \Omega$ . Find (a) dc output voltage, (b) PIV, (c) maximum, and (d) average values of power delivered to the load.

**Solution**

(a) The transformer secondary voltage  $= \frac{230}{5} = 46 \text{ V}$

Maximum value of secondary voltage,  $V_m = \sqrt{2} \times 46 = 65 \text{ V}$

Therefore, dc output voltage,  $V_{dc} = \frac{V_m}{\pi} = \frac{65}{\pi} = 20.7 \text{ V}$

(b) PIV of a diode  $V_m = 65 \text{ V}$

(c) Maximum value of load current,  $I_m = \frac{V_m}{R_L} = \frac{65}{300} = 0.217 \text{ A}$

Therefore, maximum value of power delivered to the load,

$$P_m = I_m^2 \times R_L = (0.217)^2 \times 300 = 14.1 \text{ W}$$

(d) The average value of load current,  $I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.7}{300} = 0.069 \text{ A}$

Therefore, average value of power delivered to the load,

$$P_{dc} = I_{dc}^2 \times R_L = (0.069)^2 \times 300 = 1.43 \text{ W}$$

### EXAMPLE 3.4

An HWR has a load of  $3.5 \text{ k}\Omega$ . If the diode resistance and secondary coil resistance together have a resistance of  $800 \Omega$  and the input voltage has a signal voltage of peak value 240 V. Calculate

- (a) peak, average and rms values of current flowing
- (b) dc power output
- (c) ac power input
- (d) efficiency of the rectifier

**Solution** Load resistance in an HWR,  $R_L = 3.5 \text{ k}\Omega$

Diode resistance and secondary coil resistance,  $r_f + r_s = 800 \Omega$

Peak value of input voltage = 240 V

(a) Peak value of current,  $I_m = \frac{V_m}{r_s + r_f + R_L} = \frac{240}{4300} = 55.81 \text{ mA}$

Average value of current,  $I_{dc} = \frac{I_m}{\pi} = \frac{55.81 \times 10^{-3}}{\pi} = 17.77 \text{ mA}$

The rms value of current,  $I_{rms} = \frac{I_m}{2} = \frac{55.81 \times 10^{-3}}{2} = 27.905 \text{ mA}$

(b) The dc power output is

$$P_{dc} = (I_{dc})^2 R_L = (17.77 \times 10^{-3})^2 \times 3500 = 1.105 \text{ W}$$

(c) The ac power input is

$$P_{ac} = (I_{rms})^2 \times (r_f + R_L) = (27.905 \times 10^{-3})^2 \times 4300 = 3.348 \text{ W}$$

(d) Efficiency of the rectifier is

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{1.105}{3.348} \times 100 = 33\%$$

### EXAMPLE 3.5

An HWR circuit supplies 100 mA dc to a  $250 \Omega$  load. Find the dc output voltage, PIV rating of a diode and the rms voltage for the transformer supplying the rectifier.

**Solution** Given  $I_{dc} = 100 \text{ mA}$ ,  $R_L = 250 \Omega$

(a) The dc output voltage,

$$V_{dc} = I_{dc} \times R_L = 100 \times 10^{-3} \times 250 = 25 \text{ V}$$

(b) The maximum value of secondary voltage,

$$V_m = \pi \times V_{dc} = \pi \times 25 = 78.54 \text{ V}$$

(c) PIV rating of a diode,  $V_m = 78.54 \text{ V}$

(d) The rms voltage for the transformer supplying the rectifier,

$$V_{rms} = \frac{V_m}{2} = \frac{78.54}{2} = 39.27 \text{ V}$$

### EXAMPLE 3.6

A voltage of  $200 \cos \omega t$  is applied to HWR with load resistance of  $5 \text{ k}\Omega$ . Find (a) the maximum dc current component, (b) rms current, (c) ripple factor, (d) TUF, and (e) rectifier efficiency,

**Solution** Given applied voltage =  $200 \cos \omega t$ ,  $V_m = 200 \text{ V}$ ,  $R_L = 5 \text{ k}\Omega$

(a) To find dc current:

$$I_m = \frac{V_m}{R_L} = \frac{200}{5 \times 10^3} = 40 \text{ mA}$$

Therefore,

$$I_{dc} = \frac{I_m}{\pi} = \frac{40 \times 10^{-3}}{\pi} = 12.73 \text{ mA}$$

(b) To find rms current:

$$I_{\text{rms}} = \frac{I_m}{2} = \frac{40 \times 10^{-3}}{2} = 20 \text{ mA}$$

(c) Ripple factor:  $\Gamma = \sqrt{\left(\frac{I_{\text{rms}}}{I_{\text{dc}}}\right)^2 - 1} = \sqrt{\left(\frac{20 \times 10^{-3}}{12.73 \times 10^{-3}}\right)^2 - 1} = 1.21$

(d) To determine TUF:

$$\text{TUF} = \frac{P_{\text{dc}}}{P_{\text{ac(rated)}}}$$

$$P_{\text{dc}} = I_{\text{dc}}^2 R_L = (12.73 \times 10^{-3})^2 \times 5 \times 10^3 = 0.81 \text{ W}$$

$$P_{\text{ac(rated)}} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{2} = \frac{200}{\sqrt{2}} \times \frac{40 \times 10^{-3}}{2} = 2.828$$

Therefore,

$$\text{TUF} = \frac{P_{\text{dc}}}{P_{\text{ac(rated)}}} = \frac{0.81}{2.828} = 0.2863$$

(e) Rectifier efficiency:  $\eta = \frac{P_{\text{dc}}}{P_{\text{ac}}}$

$$P_{\text{dc}} = 0.81 \text{ W}$$

$$P_{\text{ac}} = I_{\text{rms}}^2 R_L = (20 \times 10^{-3})^2 \times 5 \times 10^3 = 2 \text{ W}$$

Therefore,

$$\eta = \frac{P_{\text{dc}}}{P_{\text{ac}}} \times 100 = \frac{0.81}{2} \times 100 = 40.5\%$$

### EXAMPLE 3.7

A diode has an internal resistance of  $20 \Omega$  and  $1,000 \Omega$  load from a  $110 \text{ V}$  rms source of supply. Calculate (a) the efficiency of rectification and (b) the percentage regulation from no load to full load.

**Solution** Given  $r_f = 20 \Omega$ ,  $R_L = 1,000 \Omega$  and  $V_{\text{rms}} (\text{secondary}) = 110 \text{ V}$

(a) The half-wave rectifier uses a single diode.

$$\text{Therefore, } V_m = \sqrt{2} V_{\text{rms}} (\text{secondary}) = \sqrt{2} \times 110 = 155.56 \text{ V}$$

$$I_m = \frac{V_m}{r_f + R_L} = \frac{155.56}{20 + 1000} = 0.1525 \text{ A}$$

$$I_{\text{dc}} = \frac{I_m}{\pi} = \frac{0.1525}{\pi} = 0.04854 \text{ A}$$

$$V_{\text{dc}} = I_{\text{dc}} R_L = 0.04854 \times 1000 = 48.54 \text{ V}$$

$$P_{\text{dc}} = V_{\text{dc}} I_{\text{dc}} = 48.54 \times 0.04854 = 2.36 \text{ W}$$

$$P_{\text{ac}} = I_{\text{rms}}^2 (r_f + R_L) = \left(\frac{I_m}{2}\right)^2 (r_f + R_L) \quad \left(\text{since } I_{\text{rms}} = \frac{I_m}{2} \text{ for half-wave}\right)$$

$$= \left( \frac{0.1525}{2} \right)^2 (20 + 1000) = 5.93 \text{ W}$$

Efficiency,  $\eta = \frac{P_{dc}}{P_{ac}} \times 100 = \frac{2.36}{5.93} \times 100 = 39.7346\%$

(b) Percentage of line regulation =  $\frac{\frac{V_m}{\pi} - V_{dc}}{V_{dc}} \times 100 = \frac{\frac{155.56}{\pi} - 48.54}{48.54} \times 100 = 2\%$

### EXAMPLE 3.8

Show that maximum dc output power  $P_{dc} = V_{dc} \times I_{dc}$  in a half-wave single-phase circuit occurs when the load resistance equals diode resistance  $r_f$ .

**Solution** For a half-wave rectifier,

$$I_m = \frac{V_m}{r_f + R_L}$$

$$I_{dc} = \frac{I_m}{\pi} = \frac{V_m}{\pi(r_f + R_L)}$$

and

$$V_{dc} = I_{dc} \times R_L$$

Therefore,  $P_{dc} = V_{dc} \times I_{dc} = I_{dc}^2 R_L = \frac{V_m^2 R_L}{\pi^2 (r_f + R_L)^2}$

For this power to be maximum,

$$\frac{dP_{dc}}{dR_L} = 0$$

$$\frac{d}{dR_L} \left[ \frac{V_m^2 R_L}{\pi^2 (r_f + R_L)^2} \right] = \frac{V_m^2}{\pi^2} \left[ \frac{(r_f + R_L)^2 - R_L \times 2(r_f + R_L)}{(r_f + R_L)^4} \right] = 0$$

$$(r_f + R_L)^2 - 2R_L(r_f + R_L) = 0$$

$$r_f^2 + 2r_f R_L + R_L^2 - 2r_f R_L - 2R_L^2 = 0$$

$$r_f^2 - R_L^2 = 0$$

$$R_L^2 = r_f^2$$

Thus, the power output is maximum if  $R_L = r_f$

### EXAMPLE 3.9

The transformer of a half-wave rectifier has a secondary voltage of  $30 \text{ V}_{rms}$  with a winding resistance of  $10 \Omega$ .

The semiconductor diode in the circuit has a forward resistance of  $100 \Omega$ . Calculate (a) no load dc voltage (b) dc output voltage at  $I_L = 25 \text{ mA}$  (c) % regulation at  $I_L = 25 \text{ mA}$  (d) ripple voltage across the load (e) ripple frequency (f) ripple factor (g) dc power output and (h) PIV of the semiconductor diode.

**Solution**

$$V_{\text{rms}} (\text{secondary}) = 30 \text{ V}, r_s = 10 \Omega, r_f = 100 \Omega$$

$$V_m = \sqrt{2} \times V_{\text{rms}} = \sqrt{2} \times 30 = 42.4264 \text{ V}$$

$$(a) \quad V_{\text{dc}} = \frac{V_m}{\pi} = \frac{42.4264}{\pi} = 13.5047 \text{ V}$$

$$(b) \quad I_L = I_{\text{dc}} = 25 \text{ mA}$$

$$V_{\text{dc}} = I_{\text{dc}} R_L = \frac{I_m}{\pi} R_L = \frac{V_m}{\pi(r_f + r_s + R_L)} \times R_L$$

Here,

$$R_L = \frac{V_{\text{dc}}}{I_{\text{dc}}}$$

Therefore,

$$V_{\text{dc}} = \frac{V_m}{\pi \left( r_f + r_s + \frac{V_{\text{dc}}}{I_{\text{dc}}} \right)} \times \frac{V_{\text{dc}}}{I_{\text{dc}}}$$

$$V_{\text{dc}} = \frac{42.426 V_{\text{dc}}}{\pi \left( 100 + 10 + \frac{V_{\text{dc}}}{25 \times 10^{-3}} \right)} \times \frac{1}{25 \times 10^{-3}}$$

$$V_{\text{dc}} (110 + 40V_{\text{dc}}) = 540.1897 V_{\text{dc}}$$

$$V_{\text{dc}} = \frac{540.1897 - 110}{40} = 10.7547 \text{ V}$$

$$(c) \quad \text{Percentage of regulation} = \frac{V_{\text{dc}(NL)} - V_{\text{dc}(FL)}}{V_{\text{dc}(FL)}} \times 100 = \frac{13.5047 - 10.7547}{10.7547} \times 100 = 25.569\%$$

$$(d) \quad I_m = \frac{V_m}{r_f + r_s + R_L}, \text{ where } R_L = \frac{V_{\text{dc}}}{I_{\text{dc}}} = \frac{10.7547}{25 \times 10^{-3}} = 430.188 \text{ V}$$

Therefore,

$$I_m = \frac{42.4264}{100 + 10 + 430.188} = 0.07854 \text{ A}$$

$$I_{\text{rms}} = \frac{I_m}{2} = 0.03927 \text{ A}$$

$$\Gamma = \sqrt{\left( \frac{I_{\text{rms}}}{I_{\text{dc}}} \right)^2 - 1} = \sqrt{\left( \frac{0.03927}{25 \times 10^{-3}} \right)^2 - 1} = 1.21$$

$$\text{Ripple voltage} \quad \Gamma \times V_{\text{dc}} = 1.21 \times 10.7547 = 13.02791 \text{ V}$$

$$(e) \quad \text{Ripple frequency,} \quad f = 50 \text{ Hz}$$

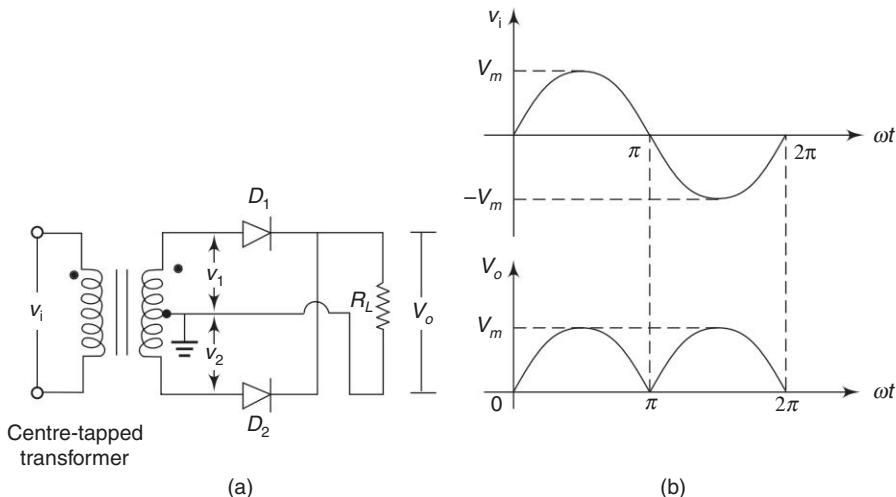
(f)  $\Gamma = \text{ripple factor} = 1.21$

(g)  $P_{\text{dc}} = V_{\text{dc}} I_{\text{dc}} = 10.7547 \times 25 \times 10^{-3} = 0.2688 \text{ W}$

(h)  $\text{PIV} = V_m = 42.4264 \text{ V}$

### 3.2.2 Full-wave Rectifier

It converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. It uses two diodes of which one conducts during one half-cycle while the other diode conducts during the other half-cycle of the applied ac voltage. There are two types of full-wave rectifiers, viz., (i), full-wave rectifier with centre tapped transformer, and (ii) full-wave rectifier without transformer (bridge rectifier).



**Fig. 3.2** Full-wave rectifier

Figure 3.2 shows the basic circuit and waveforms of full-wave rectifier with a center tap transformer. During positive half of the input signal, the anode of the diode  $D_1$  becomes positive and at the same time, the anode of diode  $D_2$  becomes negative. Hence,  $D_1$  conducts and  $D_2$  does not conduct. The load current flows through  $D_1$  and the voltage drop across  $R_L$  will be equal to the input voltage.

During the negative half-cycle of the input, the anode of  $D_1$  becomes negative and the anode of  $D_2$  becomes positive. Hence,  $D_1$  does not conduct and  $D_2$  conducts. The load current flows through  $D_2$  and the voltage drop across  $R_L$  will be equal to the input voltage.

#### Ripple Factor ( $\Gamma$ )

$$\Gamma = \sqrt{\left(\frac{V_{\text{rms}}}{V_{\text{dc}}}\right)^2 - 1}$$

The average voltage or dc voltage available across the load resistance is

$$\begin{aligned}
 V_{dc} &= \frac{1}{\pi} \int_0^{\pi} V_m \sin \omega t \, d(\omega t) \\
 &= \frac{V_m}{\pi} [-\cos \omega t]_0^{\pi} = \frac{2V_m}{\pi} \\
 I_{dc} &= \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi} \text{ and } I_{rms} = \frac{I_m}{\sqrt{2}}
 \end{aligned}$$

If the diode forward resistance ( $r_f$ ) and the transformer secondary winding resistance ( $r_s$ ) are included in the analysis, then

$$\begin{aligned}
 V_{dc} &= \frac{2V_m}{\pi} - I_{dc} (r_s + r_f) \\
 I_{dc} &= \frac{V_{dc}}{(r_s + r_f) + R_L} = \frac{2V_m}{\pi(r_s + r_f + R_L)}
 \end{aligned}$$

The rms value of the voltage at the load resistance is

$$\begin{aligned}
 V_{rms} &= \sqrt{\left[ \frac{1}{\pi} \int_0^{\pi} V_m^2 \sin^2 \omega t \, d(\omega t) \right]} = \frac{V_m}{\sqrt{2}} \\
 \text{Therefore, } \Gamma &= \sqrt{\left( \frac{V_m/\sqrt{2}}{2V_m/\pi} \right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.482
 \end{aligned}$$

**Efficiency ( $\eta$ )** The ratio of dc output power to ac input power is known as rectifier efficiency ( $\eta$ ).

$$\begin{aligned}
 \eta &= \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}} \\
 &= \frac{(V_{dc})^2 / R_L}{(V_{rms})^2 / R_L} = \frac{\left[ \frac{2V_m}{\pi} \right]^2}{\left[ \frac{V_m}{\sqrt{2}} \right]^2} \\
 &= \frac{8}{\pi^2} = 0.812 = 81.2\%
 \end{aligned}$$

The maximum efficiency of a full-wave rectifier is 81.2%.

**Transformer Utilization Factor (TUF)** The average TUF in a full-wave rectifying circuit is determined by considering the primary and secondary windings separately and it gives a value of 0.693.

- **Form Factor**

$$\text{Form factor} = \frac{\text{rms value of the output voltage}}{\text{average value of the output voltage}} = \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{\pi}{2\sqrt{2}} = 1.11$$

- **Peak Factor**

$$\text{Peak factor} = \frac{\text{peak value of the output voltage}}{\text{rms value of the output voltage}} = \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2}$$

Peak inverse voltage for full-wave rectifier is  $2V_m$  because the entire secondary voltage appears across the non-conducting diode.

### EXAMPLE 3.10

A 230 V, 60 Hz voltage is applied to the primary of a 5:1 step-down, centre-tap transformer used in a full-wave rectifier having a load of  $900\ \Omega$ . If the diode resistance and secondary coil resistance together has a resistance of  $100\ \Omega$ , determine (a) dc voltage across the load, (b) dc current flowing through the load, (c) dc power delivered to the load, (d) PIV across each diode, (e) ripple voltage and its frequency and (f) rectification efficiency.

**Solution** The voltage across the two ends of secondary  $= \frac{230}{5} = 46\ \text{V}$

$$\text{Voltage from centre tapping to one end, } V_{\text{rms}} = \frac{46}{2} = 23\ \text{V}$$

$$(a) \text{ The dc voltage across the load, } V_{\text{dc}} = \frac{2V_m}{\pi} = \frac{2 \times 23 \times \sqrt{2}}{\pi} = 20.7\ \text{V}$$

$$(b) \text{ The dc current flowing through the load, } I_{\text{dc}} = \frac{V_{\text{dc}}}{(r_s + r_f + R_L)} = \frac{20.7}{1000} = 20.7\ \text{mA}$$

$$(c) \text{ The dc power delivered to the load, } P_{\text{dc}} = (I_{\text{dc}})^2 \times R_L = (20.7 \times 10^{-3})^2 \times 900 = 0.386\ \text{W}$$

$$(d) \text{ PIV across each diode} \\ = 2V_m = 2 \times 23 \times \sqrt{2} = 65\ \text{V}$$

$$(e) \text{ Ripple voltage,} \\ V_{r,\text{rms}} = \sqrt{(V_{\text{rms}})^2 - (V_{\text{dc}})^2} \\ = \sqrt{(23)^2 - (20.7)^2} = 10.05\ \text{V}$$

$$\text{Frequency of ripple voltage} = 2 \times 60 = 120\ \text{Hz}$$

$$(f) \text{ Rectification efficiency,} \\ \eta = \frac{P_{\text{dc}}}{P_{\text{ac}}} = \frac{(V_{\text{dc}})^2 / R_L}{(V_{\text{rms}})^2 / R_L} = \frac{(V_{\text{dc}})^2}{(V_{\text{rms}})^2} \\ = \frac{(20.7)^2}{(23)^2} = \frac{428.49}{529} = 0.81$$

Therefore, percentage of rectification efficiency = 81%

### EXAMPLE 3.11

A full-wave rectifier has a centre-tap transformer of 100-0-100 V and each one of the diodes is rated at  $I_{\text{max}} = 400\ \text{mA}$  and  $I_{\text{av}} = 150\ \text{mA}$ . Neglecting the voltage drop across the diodes, determine (a) the value of load resistor that gives the largest dc power output, (b) dc load voltage and current, and (c) PIV of each diode.

**Solution**

- (a) We know that the maximum value of current flowing through the diode for normal operation should not exceed 80% of its rated current.

Therefore,  $I_{\max} = 0.8 \times 400 = 320 \text{ mA}$

The maximum value of the secondary voltage,

$$V_m = \sqrt{2} \times 100 = 141.4 \text{ V}$$

Therefore, the value of load resistor that gives the largest dc power output

$$R_L = \frac{V_m}{I_{\max}} = \frac{141.4}{320 \times 10^{-3}} = 442 \Omega$$

$$(b) \text{ The dc (load) voltage, } V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 141.4}{\pi} = 90 \text{ V}$$

$$\text{The dc load current, } I_{dc} = \frac{V_{dc}}{R_L} = \frac{90}{442} = 0.204 \text{ A}$$

$$(c) \text{ PIV of each diode} = 2V_m = 2 \times 141.4 = 282.8 \text{ V}$$

### EXAMPLE 3.12

A full-wave rectifier delivers 50 W to a load of  $200 \Omega$ . If the ripple factor is 1%, calculate the ac ripple voltage across the load.

**Solution** The dc power delivered to the load,

$$P_{dc} = \frac{V_{dc}^2}{R_L}$$

$$\text{Therefore, } V_{dc} = \sqrt{P_{dc} \times R_L} = \sqrt{50 \times 200} = 100 \text{ V}$$

$$\text{The ripple factor, } \Gamma = \frac{V_{ac}}{V_{dc}}$$

$$\text{i.e., } 0.01 = \frac{V_{ac}}{100}$$

$$\text{Therefore, the ac ripple voltage across the load, } V_{ac} = 1 \text{ V}$$

### EXAMPLE 3.13

In a full-wave rectifier, the transformer rms secondary voltage from centre tap to each end of the secondary is 50 V. The load resistance is  $900 \Omega$ . If the diode resistance and transformer secondary winding resistance together has a resistance of  $100 \Omega$ , determine the average load current and rms value of load current?

**Solution** Voltage from centre tapping to one end,  $V_{rms} = 50 \text{ V}$

$$\text{Maximum load current, } I_m = \frac{V_m}{r_s + r_f + R_L} = \frac{V_{rms} \times \sqrt{2}}{r_s + r_f + R_L} = \frac{70.7}{1000} = 70.7 \text{ mA}$$

$$\text{Average load current, } I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 70.7 \times 10^{-3}}{\pi} = 45 \text{ mA}$$

RMS value of load current,  $I_{\text{rms}} = \frac{I_m}{\sqrt{2}} = \frac{70.7 \times 10^{-3}}{\sqrt{2}} = 50 \text{ mA}$

**EXAMPLE 3.14**

A full-wave rectifier circuit uses two silicon diodes with a forward resistance of  $20 \Omega$  each. A dc voltmeter connected across the load of  $1 \text{ k}\Omega$  reads 55.4 volt. Calculate

- (a)  $I_{\text{rms}}$
- (b) average voltage across each diode
- (c) ripple factor and
- (d) transformer secondary voltage rating

**Solution** Given  $V_{\text{dc}} = 55.4 \text{ V}$  and  $R_L = 1 \text{ k}\Omega$

$$(a) I_{\text{dc}} = \frac{V_{\text{dc}}}{(r_f + R_L)} = \frac{55.4}{20 + 1000} = 54.31 \text{ mA}$$

We know that  $I_{\text{dc}} = \frac{2I_m}{\pi}$  and  $I_{\text{rms}} = \frac{I_m}{\sqrt{2}}$

$$I_m = I_{\text{dc}} \times \frac{\pi}{2} = 54.31 \times 10^{-3} \times \frac{\pi}{2} = 85.31 \text{ mA}$$

$$I_{\text{rms}} = \frac{I_m}{\sqrt{2}} = \frac{85.31 \times 10^{-3}}{\sqrt{2}} = 60.32 \text{ mA}$$

- (b) The average voltage across each silicon diode will be 0.72 V.
- (c) To find ripple factor  $\Gamma$

$$\Gamma = \sqrt{\left(\frac{I_{\text{rms}}}{I_{\text{dc}}}\right)^2 - 1} = \sqrt{\left(\frac{60.32 \times 10^{-3}}{54.31 \times 10^{-3}}\right)^2 - 1} = 0.4833$$

To find transformer secondary voltage rating

We know that,  $V_{\text{dc}} = \frac{2V_m}{\pi} - I_{\text{dc}}(r_s + r_f)$

where  $r_f$  is the diode forward resistance and  $r_s$  is the transformer secondary winding resistance.

$$55.4 = \frac{2V_m}{\pi} - 54.31 \times 10^{-3} \times 20 = \frac{2V_m}{\pi} - 1.086$$

$$56.49 = \frac{2V_m}{\pi}$$

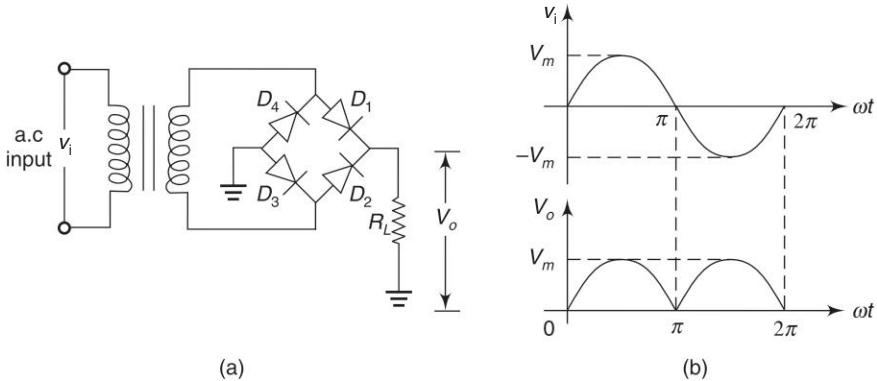
Therefore,  $V_m = 56.49 \times \frac{\pi}{2} = 88.73 \text{ V}$

$$V_{\text{rms}} = \frac{V_m}{\sqrt{2}} = \frac{88.73}{\sqrt{2}} = 62.74 \text{ V}$$

Hence, transformer secondary voltage rating is 65 V.

### 3.2.3 Bridge Rectifier

The need for a centre-tapped transformer in a full-wave rectifier is eliminated in the bridge rectifier. As shown in Fig. 3.3, the bridge rectifier has four diodes connected to form a bridge. The ac input voltage is applied to the diagonally opposite ends of the bridge. The load resistance is connected between the other two ends of the bridge.



**Fig. 3.3** Bridge rectifier

For the positive half-cycle of the input ac voltage, diodes  $D_1$  and  $D_3$  conduct, whereas diodes  $D_2$  and  $D_4$  do not conduct. The conducting diodes will be in series through the load resistance  $R_L$ . So the load current flows through  $R_L$ .

During the negative half-cycle of the input ac voltage, diodes  $D_2$  and  $D_4$  conduct, whereas diodes  $D_1$  and  $D_3$  do not conduct. The conducting diode  $D_2$  and  $D_4$  will be in series through the load  $R_L$  and the current flows through  $R_L$  in the same direction as in the previous half-cycle. Thus, a bidirectional wave is converted into an unidirectional one.

The average values of output voltage and load current for bridge rectifier are the same as for a centre-tapped full-wave rectifier. Hence,

$$V_{dc} = \frac{2V_m}{\pi} \quad \text{and} \quad I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi}$$

If the values of the transformer secondary winding resistance ( $r_s$ ) and diode forward resistance ( $r_f$ ) are considered in the analysis, then

$$V_{dc} = \frac{2V_m}{\pi} - I_{dc} (r_s + r_f)$$

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi(r_s + r_f + R_L)}$$

The maximum efficiency of a bridge rectifier is 81.2% and the ripple factor is 0.48. The PIV is  $V_m$ .

- **Advantages of the Bridge Rectifier** In the bridge rectifier, the ripple factor and efficiency of the rectification are the same as for the full-wave rectifier. The PIV across either of the non-conducting diodes is equal to the peak value of the transformer secondary voltage,  $V_m$ . The bulky centre-tapped transformer is

not required. Transformer utilization factor is considerably high. Since the current flowing in the transformer secondary is purely alternating, the TUF increases to 0.812, which is the main reason for the popularity of a bridge rectifier. The bridge rectifiers are used in applications allowing floating output terminals, i.e., no output terminal is grounded.

The bridge rectifier has only one disadvantage that it requires four diodes as compared to two diodes for centre-tapped full-wave rectifier. But the diodes are readily available at cheaper rate in the market. Apart from this, the PIV rating required for the diodes in a bridge rectifier is only half of that for a centre tapped full-wave rectifier. This is a great advantage, which offsets the disadvantage of using extra two diodes in a bridge rectifier.

**Comparison of Rectifiers** The comparison of rectifiers is given in Table 3.1.

**Table 3.1** A comparison of rectifiers

Particulars	Type of rectifier		
	Half-wave	Full-wave	Bridge
No. of diodes	1	2	4
Maximum efficiency	40.6%	81.2%	81.2%
$V_{dc}$ (no load)	$V_m/\pi$	$2V_m/\pi$	$2V_m/\pi$
Average current/diode	$I_{dc}$	$I_{dc}/2$	$I_{dc}/2$
Ripple factor	1.21	0.48	0.48
Peak inverse voltage	$V_m$	$2V_m$	$V_m$
Output frequency	$f$	$2f$	$2f$
Transformer utilisation factor	0.287	0.693	0.812
Form factor	1.57	1.11	1.11
Peak factor	2	$\sqrt{2}$	$\sqrt{2}$

### EXAMPLE 3.15

A 230 V, 50 Hz voltage is applied to the primary of a 4:1 step-down transformer used in a bridge rectifier having a load resistance of  $600\ \Omega$ . Assuming the diodes to be ideal, determine (a) dc output voltage, (b) dc power delivered to the load, (c) PIV, and (d) output frequency.

#### Solution

- (a) The rms value of the transformer secondary voltage,

$$V_{rms\ (secondary)} = \frac{V_{rms\ (primary)}}{\text{Turns ratio}} = \frac{230}{4} = 57.5$$

The maximum value of the secondary voltage

$$V_m = \sqrt{2} \times 57.5 = 81.3\ \text{V}$$

Therefore, dc output voltage,

$$V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 81.3}{\pi} = 52 \text{ V}$$

(b) The dc power delivered to the load,

$$P_{dc} = \frac{V_{dc}^2}{R_L} = \frac{52^2}{600} = 2.704 \text{ W}$$

(c) PIV across each diode =  $V_m = 81.3 \text{ V}$

(d) Output frequency =  $2 \times 50 = 100 \text{ Hz}$

### EXAMPLE 3.16

In a bridge rectifier, the transformer is connected to 200 V, 60 Hz mains and the turns ratio of the step down transformer is 11:1. Assuming the diode is ideal, find (a)  $V_{dc}$  (b)  $I_{dc}$  and (c) PIV.

**Solution** Given in a bridge rectifier, input voltage = 200 V, 60 Hz and turns ratio = 11:1

(a) To find the voltage across load,  $V_{dc}$

$$V_{dc} = \frac{2V_m}{\pi}$$

where

$$V_m = \sqrt{2} V_{rms(\text{secondary})}$$

$$V_{rms(\text{secondary})} = \frac{V_{rms(\text{primary})}}{\text{Turns ratio}} = \frac{200}{11} = 18.18 \text{ V}$$

Therefore,  $V_m = 18.18 \times \sqrt{2} = 25.7 \text{ V}$

$$\text{Hence, } V_{dc} = \frac{2 \times 25.7}{\pi} = 16.36 \text{ V}$$

(b) To find  $I_{dc}$

Assuming that  $R_L = 600 \Omega$ , then

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{16.36}{600} = 27.26 \text{ mA}$$

(c) To find PIV

$$PIV = V_m = 25.7 \text{ V}$$

### EXAMPLE 3.17

A bridge rectifier uses four identical diodes having forward resistance of  $5 \Omega$  and the secondary voltage is 30 V(rms). Determine the dc output voltage for  $I_{dc} = 200 \text{ mA}$  and value of the output ripple voltage.

**Solution** Given, transformer secondary resistance =  $5 \Omega$

Secondary voltage  $V_{rms} = 30 \text{ V}$ ,  $I_{dc} = 200 \text{ mA}$

Since only two diodes of the bridge rectifier circuit will conduct during positive or negative half cycle of the input signal, the diode forward resistance,  $r_f = 2 \times 5 \Omega = 10 \Omega$ .

We know that,

$$V_{dc} = \frac{2V_m}{\pi} - I_{dc} (r_f + r_s) \text{ where } V_m = \sqrt{2}V_{rms} = \sqrt{2} \times 30 \text{ V}$$

Therefore,  $V_{dc} = \frac{2 \times \sqrt{2} \times 30}{\pi} - 200 \times 10^{-3} (10 + 5) = 24 \text{ V}$

$$\text{Ripple factor} = \frac{\text{rms value of ripple at the output}}{\text{average value of output voltage}}$$

Therefore,  $0.48 = \frac{\text{rms value of ripple at the output}}{24}$

Hence, rms value of ripple at the output  $= 0.48 \times 24 = 11.52 \text{ V}$

### EXAMPLE 3.18

In a full-wave rectifier, the required dc voltage is 9 V and the diode drop is 0.8 V. Calculate ac rms input voltage required in centre-tapped full-wave rectifier and bridge rectifier circuits.

**Solution** (a) The dc voltage across the load of the center tapped full-wave rectifier circuit,

$$V_{dc} = 9 = \frac{2V_m}{\pi} - 0.8 = \frac{2\sqrt{2} \times V_{rms}}{\pi} - 0.8$$

where  $V_{rms}$  is the rms input voltage from centre tapping to on end. That is,

$$9.8 = \frac{2\sqrt{2} V_{rms}}{\pi}$$

Therefore,  $V_{rms} = \frac{9.8 \pi}{2\sqrt{2}} = 10.885 \text{ V}$

Hence, the voltage across the two ends of the secondary  $= 2 \times 10.885 = 21.77 \text{ V}$

(b) In the bridge rectifier,  $V_{dc} = 9 = \frac{2\sqrt{2}V_{rms}}{\pi} - 2 \times 0.8$

Therefore, the voltage across two ends of secondary,  $V_{rms} = \frac{10.6 \pi}{2\sqrt{2}} = 11.77 \text{ V}$

### 3.3 HARMONIC COMPONENTS IN A RECTIFIER CIRCUIT

The term *harmonic* is defined as “a sinusoidal component of a periodic waveform or quantity possessing a frequency, which is an integral multiple of the fundamental frequency.” By definition, a perfect sine wave has no harmonics, except fundamental component at one frequency. Harmonics are present in waveforms that are not perfect sine waves due to distortion from nonlinear loads. The French mathematician Fourier discovered that a distorted waveform can be represented as a series of sine waves, with each being an integer multiple of the fundamental frequency and each with a specific magnitude.

That is, the harmonic frequencies are integer multiples [2, 3, 4,...] of the fundamental frequency. For example, the second harmonic on a 50 Hz system is  $2 \times 50$  or 100 Hz. The sixth harmonic in a 50 Hz system, or the fifth harmonic in a 60 Hz system is 300 Hz. There are a number of different types of equipment that may experience faulty operations or failures due to high harmonic voltage and/or current levels. The amount of the harmonic voltage and current levels that a system can tolerate is dependent on the equipment and the source.

The sum of the fundamental and all the harmonics is called the ***Fourier series***. This series can be viewed as a spectrum analysis where the fundamental frequency and the harmonic component are identified.

The result of such an analysis for the current waveform of a half-wave rectifier circuit using a single diode is given by

$$i = I_m \left[ \frac{1}{\pi} + \frac{1}{2} \sin \omega t - \frac{2}{\pi} \sum_{k=2,4,6} \frac{\cos k\omega t}{(k+1)(k-1)} \right]$$

The angular frequency of the power supply is the lowest angular frequency present in the above expression. All the other terms are the even harmonics of the power frequency.

The full-wave rectifier consists of two half-wave rectifier circuits, arranged in such a way that one circuit conducts during one half cycle and the second circuit operates during the second half cycle. Therefore, the currents are functionally related by the expression  $i_1(\alpha) = i_2(\alpha + \pi)$ . Thus, the total current of the full-wave rectifier is  $i = i_1 + i_2$  as expressed by

$$i = I_m \left[ \frac{2}{\pi} - \frac{4}{\pi} \sum_{\substack{k=\text{even} \\ k \neq 0}} \frac{\cos k\omega t}{(k+1)(k-1)} \right]$$

From the above equation, it can be seen that the fundamental angular frequency is eliminated and the lowest frequency is the second harmonic term  $2\omega$ . This is the advantage that the full-wave rectifier presents in filtering of the output. Additionally, the current pulses in the two halves of the transformer winding are in such directions that the magnetic cycles formed through the iron core is essentially that of the alternating current. This avoids any dc saturation of the transformer core that could give rise to additional harmonics at the output.

### 3.4 FILTERS

---

The output of a rectifier contains dc component as well as ac component. Filters are used to minimise the undesirable ac, i.e., ripple leaving only the dc component to appear at the output.

The ripple in the rectified wave being very high, the factor being 48% in the full-wave rectifier; majority of the applications which cannot tolerate this, will need an output which has been further processed.

Figure 3.4 shows the concept of a filter, where the full-wave rectified output voltage is applied at its input. The output of a filter is not exactly a constant dc level. But it also contains a small amount of ac component. Some important filters are

- (i) Inductor filter
- (ii) Capacitor filter
- (iii) LC or L-section filter
- (iv) CLC or  $\pi$ -type filter

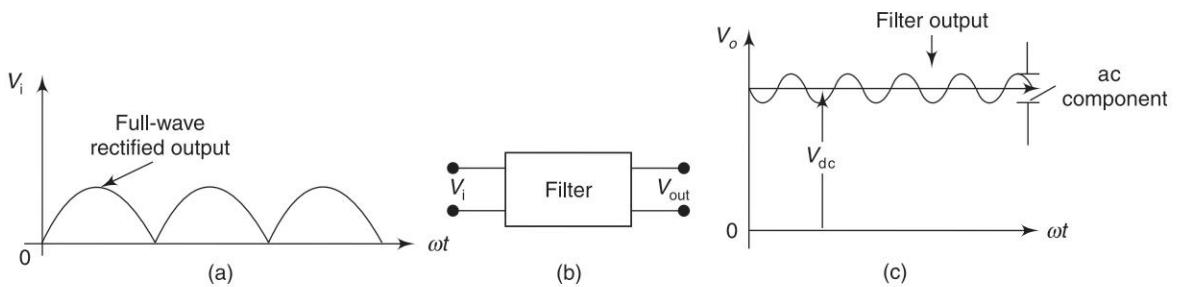


Fig. 3.4 Concept of a filter

### 3.5 INDUCTOR FILTER

Figure 3.5 shows the inductor filter. When the output of the rectifier passes through an inductor, it blocks the ac component and allows only the dc component to reach the load.

The ripple factor of the inductor filter is given by

$$\Gamma = \frac{R_L}{3\sqrt{2} \omega L}$$

It shows that the ripple factor will decrease when \$L\$ is increased and \$R\_L\$ is decreased. Clearly, the inductor filter is more effective only when the load current is high (small \$R\_L\$). The larger value of the inductor can reduce the ripple and at the same time the output dc voltage will be lowered as the inductor has a higher dc resistance.

The operation of the inductor filter depends on its well known fundamental property to oppose any change of current passing through it.

To analyse this filter for a full-wave, the Fourier series can be written as

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{\pi} \left[ \frac{1}{3} \cos 2\omega t + \frac{1}{15} \cos 4\omega t + \frac{1}{35} \cos 6\omega t + \dots \right]$$

The dc component is  $\frac{2V_m}{\pi}$ .

Assuming the third and higher terms contribute little output, the output voltage is

$$V_o = \frac{2V_m}{2\pi} - \frac{4V_m}{3\pi} \cos 2\omega t$$

The diode, choke and transformer resistances can be neglected since they are very small as compared with \$R\_L\$. Therefore, the dc component of current \$I\_m = \frac{V\_m}{R\_L}\$. The impedance of series combination of \$L\$ and \$R\_L\$ at \$2\omega\$ is

$$Z = \sqrt{R_L^2 + (2\omega L)^2} = \sqrt{R_L^2 + 4\omega^2 L^2}$$

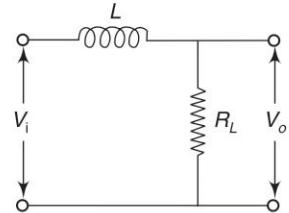


Fig. 3.5 Inductor filter

Therefore, for the ac component,

$$I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}}$$

Therefore, the resulting current  $i$  is given by,

$$i = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi} \frac{\cos(2\omega t - \varphi)}{\sqrt{R_L^2 + 4\omega^2 L^2}}$$

where  $\varphi = \tan^{-1}\left(\frac{2\omega L}{R_L}\right)$ .

The ripple factor, which can be defined as the ratio of the rms value of the ripple to the dc value of the wave, is

$$\Gamma = \frac{\frac{4V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}}}{\frac{2V_m}{\pi R_L}} = \frac{2}{3\sqrt{2}} \cdot \frac{1}{\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

If  $\frac{4\omega^2 L^2}{R_L^2} \gg 1$ , then a simplified expression for  $\Gamma$  is

$$\Gamma = \frac{R_L}{3\sqrt{2}\omega L}$$

In case, the load resistance is infinity, i.e., the output is an open circuit, then the ripple factor is

$$\Gamma = \frac{2}{3\sqrt{2}} = 0.471$$

This is slightly less than the value of 0.482. The difference being attributable to the omission of higher harmonics as mentioned. It is clear that the inductor filter should only be used where  $R_L$  is consistently small.

### EXAMPLE 3.19

Calculate the value of inductance to use in the inductor filter connected to a full-wave rectifier operating at 60 Hz to provide a dc output with 4% ripple for a  $100\Omega$  load.

**Solution**

We know that the ripple factor for inductor filter is  $\Gamma = \frac{R_L}{3\sqrt{2}\omega L}$

Therefore,

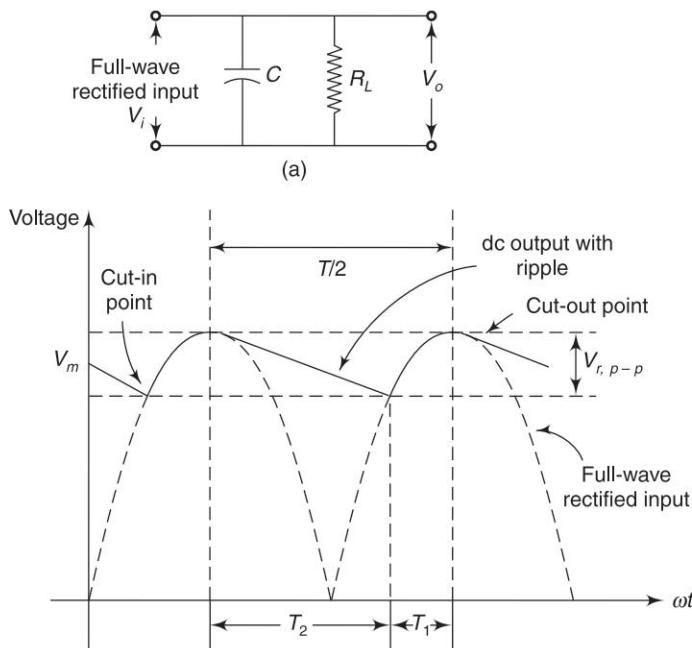
$$0.04 = \frac{100}{3\sqrt{2}(2\pi \times 60 \times L)} = \frac{0.0625}{L}$$

$$L = \frac{0.0625}{0.04} = 1.5625 \text{ H}$$

### 3.6 CAPACITOR FILTER

An inexpensive filter for light loads is found in the capacitor filter which is connected directly across the load, as shown in Fig. 3.6(a). The property of a capacitor is that it allows ac component and blocks the dc component. The operation of a capacitor filter is to short the ripple to ground but leave the dc to appear at the output when it is connected across a pulsating dc voltage.

During the positive half-cycle, the capacitor charges up to the peak value of the transformer secondary voltage,  $V_m$ , and will try to maintain this value as the full-wave input drops to zero. The capacitor will discharge through  $R_L$  slowly until the transformer secondary voltage again increases to a value greater than the capacitor voltage (equal to the load voltage). The diode conducts for a period which depends on the capacitor voltage. The diode will conduct when the transformer secondary voltage becomes more than the 'cut-in' voltage of the diode. The diode stops conducting when the transformer voltage becomes less than the diode voltage. This is called cut-out voltage.



**Fig. 3.6** (a) Capacitor filter (b) Ripple voltage triangular waveform

Referring to Fig. 3.6(b) with slight approximation, the ripple voltage waveform can be assumed as triangular. From the cut-in point to the cut-out point, whatever charge the capacitor acquires is equal to the charge the capacitor has lost during the period of non-conduction, i.e., from cut-out point to the next cut-in point.

The charge it has acquired =  $V_{r, p-p} \times C$

The charge it has lost =  $I_{dc} \times T_2$

Therefore,  $V_{r, p-p} \times C = I_{dc} \times T_2$

If the value of the capacitor is fairly large, or the value of the load resistance is very large, then it can be assumed that the time  $T_2$  is equal to half the periodic time of the waveform,

i.e.,

$$T_2 = \frac{T}{2} = \frac{1}{2f}, \text{ then } V_{r,p-p} = \frac{I_{dc}}{2fC}$$

With the assumptions made above, the ripple waveform will be triangular in nature and the rms value of the ripple is given by

$$V_{r,\text{rms}} = \frac{V_{r,p-p}}{2\sqrt{3}}$$

Therefore, from the above equation, we have

$$\begin{aligned} V_{r,\text{rms}} &= \frac{I_{dc}}{4\sqrt{3} fC} \\ &= \frac{V_{dc}}{4\sqrt{3} fCR_L}, \text{ since } I_{dc} = \frac{V_{dc}}{R_L} \end{aligned}$$

$$\text{Therefore, ripple factor } \Gamma = \frac{V_{r,\text{rms}}}{V_{dc}} = \frac{1}{4\sqrt{3} fCR_L}$$

The ripple may be decreased by increasing  $C$  or  $R_L$  (or both) with a resulting increase in dc output voltage.

$$\text{If } f = 50 \text{ Hz, } C \text{ in } \mu\text{F} \text{ and } R_L \text{ in } \Omega, \Gamma = \frac{2890}{CR_L}.$$

### EXAMPLE 3.20

Calculate the value of capacitance to use in a capacitor filter connected to a full-wave rectifier operating at a standard aircraft power frequency of 400 Hz, if the ripple factor is 10% for a load of  $500 \Omega$ .

**Solution** We know that the ripple factor for capacitor filter is

$$\Gamma = \frac{1}{4\sqrt{3} fCR_L}$$

$$\text{Therefore, } 0.01 = \frac{1}{4\sqrt{3} \times 400 \times C \times 500} = \frac{0.722 \times 10^{-6}}{C}$$

$$C = \frac{0.722 \times 10^{-6}}{0.01} = 72.2 \mu\text{F}$$

### EXAMPLE 3.21

A 15-0-15 volt (rms) 50 Hz ideal transformer is used with a full-wave rectifier circuit with diodes having forward drop of 1 volt. The load is a resistance of  $100 \Omega$  and a capacitor of  $10,000 \mu\text{F}$  is used as a filter across the load resistance. Calculate the dc load current and voltage.

**Solution** Given transformer secondary voltage = 15-0-15 V (rms);

Diode forward drop = 1 V;  $R_L = 100 \Omega$ ;  $C = 10,000 \mu\text{F}$

$$\text{We know that, } V_{dc} = V_m - \frac{V_{r,p-p}}{2} = V_m - \frac{I_{dc}}{4fC}$$

Therefore,

$$V_{dc} = V_m - \frac{V_{dc}}{R_L 4fC}, \left[ \text{since } I_{dc} = \frac{V_{dc}}{R_L} \right]$$

Simplifying, we get

$$V_{dc} = \left[ \frac{4f R_L C}{4f R_L C + 1} \right] V_m$$

We know that

$$V_m = V_{rms} \times \sqrt{2} = 15 \times \sqrt{2}$$

Therefore,

$$V_{dc} = \left[ \frac{4 \times 50 \times 100 \times 10000 \times 10^{-6}}{4 \times 50 \times 100 \times 10000 \times 10^{-6} + 1} \right] \times 15 \times \sqrt{2} = 21.105 \text{ V}$$

Considering the given voltage drop of 1 volt due to diodes,

$$V_{dc} = 21.105 - 1 = 20.105 \text{ V}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.105}{100} = 0.20105 \text{ A}$$

### EXAMPLE 3.22

A full-wave rectified voltage of 18 V peak is applied across a 500  $\mu\text{F}$  filter capacitor. Calculate the ripple and dc voltages if the load takes a current of 100 mA.

#### Solution

Given

$$V_m = 18 \text{ V}, C = 500 \mu\text{F} \text{ and } I_{dc} = 100 \text{ mA}$$

$$V_{dc} = V_m - \frac{I_{dc}}{4fC} = 18 - \frac{100 \times 10^{-3}}{4 \times 50 \times 500 \times 10^{-6}} = 17 \text{ V}$$

$$V_{r,rms} = \frac{I_{dc}}{4\sqrt{3}fC} = \frac{100 \times 10^{-3}}{4\sqrt{3} \times 50 \times 500 \times 10^{-6}} = 0.577 \text{ V}$$

Therefore, ripple,

$$\Gamma = \frac{V_{r,rms}}{V_{dc}} = \frac{0.577}{17} \times 100 = 3.39\%$$

### EXAMPLE 3.23

A bridge rectifier with capacitor filter is fed from 220 V to 40 V step down transformer. If average dc current in load is 1 A and capacitor filter of 800  $\mu\text{F}$ , calculate the load regulation and ripple factor. Assume power line frequency of 50 Hz. Neglect diode forward resistance and dc resistance of secondary of transformer.

#### Solution

$$V_{rms(\text{secondary})} = 40 \text{ V}, I_{dc} = 1 \text{ A}, C = 800 \mu\text{F}, \text{ and } f = 50 \text{ Hz}$$

$$V_m = \sqrt{2} V_{rms} = \sqrt{2} \times 40 = 56.5685 \text{ V}$$

$$V_{dc(FL)} = V_m - \frac{I_{dc}}{4fC} = 56.5685 - \frac{1}{4 \times 50 \times 800 \times 10^{-6}} = 50.3185 \text{ V}$$

On no load,

$$I_{dc} = 0$$

Hence,

$$V_{dc(NL)} = V_m = 56.5685 \text{ V}$$

Therefore, percentage of regulation =  $\frac{V_{dc(NL)} - V_{dc(NL)}}{I_{dc(NL)}} \times 100$

$$= \frac{56.5685 - 50.3185}{50.1385} \times 100 = 12.42\%$$

$$R_L = \frac{V_{dc}}{I_{dc}} = \frac{50.1385}{1} = 50.1385 \Omega$$

$$\Gamma = \frac{1}{4\sqrt{3} f C R_L} = \frac{1}{4\sqrt{3} \times 50 \times 800 \times 10^{-6} \times 50.1385} = 0.0717, \text{ i.e., } 7.17\%$$

### 3.7 L-SECTION FILTER (LC FILTER)

We know that the ripple factor is directly proportional to the load resistance  $R_L$  in the inductor filter and inversely proportional to  $R_L$  in the capacitor filter. Therefore, if these two filters are combined as LC filter or L-section filter as shown in Fig. 3.7, the ripple factor will be independent of  $R_L$ .

If the value of the inductance is increased, it will increase the time of conduction. At some critical value of inductance, one diode, either  $D_1$  or  $D_2$  in full-wave rectifier, will always be conducting.

From Fourier series, the output voltage can be expressed as

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi} \cos 2\omega t$$

$$\text{The dc output voltage, } V_{dc} = \frac{2V_m}{\pi}$$

$$\text{Therefore, } I_{rms} = \frac{4V_m}{3\pi\sqrt{2}} \cdot \frac{1}{X_L} = \frac{\sqrt{2}}{3} \cdot \frac{V_{dc}}{X_L}$$

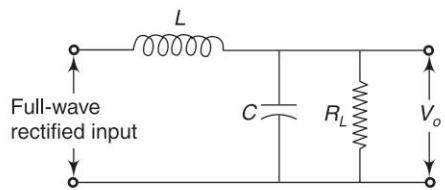


Fig. 3.7 LC filter

This current flowing through  $X_C$  creates the ripple voltage ( $V_{r, rms}$ ) in the output.

$$\text{Therefore, } V_{r, rms} = I_{rms} \cdot X_C = \frac{\sqrt{2}}{3} \cdot V_{dc} \cdot \frac{X_C}{X_L}$$

$$\begin{aligned} \text{The ripple factor, } \Gamma &= \frac{V_{r, rms}}{V_{dc}} = \frac{\sqrt{2}}{3} \cdot \frac{X_C}{X_L} \\ &= \frac{\sqrt{2}}{3} \cdot \frac{1}{4\omega^2 C_L}, \text{ since } X_C = \frac{1}{2\omega C} \text{ and } X_L = 2\omega L \end{aligned}$$

If  $f = 50 \text{ Hz}$ ,  $C$  is in  $\mu\text{F}$  and  $L$  is in Henry, ripple factor  $\Gamma = \frac{1.194}{LC}$ .

**Bleeder Resistor** It was assumed in the analysis given above that for a critical value of inductor, either of the diodes is always conducting, i.e., current does not fall to zero. The incoming current consists of two components:

(i)  $I_{dc} = \frac{V_{dc}}{R_L}$ , and (ii) a sinusoidal varying components with peak value of  $\frac{4V_m}{3\pi X_L}$ . The negative peak of the

ac current must always be less than dc, i.e.,  $\sqrt{2} I_{rms} \leq \frac{V_{dc}}{R_L}$ .

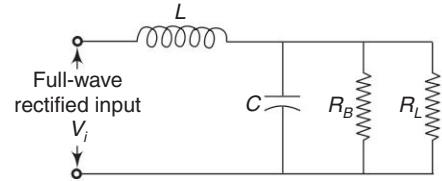
We know that for  $LC$  filter,  $I_{rms} = \frac{\sqrt{2}}{3} \times \frac{V_{dc}}{X_L}$

Hence,  $\frac{2V_{dc}}{X_L} \leq \frac{V_{dc}}{R_L}$ , i.e.,  $X_L \geq \frac{2}{3} R_L$

i.e.,  $L_C = \frac{R_L}{2\omega}$ , where  $L_C$  is the critical inductance.

It should be noted that the condition  $X_L \geq \frac{2}{3} R_L$  cannot be satisfied for all load requirements. At no load, i.e.,

when the load resistance is infinity, the value of the inductance will also tend to be infinity. To overcome this problem, a bleeder resistor  $R_B$  is connected in parallel with the load resistance as shown in Fig. 3.8. Therefore, a minimum current will always be present for optimum operation of the inductor. It improves voltage regulation of the supply by acting as the pre-load on the supply. Also, it provides safety by acting as a discharging path for capacitor.



**Fig. 3.8** Bleeder resistor connected at the filter output

### EXAMPLE 3.24

Design a filter for full-wave circuit with  $LC$  filter to provide an output voltage of 10 V with a load current of 200 mA and the ripple is limited to 2%.

**Solution** The effective load resistance,  $R_L = \frac{10}{200 \times 10^{-3}} = 50 \Omega$

We know that the ripple factor,

$$\Gamma = \frac{1.194}{LC}$$

i.e.,  $0.02 = \frac{1.194}{LC}$

i.e.,  $LC = \frac{1.194}{0.02} = 59.7$

Critical value of  $L = \frac{R_L}{3\omega} = \frac{50}{3 \times 2\pi f} = 53 \text{ mH}$

Taking  $L = 60 \text{ mH}$  (about 20% higher),  $C$  will be about  $1000 \mu\text{F}$ .

**EXAMPLE 3.25**

A full-wave rectifier (FWR) supplies a load requiring 300 V at 200 mA. Calculate the transformer secondary voltage for (a) a capacitor input filter using a capacitor of 10 mF, and (b) a choke input filter using a choke of 10 H and a capacitance of 10  $\mu\text{F}$ . Neglect the resistance of choke.

**Solution** Given  $V_{dc} = 300 \text{ V}$ ;  $I_{dc} = 200 \text{ mA}$

(a) For the capacitor filter with  $C = 10 \mu\text{F}$ ,

$$V_{dc} = V_m - \frac{I_{dc}}{4fC}$$

$$300 = V_m - \frac{200 \times 10^{-3}}{4(50)(10 \times 10^{-6})} = V_m - 100$$

Therefore,

$$V_m = 400 \text{ V}_{(p-p)}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = 282.84 \text{ V}$$

(b) For the choke, i.e., LC filter with  $L = 10 \text{ H}$ ;  $C = 10 \mu\text{F}$

$$V_{dc} = \frac{2V_m}{\pi}$$

$$300 = \frac{2V_m}{\pi}$$

Therefore,

$$V_m = 471.23 \text{ V}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = 333.21 \text{ V}$$

**EXAMPLE 3.26**

Determine the ripple factor of a L-type choke input filter comprising a 10 H choke and 8  $\mu\text{F}$  capacitor used with a FWR. Compare with a simple 8  $\mu\text{F}$  capacitor input filter at a load current of 50 mA and also at 150 mA. Assume the dc voltage of 50 V.

**Solution**  $V_{dc} = 50 \text{ V}$ ,  $L = 10 \text{ H}$ ,  $C = 8 \mu\text{F}$

Assume  $f = 50 \text{ Hz}$ , i.e.,  $\omega = 2\pi f = 100\pi \text{ rad/sec}$ .

For LC filter, the ripple factor is

$$\Gamma = \frac{1}{6\sqrt{2}\omega^2 LC} = \frac{1}{6\sqrt{2} \times (100\pi)^2 \times 10 \times 8 \times 10^{-6}} = 0.01492 \text{ i.e., } 1.492\%$$

For the simple capacitor filter,  $C = 8 \mu\text{F}$ .

(a) At  $I_L = 50 \text{ mA}$ ,

$$R_L = \frac{V_{dc}}{I_L} = \frac{50}{50 \times 10^{-3}} = 1000 \Omega$$

$$\Gamma = \frac{1}{4\sqrt{3}fCR_L} = \frac{1}{4\sqrt{3} \times 50 \times 8 \times 10^{-6} \times 1000} = 0.3608, \text{ i.e., } 36.08\%$$

(b) At  $I_L = 150 \text{ mA}$ ,

$$R_L = \frac{V_{dc}}{I_L} = \frac{50}{150 \times 10^{-3}} = 333.33 \Omega$$

$$\Gamma = \frac{1}{4\sqrt{3}fCR_L} = \frac{1}{4\sqrt{3} \times 50 \times 8 \times 10^{-6} \times 333.33} = 1.082, \text{ i.e., } 108.2\%$$

Thus, it is inferred that the  $LC$  choke input filter is more effective than capacitor input filter and the ripple factor of  $LC$  choke input filter does not depend on the load resistance.

### EXAMPLE 3.27

In a full-wave rectifier using an  $LC$  filter,  $L = 10 \text{ H}$ ,  $C = 100 \mu\text{F}$ , and  $R_L = 500 \Omega$ . Calculate  $I_{dc}$ ,  $V_{dc}$ , and ripple factor for an input of  $v_i = 30 \sin(100\pi t) \text{ V}$ .

**Solution** Comparing the input with  $v_i = V_m \sin \omega t$

$$V_m (\text{secondary}) = V_m = 30 \text{ V}$$

$$V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 30}{\pi} = 19.0985 \text{ V}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{19.0985}{500} = 0.03819 \text{ A} = 38.19 \text{ mA}$$

$$\begin{aligned} \text{Ripple factor} &= \frac{1}{6\sqrt{2}\omega^2 LC} \\ &= \frac{1}{6\sqrt{2} \times (100\pi)^2 \times 10 \times 100 \times 10^{-6}} = 1.194 \times 10^{-3} \end{aligned}$$

## 3.8 $\pi$ -SECTION FILTER

Figure 3.9 shows the CLC or  $\pi$ -type filter which basically consists of a capacitor filter followed by an LC section. This filter provided a fairly smooth output, and is characterized by a highly peaked diode currents and poor regulation.

The action of a  $\pi$ -section filter can best be understood by considering the inductor and the second capacitor as an L-section filter that acts upon the triangular output-voltage wave from the first capacitor. The output voltage is then approximately that from the input capacitor, decreased by the dc voltage drop in the inductor. The ripple contained in this output is reduced by the L-section filter.

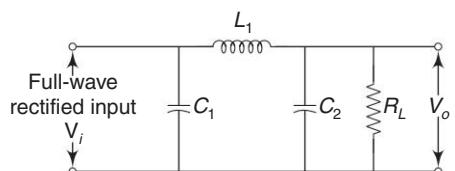


Fig. 3.9 CLC or  $\pi$ -type filter

The ripple voltage can be calculated by analyzing the triangular wave into a Fourier series and then multiplying each component by  $X_{C2}/X_{L1}$  for this harmonic. The Fourier analysis of this waveform is given by

$$v = V_{dc} - \frac{V_r}{\pi} \left( \sin 2\omega t - \frac{\sin 2\omega t}{2} + \frac{\sin 6\omega t}{3} - \dots \right)$$

We know that

$$V_r = \frac{I_{dc}}{2fC_1}$$

The rms second-harmonic voltage is

$$V_{rms} = V'_2 = \frac{V_r}{\pi\sqrt{2}} = \frac{I_{dc}}{2\pi fC_1\sqrt{2}} = \sqrt{2}I_{dc}X_{C1}$$

where  $X_{C1}$  is the reactance of  $C_1$  at the second-harmonic frequency.

The voltage  $V'_2$  is impressed on an L-section, and the output ripple is  $V'_2 X_{C2}/X_{L1}$ .

Hence, the ripple factor is

$$\Gamma = \frac{V_{rms}}{V_{dc}} = \frac{\sqrt{2} I_{dc} X_{C1} X_{C2}}{V_{dc} X_{L1}} = \sqrt{2} \frac{X_{C1} X_{C2}}{R_L X_{L1}}$$

where all reactance are calculated at the second-harmonic frequency.

For  $f = 60$  Hz, the above equation reduces to

$$\Gamma = \frac{3,300}{C_1 C_2 L_1 R_L}$$

## 3.9 MULTIPLE L-SECTION AND MULTIPLE $\pi$ -SECTION FILTER

### 3.9.1 Multiple L-section Filter

The filtering level can be improved by using two or more L-section filters in series, as shown in Fig. 3.10. It is assumed that the reactance of all the inductances are much larger than the reactance of the capacitors and the reactance of the last capacitor is small compared with the resistance of the load. Under these conditions, the impedance between 3 and 3' is  $X_{C2}$ , the impedance between 2 and 2' is  $X_{C1}$ , and the impedance between 1 and 1' is  $X_{L1}$ . The alternating current  $I_1$  through  $L_1$  is, given by

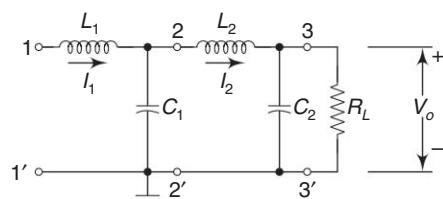
$$I_1 = \frac{\sqrt{2} V_{dc}}{3} \frac{1}{X_{L1}}$$

The ac voltage across  $C_1$  is given by

$$V_{22'} = I_1 X_{C1}$$

The alternating current  $I_2$  through  $L_2$  is given by

$$I_2 = \frac{V_{22'}}{X_{L2}}$$



**Fig. 3.10** A multiple (two-section) L-section filter

The ac voltage across  $C_2$  and hence, across the load is given by

$$V_{33'} = I_2 X_{C2} = I_1 \frac{X_{C2} X_{C1}}{X_{L2}} = \frac{\sqrt{2} V_{\text{d.c.}}}{3} \frac{X_{C2} X_{C1}}{X_{L2} X_{L1}}$$

The ripple factor is obtained by dividing the above equation by  $V_{\text{d.c.}}$ . Hence,

$$\Gamma = \frac{\sqrt{2}}{3} \frac{X_{C1} X_{C2}}{X_{L1} X_{L2}}$$

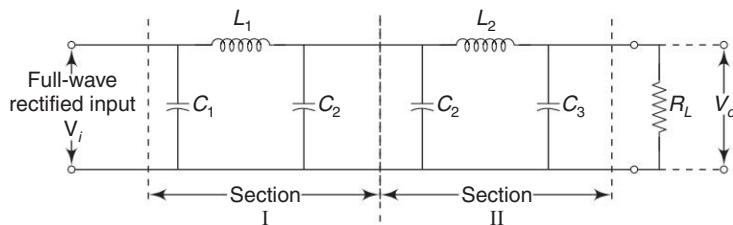
The generalized expression for any number of sections can be obtained by comparing the above equation with that of a single L-section. For example, the ripple factor of a multiple L-section filter ( $\Gamma_n$ ) is given by

$$\Gamma_n = \frac{\sqrt{2}}{3} \left( \frac{X_C}{X_L} \right)^n = \frac{\sqrt{2}}{3} \frac{1}{(16\pi^2 f^2 LC)^n}$$

where  $n$  is the number of similar  $L$ -sections.

### 3.9.1 Multiple $\pi$ -section Filter

In order to obtain pure dc at the output, more number of  $\pi$ -sections may be used in series. Such a filter using more than one  $\pi$ -section, as shown in Fig. 3.11, is called a multiple  $\pi$ -section filter.



**Fig. 3.11** Multiple  $\pi$ -section filter

The ripple factor for multiple  $\pi$ -section filter is given by

$$\Gamma = \frac{X_{C1}}{R_L} \cdot \frac{X_{C2}}{X_{L1}} \cdot \frac{X_{C3}}{X_{L2}} \cdots \frac{X_{Cn}}{X_{L(n-1)}}$$

where  $n$  is the number of  $\pi$ -sections.

#### EXAMPLE 3.28

Design a CLC or  $\pi$ -section filter for  $V_{\text{d.c.}} = 10$  V,  $I_L = 200$  mA, and  $\Gamma = 2\%$ .

#### Solution

$$R_L = \frac{10}{200 \times 10^{-3}} = 50 \Omega$$

$$0.02 = \frac{5700}{LC_1 C_2 \times 50} = \frac{114}{LC_1 C_2}$$

If we assume  $L = 10 \text{ H}$  and  $C_1 = C_2 = C$ , we have

$$0.02 = \frac{114}{LC^2} = \frac{11.4}{C^2}$$

$$C^2 = 570; \text{ therefore, } C = \sqrt{570} \approx 24 \mu\text{F}$$

### EXAMPLE 3.29

A full-wave single-phase rectifier employs a  $\pi$ -section filter consisting of two  $4 \mu\text{F}$  capacitances and a  $20 \text{ H}$  choke. The transformer voltage to the centre tap is  $300 \text{ V rms}$ . The load current is  $500 \text{ mA}$ . Calculate the dc output voltage and the ripple voltage. The resistance of the choke is  $200 \Omega$ .

#### Solution

$$C_1 = C_2 = 4 \mu\text{F}, L = 20 \text{ H}$$

$$I_{dc} = 500 \text{ mA}, R_x = 200 \Omega$$

Maximum value of secondary voltage,

$$V_{s(\max)} = \sqrt{2} \times 300 = 424.2 \text{ V}$$

$$R_L = \frac{V_{dc}}{I_{dc}} = \frac{270.19}{500 \times 10^{-3}} = 540 \Omega$$

$$V_{dc} = V_{s(\max)} - \frac{V_r}{2} - I_{dc}R_x$$

$$\text{Ripple voltage, } V_r = \frac{I_{dc}}{2fC} = \frac{500 \times 10^{-3}}{2 \times 50 \times 4 \times 10^{-6}} = 1.25 \text{ mV}$$

$$\text{The dc output voltage, } V_{dc} = 424.2 - \frac{1.25 \times 10^{-3}}{2} - (500 \times 10^{-3} \times 200) = 324.19 \text{ V}$$

**R-C Filters** Consider the  $CLC$  filter with the inductor  $L$  replaced by a resistor  $R$ . This type of filter called  $RC$  filter is shown in Fig. 3.12. The expression for the ripple factor can be obtained by replacing  $X_L$  by  $R$ . Then,

$$\Gamma = \sqrt{2} \frac{X_{C1}}{R_L} \cdot \frac{X_{C2}}{R}$$

Therefore, if resistor  $R$  is chosen equal to the reactance of the inductor which it replaces, the ripple remains unchanged.

The resistance  $R$  will increase the voltage drop and hence, the regulation will be poor. This type of filters are often used for economic reasons, as well as the space and weight requirement of the iron-cored choke for the  $LC$  filter. Such  $RC$  filters are often used only for low current power supplies.

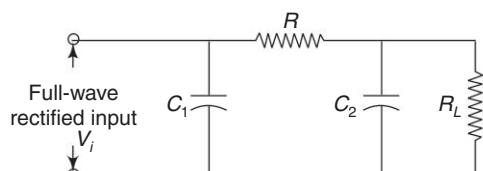


Fig. 3.12 R-C filter

### 3.10 COMPARISON OF VARIOUS FILTER CIRCUITS

Table 3.2 shows the comparison of various types of filters, when used with full-wave circuits. In all these filters, the resistances of diodes, transformer and filter elements are considered negligible and a 60 Hz power line is assumed.

**Table 3.2** Comparison of various types of filters

Particulars	Type of Filter				
	None	L	C	L-Section	$\pi$ -Section
$V_{dc}$ at no load	$0.636 V_m$	$0.636 V_m$	$V_m$	$V_m$	$V_m$
$V_{dc}$ at load $I_{dc}$	$0.636 V_m$	$0.636 V_m$	$V_m - \frac{4170 I_{dc}}{C}$	$0.636 V_m$	$V_m - \frac{4170 I_{dc}}{C}$
Ripple factor $\Gamma$	0.48	$\frac{R_L}{16000 L}$	$\frac{2410}{CR_L}$	$\frac{0.83}{LC}$	$\frac{3330}{LC_1 C_2 R_L}$
Peak inverse voltage (PIV)	$2 V_m$	$2 V_m$	$2 V_m$	$2 V_m$	$2 V_m$

### REVIEW QUESTIONS

- What is a rectifier?
  - Show that a PN diode works as rectifier.
  - Define the following terms:
    - ripple factor
    - peak inverse voltage
    - efficiency
    - transformer utilization factor
    - form factor
    - peak factor.
  - Draw the circuit diagram of an half-wave rectifier, and explain its operation.
  - Derive expressions for rectification efficiency, ripple factor, transformer utilization factor, form factor, and peak factor of an half-wave rectifier with resistive load.
  - A half-wave rectifier has a load of  $3.5 \text{ k}\Omega$ . If the diode resistance and secondary coil resistance together have a resistance of  $800 \Omega$  and the input voltage has a signal voltage of peak value 240 V, calculate
    - Peak, average and rms value of current flowing
    - dc power output
    - ac power input
    - Efficiency of the rectifier
- [Ans. (i) 55.81 mA, 17.78 mA and 27.9 mA (ii) 1.1 W (iii) 3.35 W (iv) 32.9%]
- Explain the action of a full-wave rectifier and give waveforms of input and output voltages.
  - Derive expressions of dc or average value of voltage and rms value of voltage of a full-wave rectifier with resistive load.
  - Derive an expression for a ripple factor in a full-wave rectifier with resistive load.
  - Determine the value of ripple factor in the full-wave rectifier operating at 50 Hz with a  $100 \mu\text{F}$  capacitor filter and  $100 \Omega$  load.
 

[Ans. 29%]
  - Show that a full-wave rectifier is twice as efficient as a half-wave rectifier.
  - Describe the action of a full-wave bridge rectifier.
  - What are the advantages of a bridge rectifier?

14. Compare half-wave, full-wave and bridge rectifiers.
15. What is the need for filters in power supplies?
16. Explain the various types of filters used in power supplies.
17. Obtain the ripple factor of a full-wave rectifier with shunt capacitor filter.
18. Derive an expression for the ripple factor in a full-wave rectifier using inductor filter.
19. Compare the performance of inductive, L-section and  $\pi$ -section filters.
20. An  $L-C$  filter is to be used to provide a dc output with 1% ripple from a full-wave rectifier operating at 50 Hz. Assuming  $L/C = 0.01$ , determine the required values of  $L$  and  $C$ . [Ans. 1.093 H, 109.27  $\mu\text{F}$ ]
21. In a full-wave rectifier using an  $L-C$  filter, it is known that  $L = 10 \text{ H}$ ,  $C = 100 \mu\text{F}$ , and  $R_L = 500 \Omega$ . Calculate  $I_{dc}$ ,  $V_{dc}$ ,  $I_{ac}$ ,  $V_{ac}$  if  $V_m = 30 \text{ V}$  and  $f = 50 \text{ Hz}$ . [Ans. 38.2 mA, 19.1 V, 1.43 mA, 22.7 mV]
22. The turns ratio of the transformer used in a half-wave rectifier is 2:1 and the primary is connected to 230 V, 50 Hz power mains. Assuming the diodes to be ideal, determine (i) dc voltage across the load, (ii) PIV of each diode, and (iii) medium and average values of power delivered to the load having a resistance of  $200 \Omega$ . Also find the efficiency of the rectifier and output ripple frequency. [Ans. 51.7 V, 162.2 V, 132.2 W, 13.5 W, 10.21%, 50 Hz]
23. In a full-wave rectifier, the voltage applied to each diode is  $240 \sin 377t$ , the load resistance is  $R_L = 2000 \Omega$  and each diode has a forward resistance of  $400 \Omega$ . Determine the (i) peak value of current, (ii) dc value of current, (iii) rms value of current, (iv) rectifier efficiency, (v) ripple factor, and (vi) output ripple frequency. [Ans. 100 mA, 63.8 mA, 70.7 mA, 67.6%, 0.482, 120 Hz]
24. In a bridge rectifier, the transformer is connected to 220 V, 60 Hz mains and the turns ratio of the step down transformer is 11:1. Assuming the diodes to be ideal, find (i) the voltage across the load, (ii)  $I_{dc}$  and (iii) PIV. [Ans. 18 V, 18 mA, 28.28 V]
25. In a full-wave rectifier, the transformer rms secondary voltage from centre tap to each end of secondary is 50 V. The load resistance is  $900 \Omega$ . If the diode resistance and transformer secondary winding resistance together has a resistance of  $100 \Omega$ . Determine the average load current and rms value of load current. [Ans. 45 mA, 50 mA]

### OBJECTIVE-TYPE QUESTIONS

1. A rectifier is used to
 

(a) convert ac voltage to dc voltage	(b) convert dc voltage to ac voltage
(c) both ((a) and (b))	(d) convert voltage to current
2. The maximum efficiency of a half-wave rectifier is
 

(a) 40.6%	(b) 81.2%	(c) 1.12%	(d) 48.2%
-----------	-----------	-----------	-----------
3. In a full-wave rectifier, the current in each diode flows for
 

(a) whole cycle of the input signal	(b) half-cycle of the input signal
(c) more than half-cycle of the input signal	(d) none of the above
4. In a full-wave bridge rectifier, if  $V_m$  is the peak voltage across the secondary of the transformer, the maximum voltage coming across each reverse-biased diode is
 

(a) $V_m$	(b) $2V_m$	(c) $\frac{1}{2}V_m$	(d) $\frac{V_m}{\sqrt{2}}$
-----------	------------	----------------------	----------------------------
5. The rectifier efficiency is
 

(a) $\frac{P_{dc}}{P_{ac}}$	(b) $\frac{\text{rms value}}{\text{average value}}$	(c) $\frac{\text{Peak value}}{\text{rms value}}$	(d) $\sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$
-----------------------------	---	--	--
6. The major advantages of a bridge rectifier is that
 

(a) no centre-tap transformer is required
(b) the required peak inverse voltage of each diode is double that for a full-wave rectifier

- (c) peak inverse voltage of each diode is half that for a full-wave rectifier  
 (d) the output is more smooth
7. The ripple factor decreases with  
 (a) decrease in  $C$   
 (b) increase in  $C$   
 (c) increase in frequency  
 (d) decrease in frequency
8. The primary function of a rectifier filter is to  
 (a) suppress odd harmonics  
 (b) remove ripples  
 (c) stabilize the output dc level  
 (d) minimize the input ac variations
9. The diode used in voltage regulator is  
 (a) PN-junction diode  
 (b) varactor diode  
 (c) Zener diode  
 (d) GUNN diode
10. A bleeder resistor is used in a dc power supply because it  
 (a) keeps the supply OFF  
 (b) keeps the supply ON  
 (c) improves filtering action  
 (d) improves voltage regulation
11. The ripple factor of a power supply is given by  
 (a)  $\frac{P_{dc}}{P_{ac}}$   
 (b)  $\sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$   
 (c)  $\sqrt{\left(\frac{I_{dc}}{I_{rms}}\right)} - 1$   
 (d)  $\frac{I_{dc}}{I_{rms}}$
12. For constructing a full-wave rectifier,  
 (a) at least two diodes are needed  
 (b) more than two diodes are needed  
 (c) at least four diodes are needed  
 (d) none of the above
13. Ripple factor of an ideal rectifier is  
 (a) 1  
 (b) 0  
 (c) infinity  
 (d) none of the above
14. The bridge rectifier is preferable to a full-wave rectifier with centre-tap connections because it uses four diodes  
 (a) its transformer has no centre tap  
 (b) it needs much small transformer for the same output  
 (c) it has higher safety factor  
 (d) both (b) and (c)
15. In a rectifier, larger the value of shunt capacitor filter,  
 (a) larger the peak current in the rectifying diode  
 (b) smaller the dc voltage across the load  
 (c) longer the time that current pulse flows through the diode  
 (d) all of the above
16. In an LC filter, the ripple factor  
 (a) increases with the load current  
 (b) increases with the load resistance  
 (c) remains constant with the load current  
 (d) has the lowest value
17. Consider the following rectifier circuits:  
 1. Half-wave rectifier without filter  
 2. Full-wave rectifier without filter  
 3. Full-wave rectifier with series inductance filter  
 4. Full-wave rectifier with capacitance filter.  
 The sequence of these rectifier circuits in decreasing order of their ripple factor is  
 (a) 1, 2, 3, 4  
 (b) 3, 4, 1, 2  
 (c) 1, 4, 3, 2  
 (d) 3, 2, 1, 4

# Transistor Characteristics (BJT and FET)

## 4.1 INTRODUCTION

A Bipolar Junction Transistor (BJT) is a three terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers and hence the name bipolar. The BJT is analogous to a vacuum triode and is comparatively smaller in size. It is used in amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

The quiescent operating point of a transistor amplifier should be established in the active region of its characteristics. Since the transistor parameters such as  $\beta$ ,  $I_{CO}$  and  $V_{BE}$  are functions of temperature, the operating point shifts with changes in temperature. The stability of different methods of biasing transistor circuits and compensation techniques for stabilizing the operating point are discussed in this chapter.

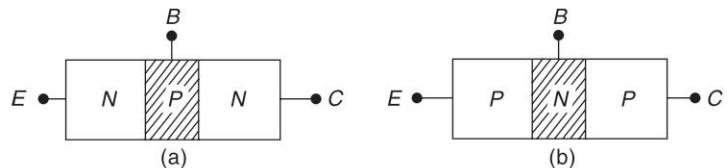
## 4.2 BIPOLAR JUNCTION TRANSISTOR

### 4.2.1 Construction

The BJT consists of a silicon (or germanium) crystal in which a thin layer of *N*-type silicon is sandwiched between two layers of *P*-type silicon. This transistor is referred to as *PNP*. Alternatively, in an *NPN* transistor, a layer of *P*-type material is sandwiched between two layers of *N*-type material. The two types of the BJT are represented in Fig. 4.1.

The symbolic representation of the two types of the BJT is shown in Fig. 4.2. The three portions of the transistor are emitter, base, and collector, shown as *E*, *B*, and *C*, respectively. The arrow on the emitter specifies the direction of current flow when the *EB* junction is forward biased.

The emitter is heavily doped so that it can inject a large number of charge carriers into the base. The base is lightly doped and very thin. It passes most of the injected charge carriers from the emitter into the collector. The collector is moderately doped.



**Fig. 4.1** Transistor: (a) NPN (b) PNP

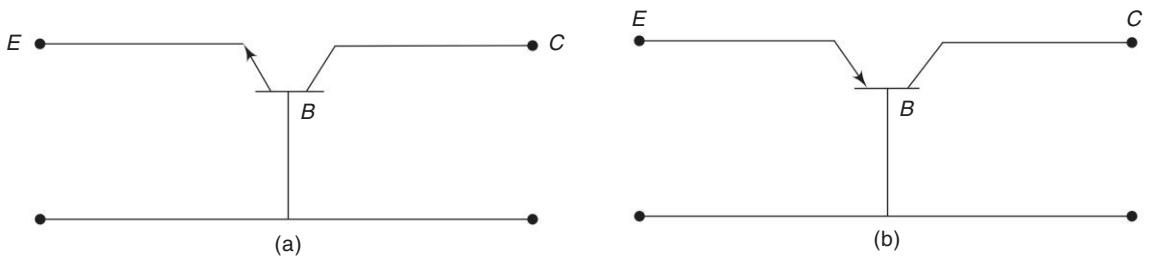


Fig. 4.2 Circuit symbol: (a) NPN transistor (b) PNP transistor

#### 4.2.2 Transistor Biasing

As shown in Fig. 4.3, usually the emitter-base junction is forward biased (F.B.) and the collector-base junction is reverse biased (R.B.). Due to the forward bias on the emitter-base junction, an emitter current flows through the base into the collector. Though the collector-base junction is reverse biased, almost the entire emitter current flows through the collector circuit.

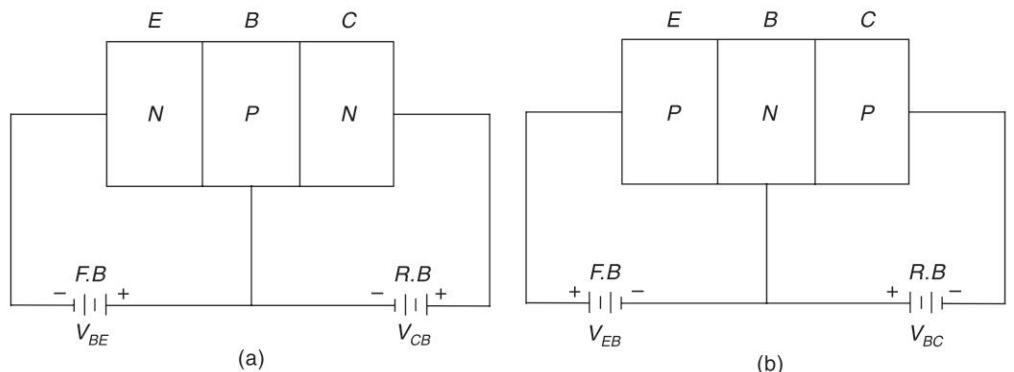


Fig. 4.3 Transistor biasing: (a) NPN transistor (b) PNP transistor

#### 4.2.3 Operation of an NPN Transistor

As shown in Fig. 4.4, the forward bias applied to the emitter-base junction of an *NPN* transistor causes a lot of electrons from the emitter region to cross over to the base region. As the base is lightly doped with *P*-type impurity, the number of holes in the base region is very small and, hence, the number of electrons that combine with holes in the *P*-type base region is also very small. Hence, a few electrons recombine with holes to constitute a base current  $I_B$ . The remaining electrons (more than 95%) cross over into the collector region to constitute a collector current  $I_C$ . Thus, the base and collector current summed up gives the emitter current, i.e.,  $I_E = -(I_C + I_B)$ .

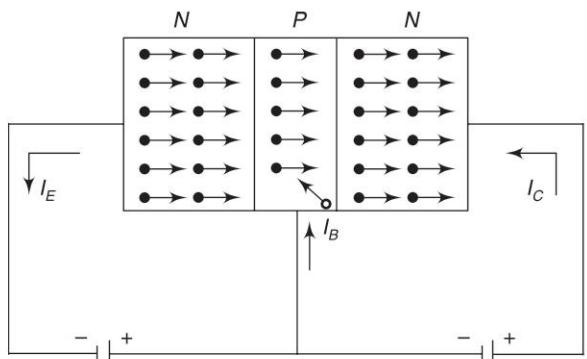


Fig. 4.4 Current in an NPN transistor

In the external circuit of the *NPN* bipolar junction transistor, the magnitudes of the emitter current  $I_E$ , the base current  $I_B$ , and the collector current  $I_C$  are related by  $I_E = I_C + I_B$ .

#### 4.2.4 Operation of a *PNP* Transistor

As shown in Fig. 4.5, the forward bias applied to the emitter-base junction of a *PNP* transistor causes a lot of holes from the emitter region to cross over to the base region as the base is lightly doped with *N*-type impurity. The number of electrons in the base region is very small and, hence, the number of holes combined with electrons in the *N*-type base region is also very small. Hence, a few holes combined with electrons to constitute a base current  $I_B$ . The remaining holes (more than 95%) cross over into the collector region to constitute a collector current  $I_C$ . Thus, the collector and base current when summed up gives the emitter current, i.e.,  $I_E = -(I_C + I_B)$ .

In the external circuit of the *PNP* bipolar junction transistor, the magnitudes of the emitter current  $I_E$ , the base current  $I_B$  and the collector current  $I_C$  are related by

$$I_E = I_C + I_B \quad (4.1)$$

This equation gives the fundamental relationship between the currents in a bipolar transistor circuit. Also, this fundamental equation shows that there are current amplification factors  $\alpha$  and  $\beta$  in common-base transistor configuration and common-emitter transistor configuration respectively for the static (dc) currents, and for small changes in the currents.

---

### 4.3 TRANSISTOR CURRENT COMPONENTS

#### 4.3.1 Current Amplification Factor

In a transistor amplifier with ac input signal, the ratio of change in output current to the change in input current is known as the current amplification factor.

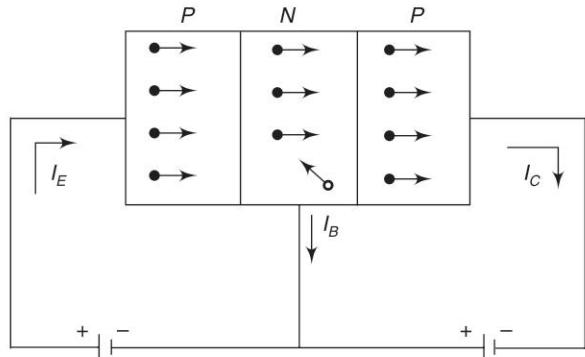
$$\text{In the CB configuration, the current amplification factor, } \alpha = \frac{\Delta I_C}{\Delta I_E} \quad (4.2)$$

$$\text{In the CE configuration, the current amplification factor, } \beta = \frac{\Delta I_C}{\Delta I_B} \quad (4.3)$$

$$\text{In the CC configuration, the current amplification factor, } \gamma = \frac{\Delta I_E}{\Delta I_B} \quad (4.4)$$

#### 4.3.2 Relationship between $\alpha$ and $\beta$

We know that  $\Delta I_E = \Delta I_C + \Delta I_B$



**Fig. 4.5** Current in a *PNP* transistor

By definition,  $\Delta I_C = \alpha \Delta I_E$

Therefore,  $\Delta I_E = \alpha \Delta I_E + \Delta I_B$

i.e.,  $\Delta I_B = \Delta I_E(1 - \alpha)$

Dividing both sides by  $\Delta I_C$ , we get

$$\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C}(1 - \alpha)$$

Therefore,  $\frac{1}{\beta} = \frac{1}{\alpha}(1 - \alpha)$

$$\beta = \frac{\alpha}{(1 - \alpha)}$$

Rearranging, we also get  $\alpha = \frac{\beta}{(1 + \beta)}$ , or  $\frac{1}{\alpha} - \frac{1}{\beta} = 1$  (4.5)

From this relationship, it is clear that as  $\alpha$  approaches unity,  $\beta$  approaches infinity. The CE configuration is used for almost all transistor applications because of its high current gain,  $\beta$ .

### 4.3.3 Relation among $\alpha$ , $\beta$ , and $\gamma$

In the CC transistor amplifier circuit,  $I_B$  is the input current and  $I_E$  is the output current.

From Eq. (4.2),  $\gamma = \frac{\Delta I_E}{\Delta I_B}$

Substituting  $\Delta I_B = \Delta I_E - \Delta I_C$ ,

$$\text{we get } \gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator on RHS by  $\Delta I_E$ , we get

$$\gamma = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1 - \alpha}$$

Therefore,  $\gamma = \frac{1}{1 - \alpha} = (\beta + 1)$  (4.6)

### 4.3.4 Large-Signal Current Gain ( $\alpha$ )

The large-signal current gain of a common-base transistor is defined as the ratio of the negative of the collector-current increment to the emitter-current change from cut-off ( $I_E = 0$ ) to  $I_E$ , i.e.,

$$\alpha = \frac{(I_C - I_{CBO})}{I_E - 0} (4.7)$$

where  $I_{CBO}$  (or  $I_{CO}$ ) is the reverse saturation current flowing through the reverse-biased collector-base junction, i.e., the collector-to-base leakage current with the emitter open. As the magnitude of  $I_{CBO}$  is negligible when compared to  $I_C$ , expression (4.7) can be written as

$$\alpha = \frac{I_C}{I_E} \quad (4.8)$$

Since  $I_C$  and  $I_E$  are flowing in opposite directions,  $\alpha$  is always positive. The typical value of  $\alpha$  ranges from 0.90 to 0.995. Also,  $\alpha$  is not a constant but varies with emitter current  $I_E$ , collector voltage  $V_{CB}$ , and temperature.

#### 4.3.5 General Transistor Equation

In the active region of the transistor, the emitter-base junction is forward biased and the collector-base junction is reverse biased. The generalized expression for collector current  $I_C$  for collector junction voltage  $V_C$  and emitter current  $I_E$  is given by

$$I_C = -\alpha I_E + I_{CBO} (1 - e^{V_C/V_T}) \quad (4.9)$$

If  $V_C$  is negative and  $|V_C|$  is very large compared with  $V_T$ , then the above equation reduces to

$$I_C = -\alpha I_E + I_{CBO} \quad (4.10)$$

If  $V_C$ , i.e.,  $V_{CB}$ , is a few volts, then  $I_C$  is independent of  $V_C$ . Hence, the collector current  $I_C$  is determined only by the fraction  $\alpha$  of the current  $I_E$  flowing in the emitter.

#### 4.3.6 Relation Among $I_C$ , $I_B$ , and $I_{CBO}$

From Eq. (4.10), we have

$$I_C = -\alpha I_E + I_{CBO}$$

Since  $I_C$  and  $I_E$  are flowing in opposite directions,

$$I_E = -(I_C + I_B)$$

Therefore,

$$I_C = -\alpha[-(I_C + I_B)] + I_{CBO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C(1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{I_{CBO}}{1 - \alpha}$$

Since

$$\beta = \frac{\alpha}{1 - \alpha} \quad (4.11)$$

the above expression becomes

$$I_C = (1 + \beta) I_{CBO} + \beta I_B \quad (4.12)$$

#### 4.3.7 Relation Among $I_C$ , $I_B$ , and $I_{CEO}$

In the common-emitter (CE) transistor circuit,  $I_B$  is the input current and  $I_C$  is the output current. If the base circuit is open, i.e.,  $I_B = 0$ , then a small collector current flows from the collector to emitter. This is denoted

as  $I_{CEO}$ , the collector-emitter current with base open. This current  $I_{CEO}$  is also called the collector-to-emitter leakage current.

In this CE configuration of the transistor, the emitter-base junction is forward-biased and collector-base junction is reverse-biased and, hence, the collector current  $I_C$  is the sum of the part of the emitter current  $I_E$  that reaches the collector, and the collector-emitter leakage current  $I_{CEO}$ . Therefore, the part of  $I_E$ , which reaches collector is equal to  $(I_C - I_{CEO})$ .

Hence, the *large-signal current gain* ( $\beta$ ) is defined as,

$$\beta = \frac{(I_C - I_{CEO})}{I_B} \quad (4.13)$$

From the equation, we have

$$I_C = \beta I_B + I_{CEO} \quad (4.14)$$

### 4.3.8 Relation Between $I_{CBO}$ and $I_{CEO}$

Comparing Eqs (4.12) and (4.14), we get the relationship between the leakage currents of transistor common-base (CB) and common-emitter (CE) configurations as

$$I_{CEO} = (1 + \beta) I_{CBO} \quad (4.15)$$

From this equation, it is evident that the collector-emitter leakage current ( $I_{CEO}$ ) in CE configuration is  $(1 + \beta)$  times larger than that in CB configuration. As  $I_{CBO}$  is temperature-dependent,  $I_{CEO}$  varies by large amount when temperature of the junctions changes.

- **Expression for Emitter Current** The magnitude of emitter current is

$$I_E = I_C + I_B$$

Substituting Eq. (4.12) in the above equation, we get

$$I_E = (1 + \beta) I_{CBO} + (1 + \beta) I_B \quad (4.16)$$

Substituting Eq. (4.11) into Eq. (4.16), we have

$$I_E = \frac{1}{1 - \alpha} I_{CBO} + \frac{1}{1 - \alpha} I_B \quad (4.17)$$

### 4.3.9 dc Current Gain ( $\beta_{dc}$ or $h_{FE}$ )

The dc current gain is defined as the ratio of the collector current  $I_C$  to the base current  $I_B$ . That is,

$$\beta_{dc} = h_{FE} = \frac{I_C}{I_B} \quad (4.18)$$

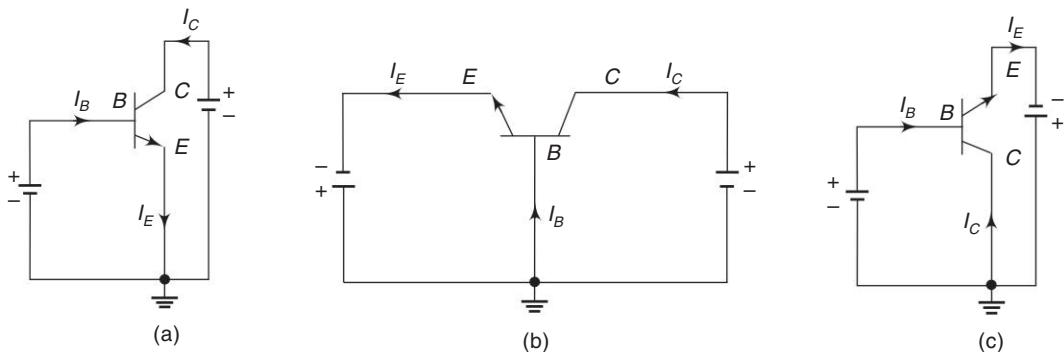
As  $I_C$  is large compared with  $I_{CEO}$ , the large-signal current gain ( $\beta$ ) and the dc current gain ( $h_{FE}$ ) are approximately equal.

## 4.4 TRANSISTOR CONFIGURATIONS (CE, CB AND CC CHARACTERISTICS)

When a transistor is to be connected in a circuit, one terminal is used as an input terminal, the other terminal is used as an output terminal, and the third terminal is common to the input and output. Depending upon the input, output, and common terminals, a transistor can be connected in three configurations. They are (i) Common Base (CB) configuration, (ii) Common Emitter (CE) configuration, and (iii) Common Collector (CC) configuration.

- **CB Configuration** This is also called *grounded-base configuration*. In this configuration, the emitter is the input terminal, the collector is the output terminal, and the base is the common terminal.
- **CE Configuration** This is also called *grounded-emitter configuration*. In this configuration, the base is the input terminal, the collector is the output terminal, and the emitter is the common terminal.
- **CC Configuration** This is also called *grounded-collector configuration*. In this configuration, the base is the input terminal, the emitter is the output terminal, and the collector is the common terminal.

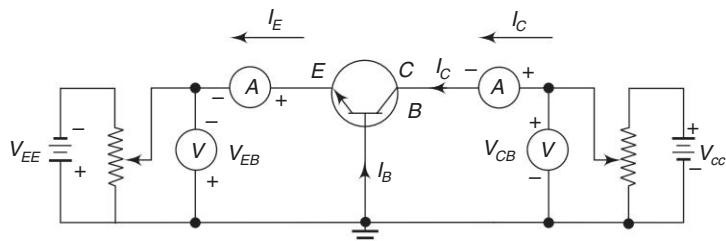
The supply voltage connections for normal operation of an *NPN* transistor in the three configurations are shown in Fig. 4.6.



**Fig. 4.6** Transistor configuration: (a) Common emitter (b) Common base (c) Common collector

### 4.4.1 CB Configuration

The circuit diagram for determining the static characteristics curves of an *NPN* transistor in the common-base configuration is shown in Fig. 4.7.



**Fig. 4.7** Circuit to determine CB static characteristics

**Input Characteristics** To determine the input characteristics, the collector-base voltage  $V_{CB}$  is kept constant at zero volt and the emitter current  $I_E$  is increased from zero in suitable equal steps by increasing  $V_{EB}$ . This is repeated for higher fixed values of  $V_{CB}$ . A curve is drawn between emitter current  $I_E$  and emitter-base voltage  $V_{EB}$  at constant collector-base voltage  $V_{CB}$ . The input characteristics thus obtained are shown in Fig. 4.8.

When  $V_{CB}$  is equal to zero and the emitter-base junction is forward biased as shown in the characteristics, the junction behaves as a forward-biased diode so that emitter current  $I_E$  increases rapidly with small increase in emitter-base voltage  $V_{EB}$ . When  $V_{CB}$  is increased keeping  $V_{EB}$  constant, the width of the base region will decrease. This effect results in an increase of  $I_E$ . Therefore, the curves shift towards the left as  $V_{CB}$  is increased.

**Output Characteristics** To determine the output characteristics, the emitter current  $I_E$  is kept constant at a suitable value by adjusting the emitter-base voltage  $V_{EB}$ . Then  $V_{CB}$  is increased in suitable equal steps and the collector current  $I_C$  is noted for each value of  $I_E$ . This is repeated for different fixed values of  $I_E$ . Now the curves of  $I_C$  versus  $V_{CB}$  are plotted for constant values of  $I_E$  and the output characteristics thus obtained is shown in Fig. 4.9.

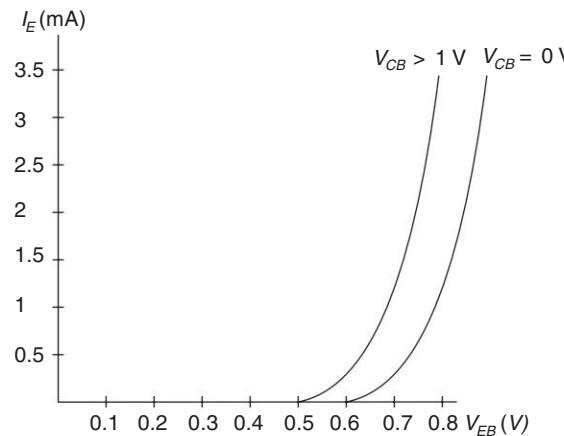


Fig. 4.8 CB input characteristics

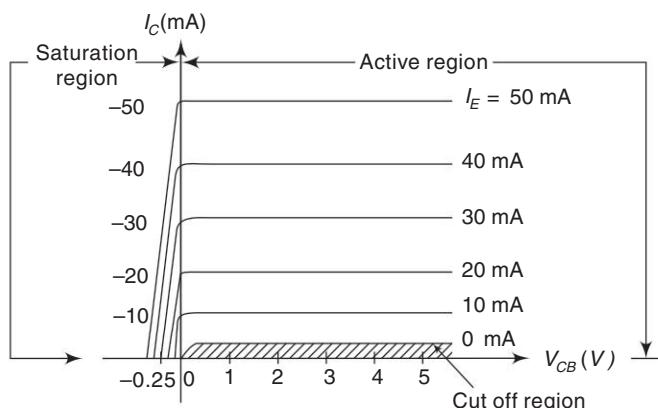


Fig. 4.9 CB output characteristics

From the characteristics, it is seen that for a constant value of  $I_E$ ,  $I_C$  is independent of  $V_{CB}$  and the curves are parallel to the axis of  $V_{CB}$ . Further,  $I_C$  flows even when  $V_{CB}$  is equal to zero. As the emitter-base junction is forward biased, the majority carriers, i.e., electrons, from the emitter are injected into the base region. Due to the action of the internal potential barrier at the reverse-biased collector-base junction, they flow to the collector region and give rise to  $I_C$  even when  $V_{CB}$  is equal to zero.

**Early Effect or Base Width Modulation** As the collector voltage  $V_{CC}$  is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base width on collector-to-base voltage is known as the *Early effect*. This decrease in effective base width has three consequences:

- (i) There is less chance for recombination within the base region. Hence,  $\alpha$  increases with increasing  $|V_{CB}|$ .
- (ii) The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.
- (iii) For extremely large voltages, the effective base width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the *punch-through*.

For higher values of  $V_{CB}$ , due to Early effect, the value of  $\alpha$  increases. For example,  $\alpha$  changes, say from 0.98 to 0.985. Hence, there is a very small positive slope in the CB output characteristics and, hence, the output resistance is not zero.

### Transistor Parameters

The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common-base *hybrid parameters* or *h-parameters*.

- **Input Impedance ( $h_{ib}$ )** It is defined as the ratio of the change in (input) emitter voltage to the change in (input) emitter current with the (output) collector voltage  $V_{CB}$  kept constant. Therefore,

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, V_{CB} \text{ constant} \quad (4.19)$$

It is the slope of CB input characteristics  $I_E$  versus  $V_{EB}$  as shown in Fig. 4.8. The typical value of  $h_{ib}$  ranges from  $20 \Omega$  to  $50 \Omega$ .

- **Output Admittance ( $h_{ob}$ )** It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) emitter current  $I_E$  kept constant. Therefore,

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, I_E \text{ constant} \quad (4.20)$$

It is the slope of CB output characteristics  $I_C$  versus  $V_{CB}$  as shown in Fig. 4.9. The typical value of this parameter is of the order of 0.1 to  $10 \mu$  mhos.

- **Forward Current Gain ( $h_{fb}$ )** It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage  $V_{CB}$  constant. Hence,

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, V_{CB} \text{ constant} \quad (4.21)$$

It is the slope of  $I_C$  versus  $I_E$  curve. Its typical value varies from 0.9 to 1.0.

- **Reverse Voltage Gain ( $h_{rb}$ )** It is defined as the ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current,  $I_E$ . Hence,

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, I_E \text{ constant} \quad (4.22)$$

It is the slope of  $V_{EB}$  versus  $V_{CB}$  curve. Its typical value is of the order of  $10^{-5}$  to  $10^{-4}$ .

#### 4.4.2 CE Configuration

**Input Characteristics** To determine the input characteristics, the collector-to-emitter voltage is kept constant at zero volt, and the base current is increased from zero in equal steps by increasing  $V_{BE}$  in the circuit shown in Fig. 4.10.

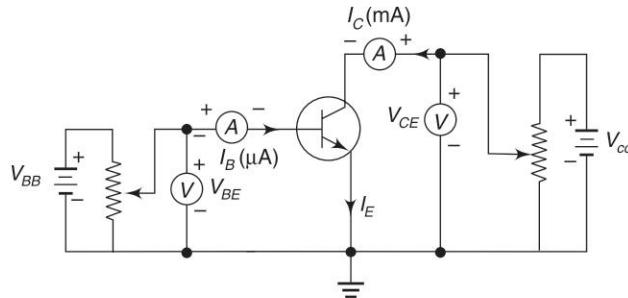


Fig. 4.10 Circuit to determine CE static characteristics

The value of  $V_{BE}$  is noted for each setting of  $I_B$ . This procedure is repeated for higher fixed values of  $V_{CE}$ , and the curves of  $I_B$  versus  $V_{BE}$  are drawn. The input characteristics thus obtained are shown in Fig. 4.11.

When  $V_{CE} = 0$ , the emitter-base junction is forward biased and the junction behaves as a forward biased diode. Hence, the input characteristic for  $V_{CE} = 0$  is similar to that of a forward-biased diode. When  $V_{CE}$  is increased, the width of the depletion region at the reverse-biased collector-base junction will increase. Hence, the effective width of the base will decrease. This effect causes a decrease in the base current  $I_B$ . Hence, to get the same value of  $I_B$  as that for  $V_{CE} = 0$ ,  $V_{BE}$  should be increased. Therefore, the curve shifts to the right as  $V_{CE}$  increases.

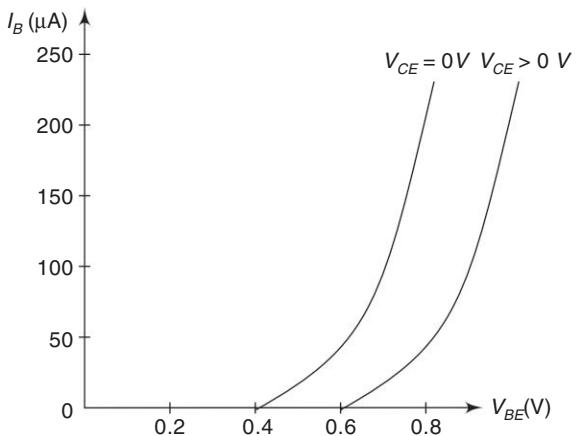


Fig. 4.11 CE input characteristics

**Output Characteristics** To determine the output characteristics, the base current  $I_B$  is kept constant at a suitable value by adjusting the base-emitter voltage,  $V_{BE}$ . The magnitude of the collector-emitter voltage  $V_{CE}$  is increased in suitable equal steps from zero and the collector current  $I_C$  is noted for each setting  $V_{CE}$ . Now, the curves of  $I_C$  versus  $V_{CE}$  are plotted for different constant values of  $I_B$ . The output characteristics thus obtained are shown in Fig. 4.12.

From Eqs. (4.11) and (4.12), we have

$$\beta = \frac{\alpha}{1 - \alpha} \quad \text{and} \quad I_C = (1 + \beta) I_{CBO} + \beta I_B$$

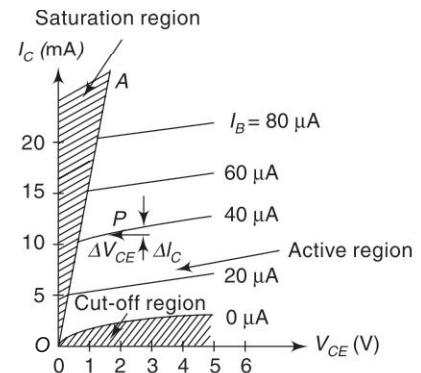


Fig. 4.12 CE output characteristics

For larger values of  $V_{CE}$ , due to Early effect, a very small change in  $\alpha$  is reflected as a very large change in  $\beta$ .

For example, when  $\alpha = 0.98$ ,  $\beta = \frac{0.98}{1 - 0.98} = 49$ . If  $\alpha$  increases to 0.985, then  $\beta = \frac{0.985}{1 - 0.985} = 66$ . Here, a slight increase in  $\alpha$  by about 0.5% results in an increase in  $\beta$  by about 34%. Hence, the output characteristics of CE configuration show a larger slope when compared with CB configuration.

The output characteristics have three regions, namely, saturation region, cut-off region, and active region. The region of curves to the left of the line  $OA$  is called the *saturation region* (hatched), and the line  $OA$  is called the saturation line. In this region, both junctions are forward biased and an increase in the base current does not cause a corresponding large change in  $I_C$ . The ratio of  $V_{CE(\text{sat})}$  to  $I_C$  in this region is called saturation resistance.

The region below the curve for  $I_B = 0$  is called the *cut-off region* (hatched). In this region, both junctions are reverse biased. When the operating point for the transistor enters the cut-off region, the transistor is OFF. Hence, the collector current becomes almost zero and the collector voltage almost equals  $V_{CC}$ , the collector-supply voltage. The transistor is virtually an open circuit between collector and emitter.

The central region where the curves are uniform in spacing and slope is called the *active region* (unhatched). In this region, emitter-base junction is forward biased and the collector-base junction is reverse biased. If the transistor is to be used as a linear amplifier, it should be operated in the active region.

If the base current is subsequently driven large and positive, the transistor switches into the saturation region via the active region, which is traversed at a rate that is dependent on factors such as gain and frequency response. In this ON condition, large collector current flows and collector voltage falls to a very low value, called  $V_{CE\text{sat}}$ , typically around 0.2 V for a silicon transistor. The transistor is virtually a short circuit in this state.

High-speed switching circuits are designed in such a way that transistors are not allowed to saturate, thus reducing switching times between ON and OFF times.

### Transistor Parameters

The slope of the CE characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common-emitter *hybrid parameters* or *h-parameters*.

- **Input Impedance ( $h_{ie}$ )** It is defined as the ratio of the change in (input) base voltage to the change in (input) base current with the (output) collector voltage  $V_{CE}$  kept constant. Therefore,

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}, V_{CE} \text{ constant} \quad (4.23)$$

It is the slope of CE input characteristics  $I_B$  versus  $V_{BE}$  as shown in Fig. 4.11. The typical value of  $h_{ie}$  ranges from 500 to 2,000  $\Omega$ .

- **Output Admittance ( $h_{oe}$ )** It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) base current  $I_B$  kept constant. Therefore,

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, I_B \text{ constant} \quad (4.24)$$

It is the slope of CE output characteristic  $I_C$  versus  $V_{CE}$  as shown in Fig. 4.12. The typical value of this parameter is of the order of 0.1 to 10  $\mu$  mhos.

- **Forward Current Gain ( $h_{fe}$ )** It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) base current keeping the (output) collector voltage  $V_{CE}$  constant. Hence,

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, V_{CE} \text{ constant} \quad (4.25)$$

It is the slope of  $I_C$  versus  $I_B$  curve. Its typical value varies from 20 to 200.

- **Reverse Voltage Gain ( $h_{re}$ )** It is defined as the ratio of the change in the (input) base voltage and the corresponding change in (output) collector voltage with constant (input) base current,  $I_B$ . Hence,

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, I_B \text{ constant} \quad (4.26)$$

It is the slope of  $V_{BE}$  versus  $V_{CE}$  curve. Its typical value is of the order of  $10^{-5}$  to  $10^{-4}$ .

### **Derivation of analytical expression for CE output characteristics of BJT**

We know that, for a PNP transistor, the collector-emitter voltage  $V_{CE}$  is given by

$$V_{CE} = V_C - V_E$$

$$\text{where } V_C = V_T \ln \left( 1 - \frac{\alpha_N I_E + I_C}{I_{CO}} \right) \text{ and } V_E = V_T \ln \left( 1 - \frac{\alpha_I I_C + I_E}{I_{EO}} \right).$$

Here,  $\alpha_N$  is the current gain when the transistor is in the normal operation and  $\alpha_I$  is the current gain when the transistor is in the inverted operation.

Therefore,

$$\begin{aligned} V_{CE} &= V_T \ln \left( 1 - \frac{\alpha_N I_E + I_C}{I_{CO}} \right) - V_T \ln \left( 1 - \frac{\alpha_I I_C + I_E}{I_{EO}} \right) \\ &= V_T \ln \left( \frac{I_{CO} - \alpha_N I_E - I_C}{I_{CO}} \right) - V_T \ln \left( \frac{I_{EO} - \alpha_I I_C - I_E}{I_{EO}} \right) \\ &= V_T \ln \left( \frac{I_{CO} - \alpha_N I_E - I_C}{I_{EO} - \alpha_I I_C - I_E} \right) \left( \frac{I_{EO}}{I_{CO}} \right) \end{aligned}$$

We know that,

$$I_E = -(I_B + I_C)$$

Hence,

$$\begin{aligned} V_{CE} &= V_T \ln \left( \frac{I_{CO} + \alpha_N I_B + \alpha_N I_C - I_C}{I_{EO} - \alpha_I I_C + I_B + I_C} \right) \left( \frac{\alpha_I}{\alpha_N} \right) \quad \left( \text{since } \frac{I_{EO}}{I_{CO}} = \frac{\alpha_I}{\alpha_N} \right) \\ &= V_T \ln \left( \frac{I_{CO} + \alpha_N I_B + (\alpha_N - 1) I_C}{I_{EO} + I_B + (1 - \alpha_I) I_C} \right) \left( \frac{\alpha_I}{\alpha_N} \right) \\ &= V_T \ln \frac{\alpha_I}{\alpha_N} + V_T \ln \left( \frac{I_{CO} + \alpha_N I_B - I_C(1 - \alpha_N)}{I_{EO} + I_B + I_C(1 - \alpha_I)} \right) \end{aligned}$$

If  $I_B \gg I_{EO}$  and  $I_B \gg \frac{I_{CO}}{\alpha_N}$ , we have

$$\begin{aligned} V_{CE} &= V_T \ln \left[ \left( \frac{\alpha_I}{\alpha_N} \right) \left( \frac{\alpha_N I_B - I_C (1 - \alpha_N)}{I_B + I_C (1 - \alpha_I)} \right) \right] \\ &= V_T \ln \left[ \frac{I_B - \left( \frac{1 - \alpha_N}{\alpha_N} \right) I_C}{\frac{I_B}{\alpha_I} + \left( \frac{1 - \alpha_I}{\alpha_I} \right) I_C} \right] \end{aligned}$$

Now dividing both numerator and denominator by  $I_B$ , we get

$$\begin{aligned} V_{CE} &= V_T \ln \left[ \frac{1 - \left( \frac{1 - \alpha_N}{\alpha_N} \right) \frac{I_C}{I_B}}{\frac{1}{\alpha_I} + \left( \frac{1 - \alpha_I}{\alpha_I} \right) \frac{I_C}{I_B}} \right] \\ &= V_T \ln \left[ \frac{1 - \frac{1}{\beta_N} \frac{I_C}{I_B}}{\frac{1}{\alpha_I} + \frac{1}{\beta_I} \frac{I_C}{I_B}} \right] \quad \left( \text{since } \beta = \frac{\alpha}{1 - \alpha} \right) \end{aligned}$$

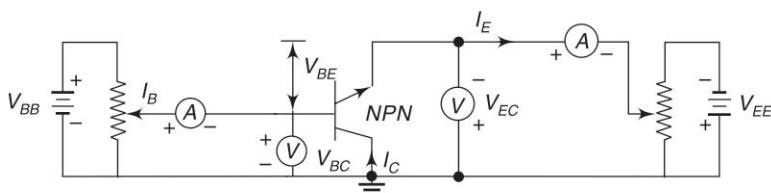
or

$$V_{CE} = -V_T \ln \left[ \frac{\frac{1}{\alpha_I} + \frac{1}{\beta_I} \frac{I_C}{I_B}}{1 - \frac{1}{\beta_N} \frac{I_C}{I_B}} \right]$$

Here, if  $I_C = 0$ ,  $V_{CE} = -V_T \ln \left( \frac{1}{\alpha_I} \right)$ . This shows that  $V_{CE}$  is not equal to zero even if  $I_C$  becomes zero and hence, the common emitter characteristic curves do not pass through the origin.

#### 4.4.3 CC Configuration

The circuit diagram for determining the static characteristics of an *NPN* transistor in the common collector configuration is shown in Fig. 4.13.



**Fig. 4.13** Circuit to determine CC static characteristics

**Input Characteristics** To determine the input characteristics,  $V_{EC}$  is kept at a suitable fixed value. The base-collector voltage  $V_{BC}$  is increased in equal steps and the corresponding increase in  $I_B$  is noted. This is repeated for different fixed values of  $V_{EC}$ . Plots of  $V_{BC}$  versus  $I_B$  for different values of  $V_{EC}$  shown in Fig. 4.14 are the input characteristics.

**Output Characteristics** To determine the output characteristics, the base current,  $I_B$ , is kept constant at a suitable value by adjusting the base-collector voltage,  $V_{BC}$ . The magnitude of the emitter-collector voltage,  $V_{EC}$ , is increased in suitable equal steps from zero and the emitter current,  $I_E$ , is noted for each setting  $V_{EC}$ . Now, the curves of  $I_E$  versus  $V_{EC}$  are plotted for different constant values of  $I_B$ . The output characteristics thus obtained are shown in Fig. 4.15. These output characteristics are the same as those of the common emitter configuration.

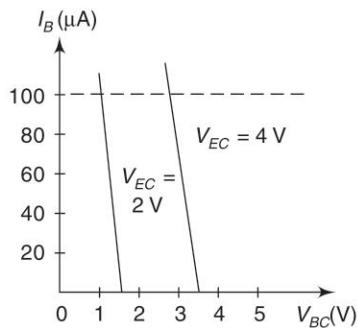


Fig. 4.14 CC input characteristics

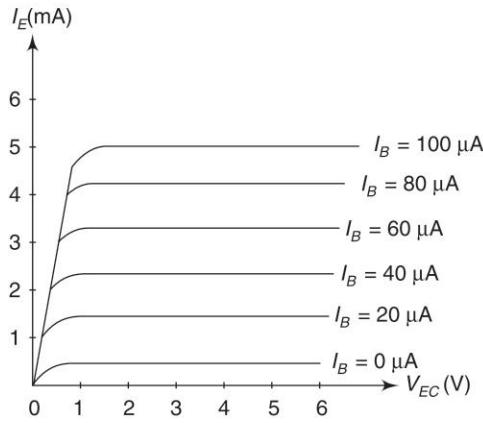


Fig. 4.15 CC output characteristics

#### 4.4.4 Comparison of Different Configurations

A comparison of different configurations is given in Table 4.1.

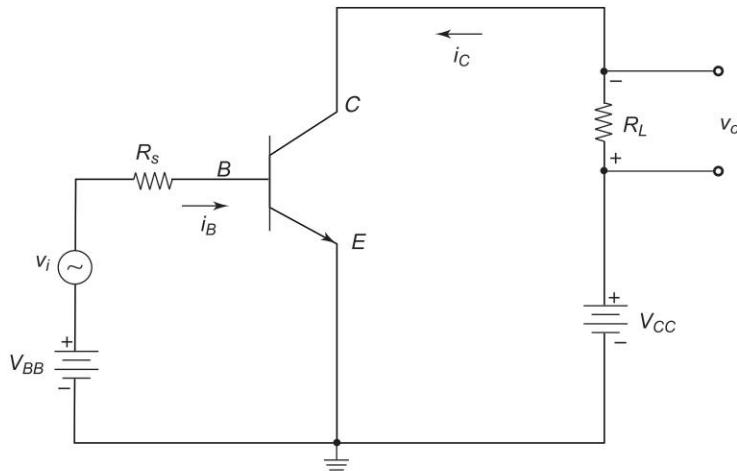
Table 4.1 A comparison of CB, CE, and CC configurations

Property	CB	CE	CC
Input resistance	Low (about $100 \Omega$ )	Moderate (about $750 \Omega$ )	High (about $750 \text{ k}\Omega$ )
Output resistance	High (about $450 \text{ k}\Omega$ )	Moderate (about $45 \text{ k}\Omega$ )	Low (about $25 \Omega$ )
Current gain	1	High	High
Voltage gain	About 150	About 500	Less than 1
Phase shift between input and output voltages	0 or $360^\circ$	$180^\circ$	0 or $360^\circ$
Applications	for high frequency circuits	for audio frequency circuits	for impedance matching

## 4.5 TRANSISTOR AS AN AMPLIFIER

**CE Transistor as an Amplifier** Figure 4.16(a) shows an amplifier circuit using CE transistor configuration. In this circuit, an NPN transistor is used in CE configuration. Here,  $V_{BB}$  supply will forward bias the emitter-

base junction and  $V_{CC}$  supply will reverse bias the collector-base junction. This biasing arrangement makes the transistor to operate in the active region. The magnitude of the input ac signal  $v_i$  always forward bias the emitter-base junction regardless of the polarity of the signal.

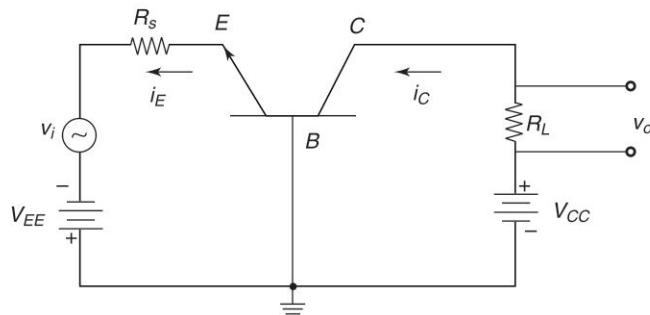


**Fig. 4.16(a)** CE transistor as an amplifier

During the positive half cycle of the input signal  $v_i$ , the forward bias across the emitter-base junction is increased. As a result, more electrons are injected into the base and reaches the collector, resulting in an increase in collector current  $i_c$ . This increase in collector current produces a greater voltage drop across the load resistance  $R_L$ .

However, during the negative half cycle of the input signal  $v_i$ , the forward bias across the emitter-base junction is decreased, resulting in a decrease in collector current  $i_c$ . This decrease in collector current produces a smaller voltage drop across the load resistance  $R_L$ . Hence, it is clear that a small change in the input ac signal in CE transistor amplifier produces a large change at the output with a voltage gain of around 500 and a phase shift of  $180^\circ$ . Here, the voltage gain is the ratio of output voltage to input voltage. Comparing to CB and CC transistor configurations, this CE transistor configuration is widely used in amplifier circuits due to its high voltage gain.

**CB Transistor as an Amplifier** A load resistor  $R_L$  is connected in series with the collector supply voltage  $V_{CC}$  of the CB transistor configuration as shown in Fig. 4.16(b).



**Fig. 4.16(b)** CB transistor as an amplifier

A small change in the input voltage between emitter and base, say  $\Delta V_i$ , causes a relatively larger change in the emitter current, say  $\Delta I_E$ . A fraction of this change in current is collected and passed through  $R_L$  and is denoted by the symbol  $\alpha'$ . Therefore, the corresponding change in voltage across the load resistor  $R_L$  due to this current is  $\Delta V_0 = \alpha' R_L \Delta I_E$ .

Here, the voltage amplification  $A_v = \frac{\Delta V_0}{\Delta V_i}$  is around 150 without any phase shift and thus, the transistor acts as an amplifier.

## 4.6 LARGE SIGNAL, dc AND SMALL-SIGNAL CE VALUES OF CURRENT GAIN

---

We know from the characteristics of CE configuration, the current amplification factor is  $\beta \equiv \frac{\alpha}{1 - \alpha}$ , and  $I_C = (1 + \beta) I_{CBO} + \beta I_B$ .

The above equation can be expressed as

$$I_C - I_{CBO} = \beta I_{CBO} + \beta I_B$$

Therefore, 
$$\beta = \frac{I_C - I_{CBO}}{I_B - (-I_{CBO})}$$

The output characteristics of CE configuration show that in the *cut-off* region, the values  $I_E = 0$ ,  $I_C = I_{CBO}$ , and  $I_B = -I_{CBO}$ . Therefore, the above equation gives the ratio of the collector-current increment to the base-current change from cut-off to  $I_B$ , and, hence,  $\beta$  is called the *large-signal current gain of common-emitter transistor*.

The dc current gain of the transistor is given by

$$\beta_{dc} \equiv h_{FE} \equiv \frac{I_C}{I_B}$$

Based on this  $h_{FE}$  value, we can determine whether the transistor is in saturation or not. For any transistor, in general,  $I_B$  is large compared to  $I_{CBO}$ . Under this condition, the value of  $h_{FE} \approx \beta$ .

The small-signal CE forward short-circuit gain  $\beta'$  is defined as the ratio of a collector-current increment  $\Delta I_C$  for a small base-current change  $\Delta I_B$ , at a fixed collector-to-emitter voltage  $V_{CE}$ .

i.e., 
$$\beta' \equiv \left. \frac{\partial I_C}{\partial I_B} \right|_{V_{CE}}$$

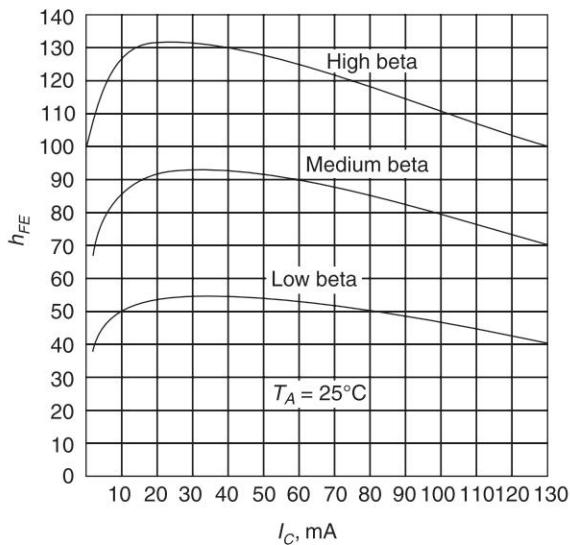
If  $\beta$  is independent of currents then  $\beta' = \beta \approx h_{FE}$ . However,  $\beta$  is a function of current, then

$$\beta' = \beta + (I_{CBO} + I_B) \frac{\partial \beta}{\partial I_B}$$

By using  $\beta' = h_{fe}$  and  $\beta \approx h_{FE}$ . Therefore, the above equation becomes

$$h_{fe} = \frac{h_{FE}}{1 - (I_{CBO} + I_B) \frac{\partial h_{FE}}{\partial I_C}}$$

In Fig. 4.17, the  $h_{FE}$  versus  $I_C$  shows a maximum and, hence,  $h_{fe} > h_{FE}$  for smaller currents, and  $h_{fe} < h_{FE}$  for larger currents. Therefore, the above equation is valid only for the active region.



**Fig. 4.17** Characteristic curves of dc current gain  $h_{FE}$  (at  $V_{CE} = -0.25$  V) versus collector current for low, medium, and high beta values

### EXAMPLE 4.1

In a common-base transistor circuit, the emitter current  $I_E$  is 10 mA and the collector current  $I_C$  is 9.8 mA. Find the value of the base current  $I_B$ .

**Solution** Given  $I_E = 10$  mA and  $I_C = 9.8$  mA

We know that emitter current is

$$I_E = I_B + I_C$$

$$\text{i.e., } 10 \times 10^{-3} = I_B + 9.8 \times 10^{-3}$$

$$\text{Therefore, } I_B = 0.2 \text{ mA}$$

### EXAMPLE 4.2

In a common-base connection, the emitter current  $I_E$  is 6.28 mA and the collector current  $I_C$  is 6.20 mA. Determine the common-base dc current gain.

**Solution** Given,  $I_E = 6.28$  mA and  $I_C = 6.20$  mA

We know that common-base dc current gain,

$$\alpha = \frac{I_C}{I_E} = \frac{6.20 \times 10^{-3}}{6.28 \times 10^{-3}} = 0.987$$

**EXAMPLE 4.3**

The common-base dc current gain of a transistor is 0.967. If the emitter current is 10 mA, what is the value of base current?

**Solution** Given  $\alpha = 0.967$  and  $I_E = 10 \text{ mA}$

The common-base dc current gain ( $\alpha$ ) is

$$\alpha = 0.967 = \frac{I_C}{I_E} = \frac{I_C}{10 \times 10^{-3}}$$

Therefore,  $I_C = 0.967 \times 10 \times 10^{-3} = 9.67 \text{ mA}$

The emitter current  $I_E = I_B + I_C$

i.e.,  $10 \times 10^{-3} = I_B + 9.67 \times 10^{-3}$

Therefore,  $I_B = 0.33 \text{ mA}$

**EXAMPLE 4.4**

The transistor has  $I_E = 10 \text{ mA}$  and  $\alpha = 0.98$ . Determine the values of  $I_C$  and  $I_B$ .

**Solution** Given,  $I_E = 10 \text{ mA}$  and  $\alpha = 0.98$

The common-base dc current gain,  $\alpha = \frac{I_C}{I_E}$

i.e.,  $0.98 = \frac{I_C}{10 \times 10^{-3}}$

Therefore,  $I_C = 0.98 \times 10 \times 10^{-3} = 9.8 \text{ mA}$

The emitter current  $I_E = I_B + I_C$

i.e.,  $10 \times 10^{-3} = I_B + 9.8 \times 10^{-3}$

Therefore,  $I_B = 0.2 \text{ mA}$

**EXAMPLE 4.5**

If a transistor has a  $\alpha$  of 0.97, find the value of  $\beta$ . If  $\beta = 200$ , find the value of  $\alpha$ .

**Solution** If  $\alpha = 0.97$ ,  $\beta = \frac{\alpha}{1 - \alpha} = \frac{0.97}{1 - 0.97} = 32.33$

If  $\beta = 200$ ,  $\alpha = \frac{\beta}{\beta + 1} = \frac{200}{200 + 1} = 0.995$

**EXAMPLE 4.6**

A transistor has  $\beta = 100$ . If the collector current is 40 mA, find the value of the emitter current.

**Solution** Given,  $\beta = 100$  and  $I_C = 40 \text{ mA}$

$$\beta = 100 = \frac{I_C}{I_B} = \frac{40 \times 10^{-3}}{I_B}$$

Therefore,

$$I_B = 40 \times 10^{-3} / 100 = 0.4 \text{ mA and}$$

$$I_E = I_B + I_C = (0.4 + 40) \times 10^{-3} = 40.4 \text{ mA}$$

### EXAMPLE 4.7

A transistor has  $\beta = 150$ . Find the collector and base currents, if  $I_E = 10 \text{ mA}$ .

**Solution** Given,  $\beta = 150$  and  $I_E = 10 \text{ mA}$

$$\text{The common-base current gain, } \alpha = \frac{\beta}{\beta + 1} = \frac{150}{150 + 1} = 0.993$$

Also,

$$\alpha = \frac{I_C}{I_E}$$

i.e.,

$$0.993 = \frac{I_C}{10}$$

Therefore,

$$I_C = 0.993 \times 10 \times 10^{-3} = 9.93 \text{ mA}$$

The emitter current

$$I_E = I_B + I_C$$

i.e.,

$$10 \times 10^{-3} = I_B + 9.93 \times 10^{-3}$$

Therefore,

$$I_B = (10 - 9.93) \times 10^{-3} = 0.07 \text{ mA}$$

### EXAMPLE 4.8

Determine the values of  $I_B$  and  $I_E$  for the transistor circuit if  $I_C = 80 \text{ mA}$  and  $\beta = 170$ .

**Solution** Given,  $\beta = 170$  and  $I_C = 80 \text{ mA}$

$$\text{We know that } (\beta), \quad \beta = 170 = \frac{I_C}{I_B} = \frac{80 \times 10^{-3}}{I_B}$$

$$\text{Therefore, } I_B = \frac{80 \times 10^{-3}}{170} = 0.47 \text{ mA}$$

and

$$I_E = I_B + I_C = (0.47 + 80) \text{ mA} = 80.47 \text{ mA}$$

### EXAMPLE 4.9

Determine the values of  $I_C$  and  $I_E$  for the transistor circuit of  $\beta = 200$  and  $I_B = 0.125 \text{ mA}$ .

**Solution** Given,  $I_B = 0.125 \text{ mA}$  and  $\beta = 200$

$$\text{Therefore, } \beta = 200 = \frac{I_C}{I_B} = \frac{I_C}{0.125 \times 10^{-3}}$$

$$\text{Therefore, } I_C = 200 \times 0.125 \times 10^{-3} = 25 \text{ mA}$$

and

$$I_E = I_B + I_C = (0.125 + 25) \times 10^{-3} = 25.125 \text{ mA}$$

**EXAMPLE 4.10**

Determine the values of  $I_C$  and  $I_B$  for the transistor circuit of  $I_E = 12 \text{ mA}$  and  $\beta = 100$ .

**Solution** Given,  $I_E = 12 \text{ mA}$  and  $\beta = 100$

$$\text{We know that base current, } I_B = \frac{I_E}{1 + \beta} = \frac{12 \times 10^{-3}}{1 + 100} = 0.1188 \text{ mA}$$

$$\text{and collector current, } I_C = I_E - I_B = (12 - 0.1188) \times 10^{-3} = 11.8812 \text{ mA}$$

**EXAMPLE 4.11**

A transistor has  $I_B = 100 \mu\text{A}$  and  $I_C = 2 \mu\text{A}$ . Find (a)  $\beta$  of the transistor, (b)  $\alpha$  of the transistor, (c) emitter current  $I_E$ , and (d) if  $I_B$  changes by  $+25 \mu\text{A}$  and  $I_C$  changes by  $+0.6 \text{ mA}$ , find the new value of  $\beta$ .

**Solution** Given,  $I_B = 100 \mu\text{A} = 100 \times 10^{-6} \text{ A}$  and  $I_C = 2 \text{ mA} = 2 \times 10^{-3} \text{ A}$ .

(a) To find  $\beta$  of the transistor

$$\beta = \frac{I_C}{I_B} = \frac{2 \times 10^{-3}}{100 \times 10^{-6}} = 20$$

(b) To find  $\alpha$  of the transistor

$$\alpha = \frac{\beta}{\beta + 1} = \frac{20}{1 + 20} = 0.952$$

(c) To find emitter current,  $I_E$

$$\begin{aligned} I_E &= I_B + I_C = 100 \times 10^{-6} + 2 \times 10^{-3} \text{ A} \\ &= (0.01 + 2) \times 10^{-3} = 2.01 \times 10^{-3} \text{ A} = 2.01 \text{ mA} \end{aligned}$$

(d) To find the new value of  $\beta$  when  $\Delta I_B = 25 \mu\text{A}$  and  $\Delta I_C = 0.6 \text{ mA}$

Therefore,  $I_B = (100 + 25) \mu\text{A} = 125 \mu\text{A}$

$$I_C = (2 + 0.6) \text{ mA} = 2.6 \text{ mA}$$

New value of  $\beta$  of the transistor,

$$\beta = \frac{I_C}{I_B} = \frac{2.6 \times 10^{-3}}{125 \times 10^{-6}} = 20.8$$

**EXAMPLE 4.12**

For a transistor circuit having  $\alpha = 0.98$ ,  $I_{CBO} = I_{CO} = 5 \mu\text{A}$ , and  $I_B = 100 \mu\text{A}$ , find  $I_C$  and  $I_E$ .

**Solution** Given,  $\alpha = 0.98$ ,  $I_{CBO} = I_{CO} = 5 \mu\text{A}$  and  $I_B = 100 \mu\text{A}$

The collector current is

$$I_C = \frac{\alpha \cdot I_B}{1 - \alpha} + \frac{I_{CO}}{1 - \alpha} = \frac{0.98 \times 100 \times 10^{-6}}{1 - 0.98} + \frac{5 \times 10^{-6}}{1 - 0.98} = 5.15 \text{ mA}$$

The emitter current is

$$I_E = I_B + I_C = 100 \times 10^{-6} + 5.15 \times 10^{-3} = 5.25 \text{ mA}$$

**EXAMPLE 4.13**

A germanium transistor used in a complementary symmetry amplifier has  $I_{CBO} = 10 \mu\text{A}$  at  $27^\circ\text{C}$  and  $h_{FE} = 50$ . (a) Find  $I_C$  when  $I_B = 0.25 \text{ mA}$ , and (b) assuming  $h_{FE}$  does not increase with temperature, find the value of new collector current, if the transistor's temperature rises to  $50^\circ\text{C}$ .

**Solution** Given,  $I_{CBO} = 10 \mu\text{A}$  and  $h_{FE} (= \beta) = 50$

(a) To find the value of collector current when  $I_B = 0.25 \text{ mA}$

$$\begin{aligned} I_C &= \beta I_B + (1 + \beta) I_{CBO} \\ &= 50 \times (0.25 \times 10^{-3}) + (1 + 50) \times (10 \times 10^{-6}) \text{ A} = 13.01 \text{ mA} \end{aligned}$$

(b) To find the value of new collector current if the temperature rises to  $50^\circ\text{C}$

We know that  $I_{CBO}$  doubles for every  $10^\circ\text{C}$  rise in temperature. Therefore,

$$\begin{aligned} I'_{CBO} (\beta = 50) &= I_{CBO} \times 2^{(T_2 - T_1)/10} = 10 \times 2^{(50 - 27)/10} \mu\text{A} \\ &= 10 \times 2^{2.3} \mu\text{A} = 49.2 \mu\text{A} \end{aligned}$$

Therefore, the collector current at  $50^\circ\text{C}$  is

$$\begin{aligned} I_C &= \beta \cdot I_B + (1 + \beta) I'_{CBO} \\ &= 50 \times (0.25 \times 10^{-3}) + (1 + 50) \times 49.2 \times 10^{-6} = 15.01 \text{ mA} \end{aligned}$$

**EXAMPLE 4.14**

When the emitter current of a transistor is changed by  $1 \text{ mA}$ , there is a change in collector current by  $0.99 \text{ mA}$ . Find the current gain of the transistor.

**Solution** The current gain of the transistor is  $\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{0.99 \times 10^{-3}}{1 \times 10^{-3}} = 0.99$

**EXAMPLE 4.15**

The dc current gain of a transistor in CE mode is 100. Determine its dc current gain in CB mode.

**Solution** The dc current gain of the transistor in CB mode is

$$\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} = \frac{100}{1 + 100} = 0.99$$

**EXAMPLE 4.16**

When  $I_E$  of a transistor is changed by  $1 \text{ mA}$ , its  $I_C$  changes by  $0.995 \text{ mA}$ . Find its common-base current gain  $\alpha$ , and common-emitter current gain  $\beta$ .

**Solution** Common-base current gain is  $\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{0.995 \times 10^{-3}}{1 \times 10^{-3}} = 0.995$

Common-emitter current gain is

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.995}{1 - 0.995} = 199$$

**EXAMPLE 4.17**

The current gain of a transistor in CE mode is 49. Calculate its common-base current gain. Find the base current when the emitter current is 3 mA.

**Solution** Given,  $\beta = 49$

We know that  $\alpha = \frac{\beta}{1 + \beta}$

Therefore, the common-base current gain is  $\alpha = \frac{49}{1 + 49} = 0.98$

We also know that  $\alpha = \frac{I_C}{I_E}$

Therefore,  $I_C = \alpha I_E = 0.98 \times 3 \times 10^{-3} = 2.94 \text{ mA}$

**EXAMPLE 4.18**

Determine  $I_C$ ,  $I_E$ , and  $\alpha$  for a transistor circuit having  $I_B = 15 \mu\text{A}$  and  $\beta = 150$ .

**Solution** The collector current,  $I_C = \beta I_B = 150 \times 15 \times 10^{-6} = 2.25 \text{ mA}$

The emitter current,

$$\begin{aligned} I_E &= I_C + I_B \\ &= 2.25 \times 10^{-3} + 15 \times 10^{-6} \\ &= 2.265 \text{ mA} \end{aligned}$$

Common-base current gain,  $\alpha = \frac{\beta}{1 + \beta} = \frac{150}{151} = 0.9934$

**EXAMPLE 4.19**

Determine the base, collector, and emitter currents and  $V_{CE}$  for the CE circuit shown in Fig. 4.18. For  $V_{CC} = 10 \text{ V}$ ,  $V_{BB} = 4 \text{ V}$ ,  $R_B = 200 \text{ k}\Omega$ ,  $R_C = 2 \text{ k}\Omega$ ,  $V_{BE(on)} = 0.7 \text{ V}$ ,  $\beta = 200$ .

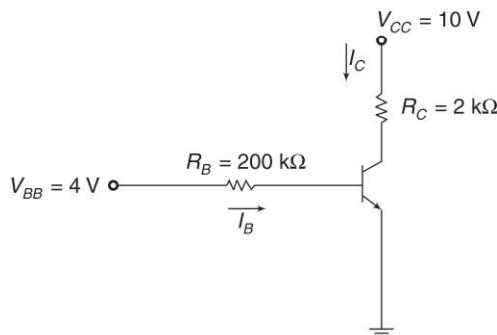


Fig. 4.18

**Solution**

Referring to Fig. 4.18, the base current is

$$I_B = \frac{V_{BB} - V_{BE(on)}}{R_B} = \frac{4 - 0.7}{200 \times 10^3} = 16.5 \mu\text{A}$$

The collector current is  $I_C = \beta I_B = 200 \times 16.5 \times 10^{-6} = 3.3 \text{ mA}$

The emitter current is  $I_E = I_C + I_B = 3.3 \times 10^{-3} + 16.5 \times 10^{-6} = 3.3165 \text{ mA}$

Therefore,  $V_{CE} = V_{CC} - I_C R_C = 10 - 3.3 \times 10^{-3} \times 2 \times 10^3 = 3.4 \text{ V}$

**EXAMPLE 4.20**

Calculate the values of  $I_C$  and  $I_E$  for a transistor with  $\alpha_{dc} = 0.99$  and  $I_{CBO} = 5 \mu\text{A}$ .  $I_B$  is measured as  $20 \mu\text{A}$ .

**Solution**

Given,  $\alpha_{dc} = 0.99$ ,  $I_{CBO} = 5 \mu\text{A}$  and  $I_B = 20 \mu\text{A}$

$$\begin{aligned} I_C &= \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}} + \frac{I_{CBO}}{1 - \alpha_{dc}} \\ &= \frac{0.99 \times 20 \times 10^{-6}}{1 - 0.99} + \frac{5 \times 10^{-6}}{1 - 0.99} = 2.48 \text{ mA} \end{aligned}$$

Therefore,  $I_E = I_B + I_C = 20 \times 10^{-6} + 2.48 \times 10^{-3} = 2.5 \text{ mA}$

**EXAMPLE 4.21**

The reverse leakage current of the transistor when connected in CB configuration is  $0.2 \mu\text{A}$  and it is  $18 \mu\text{A}$  when the same transistor is connected in CE configuration. Calculate  $\alpha_{dc}$  and  $\beta_{dc}$  of the transistor.

**Solution**

The leakage current  $I_{CBO} = 0.2 \mu\text{A}$

$$I_{CEO} = 18 \mu\text{A}$$

Assume that

$$I_B = 30 \text{ mA}$$

$$I_E = I_B + I_C$$

$$I_C = I_E - I_B = \beta I_B + (1 + \beta) I_{CBO}$$

We know that

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha} = (1 + \beta) I_{CBO}$$

$$\beta = \frac{I_{CEO}}{I_{CBO}} - 1 = \frac{18}{0.2} - 1 = 89$$

$$\begin{aligned} I_C &= \beta I_B + (1 + \beta) I_{CBO} \\ &= 89 (30 \times 10^{-3}) + (1 + 89) (0.2 \times 10^{-6}) = 2.67 \text{ A} \end{aligned}$$

$$\alpha_{dc} = 1 - \frac{I_{CBO}}{I_{CEO}} = 1 - \frac{0.2 \times 10^{-6}}{18 \times 10^{-6}} = 0.988$$

$$\beta_{dc} = \frac{I_C - I_{CBO}}{I_B - I_{CEO}} = \frac{2.67 - 0.2 \times 10^{-6}}{30 \times 10^{-3} - 18 \times 10^{-6}} = 89$$

**EXAMPLE 4.22**

If  $\alpha_{dc} = 0.99$  and  $I_{CBO} = 50 \mu A$ , find emitter current.

**Solution** Given  $\alpha_{dc} = 0.99$  and  $I_{CBO} = 50 \mu A$ ,

Assume that  $I_B = 1 \text{ mA}$

$$\begin{aligned} I_C &= \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}} + \frac{I_{CBO}}{1 - \alpha_{dc}} = \frac{0.99(1 \times 10^{-3})}{1 - 0.99} + \frac{50 \times 10^{-6}}{1 - 0.99} \\ &= \frac{0.99 \times 10^{-3}}{0.01} + \frac{50 \times 10^{-6}}{0.01} = 99 \text{ mA} + 5 \text{ mA} = 104 \text{ mA} \end{aligned}$$

$$I_E = I_C + I_B = 104 \text{ mA} + 1 \text{ mA} = 105 \text{ mA}$$

**EXAMPLE 4.23**

For the CE amplifier circuit shown in Fig. 4.19, find the percentage change in the collector current if the transistor with  $h_{fe} = 50$  is replaced by another transistor with  $h_{fe} = 150$ . Assume  $V_{BE} = 0.6$ .

**Solution**

$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{5 \times 10^3}{5 \times 10^3 + 25 \times 10^3} \times 12 = 2 \text{ V}$$

$$V_E = V_B - V_{BE} = 2 - 0.6 = 1.4 \text{ V}$$

$$\text{Here, } I_E = \frac{V_E}{R_E} = \frac{1.4}{100} = 14 \text{ mA}$$

$$\text{For } \beta = 50, I_B = \frac{I_E}{1 + \beta} = \frac{14 \times 10^{-3}}{51} = 274.5 \mu A$$

$$\text{Therefore, } I_{C1} = \beta I_B = 50 \times 274.5 \times 10^{-6} = 13.725 \text{ mA}$$

$$\text{For } \beta = 150, I_B = \frac{I_E}{1 + \beta} = \frac{14 \times 10^{-3}}{151} = 92.715 \text{ mA}$$

$$\text{Therefore, } I_{C2} = \beta I_B = 150 \times 92.715 \times 10^{-6} = 13.907 \text{ mA}$$

Hence, the percentage change in the collector current is calculated as

$$\frac{I_{C2} - I_{C1}}{I_{C1}} \times 100 = \frac{13.907 \times 10^{-3} - 13.725 \times 10^{-3}}{13.725 \times 10^{-3}} \times 100 = 1.326\%$$

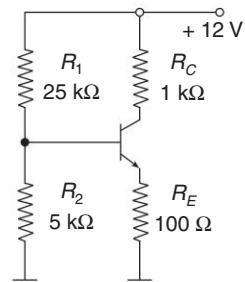


Fig. 4.19

**EXAMPLE 4.24**

Given an *NPN* transistor for which  $\alpha = 0.98$ ,  $I_{CO} = 2 \mu\text{A}$ , and  $I_{CEO} = 16 \mu\text{A}$ . A common-emitter connection is used as shown in Fig. 4.20 with  $V_{CC} = 12 \text{ V}$  and  $R_C = 4 \text{ k}\Omega$ . What is the minimum base current required in order for the transistor to enter into saturation region?

**Solution** Given,  $\alpha = 0.98$ ,  $I_{CO} = 2 \mu\text{A}$ ,  $I_{CEO} = 1.6 \mu\text{A}$ ,  $V_{CC} = 12 \text{ V}$  and  $R_C = 4 \text{ k}\Omega$ .

$$\begin{aligned} I_{C(\text{sat})} &= \frac{V_{CC}}{R_C} = \frac{12}{4 \times 10^3} = 3 \text{ mA} \\ \beta &= \frac{\alpha}{1 - \alpha} = \frac{0.98}{1 - 0.98} = 49 \\ I_{B(\text{min})} &= \frac{I_{C(\text{sat})}}{\beta} \\ &= \frac{3 \times 10^{-3}}{49} = 61.224 \times 10^{-6} = 61.224 \mu\text{A} \end{aligned}$$

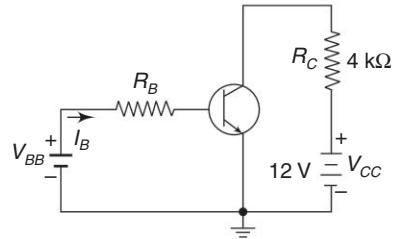


Fig. 4.20

**EXAMPLE 4.25**

A transistor operating in *CB* configuration has  $I_C = 2.98 \text{ mA}$ ,  $I_E = 3 \text{ mA}$ , and  $I_{CO} = 0.01 \text{ mA}$ . What current will flow in the collector circuit of this transistor when connected in *CE* configuration with a base current of  $30 \mu\text{A}$ ?

**Solution** Given  $I_C = 2.98 \text{ mA}$ ,  $I_E = 3 \text{ mA}$ ,  $I_{CO} = 0.01 \text{ mA}$  and  $I_B = 30 \mu\text{A}$ .

For *CB* configuration,  $I_C = \alpha I_E + I_{CO}$

$$\text{Therefore, } \alpha = \frac{I_C - I_{CO}}{I_E} = \frac{(2.98 - 0.01) \times 10^{-3}}{3 \times 10^{-3}} = 0.99$$

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.99}{1 - 0.99} = 99$$

For *CE* configuration,  $I_C = \beta I_B + (1 + \beta) I_{CO}$

$$= 99 \times 30 \times 10^{-6} + (1 + 99) \times 0.01 \times 10^{-3} = 3.97 \text{ mA.}$$

## 4.7 EBERS-MOLL MODEL OF A TRANSISTOR

The general expression for collector current  $I_C$  of a transistor for any voltage across the collector junction  $V_C$  and emitter current  $I_E$  is

$$I_C = -\alpha_N I_E - I_{CO} \left( e^{\frac{V_C}{V_T}} - 1 \right) \quad (4.27)$$

where  $\alpha_N$  is the current gain in *normal* operation and  $I_{CO}$  is the collector-junction reverse saturation current.

In inverted mode of operation, the above equation can be written as

$$I_E = -\alpha_I I_C - I_{EO} \left( e^{\frac{V_E}{V_T}} - 1 \right) \quad (4.28)$$

where  $\alpha_I$  is the inverted common-base current gain and  $I_{EO}$  is the emitter-junction reverse saturation current.

The above four parameters are related by the condition

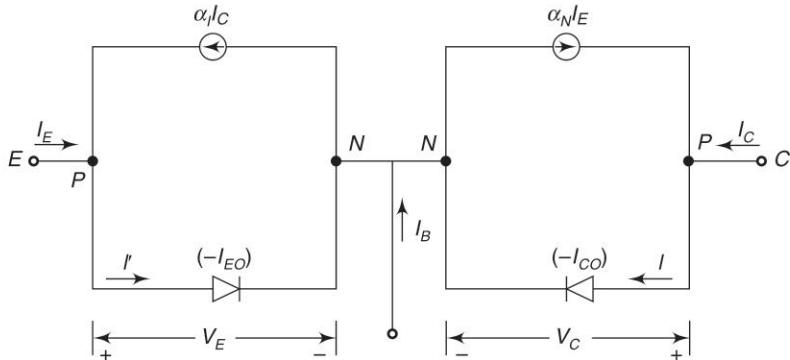
$$\alpha_I I_{CO} = \alpha_N I_{EO} \quad (4.29)$$

For many transistors,  $I_{EO}$  lies in the range  $0.5 I_{CO}$  to  $I_{CO}$ .

Figure 4.21 shows the Ebers–Moll model for a PNP transistor. Here, two separate ideal diodes are connected back to back with saturation currents  $-I_{EO}$  and  $-I_{CO}$  and there are two dependent current-controlled current sources shunting the ideal diodes. The current sources account for the minority carrier transport across the base. An application of Kirchhoff's current law to the collector node of Fig. 4.21 gives

$$I_C = -\alpha_N I_E + I = -\alpha_N I_E + I_O \left( e^{\frac{V_C}{V_T}} - 1 \right) \quad (4.30)$$

where  $I$  is the diode current.



**Fig. 4.21** Ebers–Moll model for a PNP transistor

As  $I_O$  is the magnitude of reverse saturation current, then  $I_O = -I_{CO}$ . Substituting this value of  $I_O$  in Eq. (4.30), we get

$$I_C = -\alpha_N I_E - I_{CO} \left( e^{\frac{V_C}{V_T}} - 1 \right)$$

which is nothing but the general expression for collector current of a transistor given in Eq. (4.27). Hence, this model is valid for both forward and reverse static voltages applied across the transistor junctions. Here, the base spreading resistance has been omitted and the difference between  $I_{CBO}$  and  $I_{CO}$  has been neglected.

The dependent current sources may be removed from Fig. 4.21, provided  $\alpha_N = \alpha_I = 0$ . If the base-width is made much larger than the diffusion length of minority carriers in the base, all minority carriers will recombine in the base and no minority carrier will be available to reach the collector. Therefore, the transistor

amplification factor  $\alpha$  will become zero. As a result, transistor action ceases. Hence, it is not possible to construct a transistor by simply placing two isolated diodes back to back.

#### **4.8 PUNCH-THROUGH OR REACH-THROUGH**

According to early effect, the width of the collector-junction depletion region increases with increased collector-junction voltage. As the voltage applied across the junction  $V_{CB}$  increases, the transition region penetrates deeper into the base and will have spread completely across the base to reach the emitter junction, as the base is very thin. Thus, the collector voltage has reached through the base region. This effect, known as reach-through, also affects the output characteristics of a transistor since  $I_C$  versus  $V_{CB}$  curves are no longer horizontal but take on a positive slope indicating that the device has a finite output impedance that is voltage dependent. Since the input characteristics are also affected, the input impedance is also influenced by  $V_{CB}$ .

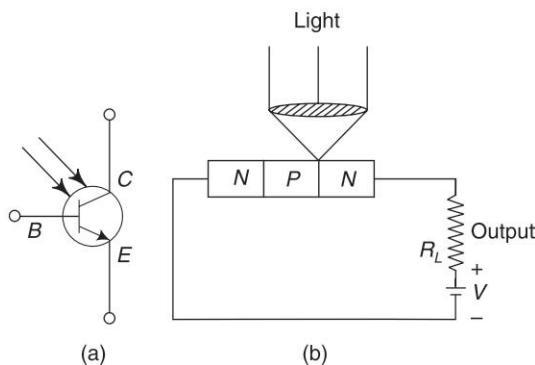
It is possible to raise the punch-through voltage by increasing the doping concentration in the base, but this automatically reduces the emitter efficiency.

Punch-through takes place at a fixed voltage between collector and base and is not dependent on circuit configuration, whereas avalanche multiplication takes place at different voltages depending upon the circuit configuration. Therefore, the voltage limit of a particular transistor is determined by either of the two types of breakdown, whichever occurs at lower voltage.

#### **4.9 PHOTOTRANSISTOR**

The phototransistor or photodiode is a much more sensitive semiconductor photodevice than the PN photodiode. The current produced by a photodiode is very low which cannot be directly used in control applications. Therefore, this current should be amplified before applying to control circuits. The phototransistor is a light detector which combines a photodiode and a transistor amplifier. When the phototransistor is illuminated, it permits a larger flow of current.

Figure 4.22 shows the circuit of an *NPN* phototransistor. It is usually connected in a CE configuration with the base open. A lens focuses the light on the base-collector junction. Although the phototransistor has three sections, only two leads, the emitter and collector leads, are generally used. In this device, base current is supplied by the current created by the light falling on the base-collector photodiode junction.



**Fig. 4.22** NPN phototransistor: (a) Symbol (b) Biasing arrangement

When there is no radiant excitation, the minority carriers are generated thermally, and the electrons crossing from the base to the collector and the holes crossing from the collector to the base constitute the reverse saturation collector current  $I_{CO}$ . With  $I_B = 0$ , the collector current is given by

$$I_C = (\beta + 1) I_{CO}$$

When the light is turned ON, additional minority carriers are photogenerated and the total collector current is

$$I_C = (\beta + 1)(I_{CO} + I_L)$$

where  $I_L$  is the reverse saturation current due to the light.

Current in a phototransistor is dependent mainly on the intensity of light entering the lens and is less affected by the voltage applied to the external circuit. Figure 4.23 shows a graph of collector current  $I_C$  as a function of collector-emitter voltage  $V_{CE}$  and as a function of illumination  $H$ .

The phototransistors find extensive applications in high-speed reading of computer punched cards and tapes, light detection systems, light operated switches, reading of film sound track, production line counting of objects which interrupt a light beam, etc.

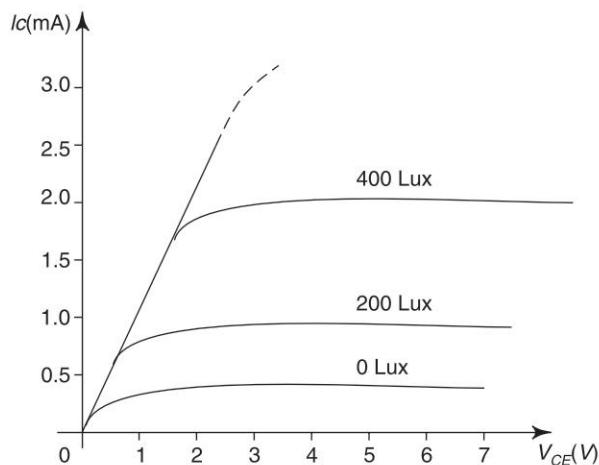


Fig. 4.23 Characteristics of a phototransistor

## 4.10 TYPICAL TRANSISTOR JUNCTION VOLTAGE VALUES

The specifications of some of the commonly used BJT-NPN small signal transistor and BJT-PNP small signal transistor are given in Table 4.2 (a) and (b), respectively.

**Table 4.2 (a)** *BJT – NPN Small Signal Transistor*

Parameter	Type	$I_C$ (max) (mA)	$P_D$ (max) (mW)	$V_{CEO}$ (max) (Volts)	$V_{CBO}$ (max) (Volts)	$h_{fe}$ (min-max) @ $I_C$ (mA)	$V_{ce}$ (Volts)	$f_T$ @MHz	Complement	Applications
BC107		100	300	45	50	110-450@2	5	300	BC177	Audio driver
BC108		100	300	20	30	110-800@2	5	300	BC178	General purpose
BC109		100	300	20	30	200-800@2	5	300	BC179	Low noise audio
BC547		100	625	45	50	110-800@2	5	300	BC557	Amplifier
BC548		100	625	30	30	110-800@2	5	300	BC558	Amplifier
BC549		100	625	30	30	110-800@2	5	250	BC559	Low noise audio
2N2369A		200	360	15	40	20 (min) @ 100	1	500 (min)	-	High speed switch
2N3904		200	350	40	60	100-300 @10	1	300 (min)	2N3906	Low level amplifier
2N4401		600	350	40	60	100-300 @ 150	2	250 (max)	2N4403	General purpose
2N3053		700	5.0W	40	60	50-250 @ 150	10	100	-	General purpose
2N2222A		800	500	40	75	100-300 @ 150	10	300	-	High speed switch
BFY50		1000	2800	35	80	30 (min) @ 150	10	60 (min)	-	General purpose
BUY82		10000	30W	60	150	40 (min) @ 1.5A	5	60	-	High power switch
2N3055		15A	115W	60	70	20-70 @ 4A	1.1	0.8	BDY 20	O/P – SW
2N916		360	25	45	50-200 @ 10	0.5	300	-	2N2222A	
2N2369		360		40	40-120 @ 10	0.35	500	-		
2N3040		360	30	40	40-160 @ 150	0.20	50	-	2N3040	
BF184		30	145	20	30	75 to 750	10	300	-	For IF amplifier
BF185		30	145	20	30	67	10	220	-	Low noise AN and FM applications
BF195		30	250	20	30	67	10	200	-	
SL100		500	800	50	60	50-280	7	-	SK100	AM for receivers class B push pull stage
PT4		2 Amps	4W	20	32	80-320	10	3	PT6	Amplifier and Radio receiver
AC176	1 Amp	155mW	32	32	83	-	Mc/S	AC128	Radio receivers, Tape recording	
BF115	30	145mW	30	50	45-165	-	230	-	General Broadcast and television	

**Table 4.2 (b)** *BjT – PNP Small Signal Transistor*

Parameter Type	$V_{CE}$ (Volts)	$V_{CB}$ (Volts)	$I_C$ (mA)	$V_{ce}@I_C$ (Volts)	$h_{fe}@I_C$ (MHz)	$f_T@I_C$ (MHz)	$P_{tot}$ (mW)	Use	Comparable Types			
BC157	-45	-50	-100	-0.25	10mA	75-260	2mA	150	10mA	300	S.S. Amplifier	BC177, BC212, BC 307
BC158	-25	-30	-100	0.25	10mA	75-500	2mA	150	10mA	300	S.S. Amplifier	BC175, BC308
BC159	-20	-25	-100	-0.25	10mA	125-500	2mA	150	10mA	300	S.S. Amplifier	BC179, BC309
BC557	-45	-50	-100	-	-	110-300	2mA	150	500	4p. small signal	BC157, DS557	
BC558	-30	-30	-100	-	-	75	2mA	150	500	4p. small signal	BC158, DS558	
AF115	-32	-32	-10	-	150	75	75	75	RF. Amplifier mixer oscillator in SW receiver	AF125, AF200		
2N2904	-40	-60	-0.6A	-	20-40	200	0.6W	Switching & driving applications	-	-		
AD162	-20	-32	-2A	-1	50-300	1.5	6W	Audio matched pair	-	-		
BC177	-45	-50	-100	-5	175-500	200	300	Audio driver	BC107	-		

## 4.11 TYPES OF FET

Based on the construction, the FET can be classified into two types as Junction FET (JFET) and Metal Oxide Semiconductor FET (MOSFET) or Insulated Gate FET (IGFET) or Metal Oxide Silicon Transistor (MOST).

Depending upon the majority carriers, JFET has been classified into two types, namely (i) N-Channel JFET with electrons as the majority carriers, and (ii) P-Channel JFET with holes as the majority carriers.

## 4.12 FET CONSTRUCTION

It consists of an *N*-type bar which is made of silicon. Ohmic contacts (terminals), made at the two ends of the bar, are called source and drain.

- **Source (S)** This terminal is connected to the negative pole of the battery. Electrons which are the majority carriers in the *N*-type bar enter the bar through this terminal.
- **Drain (D)** This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.
- **Gate (G)** Heavily doped *P*-type silicon is diffused on both sides of the *N*-type silicon bar by which *PN* junctions are formed. These layers are joined together and called the gate *G*.
- **Channel** The region *BC* of the *N*-type bar between the depletion region is called the channel. Majority carriers move from the source to drain when a potential difference  $V_{DS}$  is applied between the source and drain.

## 4.13 OPERATION AND CHARACTERISTICS OF FET

**When  $V_{GS} = 0$  and  $V_{DS} = 0$**  When no voltage is applied between drain and source, and gate and source, the thickness of the depletion regions around the *PN* junction is uniform as shown in Fig. 4.24.

### When $V_{DS} = 0$ and $V_{GS}$ is Decreased from Zero

In this case, the *PN* junctions are reverse biased and, hence, the thickness of the depletion region increases. As  $V_{GS}$  is decreased from zero, the reverse-bias voltage across the *PN* junction is increased and, hence, the thickness of the depletion region in the channel also increases until the two depletion regions make contact with each other. In this condition, the channel is said to be cut-off. The value of  $V_{GS}$  which is required to cut off the channel is called the cut off voltage  $V_C$ .

**When  $V_{GS} = 0$  and  $V_{DS}$  is Increased from Zero** Drain is positive with respect to the source with  $V_{GS} = 0$ . Now the majority carriers (electrons) flow through the *N*-channel from source to drain. Therefore,

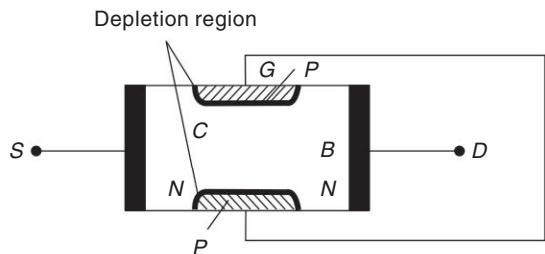


Fig. 4.24 JFET construction

the conventional current  $I_D$  flows from drain to source. The magnitude of the current will depend upon the following factors:

1. The number of majority carriers (electrons) available in the channel, i.e., the conductivity of the channel.
2. The length  $L$  of the channel.
3. The cross-sectional area  $A$  of the channel at  $B$ .
4. The magnitude of the applied voltage  $V_{DS}$ . Thus, the channel acts as a resistor of resistance  $R$  given by

$$R = \frac{\rho L}{A} \quad (4.31)$$

$$I_D = \frac{V_{DS}}{R} = \frac{AV_{DS}}{\rho L} \quad (4.32)$$

where  $\rho$  is the resistivity of the channel. Because of the resistance of the channel and the applied voltage  $V_{DS}$ , there is a gradual increase of positive potential along the channel from source to drain. Thus, the reverse voltage across the  $PN$  junctions increases and hence the thickness of the depletion regions also increases. Therefore, the channel is wedge-shaped as shown in Fig. 4.25.

As  $V_{DS}$  is increased, the cross-sectional area of the channel will be reduced. At a certain value  $V_P$  of  $V_{DS}$ , the cross-sectional area at  $B$  becomes minimum. At this voltage, the channel is said to be pinched off and the drain voltage  $V_P$  is called the pinch-off voltage.

As a result of the decreasing cross section of the channel with the increase of  $V_{DS}$ , the following results are obtained.

- (i) As  $V_{DS}$  is increased from zero,  $I_D$  increases along  $OP$ , and the rate of increase of  $I_D$  with  $V_{DS}$  decreases as shown in Fig. 4.26. The region from  $V_{DS} = 0$  V to  $V_{DS} = V_P$  is called the ohmic region. In the ohmic region, the drain-to-source resistance  $\frac{V_{DS}}{I_D}$  is related to the gate voltage  $V_{GS}$ , in an almost linear manner. This is useful as a Voltage Variable Resistor (VVR) or Voltage Dependent Resistor (VDR).
- (ii) When  $V_{DS} = V_P$ ,  $I_D$  becomes maximum. When  $V_{DS}$  is increased beyond  $V_P$ , the length of the pinch-off or saturation region increases. Hence, there is no further increase of  $I_D$ .
- (iii) At a certain voltage corresponding to the point  $B$ ,  $I_D$  suddenly increases. This effect is due to the avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and the drain. The drain voltage at which the breakdown occurs is denoted by  $BV_{DGO}$ . The variation of  $I_D$  with  $V_{DS}$  when  $V_{GS} = 0$  is shown in Fig. 4.26 by the curve  $OPBC$ .

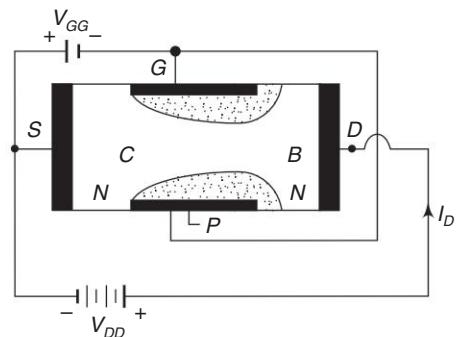


Fig. 4.25 JFET under applied bias

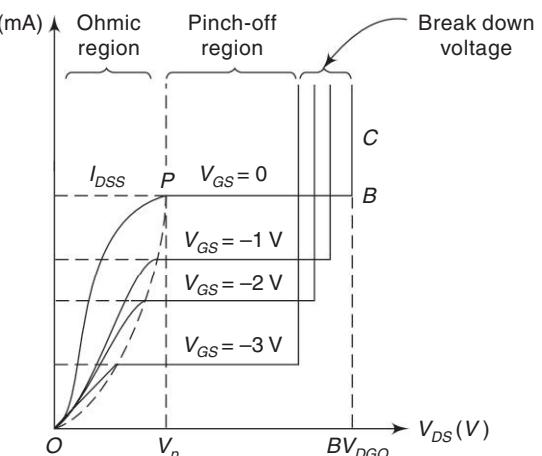


Fig. 4.26 Drain characteristics

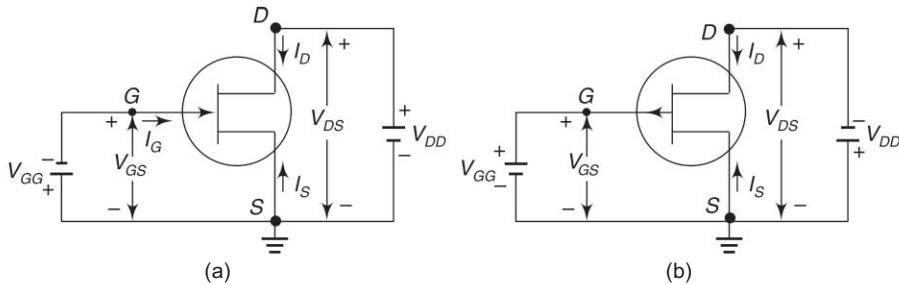
- When  $V_{GS}$  is Negative and  $V_{DS}$  is Increased When the gate is maintained at a negative voltage less than the negative cut-off voltage, the reverse voltage across the junction is further increased. Hence, for a negative value of  $V_{GS}$ , the curve of  $I_D$  versus  $V_{DS}$  is similar to that for  $V_{GS} = 0$ , but the values of  $V_P$  and  $BV_{DGO}$  are lower, as shown in Fig. 4.26.

From the curves, it is seen that above the pinch-off voltage, at a constant value of  $V_{DS}$ ,  $I_D$  increases with an increase of  $V_{GS}$ . Hence, a JFET is suitable for use as a voltage amplifier, similar to a transistor amplifier.

It can be seen from the curve that for voltage  $V_{DS} = V_P$ , the drain current is not reduced to zero. If the drain current is to be reduced to zero, then the ohmic voltage drop along the channel should also be reduced to zero. Further, the reverse biasing to the gate-source  $PN$  junction essential for pinching off the channel would also be absent.

The drain current  $I_D$  is controlled by the electric field that extends into the channel due to reverse-biased voltage applied to the gate; hence, this device has been given the name *Field Effect Transistor*.

In a bar of  $P$ -type semiconductor, the gate is formed due to  $N$ -type semiconductor. The working of the  $P$ -channel JFET will be similar to that of  $N$ -channel JFET with proper alterations in the biasing circuits; in this case, holes will be the current carriers instead of electrons. The circuit symbols for  $N$ -channel and  $P$ -channel JFETs are shown in Fig. 4.27. It should be noted that the direction of the arrow points in the direction of conventional current which would flow into the gate if the  $PN$  junction was forward biased.



**Fig. 4.27** Circuit symbols for (a) N-Channel JFET and (b) P-channel JFET

#### 4.14 JFET PARAMETERS

In a JFET, the drain current  $I_D$  depends upon the drain voltage  $V_{DS}$  and the gate voltage  $V_{GS}$ . Any one of these variables may be fixed and the relation between the other two are determined. These relations are determined by the three parameters which are defined below.

**Mutual Conductance or Transconductance,  $g_m$**  It is the slope of the transfer characteristic curves, and is defined by

$$g_m = \left( \frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}} = \frac{\Delta I_D}{\Delta V_{GS}}, V_{DS} \text{ held constant}$$

It is the ratio of a small change in the drain current to the corresponding small change in the gate voltage at a constant drain voltage. The change in  $I_D$  and  $V_{GS}$  should be taken on the straight part of the transfer characteristics. It has the unit of conductance in mho.

**Drain Resistance,  $r_d$**  It is the reciprocal of the slope of the drain characteristics and is defined by

$$r_d = \left( \frac{\partial V_{DS}}{\partial I_D} \right)_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D}, V_{GS} \text{ held constant}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in the drain current at a constant gate voltage. It has the unit of resistance in ohms.

The drain resistance at  $V_{GS} = 0$  V, i.e., when the depletion regions of the channel are absent, is called as *drain-source ON resistance*, represented as  $R_{DS}$  or  $R_{DS(ON)}$ .

The reciprocal of  $r_d$  is called the drain conductance. It is denoted by  $g_d$  or  $g_{ds}$ .

**Amplification Factor,  $\mu$**  It is defined by

$$\mu = \left( \frac{\partial V_{DS}}{\partial V_{GS}} \right) I_D = -\frac{\Delta V_{DS}}{\Delta V_{GS}}, I_D \text{ held constant}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in the gate voltage at a constant drain current. Here, the negative sign shows that when  $V_{GS}$  is increased,  $V_{DS}$  must be decreased for  $I_D$  to remain constant.

**Relationship among FET Parameters** As  $I_D$  depends on  $V_{DS}$  and  $V_{GS}$ , the functional equation can be expressed as

$$I_D = f(V_{DS}, V_{GS})$$

If the drain voltage is changed by a small amount from  $V_{DS}$  to  $(V_{DS} + \Delta V_{DS})$  and the gate voltage is changed by a small amount from  $V_{GS}$  to  $(V_{GS} + \Delta V_{GS})$  then the corresponding small change in  $I_D$  may be obtained by applying Taylor's theorem with neglecting higher order terms. Thus, the small change  $\Delta I_D$  is given by

$$\Delta I_D = \left( \frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} \Delta V_{DS} + \left( \frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}} \Delta V_{GS}$$

Dividing both the sides of this equation by  $\Delta V_{GS}$ , we obtain

$$\frac{\partial I_D}{\partial V_{GS}} = \left( \frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} \left( \frac{\Delta V_{DS}}{\Delta V_{GS}} \right) + \left( \frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}}$$

If  $I_D$  is constant, then  $\frac{\Delta I_D}{\Delta V_{GS}} = 0$

Therefore, we have

$$0 = \left( \frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} \left( \frac{\Delta V_{DS}}{\Delta V_{GS}} \right)_{I_D} + \left( \frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}}$$

Substituting the values of the partial differential coefficients, we get

$$0 = \left( \frac{1}{r_d} \right) (-\mu) + g_m$$

Hence,

$$\mu = g_m r_d$$

Therefore, amplification factor ( $\mu$ ) is the product of drain resistance ( $r_d$ ) and transconductance ( $g_m$ ).

**Power Dissipation,  $P_D$**  The FET's continuous power dissipation,  $P_D$ , is the product of  $I_D$  and  $V_{DS}$ .

**Pinch-off Voltage,  $V_P$**  A single-ended-geometry junction FET is shown in Fig. 4.28 in which the diffusion is done from one side only. The substrate is of  $P$ -type material which is epitaxially grown on an  $N$ -type channel. A  $P$ -type gate is then diffused into the  $N$ -type channel. The substrate functions as a second gate which is of relatively low-resistivity material. The diffused gate is also of very low-resistivity material, allowing the depletion region to spread mostly into the  $N$ -type channel. A slab of  $N$ -type semiconductor is sandwiched between two layers of  $P$ -type material forming two  $PN$  junction in this device.

The gate-reverse voltage that removes all the free charge from the channel is called the pinch-off voltage  $V_P$ . We consider that the  $P$ -type region is doped with  $N_A$  acceptor atoms, the  $N$ -type region is doped with  $N_D$  donor atoms and the junction formed is abrupt.

Moreover, if the acceptor impurity density is assumed to be much larger than the donor density, then the depletion region width in the  $P$ -region will be much smaller than the depletion width of the  $N$ -region, i.e.,  $N_A \gg N_D$ , then  $W_P \ll W_N$  and  $W_P = W$ . We know that, the relationship between potential and charge density is given by

$$\frac{d^2V}{dx^2} = \frac{-qN_D}{\epsilon}$$

Integrating the above equation subject to boundary conditions, we get

$$\frac{dV}{dx} = \frac{-qN_D}{\epsilon} (x - W)$$

Integrating again, we get

$$V = \frac{-qN_D}{2\epsilon} (x^2 - 2Wx)$$

At  $x = W$ ,  $V = V_B$  which is the junction or barrier potential. Thus,

$$V_B = \frac{qN_D W^2}{2\epsilon}$$

As the barrier potential represents a reverse voltage, it is lowered by an applied forward voltage  $V(x)$  at  $x$  and it is expressed as  $V_B = V_P - V(x)$ . Now, the space-charge width,  $W_n(x) = W(x)$  at a distance  $x$  along the channel in Fig. 4.29 becomes

$$W(x) = a - h(x) = \left\{ \frac{2\epsilon}{qN_D} [V_0 - V(x)] \right\}^{\frac{1}{2}}$$

where  $\epsilon$  is the dielectric constant of channel material,  $q$  is the magnitude of electronic charge,  $V_0$  is the junction contact potential at  $x$ ,  $V(x)$  is the

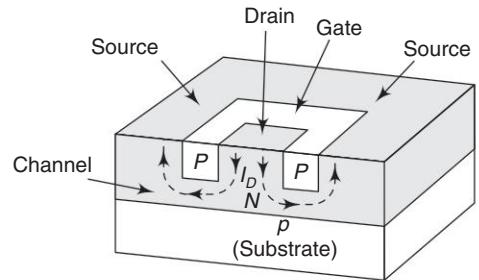


Fig. 4.28 Single-ended-geometry junction FET

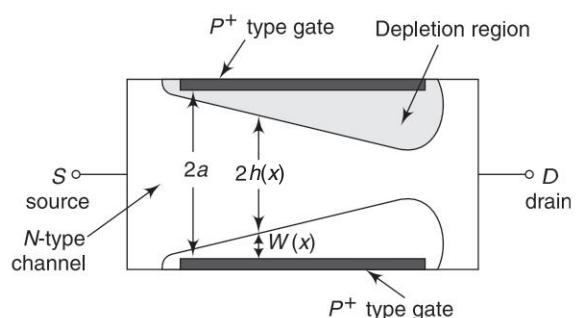


Fig. 4.29 Detailed structure of  $N$ -channel JFET

applied potential across space-charge region at  $x$  and is a negative value for an applied reverse bias,  $a$  is the metallurgical channel thickness between the substrate and  $P^+$  gate region,  $a - h(x)$  is the penetration  $W(x)$  of depletion region into channel at a point  $x$  along channel as shown in Fig. 4.29 and  $W_{PO}$  is the depletion region width at pinch-off.

If the drain current is zero,  $h(x)$  and  $V(x)$  are independent of  $x$  and hence  $h(x) = h$ . If we substitute  $h(x) = h = 0$  in the previous equation and solve for  $V$  with the assumption that  $|V_0| \ll |V|$ , the pinch-off voltage  $V_P$  can be obtained as

$$|V_P| = \frac{qN_D}{2\epsilon} a^2$$

Here, at pinch-off, the depletion width  $W_{PO} = a$  when  $|V_P| = |V_{GS}|$  and hence,

$$W_{PO} = \left( \frac{2\epsilon}{qN_D} V_{GS} \right)^{\frac{1}{2}}$$

To study the effect of  $V_{GS}$ , given  $V_{GS} = V_0 - V(x)$  in the space charge width equation, we get

$$a - h = \left\{ \frac{2\epsilon}{qN_D} V_{GS} \right\}^{\frac{1}{2}}$$

Substituting  $V_p = \frac{qN_D}{2\epsilon} a^2$  in the above equation, we get

$$a - h = \left[ \frac{a^2}{V_p} V_{GS} \right]^{\frac{1}{2}}$$

i.e., 
$$\frac{a - h}{a} = \left( \frac{V_{GS}}{V_p} \right)^{\frac{1}{2}}$$

Therefore, 
$$\left( 1 - \frac{h}{a} \right)^2 = \frac{V_{GS}}{V_p}$$

Hence, the gate-source voltage is

$$V_{GS} = \left( 1 - \frac{h}{a} \right)^2 V_p$$

For a reverse-biased  $P^+$ - $N$ -junction,  $V_{GS}$  must be a negative voltage across the gate junction and is independent of distance along the channel if  $I_D = 0$ .

### EXAMPLE 4.26

When a reverse gate voltage of 12 V is applied to JFET, the gate current is 1 nA. Determine the resistance between gate and source.

#### Solution

Given  $V_{GS} = 12 \text{ V}$ ,  $I_G = 10^{-9} \text{ A}$ .

Therefore, gate-to-source resistance =  $\frac{V_{GS}}{I_G} = \frac{12}{10^{-9}} = 12,000 \text{ M}\Omega$

### EXAMPLE 4.27

When the reverse gate voltage of JFET changes from 4.0 to 3.9 V, the drain current changes from 1.3 to 1.6 mA. Find the value of transconductance.

#### Solution

$$\Delta V_{GS} = 4.0 - 3.9 = 0.1 \text{ V}$$

$$\Delta I_D = 1.6 - 1.3 = 0.3 \text{ mA}$$

Therefore, transconductance,  $g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3 \times 10^{-3}}{0.1} = 3 \text{ m mho}$

#### 4.14.1 Expression for Saturation Drain Current

For the transfer characteristics,  $V_{DS}$  is maintained constant at a suitable value greater than the pinch-off voltage  $V_p$ . The gate voltage  $V_{GS}$  is decreased from zero till  $I_D$  is reduced to zero. The transfer characteristics  $I_D$  versus  $V_{GS}$  is shown in Fig. 4.30. The shape of the transfer characteristic is very nearly a parabola. It is found that the characteristic is approximately represented by the parabola,

$$I_{DS} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2 \quad (4.33)$$

where  $I_{DS}$  is the saturation drain current,  $I_{DSS}$  is the value of  $I_{DS}$  when  $V_{GS} = 0$ , and  $V_p$  is the pinch-off voltage.

Differentiating Eq. (4.33) with respect to  $V_{GS}$ , we can obtain an expression for  $g_m$ .

$$\frac{\partial I_{DS}}{\partial V_{GS}} = I_{DSS} \times 2 \left( 1 - \frac{V_{GS}}{V_p} \right) \left( -\frac{1}{V_p} \right)$$

We know that,  $g_m = \frac{\delta I_{DS}}{\delta V_{GS}}$ ,  $V_{DS}$  is constant.

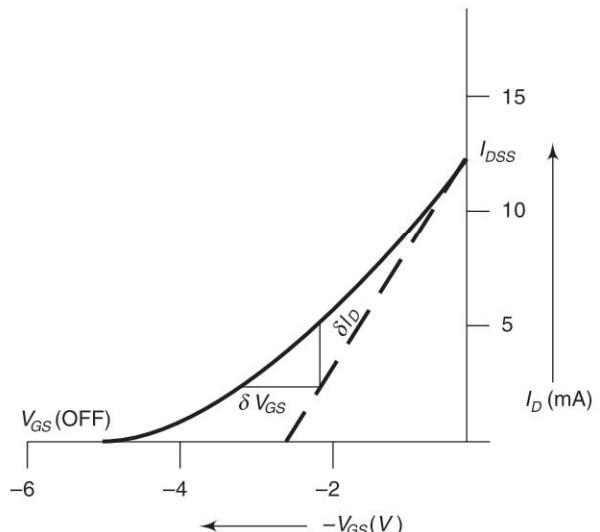
$$\text{Therefore, } g_m = \frac{-2 I_{DSS}}{V_p} \left( 1 - \frac{V_{GS}}{V_p} \right) \quad (4.34)$$

Now from Eq. (4.33), we have

$$\left( 1 - \frac{V_{GS}}{V_p} \right) = \sqrt{\frac{I_{DS}}{I_{DSS}}} \quad (4.35)$$

Substituting this value in Eq. (4.34), we get

$$g_m = \frac{-2 \sqrt{I_{DS} I_{DSS}}}{V_p}$$



**Fig. 4.30** Transfer characteristics of JFET

Suppose  $g_m = g_{mo}$ , when  $V_{GS} = 0$ , then from Eq. (4.34),

$$g_{mo} = -\frac{2I_{DSS}}{V_P} \quad (4.36)$$

Therefore, from Eqs (4.34) and (4.36),

$$g_m = g_{mo} \left( 1 - \frac{V_{GS}}{V_P} \right) \quad (4.37)$$

Equation (4.35) shows that  $g_m$  varies as the square root of the saturation drain current  $I_{DS}$ , and Eq. (4.37) shows that  $g_m$  decreases linearly with increase of  $V_{GS}$ .

#### 4.14.2 Slope of the Transfer Characteristic at $I_{DSS}$

From Eq. (4.35), we have

$$g_m = \frac{-2\sqrt{I_{DS}I_{DSS}}}{V_P}$$

or  $\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{2\sqrt{I_{DSS}I_{DSS}}}{V_P}$

Substituting  $I_{DS} = I_{DSS}$ ,

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{-2I_{DS}}{V_P} = \frac{I_{DSS}}{\frac{-V_P}{2}}$$

This equation shows that the tangent to the curve at  $I_{DS} = I_{DSS}$ ,  $V_{GS} = 0$ , will have an intercept at  $\frac{-V_P}{2}$  on the axis of  $V_{GS}$  as shown in Fig. 4.30. Therefore, the value of  $V_P$  can be found by drawing the tangent at  $I_{DS} = I_{DSS}$ ,  $V_{GS} = 0$ .

The gate-source cut-off voltage,  $V_{GS(\text{off})}$ , on the transfer characteristic is equal to the pinch-off voltage,  $V_P$ , on the drain characteristics, i.e.,  $V_P = |V_{GS(\text{off})}|$ .

Therefore,  $I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2$

#### 4.14.3 Biasing for Zero Current Drift

Figure 4.31 shows the transfer characteristics of  $N$  channel JFET for different values of temperature. Here, the drain current varies due to change in temperature. The two factors which make drain current to change with temperature are the mobility of majority carriers and the depletion region width.

The mobility of majority carriers decreases with increase in temperature. As the temperature increases, the lattice ions vibrate more vigorously and hence, the carriers cannot move freely in the crystalline structure. For the given gate-source voltage  $V_{GS}$ , their velocity is decreased and this reduces the drain current. The reduction in  $I_D$  is 0.7% for 1°C increase in the temperature.

The width of the depletion region (increase in channel width) decreases with increase in temperature. This allows  $I_D$  to increase and the increase in  $I_D$  is equivalent to a change of 2.2 mV/°C in  $|V_{GS}|$ . This is a similar phenomenon to the change of  $|V_{BE}|$  of 2.5 mV/°C in bipolar transistor.

Hence, it is required to design a biasing circuit which compensates for these two factors, so that there is no change of drain current with temperature. Such a biasing is called Biasing for zero current drift.

Due to the change in  $I_D$  and change in  $V_{GS}$  for 1°C, the condition for zero current drift can be obtained as

$$0.007|I_D| = 0.0022 g_m$$

i.e.,  $\frac{|I_D|}{g_m} = 0.314 \text{ V}$

We know that,  $I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$  and  $g_m = \frac{-2I_{DSS}}{V_P} \left[ 1 - \frac{V_{GS}}{V_P} \right]$ .

Hence,

$$\frac{|I_D|}{g_m} = \frac{I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2}{-\frac{2I_{DSS}}{V_P} \left[ 1 - \frac{V_{GS}}{V_P} \right]} = \frac{|V_P| - |V_{GS}|}{-2} = 0.314 \text{ V}$$

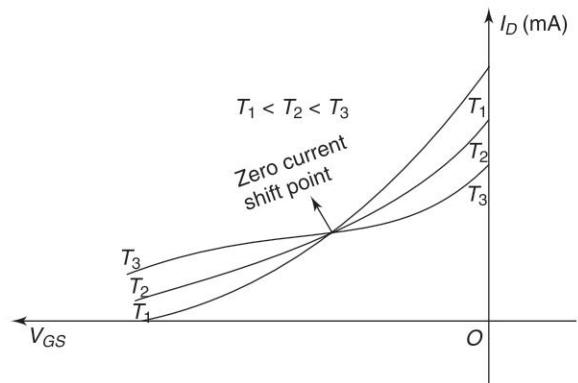
Therefore,  $|V_P| - |V_{GS}| = -0.628 \text{ V} \approx -0.63 \text{ V}$

From the above equation, it is seen that, if the value of  $V_P$  is known, the value of  $V_{GS}$  for zero drift current can be obtained.

When  $V_{GS}$  is adjusted for zero drift current, the drain current  $I_D$  and the transconductance  $g_m$  are given by

$$I_D = I_{DSS} \left[ 1 - \frac{V_P + 0.63}{V_P} \right]^2 = I_{DSS} \left[ \frac{0.63}{V_P} \right]^2$$

and  $g_m = g_{mo} \left[ 1 - \frac{V_P + 0.63}{V_P} \right] = g_{mo} \left( \frac{0.63}{|V_P|} \right)$



**Fig. 4.31** Transfer characteristics for an N channel FET as a function of temperature  $T$

#### EXAMPLE 4.28

A FET has a drain current of 4 mA. If  $I_{DSS} = 8 \text{ mA}$  and  $V_{GS(\text{off})} = -6 \text{ V}$ . Find the values of  $V_{GS}$  and  $V_P$ .

#### Solution

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2$$

$$4 = 8 \left[ 1 + \frac{V_{GS}}{6} \right]^2$$

$$1 + \frac{V_{GS}}{6} = \sqrt{\frac{4}{8}} = \frac{1}{\sqrt{2}} = 0.707$$

Therefore,

$$V_{GS} = -1.76 \text{ V}$$

$$V_P = |V_{GS(\text{off})}| = 6 \text{ V}$$

### EXAMPLE 4.29

An *N*-channel JFET has  $I_{DSS} = 8 \text{ mA}$  and  $V_P = -5 \text{ V}$ . Determine the minimum value of  $V_{DS}$  for pinch-off region and the drain current  $I_{DS}$ , for  $V_{GS} = -2 \text{ V}$  in the pinch-off region.

**Solution** The minimum value of  $V_{DS}$  for pinch-off to occur for  $V_{GS} = -2 \text{ V}$  is

$$V_{DS \min} = V_{GS} - V_P = -2 - (-5) = 3 \text{ V}$$

$$I_{DS} = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2 = 8 \times 10^{-3} [1 - (-2)/(-5)]^2 = 2.88 \text{ mA}$$

### EXAMPLE 4.30

Determine the pinch-off voltage for an *N*-channel silicon FET with a channel width of  $5.6 \times 10^{-4} \text{ cm}$  and a donor concentration of  $10^{15}/\text{cm}^3$ . Given, the dielectric constant of Si is 12.

**Solution**

$$\text{Given } N_D = 10^{15}/\text{cm}^3 = 10^{21}/\text{m}^3, \epsilon = \epsilon_r \epsilon_o = 12 \epsilon_o$$

$$a = 5.6 \times 10^{-4} \text{ cm} = 5.6 \times 10^{-6} \text{ m}$$

$$\text{The pinch-off voltage, } |V_P| = \frac{qN_D}{2\epsilon} a^2$$

where  $\epsilon$  = dielectric constant of channel material (Si) =  $\epsilon_r \epsilon_o = 12 \epsilon_o$

$q$  = magnitude of electronic charge

$a$  = in metres and  $N_D$  is in electrons/m<sup>3</sup>

$$|V_P| = \frac{1.602 \times 10^{-19} \times 10^{21}}{2 \times 12 \times 8.854 \times 10^{-12}} \times (5.6 \times 10^{-6})^2 = 23.6 \text{ V}$$

### EXAMPLE 4.31

For a *P*-channel silicon FET, with an effective channel width,  $a = 2 \times 10^{-4} \text{ cm}$  and channel resistivity  $\rho = 20 \Omega\text{-cm}$ , find the pinch-off voltage.

**Solution** We know that the pinch-off voltage for *P*-channel FET,  $V_P = \frac{qN_A}{2\epsilon} \times a^2$ .

For silicon,  $\epsilon = 12\epsilon_o$  and  $\mu_p = 500 \text{ cm}^2/\text{V-s}$

$$\sigma = \frac{1}{\rho} = p\mu_p \times q = N_A \mu_p \times q$$

i.e., 
$$qN_A = \frac{1}{\rho\mu_p} = \frac{1}{20 \times 500} = 1 \times 10^{-4}$$

Therefore, 
$$V_P = \frac{qN_A}{2\epsilon} \times a^2 = \frac{1 \times 10^{-4}}{2 \times 12 \times 8.854 \times 10^{-12}} \times (2 \times 10^{-4})^2 = 1.89 \text{ V}$$

#### 4.14.4 Comparison of JFET and BJT

1. FET operation depends only on the flow of majority carriers—holes for *P*-channel FETs and electrons for *N*-channel FETs. Therefore, they are called *unipolar devices*. Bipolar transistor (BJT) operation depends on both minority and majority current carriers.
2. As FET has no junctions and the conduction is through an *N*-type or *P*-type semiconductor material, FET is less noisy than BJT.
3. As the input circuit of FET is reverse biased, FET exhibits a much higher input impedance (in the order of 100 MΩ) and lower output impedance and there will be a high degree of isolation between input and output. So, FET can act as an excellent buffer amplifier but the BJT has low input impedance because its input circuit is forward biased.
4. FET is a voltage controlled device, i.e., voltage at the input terminal controls the output current, whereas BJT is a current controlled device, i.e., the input current controls the output current.
5. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
6. The performance of a BJT is degraded by neutron radiation because of the reduction in minority-carrier lifetime, whereas FETs can tolerate a much higher level of radiation since they do not rely on minority carriers for their operation.
7. The performance of an FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.
8. Since the FET does not suffer from minority carrier storage effects, it has higher switching speeds and cut-off frequencies. BJT suffers from minority carrier storage effects and, therefore, has lower switching speed and cut-off frequencies.
9. FET amplifiers have low gain-bandwidth product due to the junction capacitive effects and produce more signal distortion except for small-signal operation.
10. BJTs are cheaper to produce than FETs.

#### 4.14.5 Applications of JFET

1. FETs are used as a buffer in measuring instruments and receivers since they have high input impedance and low output impedance.
2. FETs are used in RF amplifiers in FM tuners, and in communication equipment for its low noise level.
3. Since the input capacitance is low, FETs are used in cascade amplifiers in measuring and test equipments.
4. Since the device is voltage controlled, FETs are used as a voltage variable resistors in operational amplifiers and tone controls.
5. FETs are used in mixer circuits in FM and TV receivers, and in communication equipment because their intermodulation distortion is low.
6. They are used in oscillator circuits because frequency drift is low.

7. As the coupling capacitor is small, FETs are used in low-frequency amplifiers in hearing aids and in inductive transducers.
8. FETs are used in digital circuits in computers, LSD, and memory circuits because of their small size.

## 4.15 MOSFET – TYPES AND CONSTRUCTION

### 4.15.1 Types of MOSFET

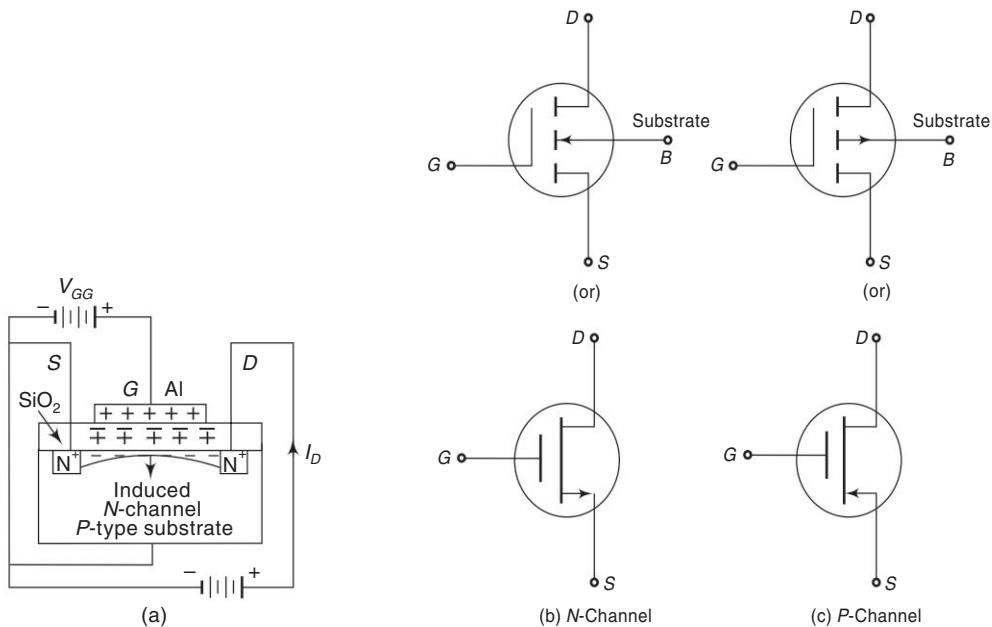
MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is the common term for the Insulated Gate Field Effect Transistor (IGFET). There are two basic forms of MOSFET: (i) Enhancement MOSFET, and (ii) Depletion MOSFET.

**Principle** By applying a transverse electric field across an insulator deposited on the semiconducting material, the thickness and, hence, the resistance of a conducting channel of a semiconducting material can be controlled.

In a depletion MOSFET, the controlling electric field reduces the number of majority carriers available for conduction, whereas in the enhancement MOSFET, application of electric field causes an increase in the majority carrier density in the conducting regions of the transistor.

### 4.15.2 Construction

The construction of an *N-channel* enhancement MOSFET is shown in Fig. 4.32(a), and the circuit symbols for an *N-channel* and a *P-channel* enhancement MOSFET are shown in Figs 4.32(b) and (c), respectively. As there is no continuous channel in an enhancement MOSFET, this condition is represented by the broken line in the symbols.



**Fig. 4.32** (a) *N*-channel enhancement MOSFET (b) and (c) Circuit symbols for enhancement MOSFET

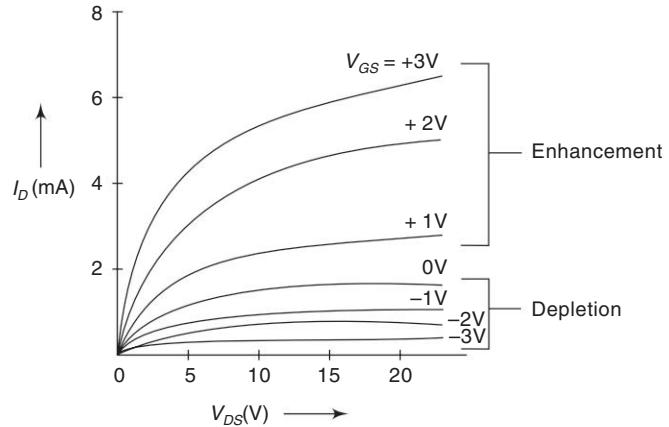
Two highly doped N<sup>+</sup> regions are diffused in a lightly doped substrate of P-type silicon substrate. One N<sup>+</sup> region is called the source S and the other one is called the drain D. They are separated by 1 mil ( $10^{-3}$  inch). A thin insulating layer of SiO<sub>2</sub> is grown over the surface of the structure and holes are cut into the oxide layer, allowing contact with source and drain. Then a thin layer of metal aluminium is formed over the layer of SiO<sub>2</sub>. This metal layer covers the entire channel region and it forms the gate G.

The metal area of the gate, in conjunction with the insulating oxide layer of SiO<sub>2</sub> and the semiconductor channel forms a parallel-plate capacitor. This device is called the insulated gate FET because of the insulating layer of SiO<sub>2</sub>. This layer gives an extremely high input impedance for the MOSFET.

## 4.16 OPERATION AND CHARACTERISTICS OF MOSFET

### 4.16.1 Operation of MOSFET

If the substrate is grounded and a positive voltage is applied at the gate, the positive charge on G induces an equal negative charge on the substrate side between the source and drain regions. Thus, an electric field is produced between the source and drain regions. The direction of the electric field is perpendicular to the plates of the capacitor through the oxide. The negative charge of electrons which are minority carriers in the P-type substrate forms an inversion layer. As the positive voltage on the gate increases, the induced negative charge in the semiconductor increases. Hence, the conductivity increases and current flows from source to drain through the induced channel. Thus, the drain current is enhanced by the positive gate voltage as shown in Fig. 4.33.



**Fig. 4.33** Volt-ampere characteristics of MOSFET

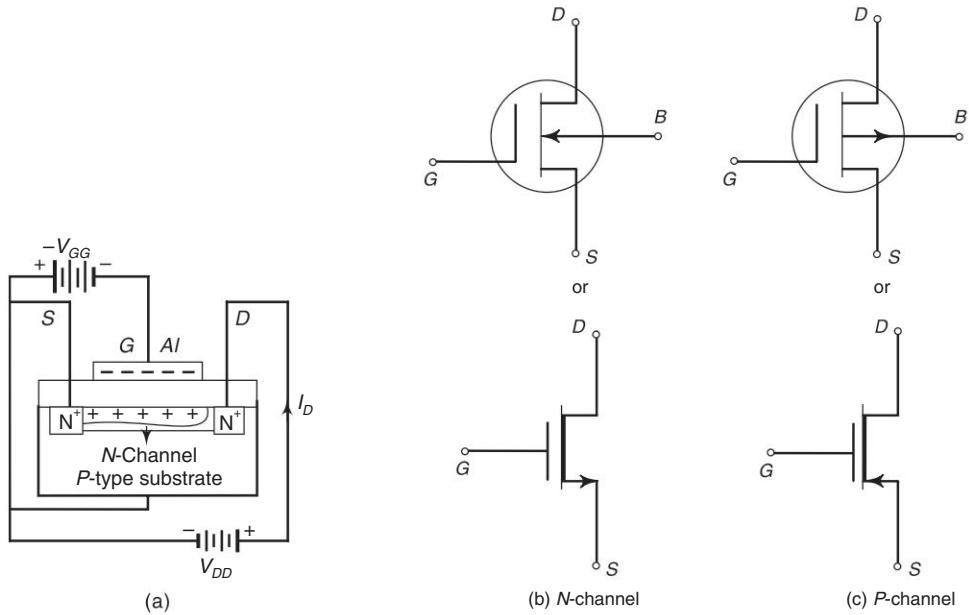
### 4.16.2 Depletion MOSFET

The construction of an N-channel depletion MOSFET is shown in Fig. 4.34(a) where an N-channel is diffused between the source and drain to the basic structure of MOSFET. The circuit symbols for an N-channel and a P-channel depletion MOSFET are shown in Figs 4.34(b) and (c), respectively.

With  $V_{GS} = 0$  and the drain D at a positive potential with respect to the source, the electrons (majority carriers) flow through the N-channel from S to D. Therefore, the conventional current  $I_D$  flows through the channel D to S. If the gate voltage is made negative, positive charge consisting of holes is induced in the channel through SiO<sub>2</sub> of the gate-channel capacitor. The introduction of the positive charge causes depletion of mobile electrons in the channel. Thus, a depletion region is produced in the channel. The shape of the depletion region depends on  $V_{GS}$  and  $V_{DS}$ . Hence, the channel will be wedge shaped as shown in Fig. 4.34(a). When  $V_{DS}$  is increased,  $I_D$  increases and it becomes practically constant at a certain value of  $V_{DS}$ , called the pinch-off voltage. The drain current  $I_D$  almost gets saturated beyond the pinch-off voltage.

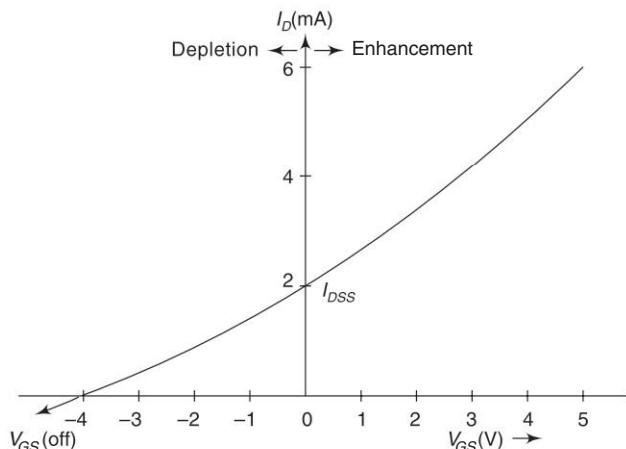
Since the current in an FET is due to majority carriers (electrons for an N-type material), the induced positive charges make the channel less conductive, and  $I_D$  drops as  $V_{GS}$  is made negative.

The depletion MOSFET may also be operated in an enhancement mode. It is only necessary to apply a positive gate voltage so that negative charges are induced into the  $N$ -type channel. Hence, the conductivity of the channel increases and  $I_D$  increases. As the depletion MOSFET can be operated with bipolar input signals irrespective of doping of the channel, it is also called *dual-mode MOSFET*. The volt-ampere characteristics are indicated in Fig. 4.33.



**Fig. 4.34** (a) N-channel depletion MOSFET, (b) and (c) Circuit symbols for depletion MOSFETs

The curve of  $I_D$  versus  $V_{GS}$  for constant  $V_{DS}$  is called the transfer characteristics of the MOSFET and is shown in Fig. 4.35.

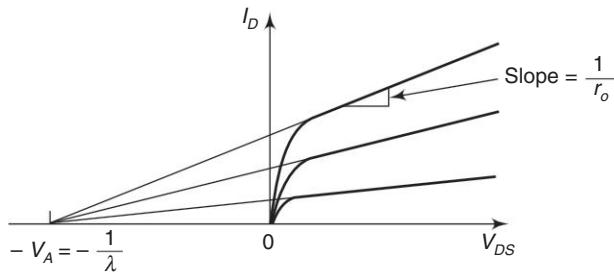


**Fig. 4.35** Transfer characteristics of MOSFET

**Effect of Channel-Length Modulation** In actual MOSFET characteristic as shown in Fig. 4.36, a non-zero slope exists beyond the saturation point. For the saturation region, i.e., ( $V_{DS} > V_{DS}$  (sat)), the effective channel length decreases and this phenomenon is called channel length modulation. For an  $N$ -channel device, the slope of the curve in the saturation region can be expressed by using the drain current  $I_D$  given by

$$I_D = K_N(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$$

where  $\lambda$  is a positive quantity called the channel-length modulation parameter or  $\lambda^{-1}$  is analogous to the Early voltage in bipolar transistors,  $K_N$  is the conduction parameter and  $V_{TN}$  is the threshold voltage. The curves are extended so that the intercept at a point  $I_D = 0$ ,  $V_{DS} = -V_E$  which means that  $V_E = 1/\lambda$ .



**Fig. 4.36** Effect of channel-length modulation due to the non-zero slope in the saturation region, resulting in a finite output resistance

The output resistance due to the channel-length modulation is expressed by

$$r_o = \left( \frac{\partial I_D}{\partial V_{DS}} \right)^{-1} \Bigg|_{V_{GS} = \text{constant}}$$

The output resistance can be determined at the  $Q$ -point by

$$r_o = [\lambda K_N(V_{GSQ} - V_{TN})^2]^{-1}$$

$$= \left[ \lambda I_{DSS} \left( 1 - \frac{V_{GSQ}}{V_P} \right)^2 \right]^{-1}$$

$$\text{i.e., } r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_E}{I_{DQ}}$$

The output resistance is an important factor in the analysis of small-signal equivalent circuit of MOSFET.

**Threshold Voltage in MOSFET** The threshold voltage is the applied gate voltage needed to achieve the threshold inversion point. The condition for this threshold inversion point is that the surface potential,  $\Phi_s = 2\Phi_{fp}$  for  $P$ -type semiconductor and  $\Phi_s = 2\Phi_{fn}$  for  $N$ -type semiconductor. Here,  $\Phi_{fp}$  and  $\Phi_{fn}$  are the difference in potential between the Fermi energy levels for  $P$ -type and  $N$ -type semiconductors. The potential  $\Phi_{fp}$  for  $P$ -type semiconductor is given by

$$\Phi_{fp} = V_T \ln \left( \frac{N_A}{n_i} \right)$$

where  $V_T = \frac{kT}{q} = 26 \text{ mV}$  at room temperature,  $N_A$  is the acceptor doping concentration and  $n_i$  is the intrinsic carrier concentration. The threshold voltage can be derived in terms of the electrical and geometrical properties of the MOS capacitor.

Figure 4.37 shows the charge distribution in the MOS capacitor at the threshold inversion point for a P-type semiconductor substrate. Consider that the space charge width reaches its maximum value. Let us assume that there are equivalent oxide charge,  $Q'_{ss}$ , and the positive charge on the metal gate at threshold,  $Q'_{mT}$ . Here, the prime on  $Q'_{ss}$  and  $Q'_{mT}$  indicates the charge per unit area and the inversion layer charge is neglected at this threshold inversion point.

The space charge width is given by

$$W_d = \left( \frac{2\epsilon_s \Phi_s}{qN_A} \right)^{1/2}$$

where  $\epsilon_s$  is the permittivity of the semiconductor and  $q$  is the charge of an electron. From conservation of charge, we can write

$$Q'_{mT} + Q'_{ss} = |Q'_{SD}(\max)|$$

where  $|Q'_{SD}(\max)| = qN_A W_{dT}$  is the magnitude of the maximum space charge density per unit area of the depletion region and  $W_{dT}$  is the maximum space charge width.

Figure 4.38 shows the energy-band diagram of the MOS device with an applied positive gate voltage. If a gate voltage is applied, the voltage across the oxide,  $V_{ox}$ , and the surface potential,  $\Phi_s$ , will change. Therefore,

$$V_G = \Delta V_{ox} + \Delta \Phi_s = V_{ox} + \Phi_s + \Phi_{ms}$$

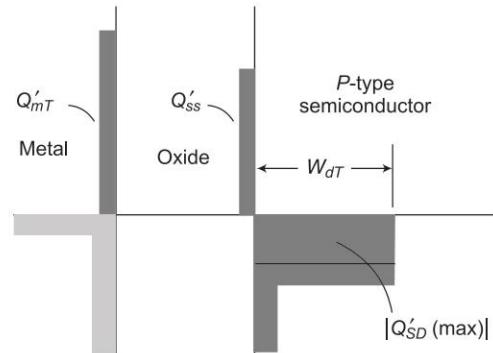
where  $\Phi_{ms}$  is metal-semiconductor work function potential difference. We know that, at threshold inversion point,  $V_G = V_{TN}$ . Since the surface potential for a P-type semiconductor is  $\Phi_s = 2\Phi_{fp}$ , the threshold voltage that creates the electron inversion layer charge is

$$V_{TN} = V_{oxT} + 2\Phi_{fp} + \Phi_{ms}$$

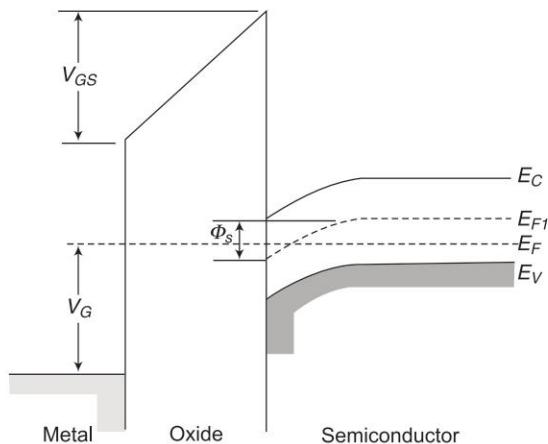
where  $V_{oxT}$  is the voltage across the oxide at the threshold inversion point.

This voltage  $V_{oxT}$  is related to the charge on the metal and oxide capacitance as given by

$$V_{oxT} = \frac{Q'_{mT}}{C_{ox}} = (|Q'_{SD}(\max)| - Q'_{ss}) \frac{1}{C_{ox}}$$



**Fig. 4.37** Charge distribution through the MOS capacitor for a P-type substrate



**Fig. 4.38** Energy-band diagram for MOSFET with a +ve gate bias,  $V_G$

where  $Q'_{mT} = (|Q'_{SD}(\max)| - Q'_{ss})$  and  $C_{ox}$  is the oxide capacitance per unit area. Therefore, the threshold voltage is

$$\begin{aligned} V_{TN} &= V_{oxT} + 2\Phi_{fp} + \Phi_{ms} \\ &= (|Q'_{SD}(\max)| - Q'_{ss}) \frac{1}{C_{ox}} + 2\Phi_{fp} + \Phi_{ms} \\ &= (|Q'_{SD}(\max)| - Q'_{ss}) \left( \frac{t_{ox}}{\epsilon_{ox}} \right) + 2\Phi_{fp} + \Phi_{ms} \end{aligned}$$

where  $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ . Hence, the threshold voltage is a function of semiconductor doping, oxide charge  $Q'_{ss}$  and oxide thickness  $t_{ox}$  for a given semiconductor material, oxide material, and gate metal.

The threshold voltage must be within the voltage range of a circuit design. If the threshold voltage of a MOSFET is beyond the operating voltage range, then the circuit cannot be turned ON and OFF.

### EXAMPLE 4.32

Consider an  $N^+$  polysilicon gate and a  $P$ -type silicon substrate doped to  $N_A = 3 \times 10^{22} \text{ m}^{-3}$ . Assume  $n_i = 1.5 \times 10^{16} \text{ m}^{-3}$ ,  $\Phi_{ms} = -1.13 \text{ V}$ ,  $\epsilon_s = 11.7$  for Si,  $\epsilon_{ox} = 3.9$  for  $\text{SiO}_2$  and  $Q'_{ss} = 10^{15} \text{ m}^{-2}$ . Determine the oxide thickness such that  $V_{TN} = 0.75 \text{ V}$ .

**Solution** The potential  $\Phi_{fp}$  for  $P$ -type semiconductor is

$$\Phi_{fp} = V_T \ln \left( \frac{N_A}{n_i} \right) = 26 \times 10^{-3} \times \ln \left( \frac{3 \times 10^{22}}{1.5 \times 10^{16}} \right) = 0.376 \text{ V}$$

The space charge width is

$$W_d = \left( \frac{2\epsilon_s \Phi_s}{qN_A} \right)^{1/2}$$

The space charge width is maximum when  $\Phi_s = 2\Phi_{fp}$  and it is given by

$$W_{dT} = \left( \frac{4\epsilon_s \Phi_{fp}}{qN_A} \right)^{1/2} = \left\{ \frac{4 \times 11.7 \times 8.854 \times 10^{-12} \times 0.376}{1.602 \times 10^{-19} \times 3 \times 10^{22}} \right\}^{1/2} = 0.18 \mu\text{m}$$

Therefore, the magnitude of the maximum space charge density is

$$\begin{aligned} |Q'_{SD}(\max)| &= qN_A W_{dT} \\ &= 1.602 \times 10^{-19} \times 3 \times 10^{22} \times 0.18 \times 10^{-6} \\ &= 8.65 \times 10^{-4} \text{ C/m}^2 \end{aligned}$$

The threshold voltage equation is

$$V_{TN} = (|Q'_{SD}(\max)| - Q'_{ss}) \left( \frac{t_{ox}}{\epsilon_{ox}} \right) + 2\Phi_{fp} + \Phi_{ms}$$

$$\begin{aligned} 0.75 &= \frac{[(8.65 \times 10^{-4}) - 10^{15} \times 1.602 \times 10^{-19}]}{3.9 \times 8.854 \times 10^{-12}} \times t_{ox} + 2(0.376) - 1.13 \\ &= 2.04 \times 10^7 \times t_{ox} - 0.248 \end{aligned}$$

Hence,

$$t_{ox} = \frac{0.75 + 0.248}{2.04 \times 10^7} = 0.4892 \times 10^{-7} \text{ m} = 48.92 \text{ nm}$$

### EXAMPLE 4.33

Calculate the threshold voltage of a MOSFET using the aluminum gate. Consider a *P*-type silicon substrate at  $T = 300 \text{ K}$  doped to  $N_A = 10^{20} \text{ m}^{-3}$ . Here,  $Q'_{ss} = 10^{14} \text{ m}^{-2}$  and  $t_{ox} = 5 \times 10^{-8} \text{ m}$ . Assume the oxide is silicon dioxide,  $n_i = 1.5 \times 10^{16} \text{ m}^{-3}$ ,  $\epsilon_s = 11.7$  and  $\Phi_{ms} = -1 \text{ V}$ .

#### Solution

We know that,

$$\begin{aligned} \Phi_{fp} &= V_T \ln\left(\frac{N_A}{n_i}\right) \\ &= 26 \times 10^{-3} \times \ln\left(\frac{10^{20}}{1.5 \times 10^{16}}\right) = 0.228 \text{ V} \end{aligned}$$

The maximum space charge width is

$$\begin{aligned} W_{dT} &= \left(\frac{4\epsilon_s \Phi_{fp}}{qN_A}\right)^{1/2} \\ &= \left\{\frac{4 \times 11.7 \times 8.854 \times 10^{-12} \times 0.228}{1.602 \times 10^{-19} \times 10^{20}}\right\}^{1/2} = 2.43 \mu\text{m} \end{aligned}$$

Therefore, the magnitude of the maximum space charge density is

$$\begin{aligned} |Q'_{SD}(\max)| &= qN_A W_{dT} \\ &= 1.602 \times 10^{-19} \times 10^{20} \times 2.43 \times 10^{-6} \\ &= 3.89 \times 10^{-5} \text{ C/m}^2 \end{aligned}$$

The threshold voltage can be calculated as

$$\begin{aligned} V_{TN} &= (|Q'_{SD}(\max)| - Q'_{ss}) \left(\frac{t_{ox}}{\epsilon_{ox}}\right) + 2\Phi_{fp} + \Phi_{ms} \\ &= [(3.89 \times 10^{-5}) - 10^{14} \times 1.602 \times 10^{-19}] \left[\frac{5 \times 10^{-8}}{3.9 \times 8.854 \times 10^{-12}}\right] + (2 \times 0.228) - 1 \\ &= -0.511 \text{ V} \end{aligned}$$

Since  $V_{TN}$  is negative for a *P*-type substrate, it implies that the device MOSFET is in depletion mode. The *P*-type substrate should be heavily doped to obtain an enhancement mode MOSFET.

**Temperature Effects** The threshold voltage  $V_{TN}$  or  $V_{TP}$  and conduction parameter  $K_N$  or  $K_P$  are functions of temperature. The magnitude of threshold voltage decreases with temperature and, hence, the drain current  $I_D$  increases with temperature at a given  $V_{GS}$ . The conduction parameter is directly proportional to mobility  $\mu_N$  or  $\mu_P$  of the carrier, which increases as the temperature decreases. Here, the temperature dependent of mobility is larger than that of the threshold voltage. Hence, the net effect of decreasing drain current at a given  $V_{GS}$  due to increase in temperature provides a negative feedback condition and hence the stability for a power MOSFET.

#### 4.17 COMPARISON OF MOSFET WITH JFET

1. In enhancement and depletion types of MOSFETs, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel. In the JFET, the transverse electric field across the reverse-biased *PN* junction controls the conductivity of the channel.
2. The gate-leakage current in a MOSFET is of the order of  $10^{-12}$  A. Hence, the input resistance of a MOSFET is very high in the order of  $10^{10}$  to  $10^{15}$   $\Omega$ . The gate-leakage current of a JFET is of the order of  $10^{-9}$  A and its input resistance is of the order of  $10^8$   $\Omega$ .
3. The output characteristics of the JFET are flatter than those of the MOSFET and, hence, the drain resistance of a JFET (0.1 to 1  $M\Omega$ ) is much higher than that of a MOSFET (1 to 50  $k\Omega$ ).
4. JFETs are operated only in the depletion mode. The depletion-type MOSFET may be operated in both depletion and enhancement mode.
5. Comparing to JFET, MOSFETs are easier to fabricate.
6. A MOSFET is very susceptible to overload voltage and needs special handling during installation. It gets damaged easily if it is not properly handled.
7. A MOSFET has zero offset voltage. As it is a symmetrical device, the source and drain can be interchanged. These two properties are very useful in analog signal switching.
8. Special digital CMOS circuits are available which involve near-zero power dissipation and very low voltage and current requirements. This makes them most suitable for portable systems.

MOSFETs are widely used in digital VLSI circuits than JFETs because of their advantages.

#### REVIEW QUESTIONS

1. What is a bipolar junction transistor? How are its terminals named?
2. Explain the operations of *NPN* and *PNP* transistors.
3. What are the different configurations of BJT?
4. Explain the input and output characteristics of a transistor in CB configuration.
5. Explain the Early effect and its consequences.
6. Derive the relationship between  $\alpha$  and  $\beta$ .
7. Why does the CE configuration provide large current amplification while the CB configuration does not?
8. Draw the circuit diagram of an *NPN* junction transistor CE configuration and describe the static input and output characteristics. Also, define active, saturation and cut-off regions, and saturation resistance of a CE transistor.
9. How will you determine *h*-parameters from the characteristics of CE configuration?

10. Determine the  $h$ -parameters from the characteristics of CB configuration.
11. What is the relation between  $I_B$ ,  $I_E$  and  $I_C$  in CB configuration?
12. Explain the laboratory setup for obtaining the CC characteristics.
13. Compare the performance of a transistor in different configurations.
14. Define  $\alpha$ ,  $\beta$ , and  $\gamma$  of a transistor. Show how they are related to each other.
15. Explain how a transistor is used as an amplifier.
16. From the characteristics of CE configuration, explain the large signal, dc, and small signal CE values of current gain.
17. Calculate the values of  $I_C$  and  $I_E$  for a transistor with  $\alpha_{dc} = 0.99$  and  $I_{CBO} = 5 \mu A$ .  $I_B$  is measured as  $20 \mu A$ . [Ans.  $I_C = 2.48 \text{ mA}$ ,  $I_E = 2.5 \text{ mA}$ ]
18. If  $\alpha_{dc} = 0.99$  and  $I_{CBO} = 50 \mu A$ , find emitter current. [Ans.  $I_C = 104 \text{ mA}$ ,  $I_E = 105 \text{ mA}$ ]
19. If  $I_C$  is 100 times larger than  $I_B$ , find the value of  $\beta_{dc}$ . [Ans. 100]
20. Find the value of  $\alpha_{dc}$ , if  $\beta_{dc}$  is equal to 100. [Ans. 0.99]
21. Find the voltage gain of a transistor amplifier if its output is  $5 \text{ V rms}$  and the input is  $100 \text{ mV rms}$ . [Ans. 50]
22. Find the value of  $\alpha_{dc}$ , when  $I_C = 8.2 \text{ mA}$  and  $I_E = 8.7 \text{ mA}$ . [Ans. 0.943]
23. If  $\alpha_{dc}$  is 0.96 and  $I_E = 9.35 \text{ mA}$ , determine  $I_C$ . [Ans. 8.98 mA]
24. Describe the two types of breakdown in transistors.
25. Draw the Ebers–Moll model for a PNP transistor and give the equations for emitter current and collector current.
26. Describe with neat diagrams the operation of a phototransistor and state its applications.
27. With output characteristics, explain how phototransistor responds to the incident light.
28. Why is a Field Effect Transistor called so?
29. Explain the construction of  $N$  channel JFET.
30. With the help of neat sketches and characteristic curves, explain the operation of the junction FET.
31. How does the FET behave for small and large values of  $|V_{DS}|$ ?
32. Define the pinch-off voltage  $V_P$ . Sketch the depletion region before and after pinch-off.
33. Explain the four distinct regions of the output characteristics of a JFET.
34. Define and explain the parameters transconductance  $g_m$ , drain resistance  $r_d$  and amplification factor  $\mu$  of a JFET. Establish the relation between them.
35. Assuming that the saturation drain current  $I_{DS}$  is given by the parabolic relation

$$I_{DS} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

Prove that the transconductance  $g_m$  is given by

$$g_m = g_{mo} \left( 1 - \frac{V_{GS}}{V_P} \right) = -\frac{2}{V_P} \sqrt{I_{DS} I_{DSS}}$$

where  $g_{mo}$  is the value of  $g_m$  for  $V_{GS} = 0$ .

36. Explain how the transconductance of a JFET varies with drain current and gate voltage.
37. What are the relative merits of an  $N$ -channel and  $P$ -channel FET?
38. Compare JFET with BJT.
39. Explain why BJTs are called bipolar devices while FETs are called unipolar devices.
40. Explain why a low-power FET is called a square-law device.
41. Briefly describe some applications of JFET.

42. A certain JFET operates in the linear region with a constant drain voltage of 1 V. When the gate voltage is 2 V, a drain current of 10 mA flows, but when the gate voltage is changed to 1 V, the drain current becomes 22.8 mA. Find (i) the pinch-off voltage of the device, and (ii) the channel resistance for zero gate voltage.

[Ans. 3 V, 18.6 Ω].

43. Show that if a JFET is operated at sufficiently low drain voltage, it behaves as a resistance  $R$  given approximately by

$$R = \frac{R_o}{1 - \left( \frac{V_{GS}}{V_p} \right)^{1/2}}$$

where  $R_o$  is the channel resistance for zero gate voltage.

44. What is a MOSFET? How many types of MOSFETs are there?  
 45. With the help of suitable diagrams, explain the working of different types of MOSFET.  
 46. How does the constructional feature of a MOSFET differ from that of a JFET?  
 47. Explain qualitatively the shapes of the  $I_D$  versus  $V_{DS}$  and  $I_D$  versus  $V_{GS}$  characteristics for the three types of FETs.  
 48. What is channel-length modulation in MOSFET? Obtain the output resistance at the  $Q$ -point.  
 49. Define threshold voltage.  
 50. Explain the threshold voltage concept in MOSFET.  
 51. Derive the expression for threshold voltage in MOSFET.  
 52. Using depletion-mode drain current equation, derive the expression for JFET drain current in enhancement mode.

### OBJECTIVE-TYPE QUESTIONS

- Which of the following statements is correct for basic transistor amplifier configurations?  
 (a) CB amplifier has low input impedance and a low current gain.  
 (b) CC amplifier has low output impedance and a low current gain.  
 (c) CE amplifier has very poor voltage gain but very high input impedance
- For a BJT, the common-base current gain  $\alpha = 0.98$  and the collector-base junction reverse-bias saturation current  $I_{CO} = 0.6 \mu\text{A}$ . This BJT is connected in the common-emitter mode and operated in the active region with a base drive current  $I_B = 20 \mu\text{A}$ . The collector current  $I_C$  for this mode of operation is  
 (a) 0.98 mA      (b) 0.99 mA      (c) 1.0 mA      (d) 1.01 mA
- In most transistors, the collector region is made physically larger than the emitter region  
 (a) for dissipating heat      (b) to distinguish it from other regions  
 (c) as it is sensitive to ultraviolet rays      (d) to reduce resistance in the path of flow of electrons
- As temperature is increased, the  $h$ -parameters  $h_{ie}$ ,  $h_{re}$ ,  $h_{fe}$  and  $h_{oe}$  of a transistor  
 (a) decrease      (b) increase      (c) remain constant      (d) none
- The biasing method which is considered independent of transistor  $\beta_{dc}$  is  
 (a) fixed biasing      (b) collector feedback bias  
 (c) voltage-divider bias      (d) base bias with collector feedback
- The power gain of a CB amplifier is approximately equal to  
 (a) current gain      (b) voltage gain      (c) both (a) and (b)      (d) none of the above
- The following is a non-inverting amplifier with voltage gain exceeding unity.  
 (a) CE amplifier      (b) CB amplifier      (c) CC amplifier      (d) None of the above

8. The voltage gain of a CB amplifier has the same magnitude as that of  
 (a) CE amplifier   (b) CC amplifier  
 (c) both CE and CC amplifiers                         (d) none of the above
9. An amplifier has good voltage, current, and power gains and the input resistance is low. It is  
 (a) common-base   (b) common-emitter  
 (c) common-collector                                     (d) none
10. The transistor configuration which provides highest output impedance is  
 (a) common base   (b) common emitter  
 (c) common collector                                     (d) none of the above
11. When a healthy *NPN* transistor is connected to an ohmmeter such that the base terminal is connected to the red lead of the meter and the emitter terminal to the black lead, then the meter shows  
 (a) an open circuit   (b) some medium resistance  
 (c) a very small resistance                                 (d) none of the above
12. For  $\alpha = 0.9$ , the value of  $\beta$  is  
 (a) 9.9   (b) 49   (c) 99   (d) 100
13. A BJT is said to be operating in the saturation region, if  
 (a) both junctions are reverse biased  
 (b) base-emitter junction is reverse biased and base collector junction is forward biased  
 (c) base-emitter junction is forward biased and base-collector junction reverse biased  
 (d) both the junctions are forward biased
14. For an *NPN* bipolar transistor, what is the main stream of current in the base region?  
 (a) Drift of holes   (b) Diffusion of holes  
 (c) Drift of electrons   (d) Diffusion of electrons
15. In saturation region in an *NPN* transistor,  
 (a)  $V_{CB}$  is  $-ve$  and  $V_{BE}$  is  $+ve$                              (b)  $V_{CB}$  is  $+ve$  and  $V_{BE}$  is  $-ve$   
 (c) both  $V_{CB}$  and  $V_{BE}$  are  $+ve$                                  (d) both  $V_{CB}$  and  $V_{BE}$  are  $-ve$
16. The Ebers-Moll model is applicable to  
 (a) bipolar junction transistors                             (b) NMOS transistors  
 (c) unipolar junction transistors                          (d) junction field-effect
17. The Early effect in a bipolar junction transistor is caused by  
 (a) fast-turn-on   (b) fast-turn-off  
 (c) large collector-base reverse bias                     (d) large emitter-base forward bias
18. Which of the following statements is true?  
 (a) FET and BJT, both are unipolar                      (b) FET and BJT, both are bipolar  
 (c) FET is bipolar and BJT is unipolar                     (d) FET is unipolar and BJT is bipolar
19. An FET has  
 (a) very high input resistance                              (b) very low input resistance  
 (c) high connection emitter junction                     (d) forward-biased *PN* junction
20. The drain source voltage at which drain current becomes nearly constant is called  
 (a) barrier voltage   (b) breakdown voltage  
 (c) pick-off-voltage   (d) pinch-off-voltage
21. The main factor which makes a MOSFET likely to breakdown during normal handling is its  
 (a) very low gate capacitance                              (b) high leakage current  
 (c) high input resistance                                     (d) both (a) and (c)
22. In an *N*-channel JFET,  
 (a) the current carriers are holes                             (b) the current carriers are electrons  
 (c)  $V_{GS}$  is positive   (d) the input resistance is very low
23. The magnitude of the current source in the ac equivalent circuit of an FET depends on  
 (a) the dc supply voltage                                     (b)  $V_{DS}$   
 (c) externally drain resistance                                 (d) transconductance and gate to source voltage

24. A CMOS amplifier, when compared to an *N*-channel MOSFET, has the advantage of  
(a) higher cut-off frequency  
(b) higher voltage gain  
(c) higher current gain  
(d) lower current drain from the power supply, thereby less dissipation
25. A junction FET can be used as a voltage variable resistor  
(a) at pinch-off condition (b) beyond pinch-off voltage  
(c) well below pinch-off condition (d) for any value of  $V_{DS}$
26. Which of the following devices is used in the microprocessors?  
(a) JEET (b) BJT (c) MOSFET (d) CMOS
27. The MOSFET switch in its ON-state may be considered as equivalent to  
(a) resistor (b) inductor (c) capacitor (d) battery
28. The pinch-off voltage for a *N*-channel JFET is 4 V. When  $V_{GS} = 1$  V, the  $|V_{DS(\min)}|$  at which the pinch-off occurs is equal to  
(a) 3 V (b) 5 V (c) 4 V (d) 1 V
29. In an *N*-channel JFET,  $V_{GS}$  is held constant.  $V_{DS}$  is less than the breakdown voltage. As  $V_{DS}$  is increased,  
(a) conducting cross-sectional area of the channel  
(b) '*S*' decreases and '*J*' decreases; '*S*' and the channel current density '*J*' both increase  
(c) '*S*' decreases and '*J*' increase  
(d) '*S*' increases and '*J*' decreases
30. In MOSFET devices, the *N*-channel type is better than the *P*-channel in the following respects:  
(a) It has better noise immunity (b) It is faster  
(c) It is TTL compatible (d) It has better drive capability
31. The 'pinch-off' voltage of a JFET is 5.0 volt, its 'cut-off' voltage is  
(a)  $(5.0)^{\frac{1}{2}} V$  (b) 2.5 V (c) 5.0 V (d)  $(5.0)^{\frac{2}{3}} V$
32. Which of the following effects can be caused by a rise in the temperature?  
(a) Increase in MOSFET current ( $I_{DS}$ ) (b) Increase in BJT current ( $I_C$ )  
(c) Decrease in MOSFET current ( $I_{DS}$ ) (d) Decrease in BJT current ( $I_C$ )
33. An *N*-channel JFET has  $I_{DSS} = 2$  mA and  $V_p = -4$  V. Its transconductance  $g_m$  (in mA/V) for an applied GATE to source voltage  $V_{GS}$  of -2 V is  
(a) 0.25 (b) 0.5 (c) 0.75 (d) 1.0
34. MOSFET can be used as a  
(a) current-controlled capacitor (b) voltage-controlled capacitor  
(c) current-controlled inductor (d) voltage-controlled inductor
35. The effective channel length of a MOSFET in saturation decreases with increase in  
(a) gate voltage (b) drain voltage (c) source voltage (d) body voltage
36. The drain of an *N*-channel MOSFET is shorted to the gate so that  $V_{GS} = V_{DS}$ . The threshold voltage ( $V_T$ ) of MOSFET is 1 V. If the drain current  $I_D$  is 1 mA for  $V_{GS} = 2$  V, then for  $V_{GS} = 3$  V,  $I_D$  is  
(a) 2 mA (b) 3 mA (c) 9 mA (d) 4 mA



# Transistor Biasing and Thermal Stabilization

## 5.1 INTRODUCTION

---

The quiescent operating point of a transistor amplifier should be established in the active region of its characteristics. Since the transistor parameters such as  $\beta$ ,  $I_{CO}$  and  $V_{BE}$  are functions of temperature, the operating point shifts with changes in temperature. The stability of different methods of biasing transistor (BJT, FET and MOSFET) circuits and compensation techniques for stabilizing the operating point are discussed in this chapter.

## 5.2 NEED FOR BIASING

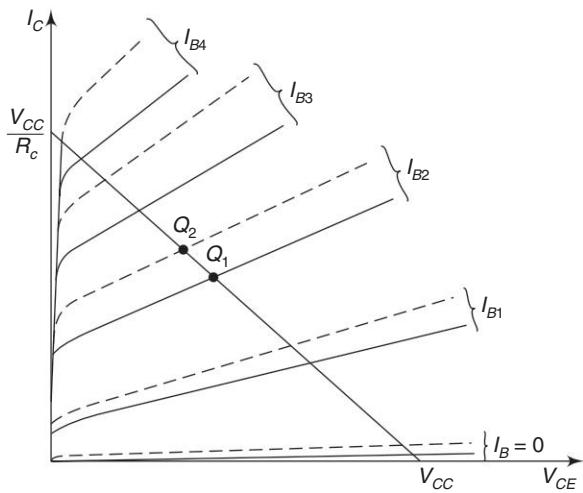
---

In order to produce distortion-free output in amplifier circuits, the supply voltages and resistances in the circuit must be suitably chosen. These voltages and resistances establish a set of dc voltage  $V_{CEO}$  and current  $I_{CQ}$  to operate the transistor in the active region. These voltages and currents are called *quiescent values* which determine the *operating point* or *Q-point* for the transistor. The process of giving proper supply voltages and resistances for obtaining the desired *Q-point* is called *biasing*. The circuits used for getting the desired and proper operating point are known as *biasing circuits*.

The collector current for a common-emitter amplifier is expressed by

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (1 + \beta)I_{CO}$$

Here, the three variables  $h_{FE}$ , i.e.,  $\beta$ ,  $I_B$ , and  $I_{CO}$  are found to increase with temperature. For every  $10^\circ\text{C}$  rise in temperature,  $I_{CO}$  doubles itself. When  $I_{CO}$  increases,  $I_C$  increases significantly. This causes power dissipation to increase and hence, to make  $I_{CO}$  increase. This will cause  $I_C$  to increase further and the process becomes cumulative which will lead to thermal runaway that will destroy the transistor. In addition, the quiescent operating point can shift due to temperature changes and the transistor can be driven into the region of saturation. The effect of  $\beta$  on the *Q-point* is shown in Fig. 5.1. One more source of bias instability to be considered is due to the variation of  $V_{BE}$  with temperature.  $V_{BE}$  is about 0.6 V for a silicon transistor and 0.2 V for a germanium transistor at room temperature. As the temperature increases,  $|V_{BE}|$  decreases at the rate of 2.5 mV/ $^\circ\text{C}$  for both silicon and germanium transistors. The transfer-characteristic curve shifts to the left at the rate of 2.5 mV/ $^\circ\text{C}$  (at constant  $I_C$ ) for increasing temperature and, hence, the operating point shifts accordingly. To establish the operating point in the active region, compensation techniques are needed.



**Fig. 5.1** Effect of  $\beta$  on  $Q$ -point

## 5.3 LOAD LINE ANALYSIS

### 5.3.1 dc Load Line

Referring to the biasing circuit of Fig. 5.2(a), the values of  $V_{CC}$  and  $R_C$  are fixed and  $I_C$  and  $V_{CE}$  are dependent on  $R_B$ .

Applying Kirchhoff's voltage law to the collector circuit in Fig. 5.2(a), we get  $V_{CC} = I_C R_C + V_{CE}$ .

The straight line represented by  $AB$  in Fig. 5.2(b) is called the dc *load line*. The coordinates of the end point  $A$  are obtained by substituting  $V_{CE} = 0$  in the above equation. Then  $I_C = \frac{V_{CC}}{R_C}$ . Therefore, the coordinates of  $A$  are  $V_{CE} = 0$  and  $I_C = \frac{V_{CC}}{R_C}$ .

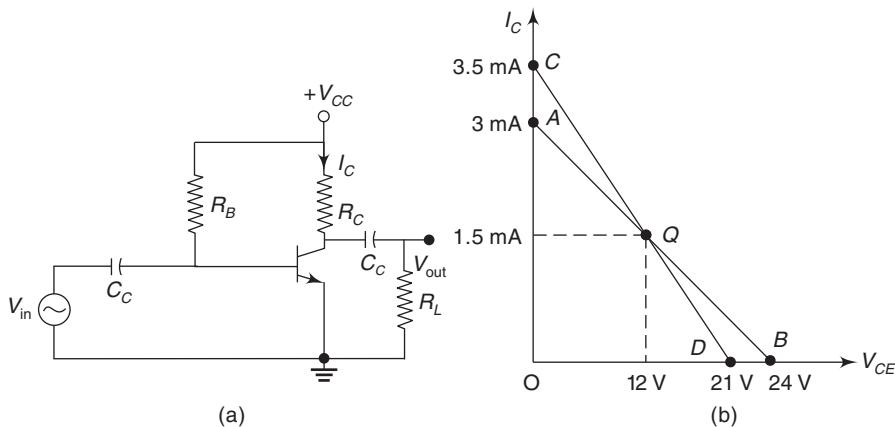
The coordinates of  $B$  are obtained by substituting  $I_C = 0$  in the above equation. Then  $V_{CE} = V_{CC}$ . Therefore, the coordinates of  $B$  are  $V_{CE} = V_{CC}$  and  $I_C = 0$ . Thus, the dc load line  $AB$  can be drawn if the values of  $R_C$  and  $V_{CC}$  are known.

As shown in Fig. 5.2(b), the optimum  $Q$ -point is located at the midpoint of the dc load line  $AB$  between the saturation and cut-off regions, i.e.,  $Q$  is exactly midway between  $A$  and  $B$ . In order to get faithful amplification, the  $Q$ -point must be well within the active region of the transistor.

Even though the  $Q$ -point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the  $Q$ -point shifts nearer to either  $A$  or  $B$ , the output voltage and current get clipped, thereby output signal is distorted.

In practice, the  $Q$ -point tends to shift its position due to any or all of the following three main factors:

- Reverse saturation current,  $I_{CO}$ , which doubles for every  $10^\circ\text{C}$  increase in temperature.
- Base-emitter voltage,  $V_{BE}$ , which decreases by  $2.5\text{ mV per }^\circ\text{C}$ .
- Transistor current gain,  $\beta$ , i.e.,  $h_{FE}$  which increases with temperature.



**Fig. 5.2** (a) Biasing circuit (b) CE output characteristics and load line

Referring to Fig. 5.2(a), the base current \$I\_B\$ is kept constant since \$I\_B\$ is approximately equal to \$V\_{CC}/R\_B\$. If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as \$\beta\$ vary over a range. This results in the variation of collector current \$I\_C\$ for a given \$I\_B\$. Hence, in the output characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the \$Q\$-point to a location which might be completely unsatisfactory.

### 5.3.2 ac Load Line

After drawing the dc load line, the operating point \$Q\$ is properly located at the center of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence, the ac load line should also pass through the operating point \$Q\$. The effective ac load resistance, \$R\_{ac}\$, is the combination of \$R\_C\$ parallel to \$R\_L\$, i.e., \$R\_{ac} = R\_C \parallel R\_L\$. So the slope of the ac load line \$CQD\$ will be  $\left( -\frac{1}{R_{ac}} \right)$ .

To draw an ac load line, two end points, viz., maximum \$V\_{CE}\$ and maximum \$I\_C\$ when the signal is applied are required.

Maximum \$V\_{CE} = V\_{CEQ} + I\_{CQ} R\_{ac}\$, which locates the point \$D(OD)\$ on the \$V\_{CE}\$ axis.

Maximum \$I\_C = I\_{CQ} + \frac{V\_{CEQ}}{R\_{ac}}\$, which locates the point \$C(OC)\$ on the \$I\_C\$ axis.

By joining points \$C\$ and \$D\$, ac load line \$CD\$ is constructed. As \$R\_C > R\_{ac}\$, the dc load line is less steep than the ac load line.

When the signal is zero, we have the exact dc conditions. From Fig. 5.2(b), it is clear that the intersection of dc and ac load lines is the operating point \$Q\$.

**Voltage Swing Limitations** In a linear amplifier, symmetrical sinusoidal signals at the input gets amplified as sinusoidal signal at the output, without any clipping. The maximum output symmetrical swing provided by the amplifier can be obtained from the ac load line. The output signal will be clipped if it exceeds this limit, resulting in signal distortion.

### EXAMPLE 5.1

Determine the maximum voltage swing at the output of common emitter amplifier in which the quiescent point is  $I_{CQ} = 0.9 \text{ mA}$  and  $V_{CEQ} = 9 \text{ V}$ . The ac resistance seen at the output terminal is  $R_{ac} = (R_C \parallel R_L) = 2\text{k}\Omega$ .

**Solution** The maximum symmetrical peak to peak ac collector current is

$$\Delta i_C = 2 I_{CQ} = 2 \times 0.9 \text{ mA} = 1.8 \text{ mA}$$

The maximum symmetrical peak to peak output voltage is

$$|\Delta v_{EC}| = |\Delta i_C| R_{ac} = 1.8 \times 10^{-3} \times 2 \times 10^3 = 3.6 \text{ V}$$

### EXAMPLE 5.2

In the transistor amplifier shown in Fig. 5.2(a),  $R_C = 8 \text{ k}\Omega$ ,  $R_L = 24 \text{ k}\Omega$  and  $V_{CC} = 24 \text{ V}$ . Draw the dc load line and determine the optimum operating point. Also draw the ac load line.

**Solution**

- (a) *dc load line:* Referring to Fig. 5.2(a), we have  $V_{CC} = V_{CE} + I_C R_C$ .

For drawing the dc load line, the two end points, viz., maximum  $V_{CE}$  point (at  $I_C = 0$ ) and maximum  $I_C$  point (at  $V_{CE} = 0$ ) are required.

$$\text{Maximum } V_{CE} = V_{CC} = 24 \text{ V}$$

$$\text{Maximum } I_C = \frac{V_{CC}}{R_C} = \frac{24}{8 \times 10^3} = 3 \text{ mA}$$

Therefore, the dc load line  $AB$  is drawn with the point  $B$  ( $OB = 24 \text{ V}$ ) on the  $V_{CE}$  axis and the point  $A$  ( $OA = 3 \text{ mA}$ ) on the  $I_C$  axis, as shown in Fig. 5.2(b).

- (b) For fixing the optimum operating point  $Q$ , mark the middle of the dc load line  $AB$  and the corresponding  $V_{CE}$  and  $I_C$  values can be found.

$$\text{Here, } V_{CEQ} = \frac{V_{CC}}{2} = 12 \text{ V} \quad \text{and} \quad I_{CQ} = 1.5 \text{ mA}$$

- (c) *ac load line:* To draw an ac load line, two end points, viz., maximum  $V_{CE}$  and maximum  $I_C$  when the signal is applied, are required.

$$\text{The ac load, } R_{ac} = R_C \parallel R_L = \frac{8 \times 24}{8 + 24} = 6 \text{ k}\Omega$$

$$\begin{aligned} \text{Maximum } V_{CE} &= V_{CEQ} + I_{CQ} R_{ac} \\ &= 12 + 1.5 \times 10^{-3} \times 6 \times 10^3 = 21 \text{ V} \end{aligned}$$

This locates the point  $D$  ( $OD = 21 \text{ V}$ ) on the  $V_{CE}$  axis.

$$\text{Maximum collector current} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = 1.5 \times 10^{-3} + \frac{12}{6 \times 10^3} = 3.5 \text{ mA}$$

This locates the point  $C$  ( $OC = 3.5$  mA) on the  $I_C$  axis. By joining points  $C$  and  $D$ , the ac load line  $CD$  is constructed.

### EXAMPLE 5.3

For the transistor amplifier shown in Fig. 5.3(a),  $V_{CC} = 12$  V,  $R_1 = 8$  k $\Omega$ ,  $R_2 = 4$  k $\Omega$ ,  $R_C = 1$  k $\Omega$ ,  $R_E = 1$  k $\Omega$  and  $R_L = 1.5$  k $\Omega$ . Assume  $V_{BE} = 0.7$  V. (a) Draw the dc load line, (b) determine the operating point, and (c) draw the ac load line.

#### Solution

- (a) *dc load line:* Referring to Fig. 5.3(a), we have  $V_{CC} = V_{CE} + I_C(R_C + R_E)$ .

To draw the dc load line, we need two end points, viz., maximum  $V_{CE}$  point (at  $I_C = 0$ ) and maximum  $I_C$  point (at  $V_{CE} = 0$ ).

Maximum  $V_{CE} = V_{CC} = 12$  V, which locates the point  $B$  ( $OB = 12$  V) of the dc load line.

$$\text{Maximum } I_C = \frac{V_{CC}}{R_C + R_E} = \frac{12}{(1+1) \times 10^3} = 6 \text{ mA}$$

This locates the point  $A$  ( $OA = 6$  mA) of the dc load line. Figure 5.3(b) shows the dc load line  $AB$ , with (12 V, 6 mA).

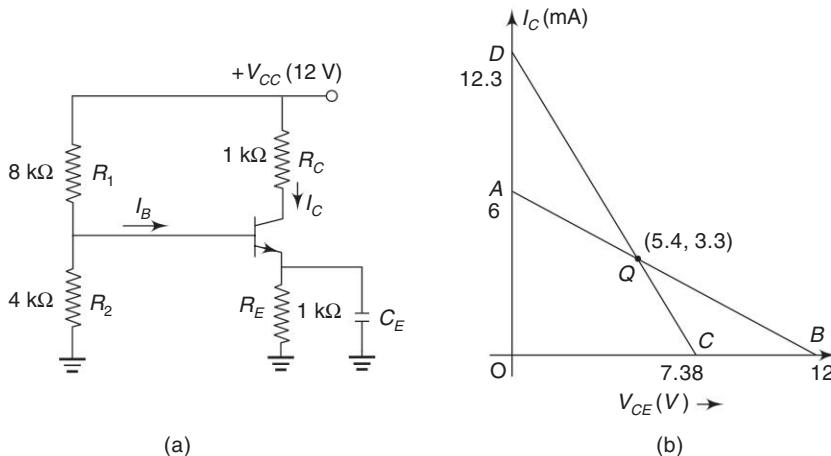


Fig. 5.3

- (b) *Operating point Q*

The voltage across  $R_2$  is  $V_2 = \frac{R}{R_1 + R_2} V_{CC}$

Therefore,  $V_2 = \frac{4 \times 10^3}{12 \times 10^3} \times 12 = 4$  V

$$V_2 = V_{BE} + I_E R_E$$

Therefore,

$$I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{4 - 0.7}{1 \times 10^3} = 3.3 \text{ mA}$$

$$I_C \approx I_E = 3.3 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 12 - 3.3 \times 10^{-3} \times 2 \times 10^3 = 5.4 \text{ V}$$

Therefore, the operating point  $Q$  is at 5.4 V and 3.3 mA, which is shown on the dc load line.

- (c) *ac load line*: To draw the ac load line, we need two end points, viz., maximum  $V_{CE}$  and maximum  $I_C$  when signal is applied.

$$\text{ac load, } R_{ac} = R_C \parallel R_L = \frac{1 \times 1.5 \text{ k}\Omega}{2.5} = 0.6 \text{ k}\Omega$$

$$\text{Therefore, maximum } V_{CE} = V_{CEQ} + I_{CQ} R_{ac} = 5.4 + 3.3 \times 10^{-3} \times 0.6 \times 10^3 = 7.38 \text{ V}$$

This locates the point  $C$  ( $OC = 7.38 \text{ V}$ ) on the  $V_{CE}$  axis.

$$\text{Maximum } I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = 3.3 \times 10^{-3} + \frac{5.4}{0.6 \times 10^3} = 12.3 \text{ mA}$$

This locates the point  $D$  ( $OD = 12.3 \text{ mA}$ ) on the  $I_C$  axis. By joining points  $C$  and  $D$ , the ac load line  $CD$  is constructed.

### EXAMPLE 5.4

Design the circuit shown in Fig. 5.4, given Q-point values are to be  $I_{CQ} = 1 \text{ mA}$  and  $V_{CEQ} = 6 \text{ V}$ . Assume that  $V_{CC} = 10 \text{ V}$ ,  $\beta = 100$  and  $V_{BE(on)} = 0.7 \text{ V}$ .

**Solution** The collector resistance is

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{10 - 6}{1 \times 10^{-3}} = 4 \text{ k}\Omega$$

The base current is

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1 \times 10^{-3}}{100} = 10 \mu\text{A}$$

The base resistance is

$$R_B = \frac{V_{CC} - V_{BE(on)}}{I_{BQ}} = \frac{10 - 0.7}{10 \times 10^{-6}} = 0.93 \text{ M}\Omega$$

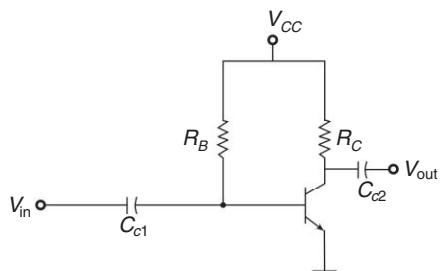


Fig. 5.4

### EXAMPLE 5.5

Determine the characteristics of a circuit shown in Fig. 5.5. Assume that  $\beta = 100$  and  $V_{BE(on)} = 0.7 \text{ V}$ .

**Solution** Referring to Fig. 5.5, Kirchhoff's voltage law equation is

$$V_{BB} = I_B R_B + V_{BE(on)} + I_E R_E$$

We know that,

$$I_E = I_B + I_C = I_B + \beta I_B = (1 + \beta) I_B$$

$$\begin{aligned} \text{The base current } I_B &= \frac{V_{BB} - V_{BE(on)}}{R_B + (1 + \beta) R_E} \\ &= \frac{5 - 0.7}{20 \times 10^3 + 101 \times 600} = 53.34 \mu\text{A} \end{aligned}$$

$$\begin{aligned} \text{Therefore, } I_C &= \beta I_B = 100 \times 53.34 \times 10^{-6} \\ &= 5.334 \text{ mA} \end{aligned}$$

$$\begin{aligned} I_E &= I_C + I_B = 5.334 \times 10^{-3} + 53.34 \times 10^{-6} \\ &= 5.38734 \text{ mA} \end{aligned}$$

$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_C - I_E R_E \\ &= 10 - 5.334 \times 10^{-3} \times 400 - 5.38734 \times 10^{-3} \times 600 = 4.634 \text{ V} \end{aligned}$$

The  $Q$  point is at  $V_{CEO} = 4.634 \text{ V}$  and  $I_{CO} = 5.334 \text{ mA}$

**Stability Factor (S)** The extent to which the collector current  $I_C$  is stabilized with varying  $I_{CO}$  is measured by a stability factor  $S$ . It is defined as the rate of change of collector current  $I_C$  with respect to the collector-base leakage current  $I_{CO}$ , keeping both the current  $I_B$  and the current gain  $\beta$  constant.

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}, \beta \text{ and } I_B \text{ constant} \quad (5.1)$$

The collector current for a CE amplifier is given by

$$I_C = \beta I_B + (\beta + 1) I_{CO} \quad (5.2)$$

Differentiating Eq. (5.2) with respect to  $I_C$ , we get

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

$$\text{Therefore, } \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta + 1)}{S}$$

$$S = \frac{1 + \beta}{1 - \beta \left( \frac{dI_B}{dI_C} \right)} \quad (5.3)$$

From this equation, it is clear that this factor  $S$  should be as small as possible to have better thermal stability.

**Stability Factors  $S'$  and  $S''$**  The stability factor  $S'$  is defined as the rate of change of  $I_C$  with  $V_{BE}$ , keeping  $I_{CO}$  and  $\beta$  constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}$$

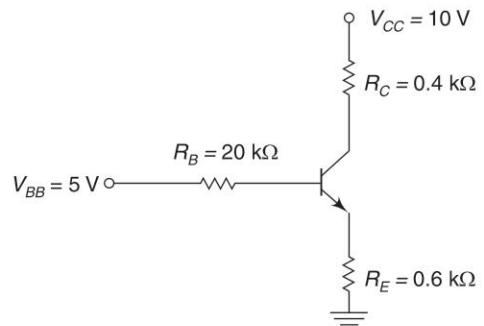


Fig. 5.5

The stability factor  $S''$  is defined as the rate of change of  $I_C$  with respect to  $\beta$ , keeping  $I_{CO}$  and  $V_{BE}$  constant.

$$S'' = \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta}$$

## 5.4 BJT BIASING – METHODS AND BASIC STABILITY

The stability factors for some commonly used biasing circuits are discussed here.

### 5.4.1 Fixed Bias or Base Resistor Method

A common-emitter amplifier using a fixed-bias circuit is shown in Fig. 5.6. The dc analysis of the circuit yields the following equation.

$$V_{CC} = I_B R_B + V_{BE} \quad (5.4)$$

Therefore,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Since this equation is independent of the current  $I_C$ ,  $dI_B/dI_C = 0$  and the stability factor given in Eq. (5.3) reduces to

$$S = 1 + \beta$$

Since  $\beta$  is a large quantity, this is a very poor bias stable circuit. Therefore, in practice, this circuit is not used for biasing the base.

The advantages of this method are (i) simplicity, (ii) small number of components required, and (iii) if the supply voltage is very large as compared to  $V_{BE}$  of the transistor, then the base current becomes largely independent of the voltage  $V_{BE}$ .

### EXAMPLE 5.6

In the fixed-bias compensation method shown in Fig. 5.7, a silicon transistor with  $\beta = 100$  is used.  $V_{CC} = 6$  V,  $R_C = 3 \text{ k}\Omega$ ,  $R_B = 530 \text{ k}\Omega$ . Draw the dc load line and determine the operating point. What is the stability factor?

**Solution**

(a) *dc load line*

$$V_{CE} = V_{CC} - I_C R_C$$

When  $I_C = 0$ ,

$$V_{CE} = V_{CC} = 6 \text{ V}$$

When  $V_{CE} = 0$ ,

$$I_C = \frac{V_{CC}}{R_C} = \frac{6}{3 \times 10^3} = 2 \text{ mA}$$

(b) *Operating point Q*

For a silicon transistor,  $V_{BE} = 0.7 \text{ V}$

$$V_{CC} = I_B R_B + V_{BE}$$

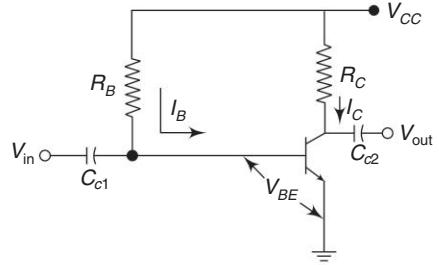


Fig. 5.6 Fixed bias circuit

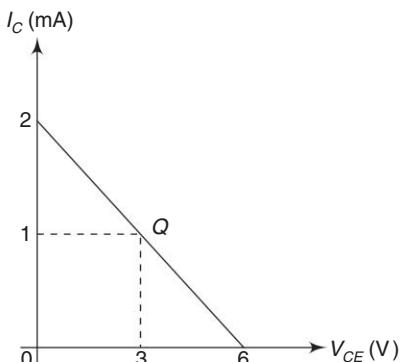


Fig. 5.7

Therefore,  $I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{6 - 0.7}{530 \times 10^3} = 10 \text{ mA}$

Therefore,  $I_C = \beta I_B = 100 \times 10 \times 10^{-6} = 1 \text{ mA}$

$$V_{CE} = V_{CC} - I_C R_C = 6 - 1 \times 10^{-3} \times 3 \times 10^3 = 3 \text{ V}$$

Therefore operating point is  $V_{CEQ} = 3 \text{ V}$  and  $I_{CQ} = 1 \text{ mA}$ .

(c) Stability factor  $S = 1 + \beta = 1 + 100 = 101$

### EXAMPLE 5.7

Find the collector current and collector-to-emitter voltage for the given circuit as shown in Fig. 5.8.

**Solution** For a silicon transistor,  $V_{BE} = 0.7 \text{ V}$

Base current  $I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{9 - 0.7}{300 \times 10^3} = 27.67 \mu\text{A}$

Collector current  $I_C = \beta I_B = 50 \times 27.67 \times 10^{-6} = 1.38 \text{ mA}$

Collector-to-emitter voltage

$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_C \\ &= 9 - 1.38 \times 10^{-3} \times 2 \times 10^3 = 6.24 \text{ V} \end{aligned}$$

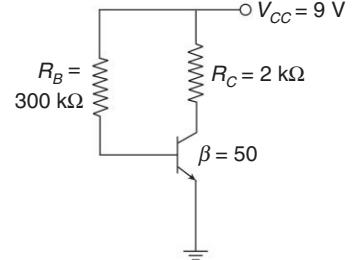


Fig. 5.8

### EXAMPLE 5.8

A germanium transistor having  $\beta = 100$  and  $V_{BE} = 0.2 \text{ V}$  is used in a fixed-bias amplifier circuit where  $V_{CC} = 16 \text{ V}$ ,  $R_C = 5 \text{ k}\Omega$  and  $R_B = 790 \text{ k}\Omega$ . Determine its operating point.

**Solution** For a germanium transistor,  $V_{BE} = 0.2 \text{ V}$

Applying KVL to the base circuit, we have

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Therefore,  $I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{16 - 0.2}{790 \times 10^3} = 20 \mu\text{A}$

$$I_C = \beta I_B = 100 \times 20 \mu\text{A} = 2 \text{ mA}$$

Applying KVL to the collector circuit, we have

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C = 16 - 2 \times 10^{-3} \times 5 \times 10^3 = 6 \text{ V}$$

Hence, the operating point is  $I_C = 2 \text{ mA}$  and  $V_{CE} = 6 \text{ V}$ .

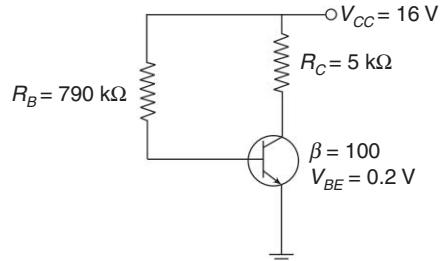


Fig. 5.9

### EXAMPLE 5.9

The circuit as shown in Fig. 5.10 has fixed bias using an *NPN* transistor. Determine the value of base current, collector current, and collector-to-emitter voltage.

**Solution** Applying KVL to the base circuit, we have

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Therefore,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{25 - 0.7}{180 \times 10^3} = 135 \mu\text{A}$$

$$I_C = \beta I_B = 80 \times 135 \times 10^{-6} = 10.8 \text{ mA}$$

Applying KVL to the collector circuit, we have

$$V_{CC} - I_C R_C - V_{CE} = 0$$

Therefore,

$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_C \\ &= 25 - 10.8 \times 10^{-3} \times 820 = 16.144 \text{ V} \end{aligned}$$

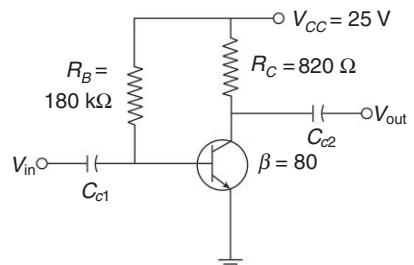


Fig. 5.10

### EXAMPLE 5.10

For a fixed-bias configuration shown in Fig. 5.6, determine  $I_C$ ,  $R_C$ ,  $R_B$ , and  $V_{CE}$  using the following specifications:  $V_{CC} = 12 \text{ V}$ ,  $V_C = 6 \text{ V}$ ,  $\beta = 80$ , and  $I_B = 40 \mu\text{A}$ .

**Solution** Assume  $V_{BE} = 0.7 \text{ V}$  for a silicon transistor.

$$I_C = \beta I_B = 80 \times 40 \mu\text{A} = 3.2 \text{ mA}$$

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{12 - 6}{3.2 \times 10^{-3}} = 1.875 \text{ k}\Omega$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.7}{40 \times 10^{-6}} = 282.5 \text{ k}\Omega$$

Since the emitter is grounded,  $V_E = 0$ .

$$V_{CE} = V_C = 6 \text{ V}$$

### 5.4.2 Emitter-Feedback Bias

The emitter-feedback bias network shown in Fig. 5.11 contains an emitter resistor for improving the stability level over that of the fixed-bias configuration. The analysis will be performed by first examining the base-emitter loop and then using the results to investigate the collector-emitter loop.

**Base-emitter Loop** Applying Kirchhoff's voltage law for the base-feedback emitter loop, we get

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \quad (5.5)$$

$$V_{CC} - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_{CC} - I_B (R_B + R_E) - V_{BE} - I_C R_E = 0$$

$$V_{CC} - V_{BE} = I_B (R_B + R_E) + I_C R_E$$

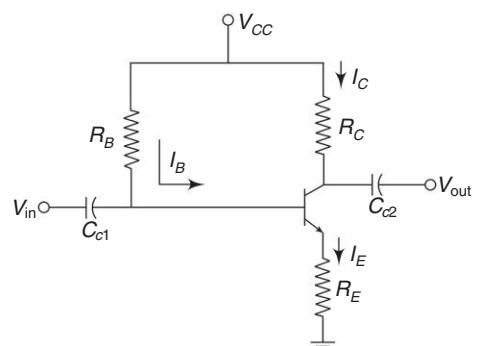


Fig. 5.11 Emitter-feedback bias circuit

Therefore,

$$I_B = \frac{V_{CC} - V_{BE}}{R_E + R_B} - \left( \frac{R_E}{R_E + R_B} \right) I_C \quad (5.6)$$

Here,  $V_{BE}$  is independent of  $I_C$ .

Hence,

$$\frac{dI_B}{dI_C} = -\left( \frac{R_E}{R_E + R_B} \right) \quad (5.7)$$

Substituting Eq. (5.7) in Eq. (5.8), we get the stability factor as

$$S = \frac{1 + \beta}{1 + \beta \frac{R_E}{R_E + R_B}} \quad (5.8)$$

Since  $1 + \frac{\beta R_E}{(R_E + R_B)} > 1$ ,  $S < (1 + \beta)$ . Note that the value of the stability factor  $S$  is always lower in emitter-feedback bias circuit than that of the fixed-bias circuit. Hence, it is clear that a better thermal stability can be achieved in an emitter-feedback bias circuit than the fixed-bias circuit.

**Collector-Emitter Loop** Applying Kirchhoff's voltage law for the collector-emitter loop, we get

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting  $I_E = I_C$ , we have

$$V_{CE} - V_{CC} + I_C (R_C + R_E) = 0$$

and

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \quad (5.9)$$

$V_E$  is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E \quad (5.10)$$

The voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$V_C = V_{CE} + V_E \quad (5.11)$$

or

$$V_C = V_{CC} - I_C R_C \quad (5.12)$$

The voltage at the base with respect to ground can be determined from

$$V_B = V_{CC} - I_B R_E \quad (5.13)$$

or

$$V_B = V_{BE} + V_E \quad (5.14)$$

### EXAMPLE 5.11

For the emitter-feedback bias circuit,  $V_{CC} = 10$  V,  $R_C = 1.5$  k $\Omega$ ,  $R_B = 270$  k $\Omega$ , and  $R_E = 1$  k $\Omega$ . Assuming  $\beta = 50$ , determine (a) stability factor,  $S$  (b)  $I_B$ , (c)  $I_C$ , (d)  $V_{CE}$ , (e)  $V_C$ , (f)  $V_E$ , (g)  $V_B$ , and (h)  $V_{BC}$ .

**Solution**

(a) The stability factor is

$$\begin{aligned} S &= \frac{1 + \beta}{1 + \frac{\beta R_E}{(R_E + R_B)}} = \frac{1 + 50}{1 + \frac{(50 \times 1 \times 10^3)}{1 \times 10^3 + 270 \times 10^3}} \\ &= \frac{51}{1 + 0.185} = \frac{51}{1.185} = 43.04 \end{aligned}$$

$$(b) I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{10 - 0.7}{27 \times 10^3 + (51)(1 \times 10^3)} = \frac{9.3}{321} = 28.97 \mu\text{A}$$

$$(c) I_C = \beta I_B = (50)(28.97 \times 10^{-6}) = 1.45 \text{ mA}$$

$$(d) V_{CE} = V_{CC} - I_C(R_C + R_E) = 10 - 1.45 \times 10^{-3}(1.5 \times 10^3 + 1 \times 10^3) = 10 - 3.62 = 6.38 \text{ V}$$

$$(e) V_C = V_{CC} - I_C R_C = 10 - 1.45 \times 10^{-3}(1.5 \times 10^3) = 7.825 \text{ V}$$

$$(f) V_E = V_C - V_{CE} = 7.825 - 6.38 = 1.445 \text{ V}$$

$$\text{or } V_E = I_E R_E = I_C R_E = 1.45 \times 10^{-3} \times 1 \times 10^3 = 1.45 \text{ V}$$

$$(g) V_B = V_{BE} + V_E = 0.7 + 1.45 = 2.15 \text{ V}$$

$$(h) V_{BC} = V_B - V_C = 2.15 - 7.825 = -5.675 \text{ V} \quad (\text{reverse bias as required})$$

**EXAMPLE 5.12**

Calculate dc bias voltage and currents in the circuit in Fig. 5.12. Neglect  $V_{BE}$  of the transistor.

**Solution** Given,  $V_{CC} = 20 \text{ V}; R_B = 400 \text{ k}\Omega, \beta = 100, R_E = 1 \text{ k}\Omega; R_C = 2 \text{ k}\Omega$

$$I_B R_B + V_{BE} + I_E R_E = V_{CC}$$

$$\frac{I_C}{\beta} R_B + 0 + (I_C + I_B) R_E = 20$$

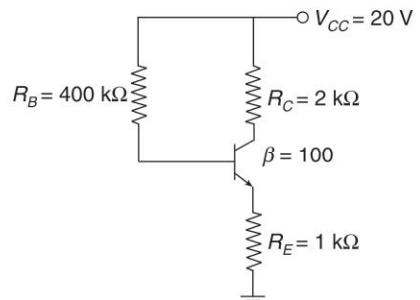
$$I_C \left[ \frac{R_B}{\beta} + R_E + \frac{R_E}{\beta} \right] = 20$$

$$\text{Therefore, } I_C = \frac{20}{\left[ \frac{400 \times 10^3}{100} + 1 \times 10^3 + 10 \right]} = 4 \text{ mA}$$

$$I_B = \frac{I_C}{\beta} = \frac{4 \times 10^{-3}}{100} = 0.4 \mu\text{A}$$

$$V_B = V_{BE} + I_E R_E$$

$$= 0 + 4 \times 10^{-3} \times 1 \times 10^3 = 4 \text{ V, since } I_C \approx I_E$$

**Fig. 5.12**

### 5.4.3 Collector-to-Base Bias or Collector-Feedback Bias

A common-emitter amplifier using collector-to-base bias circuit is shown in Fig. 5.13. This circuit is the simplest way to provide some degree of stabilization to the amplifier operating point.

If the collector current  $I_C$  tends to increase due to either increase in temperature or the transistor has been replaced by the one with a higher  $\beta$ , the voltage drop across  $R_C$  increases, thereby reducing the value of  $V_{CE}$ . Therefore,  $I_B$  decreases which, in turn, compensates the increase in  $I_C$ . Thus, greater stability is obtained.

The loop equation for this circuit is

$$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE} \quad (5.15)$$

i.e.,

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \quad (5.16)$$

$$\text{Therefore, } \frac{dI_B}{dI_C} = \frac{-R_C}{R_C + R_B} \quad (5.17)$$

Substituting Eq. (5.17) into Eq. (5.3), we get

$$S = \frac{1 + \beta}{1 + \beta \left( \frac{R_C}{R_C + R_B} \right)} \quad (5.18)$$

As can be seen, this value of the stability factor is smaller than the value obtained by fixed-bias circuit. Also,  $S$  can be made small and the stability can be improved by making  $R_B$  small or  $R_C$  large.

If  $R_C$  is very small, then  $S = (\beta + 1)$ , i.e., stability is very poor. Hence, the value of  $R_C$  must be quite large for good stabilization. Thus, collector-to-base bias arrangement is not satisfactory for the amplifier circuits like transformer-coupled amplifier where the dc load resistance in the collector circuit is very small. For such amplifiers, emitter bias or self-bias will be the most satisfactory transistor biasing for stabilization.

#### EXAMPLE 5.13

In the biasing with feedback resistor method, a silicon transistor with feedback resistor is used. The operating point is at 7 V, 1 mA and  $V_{CC} = 12$  V. Assume  $\beta = 100$ . Determine (a) the value of  $R_B$ , (b) stability factor, and (c) what will be the new operating point if  $\beta = 50$  with all other circuit values are same?

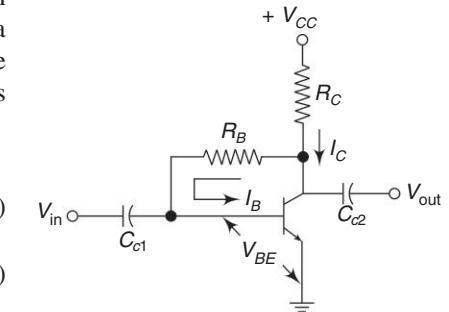
**Solution** Refer to Fig. 5.6. We know that for a silicon transistor,  $V_{BE} = 0.7$  V.

(a) *To determine  $R_B$*

The operating point is at  $V_{CE} = 7$  V and  $I_C = 1$  mA

$$\text{Here, } R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{12 - 7}{1 \times 10^{-3}} = 5 \text{ k}\Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{1 \times 10^{-3}}{100} = 10 \mu\text{A}$$



**Fig. 5.13** Collector-to-base bias circuit

Using the relation,

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B} = \frac{12 - 0.7 - 1 \times 10^{-3} \times 5 \times 10^3}{10 \times 10^{-6}} = 630 \text{ k}\Omega$$

(b) *Stability factor*

$$S = \frac{1 + \beta}{1 + \beta \left[ \frac{R_C}{R_C + R_B} \right]} = \frac{1 + 100}{1 + 100 \left[ \frac{5 \times 10^3}{(5 + 630) \times 10^3} \right]} = 56.5$$

(c) *To determine new operating point when  $\beta = 50$*

$$\begin{aligned} V_{CC} &= \beta I_B R_C + I_B R_B + V_{BE} \\ &= I_B (\beta R_C + R_B) + V_{BE} \end{aligned}$$

i.e.,

$$12 = I_B (50 \times 5 \times 10^3 + 630 \times 10^3) + 0.7$$

$$I_B = \frac{11.3}{880 \times 10^3} = 12.84 \mu\text{A}$$

Therefore,

$$I_C = \beta I_B = 50 \times 12.84 \times 10^{-6} = 0.642 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 12 - 0.642 \times 10^{-3} \times 5 \times 10^3 = 8.79 \text{ V}$$

Therefore, the coordinates of the new operating point are  $V_{CEQ} = 8.79 \text{ V}$  and  $I_{CQ} = 0.642 \text{ mA}$ .

### EXAMPLE 5.14

In an *NPN* transistor, if  $\beta = 50$  is used in common-emitter circuit with  $V_{CC} = 10 \text{ V}$  and  $R_C = 2 \text{ k}\Omega$ . The bias is obtained by connecting  $100 \text{ k}\Omega$  resistor from collector to base. Find the quiescent point and stability factor.

**Solution** Given,  $V_{CC} = 10 \text{ V}$ ,  $R_C = 2 \text{ k}\Omega$ ,

$$\beta = 50 \text{ and collector-to-base resistor } R_B = 100 \text{ k}\Omega$$

*To determine the quiescent point:* We know that for the collector-to-base bias-transistor circuit,

$$V_{CC} = \beta I_B R_C + I_B R_B + V_{BE}$$

Therefore,

$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} \\ &= \frac{10 - 0.7}{100 \times 10^3 + 50 \times 2 \times 10^3} = 46.5 \mu\text{A} \end{aligned}$$

Hence,

$$I_C = \beta \cdot I_B = 50 \times 46.5 \times 10^{-6} = 2.325 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - 2.325 \times 10^{-3} \times 2 \times 10^3 = 5.35 \text{ V}$$

Therefore, the coordinates of the new operating point are

$$V_{CEQ} = 5.35 \text{ V} \text{ and } I_{CQ} = 2.325 \text{ mA}$$

To find the stability factor  $S$

$$S = \frac{1 + \beta}{1 + \beta \left[ \frac{R_C}{R_C + R_B} \right]} = \frac{1 + 50}{1 + 50 \left[ \frac{2 \times 10^3}{2 \times 10^3 + 100 \times 10^3} \right]} = 25.75$$

### EXAMPLE 5.15

In the collector-to-base  $CE$  amplifier circuit of Fig. 5.6 having  $V_{CC} = 12$  V,  $R_C = 250$  k $\Omega$ ,  $I_B = 0.25$  mA,  $\beta = 100$ , and  $V_{CEQ} = 8$  V, calculate  $R_B$  and stability factor.

#### Solution

$$R_B = \frac{V_{CEQ}}{I_B} = \frac{8}{0.25 \times 10^{-3}} = 32 \text{ k}\Omega$$

Stability factor,

$$S = \frac{1 + \beta}{1 + \beta \left( \frac{R_C}{R_C + R_B} \right)} = \frac{101}{1 + 100 \left( \frac{250}{32 + 250} \right)} = 56.9$$

### EXAMPLE 5.16

Calculate the quiescent current and voltage of a collector-to-base bias arrangement using the following data:  $V_{CC} = 10$  V,  $R_B = 100$  k $\Omega$ ,  $R_C = 2$  k $\Omega$ ,  $\beta = 50$ , and also specify a value of  $R_B$  so that  $V_{CE} = 7$  V.

#### Solution

(a) Applying KVL to the base circuit, we have

$$V_{CC} - I_B(1 + \beta) R_C - I_B R_B - V_{BE} = 0$$

Therefore,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_C} = \frac{10 - 0.7}{100 \times 10^3 + (1 + 50) \times 2 \times 10^3} = 46 \mu\text{A}$$

$$I_C = \beta I_B = 50 \times 46 \mu\text{A} = 2.3 \text{ mA}$$

Applying KVL to the collector circuit, we have

$$V_{CC} - (I_B + I_C) R_C - V_{CE} = 0$$

Therefore,

$$\begin{aligned} V_{CE} &= V_{CC} - (I_B + I_C) R_C \\ &= 10 - (46 \times 10^{-6} + 2.3 \times 10^{-3}) \times 2 \times 10^3 \\ &= 5.308 \text{ V} \end{aligned}$$

Quiescent current,

$$I_{CQ} = 2.3 \text{ mA and}$$

Quiescent voltage,

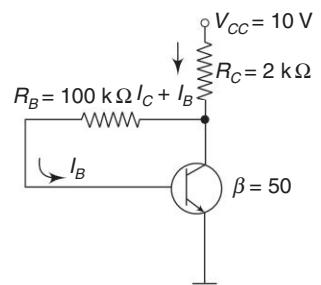
$$V_{CEQ} = 5.308 \text{ V}$$

(b) Given,

$$V_{CE} = 7 \text{ V}$$

$$(I_B + I_C) R_C = V_{CC} - V_{CE}$$

$$(1 + \beta) I_B R_C = V_{CC} - V_{CE}$$



**Fig. 5.14**

$$I_B = \frac{V_{CC} - V_{CE}}{(1 + \beta) R_C} = \frac{10 - 7}{(1 + 50) \times 2 \times 10^3} = 29.41 \mu\text{A}$$

We have,

$$V_{CC} = I_B R_B + V_{BE}$$

$$R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{7 - 0.7}{29.41 \times 10^{-6}} = 214.2 \text{ k}\Omega$$

#### 5.4.4 Collector-Emitter Feedback Bias

Figure 5.15 shows the collector-emitter feedback-bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here, collector feedback is provided by connecting a resistance  $R_B$  from the collector to the base and emitter feedback is provided by connecting an emitter resistance  $R_E$  from the emitter to ground. Both the feedbacks are used to control the collector current  $I_C$  and the base current  $I_B$  in the opposite direction to increase the stability as compared to the previous biasing circuits.

Applying Kirchhoff's voltage law to the current, we get

$$(I_B + I_C) R_E + V_{BE} + I_B R_B + (I_B + I_C) R_C - V_{CC} = 0$$

Therefore,

$$\frac{V_{CC} - V_{BE}}{R_E + R_C + R_B} - \left( \frac{R_E + R_C}{R_E + R_C + R_B} \right) I_C = I_B$$

Since  $V_{BE}$  is independent of  $I_C$ ,

$$\frac{dI_B}{dI_C} = - \left( \frac{R_E + R_C}{R_E + R_C + R_B} \right)$$

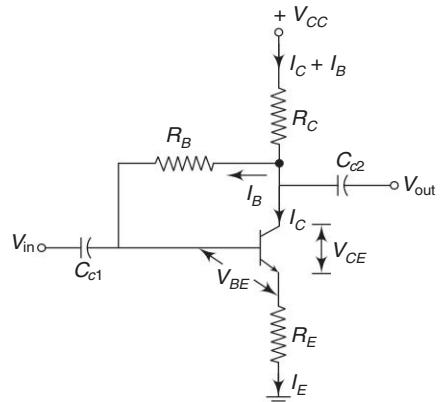
Substituting the above equation in Eq. (5.3), we get

$$S = \frac{1 + \beta}{1 + \frac{\beta(R_E + R_C)}{R_E + R_C + R_B}} \quad (5.19)$$

From this, it is clear that the stability of the collector-emitter feedback bias circuit is always better than that of the collector-feedback and emitter-feedback circuits.

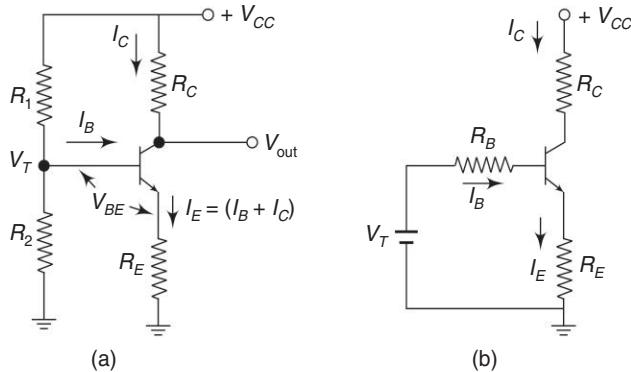
#### 5.4.5 Voltage-Divider Bias, Self-Bias, or Emitter Bias

A simple circuit used to establish a stable operating point is the self-biasing configuration. The self-bias, also called emitter bias, or emitter resistor, and potential divider circuit, that can be used for low collector resistance, is shown in Fig. 5.16. The current in the emitter resistor  $R_E$  causes a voltage drop which is in the



**Fig. 5.15** Collector-emitter feedback circuit

direction to reverse bias the emitter junction. For the transistor to remain in the active region, the base-emitter junction has to be forward biased. The required base bias is obtained from the power supply through the potential divider network of the resistances  $R_1$  and  $R_2$ .



**Fig. 5.16** (a) Self-bias circuit (b) Thevenin's equivalent circuit

**Use of Self-bias Circuit as a Constant Current Circuit** If  $I_C$  tends to increase, say, due to increase in  $I_{CO}$  with temperature, the current in  $R_E$  increases. Hence, the voltage drop across  $R_E$  increases thereby decreasing the base current. As a result,  $I_C$  is maintained almost constant.

**Advantage of Self-bias (Voltage-Divider Bias) Over Other Types of Biasing** In the fixed-bias method discussed in Section 5.4.1, the stability factor is given by

$$S = 1 + \beta$$

Since  $\beta$  is normally a large quantity, this circuit provides very poor stability. Therefore, the fixed biasing technique is not preferred for biasing the base.

In the collector-to-base bias method, when  $R_C$  is very small,  $S \approx 1 + \beta$ , which is equal to that of fixed bias. Hence, the collector-to-base bias method is also not preferable. In the self-bias method, when  $\frac{R_B}{R_E}$  is very small,  $S \approx 1$ , which provides good stability. Hence, the self-bias method is the best method over other types of ‘biasing’.

#### 5.4.6 Common Base Stability

In a common-base amplifier circuit, the equation for the collector current  $I_C$  is given by

$$I_C = \alpha I_E + I_{CO}$$

$$S \approx \frac{dI_C}{dI_{CO}} = 1$$

Since this is highly stable, the common-base amplifier circuit is not in need of bias stabilization.

## 5.5 STABILIZATION FACTORS

**To Determine Stability Factor, S** Applying Thevenin's theorem to the circuit of Fig. 5.16, for finding the base current, we have,

$$V_T = \frac{R_2 V_{CC}}{R_1 + R_2} \text{ and } R_B = \frac{R_1 R_2}{R_1 + R_2}$$

The loop equation around the base circuit can be written as

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating this equation with respect to  $I_C$ , we get

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_E + R_B}$$

Substituting this equation in Eq. (5.3), we get

$$S = \frac{1 + \beta}{1 + \beta \left( \frac{R_E}{R_E + R_B} \right)}$$

Therefore,

$$S = (1 + \beta) \frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}} \quad (5.20)$$

As can be seen, the value of  $S$  is equal to one if the ratio  $R_B/R_E$  is very small as compared to 1. As this ratio becomes comparable to unity, and beyond towards infinity, the value of the stability factor goes on increasing till  $S = 1 + \beta$ .

This improvement in the stability up to a factor equal to 1 is achieved at the cost of power dissipation. To improve the stability, the equivalent resistance  $R_B$  must be decreased, forcing more current in the voltage divider network of  $R_1$  and  $R_2$ .

Often, to prevent the loss of gain due to the negative feedback,  $R_E$  is shunted by a capacitor  $C_E$ . The capacitive reactance  $X_{CE}$  must be equal to about one-tenth of the value of the resistance  $R_E$  at the lowest operating frequency.

**To Determine the Stability Factor  $S'$**  The stability factor  $S'$  is defined as the rate of change of  $I_C$  with  $V_{BE}$ , keeping  $I_{CO}$  and  $\beta$  constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}}$$

From Fig. 5.16 (b),

$$\begin{aligned} V_T &= I_B R_B + V_{BE} + I_E R_E \\ &= I_B [R_B + R_E] + I_C R_E + V_{BE} \text{ since } [I_E = I_B + I_C] \end{aligned} \quad (5.21)$$

We have

$$I_B = \frac{I_C - (1 + \beta)I_{CO}}{\beta} \quad (5.22)$$

Substituting Eq. (5.21) in Eq. (5.22), we get

$$V_T = \frac{I_C}{\beta}(R_B + R_E) + V_{BE} + I_C R_E + \frac{I_{CO}}{\beta}(1 + \beta)\{R_B + R_E\} \quad (5.23)$$

Differentiating the above equation w.r.t.  $V_{BE}$ , we get

$$\begin{aligned} 0 &= \frac{dI_C}{dV_{BE}} \left( \frac{R_B + R_E}{\beta} \right) + 1 + R_E \frac{dI_C}{dV_{BE}} + 0 \\ -1 &= \frac{dI_C}{dV_{BE}} \left[ R_E + \frac{R_B + R_E}{\beta} \right] \\ -1 &= \frac{dI_C}{dV_{BE}} \left[ \frac{R_B + (1 + \beta)R_E}{\beta} \right] \end{aligned}$$

Therefore,

$$S' = \frac{dI_C}{dV_{BE}} = \frac{-\beta}{R_B + (1 + \beta)R_E} \quad (5.24)$$

**To Determine the Stability of  $S''$**  The stability factor  $S''$  is defined as the rate of change of  $I_C$  w.r.t.  $\beta$ , keeping  $I_{CO}$  and  $V_{BE}$  constant.

Rearranging Eq. (5.23), we have

$$I_C = \frac{\beta(V_T - V_{BE})}{R_B + (1 + \beta)R_E} + \frac{\beta \left( \frac{1 + \beta}{\beta} \right) I_{CO} (R_B + R_E)}{R_B + (1 + \beta)R_E} \quad (5.25)$$

Since  $\beta \gg 1$ , the numerator of the second term can be written as

$$(R_B + R_E) \left( \frac{1 + \beta}{\beta} \right) I_{CO} = (R_B + R_E) I_{CO} \quad (5.26)$$

Substituting Eq. (5.26) in Eq. (5.25), we have

$$I_C = \frac{\beta(V_T - V_{BE})}{R_E + (1 + \beta)R_E} + \frac{\beta(R_B + R_E)I_{CO}}{R_B + (1 + \beta)R_E}$$

$$\text{Therefore, } I_C = \frac{\beta[V_T - V_{BE} + (R_B + R_E)I_{CO}]}{R_B + (1 + \beta)R_E}$$

Let,

$$V' = (R_B + R_E)I_{CO}.$$

$$\text{Therefore, } I_C = \frac{\beta[V_T - V_{BE} + V']} {R_B + (1 + \beta)R_E} \quad (5.27)$$

Differentiating the above equation w.r.t.  $\beta$  and simplifying, we obtain

$$S'' = \frac{dI_C}{d\beta} = \frac{I_C}{\beta \left[ 1 + \beta \left( \frac{R_E}{R_E + R_B} \right) \right]} = \frac{SI_C}{\beta(1+\beta)} \quad (5.28)$$

### EXAMPLE 5.17

In a CE germanium transistor-amplifier circuit, the bias is provided by self-bias, i.e., emitter resistor and potential-divider arrangement (refer to Fig. 5.7). The various parameters are  $V_{CC} = 16$  V,  $R_C = 3$  k $\Omega$ ,  $R_E = 2$  k $\Omega$ ,  $R_1 = 56$  k $\Omega$ ,  $R_2 = 20$  k $\Omega$ , and  $\alpha = 0.985$ . Determine (a) the coordinates of the operating point, and (b) the stability factor  $S$ .

**Solution** For a germanium transistor,  $V_{BE} = 0.3$  V. As  $\alpha = 0.985$ ,

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.985}{1-0.985} = 66$$

(a) To find the coordinates of the operating point

Referring to Fig. 5.16, we have

$$\text{Thevenin's voltage, } V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{20 \times 10^3}{76 \times 10^3} \times 16 = 4.21 \text{ V}$$

$$\text{Thevenin's resistance, } R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{20 \times 10^3 \times 56 \times 10^3}{76 \times 10^3} = 14.737 \text{ k}\Omega$$

The loop equation around the base circuit is

$$\begin{aligned} V_T &= I_B R_B + V_{BE} + (I_B + I_C) R_E \\ &= \frac{I_C}{\beta} R_B + V_{BE} + \left( \frac{I_C}{\beta} + I_C \right) R_E \\ 4.21 &= \frac{I_C}{66} \times 14.737 \times 10^3 + 0.3 + I_C \left( \frac{1}{66} + 1 \right) \times 2 \times 10^3 \\ 3.91 &= I_C [0.223 + 2.03] \times 10^3 \end{aligned}$$

$$\text{Therefore, } I_C = \frac{3.91}{2.253 \times 10^3} = 1.73 \text{ mA}$$

$$\text{Since } I_B \text{ is very small, } I_C \approx I_E = 1.73 \text{ mA}$$

$$\begin{aligned} \text{Therefore, } V_{CE} &= V_{CC} - I_C R_C - I_E R_E \\ &= V_{CC} - I_C [R_C + R_E] \\ &= 16 - 1.73 \times 10^{-3} \times 5 \times 10^3 = 7.35 \text{ V} \end{aligned}$$

Therefore, the coordinates of the operating point are  $I_C = 1.73$  mA and  $V_{CE} = 7.35$  V.

(b) To find the stability factor  $S$ ,

$$S = (1 + \beta) \frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}} = (1 + 66) \frac{1 + \frac{14.737}{2}}{1 + 66 + \frac{14.737}{2}} = 67 \times \frac{8.3685}{74.3685} = 7.537$$

### EXAMPLE 5.18

Consider the self-bias circuit where  $V_{CC} = 22.5$  V,  $R_C = 5.6$  k $\Omega$ ,  $R_2 = 10$  k $\Omega$ , and  $R_1 = 90$  k $\Omega$ ,  $h_{fe} = 55$ ,  $V_{BE} = 0.6$  V. The transistor operates in active region. Determine (a) operating point, and (b) stability factor.

**Solution** For the given circuit,  $V_{BE} = 0.6$  V,  $h_{fe} = 55$

(a) To determine the operating point

Thevenin's voltage,  $V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10 \times 10^3}{100 \times 10^3} \times 22.5 = 2.25$  V

Thevenin's resistance,  $R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 10^3 \times 90 \times 10^3}{100 \times 10^3} = 9$  k $\Omega$

The loop equation around the base circuit is

$$\begin{aligned} V_B &= I_B R_B + V_{BE} + (I_B + I_C) R_E \\ &= \frac{I_C}{h_{fe}} R_B + V_{BE} + \left( \frac{I_C}{h_{fe}} + I_C \right) R_E \\ 2.25 &= \frac{I_C}{55} \times 9 \times 10^3 + 0.6 + \left( \frac{1}{55} + 1 \right) I_C \times 1 \times 10^3 \\ 2.25 &= I_C \times 0.16 \times 10^3 + 0.6 + 1.01 \times I_C \times 10^3 \\ 2.25 &= I_C \times 1.17 \times 10^3 + 0.6 \end{aligned}$$

Therefore,  $I_C = \frac{2.25 - 0.6}{1.17 \times 10^3} = 1.41$  mA

Since  $I_B$  is very small,  $I_C \approx I_E = 1.41$  mA

Therefore,  $V_{CE} = V_{CC} - I_C R_C - I_E R_E = V_{CC} - I_C (R_C + R_E)$   
 $= 22.5 - 1.41 \times 10^{-3} \times 6.6 \times 10^3 = 13.19$  V

Operating point coordinates are  $V_{CE} = 13.19$  V and  $I_C = 1.41$  mA

(b) To find the stability factor,  $S$

$$S = (1 + \beta) \frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}} = (1 + 55) \frac{1 + \frac{9 \times 10^3}{1 \times 10^3}}{1 + 55 + \frac{9 \times 10^3}{1 \times 10^3}} = \frac{56 \times 10}{65} = \frac{560}{65} = 8.6$$

**EXAMPLE 5.19**

Figure 5.17 shows the dc bias circuit of a common-emitter transistor amplifier. Find the percentage change in the collector current, if the transistor with  $h_{fe} = 50$  is replaced by another transistor with  $h_{fe} = 150$ . It is given that the base-emitter drop  $V_{BE} = 0.6$  V.

**Solution**

(a) For the given circuit,  $V_{BE} = 0.6$  V,  $h_{fe} = 50$

$$\text{Thevenin's voltage, } V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{30 \times 10^3} \times 12 = 2 \text{ V}$$

$$\text{Thevenin's resistance, } R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{25 \times 10^3 \times 5 \times 10^3}{30 \times 10^3} = 4.16 \text{ k}\Omega$$

The loop equation around the base circuit is

$$\begin{aligned} V_T &= V_B = I_B R_B + V_{BE} + (I_B + I_C) R_E \\ &= \frac{I_C}{h_{fe}} R_B + V_{BE} + \left( \frac{I_C}{h_{fe}} + I_C \right) R_E \\ 2 &= \frac{I_C}{50} \times 4.6 \times 10^3 + 0.6 + \left( \frac{1}{50} + 1 \right) \times I_C \times 0.1 \times 10^3 \\ 2 - 0.6 &= I_C \times (0.08 + 0.102) \times 10^3 \end{aligned}$$

$$\text{Therefore, } I_C = \frac{14}{0.182 \times 10^3} = 7.69 \text{ mA}$$

(b) For the given circuit,  $V_{BE} = 0.6$  V,  $h_{fe} = 150$

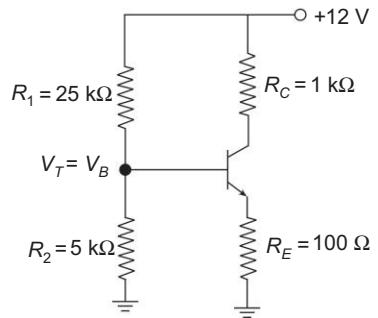
The loop equation around the base circuit is

$$\begin{aligned} V_B &= I_B R_B + V_{BE} + (I_B + I_C) R_E \\ &= \frac{I_C}{h_{fe}} R_B + V_{BE} + \left( \frac{I_C}{h_{fe}} + I_C \right) R_E \\ 2 &= \frac{I_C}{50} \times 4.6 \times 10^3 + 0.6 + \left( \frac{1}{50} + 1 \right) \times I_C \times 0.1 \times 10^3 \\ 2 - 0.6 &= I_C \times (0.028 + 0.1) \times 10^3 \end{aligned}$$

$$\text{Therefore, } I_C = \frac{1.4}{0.128 \times 10^3} = 10.93 \text{ mA}$$

$$\text{Change in collector current} = \frac{10.93 - 7.69}{7.69} = 0.42, \text{ i.e., } 42\%$$

There is 42% change in  $I_C$  when  $h_{fe}$  changes from 50 to 150.



**Fig. 5.17**

**EXAMPLE 5.20**

If the various parameters of a *CE* amplifier which uses the self-bias method are  $V_{CC} = 12$  V,  $R_1 = 10$  k $\Omega$ ,  $R_2 = 5$  k $\Omega$ ,  $R_C = 1$  k $\Omega$ ,  $R_E = 2$  k $\Omega$ , and  $\beta = 100$ , find (a) the coordinates of the operating point, and (b) the stability factor, assuming the transistor to be silicon.

**Solution**

(a) *To find the coordinates of the operating point*

Refer Fig. 5.16.

$$\text{Thevenin's voltage, } V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{15 \times 10^3} \times 12 = 4 \text{ V}$$

$$\text{Thevenin's resistance, } R_B = \frac{R_1 R_2}{(R_1 + R_2)} = \frac{5 \times 10^3 \times 10 \times 10^3}{15 \times 10^3} = 3.33 \text{ k}\Omega$$

The loop equation around the basic circuit is

$$\begin{aligned} V_T &= I_B R_B + V_{BE} + (I_B + I_C) R_E \\ &= \frac{I_C}{\beta} R_B + V_{BE} + \left( \frac{I_C}{\beta} + I_C \right) R_E \\ 4 &= \frac{I_C}{100} \times 3.33 \times 10^3 + 0.7 + I_C \left( \frac{1}{100} + 1 \right) \times 2 \times 10^3 \end{aligned}$$

$$3.3 = (33.3 + 2020) I_C$$

$$I_C = \frac{3.3}{2053.3} = 1.61 \text{ mA}$$

$$\text{Since } I_B \text{ is very small, } I_C \approx I_E = 1.61 \text{ mA}$$

$$\text{Therefore, } V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$\begin{aligned} &= V_{CC} - I_C [R_C + R_E] \\ &= 12 - 1.61 \times 10^{-3} \times 3 \times 10^3 = 7.17 \text{ V} \end{aligned}$$

Therefore, the coordinates of the operating point are  $I_C = 1.61$  mA and  $V_{CE} = 7.17$  V.

(b) *To find the stability factor S*

$$S = (1 + \beta) \frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}} = (1 + 100) \frac{1 + \frac{3.33 \times 10^3}{2 \times 10^3}}{1 + 100 + \frac{3.33 \times 10^3}{2 \times 10^3}} = 2.6$$

**EXAMPLE 5.21**

Determine the quiescent current and collector-to-emitter voltage for a germanium transistor with  $\beta = 50$  in self-biasing arrangement. Draw the circuit with a given component value with  $V_{CC} = 20$  V,  $R_C = 2 \text{ k}\Omega$ ,  $R_E = 100 \Omega$ ,  $R_1 = 100 \text{ k}\Omega$ , and  $R_2 = 5 \text{ k}\Omega$ . Also find the stability factor.

**Solution** For a germanium transistor,  $V_{BE} = 0.3$  V and  $\beta = 50$

To find the coordinates of the operating point

$$\text{Thevenin's voltage, } V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{105 \times 10^3} \times 20 = 0.95 \text{ V}$$

$$\text{Thevenin's resistance, } R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 10^3 \times 5 \times 10^3}{105 \times 10^3} = 4.76 \text{ k}\Omega$$

The loop equation around the base circuit is

$$\begin{aligned} V_T &= I_B R_B + V_{BE} + (I_B + I_C) R_E \\ &= \frac{I_C}{\beta} R_B + V_{BE} + \left( \frac{I_C}{\beta} + I_C \right) R_E \\ 0.95 &= \frac{I_C}{50} \times 4.76 \times 10^3 + 0.3 + I_C \times \frac{51}{50} \times 100 \\ 0.65 &= 197.2 I_C \end{aligned}$$

$$\text{Therefore, } I_C = \frac{0.65}{197.2} = 3.296 \text{ mA}$$

$$\text{Since } I_B \text{ is very small, } I_C \approx I_E = 3.296 \text{ mA}$$

$$\begin{aligned} \text{Therefore, } V_{CE} &= V_{CC} - I_C R_C - I_E R_E \\ &= V_{CC} - I_C (R_C + R_E) \\ &= 20 - 3.296 \times 10^{-3} \times 2.01 \times 10^3 = 13.375 \text{ V} \end{aligned}$$

Therefore, the coordinates of the operating point are  $I_C = 3.296$  mA and  $V_{CE} = 13.375$  V.

To find the stability factor  $S$

$$S = (1 + \beta) \frac{\frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}} = (1 + 50) \frac{1 + \frac{4.76 \times 10^3}{100}}{1 + 50 + \frac{4.76 \times 10^3}{100}} = 25.18$$

**EXAMPLE 5.22**

A germanium transistor is used in a self-biasing circuit configuration as shown below with  $V_{CC} = 16$  V,  $R_C = 1.5 \text{ k}\Omega$  and  $\beta = 50$ . The operating point desired is  $V_{CE} = 8$  V and  $I_C = 4$  mA. If a stability factor  $S = 10$  is desired, calculate the values of  $R_1$  and  $R_2$  and  $R_E$  of the circuit (Fig. 5.18).

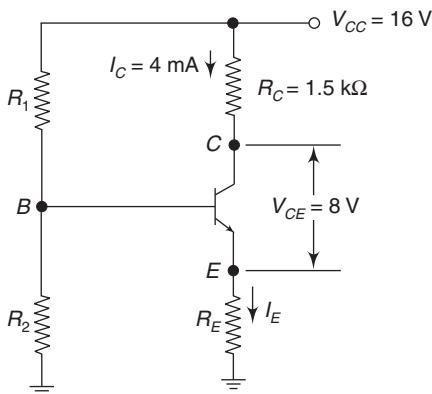


Fig. 5.18

**Solution**(a) To determine  $R_E$ 

We know that,

$$\begin{aligned}V_{CC} &= V_{CE} + I_C(R_C + R_E) \\16 &= 8 + 4 \times 10^{-3}(1.5 \times 10^3 + R_E)\end{aligned}$$

Therefore,

$$R_E = 500 \Omega$$

(b) To determine  $R_{TH}$ 

Given,

$$S = 10$$

Stability factor

$$S = \frac{1 + \beta}{1 + \beta \frac{R_E}{R_{TH} + R_E}} = \frac{1 + 50}{1 + 50 \left( \frac{500}{R_{TH} + 500} \right)}$$

Upon solving, we get  $R_{TH} = 5.58 \text{ k}\Omega$ (c) To determine  $R_2$ 

$$R_2 = 0.1 \beta R_E = 27.98 \text{ k}\Omega$$

(d) To determine  $R_1$ 

We know that,

$$R_{TH} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$5.58 \times 10^3 = \frac{R_1 \times 27.98 \times 10^3}{R_1 + 27.98 \times 10^3}$$

Therefore,

$$R_1 = 6.97 \text{ k}\Omega$$

**EXAMPLE 5.23**

A  $CE$  transistor amplifier with the voltage-divider bias circuit of Fig. 5.16 is designed to establish the quiescent point at  $V_{CE} = 12 \text{ V}$ ,  $I_C = 2 \text{ mA}$  and stability factor  $\leq 5.1$ . If  $V_{CC} = 24 \text{ V}$ ,  $V_{BE} = 0.7 \text{ V}$ ,  $\beta = 50$ , and  $R_C = 4.7 \text{ k}\Omega$ , determine the values of resistors  $R_E$ ,  $R_1$ , and  $R_2$ .

**Solution**(a) To determine  $R_E$ 

$$\begin{aligned}V_{CE} &= V_{CC} - I_C R_C - I_E R_E \\&= V_{CC} - I_C [R_C + R_E], \text{ since } I_C \approx I_E \\12 &= 24 - 2 \times 10^{-3} [4.7 \times 10^3 + R_E]\end{aligned}$$

Therefore,  $R_E = 1.3 \text{ k}\Omega$ (b) To determine  $R_1$  and  $R_2$ 

Stability factor,  $S = \frac{1 + \beta}{1 + \beta \left( \frac{R_E}{R_E + R_B} \right)}$ , where  $R_B = \frac{R_1 R_2}{(R_1 + R_2)}$

$$5.1 = \frac{51}{1 + 50 \left( \frac{1.3 \times 10^3}{1.3 \times 10^3 + R_B} \right)}$$

i.e.,  $1 + 50 \left( \frac{1.3 \times 10^3}{1.3 \times 10^3 + R_B} \right) = \frac{51}{5.1} = 10$

Therefore,  $\left( \frac{50 \times 1.3 \times 10^3}{1.3 \times 10^3 + R_B} \right) = 9$   
 $1.3 \times 10^3 + R_B = \frac{50 \times 1.3 \times 10^3}{9} = 7.2 \text{ k}\Omega$   
 $R_B = 5.9 \text{ k}\Omega$

Also, we know that for a good voltage divider, the value of the resistance  $R_2 = 0.1 \beta R_E$ Therefore,  $R_2 = 0.1 \times 50 \times 1.3 \times 10^3 = 6.5 \text{ k}\Omega$ 

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$5.9 \times 10^3 = \frac{R_1 \times 6.5 \times 10^3}{R_1 + 6.5 \times 10^3}$$

Simplifying, we get  $R_1 = 64 \text{ k}\Omega$ **EXAMPLE 5.24**In the circuit shown in Fig. 5.19, if  $I_C = 2 \text{ mA}$  and  $V_{CE} = 3 \text{ V}$ , calculate  $R_1$  and  $R_3$ .**Solution**Given,  $\beta = 100$ ,  $I_C = 2 \text{ mA}$ ,  $V_{CE} = 3 \text{ V}$ ,  $V_{BE} = 0.6 \text{ V}$ ,  $R_2 = 10 \text{ k}\Omega$  and  $R_4 = 500 \text{ }\Omega$

We know that

$$\beta = \frac{I_C}{I_B}$$

Hence,

$$I_B = \frac{I_C}{\beta} = \frac{2 \times 10^{-3}}{100} = 20 \mu A$$

$$V_{CC} = I_C R_3 + V_{CE} + I_E R_4$$

$$I_E = I_C + I_B = 20 \times 10^{-6} + 2 \times 10^{-3} = 2.02 \text{ mA}$$

Substituting the values, we get

$$15 = 2 \times 10^{-3} \times R_3 + 3 + 2.02 \times 10^{-3} \times 500$$

Therefore,

$$R_3 = 5.495 \text{ k}\Omega$$

$$V_B = V_{BE} + I_E R_4 = 0.6 + 2.02 \times 10^{-3} \times 500 = 1.61$$

From the circuit,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$1.61 = \frac{10 \times 10^3 \times 15}{R_1 + 10 \times 10^3}$$

Therefore,

$$R_1 = 83.17 \text{ k}\Omega$$

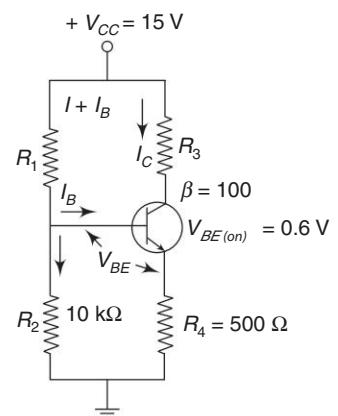


Fig. 5.19

### EXAMPLE 5.25

In an *NPN* transistor,  $\beta = 50$  is used in common-emitter circuit with  $V_{CC} = 10 \text{ V}$  and  $R_C = 2 \text{ k}\Omega$ . The bias is obtained by connecting the  $100 \text{ k}\Omega$  resistor from collector to base. Find the quiescent point and stability factor.

**Solution** Given,  $V_{CC} = 10 \text{ V}$ ,  $R_C = 2 \text{ k}\Omega$ ,  $\beta = 50$  and collector-to-base resistor,  $R_B = 100 \text{ k}\Omega$

To determine the quiescent point

We know that the collector-to-base bias-transistor circuit

$$V_{CC} = \beta I_B R_C + I_B R_B + V_{BE}$$

$$\text{Therefore, } I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta \cdot R_C} = \frac{10 - 0.7}{100 \times 10^3 + 50 \times 2 \times 10^3} = 46.5 \mu A$$

$$\text{Hence, } I_C = \beta I_B = 50 \times 46.5 \times 10^{-6} = 2.325 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - 2.325 \times 10^{-3} \times 2 \times 10^3 = 5.35 \text{ V}$$

Therefore, the coordinates of the new operating point are

$$V_{CEQ} = 5.35 \text{ V} \text{ and } I_{CQ} = 2.325 \text{ mA}$$

To find the stability factor  $S$

$$S = \frac{1 + \beta}{1 + \beta \left[ \frac{R_C}{R_C + R_B} \right]} = \frac{1 + 50}{1 + 50 \left[ \frac{2 \times 10^3}{2 \times 10^3 + 100 \times 10^3} \right]} = 25.75$$

**EXAMPLE 5.26**

Design a voltage-divider bias network using a supply of 24 V,  $\beta = 110$  and  $I_{CQ} = 4 \text{ mA}$ ,  $V_{CEQ} = 8 \text{ V}$ . Choose  $V_E = V_{CC}/8$ .

**Solution** Given:  $I_{CQ} = 4 \text{ mA}$ ,  $V_{CEQ} = 8 \text{ V}$ ,  $V_E = V_{CC}/8$ ,  $V_{CC} = 24 \text{ V}$ ,  $\beta = 110$

(a) To determine  $I_B$ ,  $I_E$  and  $V_E$

$$I_B = \frac{I_{CQ}}{\beta} = \frac{4 \times 10^3}{110} = 36.36 \mu\text{A}$$

$$I_E = I_B + I_C = 36.36 \times 10^{-6} + 4 \times 10^{-3} = 4.03636 \text{ mA}$$

$$V_E = \frac{V_{CC}}{8} = \frac{24}{8} = 3 \text{ V}$$

(b) To determine  $R_E$  and  $R_2$

$$R_E = \frac{V_E}{I_E} = \frac{3}{4.03636 \times 10^{-3}} = 743.244 \Omega$$

Applying KVL to the collector circuit,

$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$

Therefore,  $R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{24 - 8 - 3}{4 \times 10^{-3}} = 3.25 \text{ k}\Omega$

(c) To determine  $R_1$  and  $R_2$

$$V_B = V_E + V_{BE} = 3 + 0.7 = 3.7 \text{ V}$$

Referring to Fig. 5.16, consider the current through  $R_1$  to be  $I + I_B$  and that through  $R_2$  to be  $I$ . Resistors  $R_1$  and  $R_2$  form the potential divider. For proper operation of the potential divider, the current  $I$  should be atleast ten times the  $I_B$ , i.e.,  $I \geq 10 I_B$ . Therefore,

$$I = 10 I_B = 10 \times 36.36 \times 10^{-6} = 363.6 \mu\text{A}$$

$$R_2 = \frac{V_B}{I} = \frac{3.7}{363.6 \times 10^{-6}} = 10.176 \text{ k}\Omega$$

$$R_1 = \frac{V_{CC} - V_B}{I + I_B} = \frac{24 - 3.7}{(363.6 + 36.36) \times 10^{-6}} = 50.755 \text{ k}\Omega$$

**EXAMPLE 5.27**

Determine the stability factor for the circuit shown in Fig. 5.20.

**Solution**

$$I_2 = \frac{V_{BE} + (I_C + I_B) R_E}{R_2}$$

$$I_1 = I_B + I_2$$

Therefore,

$$\begin{aligned} I_1 &= I_B + \frac{V_{BE} + (I_C + I_B) R_E}{R_2} \\ &= \frac{I_B R_2 + V_{BE} + (I_C + I_B) R_E}{R_2} \end{aligned}$$

Applying KVL to the collector base-emitter loop, we have

$$\begin{aligned} V_{CC} &= (I_C + I_1) R_C - I_1 R_1 - V_{BE} - (I_C + I_B) R_E \\ &= (I_C + I_1) R_C + I_1 R_1 + V_{BE} + (I_C + I_B) R_E \\ &= I_C R_C + I_1 R_C + I_1 R_1 + V_{BE} + I_C R_E + I_B R_E \\ &= I_C (R_C + R_E) + I_1 (R_C + R_1) + V_{BE} + I_B R_E \end{aligned}$$

Substituting the value of  $I_1$  from the equation determined above, we get

$$\begin{aligned} V_{CC} &= I_C (R_C + R_E) + \frac{I_B R_2 + V_{BE} + (I_C + I_B) R_E}{R_2} (R_C + R_1) + V_{BE} + I_B R_E \\ &= I_C \left[ R_C + R_E + \frac{(R_C + R_1)}{R_2} \right] + I_B \left[ R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right] + \left[ 1 + \frac{(R_C + R_1)}{R_2} \right] V_{BE} \end{aligned}$$

We know that,  $I_C = \beta I_B + (1 + \beta) I_{CO}$

$$\text{Therefore, } I_B = \frac{I_C - (1 + \beta) I_{CO}}{\beta}$$

Substituting the value of  $I_B$ , we get

$$\begin{aligned} V_{CC} &= I_C \left[ R_C + R_E + \frac{R_E (R_C + R_1)}{R_2} \right] + \frac{I_C - (1 + \beta) I_{CO}}{\beta} \times \\ &\quad \left[ R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right] + \left[ 1 + \frac{(R_C + R_1)}{R_2} \right] V_{BE} \end{aligned}$$

We know that,  $S = \frac{dI_C}{dI_{CO}}$ . Hence, differentiating the above equation and assuming  $V_{BE}$  constant, we get

$$\begin{aligned} 0 &= \frac{\partial I_C}{\partial I_{CO}} \left[ R_C + R_E + \frac{R_E (R_C + R_1)}{R_2} \right] + \frac{\partial I_C}{\partial I_{CO}} \times \frac{1}{\beta} \left[ R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right] \\ &\quad - \frac{(1 + \beta)}{\beta} \left[ R_E + \frac{(R_E + R_2)(R_C + R_1)}{R_2} \right] \end{aligned}$$

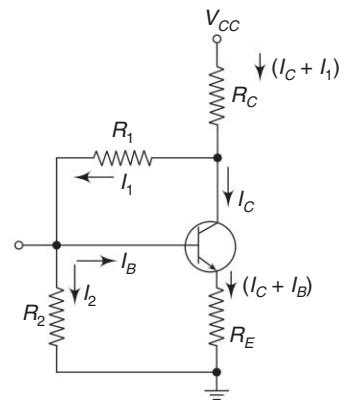


Fig. 5.20

$$\begin{aligned}
&= \frac{\partial I_C}{\partial I_{CO}} \left[ \frac{R_2 R_C + R_2 R_E + R_E R_C + R_E R_1}{R_2} \right] + \frac{\partial I_C}{\partial I_{CO}} \times \frac{1}{\beta} \times \\
&\quad \left[ \frac{R_2 R_E + R_E R_C + R_E R_1 + R_2 R_C + R_1 R_2}{R_2} \right] - \frac{1 + \beta}{\beta} \left[ \frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{R_2} \right] \\
&= \frac{\partial I_C}{\partial I_{CO}} \left[ \frac{R_2 R_C + R_E (R_1 + R_2 + R_C)}{R_2} \right] + \frac{\partial I_C}{\partial I_{CO}} \times \frac{1}{\beta} \times \left[ \frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{R_2} \right] \\
&\quad - \frac{1 + \beta}{\beta} \left[ \frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{R_2} \right] \\
&= \frac{\partial I_C}{\partial I_{CO}} \left[ \frac{R_2 R_C + R_E (R_1 + R_2 + R_C)}{R_2} \right] + \left[ \frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{\beta R_2} \right] \\
\frac{\partial I_C}{\partial I_{CO}} &= \frac{\frac{1 + \beta}{\beta} [R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)]}{R_2 R_C + R_E (R_1 + R_2 + R_C) + \frac{R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}{\beta}} \\
&= \frac{\frac{1 + \beta}{\beta} [R_2 (R_C + R_1) + (R_E (R_1 + R_2 + R_C))]}{\beta (R_2 R_C + R_E (R_1 + R_2 + R_C)) + R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)}
\end{aligned}$$

Stability factor,

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1 + \beta)[R_2 (R_C + R_1) + R_E (R_1 + R_2 + R_C)]}{R_1 R_2 + (\beta + 1)[R_2 R_C + R_E (R_1 + R_2 + R_C)]}$$

## 5.6 BIAS COMPENSATION

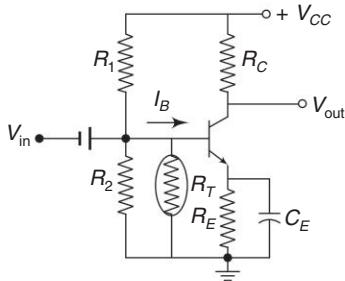
The various biasing circuits considered in the previous sections used some types of negative feedback to stabilize the operation point. Also, diodes, thermistors, and sensistors can be used to compensate for variations in current.

### 5.6.1 Thermistor and Sensistor Compensations

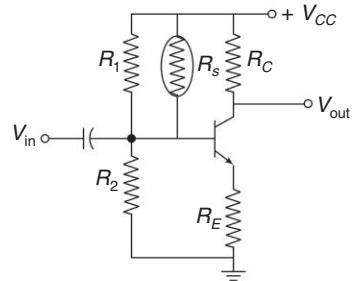
**Thermistor Compensation** In Fig. 5.21, a thermistor,  $R_T$ , having a negative temperature coefficient is connected in parallel with  $R_2$ . The resistance of the thermistor decreases exponentially with increase of temperature. An increase in temperature will decrease the base voltage  $V_{BE}$ , reducing  $I_B$  and  $I_C$ . Bias stabilization is also provided by  $R_E$  and  $C_E$ .

**Sensistor Compensation** In Fig. 5.22, a sensistor,  $R_S$ , having a positive temperature coefficient is connected across  $R_1$  (or  $R_E$ ).  $R_S$  increases with temperature. As temperature increases, the equivalent resistance of the parallel combination of  $R_1$  and  $R_S$  also increases and, hence, the base voltage  $V_{BE}$  decreases,

reducing  $I_B$  and  $I_C$ . This reduced  $I_C$  compensates for the increased  $I_C$  caused by the increase in  $I_{CO}$ ,  $V_{BE}$ , and  $\beta$  due to temperature rise.



**Fig. 5.21 Thermistor-bias compensation**



**Fig. 5.22 Sensistor-bias compensation**

## 5.6.2 Compensation Against Variation in $V_{BE}$ and $I_{CO}$

### Compensation for $V_{BE}$

- **Diode Compensation in Emitter Circuit** Figure 5.23 shows the Thevenin's equivalent circuit of the voltage-divider bias with bias-compensation technique.

Here,  $V_{DD}$  is separately used to keep the diode in the forward-biased condition. If the diode is of same material and type as the transistor, then the voltage across the diode  $V_D$  will have the same temperature coefficient ( $2.5 \text{ m V}^\circ\text{C}$ ) as the base-to-emitter voltage  $V_{BE}$ . If  $V_{BE}$  changes by a small amount with change in temperature, then  $V_D$  also changes by the same amount and, therefore, the changes cancel each other.

We know that,

$$V_{BE} = V_T - \frac{[R_B + (1 + \beta)R_E]}{\beta} I_C + \left[ \frac{(R_E + R_B)(1 + \beta)}{\beta} \right] I_{CO}$$

Rearranging, we have

$$\frac{[R_B + (1 + \beta)R_E]}{\beta I_C} I_C = V_T - V_{BE} + \left[ \frac{(R_E + R_B)(1 + \beta)}{\beta} \right] I_{CO}$$

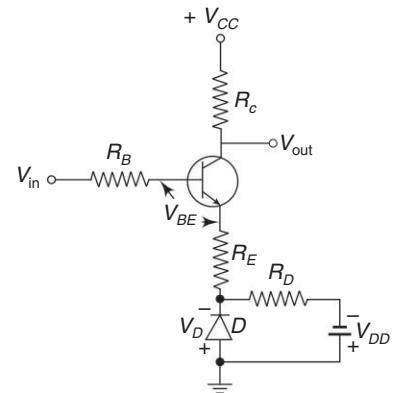
Hence,

$$I_C = \frac{\beta[V_T - V_{BE}] + (R_E + R_B)(1 + \beta)I_{CO}}{R_B + (1 + \beta)R_E}$$

From KVL equation of the base circuit of Fig. 5.23, the above equation can be written as

$$I_C = \frac{\beta[V_{in} - V_{BE} - V_D] + (R_E + R_B)(1 + \beta)I_{CO}}{R_B + (1 + \beta)R_E}$$

Since variation of  $V_D$  is same as  $V_{BE}$ , the collector current  $I_C$  will be insensitive to variation in  $V_{BE}$ .



**Fig. 5.23 Stabilization by voltage-divider bias compensation**

- Diode Compensation in Voltage-Divider Circuit** Figure 5.24 shows the diode compensation technique used in voltage-divider bias. Here, the diode is connected in series with the resistance  $R_2$  and it is in forward-biased condition. Therefore,

$$I_E = \frac{V_E}{R_E} = \frac{V_B - V_{BE}}{R_E}$$

and

$$I_C \approx I_E$$

When  $V_{BE}$  changes with temperature,  $I_C$  also changes. To cancel the change in  $I_C$ , a diode is used at the base terminal to compensate the change in  $V_{BE}$  as shown in Fig. 5.24. The voltage at the base,  $V_B$ , becomes

$$V_B = V_{R2} + V_D$$

Substituting in the above equation for  $I_C$ , we get

$$I_C \approx \frac{V_{R2} + V_D - V_{BE}}{R_E}$$

If the diode is of the same material and type as the transistor, then the voltage across the diode will have the same temperature coefficient ( $2.5 \text{ mV}/\text{C}$ ) as the base-to-emitter voltage  $V_{BE}$ . When  $V_{BE}$  changes by a small amount with change in temperature,  $V_D$  also changes by the same amount and thus, they cancel each other and the collector current remains constant. Therefore,

$$I_C = \frac{V_{R2}}{R_E}$$

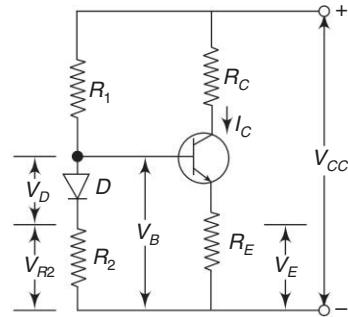
The change in  $V_{BE}$  due to temperature is compensated by a change in the diode voltage that keeps  $I_C$  stable at the  $Q$  point.

- Diode Compensation Against Variation in  $I_{CO}$**  Figure 5.25 shows a transistor amplifier with a diode  $D$  connected across the base-emitter junction for compensation of change in the collector saturation current  $I_{CO}$ . The diode is of the same material as the transistor and it is reverse biased by the base-emitter junction voltage  $V_{BE}$ , allowing the diode reverse saturation current  $I_o$  to flow through the diode  $D$ . The base current  $I_B = I - I_o$ .

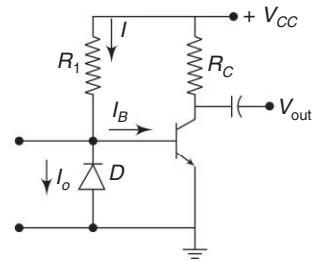
As long as temperature is constant, the diode  $D$  operates as a resistor. As the temperature increases,  $I_{CO}$  of the transistor increases. Hence, to compensate for this, the base current  $I_B$  should be decreased.

The increase in temperature will also cause the leakage current  $I_o$  through  $D$  to increase and thereby decreasing the base current  $I_B$ . This is the required action to keep  $I_C$  constant.

This method of bias compensation does not need a change in  $I_C$  to effect the change in  $I_B$ , as both  $I_o$  and  $I_{CO}$  can track almost equally according to the change in temperature.



**Fig. 5.24** Diode compensation in voltage-divider bias circuit



**Fig. 5.25** Diode-bias compensation

## 5.7 THERMAL RUNAWAY

---

The collector current for the CE circuit of Fig. 5.2 is given by  $I_C = \beta I_B + (1 + \beta) I_{CO}$ . The three variables in the equation,  $\beta$ ,  $I_B$ , and  $I_{CO}$  increase with rise in temperature. In particular, the reverse saturation current or leakage current  $I_{CO}$  changes greatly with temperature. Specifically, it doubles for every  $10^\circ\text{C}$  rise in temperature. The collector current  $I_C$  causes the collector-base junction temperature to rise which, in turn, increases  $I_{CO}$ , as a result  $I_C$  will increase still further, which will further raise the temperature at the collector-base junction. This process will become cumulative leading to *thermal runaway*. Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

The collector is normally made larger in size than the emitter in order to help dissipate the heat developed at the collector junction.

However, if the circuit is designed such that the base current  $I_B$  is made to decrease automatically with rise in temperature then the decrease in  $\beta I_B$  will compensate for the increase in  $(1 + \beta) I_{CO}$ , keeping  $I_C$  almost constant.

In power transistors, the heat developed at the collector junction may be removed by the use of a heat sink, which is a metal sheet fitted to the collector and whose surface radiates heat quickly.

## 5.8 THERMAL STABILITY

---

**Thermal Resistance** Consider a transistor used in a circuit where the ambient temperature of the air around the transistor is  $T_A$   $^\circ\text{C}$  and the temperature of the collector-base junction of the transistor is  $T_J$   $^\circ\text{C}$ . Due to heating within the transistor,  $T_J$  is higher than  $T_A$ . As the temperature difference  $T_J - T_A$  is greater, the power dissipated in the transistor,  $P_D$  will be greater, i.e.,  $T_J - T_A \propto P_D$ .

This equation can be written as  $T_J - T_A = \Theta P_D$ , where  $\Theta$  is the constant of proportionality and is called the thermal resistance. Rearranging the above equation,  $\Theta = (T_J - T_A)/P_D$ . Hence,  $\Theta$  is measured in  $^\circ\text{C}/\text{W}$  which may be as small as  $0.2\text{ }^\circ\text{C}/\text{W}$  for a high power transistor that has an efficient heat sink or up to  $1,000\text{ }^\circ\text{C}/\text{W}$  for small signal, low power transistors which have no cooling provision.

As  $\Theta$  represents total thermal resistance from a transistor junction to the ambient temperature, it is commonly referred to as  $\Theta_{J-A}$ . However, for power transistors, thermal resistance is given from junction to case,  $\Theta_{J-C}$ .

The amount of power that may be safely dissipated in the transistor is given by

$$P_D = (T_J - T_A)/\Theta_{J-A}$$

or

$$P_D = (T_J - T_C)/\Theta_{J-C}$$

The thermal resistance from junction to ambience is considered to consist of two parts.

$$\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A}$$

which indicates that heat dissipated in the junction must make its way to the surrounding air through two series paths from junction to case and from case to air. Hence, the power dissipated

$$P_D = (T_J - T_A)/\Theta_{J-A} = (T_J - T_A)/(\Theta_{J-C} + \Theta_{C-A})$$

$\Theta_{J-C}$  is determined by the type of manufacture of the transistor and how it is located in the case, but  $\Theta_{C-A}$  is determined by the surface area of the case or flange and its contact with air. If the effective surface area of

the transistor case could be increased, the resistance to heat flow, or  $\Theta_{C-A}$ , could be decreased. This can be achieved by the use of a heat sink.

The heat sink is a relatively large, finned, usually black metallic heat conducting device placed in close contact with the transistor case or flange. Many versions of heat sinks exist depending upon the shape and size of the transistor. Larger the heat sink, smaller will be its thermal resistance,  $\Theta_{HS-A}$ . This thermal resistance is not added to  $\Theta_{C-A}$  in series, but is instead in parallel with it and if  $\Theta_{HS-A}$  is much less than  $\Theta_{C-A}$ , then  $\Theta_{C-A}$  will be reduced significantly, thereby improving the dissipation capability of the transistor.

Thus,

$$\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A} \parallel \Theta_{HS-A}$$

### EXAMPLE 5.28

For a given transistor, the thermal resistance is  $8\text{ }^{\circ}\text{C/W}$  and for the ambient temperature  $T_A$  is  $27\text{ }^{\circ}\text{C}$ . If the transistor dissipates  $3\text{ W}$  of power, calculate the junction temperature  $T_J$ .

**Solution** We know that,  $T_J = T_A + \Theta P_D$

Therefore,

$$T_J = 27\text{ }^{\circ}\text{C} + (8\text{ }^{\circ}\text{C/W}) \times 3\text{W} = 27\text{ }^{\circ}\text{C} + 24\text{ }^{\circ}\text{C} = 51\text{ }^{\circ}\text{C}$$

### EXAMPLE 5.29

For a transistor,  $T_J = 160\text{ }^{\circ}\text{C}$ ,  $T_A = 40\text{ }^{\circ}\text{C}$ , and  $\Theta_{J-A} = 80\text{ }^{\circ}\text{C/W}$ . Calculate the power that the transistor can safely dissipate in free air.

$$P_D = \frac{T_J - T_A}{\Theta_{J-A}} = \frac{160 - 40}{80} = \frac{120}{80} = 1.5\text{ W}$$

### EXAMPLE 5.30

Determine the power-dissipation capability of a transistor which has been mounted with a heat sink having thermal resistance  $\Theta_{HS-A} = 8\text{ }^{\circ}\text{C/W}$ ,  $T_A = 40\text{ }^{\circ}\text{C}$ ,  $T_J = 160\text{ }^{\circ}\text{C}$ ,  $\Theta_{J-C} = 5\text{ }^{\circ}\text{C/W}$ , and  $\Theta_{C-A} = 85\text{ }^{\circ}\text{C/W}$ .

**Solution** We know that,  $\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A} \parallel \Theta_{HS-A}$

$$= 5 + 85 \parallel 8$$

$$= 5 + \frac{85 \times 8}{85 + 8} = 5 + 7.31 = 12.31\text{ }^{\circ}\text{C/W}$$

$$P_D = \frac{T_J - T_A}{\Theta_{J-A}} = \frac{160 - 40}{12.31} = \frac{120}{12.31} = 9.75\text{ W}$$

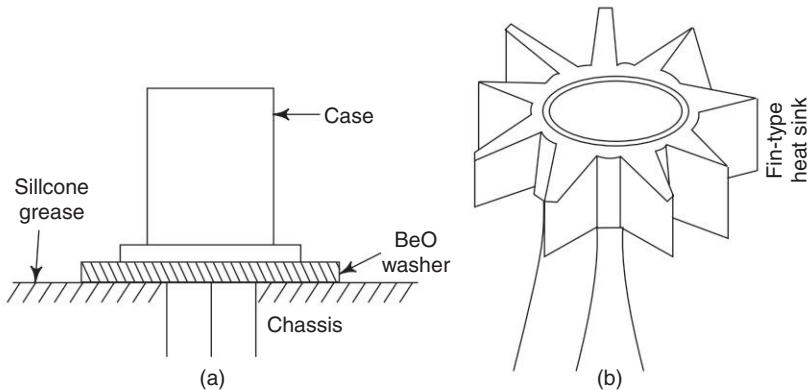
### Types of Heat Sinks

- **Low-power Transistor Type** The small-signal low-power transistors can be mounted directly on the metal chassis to increase the sufficient heat dissipation capability. Care should be taken while doing this because very often the collector of the transistor is connected to the transistor case to increase heat-dissipation capabilities. Hence, some provision for insulating the case from the chassis, which is usually at ground potential, must be provided unless a common collector is being employed.

One method of achieving this is to use a beryllium oxide insulating washer which has a good thermal conductivity, as shown in Fig. 5.26(a). By using a zinc oxide film silicon compound between the washer and

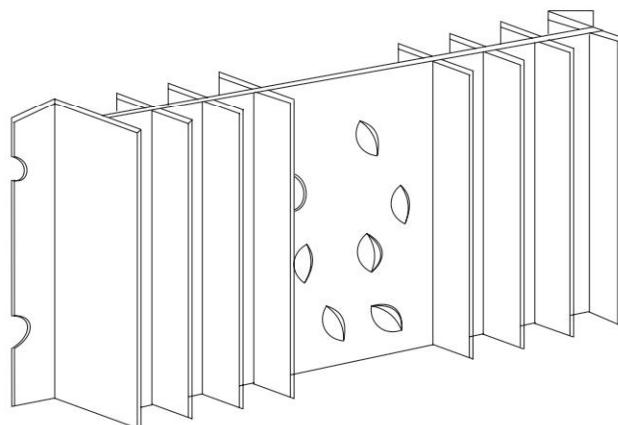
the chassis, heat transfer from the transistor case to the chassis may be improved. An insulated clamp over the top of the transistor may be used to help improve thermal dissipation and increase pressure.

When the transistor is mounted in Teflon (PTFE—Poly Tetra Fluoro Ethylene) sockets, it does not provide thermal conduction from the transistor case to the chassis. Therefore, a press-on fin type of a black anodized heat sink may be used, as shown in Fig. 5.26(b), for mounting transistors that are encased in a metal TO-5 package.



**Fig. 5.26** (a) Mounting the transistor case close to the chassis using a berillium oxide insulating washer (b) Using a separate heat sink pressed onto the transistor

- **Power-Transistor Heat Sinks** The diamond-shaped TO-3 and TO-66 types are the popular mounting packages used for the power transistors which have dissipation in the order of 100 W. These have two leads for emitter and base, but the case, or the mounting flange of the case, is the collector terminal. So, it is necessary to insulate the case from the heat sink by the use of an insulating washer. Figure 5.27 shows a typical heat sink that can accommodate a TO-3 power transistor package that provides cooling by conduction, convection, and radiation. Although measuring only 11.5 cm by 7.8 cm, it has a thermal dissipation equal to that of a flat aluminium sheet 25 cm × 20 cm × 0.32 cm. The thermal resistance of this heat sink is 3°C/W.



**Fig. 5.27** Power-transistor heat sink

## 5.9 FET BIASING – METHODS AND STABILIZATION

---

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point  $Q$  stable in the central portion of the pinch-off region. The  $Q$ -point should be independent of device-parameter variations and ambient temperature changes. This can be achieved by suitably selecting the gate to source voltage ( $V_{GS}$ ) and drain current ( $I_D$ ) which is referred to as biasing.

### 5.9.1 Fixing the $Q$ -point

The  $Q$ -point, the quiescent point or operating point for a self-biased JFET, is established by determining the value of drain current  $I_D$  for a desired value of gate-to-source voltage,  $V_{GS}$ , or vice versa. However, if the data sheet of JFET includes a transfer characteristics curve, then the  $Q$ -point may be determined by using the procedure given below.

- (i) Select a convenient value of drain current whose value is generally taken half of the maximum possible value of drain current,  $I_{DSS}$ . Then find the voltage drop across source resistor,  $R_s$ , by

$$V_s = I_D R_s$$

and the gate-to-source voltage from the equation

$$V_{GS} = -V_s$$

- (ii) Plot the assumed value of drain current,  $I_D$ , and the corresponding gate-to-source voltage,  $V_{GS}$ , on the transfer characteristics curve.
- (iii) Draw a line through the plotted point and the origin. The point of intersection of the line and the curve gives the desired  $Q$ -point. Then, read the coordinates of the  $Q$ -point.

It is necessary to fix the  $Q$ -point near the midpoint of the transfer characteristic curve of a JFET. The midpoint bias allows a maximum amount of drain current swing between the values of  $I_{DSS}$  and the origin.

The following analytical method or graphical method can be used for the design of self-bias circuit.

**Analytical Method** The values of the maximum drain current,  $I_{DSS}$ , and the gate-to-source cut-off voltage,  $V_{GS(\text{off})}$  are noted down from the data sheets of JFET.

The value of the drain current is determined by

$$I_D = \left[ 1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2$$

For example, if we select the gate-to-source voltage,  $V_{GS} = \frac{V_{GS(\text{off})}}{4}$  then the value of the drain current will be

$$I_D = I_{DSS} \{1 - 0.25\}^2 = I_{DSS} (0.75)^2 = 0.56 I_{DSS}$$

Here, the drain current is slightly more than one-half of  $I_{DSS}$ . But it will bias the JFET close to the mid-point of the curve. The value of the drain resistor,  $R_D$ , is selected in such a way that the drain voltage,  $V_D$ , is equal to half the drain supply voltage,  $R_D$ . The value of gate resistor,  $R_G$ , is chosen arbitrarily large, so that it prevents loading on the driving stages.

**Graphical Method** A self-bias line is drawn such that it intersects the transfer characteristic curve near its midpoint giving the required  $Q$ -point. Then the coordinates of the  $Q$ -point are obtained. The value of source resistance,  $R_s$ , is expressed by the ratio of gate-to-source voltage,  $V_{GS}$ , to the drain current,  $I_D$ .

Therefore, the source resistance is given by

$$R_s = \frac{V_{GS}}{I_D}$$

However, a more accurate method is to draw a self-bias line through the coordinates of  $I_{DSS}$  and  $V_{GS(\text{off})}$  as shown in Fig. 5.28. Then the point of intersection of self-bias line and the transfer characteristic curve locates the  $Q$ -point. The value of the source resistor is expressed by the relation

$$R_s = \frac{V_{GS(\text{off})}}{I_{DSS}}$$

The value of drain resistor,  $R_D$ , and the gate resistor,  $R_G$ , are selected in the same way as discussed above for the analytical method.

An FET may have a combination of self-bias and fixed bias to provide stability of the quiescent drain current against device and temperature variations.

### 5.9.2 Self-bias

Figure 5.29 shows the self-bias circuit for an  $N$ -channel FET. When the drain voltage  $V_{DD}$  is applied, a drain current  $I_D$  flows even in the absence of gate voltage ( $V_G$ ). The voltage drop across the resistor  $R_s$  produced by the drain current is given by  $V_s = I_D R_s$ . This voltage drop reduces the gate-to-source reverse voltage required for FET operation. The feedback resistor  $R_s$  prevents any variation in FET drain current.

The drain voltage,  $V_D = V_{DD} - I_D R_D$

The drain-to-source voltage,

$$\begin{aligned} V_{DS} &= V_D - V_s = (V_{DD} - I_D R_D) - I_D R_s \\ &= V_{DD} - I_D(R_D + R_s) \end{aligned}$$

The gate-to-source voltage,

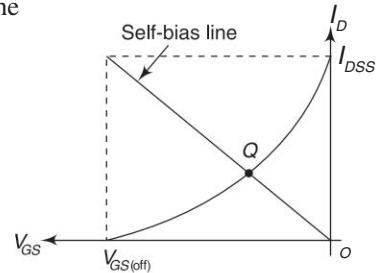
$$V_{GS} = V_{GG} - V_s = 0 - I_D R_s = -I_D R_s$$

When drain current increases, the voltage drop across  $R_s$  increases. The increased voltage drop increases the reverse gate-to-source voltage, which decreases the effective width of the channel and, hence, reduces the drain current. Now, the reduced drain current decreases the gate-to-source voltage which, in turn, increases the effective width of the channel thereby increasing the value of drain current.

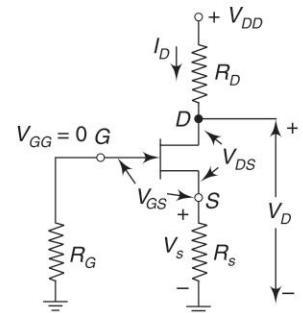
### 5.9.3 Voltage-Divider Bias

Figure 5.30(a) shows the voltage-divider bias circuit and its Thevenin's equivalent is shown in Fig. 5.30(b). Resistors  $R_1$  and  $R_2$  connected on the gate side form a voltage divider. The gate voltage,

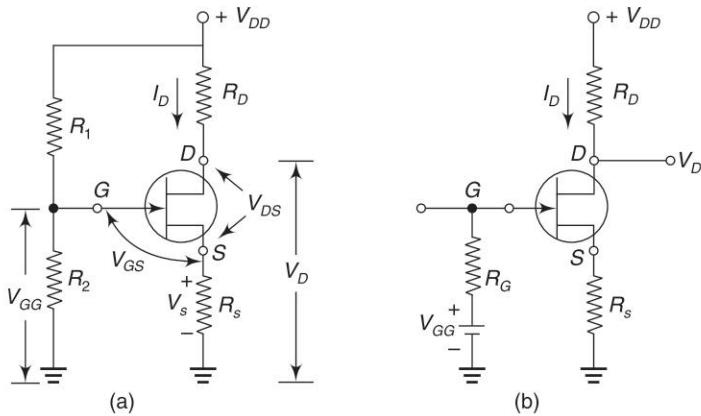
$$V_{GG} = \left( \frac{R_2}{R_1 + R_2} \right) V_{DD} \quad \text{and} \quad R_G = \frac{R_1 R_2}{R_1 + R_2}$$



**Fig. 5.28** Self-bias line through  $I_{DSS}$  and  $V_{GS(\text{off})}$



**Fig. 5.29** Self-bias circuit for an  $N$ -channel JFET



**Fig. 5.30** (a) Voltage-divider bias circuit (b) Thevenin's equivalent circuit

The bias satisfies the equation  $V_{GS} = V_{GG} - I_D R_s$ .

The drain-to-ground voltage,  $V_D = V_{DD} - I_D R_D$ . If the gate voltage  $V_{GG}$  is very large compared to gate-to-source  $V_{GS}$ , the drain current is approximately constant. In practice, the voltage-divider bias is less effective with JFET than BJT.

This is because, in a BJT,  $V_{BE} \approx 0.7$  (silicon) with only minor variations from one transistor to another. But in a JFET, the  $V_{GS}$  can vary several volt from one JFET to another.

#### 5.9.4 Fixed Bias

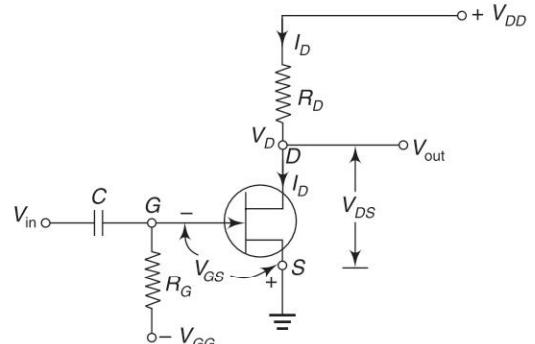
The FET device needs dc bias for setting the gate-to-source voltage  $V_{GS}$  to give desired drain-current  $I_D$ . For a JFET, the drain current is limited by  $I_{DSS}$ . Since the FET has a high input impedance, it does not allow the gate current to flow and the dc voltage of the gate set by a voltage divider or a fixed battery is not affected or loaded by the FET.

The fixed bias circuit for an *N*-channel JFET shown in Fig. 5.31 is obtained by using a supply  $V_{GG}$ . This supply ensures that the gate is always negative with respect to source and no current flows through resistor  $R_G$  and gate terminal, i.e.,  $I_G = 0$ . The  $V_{GG}$  supply provides a voltage  $V_{GS}$  to bias the *N*-channel JFET, but no resulting current is drawn from the battery  $V_{GG}$ . Resistor  $R_G$  is included to allow any ac signal applied through capacitor  $C$  to develop across  $R_G$ . While any ac signal will develop across  $R_G$ , the dc voltage drop across  $R_G$  is equal to  $I_G R_G$  which is equal to zero volt.

Then, the gate to source voltage  $V_{GS}$  is

$$V_{GS} = V_G - V_s = -V_{GG} - 0 = -V_{GG}$$

The drain-source current  $I_D$  is then fixed by the gate-source voltage. This current will cause a voltage drop the drain resistor  $R_D$  and is given as



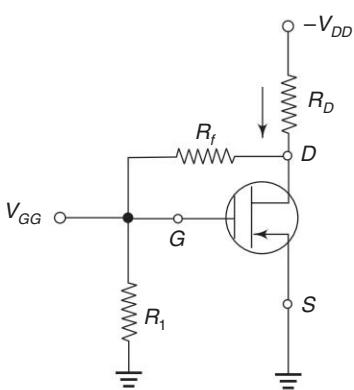
**Fig. 5.31** Fixed bias circuit for an *N*-Channel JFET

$$V_{DD} = I_D R_D + V_{DS}$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

## 5.10 BIASING THE MOSFET

### 5.10.1 Biasing of Enhancement MOSFET



**Fig. 5.32** Drain-to-gate bias circuit for enhancement MOSFET

Figure 5.32 shows the drain-to-gate bias circuit for enhancement mode MOSFET. Here, the gate bias voltage is

$$V_{GS} = \left[ \frac{R_1}{R_1 + R_f} \right] V_{DS}$$

This circuit offers the dc stabilization through the feedback resistor  $R_f$ . However, the input resistance is reduced because of Miller effect.

Also, the voltage-divider biasing technique given for JFET can be used for the enhancement MOSFET. Here, the dc stability is accomplished by the dc feedback through  $R_s$ .

But the self-bias technique given for JFET cannot be used for establishing an operating point for the enhancement MOSFET because the voltage drop across  $R_s$  is in a direction to reverse-bias the gate and it actually needs forward-gate bias.

Figure 5.33 shows an *N*-channel enhancement mode MOSFET common-source circuit with source resistor. The gate voltage is

$$V_G = V_{GS} = \left( \frac{R_2}{R_1 + R_2} \right) (V_{DD})$$

and the gate-to-source voltage is

$$V_{GS} = V_{DD} - V_G$$

Assuming that  $V_{GS} > V_{TN}$  and the MOSFET is biased in the saturation region, the drain current is

$$I_D = K_N (V_{GS} - V_{TN})^2$$

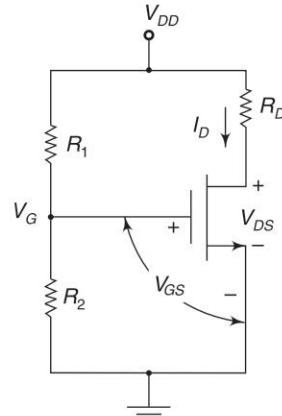
Here, the threshold voltage  $V_{TN}$  and conduction parameter  $K_N$  are functions of temperature.

The drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D$$

If  $V_{DS} > V_{DS(sat)} = V_{GS} - V_{TN}$ , then the MOSFET is biased in the saturation region. If  $V_{DS} < V_{DS(sat)} = V_{GS} - V_{TN}$ , then the MOSFET is biased in the non-saturation region, and the drain current is given by

$$I_D = K_N [2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2]$$



**Fig. 5.33** *N*-channel enhancement mode MOSFET common-source circuit with source resistor

### 5.10.2 Biasing of Depletion MOSFET

Both the self-bias technique and voltage-divider bias circuit given for JFET can be used to establish an operating point for the depletion-mode MOSFET.

#### EXAMPLE 5.31

Calculate the operating point of the self-biased JFET having the supply voltage  $V_{DD} = 20$  V, maximum value of drain current  $I_{DSS} = 10$  mA and  $V_{GS} = -3$  V at  $I_D = 4$  mA. Also, determine the values of resistors  $R_D$  and  $R_s$  to obtain this bias condition.

**Solution** We know that the value of drain current at  $Q$ -point,

$$I_{DQ} = \frac{I_{DSS}}{2} = \frac{10 \times 10^{-3}}{2} = 5 \text{ mA}$$

and the value of drain-to-source voltage at  $Q$ -point,

$$V_{DSQ} = \frac{V_{DD}}{2} = \frac{20}{2} = 10 \text{ V}$$

Therefore, the operating point is at  $V_{DS} = 10$  V and  $I_D = 5$  mA.

Also, we know that the drain-to-source voltage,

$$\begin{aligned} V_{DS} &= V_{DD} - I_D R_D \\ 10 &= 20 - (4 \times 10^{-3}) R_D \end{aligned}$$

$$\text{Therefore, } R_D = \frac{20 - 10}{4 \times 10^{-3}} = 2.5 \text{ k}\Omega$$

The source voltage or voltage across the source resistor  $R_s$  is

$$V_s = -V_{GS} = -3 \text{ V}$$

$$\text{Also, } V_s = I_D R_s, \text{ i.e., } 3 = (4 \times 10^{-3}) R_s$$

$$\text{Therefore, } R_s = \frac{3}{4 \times 10^{-3}} = 750 \Omega$$

#### EXAMPLE 5.32

Calculate the values of  $R_s$  required to self-bias an  $N$ -channel JFET with  $I_{DSS} = 40$  mA,  $V_P = -10$  V and  $V_{GSQ} = -5$  V.

**Solution** We know that,  $I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$

Substituting the given values, we get

$$I_D = 40 \times 10^{-3} \left[ 1 - \frac{(-5)}{(-10)} \right]^2 = 10 \text{ mA}$$

$$\text{Therefore, } R_s = \left| \frac{V_{DSQ}}{I_D} \right| = \frac{5}{10 \times 10^{-3}} = 500 \Omega$$

**EXAMPLE 5.33**

A JFET amplifier with a voltage-divider biasing circuit, shown in Fig. 5.30, has the following parameters:  $V_p = -2$  V,  $I_{DSS} = 4$  mA,  $R_D = 910 \Omega$ ,  $R_s = 3 \text{ k}\Omega$ ,  $R_1 = 12 \text{ M}\Omega$ ,  $R_2 = 8.57 \text{ M}\Omega$  and  $V_{DD} = 24$  V. Find the value of the drain current  $I_D$  at the operating point. Verify whether the FET will operate in the pinch-off region.

**Solution**

We obtain,

$$V_{GG} = V_{DD} \frac{R_2}{R_1 + R_2} = 24 \times \frac{8.57 \times 10^6}{(12 + 8.57) \times 10^6} = 10 \text{ V}$$

We know that,

$$\begin{aligned} I_D &= I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2 \\ &= I_{DSS} \left( 1 - \frac{V_{GG} - I_D R_s}{V_p} \right)^2, \text{ where } V_{GS} = V_{GG} - I_D R_s \end{aligned}$$

Expressing  $I_D$  and  $I_{DSS}$  in mA and  $R_s$  in  $\text{k}\Omega$ , we have

$$I_D = 4 \times \left( 1 - \frac{10 - I_D \times 3}{-2} \right)^2$$

$$\text{i.e., } 9I_D^2 - 73I_D + 144 = 0$$

$$\text{Therefore, } I_D = 3.39 \text{ mA or } 4.72 \text{ mA}$$

As  $I_D = 4.72 \text{ mA} > 4 \text{ mA} = I_{DSS}$ , this value is inappropriate. So,  $I_{DQ} = 3.39 \text{ mA}$  is selected.

Therefore,

$$\begin{aligned} V_{GSQ} &= V_{GG} - I_{DQ} R_s \\ &= 10 - (3.39 \times 10^{-3} \times 3 \times 10^3) = -0.17 \text{ V} \end{aligned}$$

and

$$\begin{aligned} V_{DSQ} &= V_{DD} - I_{DQ} (R_D + R_s) \\ &= 24 - 3.39 \times 10^{-3} (0.91 + 3) \times 10^3 = 10.745 \text{ V} \end{aligned}$$

Then

$$\begin{aligned} V_{DGQ} &= V_{DSQ} - V_{GQS} \\ &= 10.745 + 0.17 = 10.915 \text{ V} \end{aligned}$$

which is greater than  $|V_p| = 2$  V. Hence, the FET is in the pinch-off region.

**EXAMPLE 5.34**

A voltage-divider bias is provided to an *N*-channel JFET circuit as shown in Fig. 5.34. To establish  $I_{DSS} = 10$  mA,  $V_p = -3.5$  V,  $R_1 + R_2 = 20 \text{ k}\Omega$ ,  $I_D = 5$  mA and  $V_{DS} = 5$  V, determine the values of  $R_1$ ,  $R_2$  and  $R_D$ .

**Solution**

Let us assume that the JFET is biased in the saturation region. Then the dc drain current is given by

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$$

Therefore,

$$5 = 10 \left( 1 - \frac{V_{GS}}{(-3.5)} \right)^2$$

By solving, we get  $V_{GS} = -1.008 \text{ V}$

The voltage at the source terminal is

$$V_s = I_D R_s - 5 = (5 \times 10^{-3}) (0.5 \times 10^3) - 5 = -2.5 \text{ V}$$

The gate voltage is

$$V_G = V_{GS} + V_s = -1.008 - 2.5 = -3.508 \text{ V}$$

The gate voltage can be written as

$$V_G = \left( \frac{R_2}{R_1 + R_2} \right) (10) - 5$$

Therefore,

$$-3.508 = \frac{R_2}{20 \times 10^3} (10) - 5$$

i.e.,

$$R_2 = 2.984 \text{ k}\Omega$$

and

$$R_1 = 117.016 \text{ k}\Omega$$

The drain-to-source voltage is

$$V_{DS} = 5 - I_D R_D - I_D R_s - (-5)$$

Substituting the specified values, we get

$$R_D = \frac{10 - V_{DS} - I_D R_s}{I_D} = \frac{10 - 5 - (5)(0.5)}{5} = 0.5 \text{ k}\Omega$$

$$V_{GS} - V_P = -1.24 - (-3.5) = 2.26 \text{ V}$$

Here, since  $V_{DS} > (V_{GS} - V_P)$ , the JFET is biased in the saturation region, which satisfies the initial assumption.

### EXAMPLE 5.35

For the circuit shown in Fig. 5.35, find the values of  $V_{DS}$  and  $V_{GS}$ . Given,  $I_D = 5 \text{ mA}$ ,  $V_{DD} = 10 \text{ V}$ ,  $R_D = 1 \text{ k}\Omega$  and  $R_s = 500 \Omega$ .

#### Solution

$$V_{GG} = V_{GS} + I_D R_s$$

Since

$$V_{GG} = 0,$$

$$\begin{aligned} V_{GS} &= -I_D R_s \\ &= -5 \times 10^{-3} \times 500 \\ &= -2.5 \text{ V} \end{aligned}$$

We know that,

$$V_{DD} = I_D (R_D + R_s) + V_{DS}$$

Therefore,

$$\begin{aligned} V_{DS} &= V_{DD} - I_D (R_D + R_s) \\ &= 10 - 5 \times 10^{-3} (1500) = 2.5 \text{ V} \end{aligned}$$

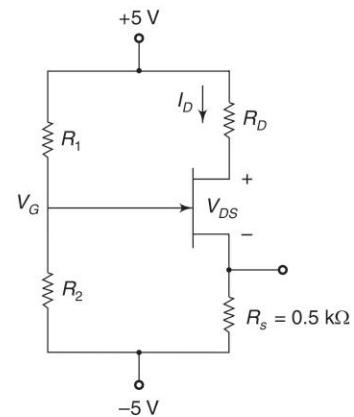


Fig. 5.34

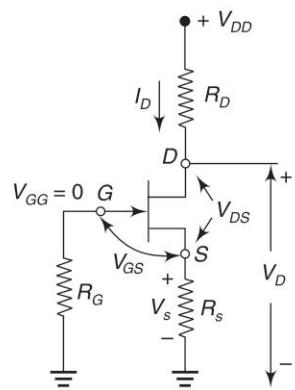


Fig. 5.35

**EXAMPLE 5.36**

Determine the following for the network shown in Fig. 5.36.

- (a)  $V_{GSQ}$  (b)  $V_{DS}$  (c)  $V_D$  (d)  $V_G$  (e)  $V_s$

**Solution**

$$(a) \quad V_{GSQ} = -V_{GG} = -3V$$

$$(b) \quad I_{DQ} = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

$$= 12 \times 10^{-3} \left[ 1 - \left( \frac{-3}{-6} \right) \right]^2 = 3 \text{ mA}$$

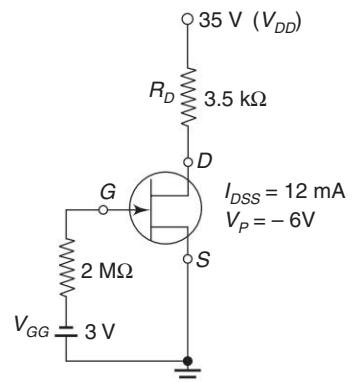
$$V_{DS} = V_{DSQ} = V_{DD} - I_{DQ}R_D$$

$$= 35 - 3 \times 10^{-3} \times 3.5 \times 10^3 = 24.5 \text{ V}$$

$$(c) \quad V_D = V_{DS} + V_s = 24.5 + 0 = 24.5 \text{ V}$$

$$(d) \quad V_G = -3V$$

$$(e) \quad V_s = 0 \text{ V}$$

**Fig. 5.36****EXAMPLE 5.37**

Determine  $I_{DQ}$ ,  $V_{GSQ}$ ,  $V_D$ ,  $V_{DS}$ , and  $V_{DG}$  for the given network shown in Fig. 5.37.

**Solution** To find expression for  $V_{GS}$ 

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{270 \times 10^3}{(2100 + 270) \times 10^3} \times 20 = 2.28 \text{ V}$$

$$V_s = 1.5 I_D$$

$$\text{Therefore, } V_{GS} = V_G - V_s = (2.28 - 1.5 I_D)$$

To find  $I_D$ :

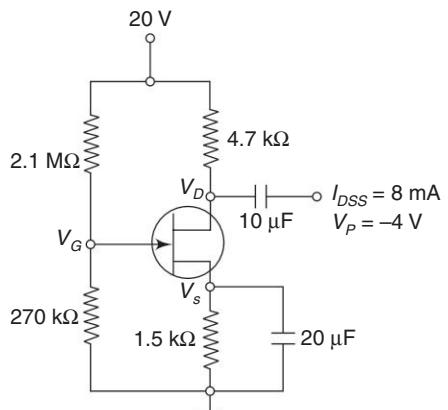
$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2 \text{ mA}$$

$$I_D = 8 \left[ 1 - \frac{(2.28 - 1.5 I_D)}{-4} \right]^2 \text{ mA}$$

$$\text{Therefore, } I_D = \frac{8}{16} [4 + 2.28 - 1.5 I_D]^2 = 0.5 (6.28 - 1.5 I_D)^2$$

$$2I_D = 39.44 - 18.84 I_D + 2.25 I_D^2$$

$$2.25 I_D^2 - 20.84 I_D + 39.44 = 0$$

**Fig. 5.37**

Therefore,

$$I_D = \frac{20.84 \pm \sqrt{(20.84^2 - (4 \times 2.25 \times 39.44)}}{2 \times 2.25} = 6.6 \text{ mA or } 2.6 \text{ mA}$$

For  $I_D = 6.6 \text{ mA}$ ,  $V_{DS} = V_{DD} - I_D(R_D + R_s)$   
 $= 20 - 6.6 \times 10^{-3} (4.7 + 15) \times 10^3 = -20.92$

Since  $V_{DS}$  is negative, this value may be neglected. Let us choose  $I_D = 2.65 \text{ mA}$ .

Therefore,  $I_{DQ} = 2.65 \text{ mA}$ .

To find  $V_{GSQ}$ :

$$V_{GSQ} = 2.28 - 1.5 I_{DQ} = 2.28 - (1.5 \times 2.65) = -1.695 \text{ V}$$

To find  $V_{DSQ}$ :

$$V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_s)$$

Therefore,

$$V_{DSQ} = 20 - 2.65 \times 10^{-3} (4.7 + 1.5) \times 10^3 = 3.57 \text{ V}$$

To find  $V_D$ ,  $V_s$  and  $V_{DG}$ :

$$V_s = I_D R_s = 2.65 \times 10^{-3} \times 1.5 \times 10^3 = 3.975 \text{ V}$$

$$V_D = V_s + V_{DS} = 3.975 + 3.57 = 7.545 \text{ V}$$

Hence,

$$V_{DG} = V_D - V_G = 7.545 - 2.28 = 5.265 \text{ V}$$

### EXAMPLE 5.38

For the given measurement  $V_s = 1.7 \text{ V}$  for the network as shown in Fig. 5.38, determine

- (a)  $I_{DQ}$
- (b)  $V_{GSQ}$
- (c)  $I_{DSS}$
- (d)  $V_D$
- (e)  $V_{DS}$

**Solution** Given,  $V_s = 1.7 \text{ V}$

(a)  $V_s = I_D R_s$

$$I_{DQ} = \frac{V_s}{R_s} = \frac{1.7}{510} = 3.33 \text{ mA}$$

(b)  $V_{GSQ} = V_G - V_s = -V_s = -1.7 \text{ V}$

(c)  $I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$

$$I_{DSS} = \frac{I_D}{\left( 1 - \frac{V_{GS}}{V_P} \right)^2} = \frac{3.33 \times 10^{-3}}{\left( 1 - \frac{(-1.7)}{(-4)} \right)^2} = 10 \text{ mA}$$

(d)  $V_D = V_{DD} - I_D R_D = 18 - 3.33 \times 10^{-3} \times 2 \times 10^3 = 11.34 \text{ V}$

(e)  $V_{DS} = V_D - V_s = 11.34 - 1.7 = 9.64 \text{ V}$

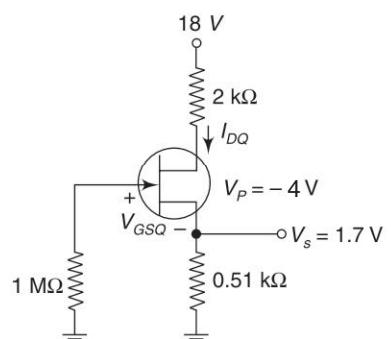


Fig. 5.38

**EXAMPLE 5.39**

For the circuit shown in Fig. 5.39, calculate  $V_0$ ,  $Z_i$ , and  $Z_o$ . Given input is  $V_i = 0.2$  V(rms),  $I_{DSS} = 9$  mA and  $V_P = -4.5$  V.

**Solution**

$$Z_i = R_G = 10 \text{ M}\Omega$$

$$\begin{aligned} I_D &= I_{DD} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \\ &= 9 \times 10^{-3} \left( 1 - \frac{-I_D R_s}{V_P} \right)^2 \\ &= 9 \times 10^{-3} \left( 1 - \frac{(-1000 I_D)}{-4.5} \right)^2 \\ &= 9 \times 10^{-3} (1 - 222.22 I_D)^2 \\ &= 9 \times 10^{-3} (1 - 444.44 I_D + 49383 I_D^2) \\ I_D &= 9 \times 10^{-3} - 4I_D + 444.45 I_D^2 \end{aligned}$$

$$\text{Therefore, } 444.45 I_D^2 - 5I_D + 9 \times 10^{-3} = 0$$

Solving the quadratic equation, we get

$$I_D = 2.25 \text{ mA or } 9 \text{ mA}$$

Since  $I_D < I_{DSS}$ , we take  $I_D = 2.25$  mA. Therefore,

$$g_{mo} = \frac{2I_{DSS}}{|V_P|} = \frac{2 \times (9 \times 10^{-3})}{4.5} = 4 \text{ mS}$$

$$g_m = g_{mo} \left( 1 - \frac{V_{GSQ}}{V_P} \right)$$

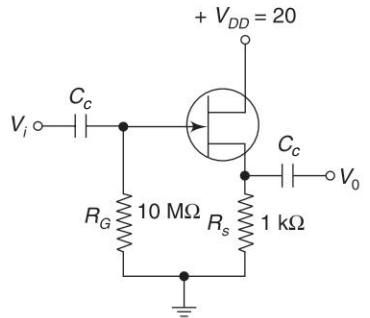
$$\text{where } V_{GSQ} = -I_D R_s = -2.25 \times 10^{-3} \times 1000 = -2.25 \text{ V}$$

$$g_m = 4 \times 10^{-3} \left( 1 - \frac{(2.25)}{(-4.5)} \right) = 2 \text{ mS}$$

$$Z_o = \frac{1}{g_m} \| R_s = \frac{1}{2 \times 10^{-3}} \| 1 \times 10^3 = 333.33 \Omega$$

$$A_V = \frac{g_m (r_d \| R_s)}{1 + g_m (r_d \| R_s)} = \frac{g_m R_s}{1 + g_m R_s} = \frac{2 \times 10^{-3} \times 1 \times 10^3}{1 + (2 \times 10^{-3} \times 1 \times 10^3)} = 0.667$$

$$V_o = V_i \times A_V = 0.2 \times 0.667 = 0.133 \text{ V}$$



**Fig. 5.39**

**EXAMPLE 5.40**

An *N*-channel JFET having  $V_P = -4$  V and  $I_{DSS} = 10$  mA is used in the circuit of Fig. 5.40. The parameter values are  $V_{DD} = 18$  V,  $R_s = 2\text{k}\Omega$ ,  $R_1 = 450\text{k}\Omega$ , and  $R_2 = 90\text{k}\Omega$ . Determine  $I_D$  and  $V_{DS}$ .

**Solution**

To find  $V_{GS}$

$$V_{GS} = V_G - I_D R_s$$

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{90 \times 10^3}{(450 + 90) \times 10^3} \times 18 = 3 \text{ V}$$

Therefore,  $V_{GS} = (3 - 2 \times 10^3 I_D)$

To find  $I_D$

$$\begin{aligned} I_D &= I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2 = 10 \times 10^{-3} \left[ 1 - \frac{(3 - 2 \times 10^3 I_D)}{-4} \right]^2 \\ &= \frac{10 \times 10^{-3}}{16} [-4 - 3 + 2 \times 10^3 I_D]^2 \end{aligned}$$

Therefore,  $1.6 I_D = 10^{-3} [-7 - 2 \times 10^3 I_D]^2$

$$= 0.049 - 28 I_D + 4 \times 10^3 I_D^2$$

$$4 \times 10^3 I_D^2 - 29.6 I_D + 0.049 = 0$$

$$I_D = \frac{29.6 \pm \sqrt{(29.6)^2 - 4 \times 4 \times 10^3 \times 0.049}}{2 \times 4 \times 10^3}$$

Therefore,  $I_D = 4.9$  mA or  $2.5$  mA

If  $I_D = 4.9$  mA, then

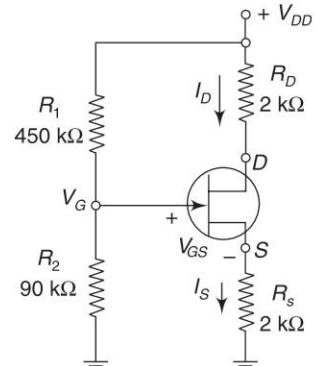
$$\begin{aligned} V_{DS} &= V_{DD} - I_D (R_D + R_S) \\ &= 18 - 4.9 \times 10^{-3} (2 + 2) \times 10^3 = -3.6 \text{ V} \end{aligned}$$

Since  $V_{DS}$  would be negative, this value of  $I_D$  is not acceptable

Therefore,  $I_{DQ} = 2.5$  mA

To find  $V_{DS}$

$$V_{DS} = V_{DD} - I_{DQ}(R_D + R_S) = 18 - 2.5 \times 10^{-3} (2 + 2) \times 10^3 = 8 \text{ V}$$



**Fig. 5.40**

**EXAMPLE 5.41**

Determine  $V_{GS}$ ,  $I_D$ ,  $V_{DS}$ ,  $V_D$  and  $V_G$  for the circuit shown in Fig. 5.41.

**Solution**

To find  $V_{GSQ}$

For a self-bias circuit,  $V_{GSQ} = -I_D R_s = -I_D \times 10^3$

To find  $I_D$

$$\begin{aligned} I_D &= I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2 = 8 \times 10^{-3} \left[ 1 + \frac{(1 \times 10^3 I_D)}{-6} \right]^2 \\ &= 8 \times 10^{-3} \left[ 1 - \frac{1000 I_D}{6} \right]^2 \end{aligned}$$

Therefore,  $36 I_D = 8 \times 10^{-3} [6 - 1000 I_D]^2$

$$= 8 \times 10^{-3} [36 - 12 \times 10^3 I_D + 10^6 I_D^2]$$

Hence,  $8 \times 10^3 I_D^2 - 132 I_D + 0.288 = 0$

$$I_D = \frac{132 \pm \sqrt{(132)^2 - 4 \times 8 \times 10^3 \times 0.288}}{2 \times 8 \times 10^3}$$

Therefore,  $I_D = 13.9 \text{ mA or } 2.5 \text{ mA}$

But  $I_D$  cannot be higher than  $I_{DSS}$ , Therefore,  $I_D = 2.5 \text{ mA}$

To find  $V_{DS}$

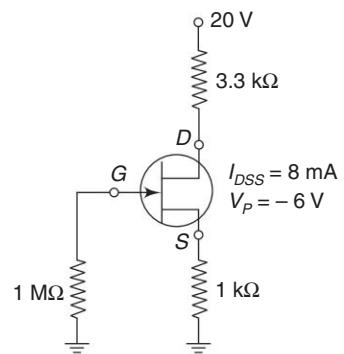
$$V_{DS} = V_{DD} - I_D (R_D + R_s) = 20 - 2.5 \times 10^{-3} (3.3 + 1) \times 10^3 = 9.25 \text{ V}$$

To find  $V_{GS}$ ,  $V_D$  and  $V_s$

$$V_{GS} = 1 \times 10^3 \times I_D = 1 \times 10^3 \times 2.5 \times 10^{-3} = 2.5 \text{ V}$$

$$V_s = I_D R_s = 2.5 \times 10^{-3} \times 1 \times 10^3 = 2.5 \text{ V}$$

$$V_D = V_s + V_{DS} = 2.5 + 9.25 = 11.75 \text{ V}$$



**Fig. 5.41**

### EXAMPLE 5.42

For the network shown in Fig. 5.42, determine the values of  $V_{DSQ}$ ,  $I_{DQ}$ ,  $V_D$ ,  $V_G$ ,  $V_S$  and  $V_{DS}$ .

**Solution**

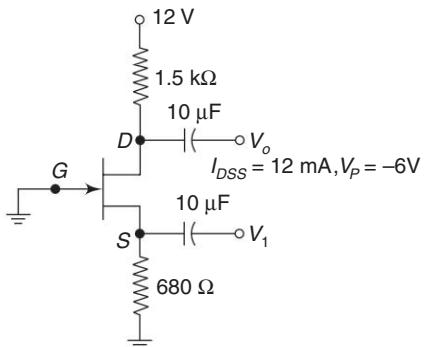
$$V_G = 0, V_s = I_D R_s$$

$$V_{GS} = V_G - V_s = 0 - I_D R_s = -680 I_D$$

To find  $I_D$

$$\begin{aligned} \text{We know that, } I_D &= I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \\ &= 12 \times 10^{-3} \left( 1 - \left( \frac{-680 I_D}{-6} \right) \right)^2 \\ &= 154.12 I_D^2 - 3.7 I_D + 0.012 = 0 \end{aligned}$$

$$\text{Therefore, } I_D = \frac{3.7 \pm \sqrt{13.69 - 7.39}}{308.24} = 20 \text{ mA or } 3.8 \text{ mA}$$



**Fig. 5.42**

Since  $I_D$  is less than  $I_{DSS}$ ,  $I_{DQ} = 3.8 \text{ mA}$

To find  $V_{GSQ}$

$$V_{GSQ} = -680 I_D = -680 \times 3.8 \times 10^{-3} = -3.6 \text{ V}$$

To find  $V_s$

$$V_s = I_D R_s = 3.8 \times 10^{-3} \times 680 = 2.58 \text{ V}$$

To find  $V_{DS}$

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_s) \\ &= 12 - 3.8 \times 10^{-3} (1.5 \times 10^3 + 680) = 12 - 8.28 = 3.72 \text{ V} \end{aligned}$$

To find  $V_D$

$$V_D = V_s + V_{DS} = 2.58 + 3.72 = 6.3 \text{ V}$$

### EXAMPLE 5.43

For the common-source  $N$ -channel MOSFET circuit shown in Fig. 5.43(a) with the threshold voltage  $V_{TN} = 1.5 \text{ V}$ , conduction parameter  $K_N = 1 \text{ mA/V}^2$ , the channel-length modulation parameter  $\lambda = 0.01 \text{ V}^{-1}$ ,  $R_i = R_1 \parallel R_2 = 100 \text{ k}\Omega$  and the current at the transition point  $I_{Dt} = 4 \text{ mA}$ . Design the MOSFET circuit with voltage-divider bias such that  $I_{DQ} = 1.5 \text{ mA}$  and  $Q$ -point is in the middle of the saturation region.

#### Solution

To determine  $V_{DSI}$

We know that,  $I_{Dt} = K_N(V_{GSt} - V_{TN})^2$

$$\text{i.e., } 4 \times 10^{-3} = 1 \times 10^{-3} (V_{GSt} - 1.5)^2$$

where the subscript  $t$  indicates transition point values.

Solving, we get  $V_{GSt} = 3.5 \text{ V}$

Therefore,  $V_{DSI} = V_{GSt} - V_{TN} = 3.5 - 1.5 = 2 \text{ V}$

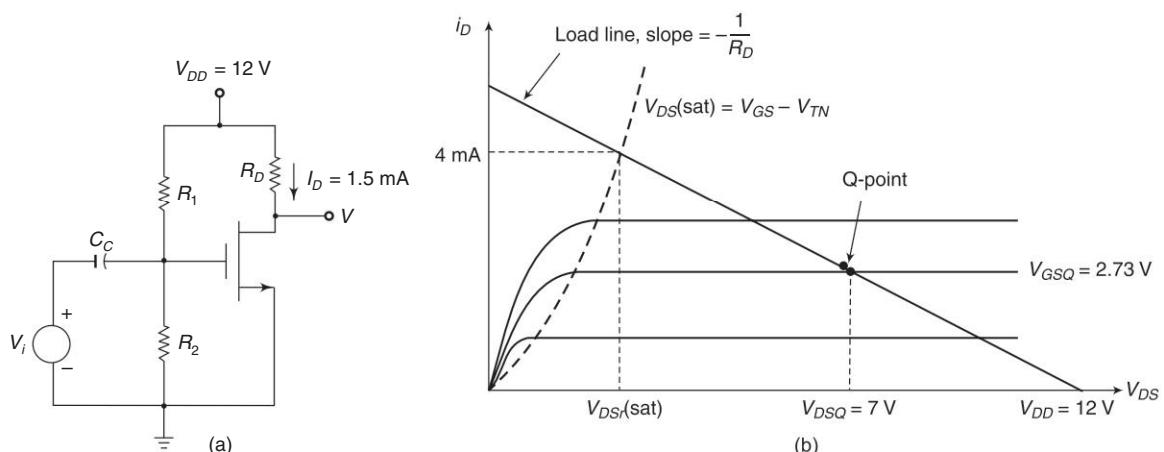


Fig. 5.43

Referring to Fig. 5.43(b), if the  $Q$ -point is in the middle of the saturation region then  $V_{DSQ} = 7$  V, which gives 10 V peak-to-peak symmetrical output voltage.

Therefore,  $V_{DSQ} = V_{DD} - I_{DQ}R_D$

$$\text{i.e., } R_D = \frac{V_{DD} - V_{DSQ}}{I_{DQ}} = \frac{12 - 7}{1.5 \times 10^{-3}} = 3.33 \text{ k}\Omega$$

Then,  $I_{DQ} = K_N(V_{GSQ} - V_{TN})^2$

$$1.5 \times 10^{-3} = 1 \times 10^{-3} (V_{GSQ} - 1.5)^2$$

Therefore,  $V_{GSQ} = 2.73$  V

$$\text{Then, } V_{GSQ} = 2.73 = \left( \frac{R_2}{R_1 + R_2} \right) (V_{DD}) = \left( \frac{1}{R_1} \right) \left( \frac{R_1 R_2}{R_1 + R_2} \right) (V_{DD})$$

$$2.73 = \frac{R_i}{R_1} (V_{DD}) = \frac{(100 \times 10^3)(12)}{R_1}$$

By solving, we get  $R_1 = 439.6$  k $\Omega$  and  $R_2 = 129.45$  k $\Omega$

#### EXAMPLE 5.44

For the  $N$ -channel depletion-mode MOSFET circuit shown in Fig. 5.44.  $V_{TN} = -2$  V and  $K_N = 0.1$  mA/V $^2$ . Assume that  $V_{DD} = 5$  V and  $R_s = 5$  k $\Omega$ . Determine  $I_D$  and  $V_{DS}$ .

**Solution** Let us assume that the MOSFET is biased in the saturation region. Then the dc drain current is

$$\begin{aligned} I_D &= K_N(V_{GS} - V_{TN})^2 \\ &= K_N(-V_{TN})^2 \\ &= (0.1)(-(-2))^2 = 0.4 \text{ mA} \end{aligned}$$

The dc drain-to-source voltage is

$$\begin{aligned} V_{DS} &= V_{DD} - I_D R_s \\ &= 5 - (0.4)(5) = 3 \text{ V} \end{aligned}$$

Then,

$$\begin{aligned} V_{DS(\text{sat})} &= V_{GS} - V_{TN} \\ &= 0 - (-2) = 2 \text{ V} \end{aligned}$$

Since  $V_{DS} > V_{DS(\text{sat})}$ , the MOSFET is biased in the saturation region.

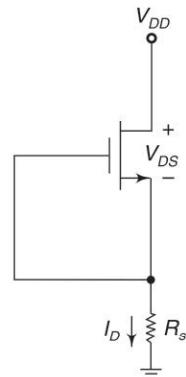


Fig. 5.44

#### REVIEW QUESTIONS

- What is meant by  $Q$ -point?
- What is the need for biasing a transistor?
- What factors are to be considered for selecting the operating point  $Q$  for an amplifier?
- Distinguish between dc and ac load lines with suitable diagrams.

5. Briefly explain the reasons for keeping the operating point of a transistor fixed.
6. What is thermal runaway? How can it be avoided?
7. What three factors contribute to thermal instability?
8. Define 'stability factor.' Why would it seem more reasonable to call this an instability factor?
9. Draw a fixed-bias circuit and derive an expression for the stability factor.
10. If the coordinates of the operating point of a CE amplifier using fixed bias or base-resistor method of biasing are  $V_{CE} = 6$  V and  $I_C = 1$  mA, determine the value of  $R_C$  and  $R_B$ . [Ans.  $R_C = 3$  kΩ,  $R_B = 300$  kΩ]
11. Consider a common emitter NPN transistor with fixed bias as shown in Fig. 5.28. If  $\beta = 80$ ,  $R_B = 390$  kΩ,  $R_C = 1.5$  kΩ, and  $V_{CC} = 30$  V, find the coordinates of the Q-point. [Ans. 21 V, 6 mA]
12. A germanium transistor having  $\beta = 100$  and  $V_{BE} = 0.2$  V is used in a fixed-bias amplifier circuit where  $V_{CC} = 16$  V,  $R_C = 5$  kΩ and  $R_B = 790$  kΩ. Determine its operating point.
13. Derive an expression for the stability factor of a collector-to-base bias circuit.
14. Mention the disadvantages of collector-to-base bias. Can they be overcome?
15. In a germanium transistor CE amplifier biased by feedback resistor method,  $V_{CC} = 20$  V,  $V_{BE} = 0.2$  V,  $\beta = 100$  and the operating point is chosen such that  $V_{CE} = 10.4$  V and  $I_C = 9.9$  mA. Determine the values of  $R_B$  and  $R_C$ . [Ans. 100 kΩ, 1 kΩ]
16. Draw a circuit diagram of CE transistor amplifier using emitter biasing. Describe qualitatively the stability action of the circuit.
17. Draw a voltage-divider bias circuit and derive an expression for its stability factor.
18. Why does the potential divider method of biasing become universal?
19. If the various parameters of a CE amplifier which uses the self-bias method are  $V_{CC} = 12$  V,  $R_1 = 10$  kΩ,  $R_2 = 5$  kΩ,  $R_C = 1$  kΩ,  $R_E = 2$  kΩ and  $\beta = 100$ , find (i) the coordinates of the operating point, and (ii) the stability factor, assuming the transistor to be of silicon. [Ans.  $V_{CE} = 7.05$  V,  $I_C = 1.65$  mA,  $S = 2.62$ ]
20. In a CE germanium transistor amplifier using self-bias circuit,  $R_C = 2.2$  kΩ,  $\beta = 50$ ,  $V_{CC} = 9$  V and the operating point is required to be set at  $I_C = 2$  mA and  $V_{CE} = 3$  V. Determine the values of  $R_1$ ,  $R_2$  and  $R_E$ . [Ans.  $R_1 = 17.75$  kΩ,  $R_2 = 4.75$  kΩ,  $R_E = 800$  Ω]
21. Determine the operating point for the circuit of a potential-divider bias arrangement with  $R_2 = R_C = 5$  kΩ,  $R_E = 1$  kΩ and  $R_1 = 40$  kΩ. [Ans.  $V_{CE} = 6$  V,  $I_C = 1$  mA]
22. Calculate the values of  $R_1$  and  $R_C$  in the voltage-divider bias circuit so that Q-point is at  $V_{CE} = 6$  V and  $I_C = 2$  mA. Assume the transistor parameters are:  $\alpha = 0.985$ ,  $I_{CBO} = 4$  μA and  $V_{BE} = 0.2$  V. [Ans.  $R_C = 3$  kΩ,  $R_1 = 5.54$  kΩ]
23. Determine the stability factor for a CB amplifier circuit.
24. Draw a circuit which uses a diode to compensate for changes in  $I_{CO}$ . Explain how stabilization is achieved in the circuit.
25. How will you provide temperature compensation for the variations of  $V_{BE}$  and stabilization of the operating point?
26. What is the principle of providing thermal stabilization by means of different methods of transistor biasing? How does this differ from the compensation techniques using a diode or thermistor or sensistor?
27. What is thermal resistance? What is the unit of thermal resistance?
28. What is a heat sink? How does it contribute to increase in power dissipation?
29. Why are power transistors provided with heat sinks?
30. Briefly explain the commonly available heat sinks.
31. Determine the values of resistors  $R_D$  and  $R_s$  for a self-biased P-channel JFET having the following parameters:  $V_p = 5$  V,  $I_{DSS} = 12$  mA,  $V_{DD} = 12$  V,  $I_D = 5$  mA and  $V_{DS} = 6$  V. [Ans.  $R_D = 1.5$  kΩ;  $R_s = 525\Omega$ ]
32. Determine the value of  $R_s$  required to self-bias an N-channel JFET with  $I_{DSS} = 50$  mA,  $V_p = -10$  V and  $V_{GSQ} = -5$  V. [Ans.  $R_s = 400$  Ω]

33. In a self-bias  $N$ -channel JFET circuit, the operating point is to be set at  $I_D = 1.5$  mA and  $V_{DS} = 10$  V. The JFET parameters are  $I_{DSS} = 5$  mA and  $V_P = -2$  V. Find the values of  $R_s$  and  $R_D$ . Given that  $V_{DD} = 20$  V.  
 [Ans.  $R_s = 0.6$  k $\Omega$ ,  $R_D = 6$  k $\Omega$ ]
34. In an  $N$ -channel JFET biased by potential divider method, it is desired to set the operating point at  $I_D = 2.5$  mA and  $V_{DS} = 8$  V. If  $V_{DD} = 30$  V,  $R_1 = 1$  M $\Omega$  and  $R_2 = 500$  k $\Omega$ . Find the value of  $R_s$ . The parameters of JFET are  $I_{DSS} = 10$  mA and  $V_P = -5$  V.  
 [Ans.  $R_s = 5$  k $\Omega$ ]
35. Draw two biasing circuits for an enhancement type MOSFET.
36. Explain how an FET is used as a voltage variable resistor.

### OBJECTIVE-TYPE QUESTIONS

1. The internal resistance of a current source used in the model of a BJT while analyzing a circuit using BJT is
 

(a) very high	(b) very low
(c) zero	(d) of the order of a few mega-ohms
2. The common-emitter short-circuit current gain  $\beta$  of a transistor
 

(a) is a monotonically increasing function of the collector current $I_C$ .	(b) is a monotonically decreasing function of $I_C$ .
(c) increases with $I_C$ , for low $I_C$ , reaches a maximum and then decreases with further increase in $I_C$ .	(d) is not a function of $I_C$ .
3. The resistance of thermistor
 

(a) decreases exponentially with increase of temperature	(b) decreases exponentially with decrease of temperature
(c) increases exponentially with increase of temperature	(d) increases exponentially with decrease of temperature
4. If the base resistor is shorted in the fixed-bias circuit, then
 

(a) the transistor may get damaged	(b) the base voltage will be zero
(c) the collector voltage will be equal to the supply voltage	(d) the collector current is zero



# Small Signal Low Frequency Transistor Amplifier Models (BJT and FET)

## 6.1 INTRODUCTION

The equivalent circuit for a transistor can be drawn using simple approximations by retaining its essential features, at the same time discarding its less important qualities. These equivalent circuits will aid in analyzing transistor circuits easily and rapidly. In this chapter, small-signal equivalent circuits of the transistor are derived. Small-signal operation is that in which the ac input signal voltages and currents are in the order of  $\pm 10\%$  of  $Q$ -point voltages and currents.

## 6.2 BJT AS A TWO PORT NETWORK

A transistor can be treated as a two-port network. The terminal behaviour of any two-port network can be specified by the terminal voltages  $v_1$  and  $v_2$  at ports 1 and 2, respectively, and currents  $i_1$  and  $i_2$ , entering ports 1 and 2, respectively, as shown in Fig. 6.1. Of these four variables  $v_1$ ,  $v_2$ ,  $i_1$ , and  $i_2$ , two can be selected as independent variables and the remaining two can be expressed in terms of these independent variables. This leads to various two-port parameters out of which the following three are more important.

- (i) Z-parameters or impedance parameters
- (ii) Y-parameters or admittance parameters
- (iii) h-parameters or hybrid parameters.



**Fig. 6.1** Two-port network

### 6.2.1 Z-Parameters or Impedance Parameters

Here,  $i_1$  and  $i_2$  are taken as independent variables. The voltages  $v_1$  and  $v_2$  are given by the equations

$$v_1 = Z_{11}i_1 + Z_{12}i_2 \quad (6.1)$$

$$v_2 = Z_{21}i_1 + Z_{22}i_2 \quad (6.2)$$

These four impedance parameters,  $Z_{11}$ ,  $Z_{22}$ ,  $Z_{12}$ , and  $Z_{21}$  are defined as follows:

$$Z_{11} = \left[ \frac{v_1}{i_1} \right] \text{ with } i_2 = 0$$

= input impedance with output port open-circuited

$$Z_{22} = \left[ \frac{v_2}{i_2} \right] \text{ with } i_1 = 0$$

= output impedance with input port open-circuited

$$Z_{12} = \left[ \frac{v_1}{i_2} \right] \text{ with } i_1 = 0$$

= reverse transfer impedance with Port 1 open-circuited

$$Z_{21} = \left[ \frac{v_2}{i_1} \right] \text{ with } i_2 = 0$$

= forward transfer impedance with Port 2 open-circuited.

### 6.2.2 Y-Parameters or Admittance Parameters

Here,  $v_1$  and  $v_2$  are taken as independent variables. The currents  $i_1$  and  $i_2$  are given by the equations

$$i_1 = y_{11}v_1 + y_{12}v_2 \quad (6.3)$$

$$i_2 = y_{21}v_1 + y_{22}v_2 \quad (6.4)$$

$y_{11}$ ,  $y_{12}$ ,  $y_{21}$ , and  $y_{22}$  represent short-circuit admittance parameters or simply admittance parameters or y-parameters. They are defined as follows:

$$y_{11} = \left[ \frac{i_1}{v_1} \right] \text{ with } v_2 = 0$$

= input admittance with Port 2 short-circuited

$$y_{22} = \left[ \frac{i_2}{v_2} \right] \text{ with } v_1 = 0$$

= output admittance with Port 1 short-circuited

$$y_{12} = \left[ \frac{i_1}{v_2} \right] \text{ with } v_1 = 0$$

= reverse transfer admittance with Port 1 short-circuited

$$y_{21} = \begin{bmatrix} i_2 \\ v_1 \end{bmatrix} \text{ with } v_2 = 0$$

= forward transfer admittance with Port 2 short-circuited

### 6.2.3 Hybrid Parameters or *h*-Parameters

If the input current  $i_1$  and the output voltage  $v_2$  are taken as independent variables, the input voltage  $v_1$  and output current  $i_2$  can be written as

$$v_1 = h_{11}i_1 + h_{12}v_2 \quad (6.5)$$

$$i_2 = h_{21}i_1 + h_{22}v_2 \quad (6.6)$$

The four hybrid parameters  $h_{11}$ ,  $h_{12}$ ,  $h_{21}$ , and  $h_{22}$  are defined as follows:

$$h_{11} = \begin{bmatrix} v_1 \\ i_1 \end{bmatrix} \text{ with } v_2 = 0$$

= input impedance with output port short-circuited

$$h_{22} = \begin{bmatrix} i_2 \\ v_2 \end{bmatrix} \text{ with } i_1 = 0$$

= output admittance with input port open-circuited

$$h_{12} = \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \text{ with } i_1 = 0$$

= reverse voltage gain with input port open-circuited

$$h_{21} = \begin{bmatrix} i_2 \\ i_1 \end{bmatrix} \text{ with } v_2 = 0$$

= forward current gain with output port short-circuited.

The dimensions of *h*-parameters are as follows:

$$h_{11} - \Omega$$

$$h_{22} - \text{mho}$$

$$h_{12}, h_{21} - \text{dimensionless}$$

As the dimensions are not alike, i.e., they are hybrid in nature, these parameters are called hybrid parameters.

An alternative subscript notation recommended by IEEE is commonly used:

$$i = 11 = \text{input}; o = 22 = \text{output}$$

$$f = 21 = \text{forward transfer}; r = 12 = \text{reverse transfer}$$

### 6.2.4 Notations Used in Transistor Circuits

When *h*-parameters are applied to transistors, it is a common practice to add a second subscript to designate the type of configuration considered: *e* for common emitter, *b* for common base, and *c* for common collector.

Thus, for a common emitter (CE) configuration,

$h_{ie} = h_{11e}$  = short-circuit input impedance

$h_{oe} = h_{22e}$  = open-circuit output admittance

$h_{re} = h_{12e}$  = open-circuit reverse voltage gain

$h_{fe} = h_{21e}$  = short-circuit forward current gain

### 6.3 TRANSISTOR HYBRID MODEL

Based on the definition of hybrid parameters, the mathematical model for two-port networks known as  $h$ -parameter model can be developed. Equations (6.5) and (6.6) can be written as

$$v_1 = h_i i_1 + h_r v_2 \quad (6.7)$$

$$i_2 = h_f i_1 + h_o v_2 \quad (6.8)$$

The proposed model shown in Fig. 6.2 should satisfy these two equations and it can be readily verified by writing Kirchhoff's voltage law equation in the input loop and Kirchhoff's current law equation for the output node. It is to be noted that the input circuit has a dependent voltage generator and the output circuit contains a dependent current generator.

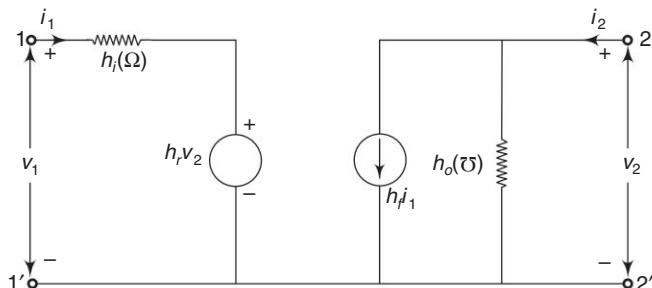


Fig. 6.2 Hybrid model for a two-port network

### 6.4 DETERMINATION OF $h$ -PARAMETERS

On extending the hybrid model for a two-port network to a transistor, it is assumed that the signal excursion about the  $Q$ -point is small so that the transistor parameters may be considered constant over the signal excursion.

Use of  $h$ -parameters to describe a transistor has the following advantages:

- (i)  $h$ -parameters are real numbers up to radio frequencies.
- (ii) They are easy to measure.
- (iii) They can be determined from the transistor static characteristics curves.
- (iv) They are convenient to use in circuit analysis and design.
- (v) They are easily convertible from one configuration to other.
- (vi) They are readily supplied by manufacturers.

In order to derive a hybrid model for a transistor, consider the CE circuit of Fig. 6.3. The variables are  $i_b$ ,  $i_c$ ,  $v_b$  ( $= v_{be}$ ) and  $v_c$  ( $= v_{ce}$ ).  $i_b$  and  $v_c$  are considered independent variables.

$$\text{Then, } v_b = f_1(i_b, v_c) \quad (6.9)$$

$$i_c = f_2(i_b, v_c) \quad (6.10)$$

Making a Taylor's series expansion around the quiescent point  $I_b$ ,  $V_c$  and neglecting higher order terms, the following two equations are obtained:

$$\Delta v_b = \left( \frac{\partial f_1}{\partial i_b} \right)_{V_c} \Delta i_b + \left( \frac{\partial f_1}{\partial v_c} \right)_{I_b} \Delta v_c \quad (6.11)$$

$$\Delta i_c = \left( \frac{\partial f_2}{\partial i_b} \right)_{V_c} \Delta i_b + \left( \frac{\partial f_2}{\partial v_c} \right)_{I_b} \Delta v_c \quad (6.12)$$

The partial derivatives are taken keeping the collector voltage or base current constant

as indicated by the subscript attached to the derivative.  $\Delta v_b$ ,  $\Delta v_c$ ,  $\Delta i_b$ , and  $\Delta i_c$  represent the small-signal (incremental) base and collector voltages and currents. They are represented by symbols  $v_b$ ,  $v_c$ ,  $i_b$ , and  $i_c$ , respectively. Hence, Eqs (6.11) and (6.12) may be written as

$$v_b = h_{ie} i_b + h_{re} v_c$$

$$i_c = h_{fe} i_b + h_{oe} v_c$$

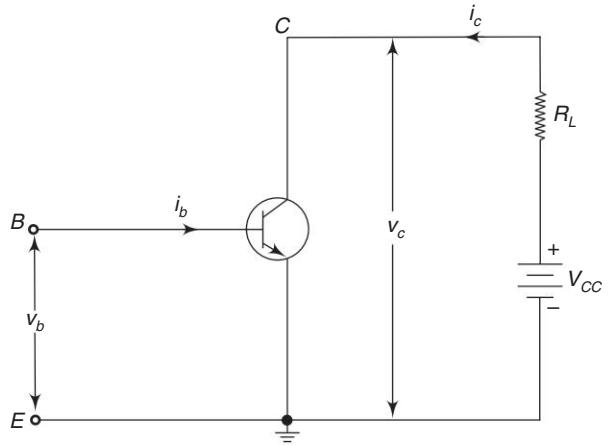
where

$$h_{ie} = \left( \frac{\partial f_1}{\partial i_b} \right)_{V_c} = \left( \frac{\partial v_b}{\partial i_b} \right)_{v_c} \approx \left( \frac{\Delta v_b}{\Delta i_b} \right)_{v_c} = \left( \frac{v_b}{i_b} \right)_{v_c} \quad (6.13)$$

$$h_{re} = \left( \frac{\partial f_1}{\partial v_c} \right)_{i_b} = \left( \frac{\partial v_b}{\partial v_c} \right)_{i_b} \approx \left( \frac{\Delta v_b}{\Delta v_c} \right)_{i_b} = \left( \frac{v_b}{v_c} \right)_{i_b} \quad (6.14)$$

$$h_{fe} = \left( \frac{\partial f_2}{\partial i_b} \right)_{V_c} = \left( \frac{\partial i_c}{\partial i_b} \right)_{v_c} \approx \left( \frac{\Delta i_c}{\Delta i_b} \right)_{v_c} = \left( \frac{i_c}{i_b} \right)_{v_c} \quad (6.15)$$

$$h_{oe} = \left( \frac{\partial f_2}{\partial v_c} \right)_{i_b} = \left( \frac{\partial i_c}{\partial v_c} \right)_{i_b} \approx \left( \frac{\Delta i_c}{\Delta v_c} \right)_{i_b} = \left( \frac{i_c}{v_c} \right)_{i_b} \quad (6.16)$$



**Fig. 6.3** CE transistor circuit

The above equations define the  $h$ -parameters of the transistor in CE configuration. The same theory can be extended to transistors in other configurations.

The hybrid models and equations given in Table 6.1 are valid for *NPN* as well as *PNP* transistors and hold good for all types of loads and methods of biasing. Table 6.2 gives the typical  $h$ -parameter values for a transistor.

**Table 6.1** Hybrid model for the transistor in three different configurations

<b>CE</b>		$v_b = h_{ie} \cdot i_b + h_{re} \cdot v_c$ $i_c = h_{fe} \cdot i_b + h_{oe} \cdot v_c$
<b>CB</b>		$v_e = h_{ib} \cdot i_e + h_{rb} \cdot v_c$ $i_c = h_{fb} \cdot i_e + h_{ob} \cdot v_c$
<b>CC</b>		$v_b = h_{ic} \cdot i_b + h_{re} \cdot v_e$ $i_e = h_{fc} \cdot i_b + h_{oc} \cdot v_e$

**Table 6.2** Typical h-parameter values for a transistor

Parameter	CE	CC	CB
$h_i$	$1100 \Omega$	$1100 \Omega$	$22 \Omega$
$h_r$	$2.5 \times 10^{-4}$	1	$3 \times 10^{-4}$
$h_f$	50	-51	-0.98
$h_o$	$25 \mu\text{A/V}$	$25 \mu\text{A/V}$	$0.49 \mu\text{A/V}$

## 6.5 CONVERSION OF $h$ -PARAMETERS

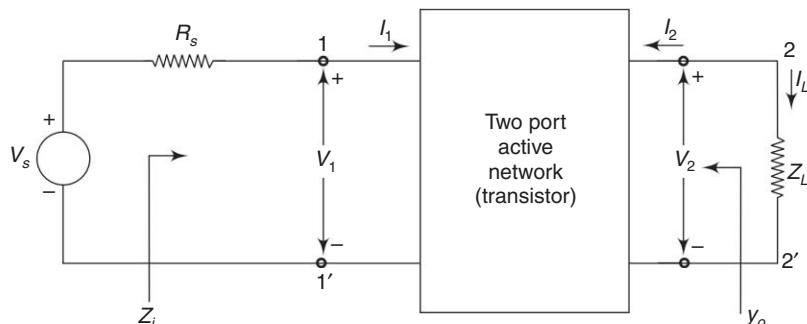
Table 6.3 gives the conversion formulae to find the  $h$ -parameters for CC and CB configurations, given the  $h$ -parameters for CE configuration.

**Table 6.3** Conversion formulae for hybrid parameters

CC	CB
$h_{ic} = h_{ie}$	$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$
$h_{rc} = 1$	$h_{rb} = \frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}$
$h_{fc} = -(1 + h_{fe})$	$h_{fb} = \frac{-h_{fe}}{1 + h_{fe}}$
$h_{oc} = h_{oe}$	$h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$

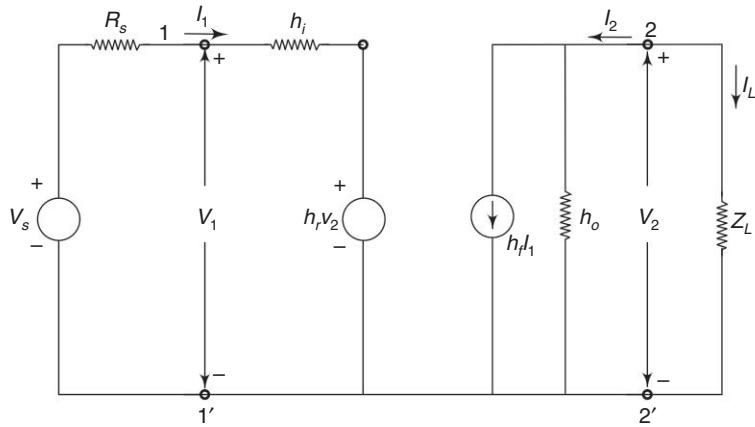
## 6.6 GENERALIZED ANALYSIS OF TRANSISTOR AMPLIFIER MODEL USING $h$ -PARAMETERS

A transistor amplifier can be constructed by connecting an external load and signal source as indicated in Fig. 6.4 and biasing the transistor properly.



**Fig. 6.4** Basic amplifier circuit

The two-port active network of Fig. 6.5 represents a transistor in any one of its configurations. The hybrid equivalent circuit is valid for any type of load whether it is pure resistance or impedance or another transistor. It is assumed that  $h$ -parameters remain constant over the operating range. Further, the input is sinusoidal and  $I_1$ ,  $V_1$ ,  $I_2$ , and  $V_2$  are phasor quantities.



**Fig. 6.5** Circuit of Fig. 6.4 with transistor replaced by its hybrid model

### 6.6.1 Current Gain or Current Amplification, $A_I$

For a transistor amplifier, the current gain  $A_I$  is defined as the ratio of output current to input current, i.e.,

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1} \quad (6.17)$$

From the circuit of Fig. 6.5,

$$I_2 = h_f I_1 + h_o V_2 \quad (6.18)$$

Substituting

$$V_2 = I_L Z_L = -I_2 Z_L,$$

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$$I_2 + I_2 Z_L h_o = h_f I_1$$

$$I_2(1 + Z_L h_o) = h_f I_1$$

$$A_I = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o Z_L} \quad (6.19)$$

Therefore,

$$A_I = \frac{-h_f}{1 + h_o Z_L}$$

### 6.6.2 Input Impedance, $Z_i$

In the circuit of Fig. 6.5,  $R_s$  is the signal source resistance. The impedance seen when looking into the amplifier terminals (1,1') is the amplifier input impedance  $Z_i$ , i.e.,

$$Z_i = \frac{V_1}{I_1} \quad (6.20)$$

From the input circuit of Fig. 6.5,  $V_1 = h_i I_1 + h_r V_2$

Hence,

$$\begin{aligned} Z_i &= \frac{h_i I_1 + h_r V_2}{I_1} \\ &= h_i + h_r \frac{V_2}{I_1} \end{aligned}$$

Substituting

$$\begin{aligned} V_2 &= -I_2 Z_L = A_I I_1 Z_L \\ Z_i &= h_i + h_r \frac{A_I I_1 Z_L}{I_1} \end{aligned}$$

resulting in

$$Z_i = h_i + h_r A_I Z_L \quad (6.21)$$

Substituting for  $A_I$ ,

$$\begin{aligned} Z_i &= h_i - \frac{h_f}{1 + h_o Z_L} h_r Z_L \\ &= h_i - \frac{h_f h_r}{Z_L \left( \frac{1}{Z_L} + h_o \right)} Z_L \end{aligned}$$

Taking the load admittance as  $Y_L = \frac{1}{Z_L}$

$$Z_i = h_i - \frac{h_f h_r}{Y_L + h_o} \quad (6.22)$$

Note that the input impedance is a function of load impedance.

### 6.6.3 Voltage Gain or Voltage Amplification Factor, $A_V$

The ratio of output voltage  $V_2$  to input voltage  $V_1$  gives the voltage gain of the transistor, i.e.,

$$A_V = \frac{V_2}{V_1} \quad (6.23)$$

Substituting

$$V_2 = -I_2 Z_L = A_I I_1 Z_L$$

$$A_V = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{Z_i} \quad (6.24)$$

### 6.6.4 Output Admittance, $Y_o$

By definition,  $Y_o$  is obtained by setting  $V_s$  to zero,  $Z_L$  to infinity and by driving the output terminals from a generator  $V_2$ . If the current drawn from  $V_2$  is  $I_2$ , then  $Y_o \equiv \frac{I_2}{V_2}$  with  $V_s = 0$  and  $R_L = \infty$ .

From the circuit of Fig. 6.5,

$$I_2 = h_f I_1 + h_o V_2$$

Dividing by  $V_2$ ,

$$\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o \quad (6.25)$$

With  $V_s = 0$ , by KVL in the input circuit,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0 \quad (6.26)$$

$$I_1 (R_s + h_i) + h_r V_2 = 0$$

Hence,  $\frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i}$

Substituting Eq. (6.26) in Eq. (6.25), we get

$$\begin{aligned} \frac{I_2}{V_2} &= h_f \left( \frac{-h_r}{R_s + h_i} \right) + h_o \\ Y_o &= h_o - \frac{h_f h_r}{h_i + R_s} \end{aligned} \quad (6.27)$$

From Eq. (6.27), the output admittance is a function of the source resistance. If the source impedance is resistive, then  $Y_o$  is real.

### 6.6.5 Voltage Amplification ( $A_{Vs}$ ) taking into account the Source Resistance ( $R_s$ )

This overall voltage gain  $A_{Vs}$  is given by

$$A_{Vs} = \frac{V_2}{V_s} = \frac{V_2 V_1}{V_1 V_s} = A_V \frac{V_1}{V_s} \quad (6.28)$$

From the equivalent input circuit using Thevenin's equivalent for the source shown in Fig. 6.6,

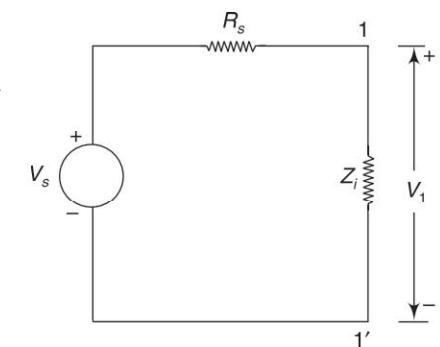
$$V_1 = \frac{V_s Z_i}{Z_i + R_s} \quad (6.29)$$

$$\frac{V_1}{V_s} = \frac{Z_i}{Z_i + R_s}$$

Then,  $A_{Vs} = \frac{A_V Z_i}{Z_i + R_s} \quad (6.30)$

Substituting  $A_V = \frac{A_I Z_L}{Z_i}$

$$A_{Vs} = \frac{A_I Z_L}{Z_i + R_s} \quad (6.31)$$

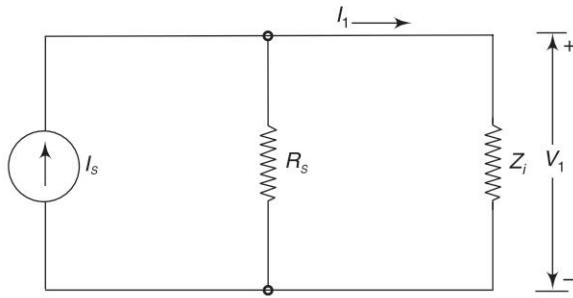


**Fig. 6.6** Equivalent input circuit

Note that if  $R_s = 0$ , then  $A_{Vs} = \frac{A_I Z_L}{Z_i} = A_V$ . Hence,  $A_V$  is the voltage gain with an ideal voltage source (with  $R_s = 0$ ). In practice,  $A_{Vs}$  is more meaningful than  $A_V$  because the source resistance has an appreciable effect on the overall amplification.

### 6.6.6 Current Amplification ( $A_{Is}$ ) taking into account the Source Resistance ( $R_s$ )

The modified input circuit using Norton's equivalent circuit for the source for the calculation of  $A_{Is}$  is shown in Fig. 6.7.



**Fig. 6.7** Modified input equivalent circuit

$$\text{Overall current gain, } A_{Is} = \frac{-I_2}{I_s} = \frac{-I_2}{I_1} \cdot \frac{I_1}{I_s} = A_I \frac{I_1}{I_s} \quad (6.32)$$

$$\text{From Fig. 6.7, } I_1 = I_s \frac{R_s}{R_s + Z_i} \quad (6.33)$$

$$\frac{I_1}{I_s} = \frac{R_s}{R_s + Z_i}$$

$$\text{and hence, } A_{Is} = A_I \frac{R_s}{R_s + Z_i} \quad (6.34)$$

If  $R_s = \infty$ , then  $A_{Is} = A_I$ . Hence,  $A_I$  is the current gain with an ideal current source (one with infinite source resistance).

From Eq. (6.31),

$$A_{Vs} = \frac{A_I Z_L}{Z_i + R_s} \frac{R_s}{R_s}$$

$$\text{Then, } A_{Vs} = \frac{A_I Z_L}{R_s} \quad (6.35)$$

### 6.6.7 Operating Power Gain, $A_P$

From Fig. 6.5, average power delivered to the load is  $P_2 = |V_2| |I_L| \cos \theta$ , where  $\theta$  is the phase angle between  $V_2$  and  $I_L$ . Assume that  $Z_L$  is resistive, i.e.,  $Z_L = R_L$ . Since  $h$ -parameters are real at low frequencies, the power

delivered to the load is  $P_2 = V_2 I_L = -V_2 I_2$ . Since the input power  $P_1 = V_1 I_1$ , the operating power gain  $A_P$  of the transistor is defined as

$$\begin{aligned} A_P &= \frac{P_2}{P_1} = \frac{-V_2 I_2}{V_1 I_1} = A_V A_I = A_I A_I \frac{R_L}{R_i} \\ A_P &= A_I^2 \left( \frac{R_L}{R_i} \right) \end{aligned} \quad (6.36)$$

The important relations derived above are summarized in Table 6.4.

**Table 6.4** Small signal analysis of a transistor amplifier

$A_I = \frac{-h_f}{1 + h_o Z_L}$	$A_V = \frac{A_I Z_L}{Z_i}$
$Z_i = h_i + h_r A_I Z_L = h_i - \frac{h_f h_r}{Y_L + h_o}$	$A_{Vs} = \frac{A_V Z_i}{Z_i + R_s} = \frac{A_I Z_L}{Z_i + R_s} = A_{Is} \frac{Z_L}{R_s}$
$Y_o = h_o - \frac{h_f h_r}{h_i + R_s} = \frac{1}{Z_o}$	$A_{Is} = \frac{A_I R_s}{Z_i + R_s} = A_{Vs} \frac{R_s}{Z_L}$

### EXAMPLE 6.1

A CE amplifier has the  $h$ -parameters given by  $h_{ie} = 1000 \Omega$ ,  $h_{re} = 2 \times 10^{-4}$ ,  $h_{fe} = 50$ , and  $h_{oe} = 25 \mu \text{ mho}$ . If both the load and source resistances are  $1 \text{ k}\Omega$ , determine the (a) current gain, and (b) voltage gain.

**Solution** Given  $R_s = 1 \text{ k}\Omega$  and  $R_L = 1 \text{ k}\Omega$

$$(a) \text{ Current gain, } A_i = \frac{h_{fe}}{1 + h_{oe} \times R_L} = \frac{50}{1 + 25 \times 10^{-6} \times 1 \times 10^3} = 48.78$$

$$(b) \text{ Voltage gain, } A_V = \frac{-h_{fe}}{\left( h_{oe} + \frac{1}{R_L} \right) Z_{in}}$$

Here,

$$\begin{aligned} Z_{in} &= h_{ie} - \frac{h_{re} h_{fe}}{h_{oe} + \frac{1}{R_L}} \\ &= 1000 - \frac{2 \times 10^{-4} \times 50}{25 \times 10^{-6} + 1 \times 10^{-3}} = 990.24 \Omega \end{aligned}$$

Therefore,

$$A_V = \frac{-50}{(25 \times 10^{-6} + 1 \times 10^{-3}) \times 990.24} = -49.26$$

The output voltage is  $180^\circ$  out of phase to the input signal with a gain of 49.26.

**EXAMPLE 6.2**

A transistor amplifier circuit  $R_1 = 100\text{k}\Omega$ ,  $R_2 = 50\text{k}\Omega$ ,  $R_c = 10\text{k}\Omega$  and  $R_L = 40\text{k}\Omega$  has the  $h$ -parameters as follows:  $h_{ie} = 1100 \Omega$ ,  $h_{fe} = 100$ ,  $h_{re} = 10 \times 10^{-4}$ ,  $h_{oe} = 4 \times 10^{-4}$  mho. Determine the (a) ac input impedance of the amplifier, and (b) the voltage gain.

**Solution** At load resistance of the amplifier,

$$R'_L = R_C \parallel R_L \frac{10 \times 10^3 \times 40 \times 10^3}{10 \times 10^3 + 40 \times 10^3} = 8 \text{k}\Omega = 8000 \Omega$$

$$\begin{aligned} \text{(a) Input impedance, } Z_{\text{in}} &= h_{ie} - \frac{h_{re}h_{fe}}{h_{oe} + \frac{1}{R'_L}} \\ &= 1100 - \frac{4 \times 10^{-4} \times 100}{4 \times 10^{-4} + \frac{1}{8000}} = 1024 \Omega \end{aligned}$$

The ac input resistance of the entire stage  $R_{\text{ac}}$  is

$$\begin{aligned} R_{\text{ac}} &= Z_{\text{in}} \parallel R_1 \parallel R_2 \\ &= 1024 \parallel 100 \times 1000 \parallel 50 \times 1000 = 993.4 \Omega \end{aligned}$$

$$\text{(b) Voltage gain, } A_V = \frac{-h_{fe}}{\left( h_{oe} + \frac{1}{R'_L} \right) Z_{\text{in}}} = \frac{-100}{\left( 4 \times 10^{-4} + \frac{1}{8000} \right) 1024} = -186.34$$

The output is  $180^\circ$  out of phase to the input with a gain of 186.34.

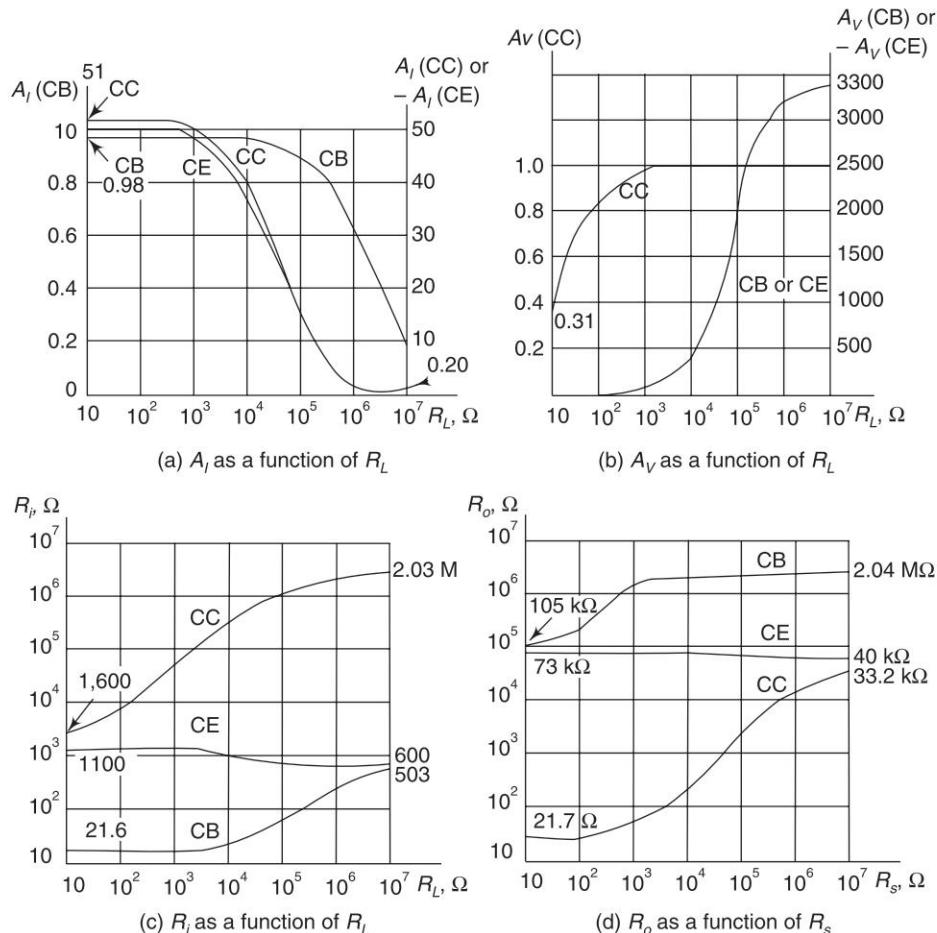
## 6.7 COMPARISON OF TRANSISTOR AMPLIFIERS

The characteristics of three configurations are summarized in Table 6.5. Here, the quantities  $A_i$ ,  $A_V$ ,  $R_i$ ,  $R_o$  and  $A_P$ , are calculated for a typical transistor whose  $h$ -parameters are given in Table 6.2. The values of  $R_L$  and  $R_s$  are taken as  $3 \text{k}\Omega$ .

**Table 6.5** Performance schedule of three-transistor configurations

Quantity	CB	CC	CE
$A_i$	0.98	47.5	- 46.5
$A_V$	131	0.989	- 131
$A_P$	128.38	46.98	6091.5
$R_i$	$22.6 \Omega$	$144 \text{k}\Omega$	$1065 \Omega$
$R_o$	$1.72 \text{M}\Omega$	$80.5 \Omega$	$45.5 \text{k}\Omega$

The values of current gain, voltage gain, input impedance, and output impedance calculated as a function of load and source impedances can be shown graphically as in Fig. 6.8.



**Fig. 6.8** Comparison of transistor amplifier configurations: (a) Current gain as a function on  $R_L$  (b) Voltage gain as a function of  $R_L$  (c) Input impedance as a function of  $R_L$  (d) Output impedance as a function of  $R_s$

From Table 6.5 and Fig. 6.8, the performance of the CB, CC, and CE amplifiers can be summarized as follows:

#### Characteristics of Common-Base Amplifiers

- (i) Current gain is less than unity and its magnitude decreases with the increase of load resistance  $R_L$ ,
- (ii) Voltage gain  $A_V$  is high for normal values of  $R_L$ ,
- (iii) The input resistance  $R_i$  is the lowest of all the three configurations, and
- (iv) The output resistance  $R_o$  is the highest of all the three configurations.

- **Applications** The CB amplifier is not commonly used for amplification purpose. It is used for

- (i) matching a very low impedance source
- (ii) as a non-inverting amplifier with voltage gain exceeding unity
- (iii) for driving a high impedance load
- (iv) as a constant current source

### **Characteristics of Common-Collector Amplifiers**

- (i) For low value of  $R_L$  ( $< 10 \text{ k}\Omega$ ), the current gain  $A_I$  is high and almost equal to that of a CE amplifier.
- (ii) The voltage gain  $A_V$  is less than unity.
- (iii) The input resistance is the highest of all the three configurations.
- (iv) The output resistance is the lowest of all the three configurations.

- **Applications** The CC amplifier is widely used as a buffer stage between a high-impedance source and a low-impedance load. The CC amplifier is called the *emitter follower*.

### **Characteristics of Common-Emitter Amplifiers**

- (i) The current gain  $A_I$  is high for  $R_L < 10 \text{ k}\Omega$ .
- (ii) The voltage gain is high for normal values of load resistance  $R_L$ .
- (iii) The input resistance  $R_i$  is medium.
- (iv) The output resistance  $R_o$  is moderately high.

- **Applications** Of the three configurations, the CE amplifier alone is capable of providing both voltage gain and current gain. Further, the input resistance  $R_i$  and the output resistance  $R_o$  are moderately high. Hence, the CE amplifier is widely used for amplification purpose.

---

## **6.8 APPROXIMATE HYBRID MODEL**

As the  $h$ -parameters themselves vary widely for the same type of transistor, it is justified to make approximations and simplify the expressions for  $A_I$ ,  $A_V$ ,  $A_P$ ,  $R_i$ , and  $R_o$ . In addition, a better understanding of the behaviour of the transistor circuit can be obtained by using the simplified hybrid model. Since the CE configuration is more useful and general, it is taken for consideration.

The  $h$ -parameter equivalent circuit of the transistor in the CE configuration is shown in Fig. 6.9. Here,  $\frac{1}{h_{oe}}$  is parallel with  $R_L$ . The parallel combination of two unequal impedances, i.e.,  $\frac{1}{h_{oe}}$  and  $R_L$  is approximately equal to the lower value, i.e.,  $R_L$ . Hence, if  $\frac{1}{h_{oe}} \gg R_L$ , then the term  $h_{oe}$  may be neglected provided that  $h_{oe}R_L \ll 1$ . Further, if  $h_{oe}$  is omitted, the collector current  $I_C$  is given by  $I_C = h_{fe}I_b$ .

Under this condition, the magnitude of voltage of the generator in the emitter circuit is

$$h_{re}|V_C| = h_{re}I_C R_L = h_{re}h_{fe}I_b R_L$$

Since  $h_{re}h_{fe} \approx 0.01$ , this voltage may be neglected in comparison with the voltage drop across  $h_{ie} = h_{ie}I_b$  provided that  $R_L$  is not too large.

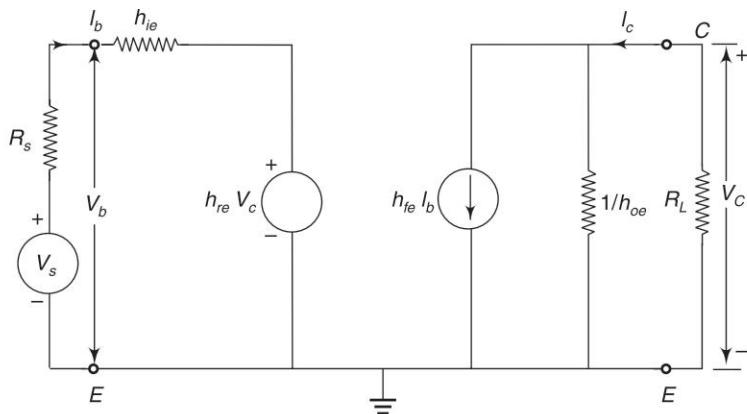


Fig. 6.9 Exact CE hybrid model

To conclude, if the load resistance  $R_L$  is small, it is possible to neglect the parameter  $h_{re}$  and  $h_{oe}$  and obtain the approximate equivalent circuit as shown in Fig. 6.10. It can be shown that if  $h_{oe} R_L \leq 0.1$ , the error in calculating  $A_I$ ,  $A_V$ ,  $R_i$ , and  $R_o$  for CE configuration is less than 10%.

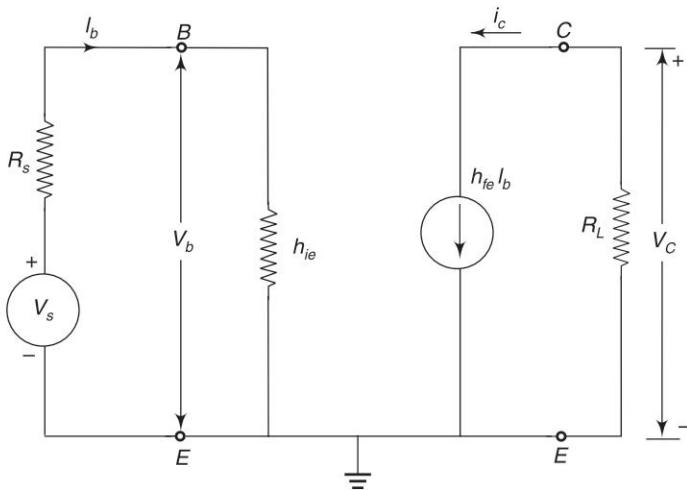
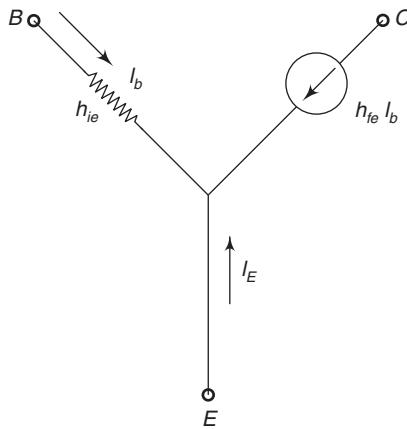


Fig. 6.10 Approximate CE hybrid model

### Generalized Approximate Model

Figure 6.11 shows the simplified hybrid circuit that can be used for any configuration by simply grounding the appropriate terminal. The signal is connected between input and ground and the load is connected between output and ground. The errors introduced in calculating the various parameters using the approximate hybrid model are to be found out now. This is done for the CE configuration.



**Fig. 6.11** Approximate hybrid model valid for all configurations

## 6.9 ANALYSIS OF CE USING APPROXIMATE ANALYSIS

**Current Gain** From Eq. (6.19), the current gain for CE configuration is

$$A_I = \frac{-h_{fe}}{1 + h_{oe} R_L}$$

If  $h_{oe} R_L < 0.1$ ,

$$A_I \approx -h_{fe} \quad (6.37)$$

This new  $A_I$  overestimates the magnitude of current gain by less than 10% provided  $h_{oe} R_L < 0.1$ .

**Input Impedance** From Eq. (6.21), the input impedance

$$R_i = h_{ie} + h_{re} A_I R_L$$

It may be put in the form

$$R_i = h_{ie} \left( 1 - \frac{h_{re} h_{fe} |A_I| h_{oe} R_L}{h_{ie} h_{oe} h_{fe}} \right)$$

Using the typical values for the  $h$ -parameters,

$$\frac{h_r h_{fe}}{h_{ie} h_{oe}} \approx 0.5$$

Further,  $|A_I| = \frac{h_{fe}}{1 + h_{oe} R_L} \approx h_{fe}$

Hence, the equation approximates to

$$R_i \approx h_{ie} \left( 1 - \frac{0.5 h_{fe} h_{oe} R_L}{h_{fe}} \right)$$

If  $h_{oe}R_L < 0.1$ ,

$$R_i \approx h_{ie} = \frac{V_b}{I_b} \quad (6.38)$$

This overestimates the input resistance by less than 5%.

**Voltage Gain** From Eq. (6.24),

$$\text{voltage gain, } A_V = A_I \frac{R_L}{R_i} = -\frac{h_{fe}R_L}{h_{ie}} \quad (6.39)$$

By taking the logarithm of this equation and then the differential,

$$\frac{dA_V}{A_V} = \frac{dA_I}{A_I} - \frac{dR_i}{R_i}$$

$$\text{with } h_{oe}R_L < 0.1, \quad \frac{dA_I}{A_I} = +0.1 \quad \text{and} \quad \frac{dR_i}{R_i} = +0.05$$

$$\text{Therefore, } \frac{dA_V}{A_V} = 0.1 - 0.05 = 0.05$$

$$\frac{dA_V}{A_V} \% = 5\%$$

Hence, the maximum error in voltage gain is 5% and the magnitude of  $A_V$  is overestimated by this amount.

**Output Impedance** It is the ratio of  $V_C$  to  $I_C$  with  $V_s = 0$  and  $R_L$  excluded.

The simplified circuit has infinite output impedance because with  $V_s = 0$  and external voltage source applied at the output, it is found that  $I_b = 0$  and hence,  $I_C = 0$ .

However, the actual value of output impedance depends on the source resistance  $R_s$  and lies between 40 kΩ and 80 kΩ. With the load resistance  $R_L$  included, the output resistance  $R_o$  calculated using the approximate model increases, but not more than 10%.

### EXAMPLE 6.3

A CE amplifier is driven by a voltage source of internal resistance  $R_s = 800 \Omega$ , and the load impedance is a resistance  $R_L = 1000 \Omega$ . The  $h$ -parameters are  $h_{ie} = 1 \text{ k}\Omega$ ,  $h_{re} = 2 \times 10^{-4}$ ,  $h_{fe} = 50$ , and  $h_{oe} = 25 \mu\text{A/V}$ . Compute the current gain  $A_I$ , input resistance  $R_i$ , voltage gain  $A_V$  and, output resistance  $R_o$  using exact analysis and using approximate analysis.

#### Solution

*Exact analysis*

$$\begin{aligned} \text{Current gain, } A_I &= \frac{-h_{fe}}{1 + h_{oe}R_L} \\ &= \frac{-50}{1 + 25 \times 10^{-6} \times 10^3} = -48.78 \end{aligned}$$

Input resistance,

$$R_i = h_{ie} - \frac{h_{fe} h_{re}}{h_{oe} + \frac{1}{R_L}}$$

$$= 1000 - \frac{50 \times 2 \times 10^{-4}}{25 \times 10^{-6} + \frac{1}{1000}} = 990.24 \Omega$$

Voltage gain,

$$A_V = A_I \frac{R_L}{R_i} = (-48.78) \times \frac{1000}{990.24} = -49.26$$

Output resistance,  $R_o$

$$Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s} = 25 \times 10^{-6} - \frac{50 \times 2 \times 10^{-4}}{1000 + 800} = 1.94 \times 10^{-5} \text{ mho}$$

$$R_o = \frac{1}{Y_o} = 51.42 \text{ k}\Omega$$

Approximate analysis

$$A_I = -h_{fe} = -50$$

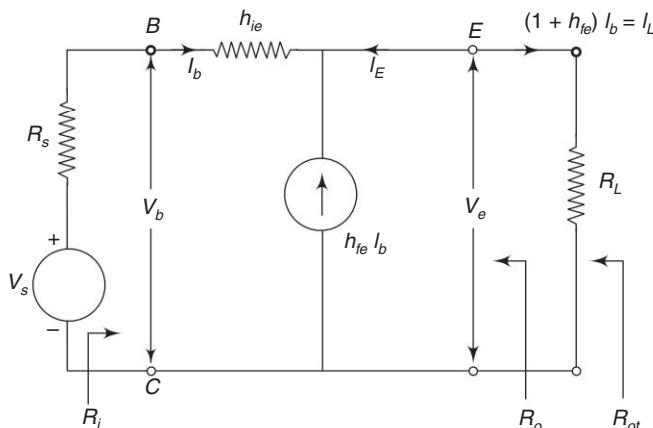
$$R_i = h_{ie} = 1 \text{ k}\Omega$$

$$A_V = -\frac{h_{fe} R_L}{h_{ie}} = -\frac{50 \times 1000}{1000} = -50$$

$$R_o = \infty$$

## 6.10 ANALYSIS OF CC USING APPROXIMATE ANALYSIS

Figure 6.12 shows the equivalent circuit of the CC amplifier using the approximate model, with the collector grounded, input signal applied between base and ground, and load connected between emitter and ground.



**Fig. 6.12** Simplified hybrid model for the CC circuit

### Current Gain

Current gain,  $A_I = \frac{I_L}{I_b} = 1 + h_{fe}$  (6.40)

**Input Resistance** From the circuit of Fig. 6.12,

$$V_b = I_b h_{ie} + (1 + h_{fe}) I_b R_L$$

Input resistance,  $R_i = \frac{V_b}{I_b} = h_{ie} + (1 + h_{fe}) R_L$  (6.41)

### Voltage Gain

$$\begin{aligned} A_V &= \frac{V_e}{V_b} = \frac{(1 + h_{fe}) I_b R_L}{[h_{ie} I_b + (1 + h_{fe}) I_b R_L]} \\ &= \frac{(1 + h_{fe}) R_L}{[h_{ie} + (1 + h_{fe}) R_L]} \end{aligned} \quad (6.42)$$

$$\begin{aligned} &= \frac{h_{ie} + (1 + h_{fe}) R_L - h_{ie}}{[h_{ie} + (1 + h_{fe}) R_L]} \\ &= 1 - \frac{h_{ie}}{h_{ie} + (1 + h_{fe}) R_L} \end{aligned} \quad (6.43)$$

Therefore,  $A_V = 1 - \frac{h_{ie}}{R_i}$  (6.44)

### Output Impedance

$$\text{Output admittance } (Y_o) = \frac{\text{Short-circuit current in output terminals}}{\text{Open-circuit voltage between output terminals}}$$

$$\text{Short-circuit current in output terminals} = (1 + h_{fe}) I_b = \frac{(1 + h_{fe}) V_s}{h_{ie} + R_s}$$

$$\text{Open-circuit voltage between output terminals} = V_s$$

$$Y_o = \frac{1 + h_{fe}}{h_{ie} + R_s} \quad (6.45)$$

and  $Z_o = \frac{1}{Y_o} = \frac{h_{ie} + R_s}{1 + h_{fe}}$  (6.46)

Output impedance including  $R_L$ , i.e.,  $R'_o = R_o \parallel R_L$ .

### EXAMPLE 6.4

A voltage source of internal resistance  $R_s = 900 \Omega$  drives a CC amplifier using load resistance  $R_L = 2000 \Omega$ . The CE  $h$ -parameters are  $h_{ie} = 1200 \Omega$ ,  $h_{re} = 2 \times 10^{-4}$ ,  $h_{fe} = 60$ , and  $h_{oe} = 25 \mu\text{A/V}$ . Compute the current gain

$A_I$ , the input impedance  $R_i$ , voltage gain  $A_V$ , and output resistance  $R_o$  using approximate analysis and exact analysis.

**Solution**

Conversion formulae:  $h_{ic} = h_{ie} = 1200 \Omega$ ,  $h_{fc} = -(1 + h_{fe}) = -(1 + 60) = -61$   
 $h_{rc} = 1$ ,  $h_{oc} = h_{oe} = 25 \mu\text{A/V}$

*Exact analysis*

Current gain,

$$A_I = \frac{-h_{fc}}{1 + h_{oc} R_L}$$

$$= \left[ \frac{-(-61)}{1 + 25 \times 10^{-6} \times 2 \times 10^3} \right] = 58.095$$

Input impedance,

$$R_i = h_{ic} + h_{rc} A_I R_L$$

$$= 1200 + (1)(58.095)(2000) = 117.39 \text{ k}\Omega$$

Voltage gain,

$$A_V = \frac{A_I R_L}{R_i} = \frac{(58.095)(2 \times 10^3)}{117.39 \times 10^3} = 0.9897$$

Output resistance,  $R_o$ :

$$Y_o = h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic} + R_s}$$

$$= 25 \times 10^{-6} - \frac{(-61)(1)}{(1200) + (900)} = 0.029 \text{ mho}$$

$$R_o = \frac{1}{Y_o} = \frac{1}{0.029} = 34.48 \Omega$$

*Approximate analysis*

Current gain,

$$A_I = 1 + h_{fe} = 1 + 60 = 61$$

Input impedance,

$$R_i = h_{ie} + (1 + h_{fe}) R_L = 1200 + (61)(2000) = 123.2 \text{ k}\Omega$$

Voltage gain,

$$A_V = 1 - \frac{h_{ie}}{R_i} = 1 - \frac{1200}{123.2 \times 10^3} = 0.9903$$

Output resistance,  $R_o$ :

$$Y_o = \frac{1}{R_o} = \frac{1 + h_{fe}}{h_{ie} + R_s} = \frac{1 + 60}{1200 + 900} = 0.029 \text{ mho}$$

$$R_o = \frac{1}{Y_o} = \frac{1}{0.029} = 34.48 \Omega$$

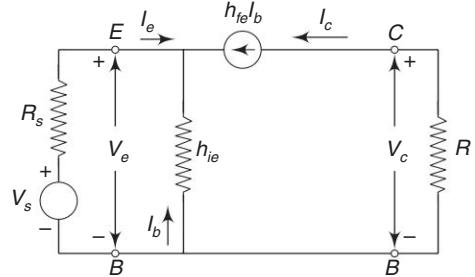
## 6.11 ANALYSIS OF CB USING APPROXIMATE ANALYSIS

Figure 6.13 shows the equivalent circuit of the CB amplifier using the approximate model, with the base grounded, input signal applied between emitter and base, and load connected between collector and base.

### Current Gain

$$\begin{aligned} A_I &= \frac{-I_c}{I_e} = \frac{-h_{fe} I_b}{I_e} \\ &= \frac{-h_{fe} I_b}{-(h_{fe} I_b + I_b)} = \frac{h_{fe}}{1 + h_{fe}} = -h_{fb} \quad (\text{from Table 6.3}) \end{aligned}$$

Hence, current gain,  $A_I = \frac{h_{fe}}{1 + h_{fe}} = -h_{fb}$  (6.47)



**Fig. 6.13** Simplified hybrid model for the CB circuit

### Input Resistance

$$\begin{aligned} R_i &= \frac{V_e}{I_e} \\ &= \frac{-I_b h_{ie}}{-(1 + h_{fe}) I_b} = \frac{h_{ie}}{1 + h_{fe}} \\ &= h_{ib} \quad (6.48) \end{aligned}$$

### Voltage Gain

$$\begin{aligned} A_V &= \frac{V_c}{V_e} \\ &= \frac{-h_{fe} I_b R_L}{-I_b h_{ie}} \\ &= \frac{h_{fe} R_L}{h_{ie}} \quad (6.49) \end{aligned}$$

$A_I$ ,  $A_V$ , and  $R_i$  do not differ from exact values by more than 10%.

### Output Impedance

$$R_o = \frac{V_c}{I_c} \text{ with } V_s = 0, R_L = \infty$$

With  $V_s = 0$ ,  $I_e = 0$  and  $I_b = 0$

Hence,  $I_c = 0$ .

Therefore,  $R_o = \infty$  using the approximate model.

### EXAMPLE 6.5

For a CB transistor amplifier driven by a voltage source of internal resistance  $R_s = 1200 \Omega$ , the load impedance is a resistor  $R_L = 1000 \Omega$ . The  $h$ -parameters are  $h_{ib} = 22 \Omega$ ,  $h_{rb} = 3 \times 10^{-4}$ ,  $h_{fb} = -0.98$  and  $h_{ob} = 0.5 \mu\text{A/V}$ . Compute the current gain  $A_I$ , the input impedance  $R_i$ , voltage gain  $A_V$ , overall voltage gain  $A_{Vs}$ , overall current gain  $A_{Is}$ , output impedance  $Z_o$ , and power gain  $A_P$  using exact analysis and approximate analysis.

**Solution***Exact analysis*

Current gain,  $A_I = \frac{-h_{fb}}{1 + h_{ob} R_L} = \frac{-(-0.98)}{1 + 0.5 \times 10^{-6} \times 1000} = 0.98$

Input impedance,  $R_i = h_{ib} + h_{rb} A_I R_L$   
 $= 22 + (3 \times 10^{-4}) \times 0.98 \times 1000 = 22.3 \Omega$

Voltage gain,  $A_V = \frac{A_I R_L}{R_i} = \frac{0.98 \times 1000}{22.3} = 43.946$

Overall voltage gain,  $A_{Vs} = \frac{A_V R_i}{R_i + R_s} = \frac{43.946 \times 22.3}{22.3 + 1200} = 0.802$

Overall current gain,  $A_{Is} = \frac{A_I R_s}{R_i + R_s} = \frac{0.98 \times 1200}{22.3 + 1200} = 0.962$

Output admittance,  $Y_o = h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R_s} = 0.5 \times 10^{-6} - \frac{(0.98)(3 \times 10^{-4})}{22 + 1200}$   
 $= 0.7405 \times 10^{-6} \text{ mho}$

$$R_o = \frac{1}{Y_o} = 1.35027 \text{ M}\Omega$$

Power gain,  $A_P = A_V A_I = 0.98 \times 43.946 = 43.06$

*Approximate analysis*

Current gain,  $A_I = -h_{fb} = 0.98$

Input impedance,  $R_i = h_{ib} = 22 \Omega$

Voltage gain,  $A_V = \frac{h_{fe} R_L}{h_{ie}}$

From Table 6.3,  $h_{fb} = \frac{-h_{fe}}{1 + h_{fe}}$

Rearranging this equation,  $h_{fe} = \frac{-h_{fb}}{1 + h_{fb}}$

From the given data,  $h_{fe} = \frac{-(-0.98)}{1 - 0.98} = 49$

From Table 6.3,  $h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$

$$h_{ie} = h_{ib}(1 + h_{fe}) = 22(1 + 49) = 1100 \Omega$$

$$A_V = \frac{49 \times 1000}{1100} = 44.54$$

Output impedance,

$$R_o = \infty$$

Overall voltage gain,

$$A_{Vs} = \frac{A_V R_i}{R_i + R_s} = \frac{44.54 \times 22}{22 + 1200} = 0.802$$

Overall current gain,

$$A_{Is} = \frac{A_I R_s}{R_i + R_s} = \frac{0.98 \times 1200}{22 + 1200} = 0.962$$

Power gain,

$$A_P = A_V A_I = 44.54 \times 0.98 = 43.65$$

### EXAMPLE 6.6

Calculate the values of input resistance, output resistance, current gain, and voltage gain for the common base amplifier circuit shown in Fig. 6.14. The transistor parameters are  $h_{ib} = 24 \Omega$ ,  $h_{fb} = 0.98$ ,  $h_{ob} = 0.49 \mu\text{A/V}$ ,  $h_{rb} = 2.9 \times 10^{-4}$ .

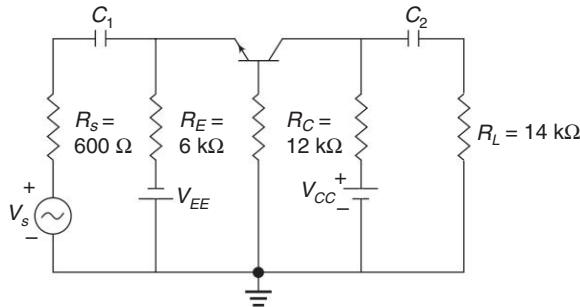


Fig. 6.14

#### Solution

Current gain

$$A_I = \frac{-h_{fb}}{1 + h_{ob} R'_L}$$

where

$$R'_L = R_C \parallel R_L = 12 \text{ k}\Omega \parallel 14 \text{ k}\Omega = 6.46 \text{ k}\Omega$$

Therefore,

$$A_I = \frac{-(-0.98)}{1 + (0.49 \times 10^{-6})(6.46 \times 10^3)} = 0.977$$

Input impedance  $R_i$ :

$$R_i = h_{ib} + h_{rb} A_I R'_L = 24 + 2.9 \times 10^{-4} \times 0.977 \times 6.46 \times 10^3 = 25.83 \Omega$$

Voltage gain  $A_V$ :

$$A_V = \frac{A_I R'_L}{R_i} = \frac{(0.977) \times (6.46 \times 10^3)}{25.83} = 244.34$$

Output resistance  $R_o$ :

The output admittance is

$$\begin{aligned} Y_o &= \frac{1}{R_o} = h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R'_s} \quad \text{where } R'_s = R_s \parallel R_E \\ &= 0.49 \times 10^{-6} - \frac{(-0.98)(2.9 \times 10^{-4})}{24 + 600 \parallel 6000} = 0.989 \times 10^{-6} \text{ mho} \end{aligned}$$

$$R_o = \frac{1}{Y_o} = 1.011 \text{ M}\Omega$$

$$R'_s = R_o \parallel R'_L = 1.011 \times 10^{-6} \parallel 6.46 \times 10^3 = 6.42 \text{ k}\Omega$$

## 6.12 BJT AMPLIFIERS

---

A circuit that increases the amplitude of the given input signal is an amplifier. A small ac signal fed to the amplifier is obtained as a larger ac signal of the same frequency at the output. Amplifiers constitute an essential part of radio, television, and other communication circuits. In discrete circuits, Bipolar junction transistors and field effect transistors are commonly used as amplifying elements. Depending on the nature and level of amplification and the impedance matching requirements, different types of amplifiers can be considered and they are discussed in this chapter.

### Classification of Amplifiers

Amplifiers can be classified as follows:

1. Based on the transistor configuration
  - (a) Common-Emitter (CE) amplifier
  - (b) Common-Collector (CC) amplifier
  - (c) Common-Base (CB) amplifier
2. Based on the active device
  - (a) BJT amplifier
  - (b) FET amplifier
3. Based on the *Q*-point (operating condition)
  - (a) Class A amplifier
  - (b) Class B amplifier
  - (c) Class AB amplifier
  - (d) Class C amplifier
4. Based on the number of stages
  - (a) Single-stage amplifier
  - (b) Multistage amplifier
5. Based on the output
  - (a) Voltage amplifier
  - (b) Power amplifier
6. Based on the frequency response
  - (a) Audio Frequency (AF) amplifier
  - (b) Intermediate Frequency (IF) amplifier
  - (c) Radio Frequency (RF) amplifier
7. Based on the bandwidth
  - (a) Narrow-band amplifier (normally RF amplifier)
  - (b) Wide-band amplifier (normally video amplifier)

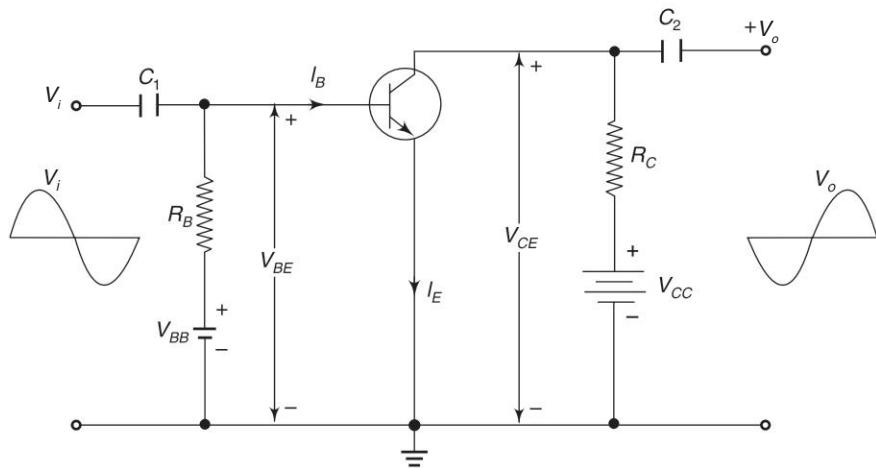
## 6.13 SINGLE-STAGE AMPLIFIERS

---

Single-stage amplifiers have only one amplifying device, say, BJT in CE, CC, or CB configurations or FET in CS, CD, or CG configurations.

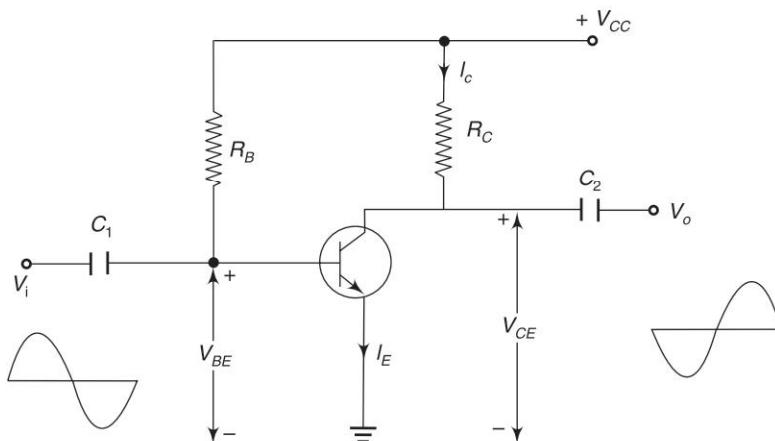
### 6.13.1 Common-Emitter (CE) Amplifier

Figure 6.15 shows the circuit of a single-stage CE amplifier using an *NPN* transistor. The emitter-base junction is forward biased by the power supply  $V_{BB}$ , and the collector-base junction is reverse biased by the power supply  $V_{CC}$ , so that the transistor remains in the active region throughout its operation. The quiescent ( $Q$ ) point is determined by  $V_{CC}$ ,  $R_B$ , and  $R_C$ . The input signal is applied to the base-emitter circuit and the amplified output signal is taken from the CE circuit.  $C_1$  and  $C_2$  are coupling capacitors to provide dc isolation at the input and output of the amplifier.



**Fig. 6.15** Common-emitter amplifier

Instead of using two power supplies, the same bias conditions can be set up in the CE amplifier circuit with a single power supply as shown in Fig. 6.16.



**Fig. 6.16** CE Amplifier with a single power supply

Referring to Fig. 6.16, when no ac signal input is given, i.e., under dc conditions,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \approx \frac{V_{CC}}{R_B} \quad (6.50)$$

$$I_C = \beta I_B \quad (6.51)$$

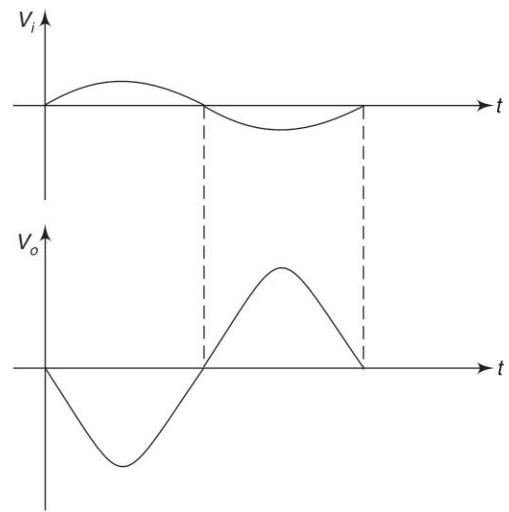
$$V_{CE} = V_{CC} - I_C R_C \quad (6.52)$$

When a sinusoidal ac signal is applied at the input terminals of the circuit, during the positive half cycle, the forward bias of the base-emitter junction  $V_{BE}$  is increased, resulting in an increase in  $I_B$ . The collector  $I_C$  is increased by  $\beta$  times the increase in  $I_B$ . From Eq. (6.52),  $V_{CE}$  is correspondingly decreased, i.e., the output voltage gets decreased as shown in Fig. 6.17.

Thus, in a CE amplifier, a positive-going input signal is converted into a negative-going output signal, i.e., a  $180^\circ$  phase shift is introduced between the output and input signal and further, the output signal is an amplified version of the input signal.

### Characteristics of a CE Amplifier

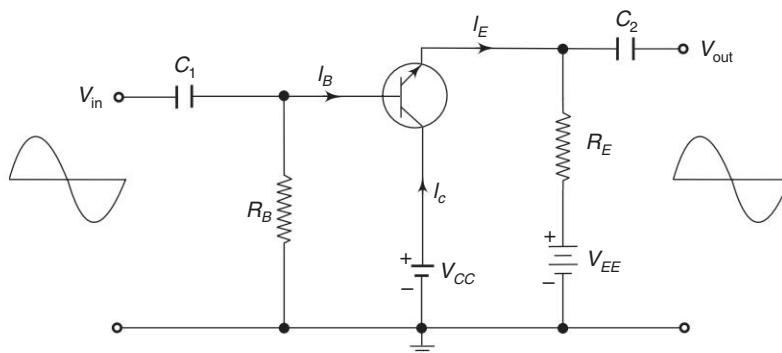
- (i) Large current gain ( $A_I$ )
- (ii) Large voltage gain ( $A_V$ )
- (iii) Large power gain ( $A_P = A_I \cdot A_V$ )
- (iv) Voltage phase shift of  $180^\circ$
- (v) Moderate input impedance
- (vi) Moderate output impedance



**Fig. 6.17** Input and output voltages of a CE amplifier

### 6.13.2 Common-Collector (CC) Amplifier

Figure 6.18 shows the circuit of a single-stage CC amplifier using an NPN transistor. The emitter-base junction is forward biased by the power supply  $V_{EE}$ , and the collector-base junction is reverse biased by  $V_{CC}$ , so that the transistor remains in the active region throughout its operation.



**Fig. 6.18** CC amplifier

The input signal is given to the base-collector circuit and the output signal is taken from the emitter-collector circuit.

Instead of using two power supplies, the required bias condition can be set up in a CC amplifier circuit with a single power supply as shown in Fig. 6.19.

$C_1$  and  $C_2$  are coupling capacitors to provide dc isolation at the input and output of the amplifier.

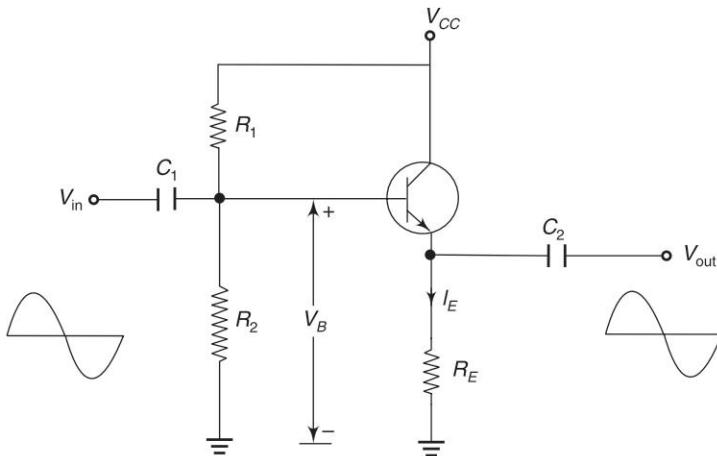


Fig. 6.19 CC amplifier with a single power supply

From Fig. 6.19,

$$\text{Output voltage } V_o = I_E R_E = \beta I_B R_E \quad (6.53)$$

When a sinusoidal ac signal is applied at the input, during the positive half cycle of the signal applied, the base potential  $V_B$  increases, thereby increasing the base current  $I_B$ . Hence, emitter current  $I_E = I_C + I_B$  increases and voltage drop across  $R_E$ , i.e., the output voltage increases.

Thus, a positive-going input signal results in a positive-going output signal as shown in Fig. 6.20. Hence, in a CC amplifier, input and output signals are in phase with each other and further, the voltage gain is approximately unity.

As the output signal taken at the emitter terminal almost follows the input signal, the CC amplifier is called the *emitter Follower*.

### Characteristics of a CC Amplifier

- (i) High current gain
- (ii) Voltage gain of approximately unity
- (iii) Power gain approximately equal to current gain
- (iv) No current or voltage phase shifts
- (v) Large input impedance
- (vi) Small output impedance

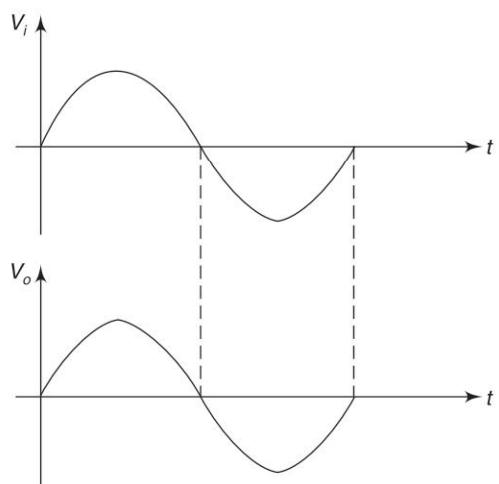
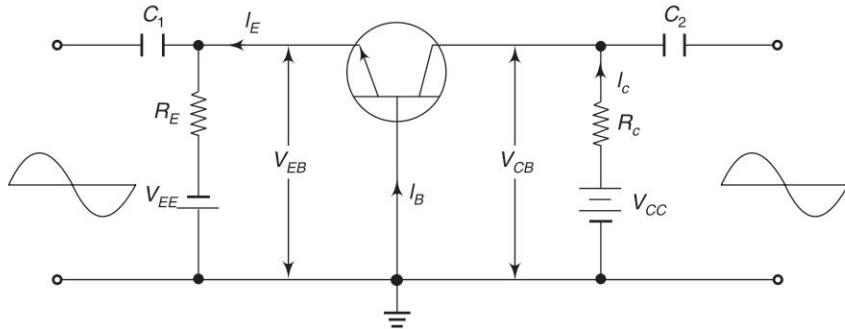


Fig. 6.20 Input and output voltages of a CC amplifier

### 6.13.3 Common-Base (CB) Amplifier

Figure 6.21 shows the circuit of a single-stage CB amplifier using an *NPN* transistor. The emitter-base junction is forward biased by the power supply  $V_{EE}$ , whereas the collector-base junction is reverse biased by  $V_{CC}$ , so that the transistor remains in the active region throughout its operation.



**Fig. 6.21** Common base amplifier

The input signal applied to the emitter-base circuit, and the output signal is taken from collector-base circuit. The output voltage ( $= V_{CB}$ ) is given by the equation

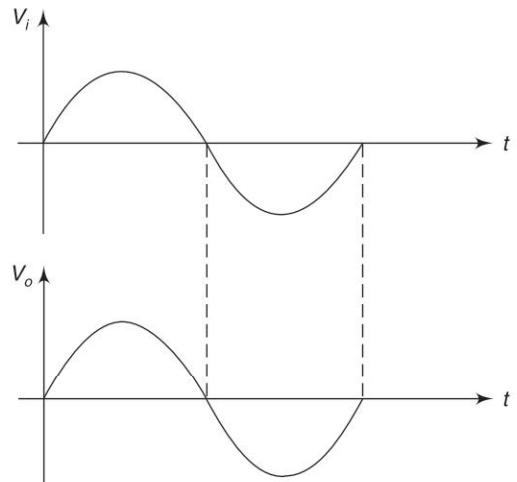
$$V_o = V_{CC} - I_C R_C \quad (6.54)$$

When a sinusoidal ac signal is applied at the input, during the positive half cycle of the applied signal, the amount of forward bias to base-emitter junction is decreased, resulting in a decrease in  $I_B$ . As a result,  $I_E$  ( $\approx \beta I_B$ ) and hence,  $I_C$  also decreases.

From Eq. (6.54), the drop  $I_C R_C$  decreases, hence  $V_o = V_{CB}$  correspondingly increases. Thus, a positive half cycle appears at the output without any phase reversal as shown in Fig. 6.22.

#### Characteristics of a CB Amplifier

- (i) Current gain of less than unity
- (ii) High voltage gain
- (iii) Power gain approximately equal to voltage gain
- (iv) No phase shift for current or voltage
- (v) Small input impedance
- (vi) Large output impedance.



**Fig. 6.22** Input and output voltages of a CB amplifier

## 6.14 SMALL-SIGNAL ANALYSIS OF SINGLE-STAGE BJT AMPLIFIERS

### 6.14.1 CE Amplifier with Fixed Bias

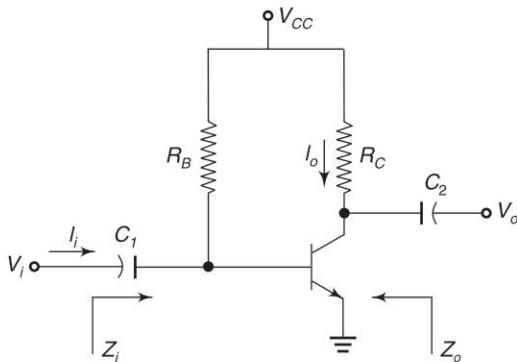
The circuit of Fig. 6.23 shows a CE amplifier in fixed-bias configuration. The ac equivalent circuit of the amplifier can be drawn by the steps mentioned as follows.

- Remove the dc effects of power supply ( $V_{CC}$ ) by grounding them.
- Replace the capacitors ( $C_1$  and  $C_2$ ) by short circuits.

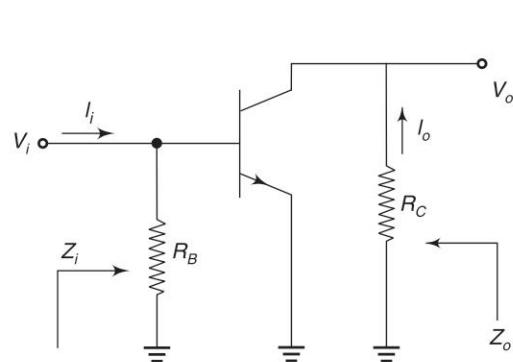
Thus, the circuit of Fig. 6.23 reduces to the ac equivalent circuit of Fig. 6.24.

Substituting the approximate hybrid model for the transistor in Fig. 6.24, the circuit reduces to that shown in Fig. 6.25.

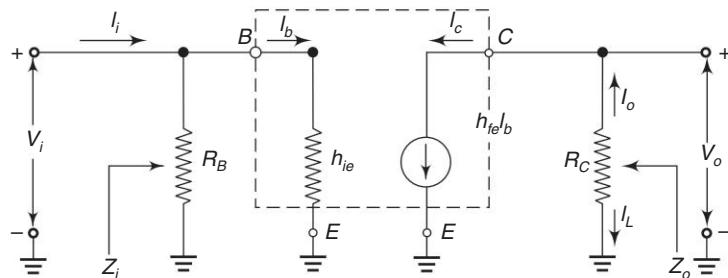
From the circuit of Fig. 6.25, the equations for input impedance, output impedance, voltage gain, and current gain can be derived.



**Fig. 6.23** CE fixed-bias configuration



**Fig. 6.24** ac equivalent circuit of CE fixed-bias amplifier



**Fig. 6.25** ac equivalent circuit of CE fixed-bias amplifier using hybrid model

### Input Impedance

$$Z_i = R_B \parallel h_{ie} \quad (6.55)$$

If

$$R_B \gg h_{ie}, \quad Z_i \approx h_{ie} \quad (6.56)$$

**Output Impedance** It is the impedance determined with  $V_i = 0$ . With  $V_i = 0$ ,  $I_b = 0$ , and  $h_{fe} I_b = 0$  indicating an open-circuit equivalence for the current source.

Hence,  $Z_o = R_L (= R_C)$

**Voltage Gain**

Voltage gain,  $A_V = \frac{V_o}{V_i}$

$$V_o = -I_o R_C$$

Substituting  $I_o = h_{fe} I_b$

$$V_o = -h_{fe} I_b R_C$$

Assuming that  $R_B \gg h_{ie}$ ,

$$I_i \approx I_b \quad \text{and} \quad V_i = I_b h_{ie}$$

Therefore,  $A_V = \frac{-h_{fe} I_b R_C}{I_b h_{ie}}$

$$= \frac{-h_{fe} R_C}{h_{ie}} \quad (6.57)$$

As  $h_{fe}$  and  $h_{ie}$  are positive,  $A_V$  is negative. The negative sign indicates a  $180^\circ$  phase shift between input and output signals.

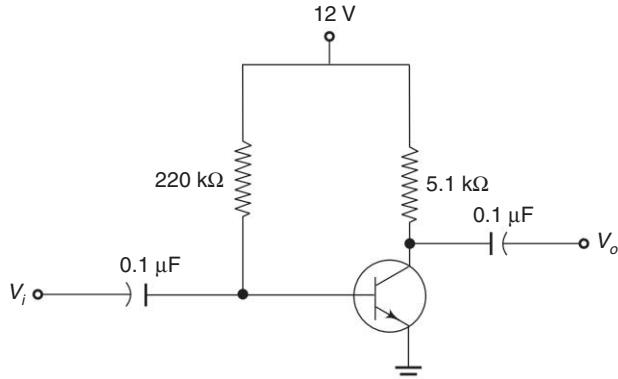
**Current Gain**

$$\begin{aligned} A_I &= \frac{I_L}{I_i} \\ &= \frac{-I_o}{I_i} \approx \frac{-h_{fe} I_b}{I_b} = -h_{fe} \end{aligned} \quad (6.58)$$

**Note:** The sign for  $A_I$  will be positive if  $A_I$  is defined as the ratio of  $I_o$  to  $I_i$ .

**EXAMPLE 6.7**

Determine the input impedance, output impedance, voltage gain, and current-gain for the CE amplifier of Fig. 6.26. The  $h$ -parameters of the transistor are  $h_{fe} = 60$ ,  $h_{ie} = 500 \Omega$  at  $I_C = 3 \text{ mA}$ .

**Fig. 6.26**

**Solution**  $R_B = 220 \text{ k}\Omega \gg h_{ie} = 500 \Omega$

From  $h$ -parameter model

$$Z_i = h_{ie} = 500 \Omega$$

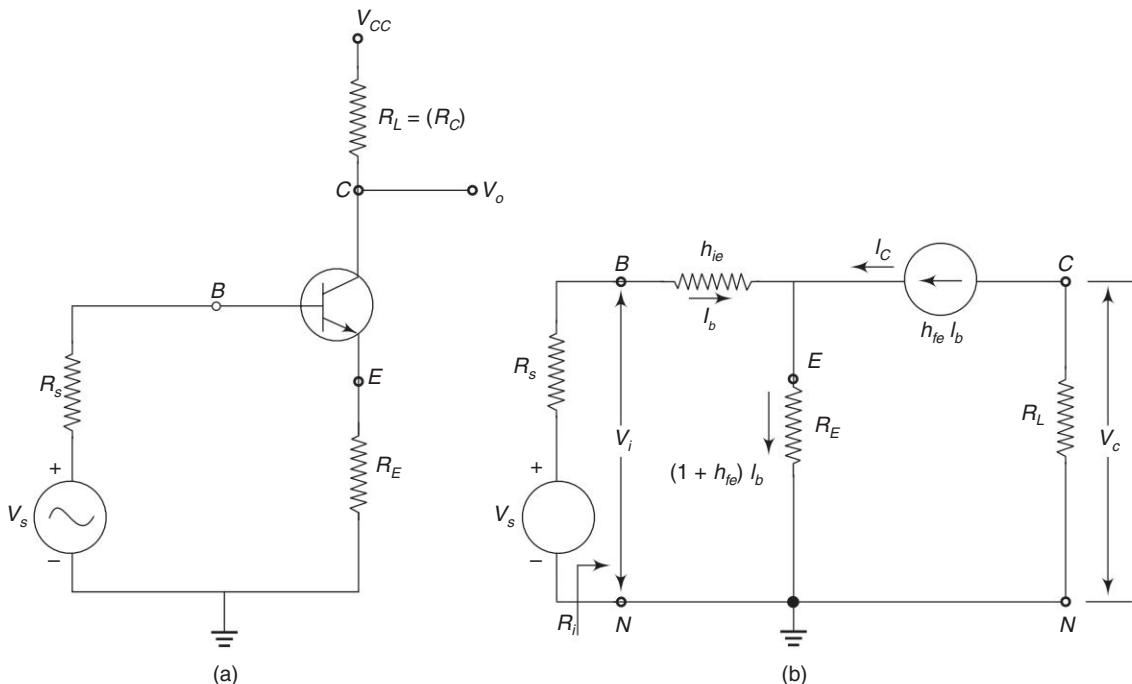
$$Z_o = R_C = 5.1 \text{ k}\Omega$$

$$A_V = \frac{-h_{fe} R_C}{h_{ie}} = \frac{-60(5.1 \times 10^3)}{500} = -612$$

$$A_I = -h_{fe} = -60$$

### 6.14.2 Common-Emitter Amplifier with Emitter Resistor

A simple and effective way to provide voltage-gain stabilization in a CE amplifier is to add an emitter resistor  $R_E$  which provides feedback as shown in Fig. 6.27. An approximate solution for this arrangement can be obtained by considering the simplified hybrid model equivalent circuit.



**Fig. 6.27** (a) CE amplifier with emitter resistor (b) Approximate small-signal equivalent circuit

#### Current Gain, $A_I$

$$A_I = -\frac{I_c}{I_b} = \frac{-h_{fe} I_b}{I_b} = -h_{fe}$$

Thus, the current gain is equal to the short-circuit current gain with  $R_E = 0$  and is unaffected by  $R_E$ .

**Input Resistance,  $R_i$** 

$$R_i = \frac{V_i}{I_b} = \frac{[h_{ie} + (1 + h_{fe})R_E]I_b}{I_b}$$

$$R_i = h_{ie} + (1 + h_{fe})R_E \quad (6.59)$$

Comparing with Eq. (6.38), the input resistance is augmented by  $(1 + h_{fe})R_E$  and may be very much larger than  $h_{ie}$ . For example, with  $R_E = 1\text{ k}\Omega$ ,  $h_{fe} = 60$ ,  $(1 + h_{fe})R_E = 61\text{ k}\Omega \gg h_{ie} \approx 1\text{ k}\Omega$ .

Hence,  $R_E$  greatly increases the input resistance of the amplifier.

**Voltage Gain,  $A_V$**  From Eq. (6.24),

$$A_V = A_I \frac{R_L}{R_i} = -\frac{h_{fe} R_L}{h_{ie} + (1 + h_{fe})R_E} \quad (6.60)$$

Thus, the addition of emitter-resistor  $R_E$  greatly reduces the voltage amplification as  $R_i$  has increased from  $h_{ie}$  to  $h_{ie} + (1 + h_{fe})R_E$ . This reduction in gain is compensated by stability improvement.

If  $(1 + h_{fe})R_E \gg h_{ie}$  and  $h_{fe} \gg 1$ , then

$$A_V \approx -\frac{h_{fe} R_L}{(1 + h_{fe})R_E} \approx \frac{-R_L}{R_E} \quad (6.61)$$

Hence, under these approximations,  $A_V$  is completely stable and independent of all transistor parameters provided stable resistances are used for  $R_L$  and  $R_E$ .

**Output Resistance,  $R_o$**  Output resistance  $R_o$  with  $R_L$  excluded is infinite and with  $R_L$  included, it is equal to  $R_L$  and is independent of  $R_E$ .

**EXAMPLE 6.8**

A CE amplifier uses load resistor  $R_C = 2\text{ k}\Omega$  in the collector circuit and is given by the voltage source  $V_s$  of internal resistance  $1000\text{ }\Omega$ . The  $h$ -parameters of the transistor are  $h_{ie} = 1300\text{ }\Omega$ ,  $h_{re} = 2 \times 10^{-4}$ ,  $h_{fe} = 55$  and  $h_{oe} = 22\text{ }\mu\text{mhos}$ . Neglecting the biasing resistors, compute the current gain  $A_I$ , input resistance  $R_i$ , voltage gain  $A_V$ , output resistance  $R_o$ , and output terminal resistance  $R_{oT}$  for the following values of emitter resistor  $R_E$  inserted in the emitter circuit: (a)  $200\text{ }\Omega$ , (b)  $400\text{ }\Omega$ , and (c)  $1000\text{ }\Omega$ . Use the approximate model for the transistor if permissible.

**Solution**

(a) For  $R_E = 200\text{ }\Omega$

$$h_{oe} \times (R_E + R_C) = (2 \times 10^3 + 200) \times (22 \times 10^{-6}) = 0.0484$$

Since  $h_{oe} \times (R_E + R_C) < 0.1$ , the approximate model is permissible.

$$A_I = -h_{fe} = -55$$

$$R_i = h_{ie} + (1 + h_{fe})R_E = 12.5\text{ k}\Omega$$

$$A_V = A_I \frac{R_C}{R_i}$$

$$= -55 \times \frac{2000}{12,500} = -8.8$$

Output resistance,  $R_o = \infty$

Output terminal resistance,  $R_{OT} = R_o \parallel R_C = 2 \text{ k}\Omega$

- (b) For  $R_E = 400 \Omega$

$$\begin{aligned} h_{oe} \times (R_E + R_C) &= (2 \times 10^3 + 400) \times (22 \times 10^{-6}) \\ &= 0.0528 \end{aligned}$$

Since  $h_{oe} \times (R_E + R_C) < 0.1$ , approximate model is permissible.

$$A_I = -h_{fe} = -55$$

$$\begin{aligned} R_i &= h_{ie} + (1 + h_{fe}) R_E \\ &= 23.7 \text{ k}\Omega \end{aligned}$$

$$A_V = A_I \frac{R_C}{R_i}$$

$$= -55 \times \frac{2000}{23,700} = -4.654$$

Output resistance,  $R_o = \infty$

Output terminal resistance,  $R_{OT} = R_o \parallel R_C = 2 \text{ k}\Omega$

- (c) For  $R_E = 1000 \Omega$

Since  $h_{oe} \times (R_E + R_C) < 0.1$ , approximate model is permissible.

$$A_I = -h_{fe} = -55$$

$$\begin{aligned} R_i &= h_{ie} + (1 + h_{fe}) R_E \\ &= 57.3 \text{ k}\Omega \end{aligned}$$

$$A_V = A_I \frac{R_C}{R_i}$$

$$= -55 \times \frac{2000}{57,300} = -1.92$$

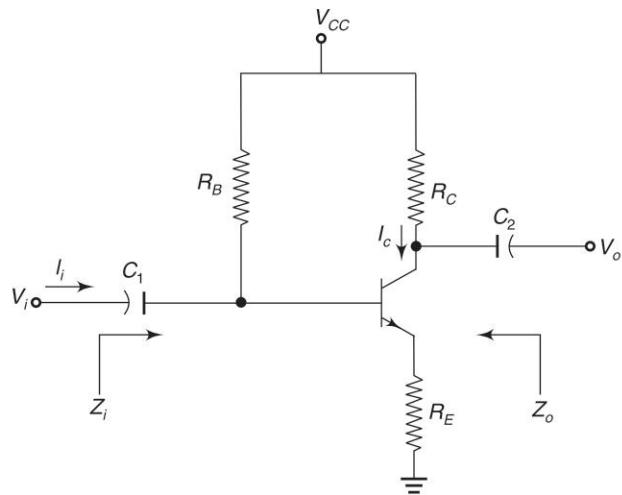
Output resistance,  $R_o = \infty$

Output terminal resistance,  $R_{OT} = R_o \parallel R_C = 2 \text{ k}\Omega$

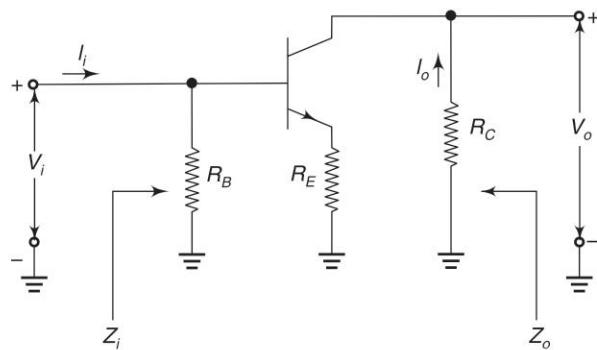
### 6.14.3 CE Amplifier with Unbypassed Emitter Resistor

The ac equivalent circuit for this amplifier shown in Fig. 6.28 can be drawn by following the steps mentioned earlier.

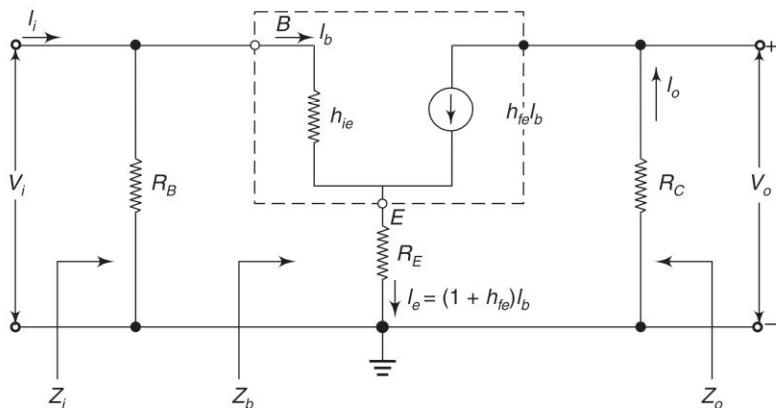
By substituting the hybrid equivalent circuit for the transistor of Fig. 6.29, the circuit reduces to that shown in Fig. 6.30.



**Fig. 6.28** CE amplifier with an unbypassed emitter resistor



**Fig. 6.29** ac equivalent circuit for a CE amplifier with an unbypassed emitter resistor



**Fig. 6.30** ac equivalent circuit for a CE amplifier with an unbypassed emitter resistor using hybrid model

**Input Impedance** Current through the emitter resistor  $R_E$  is

$$I_e = I_b + h_{fe}I_b = (1 + h_{fe})I_b$$

From Fig. 6.30,

$$V_i = I_b h_{ie} + (1 + h_{fe}) I_b R_E$$

$$Z_b = \frac{V_i}{I_b} = h_{ie} + (1 + h_{fe}) R_E \quad (6.62)$$

As  $h_{fe} \gg 1$ ,

$$Z_b \approx h_{ie} + h_{fe} R_E \quad (6.63)$$

Normally,  $h_{fe} R_E \gg h_{ie}$  leading to

$$Z_b \approx h_{fe} R_E \quad (6.64)$$

From the circuit of Fig. 6.30,

$$Z_i = R_B \parallel Z_b \quad (6.65)$$

**Output Impedance** With  $V_i = 0$ ,  $I_b = 0$ ,  $h_{fe} I_b = 0$  indicating open circuit for current source.

Hence,

$$Z_o = R_C \quad (6.66)$$

### Voltage Gain

$$A_V = \frac{V_o}{V_i}$$

From the circuit of Fig. 6.30,

$$\begin{aligned} V_o &= -I_o R_C \\ &= -(h_{fe} I_b) R_C \\ &= -h_{fe} \left( \frac{V_i}{Z_b} \right) R_C \\ A_V &= \frac{V_o}{V_i} = \frac{-h_{fe} R_C}{Z_b} \end{aligned} \quad (6.67)$$

With  $Z_b \approx h_{fe} R_E$ ,

$$\begin{aligned} A_V &= \frac{-h_{fe} R_C}{h_{fe} R_E} \\ &= \frac{-R_C}{R_E} \end{aligned} \quad (6.68)$$

### Current Gain

$$A_I = \frac{-I_o}{I_i}$$

$$I_o = h_{fe} I_b$$

where

$$I_b = I_i \frac{R_B}{R_B + Z_b}$$

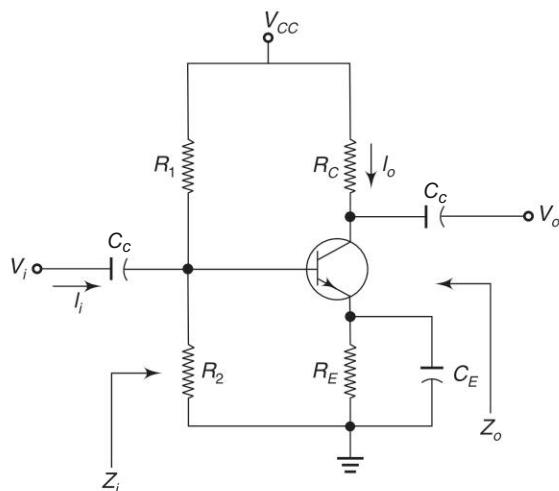
Therefore,

$$I_o = h_{fe} I_i \frac{R_B}{R_B + Z_b}$$

$$A_I = \frac{-I_o}{I_i} = \frac{-h_{fe} R_B}{R_B + Z_b} \quad (6.69)$$

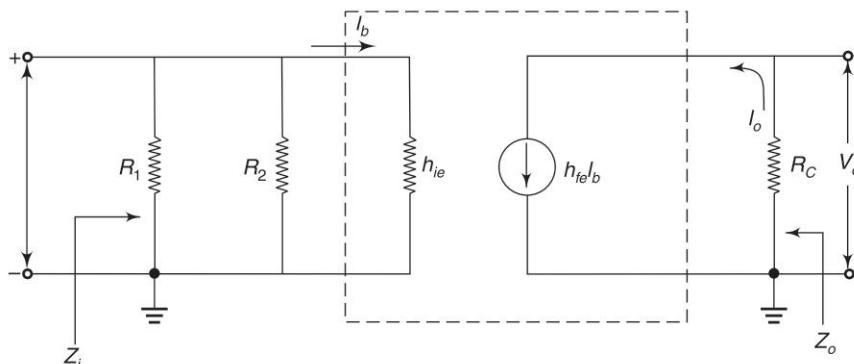
#### 6.14.4 CE Amplifier with Voltage-Divider Bias

Consider the CE amplifier of Fig. 6.31 in which the base bias is obtained by two resistors,  $R_1$  and  $R_2$ .



**Fig. 6.31** CE amplifier with voltage-divider bias

By substituting the  $h$ -parameter equivalent for the transistor, the ac equivalent circuit can be obtained directly as shown in Fig. 6.32. As the capacitor  $C_E$  bypasses  $R_E$  in the operating frequency range,  $R_E$  is omitted in the equivalent circuit.



**Fig. 6.32** ac equivalent circuit of a CE amplifier with voltage-divider bias using hybrid model

***Input Impedance***

Let

$$R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$Z_i = R_B \parallel h_{ie} \quad (6.70)$$

***Output Impedance***

$$Z_o = R_C \quad (6.71)$$

***Voltage Gain***

$$A_V = \frac{V_o}{V_i}$$

Substituting

$$V_o = -h_{fe} I_b R_C \quad \text{and} \quad V_i = I_b h_{ie}$$

$$\begin{aligned} A_V &= \frac{-h_{fe} I_b R_C}{I_b h_{ie}} \\ &= \frac{-h_{fe} R_C}{h_{ie}} \end{aligned} \quad (6.72)$$

***Current Gain***

$$A_I = \frac{-I_o}{I_i}$$

Substituting

$$I_o = -h_{fe} I_b$$

where

$$I_b = I_i \frac{R_B}{R_B + h_{ie}}$$

Therefore,

$$\begin{aligned} I_o &= -h_{fe} I_i \frac{R_B}{R_B + h_{ie}} \\ A_I &= -h_{fe} \frac{R_B}{R_B + h_{ie}} \end{aligned} \quad (6.73)$$

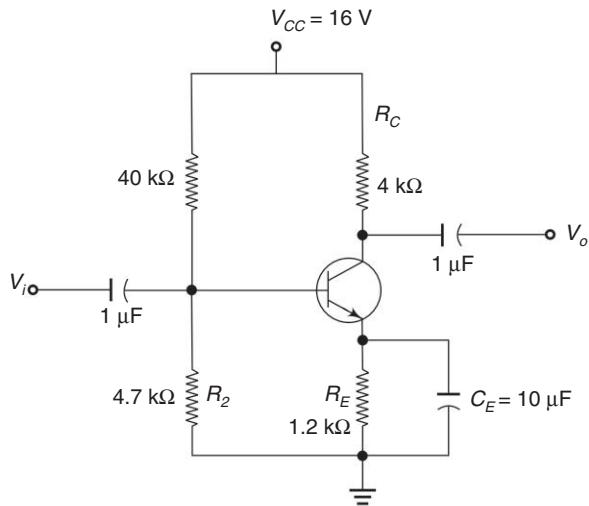
**EXAMPLE 6.9**

Determine the input impedance, output impedance, voltage gain, and current gain of the CE amplifier of Fig. 6.33 using *h*-parameter model for the transistor with  $h_{ie} = 3.2 \text{ k}\Omega$  and  $h_{fe} = 100$  at the operating conditions.

**Solution***h*-Parameter analysis

$$Z_i = R_B \parallel h_{ie}$$

$$R_B = R_1 \parallel R_2 = 40 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega = 4.2 \text{ k}\Omega$$

**Fig. 6.33**

$$Z_i = 4.2 \text{ k}\Omega \parallel 3.2 \text{ k}\Omega = 1.82 \text{ k}\Omega$$

$$Z_o = R_C = 4 \text{ k}\Omega$$

$$A_V = \frac{-h_{fe} R_C}{h_{ie}} = \frac{-100 \times 4 \times 10^3}{3.2 \times 10^3} = -125$$

$$A_I = \frac{-h_{fe} R_B}{R_B + h_{ie}} = \frac{-100 \times 4.2 \times 10^3}{(4.2 + 3.2) \times 10^3} = -56.76$$

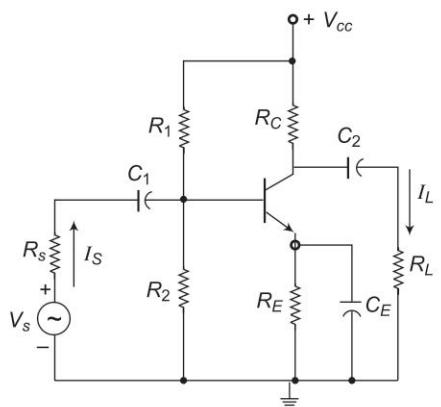
### EXAMPLE 6.10

Consider a single stage CE amplifier with  $R_s = 1 \text{ k}\Omega$ ,  $R_1 = 50 \text{ k}\Omega$ ,  $R_2 = 2 \text{ k}\Omega$ ,  $R_C = 1 \text{ k}\Omega$ ,  $R_L = 1.2 \text{ k}\Omega$ ,  $h_{fe} = 50$ ,  $h_{ie} = 1.1 \text{ k}\Omega$ ,  $h_{oe} = 25 \mu\text{A/V}$  and  $h_{re} = 2.5 \times 10^{-4}$  as shown in Fig. 6.34(a). Determine  $A_v$ ,  $R_i$ ,  $A_p$ ,  $A_I$ ,  $A_{Vs}$  and  $R_o$ .

#### Solution

*Input resistance*

$$R_i = h_{ie} - \frac{h_{fe} h_{re}}{h_{oe} + \frac{1}{R_L}} = 1.1 \times 10^{-3} - \frac{50 \times 2.5 \times 10^{-4}}{25 \times 10^{-6} + \frac{1}{545.45}} \\ = 1093.27 \Omega$$

**Fig. 6.34(a)**

*Voltage gain*

$$A_V = \frac{A_I R'_L}{R_i} = \frac{-49.32 \times 545.45}{1093.27} = -24.61 \quad (\text{since } R'_L = R_C \parallel R_L = 1\text{k} \parallel 1.2\text{k} = 545.45\Omega)$$

*Overall input resistance*

$$R'_i = R_i \parallel R_1 \parallel R_2 = 1093.27 \parallel 50 \times 10^3 \parallel 2 \times 10^3 = 696.9\Omega$$

*Overall voltage gain*

$$A_{Vs} = \frac{V_c}{V_s} = \frac{V_c}{V_b} \times \frac{V_b}{V_s}$$

Looking at voltage divider equation, we get

$$\begin{aligned} V_b &= \frac{V_s R'_i}{R_s + R'_i} \\ A_{Vs} &= \frac{V_c}{V_b} \times \frac{V_b}{V_s} = A_V \times \frac{R'_i}{R_s + R'_i} \\ &= 24.61 \times \frac{696.9}{1 \times 10^3 + 696.9} = -10.1 \end{aligned}$$

*Current gain*

$$\begin{aligned} A_I &= \frac{-h_{fe}}{1 + h_{oe} R'_L} \quad \text{where } R'_L = R_C R_L \\ &= -\frac{50}{1 + \frac{25 \times 10^{-6}}{(545.45)}} = -49.32 \end{aligned}$$

*Overall Current gain*

$$A_{Is} = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s}$$

Figure 6.34(b) shows the current division at collector and base terminals.

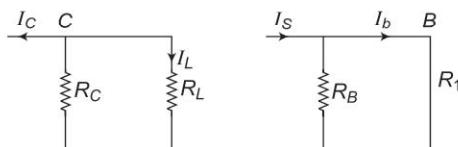


Fig. 6.34(b) Current division at Collector and Base terminals

Here

$$I_L = \frac{-I_c R_C}{R_C + R_L}$$

$$\frac{I_L}{I_c} = \frac{-R_C}{R_C + R_L}$$

$$I_b = \frac{I_s R_B}{R_B + R_i}$$

$$R_B = R_1 \parallel R_2 = 50 \times 10^3 \parallel 2 \times 10^3 = 1.923 \times 10^3 \Omega$$

$$\frac{I_b}{I_s} = \frac{R_B}{R_B + R_i}$$

$$A_{Is} = \frac{-R_C}{R_C + R_L} \times 49.32 \times \frac{R_B}{R_B + R_i}$$

$$= \frac{-1 \times 10^3}{1 \times 10^3 + 1.2 \times 10^3} \times 49.32 \times \frac{1.923 \times 10^3}{1.923 \times 10^3 + 1.093 \times 10^3} = 14.29$$

*Overall Output Resistance*

Output Admittance

$$Y_o = h_{oe} - \frac{h_{fe}h_{re}}{h_{ie} + R_s} = 25 \times 10^{-6} - \frac{50 \times 2.5 \times 10^{-4}}{1.1 \times 10^3 + 657.9} = 1.7889 \times 10^{-5} \text{ mho}$$

Output resistance

$$R_o = \frac{1}{Y_o} = 55.899 \text{ k}\Omega$$

*Overall output resistance*

$$R'_o = R_o \parallel R'_L = 55.899 \times 10^3 \Omega \parallel 545.45 = 540 \Omega$$

### EXAMPLE 6.11

A transistor has the following parameters  $h_{ie} = 800 \Omega$ ,  $h_{oe} = 10^{-7} \text{ A/V}$ ,  $h_{re} = 10^{-4}$ ,  $h_{fe} = 80$ , for a load of  $3 \text{ k}\Omega$ . Calculate the current gain, voltage gain and power gain.

#### Solution

*Current gain*

$$A_I = \frac{-h_{fe}}{1 + h_{oe}R_L} = \frac{-80}{1 + 1 \times 10^{-7} \times 3 \times 10^3} = -79.976$$

$$R_i = h_{ie} - \frac{h_{fe}h_{re}}{h_{oe} + \frac{1}{R_L}} = 800 - \frac{80 \times 10^{-4}}{10^{-4} + \frac{1}{3 \times 10^3}} = 799.9 \Omega$$

*Voltage Gain*

$$A_V = \frac{A_I R_L}{R_i} = \frac{-79.976 \times 3000}{799.9} = -299.94$$

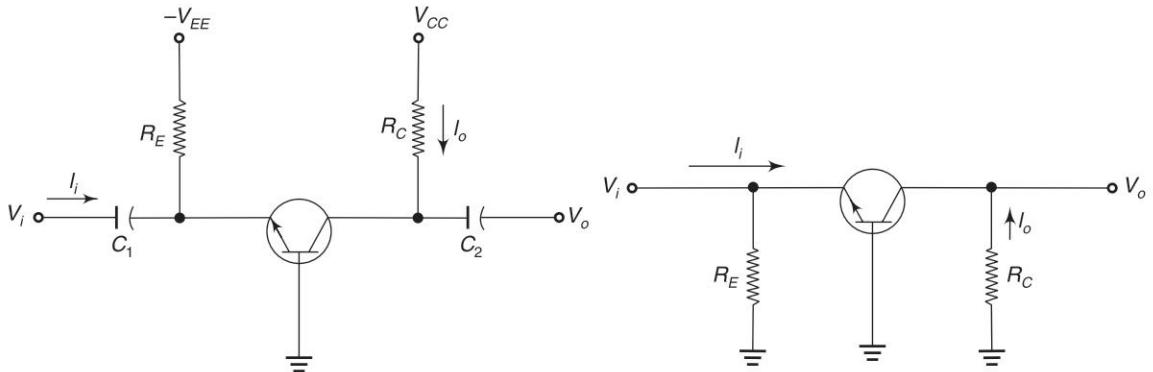
$$A_P = A_V \times A_I = -299.94 \times -79.976 = 23988$$

### 6.14.5 CB Amplifier

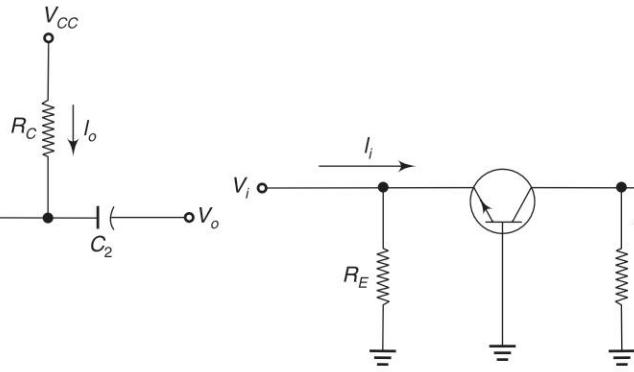
Figure 6.35 shows the circuit of a CB amplifier.

By applying the steps mentioned earlier to draw the ac equivalent circuit, the circuit of Fig. 6.35 reduces to the circuit of Fig. 6.36.

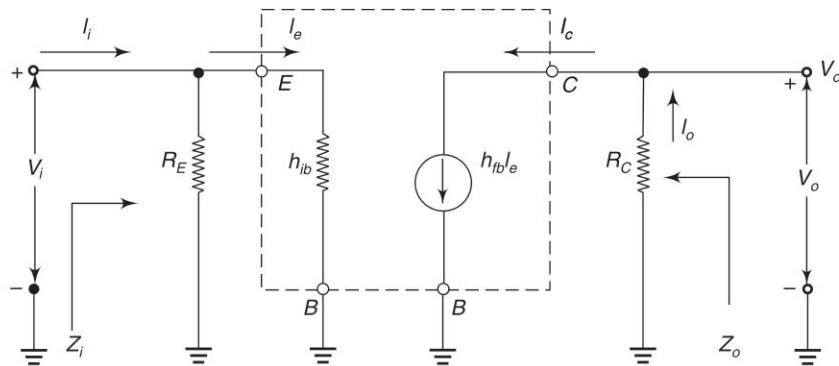
Substituting the approximate hybrid model for the transistor in CB connection, the circuit of Fig. 6.36 reduces to the circuit of Fig. 6.37.



**Fig. 6.35** CB amplifier



**Fig. 6.36** ac equivalent circuit of a CB amplifier



**Fig. 6.37** ac equivalent circuit of a CB amplifier using hybrid model

#### Input Impedance

$$Z_i = R_E \parallel h_{ib} \quad (6.74)$$

#### Output Impedance

$$Z_o = R_C \quad (6.75)$$

#### Voltage Gain

$$A_V = \frac{V_o}{V_i}$$

$$V_o = -I_o R_C = -h_{fb} I_e R_C$$

Assuming that  $R_E \gg h_{ib}$ ,

$$\begin{aligned} I_e &\approx I_i \text{ and } V_i = I_e h_{ib} \\ A_V &= \frac{V_o}{V_i} = \frac{-h_{fb} R_C}{h_{ib}} \end{aligned} \quad (6.76)$$

### Current Gain

$$\begin{aligned} A_I &= \frac{-I_o}{I_i} \\ &\approx \frac{-h_{fb} I_e}{I_e} \\ A_I &= -h_{fb} \end{aligned} \quad (6.77)$$

**Note:** As  $h_{fb}$  is negative,  $A_V$  and  $A_I$  are positive for CB configuration.

#### 6.14.6 CC Amplifier or Emitter Follower

Figure 6.38 shows the emitter-follower circuit in which the output is taken from the emitter terminal with respect to ground and the collector terminal is directly connected to  $V_{CC}$ . Since  $V_{CC}$  is at signal ground in the ac equivalent circuit as shown in Fig. 6.38, the emitter-follower circuit is also called *common-collector amplifier*.

**Current Gain** The small-signal current gain,  $A_i$ , is defined as the ratio of the output load current  $I_L$  to the input current  $I_b$ .

$$A_i = \frac{I_L}{I_b} = -\frac{I_e}{I_b} = \frac{(1 + h_{fe})I_b}{I_b} = 1 + h_{fe}$$

where

$$I_e = -(1 + h_{fe})I_b$$

**Input Resistance** From Fig. 6.39, the input resistance looking into the base is denoted as  $R_i$ , that is,

$$R_i = \frac{V_b}{I_b} = h_{ie} + (1 + h_{fe}) R_L$$

where

$$V_b = h_{ie} I_b + (1 + h_{fe}) I_b R_L$$

Therefore, the input resistance seen by the signal source  $R'_i$  is

$$R'_i = R_i \parallel R_1 \parallel R_2$$

**Voltage Gain** The small-signal voltage gain,  $A_V$ , is defined as the ratio of output voltage,  $V_o$ , to input voltage,  $V_i$ .

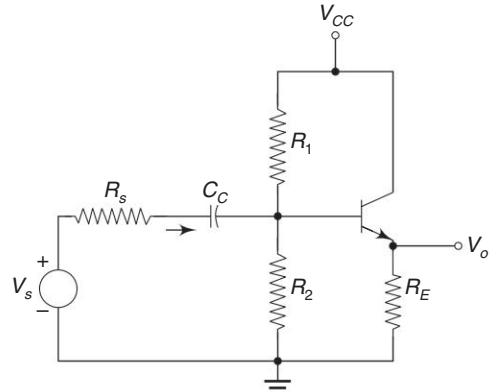


Fig. 6.38 Emitter-follower circuit

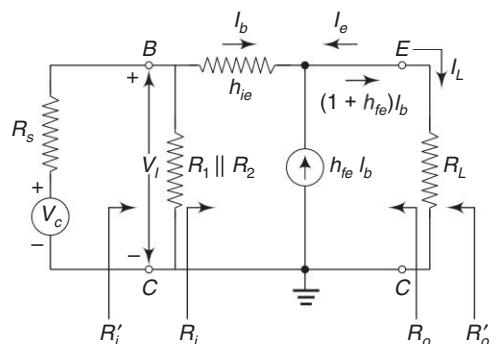


Fig. 6.39 Simplified hybrid model for emitter-follower circuit

That is,

$$A_V = \frac{V_o}{V_i} = \frac{A_i R_L}{V_i} = \frac{R_i - h_{ie}}{R_i} = 1 - \frac{h_{ie}}{R_i}$$

Therefore,  $A_V \approx 1$  but is always slightly less than one since  $R_i \gg h_{ie}$ .

**Output Admittance** From Fig. 6.39, the output admittance looking back into the emitter is denoted as  $Y_0$ , that is,

$$Y_o = h_{oe} - \frac{h_{fc} h_{rc}}{h_{ic} + R'_s}$$

where

$$R'_s = R_s \parallel R_1 \parallel R_2$$

Neglecting  $h_{oc}$  and assuming  $h_{rc} = 1$ ,  $h_{fc} = -(1 + h_{fe})$ , we get

$$Y_o = \frac{-h_{fe}}{h_{ie} + R'_s}$$

Therefore,

$$R_o = \frac{-h_{ic} + R'_s}{h_{fc}} = \frac{h_{ie} + R'_s}{1 + h_{fe}}$$

Hence, the output resistance looking back into the output terminals,  $R'_o$ , is the load resistance,  $R_L$ , in parallel with the resistance looking back into the emitter,  $R_o$ , that is,

$$R'_o = R_o \parallel R_L$$

### EXAMPLE 6.12

For the emitter follower shown in Fig. 6.38, the circuit parameters are  $R_s = 500 \Omega$ ,  $R_1 = R_2 = 50 \text{ k}\Omega$ ,  $R_L = 2 \text{ k}\Omega$ ,  $h_{fe} = 100$ , and  $h_{ie} = 1.1 \text{ k}\Omega$ . Determine the input resistance, output resistance, current gain and voltage gain.

#### Solution

(a) To determine input resistance ( $R_i$ )

$$R_i = h_{ie} + (1 + h_{fe})R_L = 1.1 \times 10^3 + (1 + 100) \times 2 \times 10^3 = 203.1 \text{ k}\Omega$$

$$R'_i = R_i \parallel R_1 \parallel R_2 = 203.1 \times 10^3 \parallel 50 \times 10^3 \parallel 50 \times 10^3 = 22.26 \text{ k}\Omega$$

(b) To determine output resistance ( $R_o$ )

$$\begin{aligned} R_o &= \frac{h_{ie} + R'_s}{1 + h_{fe}} = \frac{1.1 \times 10^3 + (500 \parallel 50 \times 10^3 \parallel 50 \times 10^3)}{1 + 100} \\ &= \frac{1.59 \times 10^3}{101} = 15.74 \Omega \end{aligned}$$

$$R'_o = R_o \parallel R_L = 15.74 \parallel 2 \times 10^3 = 15.62 \Omega$$

(c) To determine current gain ( $A_i$ )

$$A_i = 1 + h_{fe} = 1 + 100 = 101$$

(d) To determine voltage gain ( $A_V$ )

$$A_V = 1 - \frac{h_{ie}}{R_i} = 1 - \frac{1.1 \times 10^3}{203.1 \times 10^3} = 0.9946$$

### EXAMPLE 6.13

Calculate the current gain  $A_I$ , voltage gain  $A_V$ , input resistance  $R_i$ , and output resistance  $R_o$  for the common collector amplifier shown in Fig. 6.40. The transistor parameters are  $h_{ic} = 1.4 \text{ k}\Omega$ ,  $h_{fc} = 100$ ,  $h_{rc} = 20 \mu\text{A/V}$ , and  $h_{oc} = 20 \times 10^6$ .

#### Solution

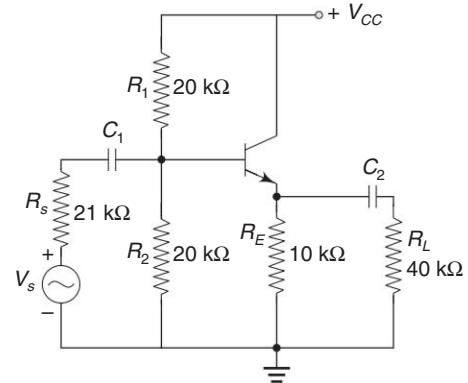
Current gain  $A_I = \frac{-h_{fc}}{1 + h_{oc} R'_L}$

where  $R'_L = R_E \parallel R_L = (40 \parallel 10) \text{ k}\Omega = 8 \text{ k}\Omega$

$$A_I = \frac{-(-100)}{1 + (20) \times 10^6 \times 8 \times 10^3} = \frac{100}{1.16} = 86.2$$

Input resistance

$$\begin{aligned} R_i &= h_{ic} + h_{rc} A_I R'_L \\ &= 1.4 \times 10^3 + (1)(86.2)(8 \times 10^3) = 691 \text{ k}\Omega \end{aligned}$$



**Fig. 6.40**

Voltage gain  $A_V = \frac{A_I R'_L}{R_i} = \frac{(86.2)(8 \times 10^3)}{691 \times 10^3} = 0.998$

Output resistance,

$$R_o = \frac{1}{Y_o}$$

$$Y_o = h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic} + R'_s}$$

where  $R'_s = R_s \parallel R_1 \parallel R_2 = 1 \parallel 20 \parallel 20 \text{ k}\Omega = 0.9 \text{ k}\Omega$

$$Y_o = 20 \times 10^{-6} - \frac{(-100)(1)}{(1.4 \times 10^3) + (0.9 \times 10^3)} = 43478.26 \times 10^{-6}$$

$$R_o = 22.99 \text{ }\Omega$$

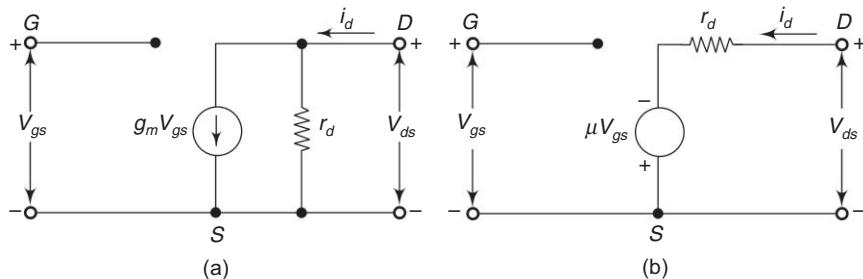
$$R'_o = R_o \parallel R'_L = (22.99) \parallel (8 \times 10^3) = 22.92 \text{ }\Omega$$

## 6.15 GENERALIZED ANALYSIS OF FET SMALL SIGNAL MODEL

The small-signal models for the common source FET can be used for analyzing the three basic FET amplifier configurations: (i) Common source (CS), (ii) Common drain (CD) or *source-follower*, and (iii) Common gate (CG). The CS amplifier which provides good voltage amplification is most frequently used. The CD amplifier

with high input impedance and near-unity voltage gain is used as a buffer amplifier and the CG amplifier is used as a high-frequency amplifier. The small-signal current-source model for the FET in CS configuration is redrawn in Fig. 6.41(a) and the voltage-source model shown in Fig. 6.41(b) can be derived by finding the Thevenin's equivalent for the output part of Fig. 6.41(a).  $\mu$ ,  $r_d$  and  $g_m$  are the amplification factor, drain resistance, and mutual conductance of the FET.

Field Effect Transistor (FET) amplifiers provide an excellent voltage gain with the added feature of high input impedance. They have low power consumption with a good frequency range, and minimal size and weight. The noise output level is low. This feature makes them very useful in the amplifier circuits meant for very small-signal amplifications. JFETs, depletion MOSFETs and enhancement MOSFETs are used in the design of amplifiers having comparable voltage gains. However, the depletion MOSFET circuit realizes much higher input impedance than the equivalent JFET configuration. Because of the high input impedance characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. The common-source configuration is the most popular one, providing an inverted and amplified signal. However, one also finds the common drain (source follower) circuits providing unity gain with no inversion and common gate circuits providing gain with no inversion. Due to very high input impedance, the input current is generally assumed to be negligible, and it is of the order of few microamperes and the current gain is an undefined quantity. Output impedance values are comparable for both the BJT and FET circuits



**Fig. 6.41** (a) Small-signal current-source model for FET in CS configuration  
 (b) Voltage-source model for FET in CS configuration

## 6.16 ANALYSIS OF CS AMPLIFIER

A simple common-source amplifier is shown in Fig. 6.42(a), and the associated small-signal equivalent circuit using the voltage-source model of FET is shown in Fig. 6.42(b).

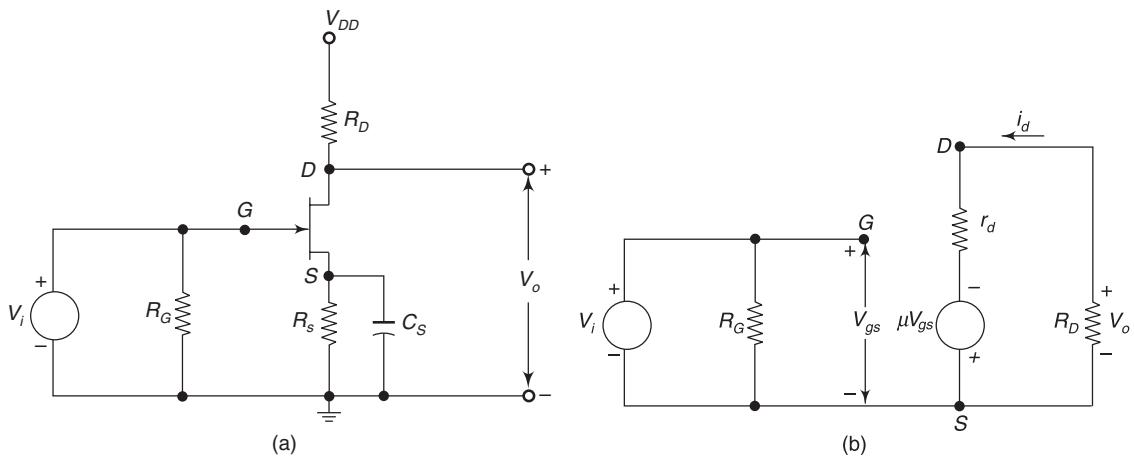
**Voltage Gain** Source resistor ( $R_s$ ) is used to set the  $Q$ -point but is bypassed by  $C_s$  for mid-frequency operation. From the small-signal equivalent circuit, the output voltage,

$$V_o = \frac{-R_D}{R_D + r_d} \mu V_{gs} \quad (6.78)$$

where  $V_{gs} = V_i$ , the input voltage.

Hence, the voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{-\mu R_D}{R_D + r_d} \quad (6.79)$$



**Fig. 6.42** (a) Common source amplifier (b) Small-signal equivalent circuit of CS amplifier

**Input Impedance** From Fig. 6.42(b), the input impedance is given by

$$Z_i = R_G$$

For voltage divider bias as in  $CE$  amplifiers of BJT,

$$R_G = R_1 \parallel R_2$$

**Output Impedance** Output impedance is the impedance measured at the output terminals with the input voltage  $V_i = 0$ .

From Fig. 6.42(b), when  $V_i = 0$ ,  $V_{gs} = 0$  and hence,

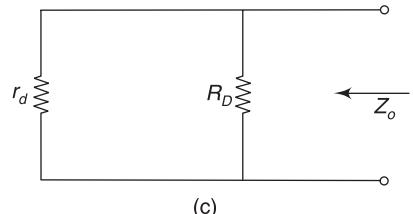
$$\mu V_{gs} = 0$$

Then the equivalent circuit for calculating output impedance is given in Fig. 6.42(c).

Output impedance  $Z_o = r_d \parallel R_D$

Normally,  $r_d$  will be far greater than  $R_D$ .

Hence,  $Z_o \approx R_D$



**Fig. 6.42** (c) Calculation of output impedance

### EXAMPLE 6.14

In the CS amplifier of Fig. 6.42(a), let  $R_D = 5 \text{ k}\Omega$ ,  $R_G = 10 \text{ M}\Omega$ ,  $\mu = 50$ , and  $r_d = 35 \text{ k}\Omega$ . Evaluate the voltage gain  $A_V$ , input impedance  $Z_i$ , and output impedance  $Z_o$ .

**Solution** The voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{-\mu R_D}{R_D + r_d} = \frac{-50 \times 5 \times 10^3}{5 \times 10^3 + 35 \times 10^3} = \frac{-250 \times 10^3}{40 \times 10^3} = -6.25$$

The minus sign indicates a  $180^\circ$  phase shift between  $V_i$  and  $V_o$ .

Input impedance  $Z_i = R_G = 10 \text{ M}\Omega$

Output impedance  $Z_o \approx R_D = 5 \text{ k}\Omega$

### EXAMPLE 6.15

A FET amplifier in the common-source configuration uses a load resistance of  $500 \text{ k}\Omega$ . The ac drain resistance of the device is  $100 \text{ k}\Omega$  and the transconductance is  $0.8 \text{ mA V}^{-1}$ . Calculate the voltage gain of the amplifier.

#### Solution

Given load resistance,  $R_L = R_D = 500 \text{ k}\Omega$ ,  $r_d = 100 \Omega$ ,  $g_m = 0.8 \text{ mA V}^{-1}$

The transconductance  $\mu = g_m r_d = 0.8 \times 10^{-3} \times 100 \times 10^3 = 80$

The voltage gain,  $A_V = -\frac{\mu R_D}{R_D + r_d} = \frac{-80 \times 500 \times 10^3}{500 \times 10^3 + 100 \times 10^3} = -\frac{40 \times 10^6}{600 \times 10^3} = -66.67$

## 6.17 ANALYSIS OF CD AMPLIFIER

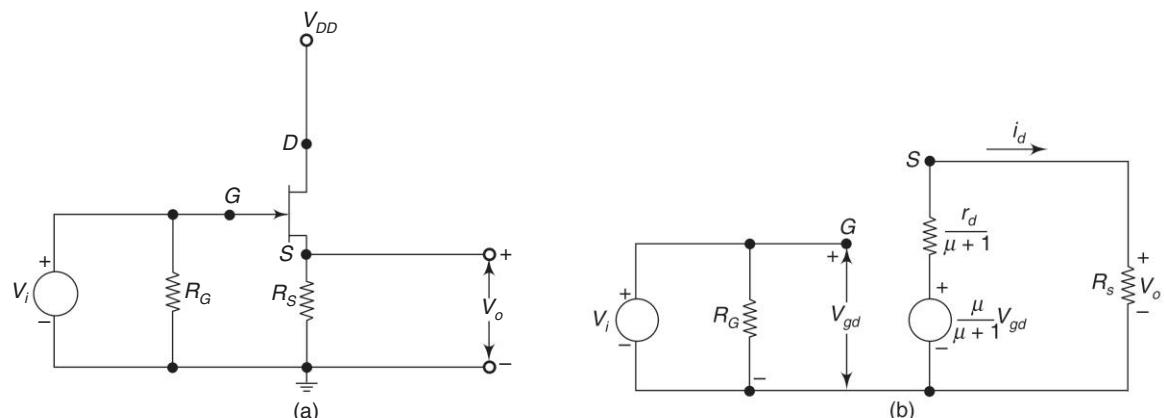
A simple common-drain amplifier is shown in Fig. 6.43(a) and the associated small-signal equivalent circuit using the voltage-source model of FET is shown in Fig. 6.43(b). Since voltage  $V_{gd}$  is more easily determined than  $V_{gs}$ , the voltage source in the output circuit is expressed in terms of  $V_{gd}$  using Thevenin's theorem. The output voltage,

$$V_o = \frac{R_s}{R_s + \frac{r_d}{\mu + 1}} \times \frac{\mu}{\mu + 1} V_{gd} = \frac{\mu R_s V_{gd}}{(\mu + 1) R_s + r_d} \quad (6.80)$$

where  $V_{gd} = V_i$ , the input voltage.

Hence, the voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{\mu R_s}{(\mu + 1) R_s + r_d} \quad (6.81)$$



**Fig. 6.43** (a) Common drain amplifier (b) Small-signal equivalent circuit of a CD amplifier

**Input Impedance** From Fig. 6.43(b), input impedance  $Z_i = R_G$

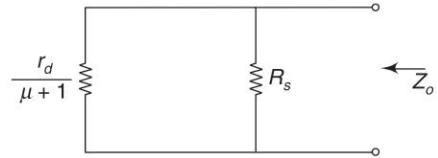
**Output Impedance** From Fig. 6.43(b), output impedance measured at the output terminals with input voltage  $V_i = 0$  can be simply calculated from the following equivalent circuit.

$$\text{As } V_i = 0; V_{gd} = 0; \frac{\mu}{\mu + 1} V_{gd} = 0$$

$$\text{Output impedance } Z_o = \frac{r_d}{\mu + 1} \| R_s$$

when  $\mu \gg 1$  (typical value of  $\mu = 50$ )

$$Z_o \approx \frac{r_d}{\mu} \| R_s = \frac{1}{g_m} \| R_s$$



**Fig. 6.43 (c)** Calculation of output impedance

### EXAMPLE 6.16

In the CD amplifier of Fig. 6.43(b), let  $R_s = 4 \text{ k}\Omega$ ,  $R_G = 10 \text{ M}\Omega$ ,  $\mu = 50$ , and  $r_d = 35 \text{ k}\Omega$ . Evaluate the voltage gain  $A_V$ , input impedance  $Z_i$  and output impedance  $Z_o$ .

#### Solution

The voltage gain,

$$\begin{aligned} A_V &= \frac{V_o}{V_i} = \frac{\mu R_s}{(\mu + 1) R_s + r_d} \\ &= \frac{50 \times 4 \times 10^3}{(50 + 1) \times 4 \times 10^3 + 35 \times 10^3} = 0.836 \end{aligned}$$

The positive value indicates that  $V_o$  and  $V_i$  are in-phase and further note that  $A_V < 1$  for CD amplifier.

$$\text{Input impedance } Z_i = R_G = 10 \text{ M}\Omega$$

$$\begin{aligned} \text{Output impedance } Z_o &= \frac{1}{g_m} \| R_s = \left( \frac{r_d}{\mu} \right) \| R_s \\ Z_o &= \frac{35 \times 10^3}{50} \| 4 \times 10^3 = 595.7 \Omega \end{aligned}$$

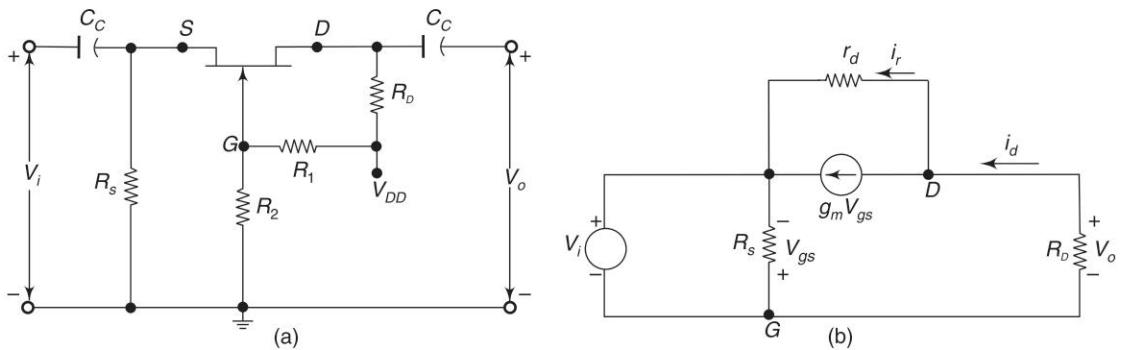
## 6.18 ANALYSIS OF CG AMPLIFIER

A simple common-gate amplifier is shown in Fig. 6.44(a) and the associated small-signal equivalent circuit using the current-source model of FET is shown in Fig. 6.44(b).

**Voltage Gain** From the small-signal equivalent circuit by applying KCL,  $i_r = i_d - g_m V_{gs}$ . Applying KVL around the outer loop gives

$$V_o = (i_d - g_m V_{gs}) r_d - V_{gs}$$

$$\text{But } V_i = -V_{gs} \quad \text{and} \quad i_d = \frac{-V_o}{R_D}$$

**Fig. 6.44 (a) Common-gate amplifier (b) Small-signal equivalent circuit of a CG amplifier**

$$\text{Thus, } V_o = \left( -\frac{V_o}{R_D} + g_m V_i \right) r_d + V_i$$

Hence, the voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{(g_m r_d + 1) R_D}{R_D + r_d} \quad (6.82)$$

**Input Impedance** Figure 6.44(b) is modified for calculation of input impedance as shown in Fig. 6.44(c).

Current through  $r_d$  is given by

$$I_{rd} = -I_r = I_1 + g_m V_{gs}$$

$$I_1 = I_{rd} - g_m V_{gs}$$

where

$$I_{rd} = \frac{V_i - V_o}{r_d}$$

$$= \frac{V_i - I_{RD} R_D}{r_d}$$

$$\text{Hence, } I_1 = \frac{V_i - I_{RD} R_D}{r_d} - g_m V_{gs}$$

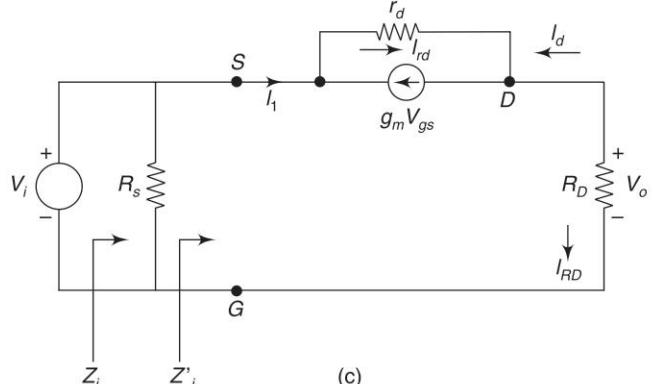
From Fig. 6.44(c),

$$V_i = -V_{gs}$$

$$I_1 = \frac{V_i - I_{RD} R_D}{r_d} + g_m V_i$$

$$= \frac{V_i}{r_d} - \frac{I_{RD} R_D}{r_d} + g_m V_i$$

$$I_1 + \frac{I_{RD} R_D}{r_d} = \frac{V_i}{r_d} + g_m V_i$$

**Fig. 6.44 (c) Modified equivalent circuit**

From Fig. 6.44(c),

$$I_1 = I_{RD}$$

Therefore,  $I_1 \left[ \frac{r_d + R_D}{r_d} \right] = V_i \left[ \frac{1}{r_d} + g_m \right]$

$$\frac{V_i}{I_1} = \frac{r_d + R_D}{1 + g_m r_d} = Z'_i$$

From Fig. 6.44(c),

$$\begin{aligned} Z_i &= R_s \parallel Z'_i \\ &= R_s \parallel \frac{r_d + R_D}{1 + g_m r_d} \end{aligned}$$

In practice,  $r_d \gg R_D$  and  $g_m r_d \gg 1$ .

Therefore,  $Z_i = R_s \parallel \frac{r_d}{g_m r_d}$

Therefore,  $Z_i = R_s \parallel \frac{1}{g_m}$

**Output Impedance** It is the impedance seen from the output terminals with input short-circuited.

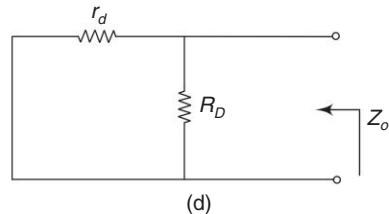
From Fig. 6.44(c), when  $V_i = 0$ ,  $V_{sg} = 0$ , the resultant equivalent circuit is shown in Fig. 6.44(d).

$$Z_o = r_d \parallel R_D$$

as

$$r_d \gg R_D$$

$$Z_o \approx R_D$$



**Fig. 6.44 (d)** Equivalent circuit for output impedance

### EXAMPLE 6.17

In the CG amplifier of Fig. 6.44(b), let  $R_D = 2 \text{ k}\Omega$ ,  $R_s = 1 \text{ k}\Omega$ ,  $g_m = 1.43 \times 10^{-3} \text{ mho}$ , and  $r_d = 35 \text{ k}\Omega$ . Evaluate the voltage gain  $A_V$ , input impedance  $Z_i$ , and output impedance  $Z_o$ .

**Solution** The voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{(g_m r_d + 1)R_D}{R_D + r_d} = \frac{(1.43 \times 10^{-3} \times 35 \times 10^3 + 1) 2 \times 10^3}{2 \times 10^3 + 35 \times 10^3} = 2.75$$

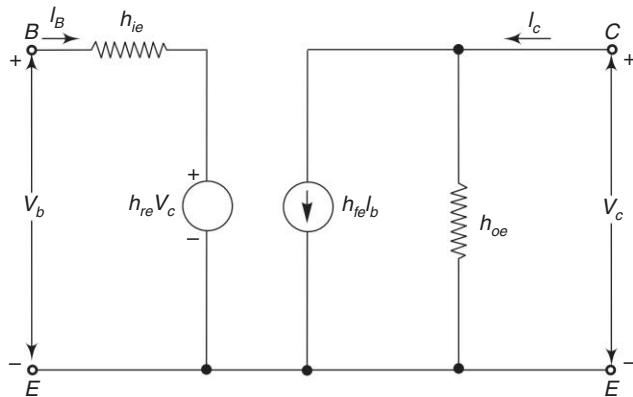
Input impedance  $Z_i = R_s \parallel \frac{1}{g_m} = 1 \times 10^3 \parallel \frac{10^3}{1.4} = 0.41 \text{ k}\Omega$

Output impedance  $Z_o \approx R_D = 2 \text{ k}\Omega$

## 6.19 COMPARISON OF FET MODEL WITH BJT MODEL

The  $h$ -parameter model of a BJT in CE configuration is redrawn in Fig. 6.45 for comparison.

The BJT also has a Norton's output circuit, but the current generated depends on the input current and not on the input voltage as in FET. There is no feedback from output to input in the FET, whereas a feedback exists in the BJT through the parameter  $h_{re}$ . The high (almost infinite) input resistance of the FET is replaced by an input resistance of about  $1\text{ k}\Omega$  for a CE amplifier.



**Fig. 6.45**  $h$ -parameter model of BJT in CE configuration

Due to the high input impedance and the absence of feedback from output to input, FET is a much more ideal amplifier than the BJT at low frequencies. This becomes invalid beyond the audio range as the low frequency model of FET, shown in Fig. 6.41(a), is not valid in the high frequency range.

### REVIEW QUESTIONS

- Derive the network parameters for two-port devices.
- Why are hybrid parameters called so? Define them.
- What are the salient features of hybrid parameters?
- Derive the equations for voltage gain, current gain, input impedance, and output admittance for a BJT using low frequency  $h$ -parameter model for (i) CE configuration (ii) CB configuration, and (iii) CC configuration.
- Compare the performance of a BJT as an amplifier in CE, CB, and CC configurations.
- Justify the validity of approximate hybrid model applicable in low-frequency region.
- Derive the equations for voltage gain, current gain, input impedance, and output impedance for a BJT using the approximate  $h$ -parameter model for (i) CE configuration, (ii) CB configuration, and (iii) CC configuration.
- A CE amplifier is drawn by a voltage source of internal resistance  $R_s = 1000\ \Omega$  and the load impedance is a resistance  $R_L = 1200\ \Omega$ . The  $h$ -parameters are  $h_{ie} = 1.2\text{ k}\Omega$ ,  $h_{re} = 2 \times 10^{-4}$ ,  $h_{fe} = 60$  and  $h_{oe} = 25\ \mu\text{A/V}$ . Compute the current gain  $A_i$ , input resistance  $R_i$ , voltage gain  $A_V$  and output resistance  $R_o$  using exact analysis and using approximate analysis.

[Ans. Exact analysis:  $A_i = -58.25$ ,  $R_i = 1.186\text{ k}\Omega$ ,  $A_V = -58.937$ ,  $R_o = 51.162\text{ k}\Omega$ ,  
Approximate analysis:  $A_i = -60$ ,  $R_i = 1.2\text{ k}\Omega$ ,  $A_V = -60$ ,  $Z_o = \infty$ ]

- A CE amplifier uses a load resistor  $R_C = 2.5\text{ k}\Omega$  in the collector circuit and is given by the voltage

source  $V_s$  of internal resistance  $600 \Omega$ . The  $h$ -parameters of the transistor are  $h_{ie} = 1300 \Omega$ ,  $h_{re} = 2 \times 10^{-4}$ ,  $h_{fe} = 55$  and  $h_{oe} = 22 \mu$  mhos. Neglecting the biasing resistors across the  $V_{CC}$  supply, compute the current gain  $A_I$ , input resistance  $R_i$ , voltage gain  $A_V$ , output resistance  $R_o$ , and output terminal resistance  $R_{oT}$  for the following values of emitter resistor  $R_E$  inserted in the emitter circuit: (i)  $200 \Omega$ , (ii)  $400 \Omega$ , and (iii)  $1000 \Omega$ . Use the approximate model for the transistor if permissible.

$$\begin{aligned} &[Ans. (i) A_I = -55, R_i = 12.5 \text{ k}\Omega, A_V = -11, R_o = \infty, R_{oT} = 2.5 \text{ k}\Omega \\ &\quad (ii) A_I = -55, R_i = 23.7 \text{ k}\Omega, A_V = -5.8, R_o = \infty, R_{oT} = 2.5 \text{ k}\Omega \\ &\quad (iii) A_I = -55, R_i = 57.3 \text{ k}\Omega, A_V = -2.399, R_o = \infty, R_{oT} = 2.5 \text{ k}\Omega.] \end{aligned}$$

10. For a CB transistor amplifier driven by a voltage source of internal resistance  $R_s = 600 \Omega$ , the load impedance is a resistor  $R_L = 1200 \Omega$ . The  $h$ -parameters are  $h_{ib} = 22 \Omega$ ,  $h_{rb} = 4 \times 10^{-4}$ ,  $h_{fb} = -0.98$  and  $h_{ob} = 0.25 \mu\text{A/V}$ . Compute the current gain  $A_I$ , the input impedance  $R_i$ , voltage gain  $A_V$ , overall voltage gain  $A_{Vs}$ , overall current gain  $A_{Is}$ , output impedance  $Z_o$ , and power gain  $A_P$ .

$$\begin{aligned} &[Ans. \text{ Exact analysis: } A_I = 0.9797, R_i = 22.47 \Omega, A_V = 52.32, \\ &\quad A_{Vs} = 1.8886, A_{Is} = 0.9443, R_o = 1.13607 \text{ M}\Omega, A_P = 51.257. \\ &\quad \text{Approximate analysis } A_I = 0.98, R_i = 22 \Omega, A_V = 53.4545, \\ &\quad A_{Vs} = 1.8906, A_{Is} = 0.9453, R_o = \infty, A_P = 52.381] \end{aligned}$$

11. A voltage source of internal resistance  $R_s = 600 \Omega$  drives a CC amplifier using load resistance  $R_L = 1000 \Omega$ . The CE  $h$ -parameters are  $h_{ie} = 1200 \Omega$ ,  $h_{re} = 2 \times 10^{-4}$ ,  $h_{fe} = 60$ , and  $h_{oe} = 25 \mu\text{A/V}$ . Compute the current gain  $A_I$ , the input impedance  $R_i$ , voltage gain  $A_V$  and output resistance  $R_o$  using approximate analysis and exact analysis.

$$\begin{aligned} &[Ans. \text{ Exact analysis: } A_I = 59.512, R_i = 60.712 \text{ k}\Omega, A_V = 0.9802, R_o = 29.486 \Omega. \\ &\quad \text{Approximate analysis } A_I = 61, R_i = 62.2 \text{ k}\Omega, A_V = 0.9807, R_o = 29.508 \Omega] \end{aligned}$$

12. What is an amplifier? What are the various types of amplifiers?  
 13. Draw the circuit diagram of a CE amplifier and explain its working.  
 14. Draw the circuit diagram of a CC amplifier and explain its working.  
 15. What is an emitter follower? Explain.  
 16. Draw the circuit diagram of a CB amplifier and explain its working.  
 17. Draw the ac equivalent of a CE amplifier with fixed bias using  $h$ -parameter model and derive the equations for input impedance, output impedance, voltage gain, and current gain.  
 18. Determine the input impedance, output impedance, voltage gain, and current gain for the CE amplifier of Fig. 6.23 using  $h$ -parameter model. The biasing resistors are  $R_C = 4 \text{ k}\Omega$  and  $R_B = 1.13 \text{ M}\Omega$ . The supply voltage  $V_{CC} = 12 \text{ V}$ . The  $h$ -parameters of the transistor are  $h_{fe} = 100$ ,  $h_{ie} = 2600 \Omega$  at 1 mA.

$$[Ans. Z_i = 2.6 \text{ k}\Omega; Z_o = 4 \text{ k}\Omega; A_V = -153.8; A_I = -100]$$

19. Draw the ac equivalent circuit of a CE amplifier with unbypassed emitter resistor using  $h$ -parameter model and derive the equations for input impedance, output impedance, voltage gain, and current gain.  
 20. Draw the ac equivalent circuit of a CE amplifier with voltage divider bias using  $h$ -parameter model and derive the equations for input impedance, output impedance, voltage gain, and current gain.  
 21. Determine the input impedance, output impedance, voltage gain, and current gain for the CE amplifier of Fig. 6.33 using  $h$ -parameter model. The biasing resistors are  $R_C = 5 \text{ k}\Omega$ ,  $R_E = 0.75 \text{ k}\Omega$ ,  $R_1 = 23 \text{ k}\Omega$  and  $R_2 = 2.8 \text{ k}\Omega$ . The supply voltage  $V_{CC} = 11 \text{ V}$ . The  $h$ -parameters of the transistor are  $h_{fe} = 90$  and  $h_{ie} = 2.835 \text{ k}\Omega$ .

$$[Ans. h\text{-parameter: } Z_i = 1.32 \text{ k}\Omega; Z_o = 5 \text{ k}\Omega; A_V = -158.73; A_I = -42.17]$$

22. Draw the ac equivalent circuit of a CB amplifier using  $h$ -parameter model and derive the equations for input impedance, output impedance, voltage gain, and current gain.  
 23. Draw the ac equivalent circuit of a CC amplifier using  $h$ -parameter model and derive the equations for input impedance, output impedance, voltage gain, and current gain.  
 24. Draw the small-signal model of FET for low-frequency region and compare them with the BJT models.

25. Draw the small-signal equivalent circuit of FET amplifier in CS connection and derive the equations for voltage gain, input impedance, and output impedance.
26. In the CS amplifier of Fig. 6.42(a), let  $R_D = 4 \text{ k}\Omega$ ,  $R_G = 50 \text{ M}\Omega$ ,  $\mu = 40$ ,  $r_d = 40 \text{ k}\Omega$ . Evaluate  $A_V$ ,  $Z_i$  and  $Z_o$ . [Ans.  $A_V = -3.64$ ,  $Z_i = 50 \text{ M}\Omega$   $Z_o = 4 \text{ k}\Omega$ ]
27. Draw the small-signal equivalent circuit of FET amplifier in CD connection and derive the equation for voltage gain, input impedance, and output impedance.
28. In the CD amplifier of Fig. 6.43(a), let  $R_s = 2 \text{ k}\Omega$ ,  $R_G = 10 \text{ M}\Omega$ ,  $\mu = 40$ ,  $r_d = 40 \text{ k}\Omega$ . Calculate  $A_v$ ,  $Z_i$ , and  $Z_o$ . [Ans.  $A_V = 0.66$ ,  $Z_i = 10 \text{ M}\Omega$   $Z_o = 0.67 \text{ k}\Omega$ ]
29. Draw the small-signal equivalent circuit of a FET amplifier in CG connection and derive the equation for voltage gain, input impedance and output impedance.
30. In the CG amplifier of Fig. 6.44(b), let  $R_D = 4 \text{ k}\Omega$ ,  $R_s = 2 \text{ k}\Omega$ ,  $g_m = 2 \times 10^{-3} \text{ mho}$ ,  $r_d = 40 \text{ k}\Omega$ . Calculate  $A_V$ ,  $Z_i$  and  $Z_o$ . [Ans.  $A_V = 7.36$ ,  $Z_i = 0.4 \text{ k}\Omega$ ,  $Z_o = 4 \text{ k}\Omega$ ]

### OBJECTIVE-TYPE QUESTIONS

1. Y-parameters are otherwise called
  - (a) admittance parameter
  - (b) hybrid parameters
  - (c) impedance parameters
  - (d) reluctance parameters
2. The parameter  $h_1$  has the dimension of
  - (a)  $\Omega$
  - (b)  $\text{V}$
  - (c)  $\text{V}$
  - (d) dimensionless
3. The amplifier that gives unity voltage gain is
  - (a) common emitter
  - (b) common collector
  - (c) common base
  - (d) all the above
4. The amplifier that gives  $180^\circ$  voltage phase shift is
  - (a) common emitter
  - (b) common collector
  - (c) common base
  - (d) all the above
5. The amplifier that gives power gain approximately equal to current gain is
  - (a) common emitter
  - (b) common collector
  - (c) common base
  - (d) all the above
6. In a common-emitter amplifier having a small unbypassed emitter resistance ( $R_E$ ), the input resistance is approximately equal to
  - (a)  $R_E$
  - (b)  $h_{fe}$
  - (c)  $h_{fe} \cdot R_E$
  - (d)  $R_E/h_{fe}$
7. Which of the following transistor amplifiers has the highest voltage gain?
  - (a) Common-base
  - (b) Common-collector
  - (c) Common-emitter
  - (d) all of them
8. If the internal resistance of the ac signal source in an ac amplifier is larger, then its
  - (a) overall voltage gain is greater
  - (b) input impedance is greater
  - (c) current gain is smaller
  - (d) circuit voltage gain is smaller
9. In a single-stage amplifier, the voltage gain is increased when
  - (a) its ac load is decreased
  - (b) the load resistance is increased
  - (c) the emitter resistance  $R_E$  is increased
  - (d) the resistance of signal source is increased
10. The  $h$ -parameter is called hybrid parameter because it is
  - (a) different from  $y$ - and  $z$ -parameters
  - (b) mixed with other parameters
  - (c) applied to circuits contained in a box
  - (d) defined by using both open-circuit and short-circuit terminations
11. The input impedance  $h_{11}$  of a network with output shorted is expressed by
  - (a)  $v_1/i_1$
  - (b)  $v_1/v_2$
  - (c)  $i_2/i_1$
  - (d)  $i_1/v_2$
12. If the spacing between the curves of the output characteristics of a transistor is larger, then
  - (a) the value of  $h_{fe}$  is smaller
  - (b) the value of  $h_{fe}$  is larger
  - (c)  $h_{fe}$  is independent of the spacing

- (d)  $h_{fe}$  can increase or decrease depending upon the circuit configuration

**13.** A CMOS amplifier when compared to an  $N$ -channel MOSFET, has the advantage of
 
  - (a) higher cut-off frequency
  - (b) higher voltage gain
  - (c) higher current gain
  - (d) lower current drain from the power supply, thereby less dissipation

**14.** The distortion that produces new frequency components at the output of amplifier is
 
  - (a) frequency distortion
  - (b) harmonic distortion
  - (c) phase distortion
  - (d) delay distortion

**15.** Choose the correct match for input resistance of various amplifier configurations shown below:

<i>Configuration</i>	<i>Input resistance</i>
CB: Common Base	LO: low
CC: Common Collector	MO: Moderate
CE: Common Emitter	HI: High
(a) CB-LO, CC-MO, CE-Hi	(b) CB-LO, CC-HI, CE-MO
(c) CB-MO, CC-HI, CE-LO	(d) CB-HI, CC-LO, CE-MO

**16.** A bipolar transistor is operating in the active region with a collector current of 1 mA. Assuming that the  $\beta$  of the transistor is 100 and the thermal voltage ( $V_T$ ) is the transconductance ( $g_m$ ) and the input resistance ( $r_\pi$ ) of the transistor in the common-emitter configuration are

  - (a)  $g_m = 25 \frac{mA}{V}$  and  $r_\pi = 15.625 \text{ k}\Omega$
  - (b)  $g_m = 40 \frac{mA}{V}$  and  $r_\pi = 4.0 \text{ k}\Omega$
  - (c)  $g_m = 25 \frac{mA}{V}$  and  $r_\pi = 2.5 \text{ k}\Omega$
  - (d)  $g_m = 40 \frac{mA}{V}$  and  $r_\pi = 2.5 \text{ k}\Omega$

**17.** In a CS amplifier with diode connected load, the input-output characteristics is relatively
 
  - (a) zero
  - (b) constant
  - (c) non linear
  - (d) linear

**18.** The voltage gain of the CS amplifier if  $R_D = 4 \text{ k}\Omega$ ,  $\mu = 40$  and  $r_d = 40 \text{ k}\Omega$  is
 
  - (a) -3.64
  - (b) 0.66
  - (c) -0.66
  - (d) 1.66

**19.** The voltage gain of a given common-source JFET amplifier does not depend on its
 
  - (a) input impedance
  - (b) amplification factor
  - (c) dynamic drain resistance
  - (d) drain load resistance

**20.** The voltage gain in CD amplifier depends on
 
  - (a)  $g_m$  and  $R_D$
  - (b)  $g_m$  and  $R_s$
  - (c)  $g_m$
  - (d)  $R_D$



# appendix A

## Probable Values of General Physical Constants

Constant	Symbol	Value
Electronic charge	q	$1.602 \times 10^{-19}$ C
1 electron volt	eV	$1.602 \times 10^{-19}$ Joules
Electronic mass	m	$9.109 \times 10^{-31}$ kg
Ratio of charge to mass of an electron	q/m	$1.759 \times 10^{11}$ C/kg
Planck's constant	h	$6.626 \times 10^{-34}$ J-s
Boltzmann constant	k	$8.620 \times 10^{-5}$ eV/°K
Velocity of light	c	$2.998 \times 10^8$ m/s
Acceleration of gravity	g	$9.807$ m/s <sup>2</sup>
Permeability of free space	$\mu_0$	$1.257 \times 10^{-6}$ H/m
Permittivity of free space	$\epsilon_0$	$8.854 \times 10^{-12}$ F/m
1 joule	J	$6.25 \times 10^{18}$ eV



# Conversion Factors and Prefixes

Constant	Value
1 ampere (A)	1 C/s
1 angstrom unit ( $\text{\AA}$ )	$10^{-10} \text{ m} = 10^{-8} \text{ cm}$
1 coulomb (C)	1 A-s
1 farad (F)	1 C/V
1 henry (H)	1 V-s/A
1 hertz (Hz)	1 cycle/s
1 lumen	0.0016 W (at 0.55 $\mu$ m)
1 mil	$10^{-3}$ inch = 25 $\mu$ m
1 micron	$1 \mu \text{ m} = 10^{-6} \text{ m}$
1 newton (N)	1 kg = m/s <sup>2</sup>
1 Volt (V)	1 W/A
1 watt (W)	1 J/s
1 weber (Wb)	1 V-s
1 weber per square meter (Wb/m <sup>2</sup> )	$10^4$ gauss
1 tesla (T)	1 Wb/m <sup>2</sup>



# Previous Years' Solved JNTU Examination Questions

1. Find the concentration of holes and electrons in a P-type germanium at 300K, if the conductivity is  $100 \Omega\text{-cm}$ , and mobility of holes in germanium,  $\mu_p = 1800 \text{ cm}^2/\text{V}\text{-sec}$ . **(May/June 2017)**

**Solution** Given  $\sigma = 100 \Omega\text{-cm}$ ,  $T = 300\text{K}$ ,  $\mu_p = 1800 \text{ cm}^2/\text{V}\text{-sec}$ , and  $n_i = 2.5 \times 10^{19} \text{ m}^{-3}$

We know that the conductivity of P-type silicon is  $\sigma = qp\mu_p$ .

$$\text{Hence, concentration of holes is } p = \frac{\sigma}{q\mu_p} = \frac{100}{(1.602 \times 10^{-19})(1800)} = 3.4678 \times 10^{17} \text{ cm}^{-3}$$

$$\text{Concentration of electrons is } n = \frac{n_i^2}{p} = \frac{(2.5 \times 10^{19} \times 10^{-6})^2}{3.4678 \times 10^{17}} = 1.8023 \times 10^7 \text{ cm}^{-3}$$

2. What is the ratio of the current for a forward bias of 0.05V to the current for the same magnitude of reverse bias for a germanium diode? And what are the observations? **(May/June 2017)**

**Solution** Given  $V = 0.05 \text{ V}$  and  $\eta = 1$

The diode current with forward bias is

$$I_F = I_0 \left[ e^{\left(\frac{V}{\eta V_T}\right)} - 1 \right]$$

The diode current with reverse bias is

$$I_R = I_0 \left[ e^{\left(\frac{-V}{\eta V_T}\right)} - 1 \right]$$

The ratio of current for a forward bias to the current for reverse bias is

$$\frac{I_F}{I_R} = \frac{I_0 \left[ e^{\left(\frac{V}{\eta V_T}\right)} - 1 \right]}{I_0 \left[ e^{\left(\frac{-V}{\eta V_T}\right)} - 1 \right]}$$

Simplifying, we get

$$\frac{I_F}{I_R} = -e^{\frac{V}{\eta V_T}}$$

Substituting the given values in above equation, we get

$$\frac{I_F}{I_R} = -e^{\frac{0.05}{1 \times 26 \times 10^{-3}}} = -6.842$$

Therefore,

$$I_F = -6.842 \times I_R$$

The minus sign denotes the opposite direction of forward current to the reverse current.

Magnitude of forward current is 6.842 times the reverse current.

3. A diode whose internal resistance is  $20 \Omega$  is to supply power to a  $100 \Omega$  load from  $110V$  (rms) source of supply. Calculate (i) peak load current (ii) dc load current (iii) ac load current and (iv) % regulation from no load to given load. **(May/June 2017)**

**Solution** Given  $R_{in} = 20 \Omega$ ,  $R_L = 100 \Omega$ ,  $V_{rms} = 110 V$

- (i) To determine the peak load current:

$$V_{rms} = I_{rms} \times R_L$$

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{110}{100} = 1.1 A$$

$$I_m = \sqrt{2} I_{rms} = 1.55 A$$

- (ii) To determine the dc load current:

$$\text{Voltage across the load, } V_{dc} = \frac{2V_m}{\pi}$$

$$\text{where } V_m = \sqrt{2} V_{rms} = \sqrt{2} \times 110$$

$$\text{Therefore, } V_{dc} = \frac{2 \times \sqrt{2} \times 110}{\pi} = 99.034 V$$

$$\text{Hence, the dc load current, } I_{dc} = \frac{V_{dc}}{R_L} = \frac{99.034}{100} = 0.99034 A$$

- (iii) To determine the ac load current:

$$I_{ac} = I_m \cos \omega t = 1.55 \cos \omega t$$

$$(iv) \text{ Percentage of regulation} = \frac{V_{FL} - V_{NL}}{V_{FL}} \times 100 = \frac{\frac{V_{dc} - V_m}{\pi}}{\frac{V_{dc}}{\pi}} \times 100 = \frac{99.034 - 49.52}{99.034} \times 100 = 50\%$$

4. Determine the value of the base current of a CB configuration whose current amplification factor is 0.92 and emitter current is 1 mA. (May/June 2017)

**Solution** Given  $I_E = 1$  mA,  $\alpha = 0.92$

$$\text{Current amplification factor, } \alpha = \frac{I_C}{I_E}$$

Therefore, the collector current is

$$I_C = I_E \times 0.92 = 1 \times 10^{-3} \times 0.92 = 0.92 \text{ mA}$$

$$I_B = I_E - I_C = 1 \times 10^{-3} - 0.92 \times 10^{-3} = 80 \mu\text{A}$$

5. Find the concentrations of holes and electrons in a P-type silicon at 300°K. Assume resistivity as 0.02 Ω-cm,  $\mu_p = 475 \text{ m}^2/\text{V-sec}$ , and  $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$ . (Oct/Nov 2017)

**Solution** Given  $T = 300^\circ\text{K}$ ,  $\mu_p = 475 \text{ m}^2/\text{V-sec}$ ,  $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$ ,  $\rho = 0.02 \Omega\text{-cm}$  and  $\mu_p = 475 \times 10^4 \text{ cm}^2/\text{V-sec}$ .

$$\text{Conductivity, } \sigma = \frac{1}{\rho} = \frac{1}{0.02 \Omega} = 50 \text{ mho-cm}$$

$$\text{Also, conductivity } \sigma = qp\mu_p$$

$$\text{Concentration of holes, } p = \frac{\sigma}{q\mu_p} = \frac{50}{(1.602 \times 10^{-19})(475 \times 10^4)} = 6.570 \times 10^{13} \text{ cm}^{-3}$$

$$\text{Concentration of electrons, } n = \frac{n_i^2}{p} = \frac{(1.45 \times 10^{10})^2}{6.570 \times 10^{13}} = 3.2 \times 10^6 \text{ cm}^{-3}$$

6. The energy gap of Si is 1.1 eV. Its electron and hole mobilities at room temperatures are 0.15 and 0.06  $\text{m}^2/\text{V-sec}$  respectively. Evaluate its conductivity. (Oct/Nov 2017)

**Solution** Given the energy gap  $E_g$  of Si = 1.1 eV

$$\mu_n = 0.15 \times 10^4 \text{ cm}^2/\text{V-sec}$$

$$\mu_p = 0.06 \times 10^4 \text{ cm}^2/\text{V-sec}$$

The intrinsic concentration of silicon at room temperature is  $n_i = 1.38 \times 10^{10} \text{ cm}^{-3}$ .

$$\begin{aligned} \text{Conductivity, } \sigma &= qn_i(\mu_n + \mu_p) = 1.602 \times 10^{-19} \times 1.38 \times 10^{10} (0.15 + 0.06) \times 10^4 \\ &= 4.642 \times 10^{-6} \text{ mho-cm} \end{aligned}$$

7. A sinusoidal voltage whose  $V_m = 24$  V is applied to half-wave rectifier. The diode may be considered to be ideal and  $R_L = 1.8 \text{ k}\Omega$  is connected as load. Find the peak value of current, rms value of current, dc value of current and ripple factor. (Oct/Nov 2017)

**Solution** Given  $V_m = 24$  V and  $R_L = 1.8 \text{ k}\Omega$

$$\text{We know that, } V_{dc} = \frac{V_m}{\pi} = \frac{24}{\pi} = 7.639 \text{ V}$$

$$\text{Therefore, the dc current, } I_{dc} = \frac{V_{dc}}{R_L} = \frac{7.639}{1.8K} = 4.243 \text{ mA}$$

Peak value of current,  $I_m = I_{dc} \times \pi = 4.243 \times 10^{-3} \times \pi = 13.33 \text{ mA}$

For HWR, the rms value of current is  $I_{rms} = \frac{I_m}{2} = \frac{13.33 \times 10^{-3}}{2} = 6.67 \text{ mA}$

Ripple factor is

$$\Gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = \sqrt{\left[\frac{\frac{V_m}{2}}{\frac{V_m}{\pi}}\right]^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21$$

8. The reverse saturation current of the Ge transistor is  $2 \mu\text{A}$  at room temperature of  $25^\circ\text{C}$  and increases by a factor of 2 for each temperature increase of  $10^\circ\text{C}$ . Find the saturation current of the transistor at a temperature of  $75^\circ\text{C}$ . (Oct/Nov 2017)

**Solution** Given:  $I_{01} = 2 \mu\text{A}$  at  $T_1 = 25^\circ\text{C}$

Therefore, the reverse saturation current of the transistor at  $T_2 = 75^\circ\text{C}$  is

$$I_{02} = I_{01} \times 2^{\left(\frac{T_2-T_1}{10}\right)} = 2 \times 10^{-6} \times 2^{\left(\frac{75-25}{10}\right)} = 64 \mu\text{A}$$

9. Design a collector to base bias circuit for the specified conditions:  $V_{CC} = 15 \text{ V}$ ,  $V_{CE} = 5 \text{ V}$ ,  $I_{CE} = 5 \text{ mA}$  and  $\beta = 100$ . (Oct/Nov 2017)

**Solution** Given  $V_{CC} = 15 \text{ V}$ ,  $V_{CE} = 5 \text{ V}$ ,  $I_{CE} = 5 \text{ mA}$  and  $\beta = 100$ .

Input loop equation of this circuit is

$$V_{CC} = (I_B + I_C)R_C + I_B R_B + V_{BE}$$

Simplifying the above equation, we get

$$R_B = \frac{V_{CC} - V_{BE} - R_C(I_B + I_C)}{I_B}$$

Base current,  $I_B = \frac{I_C}{\beta} = \frac{5 \times 10^{-3} \text{ mA}}{100} = 50 \mu\text{A}$

Output loop equation is

$$V_{CC} = (I_B + I_C)R_C + V_{CE}$$

Therefore,  $R_C = \frac{V_{CC} - V_{CE}}{I_B + I_C} = \frac{15 - 5}{5 \times 10^{-3} + 50 \times 10^{-6}} = \frac{10}{5.05 \times 10^{-3}} = 1.98 \text{ k}\Omega$

We know that,  $R_B = \frac{V_{CC} - V_{BE} - R_C(I_B + I_C)}{I_B}$

Substituting  $I_B$  and given values in the above equation, we get

$$R_B = \frac{15 - 0.7 - 1.98 \times 10^3 (50 \times 10^{-6} + 5 \times 10^{-3})}{50 \times 10^{-6}} = 86.02 \text{ k}\Omega$$