Reg. No.	RA2011004010051

B.Tech. DEGREE EXAMINATION, MAY 2023

OPEN BOOK EXAMINATION

Sixth Semester

18ECC206J – VLSI DESIGN

(For the candidates admitted from the academic year 2018-2019 to 2021-2022)

- Specific approved THREE text books (Printed or photocopy) recommended for the course
- Handwritten class notes (certified by the faculty handling the course / head of the department)

Time: 3 Hours | Max. Marks: 100

Answer **FIVE** questions

(Question No 1 is compulsory)

		Marks	BL	CO	PO
1.a.i.	Design a Moore FSM model to detect the binary sequence "1011" in the input string. Write a Verilog HDL behavioral modeling and test bench to verify it.	9	2	1	3
ii.	Implement the Boolean function. $F_1 = \sum m(1,2,4,7)$; $F_2 = \sum m(3,5,6,7)$ using suitable multiplexer. Multiplexer must be implemented in CMOS transmission gate logic in Verilog switch level model. Boolean function implementation in gate-level modeling.	9	3	1	2
b.	The statement that supports UDP is (A) UDP can be defined inside modules (B) UDP can be instantiated inside modules (C) UDP supports in out ports (D) UDP can take both scalar and vector parts	1	1	1	2

c.	For the code segment given below
	always @(posedge clk)
	a=b;
	always @ (posedge clk)
	b=a;
	(A) Values of a and b are swapped (B) Values of a and b can be swapped depending on simulator
	(C) Values of a and b cannot be swapped (D) Cannot determine
		1	1	1	2

2.a.i.	Implement a 4-bit adder/subtractor architecture in a Verilog gate-level modeling. Write a related test bench program to check the functionality of the circuit.	9	3	1	5
ii.	Define user defined primitive (UDP) in Verilog modeling. Justify the role of UDP modeling in Verilog by design a positive edge-sensitive sequential UDP for a D-flip flop.	9	2	1	3

b. For the code segment choose the right answer, if a is 1'bx (or) 1'bz

1 1 1 2

```
reg a;
case x(a)
1'b0 : statement1;
1'b1 : statement2;
1'bx : statement3;
1'bz : statement4;
end case
```

(A) Statement 1 is executed
(B) Procedural continuous assignment
(C) Blocking assignment
(D) Non-blocking assignment

c. If $A = 1'b1,\ B = 2'b11, C = 3'b010$ then $Y = \{A, B[1], C[2]\}$ equals

1 1 1 2

(A) $3'b110$
(B) $4'b0110$
(C) $3'b111$
(D) $1'b0$

3.a.i. For a PMOS capacitor of area 100 μm × 100 μm operated at T=300 K, with $\phi_m = 5.2eV$, $x_0 = 3nm$ and $N_D = 10^{17} cm^{-3}$. Determine

9 3 2 2

(i) Threshold voltage (V_T)
(ii) Maximum small-signal capacitance
(iii) Minimum small-signal capacitance
(iv) Number of donor atom to be added to shift V_t more negative from $-0.327V$ to $-0.3V$.

ii. Determine the drain current expression in a MOS transistor, considering its major region of operation. Also derive the derivation of threshold voltage of a MOS device.

9 2 2 3

b. The low voltage on the gate of P-MOSFET forms

1 1 2 3

(A) Channel of negative carriers
(B) Channel is not formed
(C) Channel is clipped
(D) Channel of positive carriers

c. Consider a MOS structure with equilibrium FERMI potential of the doped silicon substrate is 0.3 eV. Electron affinity of Si is 4.15 eV and metal is 4.1eV. Find the built-in potential of the MOS system.

1 1 2 3

(A) –0.8 eV
(B) 0.8 eV
(C) 0.9 eV
(D) –0.9 eV

4.a.i. Define scaling in MOS transistor and its significant type with an illustration. Also demonstrate that for a long-channel transistor, full-voltage scaling results in a reduction of the intrinsic delay with a factor S^2, while increasing the power dissipation/device by S.

9 2 3 1

ii. Explain with necessary derivation the DC transfer characteristics of CMOS inverter in detail.

9 2 4 3

b. If $\beta_n = \beta_p$ in a CMOS inverter, then $V_{\tau n}$ is equal to _____.

1 1 4 2

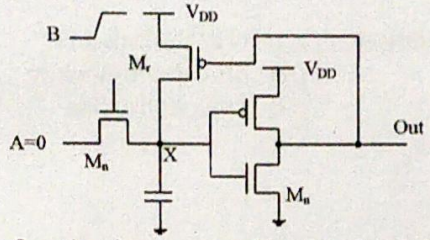
(A) V_{dd}
(B) V_{ss}
(C) $0.5V_{dd}$
(D) $2V_{dd}$

c. The number of transistor for implementing a 2-input XOR CMOS logic is _____. 1 1 4 2

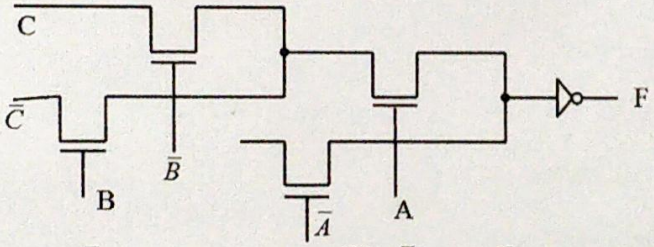
(A) 5 (B) 10
(C) 8 (D) 9

5.a.i. Implement the Boolean function $F = \overline{AB + CD + E(F+G)}$ in a static CMOS logic, dynamic and domino CMOS logic. Do performance analysis on each style of implementation and suggest the efficient implementation. 9 3 4 2

ii. For the circuit shown below, assume that the pull-down device consists of 6 pass transistor in series with a device size of 0.5 μm/0.25 μm (replacing transistor M_n). Determine the maximum W/L size for the level restorer transistor for correct functionality. 9 3 4 2



b. _____ is the function implemented by the circuit below. 1 1 4 3



(A) $A + BC + B\bar{C}$ (B) $\bar{A} + BC + \bar{B}C$
(C) $\bar{A} + BC + \bar{B}\bar{C}$ (D) $A + \bar{B}\bar{C} + B\bar{C}$

c. In a body effect, substrate is biased with respect to _____ 1 1 4 2

(A) Drain (B) Source
(C) Gate (D) V_{SS}

6.a.i. Explain the dynamic and static power consumption in a typical CMOS logic design. Also illustrate with an example and mathematical derivation how transistor sizing supports energy minimization. 9 2 5 3

ii. Design a two input XOR, XNOR and NAND logic in pass transistor logic (PTL), complementary PTC and differential cascaded voltage switch logic (DCVSL). Perform analysis in terms of transistor count and voltage transfer characteristics for each logic. 9 3 5 2

b. How many transistor might bring up latch up effect in P-well structure? 1 1 5 2

(A) Two (B) Three
(C) One (D) Four

c.	Velocity of charged particle in a MOS transistor is _____ (A) μ / V_{ds} (B) μ / E_{ds} (C) $\mu * E_{ds}$ (D) E_{ds} / μ	1	1	3	1
7.a.i.	Discuss in detail the design strategies to reduce RC delays in the interconnect used for CMOS logic design. Also optimize the interconnect architecture to reduce propagation delay.	9	2	6	3
ii.	Explain with a neat sketch the fabrication techniques in a silicon on insulator to avoid latch-up effect in a CMOS fabrication.	9	2	6	2
b.	The photoresist layer is exposed to _____ (A) Visible light (B) Ultraviolet light (C) Infrared light (D) LED	1	1	6	2
c.	The commonly used bulk substrate in a nMOS fabrication is _____ (A) Silicon crystal (B) Silicon-on-sapphire (C) Phosphorous (D) Silicon-di-oxide	1	1	5	2

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