A transceiver consists of a receiver and a transmitter. The architecture and key characteristics of different types of receivers and transmitters are covered in this notes

1. Main analog components for receivers
   - *amplifiers*
   - *filters*
   - *mixers*
   - *oscillators*
2. Receiver architectures and their properties
   - *superheterodyne principle*
   - *direct conversion*
     - *DC offsets as a challenging problem*
   - *low IF, Weaver*
   - *effects of I/Q imbalance*
3. Non-idealities and performance meatrics of the analog front-end modules
   - *sensitivity, dynamic range*
   - *noise figure*
   - *intermodulation distortion, IP3*
   - *system calculation principles*
   - *leakage, spurious frequencies*
   - *phase noise*

Super-heterodyne Receiver

In 1917, Armstrong invented a further receiver principle, which is still used for a majority of wireless systems. It is the super-heterodyne topology as illustrated in

The signal is received by the antenna, coarse filtered by a bandpass filter, amplified by an LNA and converted down to an intermediate frequency (IF) by means of a mixer fed by a local oscillator (LO) signal. The demanding channel filter is employed at IF frequency, followed by an analogue to digital converter and a digital signal processor performing the demodulation and the data decoding. As

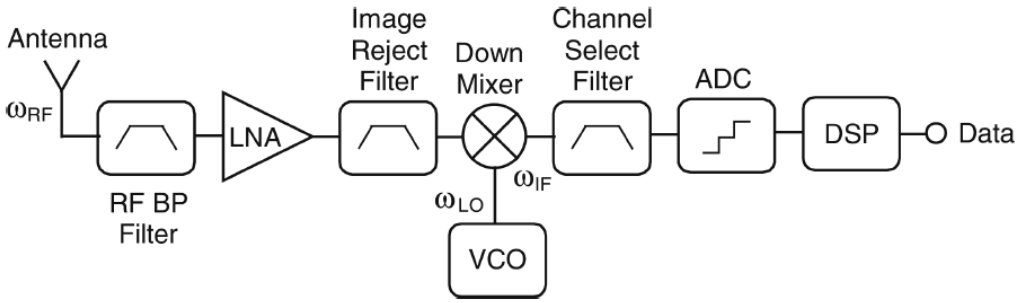


Fig. 2.2. Simplified architecture of the super-heterodyne receiver with single down-conversion, BP: Bandpass, LNA: Low Noise Amplifier, VCO: Voltage Controlled Oscillator, ADC: Analogue Digital Converter, DSP: Digital Signal Processor

illustrated in Fig. 2.4. Two different IF frequencies are used. Image rejection is carried out at high IF, whereas channel selection is accomplished at low IF, thereby relaxing the requirements for both filters simultaneously. A constant frequency can be used for the demanding first VCO. Frequency tuning can be performed by the second VCO operating at lower frequency. Unfortunately, two mixers and two oscillators are required increasing the circuit complexity, power consumption and costs.

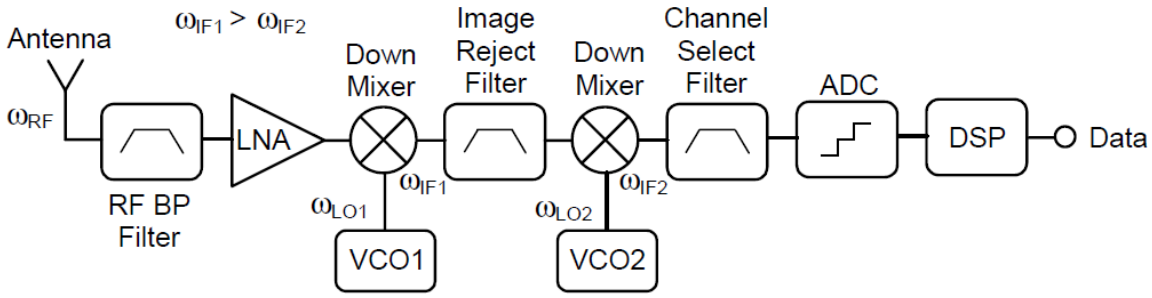


Fig. 2.4. Simplified architecture of super-heterodyne receiver with double down-conversion

2.1.4 Direct Conversion Receiver

The motivation of increased integration has led to the direct conversion receiver, which is also referred to as homodyne or zero-IF approach [Raz97, Zha03]. The idea is to translate the RF signal directly to zero-IF frequency thereby exhibiting the following advantages. First, the channel filtering can be performed by a lowpass filter. Recall that a more complex bandpass filter is necessary for the superheterodyne receiver. Second, the IF frequency of zero eliminates the image problem. Hence, no external high-Q image reject filter is required making fully integrated solutions feasible.

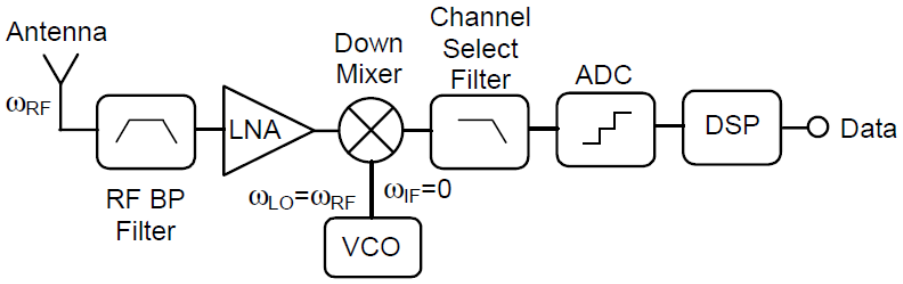


Fig. 2.6. Illustration of zero-IF approach

In Fig. 2.6, a simple direct conversion architecture is illustrated, which can be used for processing of amplitude modulated signals featuring the same information at the two sidebands allocated around the carrier frequency. For more sophisticated frequency and phase modulations schemes, the information within the two sidebands can be different. However, after conversion around DC, these sidebands can't be separated leading to a loss of information. This can be prevented by using quadrature mixing with in-phase (I) and quadrature (Q) signals as illustrated in Fig. 2.7. Consequently, the information of both sidebands can be preserved allowing efficient modulation schemes.

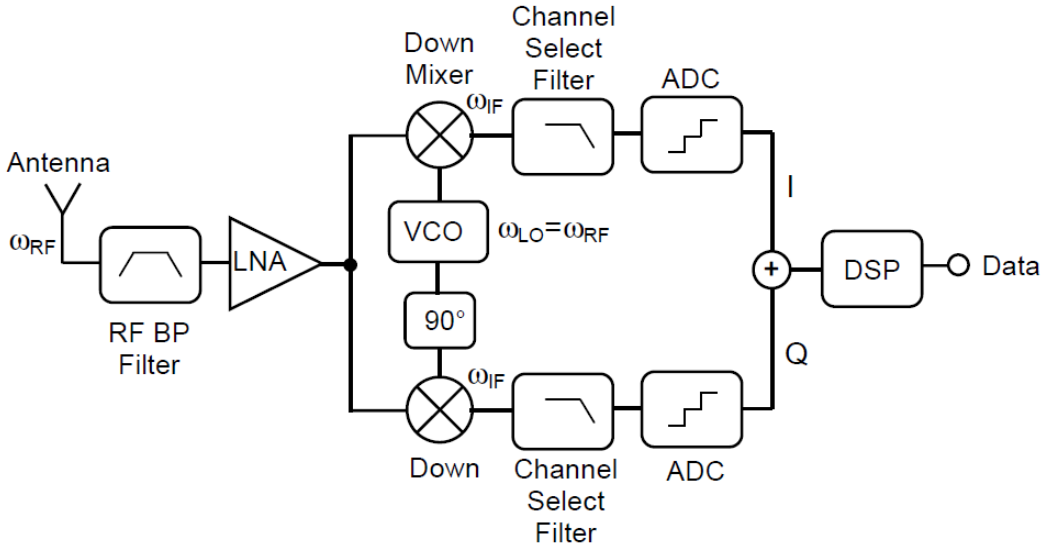


Fig. 2.7. Illustration of the zero IF approach with I/Q quadrature mixing

2.1.6 Digital-IF Receiver

To make systems more flexible, as much signal processing as possible is transferred into the digital domain. Figure 2.8 depicts a realisation of a digital-IF receiver. The idea is to perform the demanding channel filtering completely in the digital domain. Thus, the requirements for the RF filters are relaxed. Simple RF filters may be employed for coarse band selection. The major advantage is the flexibility of the architecture. The receiver can be reconfigured for a variety of systems with different modulation types, channel frequencies and bandwidths meeting the demands of different standards. Moreover, the digital approach avoids the phase and amplitude mismatch problems of analogue I/Q signals. Generally, the impact of process tolerances is less significant.

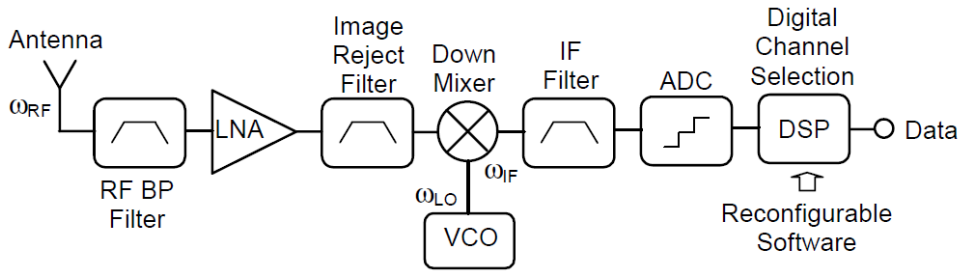
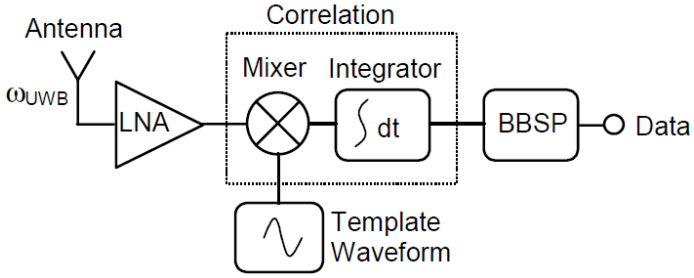


Fig. 2.8. Simplified digital-IF receiver

2.1.7 Impulse Radio Receiver

In recent years, impulse based radios receive a revival due to its promising properties for short range, low power and high speed applications [Por03, Uwb06, Weis04, Paq04, Opp04, Zas03, Sto04, Bar06, Ba206]. In the USA, corresponding UWB (Ultra-Wideband) standards have already been published by the FCC (Federal Communications Commission) [Fcc02], whereas in Europe the community is still waiting for adequate standards. A complete UWB chip set is already available



ole of top-level schematics of impulse radio receiver, BBSP:

Table 2.1. Comparison of receiver architectures

Architecture	Complexity	Full integration	Power cons.	Comments	
Super-regenerative	Low	Possible	Very low	No carrier, impulse with wide bandwidth can cause interferences with other systems if emitted power not limited	High sensitivity because of resonant feedback
Impulse radio					High bandwidth of 3.11–10.6 GHz allows high data rates
Super-heterodyne	Moderate	Off-chip image reject and channel select filter required	Moderate	IF has to be traded off for image rejection and channel selection	
Dual super-heterodyne	High		High	Good image rejection and channel selection possible	
Direct conversion	Low	Possible	Low	DC offsets can significantly degrade the performance, sensitive to flicker noise	
Low-IF	Low/moderate	Possible	Low/moderate	Good overall performance	
Digital-IF	RF: very low Baseband: very high	Possible	Very high	Very flexible architecture, can handle different standards, modulation and frequencies, ADC limits dynamic range which is a major drawback	

2.2.1 Direct Conversion Transmitter

Figure 2.11 illustrates the principle of a direct conversion architecture. The baseband signal is up-converted to RF, bandpass filtered, amplified and lowpass filtered before the signal is emitted by the antenna. The direct up-conversion architecture suffers from the so called injection pulling, where a part of the strong power amplifier signal is coupled back to the oscillator operating at the same RF frequency. Thus, undesired DC components are generated. Reasons for the coupling are the non-ideal substrate isolation and reflections at the component interfaces.

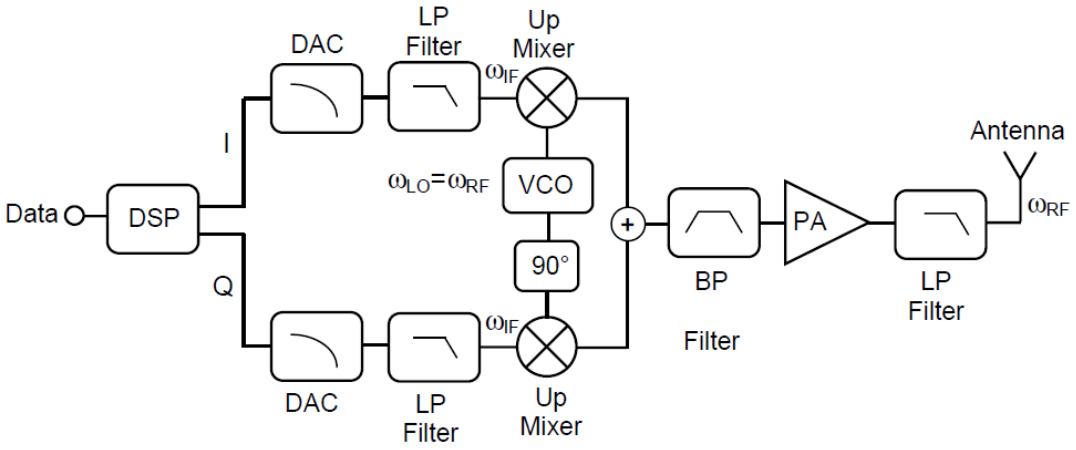


Fig. 2.11. Architecture of direct conversion transmitter, PA: Power Amplifier, DAC: Digital Analogue Converter

2.2.2 Direct Modulation Transmitter

A typical architecture of a direct modulation transmitter is illustrated in Fig. 2.13. The baseband signal is modulated and up-converted in one single step. By means of the frequency control voltage, the VCO is modulated by the applied data. Subsequently, the signal is amplified, low pass filtered and emitted via antenna. Amplitude modulated signals can't be transmitted since the VCO is always in saturation. The architecture is well suited for frequency and phase modulations. Among the advantages of this approach are the low complexity, the increased ability for integration and the low power consumption.

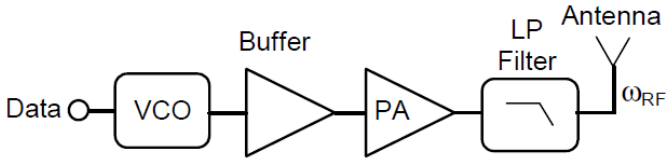


Fig. 2.13. Architecture of direct modulation transmitter

2.2.3 Impulse Radio Transmitter

In Fig. 2.14, the simple architecture of an impulse radio transmitter is illustrated consisting of a pulse generator, a timing circuit and a clock oscillator [Opp05]. PPM is used for data modulation. A programmable delay circuit can be employed to determine the timing. The desired waveform is produced by the pulse generator, while the clock oscillator defines the pulse repetition frequency. Step, Gaussian or monocycle pulses are suited for UWB communication since they have a broadband frequency spectrum.

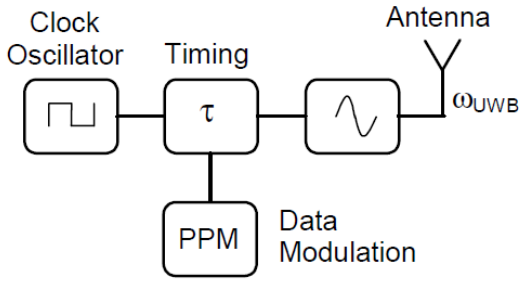


Fig. 2.14. Example of top-level schematics of impulse radio transmitter

Table 2.2. Comparison of transmitter architectures

Architecture	Complexity	Full integration	Power consumption	Comments
Direct conversion	Low	Possible since no sophisticated filters are required. However technology must be capable of providing enough output power	Similar since major power drawn by PA, offset approaches slightly higher	Sensitive to injection pulling
Offset direct conversion	Moderate			Injection pulling alleviated
Direct modulation	Very low			Modulation can be corrupted by frequency variations
Impulse radio	Very low		Very low since output power restricted due to potential for interferences with other standards	High bandwidth allows high data range at low coverage range

2.3 Transceiver Example

Obviously, transceivers consist of both a receiver and a transmitter. Figure 2.15 depicts a simple super-heterodyne transceiver. In many cases, a transceiver needs only one multifunctional VCO since it may be used for both the receiver and transmitter. This holds also for the antenna. SPDT (Single Pole Double Throw) switches can be employed to change between the receive- and transmit- modes. Drawback of these switches is the additional losses of around 0.5–2 dB, which directly add to the overall noise figure in the receiver and reduce the effective PA power. However, the benefit regarding the saved space and costs with respect to a second antenna may be considerable. For detailed information concerning switches, the reader is referred to Sect. 13.1.

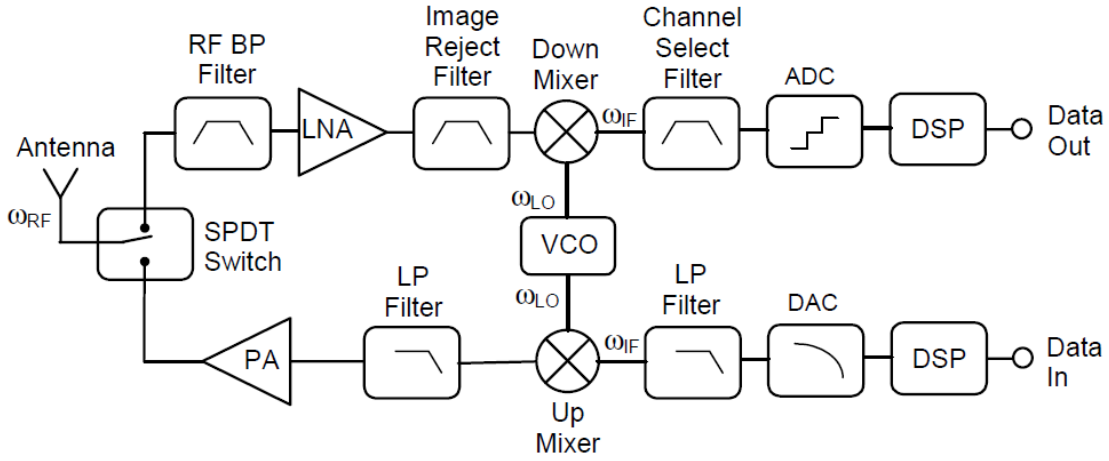


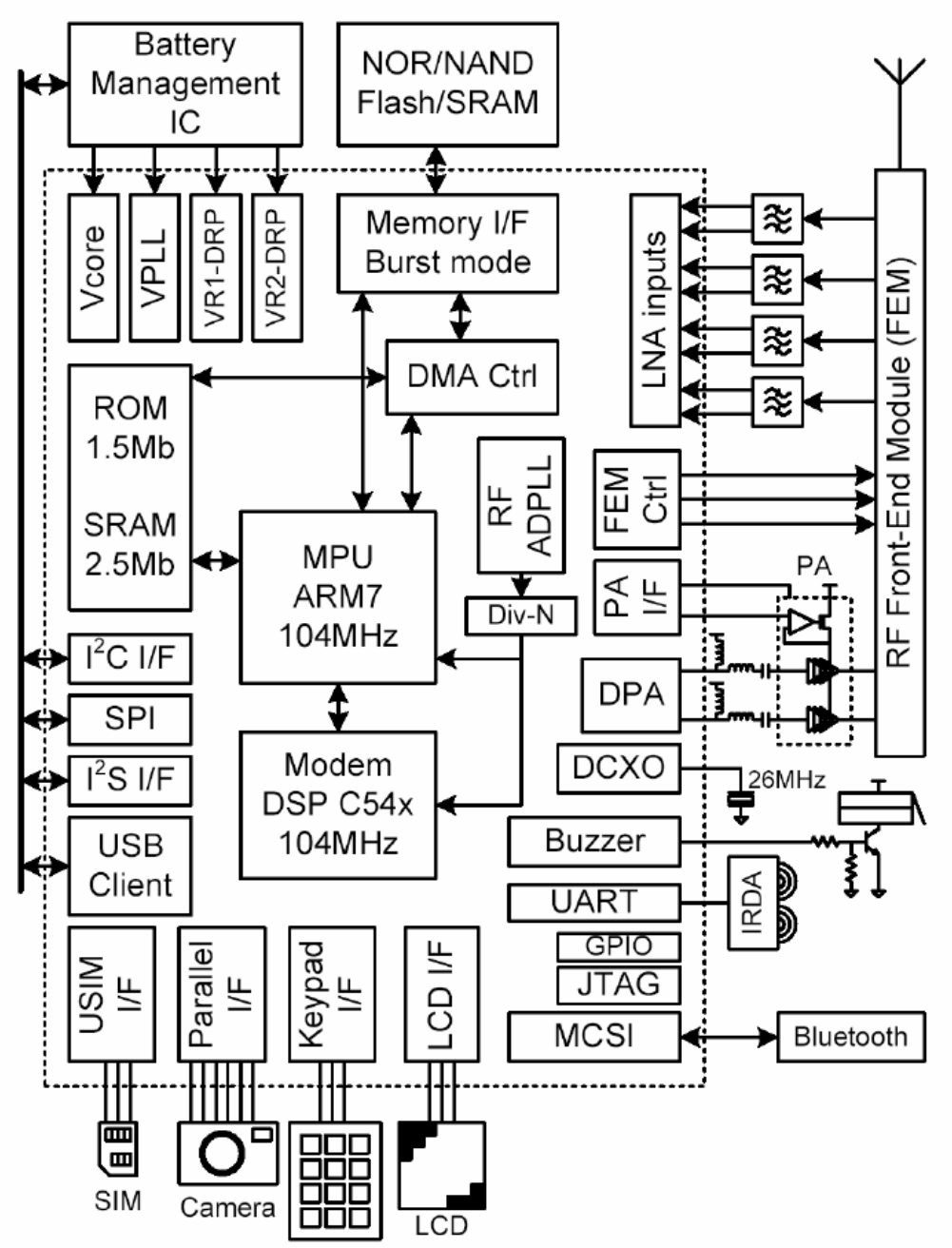
Fig. 2.15. Transceiver architecture of super-heterodyne transceiver, SPDT: Single Pole Double Throw

3.2.1 Superheterodyning Architecture

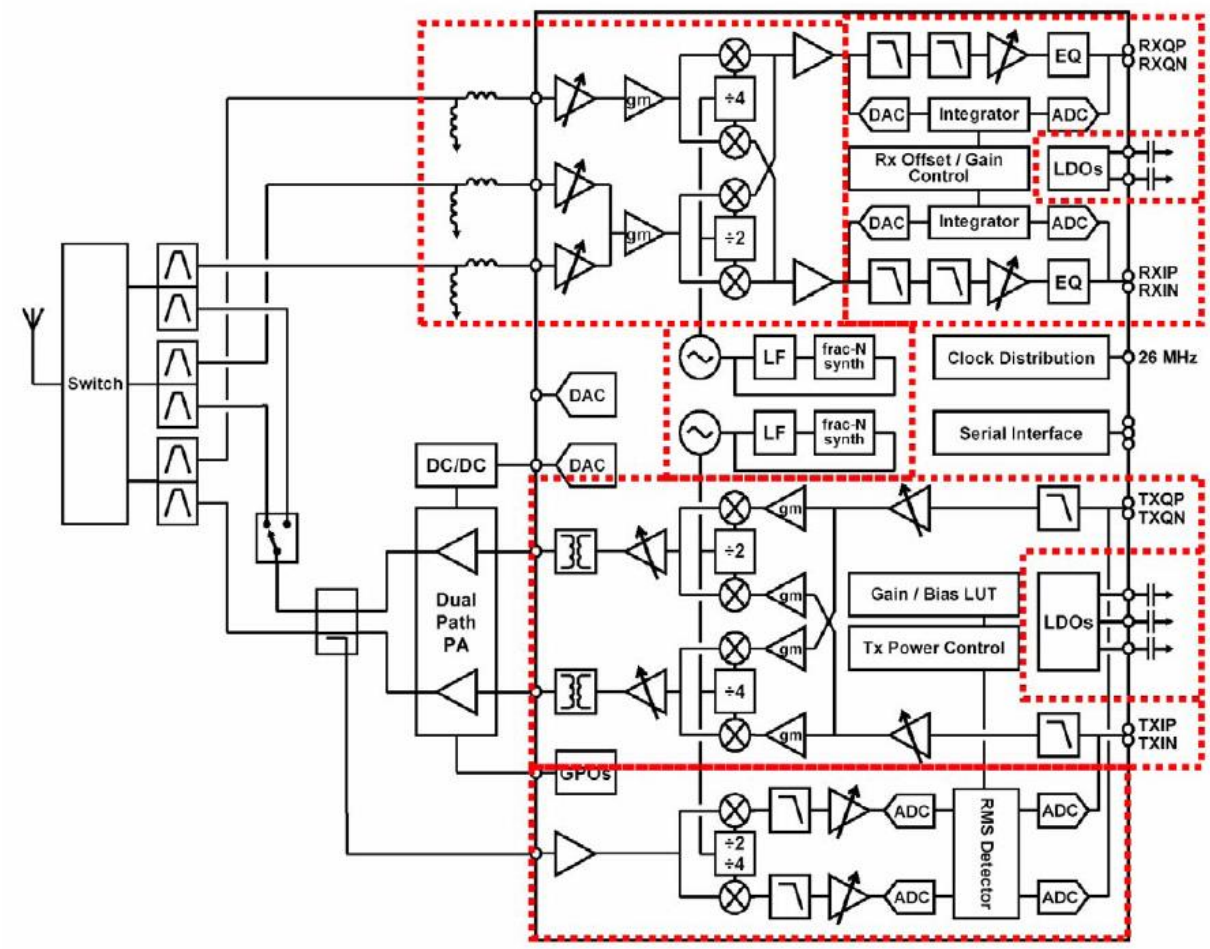
Let us consider a simple architecture as depicted in Figure 3.3(a). This figure shows a basic 60 GHz RF front-end architecture for application at a portable station (PS). Ideally, it should be an integrated on-chip solution consisting of a receiving branch, a transmitting branch, and a frequency generation function. The receiving branch consists of the receiving antenna, a low noise amplifier, and a mixer that down converts the signal from millimeter wave range to intermediate frequency (IF) range. The transmitting branch consists of a mixer, a power amplifier (PA), and the transmitting antenna. The antennas are (integrated) patch antennas. The mixers are image rejecting mixers. They need not to be in-phase/quadrature (IQ) mixers. The IF in this example is considered to be 5 GHz, with the idea that, with appropriate modifications, an IEEE 802.11a RF chip set can serve as the IF to allow dual mode operation and interoperability. A superheterodyning architecture requires more components and more DC power, so it is not preferred for mobile devices.

A radio receiver generally includes an antenna section filter, a low noise amplifier, a down conversion mixer, an intermediate frequency stage, and a demodulator. In

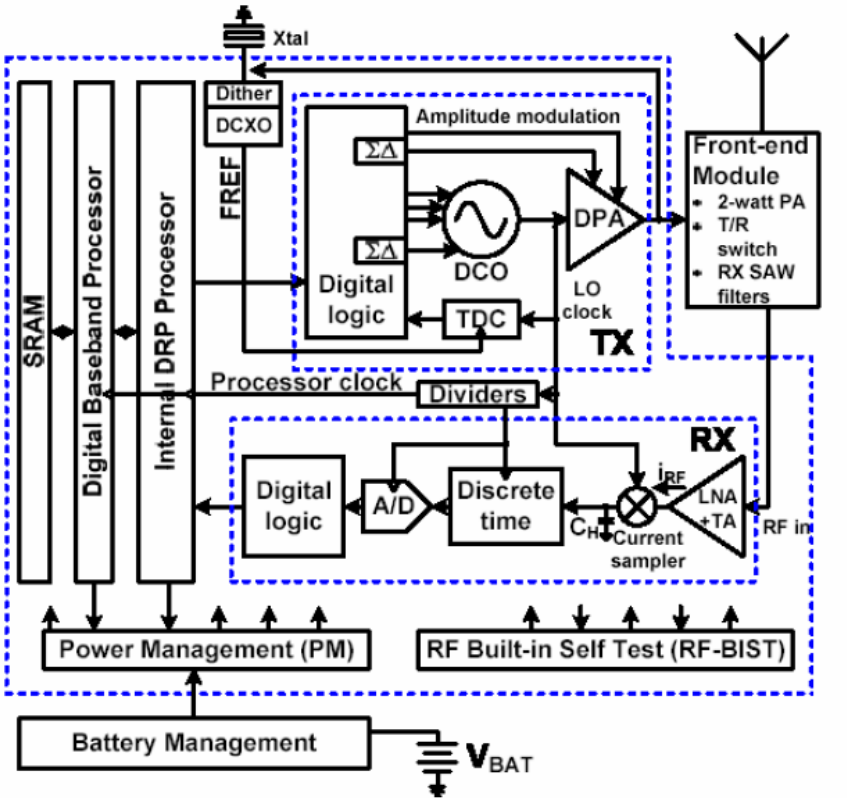
2. Quad-Band GSM Transceiver



1. Tri-Band WDMA Transceiver: 900 MHz, 2 GHz, 2.5 GHz

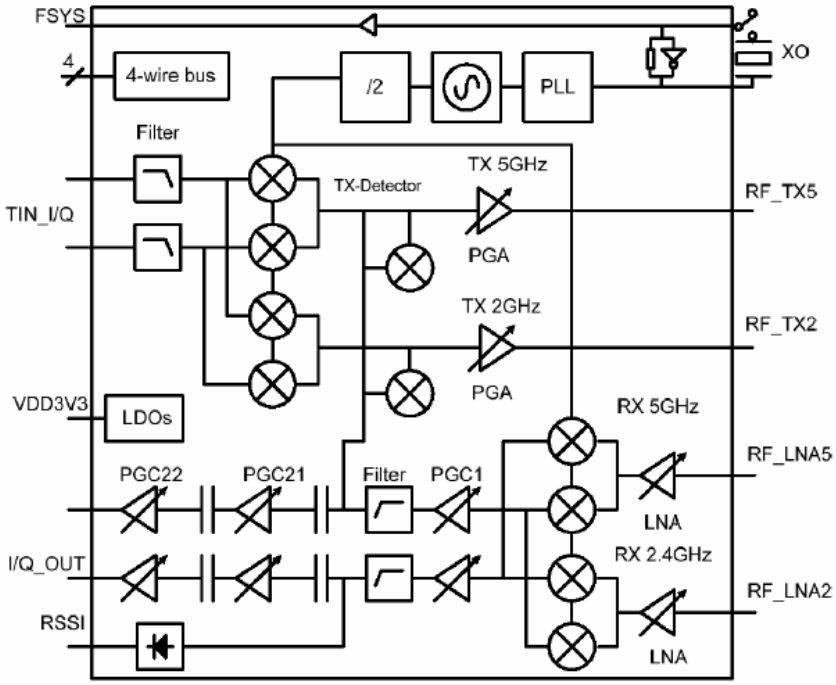


Detailed architecture for one band:

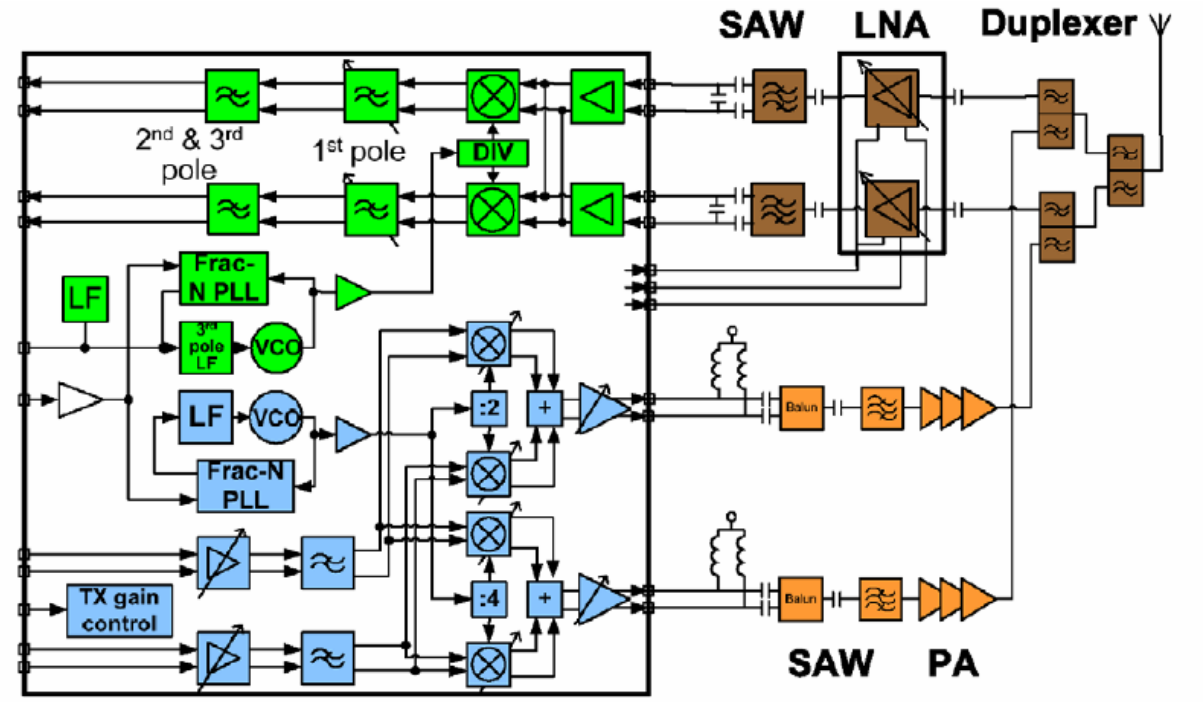


3. 11a/b/g Transceiver

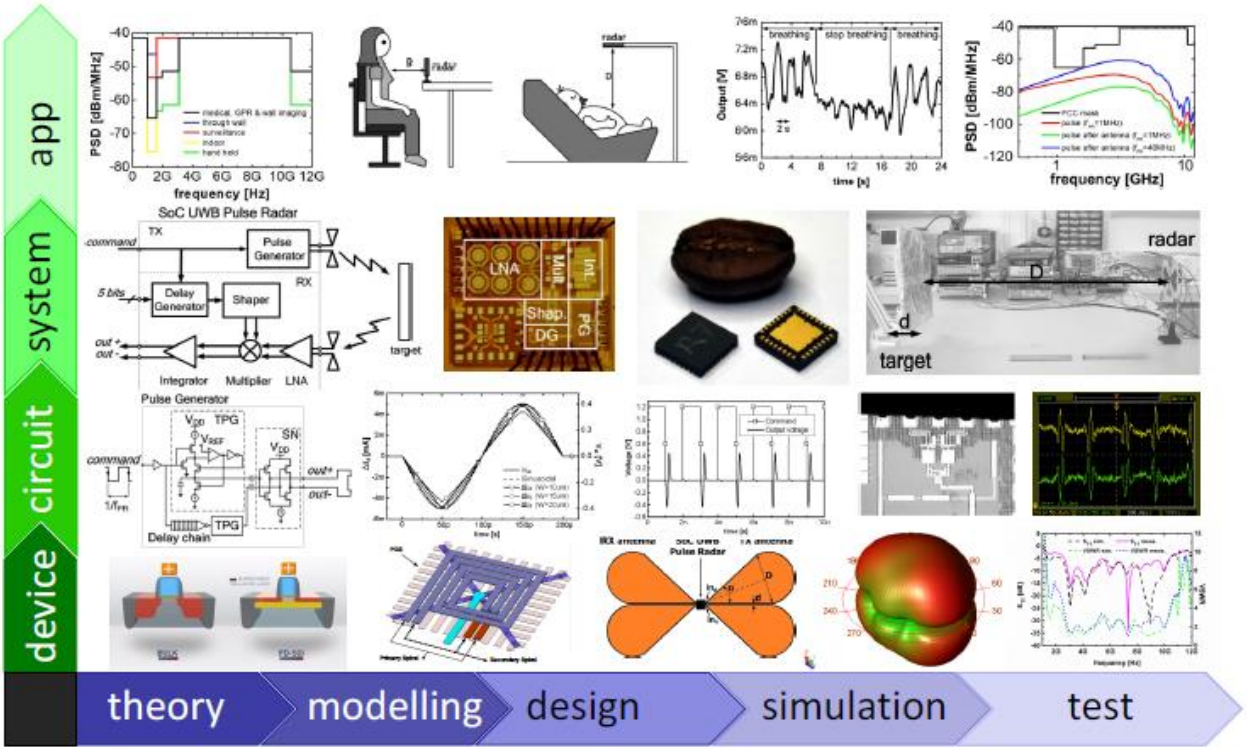
[Simon, ISSCC07]



4. CDMA2000 Transceiver



Research & Innovation Space



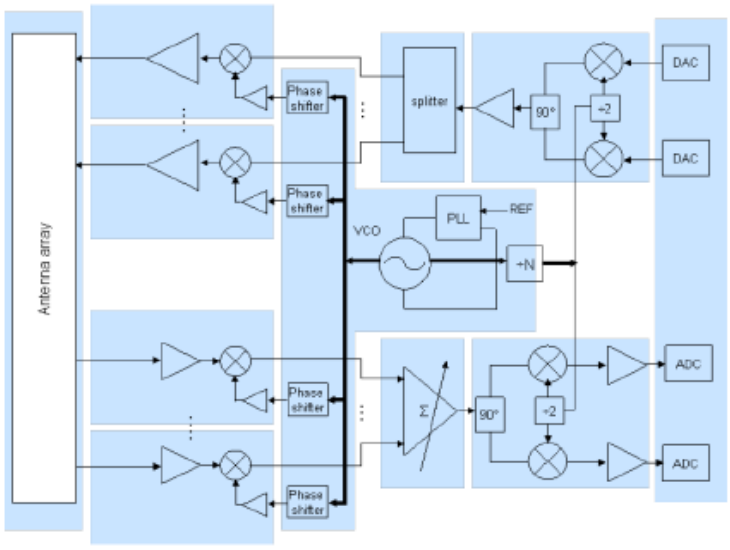
- **World-1st SoC UWB Pulse RADAR**
- **1st of 6 best ISSCC papers Tech. for Health**
- **Invited paper IEEE T-BioCAS**
- **Best Tyndall Paper 2011**
- **Successful model in ICT for Health across EU FP**

Receiver/Transmitter & Building blocks

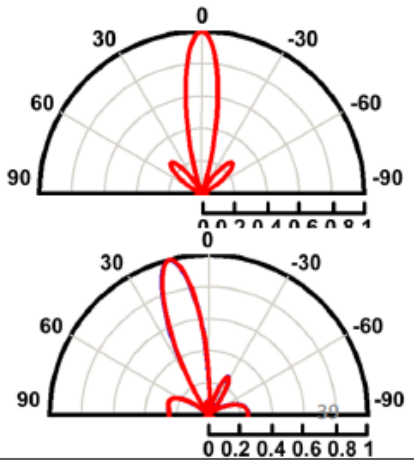
- Low Noise Amplifiers (LNAs)
- Voltage Controlled Oscillators (VCOs)
- Passive Components
- Active Inductors
- Power Amplifiers (not shown)
- Phase Shifters

Timed(Phased)-array Transceivers

- Electronic beam steering
- Compact antennas
- Phase shifting (hardware↑, power ↑)

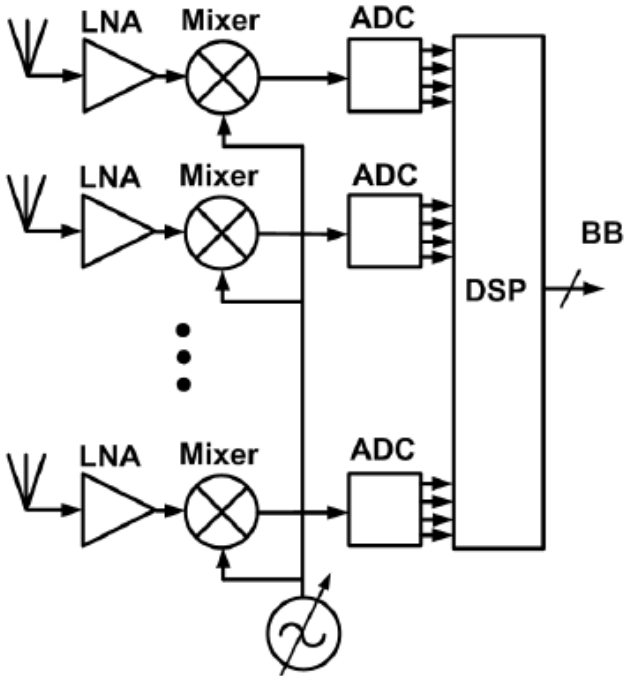


(Courtesy of Prof. S.P. Voinigescu, University of Toronto)



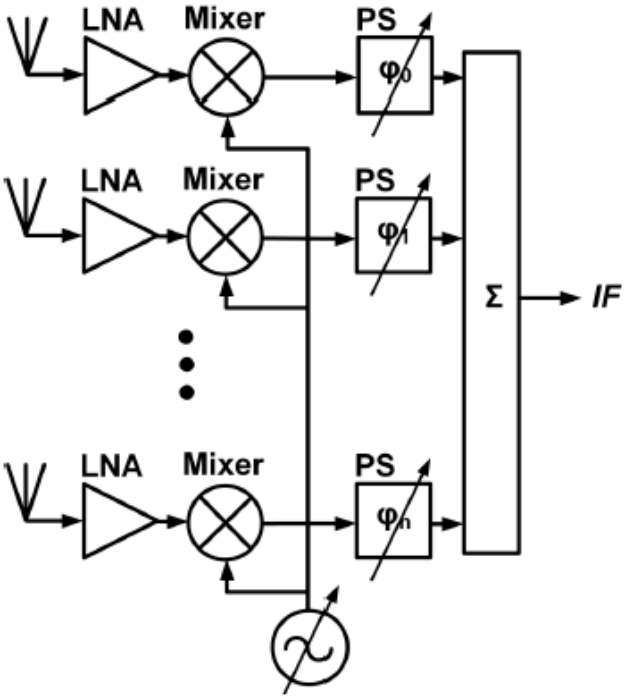
Phased-Array Architectures

- Digital (BB) phase shifting



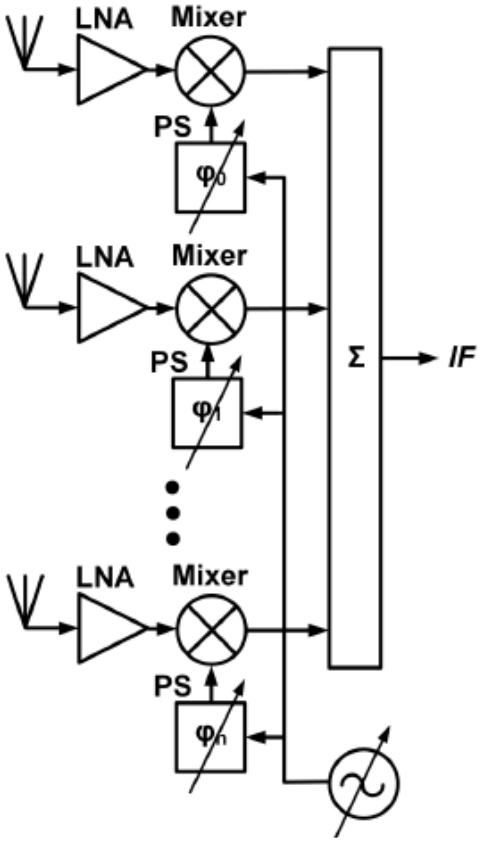
Phased-Array Architectures

– IF phase shifting



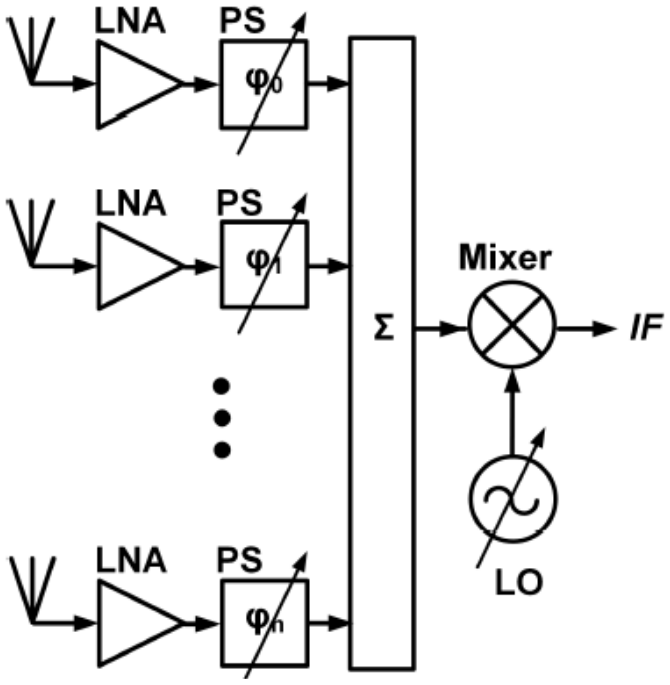
Phased-Array Architectures

– LO phase shifting

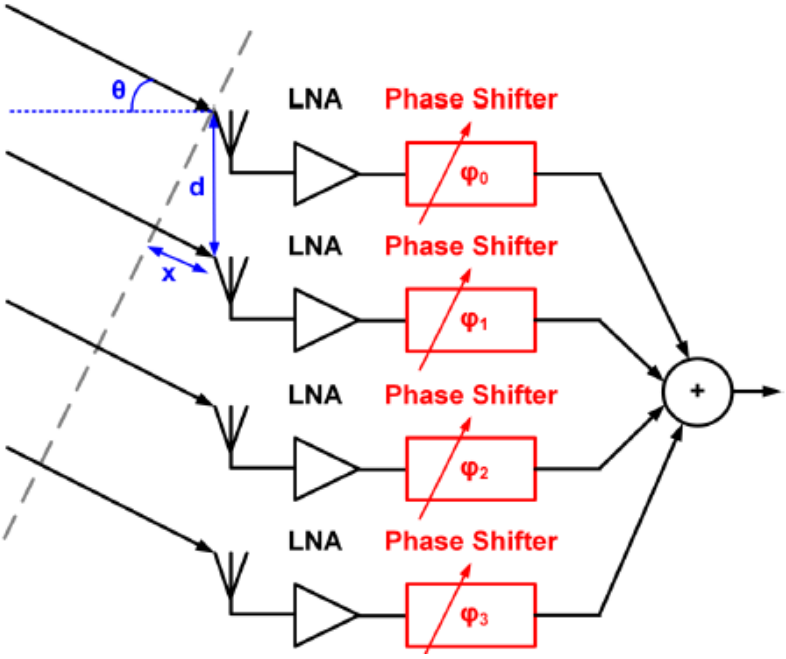


Phased-Array Architectures

– RF phase shifting



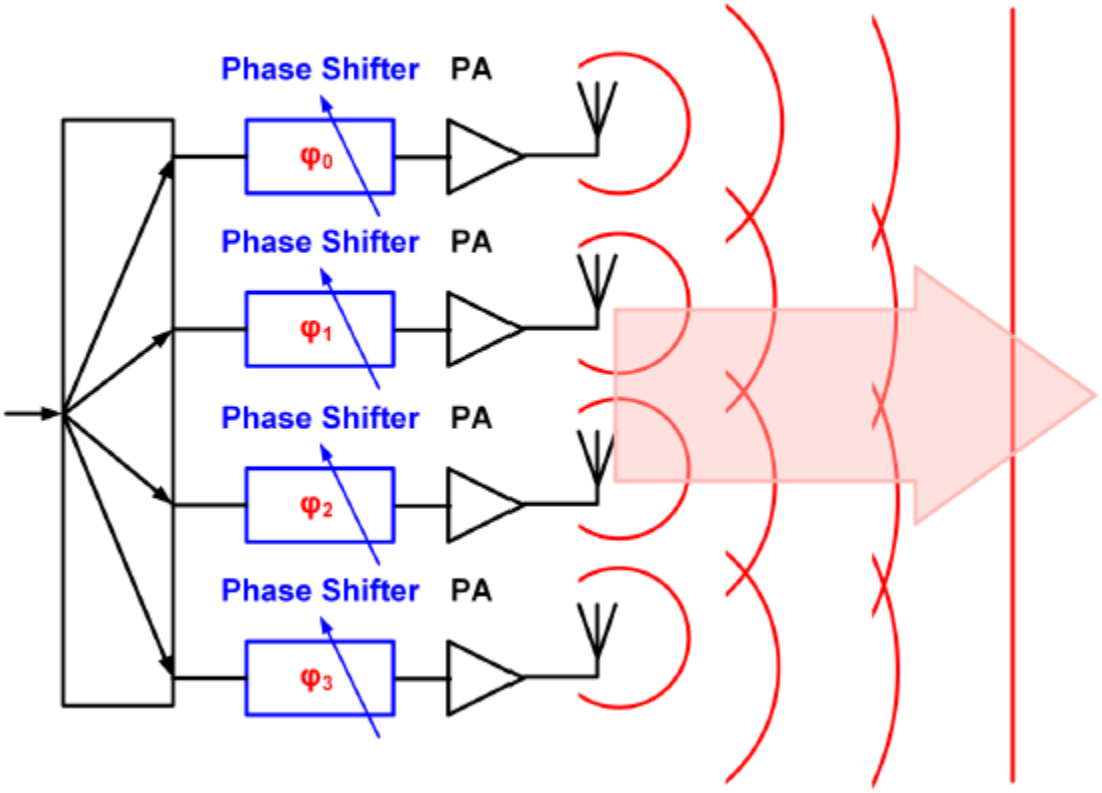
- RF phase shifting (4-element receiver)



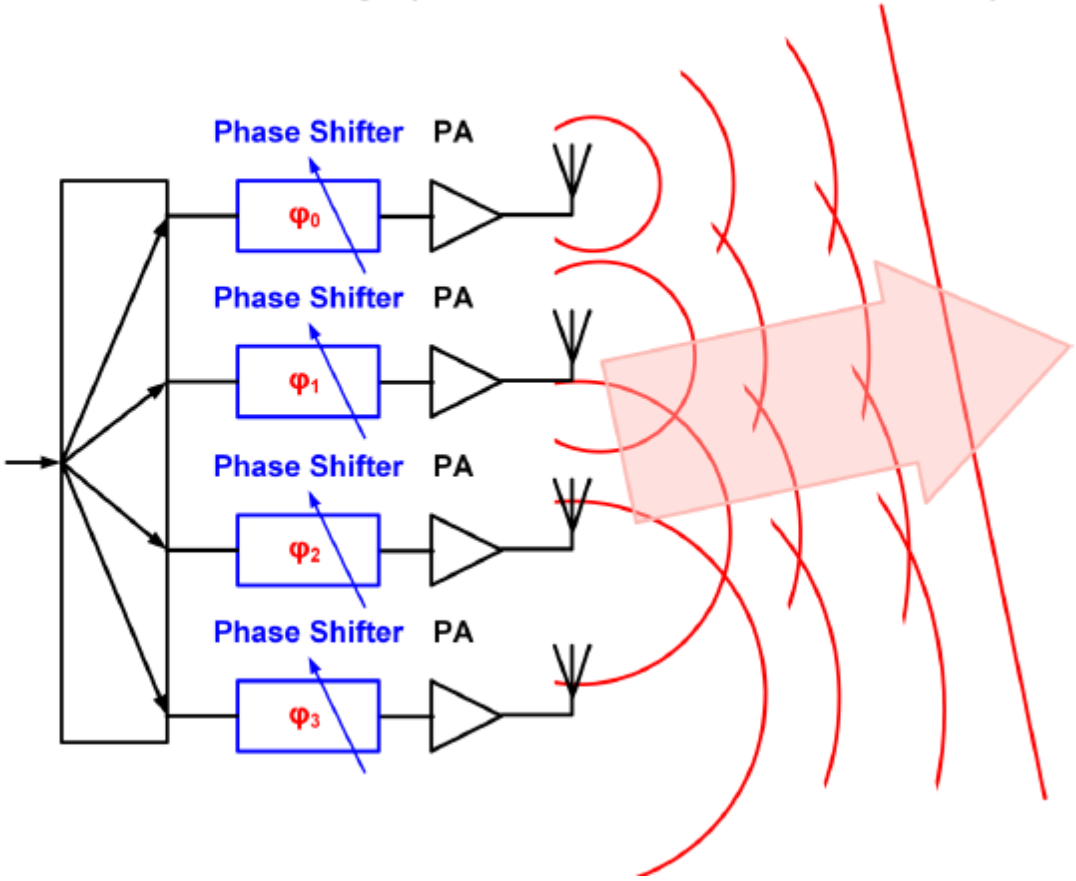
$$x = c \times \tau = d \times \sin\theta$$

$$\Delta\varphi = \frac{360^\circ \times d \times \sin\theta}{\lambda}$$

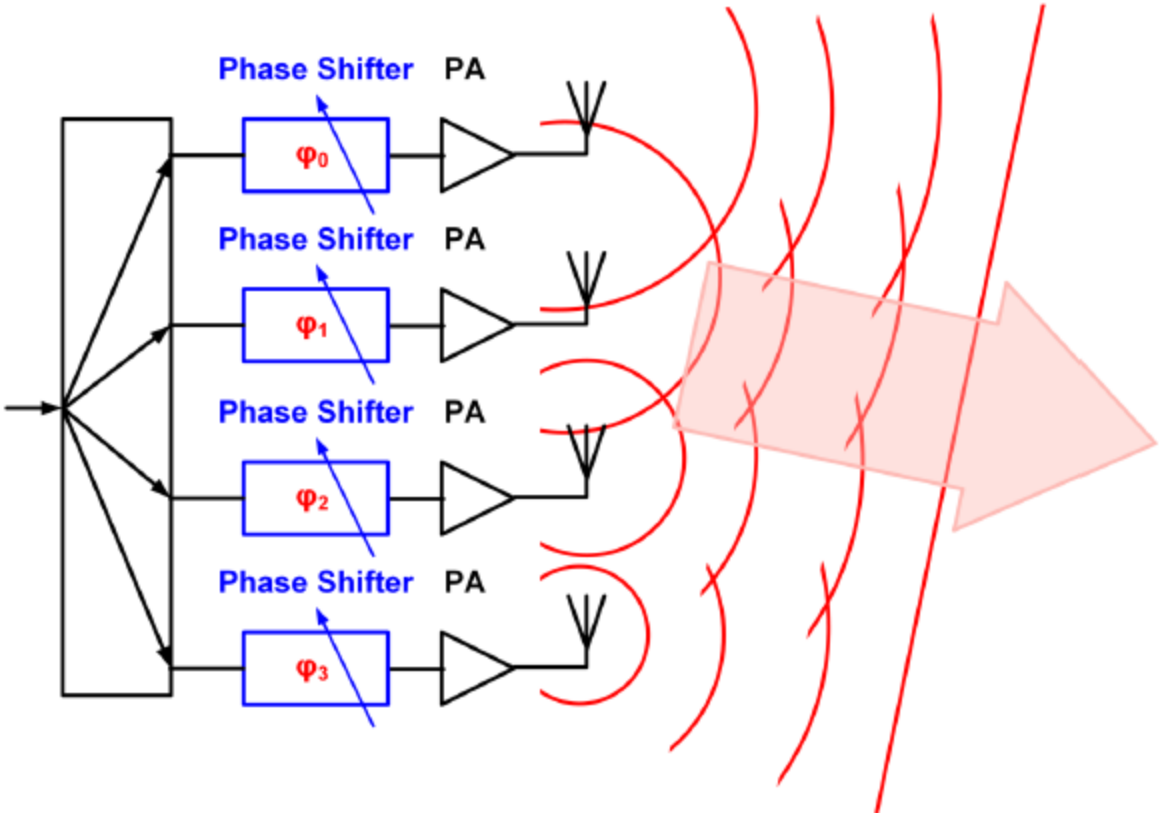
RF phase shifting (4-element transmitter)



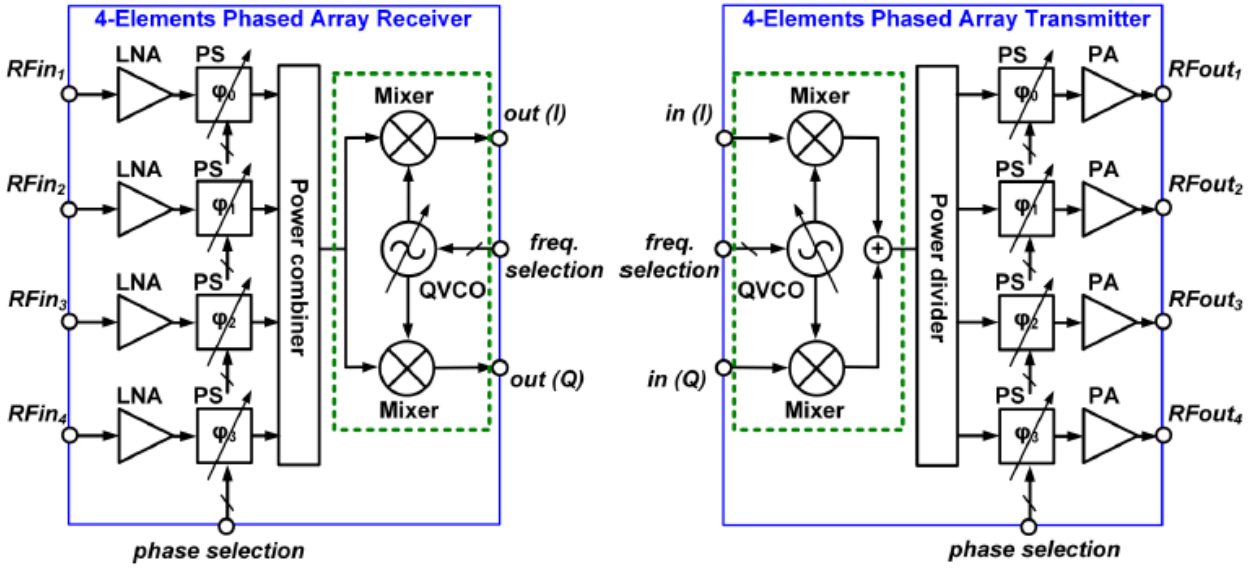
RF phase shifting (4-element transmitter)



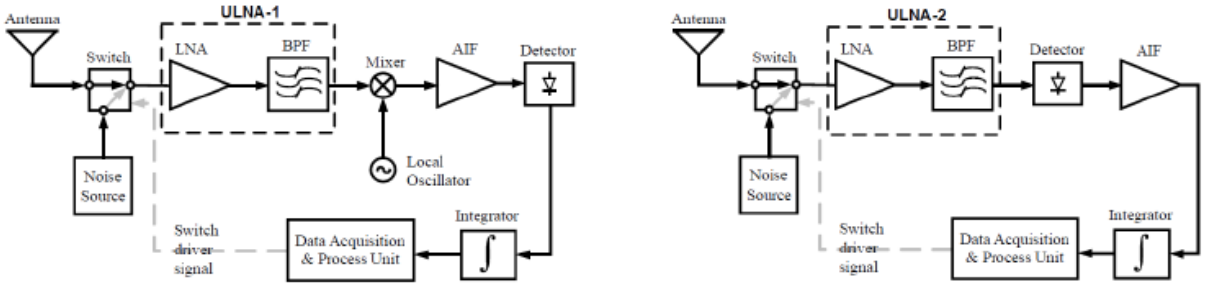
RF phase shifting (4-element transmitter)



- RF phase shifting (4-element transceiver)



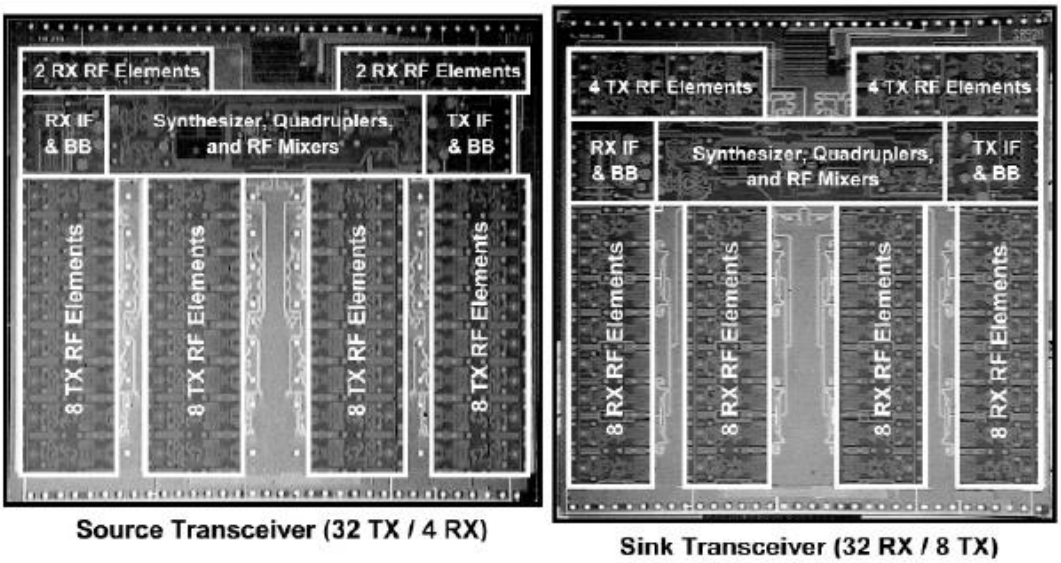
- Ultra-low noise radio receivers
  - Input signal is noise (very high sensitivity)
  - Noise source reference (accurate calibration)
  - Direct-conversion Detection & Direct Detection architectures (pros & cons)



$$\rho_T = \sqrt{\frac{2(T_A+T_R)^2}{BW\tau} + \frac{2(T_N+T_R)^2}{BW\tau} + 2(T_A - T_R)^2 \left(\frac{\Delta G}{G}\right)^2}$$

Zito, et al., "CMOS Microwave Radiometer: Experiments on Down-Conversion and Direct Detections", IEEE ICECS 2008

- 60 GHz Uncompressed Wireless HD Video Area
  - Commercial development



Source Transceiver (32 TX / 4 RX)

Sink Transceiver (32 RX / 8 TX)

S. Enami et al. "60GHz CMOS Phased-Array Transceiver Pair for Multi-Gb/s Wireless Communications", IEEE ISSCC 2011

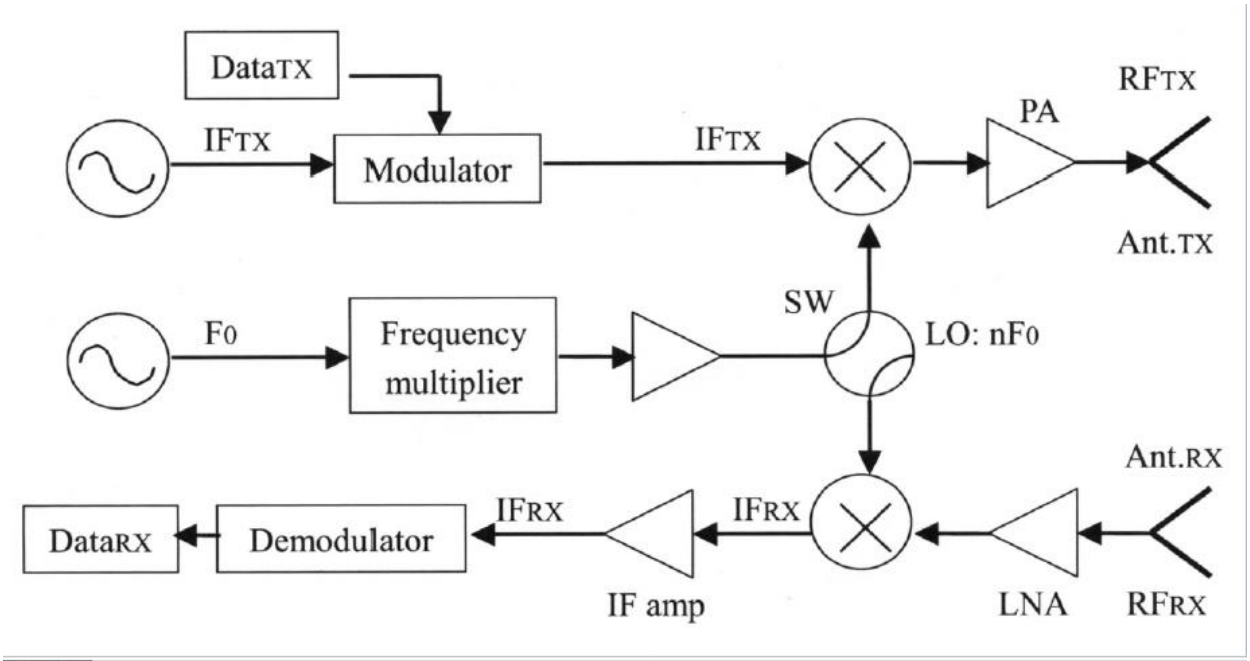
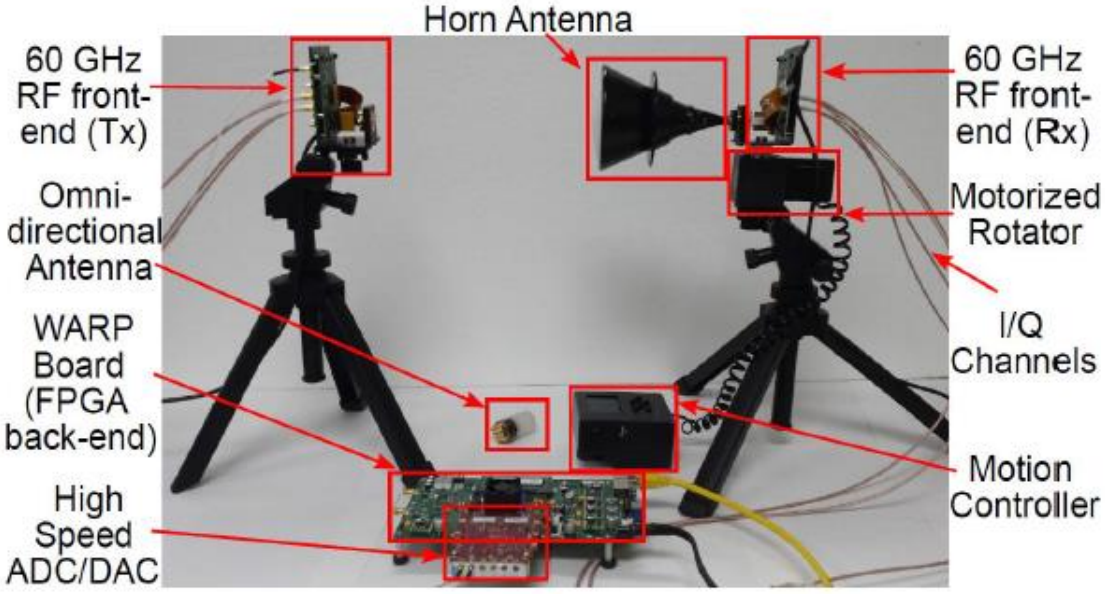


Fig. 1 *A typical configuration for MMW front-end modules*

Fig. schematically shows a typical configuration for MMW front-end modules. Millimeterwave wireless communications equipment, consisting of a number of components, is based on a wide range of technical factors: high capability in each component, analysis and design arts, and test and measurement techniques along with innovations in electronic devices and materials.

WiMi (Wisconsin Millimeter-wave software radio)

- Reconfigurable 60 GHz transmitter/receiver
- Programmable sensing/imaging radar



WiMi (Wisconsin Millimeter-wave software radio)

- Antennas with different beam patterns and steerable motion control system

Baseband: Vertex-6 FPGA plus high-speed AD/DA, 245.76Msps sampling rate; programmable waveform generator/processor

RF front-end: Vubiq V60WDG03, 57-64GHz frequency upconverter/downconverter with ~2GHz analog bandwidth; adjustable output power (up to 10 dBm)

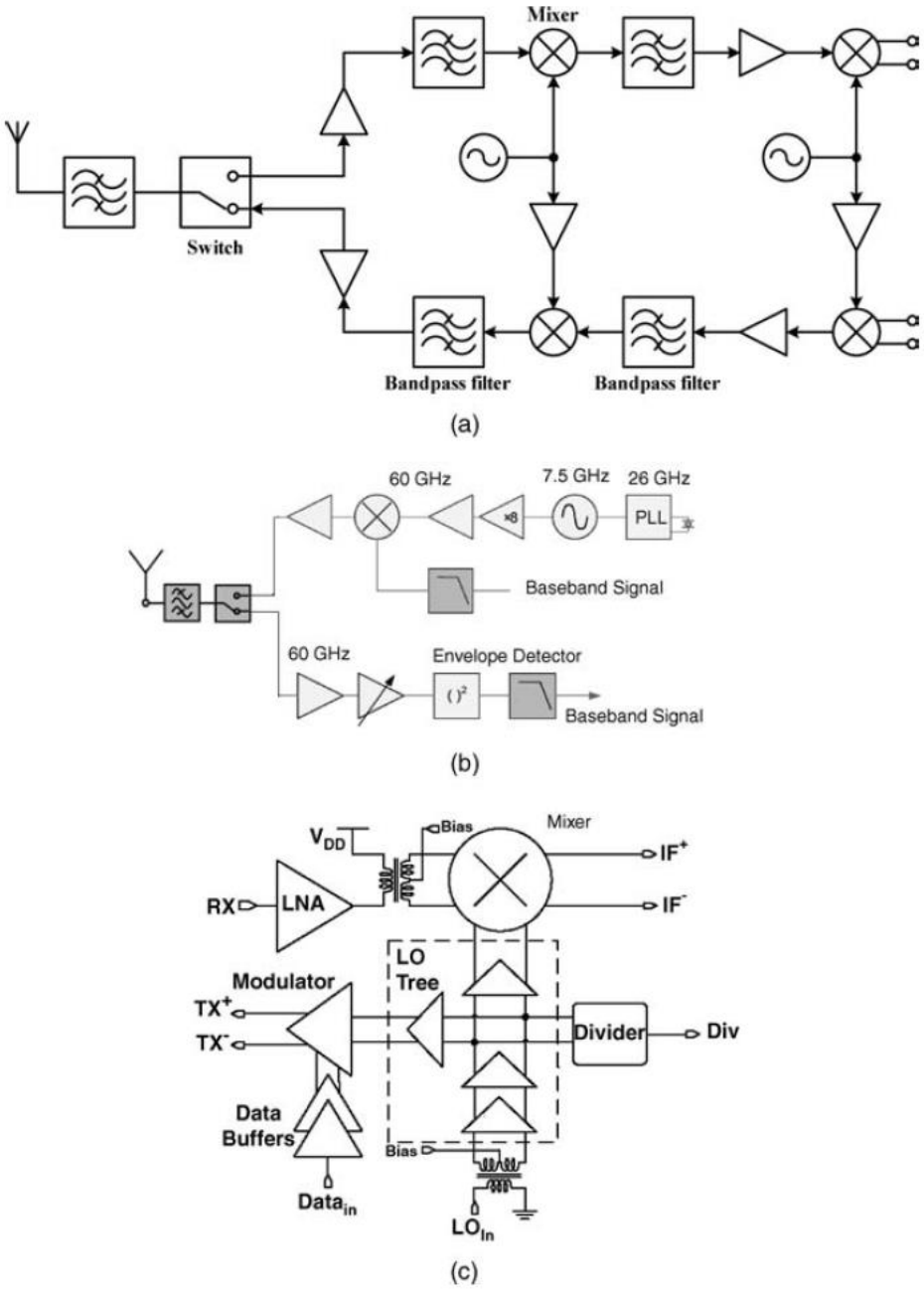


Figure 3.3. (a) Block diagram for millimeter wave/microwave superheterodyning system. (b) Block diagram for 60 GHz direct conversion system with noncoherent on/off keying (OOK) modulation. (c) Block diagram for 65 nm CMOS 60 GHz direct conversion system with coherent BPSK/QPSK modulation [11] (©2008 IEEE)