VLSI Design Lab Experiment - V

I Pre-hab Oversions:

1. White the epiphossion by propagate and generate term in a

de Pi = ai e bi

2. List the efficient method Bi- implementing 64- addler using CSA technique.

Soln a) Divide To implement a 64 bit addle using Carry Ship addler, divide into 16 4-bit blocks, implement 4-bit carry Ship addler, Connect Carry out to Carry in 61- Each block, add any remaining carry bits with a lineal 4-bit adder, and Connect Brinal Carry out to Carry out of little block.

I Post- Lab Diestions.

Compare to Chear, Johns got power tepart of tipple carry and CSA in/Xilinx JSE. Greate a Comparision chart and justify the results.

Solo

	Riple Carry Atter	Carry Ship adda.
Atra	8 male	hanse
Delay	Large	Smell
Ruer.	More Edicient.	help agricunt.

hist the application of CSA in VLSI Design.

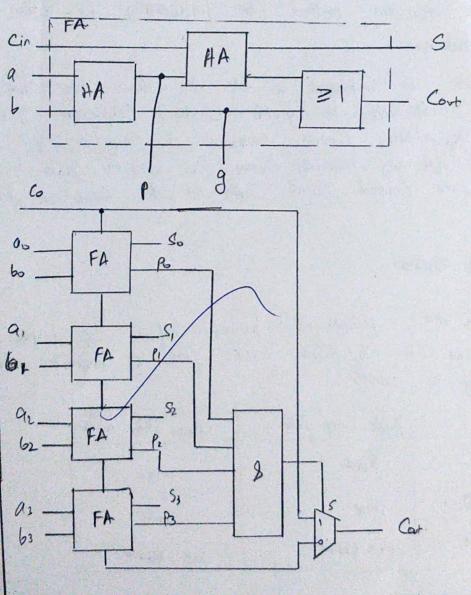
John Carry Ship addes are willy used in VLCO Design Br high speed arithmetic sporations in microprocessors, DSP, image.

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and vite processing, Cryptography, and high-performance Comparing. They anable flost and policible abithmetic offortations in a wite former of applications

Prepare the Synthesis Chart Bor a 4-bit Carry Ship addle.

Soln.



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4. Con belining mechanism improve the Spools auxilia in CSA applications?

Yes, Retining mechanism on infrare the Steed of Carry Shiph adder by pedvicing the number of loves and logic and minimizing the tellay caused by the Carry Chain.

RESULT:

Solo.

Thus, the beign of 4-bit Goty Aix adds Circuit was Simulated in votiles and Synthesical Using EDA tooks.