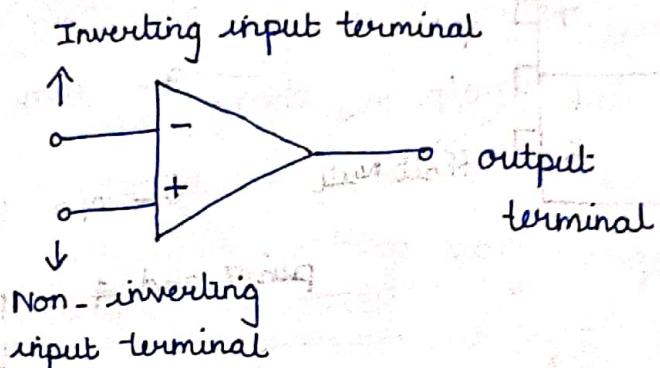


OPERATIONAL AMPLIFIER CHARACTERISTICS

IC is a miniature, low cost electronic circuit consisting of Active and passive components that are joined together on single chip of Silicon

OP-AMPSymbol

OP-AMP is operational amplifier. It is a multi terminal device

OP-AMP Packages:

op-amp packages may contain single, two (dual) or four (quad) op-amps.

Three popular packages available

- (i) Metal can (TO) package
- (ii) Dual - in - line package
- (iii) flat package or flat pack

→ no. of
Terminals
may be 8 or
10 or 14.

e.g.: $\mu A 741 \rightarrow$ 8-pin can, 8 pin DIP

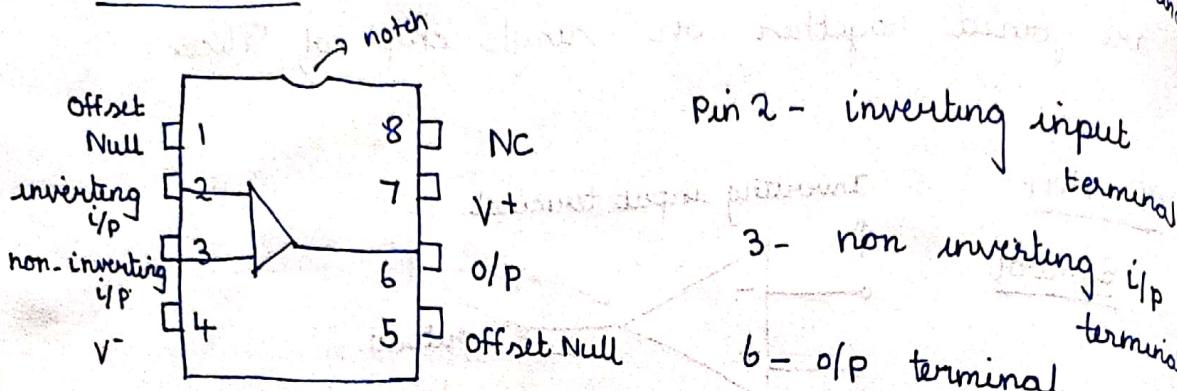
10 pin flat pack or 14-pin
DIP.

OP- AMP Terminals:

OP-amps have 5 basic terminals

- 2 i/p terminals
- 1 o/p terminal
- 2 power supply terminals

8 PIN DIP.



Pin 2 - inverting input terminal

3 - non inverting i/p terminal

6 - o/p terminal

pin 7 and 4 - power Supply terminals labelled as V^+ and V^-

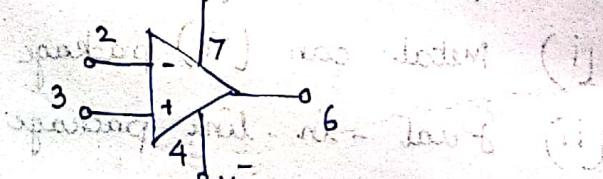
1 and 5 - dc offset

pin 8 - 'NC' - No connection

Top pin on left of notch locates pin 1 (DIP)

& flat pack has a dot on it for identification.

other pins are numbered (in counter clockwise) from pin 1



SPECIFICATIONS:

OP-amp - 741

e.g: National Semiconductor - LM741

Motorola - MC1741

RCA

- CA3741

Texas Instruments - SN52741

Signetics - N5741

last 3 digits are 741. All these have same specifications.
Some linear IC's have classes such as A, C, E, S, SC.
Main difference is

741 - Military grade OP-AMP.

741C - commercial "

741A - improved version of 741

741E - " of 741C

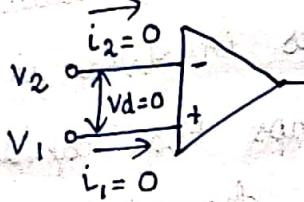
741S - Military grade OP-AMP with higher slew rate

741SC - commercial " " " " " "

POWER SUPPLY Power supply voltage may range from $\pm 5V$ to $\pm 22V$

IDEAL OPERATIONAL AMPLIFIER:

It has two input terminals and one output terminal.



The - and + symbols at the input refers to inverting and non inverting input terminals i.e.,

$V_1 = 0$; o/p $V_0 = 180^\circ$ out of phase with input signal V_2

$V_2 = 0$; V_0 inphase with i/p signal V_1

The ideal op-amp has following characteristics. hence (inverting & non inverting terminals are at equal voltages). hence open loop voltage gain, $A_{OL} = \infty$ voltage diff is zero.

Input impedance, $R_{in} = \infty$

$$\text{gain} = \frac{V_o}{V_i}$$

output impedance, $R_o = 0$

$$= \frac{V_o}{0} = \infty$$

Bandwidth, $BW = \infty$

Zero offset, ie $V_0 = 0$ when

- (i) an ideal op-amp draws no current at both the input terminals i.e., $i_1 = i_2 = 0$. Because of infinite input impedance, any signal source can drive it and there

(i) no loading on the preceding driver stage

(ii) The gain of the ideal op-amp is infinite

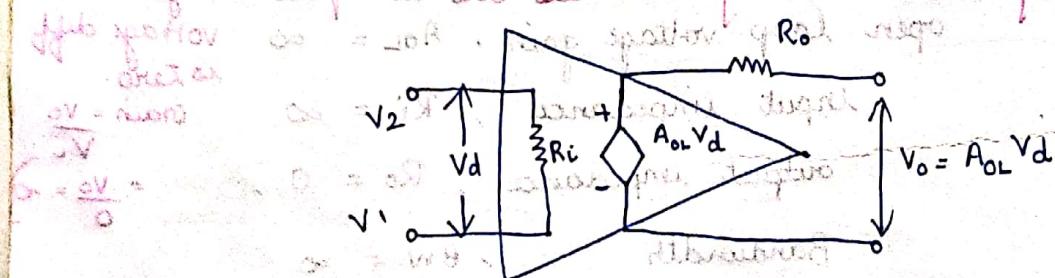
Hence, the voltage between the inverting and non-inverting terminals is essentially zero for a finite output voltage.

(iii) The output voltage V_o is independent of the output current drawn from the op-amp since $R_o = 0$. This means that the output can drive an infinite number of output devices of any impedance value.

The above properties can never be realized in practice; however, the use of such an Ideal opamp model simplifies the mathematics involved in op-amp circuits. There are practical op-amps that can be made to approximate some of these characteristics.

PRACTICAL OP-AMP:

A physical op-amp is not ideal. The equivalent circuit of an op-amp is shown below



$$\text{where } A_{OL} \neq \infty, R_i = \infty \text{ & } R_o \neq 0.$$

It can be seen that op-amp is a voltage controlled voltage source and $A_{OL}V_d$ is equivalent to a dependent voltage source.

voltage source and R_o is the thevenins equivalent resistance looking back into o/p terminal of an op-amp

This equivalent circuit is useful in analyzing the basic operating principles of op-amp.

The output voltage is

$$V_o = A_{OL} V_d$$

$$= A_{OL}(V_1 - V_2)$$

This equation shows that the op-amp amplifies the difference between the two input voltages.

OPEN LOOP CONFIGURATIONS:

The term open-loop indicates that no feedback is fed to input from output. In this configuration op-amp functions as very high gain amplifier.

There are three open loop configurations

(i) differential amplifier

(ii) inverting amplifier

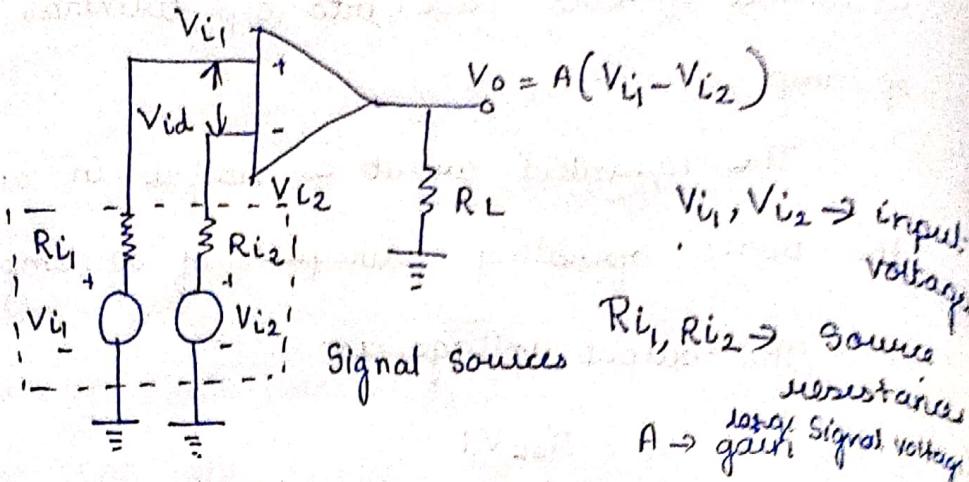
(iii) Non inverting amplifier

classifications are made based on no. of inputs used and terminal to which input is applied.

differential amplifier

(i) Inputs are applied to both inverting and non inverting input terminals and it amplifies

the difference between two input voltages.



ii) R_{i1} & R_{i2} are negligible when compared to very high input resistance offered by op amp.

iii) Thus voltage drop across these source resistances is assumed to be zero. The output voltage V_o is given by

$$V_o = A(V_{i1} - V_{i2})$$

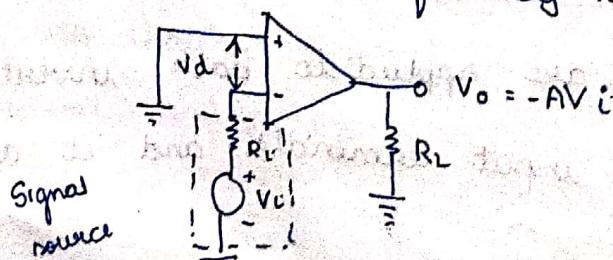
(iv) o/p voltage is equal to voltage gain A times the difference between the two input voltages. That's why it is called differential amplifier.

Inverting amplifier

(i) The g/p signal is applied to inverting input terminal of op amp and non inverting terminal is connected to ground.

(ii) o/p voltage is 180° out of phase with input & hence V_o is given by $V_o = -AV_i$

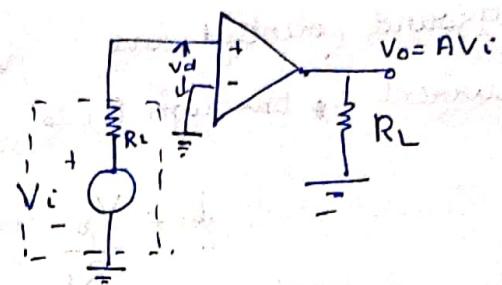
(iii) \therefore In inverting amplifier g/p signal is amplified by open loop gain A and phase shifted by 180° .



Non inverting amplifier

- (i) g/p signal is applied to non inverting input terminal of opamp and the inverting i/p terminal is connected to ground
- (ii) g/p signal is amplified by open-loop gain A and the o/p is in phase with the i/p signal

$$V_o = A V_i$$



Limitations:

- (i) clipping of output waveform occurs when o/p voltage exceeds saturation level of op-amp. This is due to very high loop gain of op-amp. Thus it amplifies only very low frequency signals of order of microvolt or even less which are more susceptible to noise and amplification is almost impossible.
- (ii) open loop gain is not constant as it varies with temperature and variations in power supply. Also b/w is negligibly small. This makes it unsuitable for ac applications.
- (iii) cannot be used for linear applications.

CLOSE LOOP CONFIGURATIONS:

o/p is fed back to input. If signal feedback is 180° out of phase w.r.t i/p then f/b is -ve feedback
if the feed back signal is in phase with input then feedback is positive feedback.

The Inverting amplifier

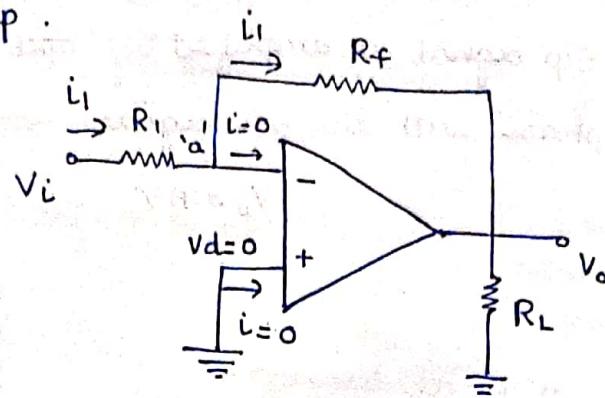
The output voltage V_o is fed back to inverting input terminal through $R_f - R_i$ where $R_f \rightarrow$ feedback resistor

Input Signal v_i is applied to inverting input terminal through R_1 , and non-inverting input terminal of op-amp is grounded

Assume ideal op-amp.

As $V_d = 0$, node 'a' is at ground potential and current i_1 through R_1 is

$$i_1 = \frac{V_i}{R_1}$$



Also since op-amp draws no current, all current flowing through R_1 must flow through R_f . The output voltage,

$$V_o = -i_1 R_f = -\frac{V_i}{R_1} R_f$$

gain of inverting amplifier is

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Alternatively,

nodal eqn at node 'a' is

$$\frac{V_a - V_i}{R_1} + \frac{V_a - V_o}{R_f} = 0$$

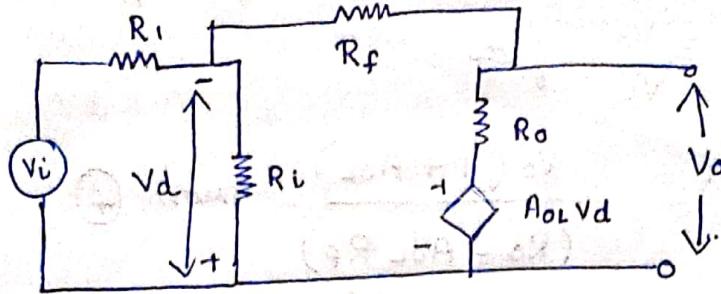
$V_a \rightarrow$ voltage at node 'a'

since node 'a' is at virtual ground, $V_a = 0$

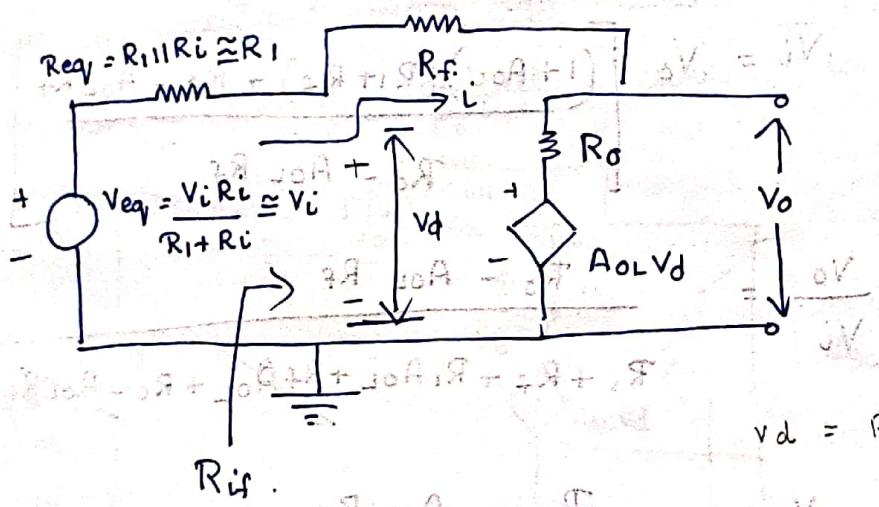
$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

-ve sign indicates phase shift of 180° between V_i and V_o .

practical inverting amplifier



eqn ① is valid only for ideal case. for practical op-amp closed loop voltage gain is calculated using low frequency model. This circuit is replaced by applying Thevenin's Theorem. The input impedance R_{in} is much greater than R_1 ,
so $V_{eq} \approx V_i$ & $R_{eq} \approx R_1$



$$V_o = iR_o + AOL V_d \quad \text{--- } ②$$

$$\text{Also } V_d + iR_f + V_o = 0 \quad \text{--- } ③$$

sub ③ in ②

$$V_o = iR_o + AOL(-V_o - iR_f)$$

$$V_o(1 + AOL) = iR_o - iR_f AOL$$

$$V_o(1 + AOL) = i(R_o - AOL R_f) \quad \text{--- } ④$$

Also KVL loop eqn gives

$$V_i = i(R_1 + R_f) + V_o \quad \text{--- } ⑤$$

put value of i from ④ in ⑤ & solving for closed

loop gain $A_{CL} = \frac{V_o}{V_i}$, gives

$$i = \frac{V_o(1 + A_{OL})}{(R_o - A_{OL}R_f)} \quad \text{from ④}$$

Sub in ⑤

$$V_i = \frac{V_o(1 + A_{OL})(R_i + R_f)}{(R_o - A_{OL}R_f)} + V_o$$

$$V_i = V_o \left[\frac{(1 + A_{OL})(R_i + R_f)}{R_o - A_{OL}R_f} + 1 \right]$$

$$V_i = V_o \left[\frac{(1 + A_{OL})(R_i + R_f) + R_o - A_{OL}R_f}{R_o - A_{OL}R_f} \right]$$

$$\frac{V_o}{V_i} = \frac{R_o - A_{OL}R_f}{R_i + R_f + R_i A_{OL} + R_f A_{OL} + R_o - A_{OL}R_f}$$

$$A_{CL} = \frac{V_o}{V_i} = \frac{R_o - A_{OL}R_f}{R_o + R_f + R_i(1 + A_{OL})} \quad \text{--- ⑥}$$

It can be seen that $A_{OL} \gg 1$ and $A_{OL}R_i \gg R_o + R_f$

$$A_{CL} \approx -\frac{R_f}{R_i}$$

INPUT RESISTANCE R_{if}

from the diagram, $R_{if} = \frac{V_d}{i} \quad \text{--- ⑦}$

writing loop equation and solving

$$V_d + i(R_f + R_o) + A_{OL} V_d = 0; \quad V_d = iR_f + iR_o - A_{OL}V_d$$

$$V_d + A_{OL}V_d - iR_f - iR_o = 0$$

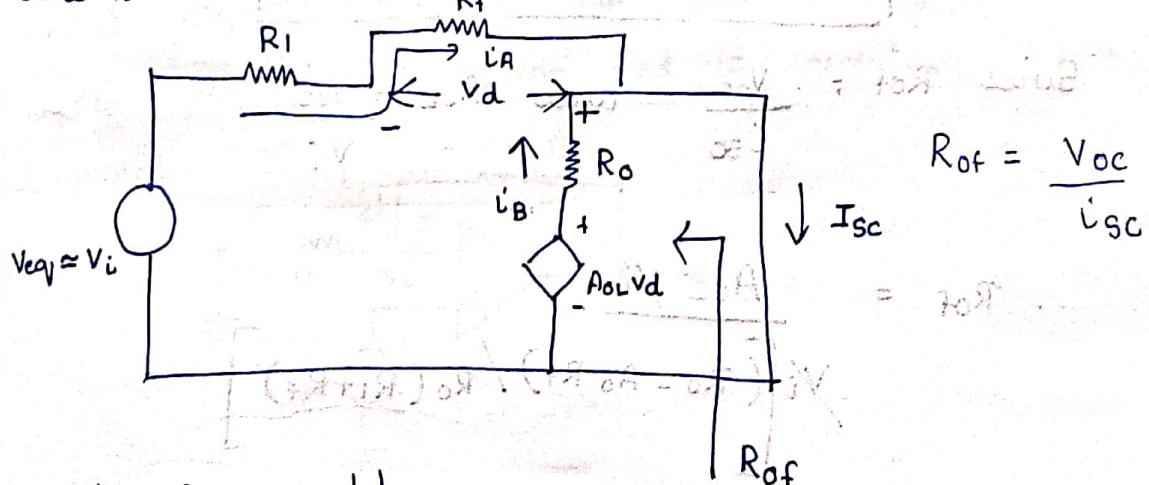
$$V_d (1 + A_{OL}) = i(R_f + R_o)$$

$$\frac{V_d}{i} = \frac{R_f + R_o}{1 + A_{OL}}$$

$$\therefore R_{if} = \frac{R_f + R_o}{1 + A_{OL}} \quad - \textcircled{8}$$

OUTPUT RESISTANCE R_{of}

R_{of} is calculated from open circuit output voltage V_{oc} and short circuit output current I_{sc}



under S.C condition,

$$i_A = \frac{V_i}{R_1 + R_f} \quad \text{and} \quad i_B = \frac{A_{OL} V_d}{R_o}$$

$$\text{Since } V_d = -i_A R_f$$

$$i_B = -\frac{A_{OL} i_A R_f}{R_o}$$

$$i_{sc} = i_A + i_B \quad (\text{KCL at node}) \quad - \textcircled{9}$$

Sub i_A and i_B in $\textcircled{9}$

$$i_{sc} = \frac{Vi}{R_i + R_f} - \frac{A_{OL} i_A R_f}{R_o}$$

Sub values
in here

$$\times \left(= \frac{Vi R_o - A_{OL} i_A R_f (R_i + R_f)}{R_o (R_i + R_f)} \right) \times$$

$$= \frac{Vi}{R_i + R_f} - \frac{A_{OL} \cdot Vi \cdot R_f}{R_o (R_i + R_f)}$$

$$= \frac{Vi R_o - A_{OL} Vi R_f}{R_o (R_i + R_f)}$$

$$i_{sc} = \frac{Vi (R_o - A_{OL} R_f)}{R_o (R_i + R_f)}$$

- 10

Since $R_{of} = \frac{V_{oc}}{i_{sc}}$ and $A_{CL} = \frac{V_{oc}}{Vi}$

$$\therefore R_{of} = \frac{A_{CL} Y_i}{Y_i [(R_o - A_{OL} R_f) / R_o (R_i + R_f)]}$$

But ^{sub} A_{CL} from eqn 6

$$\therefore R_{of} = \frac{\cancel{R_o - A_{OL} R_f}}{R_o + R_f + R_i (1 + A_{OL})}$$

$$\frac{\cancel{R_o - A_{OL} R_f}}{R_o (R_i + R_f)}$$

$$R_{of} = \frac{R_o (R_i + R_f)}{R_o + R_f + R_i (1 + A_{OL})}$$

- 11

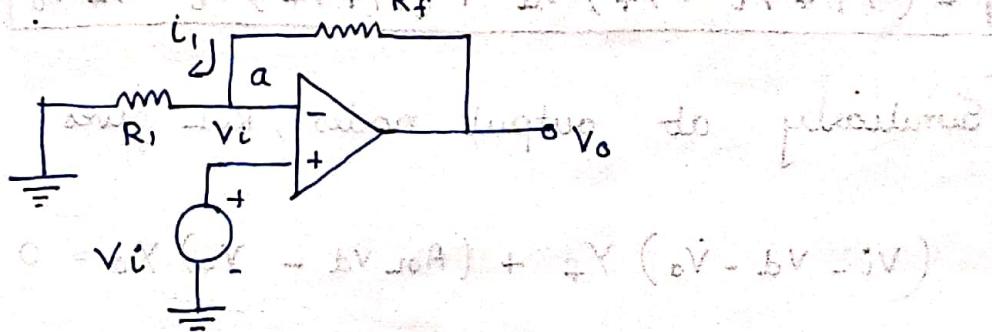
This can be alternatively written as

$$R_{of} = \frac{R_o(R_i + R_f)}{R_o + R_i + R_f} - \textcircled{12}$$
$$= 1 + \frac{R_i A_{BL}}{R_o + R_i + R_f}$$

Numerators from $\textcircled{12}$ consist of term $R_o(R_i + R_f)$ and is smaller than R_o . R_{of} is therefore always less than 1. and for $A_{CL} \rightarrow \infty$, $R_{of} \rightarrow 0$.

THE NON INVERTING AMPLIFIER.

This circuit amplifies without inverting the input signal. This is also called as negative feedback system as o/p is being fed to inverting input terminal.



As differential voltage V_d at input terminal is zero, the voltage at node 'a' is V_i . Now R_f & R_i forms a potential divider.

$$\therefore V_i = \frac{V_o}{R_i + R_f} \cdot R_i$$

As no current flows in the op-amp

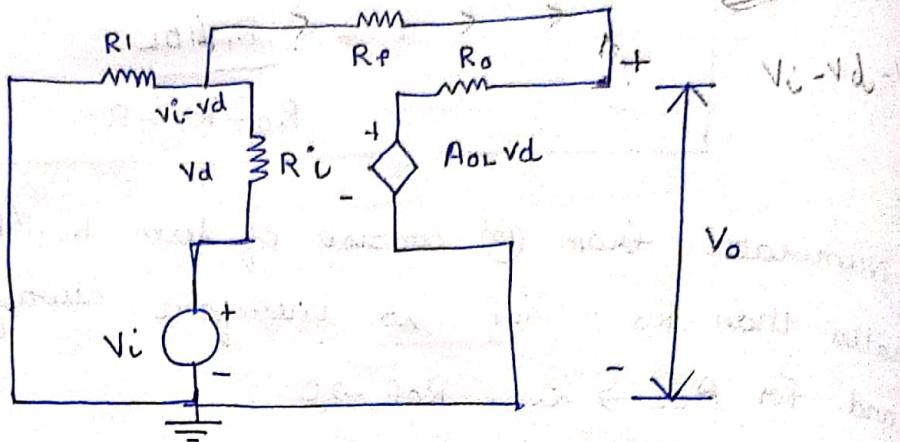
$$\frac{V_o}{V_i} = \frac{R_i + R_f}{R_i} = 1 + \frac{R_f}{R_i}$$

∴ for non-inverting amplifier the voltage gain -

$$A_{CL} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_i}$$

Practical Non-inverting amplifier

$$- [V_o - (V_i + V_d)]$$



writing KCL at node

$$(V_i - V_d)Y_1 + V_d Y_i + (V_i - V_d - V_o)Y_f = 0$$

(or) contribution of both nodes

$$-(Y_1 + Y_i + Y_f)V_d + (Y_1 + Y_f)V_i = Y_f V_o \quad \text{--- (1)}$$

Similarly at output nodes, KCL gives

$$(V_i - V_d - V_o)Y_f + (A_{OL}V_d - V_o)Y_o = 0$$

i.e.,

$$-(Y_f - A_{OL}Y_o)V_d + Y_f V_i = (Y_f + Y_o)V_o \quad \text{--- (2)}$$

Now solving (1) & (2) for V_o/V_i , we get

$$\begin{aligned} A_{CL} = \frac{V_o}{V_i} &= \frac{A_{OL} Y_o (Y_1 + Y_f) + Y_f Y_i}{(A_{OL} + 1) Y_o Y_f + (Y_1 + Y_i)(Y_f + Y_o)} \\ &\quad \text{--- (3)} \end{aligned}$$

If $A_{OL} \rightarrow \infty$, the eqn (3) reduces to

$$A_{CL} \simeq \frac{A_{OL} Y_o (Y_i + Y_f)}{A_{OL} Y_o Y_f} = \frac{Y_i + Y_f}{Y_f} = \frac{1 + \frac{Y_i}{Y_f}}{1}$$

$$\boxed{A_{CL} = 1 + \frac{R_f}{R_i}}$$

eqn ② & eqn ③

$$-(Y_f - A_{OL} Y_o) \frac{V_d}{V_i} + Y_f = (Y_f + Y_o) \frac{V_o}{V_i}$$

$$-(Y_i + Y_o + Y_f) \frac{V_d}{V_i} + (Y_i + Y_f) = Y_f \frac{V_o}{V_i}$$

in Vorheriger Schritt ist Lösung der Gleichung q/o
 $-(Y_f - A_{OL} Y_o) V_d + Y_f V_i = Y_o V_o - (Y_i + Y_o + Y_f) V_d$
 mit vorheriger Gleichung kann man
 $+ (Y_i + Y_f) V_i$

$$-(V_o - V_i + V_d)$$

ist die gesuchte Gleichung für V_o

Es ist eine analoge Gleichung für V_i zu schreiben

Um diese Gleichung zu erhalten müssen wir die Gleichung q/o

umstellen so dass es möglich ist die Gleichung q/o

umzubilden so dass es möglich ist die Gleichung q/o

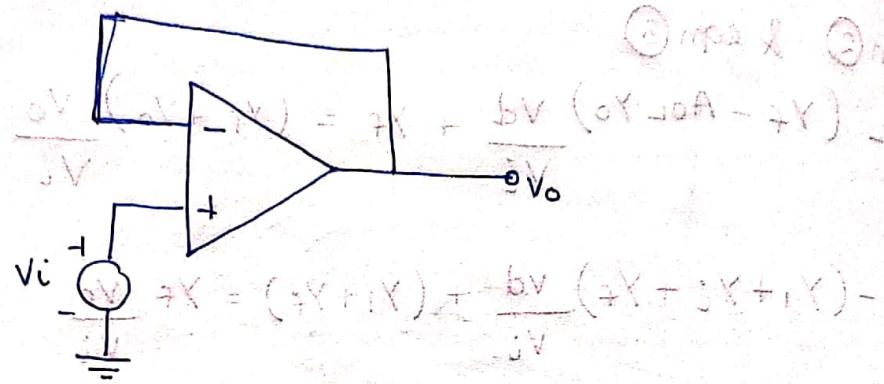
umzubilden so dass es möglich ist die Gleichung q/o

VOLTAGE FOLLOWER

In non inverting amplifier if $R_f = 0$ and $R_i = \infty$, we get the circuit

$$\text{we have } A_{CL} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_i}$$

$$\therefore V_o = V_i$$

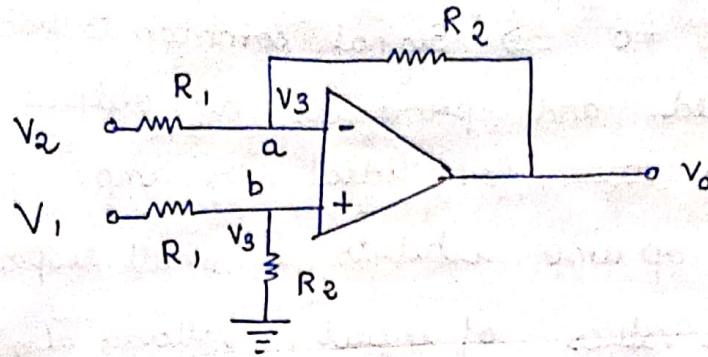


o/p voltage is equal to input voltage, both in phase and magnitude. o/p voltage follows the input voltage exactly. hence it is called voltage follower.

The use of unity gain circuit lies in the fact that its input impedance is very high & o/p impedance is zero. \therefore it draws negligible current from source.

\therefore voltage follower may be used as buffer for impedance matching, that is to connect high impedance source to low impedance load.

DIFFERENTIAL AMPLIFIER



differential voltage at input terminals of op-amp is

Zero., nodes 'a' and 'b' are at same potential.

The nodal eqn at 'a' is

$$\frac{V_3 - V_2}{R_1} + \frac{V_3 - V_o}{R_2} = 0 \quad \text{and at } b \text{ is} \quad (1)$$

$$\frac{V_3 - V_1}{R_1} + \frac{V_3}{R_2} = 0 \quad (2)$$

Rearranging,

$$\left(\frac{1}{R_1} + \frac{1}{R_2} \right) V_3 - \frac{V_2}{R_1} = \frac{V_o}{R_2} \quad \text{from } (1) \quad (3)$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2} \right) V_3 - \frac{V_1}{R_1} = 0 \quad \text{from } (2) \quad (4)$$

Sub (4) from (3)

$$-\frac{V_2}{R_1} + \frac{V_1}{R_1} = \frac{V_o}{R_2}$$

$$\frac{1}{R_1} (V_1 - V_2) = \frac{V_o}{R_2}$$

$$\therefore V_o = \frac{R_2}{R_1} (V_1 - V_2)$$

DIFFERENCE AND COMMON MODE GAINS:

If $v_1 = v_2$; $v_o = 0 \Rightarrow$ Signal common to both inputs get cancelled and produces no output voltage. This is true for ideal op-amp. However practical op amp exhibits a small response to common mode values of input voltages also. The o/p voltage depends not only on difference between input signals but it also depends on common mode signal.

Differential & common mode gains are given by

$$A_{dm} = \frac{1}{2}(A_1 - A_2) \quad \&$$

$$A_{cm} = A_1 + A_2$$

COMMON MODE REJECTION RATIO (CMRR):

It is defined as ratio of differential gain A_{dm} to common mode gain A_{cm} .

$$CMRR = \frac{A_{dm}}{A_{cm}}$$

unit is decibels

DC CHARACTERISTICS

Ideal op-amp draws no current from signal source and its response is independent of temperature variations; practical op-amp gets affected by environment. The current is indeed taken from the source into the input of opamp and the two inputs respond differently to input voltage and current. This happens due to inherent mismatch among transistors.

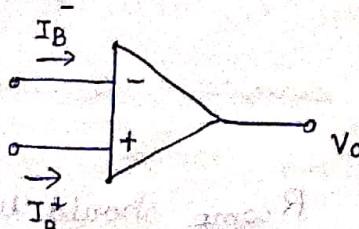
Non ideal dc characteristics of op-amp are

- (i) g/p bias current [adds error component to dc output voltage].
- (ii) g/p offset current
- (iii) g/p offset voltage
- (iv) Thermal drift

INPUT BIAS CURRENT

op-amp's input is differential amplifier which may be BJT or FET. They should be biased into linear region by supplying current into base; practically, input terminals do conduct a small value of dc current to bias input transistor. Base current entering into inverting and non-inverting terminals are I_B^- and I_B^+ .

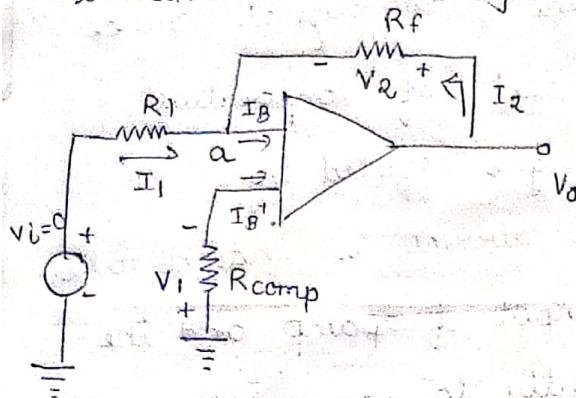
$$\text{Input bias current}, I_B = \frac{I_B^+ + I_B^-}{2} \quad \text{--- (1)}$$



I_B^+ & I_B^- are not equal due to internal imbalance

$$\text{If } V_i = 0, \Rightarrow V_o \text{ should be } 0 \text{ instead it is offset by } V_o = (I_B^-)R_f$$

This effect can be compensated by adding R_{comp} between non inverting terminal and ground.



By applying KVL

$$-V_1 + 0 + V_2 - V_o = 0$$

$$V_o = V_2 - V_1 \quad \text{--- (2)}$$

$$V_1 + V_2 = 2V_o$$

By selecting proper value of R_{comp} , V_2 can be cancelled with V_1 and o/p V_o will be zero.

$$V_1 = I_B^+ R_{comp}, \quad I_B^+ = \frac{V_1}{R_{comp}} \quad \text{--- (3)}$$

$$\text{we have } I_1 = \frac{V_1}{R_1}, \quad I_2 = \frac{V_2}{R_f} \quad \text{--- (4)}$$

for compensation, V_o should be zero for $V_i = 0$. B

$$\text{sub in (2)} \quad V_1 = V_2 \quad \text{sub in (3)}$$

$$\therefore I_2 = \frac{V_1}{R_f}$$

KCL at node 'a' gives

$$I_B^- = I_2 + I_1 = \frac{V_1}{R_f} + \frac{V_1}{R_1} = V_1 \left(\frac{1}{R_1} + \frac{1}{R_f} \right)$$

Assuming no distortion due to diodes - 7

$$I_B^- = I_B^+ \quad \text{so } I_B^- = I_B^+$$

$$\frac{V_p}{R_{comp}} = V_1 \left(\frac{1}{R_1} + \frac{1}{R_f} \right)$$

input bias current I_B

$$\text{formula of } R_{comp} = \frac{R_1 R_f}{R_1 + R_f} \quad R_{comp} \text{ should be equal to } 11^{\text{th}} \text{ combination of resistors to invert}$$

INPUT OFFSET CURRENT:

Bias current compensation works if I_B^+ and I_B^- are equal. Since input transistors cannot be made identical, there will be some small difference between I_B^+ and I_B^- .

This difference is called offset current I_{OS} .

$$|I_{OS}| = I_B^+ - I_B^-$$

w.k.t., $V_I = I_B^+ R_{comp}$; $I_1 = \frac{V_I}{R_1}$

KCL at node 'a' [dia-puerto page]

$$I_2 = (I_B^- - I_1)$$

$$I_2 = I_B^- - \left(\frac{I_B^+ R_{comp}}{R_1} \right)$$

Again

$$I_2 = (I_B^- - I_1) = I_B^- - \left(\frac{I_B^+ R_{comp}}{R_1} \right) \times$$

$$V_o = I_2 R_f - V_F \approx I_2 R_f - I_B^+ R_{comp}$$

$$= (I_B^- - \left(\frac{I_B^+ R_{comp}}{R_1} \right) R_f) - (I_B^+ R_{comp})$$

Sub $R_{comp} = \frac{R_1 R_f}{R_1 + R_f}$ in above eqn & after manipulation

We get

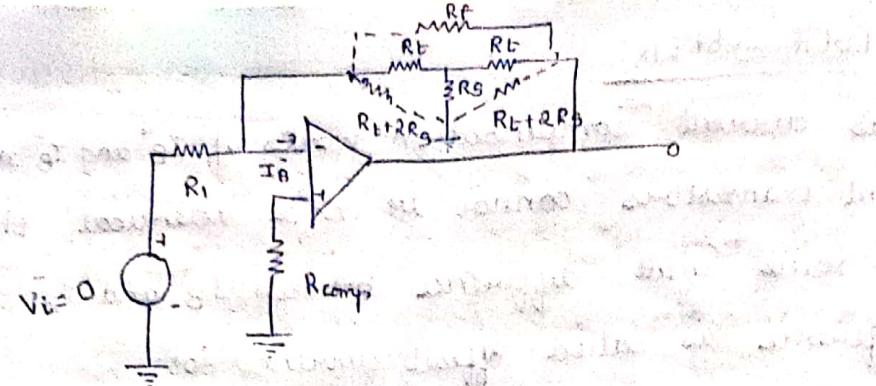
$$V_o = R_f \left[I_B^- - I_B^+ \right] = 0V$$

$$V_o = R_f I_{OS}$$

It can be seen from the eqn that effect of offset current can be minimized by keeping feedback resistance small. To keep input Imp high R_1 should be large, T feedback network is a good solution.

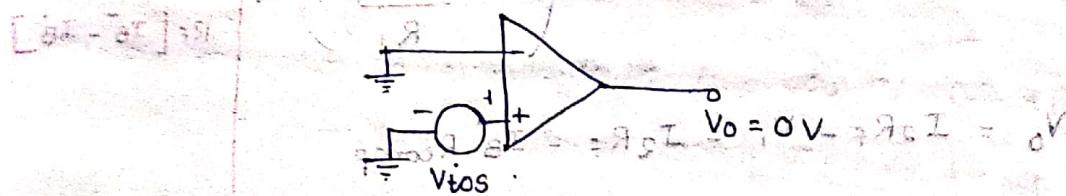
T network provides a feedback signal as if there were a single f/b resistor. Result R_f must be high.

T is good solution



INPUT OFFSET VOLTAGE:

It is found that output may still not be zero with zero input voltage. This is due to unavoidable imbalances in the op-amp and one may have to apply a small voltage at input terminals to make output voltage zero. This voltage is input offset voltage.



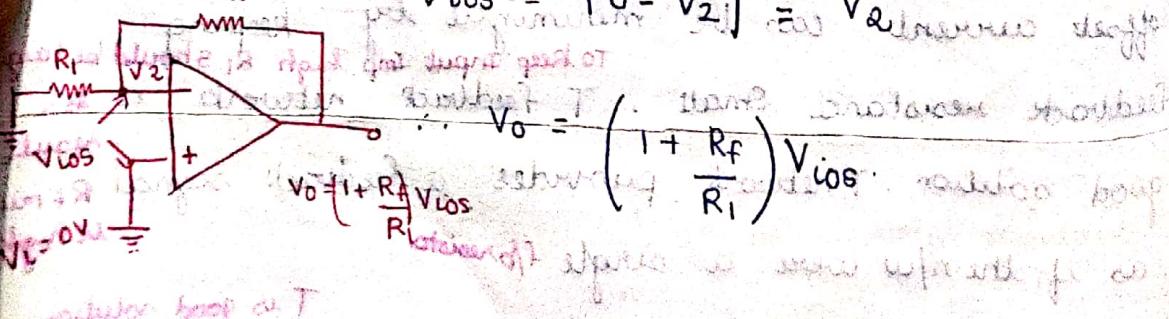
The voltage (V_2) at (-) input terminal is given by

$$V_2 = \left(\frac{R_f}{R_f + R_1} \right) V_o$$

$$\text{or } V_o = \left(\frac{R_1 + R_f}{R_f} \right) V_2 = + \left(1 + \frac{R_f}{R_1} \right) V_2$$

Since $V_{iOS} = |V_i - V_2|$ & $V_i = 0$

$$V_{iOS} = |0 - V_2| = V_2 \text{ (reverse sign)}$$



TOTAL OUTPUT OFFSET VOLTAGE

This can be either more or less than the offset voltage produced at the o/p due to input bias current or input offset voltage alone. This is because input offset voltage V_{ios} & input bias current I_B could be either positive or negative w.r.t. ground. Therefore maximum offset voltage at o/p with out any compensating techniques used is given by:

$$V_{OT} = \left(1 + \frac{R_f}{R_i}\right) V_{ios} + R_f I_B$$

with R_{comp} , - the total o/p offset voltage will be

$$V_{OT} = \left(1 + \frac{R_f}{R_i}\right) V_{ios} + R_f I_{os}$$

THERMAL DRIFT:

Bias current, offset current & offset voltage change with Temperature: A circuit carefully nulled at $25^\circ C$ may not remain so when the temperature rises to $35^\circ C$. This is called drift.

careful printed circuit board layout must be used to minimize effect of drift.

so the first step is to make layout as follows:

- PCB layout as per requirement with no vias or pads
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AC CHARACTERISTICS

when only ac signal is present, the primary design consideration is determined by noise & frequency response. For large ac signal slew rate limiting characteristics decides whether distortion will be introduced or not.

The ac response characteristics to be studied are

- (i) Frequency response
- (ii) Bandwidth
- (iii) Slew rate

Frequency response

Gain is assumed to be constant. But

practically any change in operating frequency causes variation in gain. Op-amp should have infinite bandwidth. If open loop gain is specified

as a particular value, it must remain. Same is found audio & high radio freq ranges. The gain of practical op-amp decreases or rolls off at higher frequencies. This is due to capacitive component

included in equivalent circuit of op-amp.

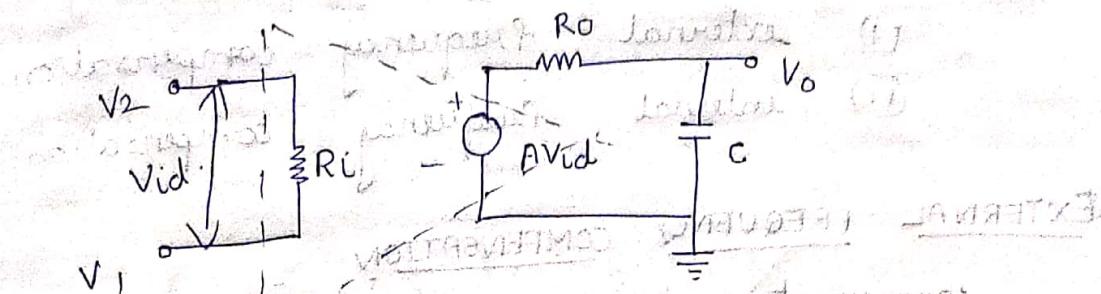
Two major sources can be considered responsible for this capacitive component

(i) G.C's contain junction capacitors. They act as open circuits at low frequencies and as reactive paths at higher frequencies. As freq \uparrow reactance \downarrow .

(ii) Internal conductors of op-amp with transistors resistors & capacitors integrated on same substrate

introduces parasitic or stray capacitances.

The combined effect of these capacitances reduces the gain of op-amp at high freq.



Bandwidth

Bandwidth is defined as range of frequencies within which gain remains constant. Gain & b/w product of an op-amp is always constant.

Gain & b/w are inversely proportional to one another. b/w can be ↑ by providing f/b signal to its input.

Slew rate

Slew rate limits the b/w for large signals. It indicates how fast the o/p voltage can change.

Slew rate of op-amp is related to its frequency response.

Op-amps with wide b/w have better slew rates.

Slew rate limiting affects all amplifiers where capacitance on internal nodes or as part of external load has to be charged & discharged as voltage levels vary.

FREQUENCY COMPENSATION

When To achieve wider b/w & limited closed-loop gain, compensation techniques are required. Two types of compensation techniques used are:

- (i) External frequency compensation
- (ii) Internal frequency compensation

EXTERNAL FREQUENCY COMPENSATION

compensating n/w is connected externally to op-amp. It alters the response so that -20 dB/decade of roll-off rate is achieved over broad range of freq.

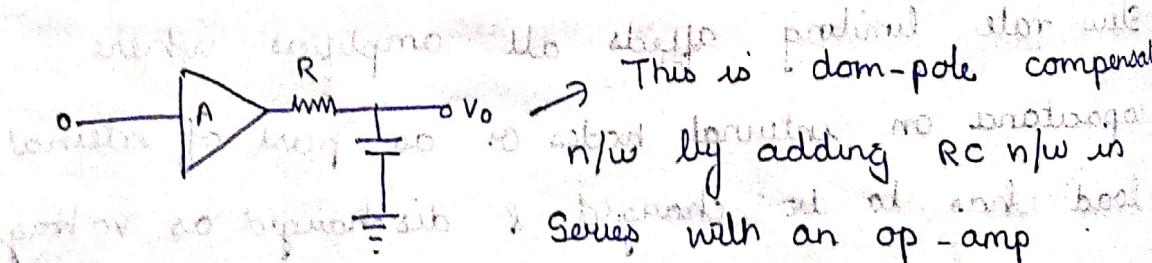
The commonly used external compensation methods are:

- (i) dominant pole compensation
- (ii) pole-zero compensation
- (iii) Miller effect compensation

Dominant pole compensation

uncompensated transfer fn of op-amp is given by

$$A_f = \frac{A_0 \omega_1 \omega_2 \omega_3}{(s + \omega_1)(s + \omega_2)(s + \omega_3)}$$



or it can be achieved by connecting capacitor C at high resistance node with respect to ground

compensated Transfer fn A' is given by

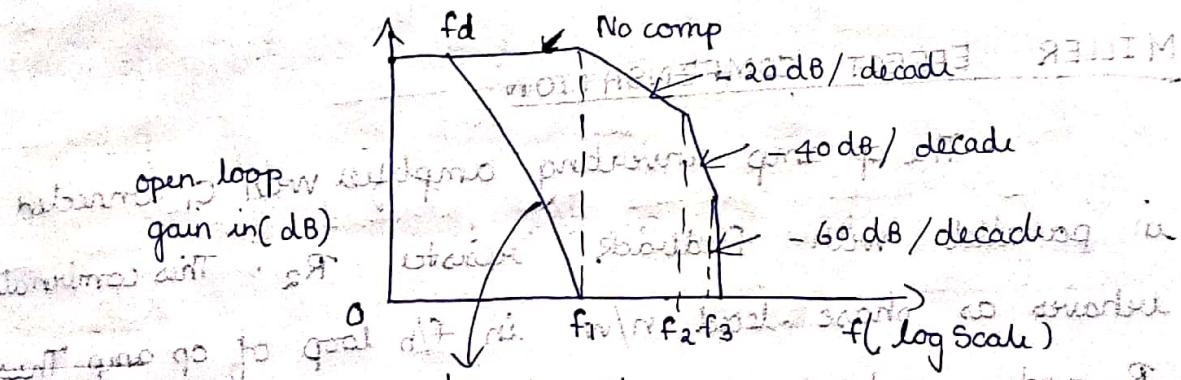
$$A' = \frac{V_o}{V_i} = A_0 \left(\frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \right) = \frac{A_0}{1 + j(f/f_d)} \quad \text{where } f_d = \frac{1}{2\pi R C}$$

so break freq. of compensating n/w .
using eqn ① we get compensated Transfer fn as

$$A' = \frac{A_0}{\left(1 + j\frac{f}{f_d} \right) \left(1 + j\frac{f}{f_1} \right) \left(1 + j\frac{f}{f_2} \right) \left(1 + j\frac{f}{f_3} \right)} \quad \text{where } f_d < f_1 < f_2 < f_3$$

Advantage is improved noise immunity

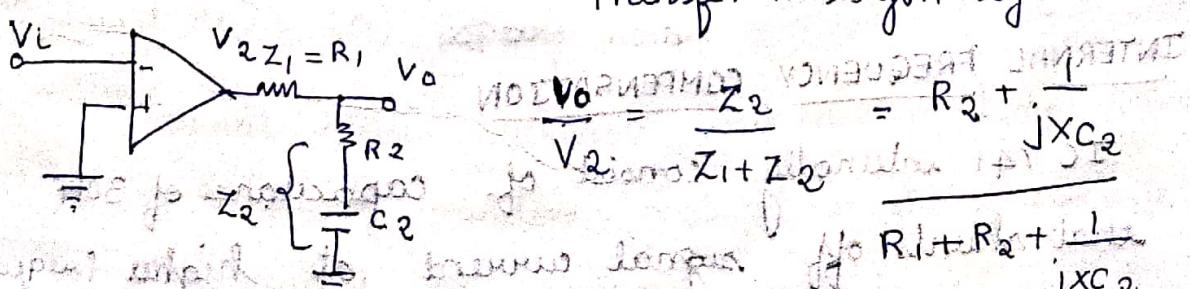
disadvantage is b/w reduces drastically



A' passes through 0dB at frequency f_1
pole-Zero compensation

Here both pole and a zero are added to the uncompensated transfer fn. Zero is added at a higher frequency than pole.

Transfer fn is given by.

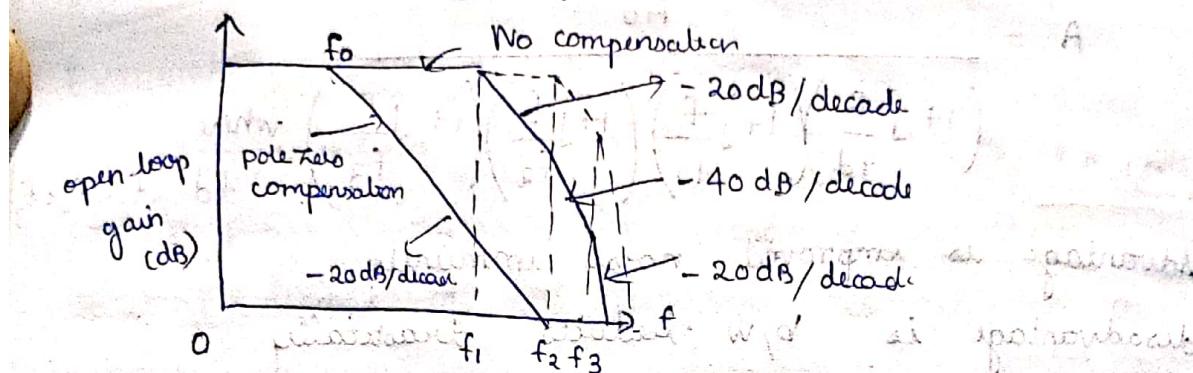


$$= \frac{1 + j\omega R_2 C_2}{1 + j\omega(R_1 + R_2)C_2} = \frac{1 + j(f/f_1)}{1 + j(f/f_0)}$$

$$= \frac{1 + j\omega(R_1 + R_2)C_2}{1 + j(f/f_0)}$$

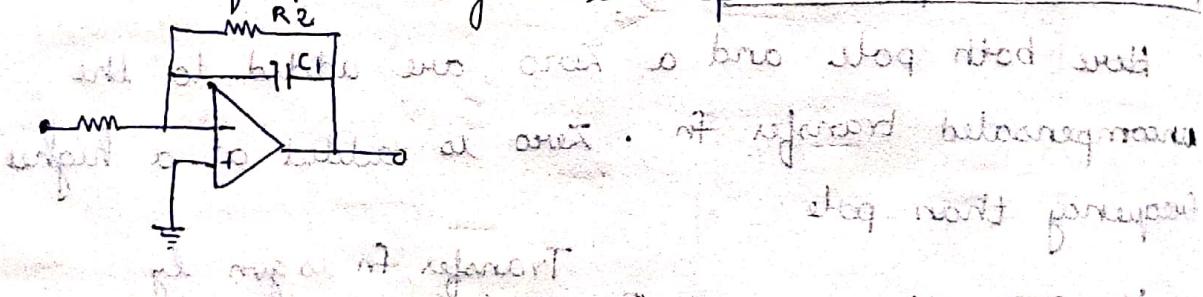
$$\text{where } f_1 = \frac{1}{2\pi(R_1 + R_2)C_2}; f_0 = \frac{1}{2\pi(R_1 + R_2)C_2}$$

compensating n/w is designed to produce a zero at first corner freq of uncompensated transfer function. This zero will cancel effect of pole at f_1 . Pole of compensating n/w at $f_0 = \frac{\omega_0}{2\pi}$ is selected so that A' passes through 0dB at second corner frequency f_2



MILLER EFFECT COMPENSATION

The op amp inverting amplifier with C_1 connected in parallel with feedback resistor R_2 . This combination behaves as phase-lead in/n/w in f/b loop of op amp. Thus R_1 and C_1 introduces a phase lead to cancel some amount of phase lag in the loop.



INTERNAL FREQUENCY COMPENSATION

IC 741 internally consists of a capacitance of 30PF that shunts off signal current at higher frequencies leading to decrease in output signal.

Internal compensating capacitor causes open loop gain to roll off at -20 dB/decade rate that assures stability.

NOISE

It is major source of interference, and it is undesirable electrical signals present on desired o/p. Any unwanted signal is noise and it is random in nature. Drift and offset can be considered as noise of very low frequency. Noise can be categorised as:

- (i) Internal or self induced
- (ii) external or man made

Internal noise is caused by random voltage of ac signals, switching of other circuit nodes. Amount of noise is determined by rate of change of current & voltage, freq of operation and type of coupling.

External noise sources are electrical devices and their controls. Natural phenomena such as lightning may also be an external noise source.

NOISE IN OP-AMP CIRCUITS

Common types of noise factors are

- (i) Thermal noise
- (ii) shot noise
- (iii) $1/f$ noise or flicker noise
- (iv) Burst noise (a) popcorn noise

Thermal noise increases with rise in temperature and it is result of random motion of charge carriers.

Shot noise is induced due to discrete nature of current flow in device.

Flicker noise or $1/f$ noise increases with decrease in frequency.

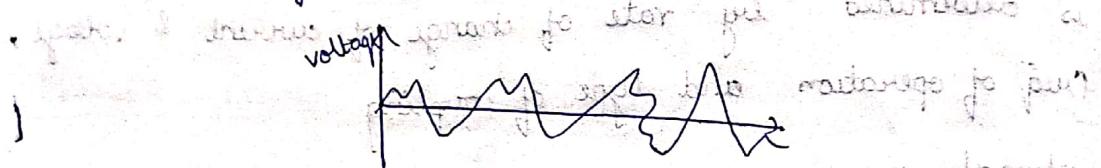
Pop corn noise results from sudden change in input bias current usually at freq less than 100 Hz, which is due to imperfect S/C surface conditions.

These sources combined to form net cumulative noise which are classified as

(i) white noise

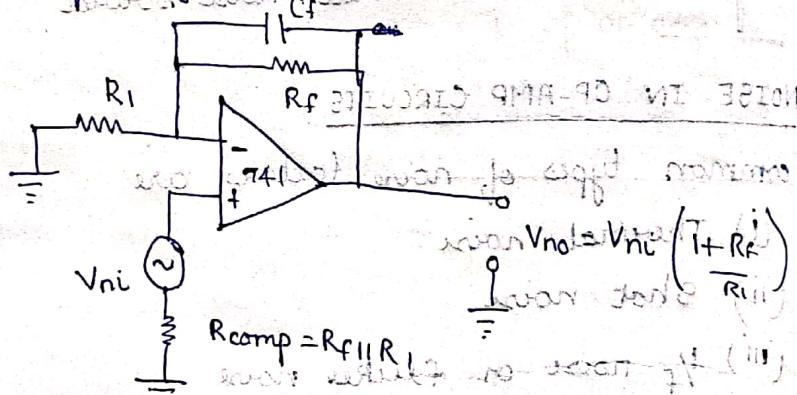
(ii) flicker noise based on freq distn

White noise has its frequency spectrum constant over a very wide b/w



It is random process with erratic behaviour with no pattern or rule.

Noise model is given by



RMS noise voltage at o/p is given by (i) even law

$$V_{no} = K_n V_{ni}$$

where K_n is noise gain

$$K_n = 1 + \frac{R_f}{R_1}$$

To minimize noise

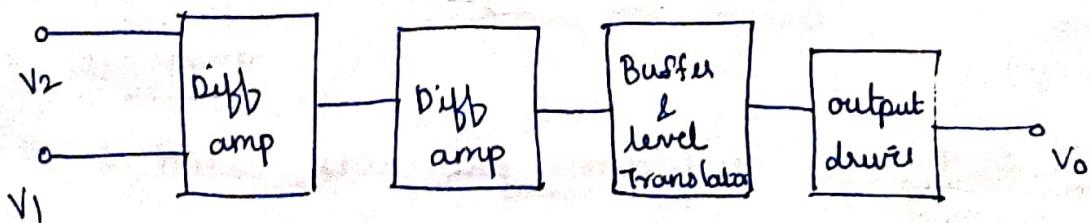
(i) Avoid large values of R_f & R_1

- (ii) place small capacitor of value 3pF across R_1 to shunt it for high noise freq
- (iii) do not connect any capacitor across R_1 , since at high freq R_{ic} will generate smaller impedance & gain will tend to \uparrow with freq which will further aggregate noise effect
- physical shielding of ICs helps to prevent external electromagnetic radiation from introducing noise

GENERAL DESCRIPTION

- (i) $\mu\text{A}741$ is internally compensated op-amp
- (ii) It is monolithic IC, fabricated using planar epitaxial process
- (iii) It has internal short circuit protection
- (iv) It is used for integrators, differentiators, adder, subtractor, voltage follower or buffer
- (v) It consumes low power

OPERATIONAL AMPLIFIER INTERNAL CIRCUIT:



first two stages are cascaded to provide high gain and high input resistance.

Third stage acts as a buffer as well as level shifter

The buffer is usually an emitter follower whose input impedance is very high so that it prevents loading of high gain stage. The level shifter adjusts the dc voltages so that output voltage is zero for zero inputs. The adjustments of dc level is required as the gain stages are direct coupled. As it is not possible to fabricate large values of capacitors, all IC's are direct coupled usually.

The o/p stage is designed to provide low output impedance. The o/p voltage should swing w.r.t. ground. To allow such swing amplifier is provided with +ve & -ve supply voltages. Additionally op amp incorporates circuitry to provide drift compensation and frequency compensation.