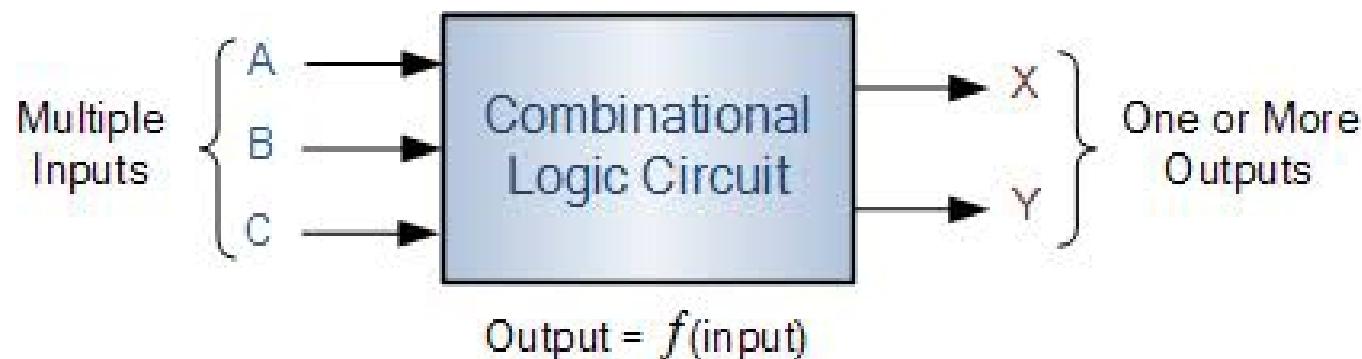


Unit - 4

Flip Flops

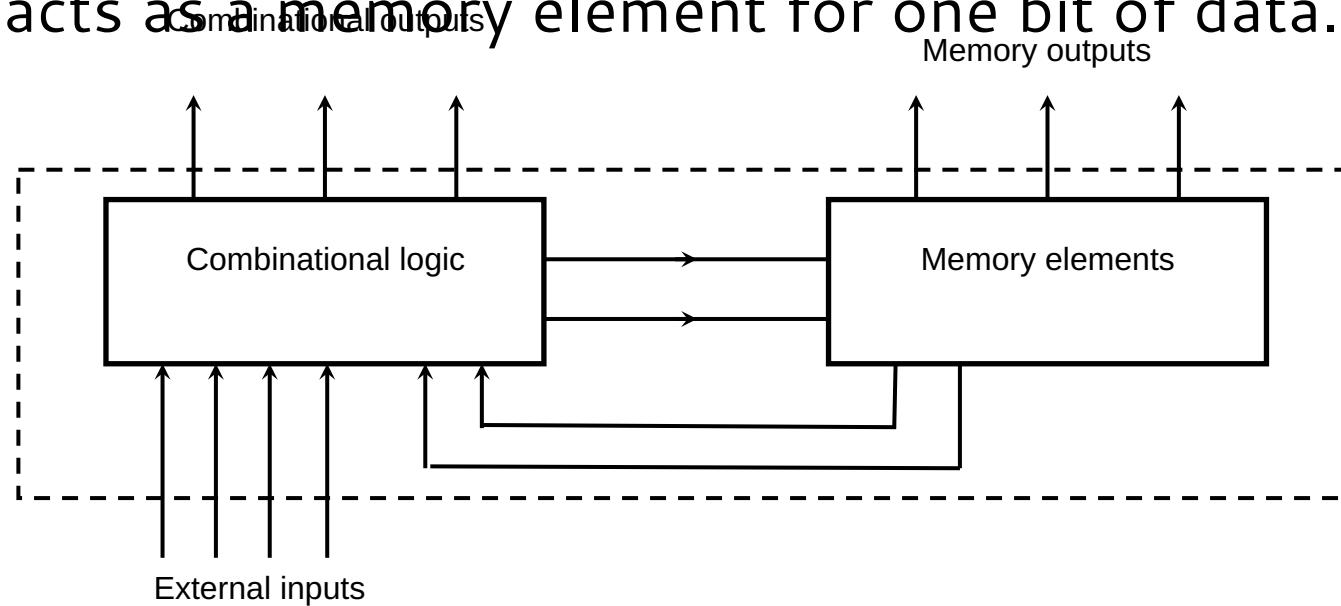
Combinational Logic

- The outputs depend only on the state of the inputs all of the time. Any change in the state of one of the inputs will ripple through the circuit immediately.
 - Examples of combinational logic are NAND and NOR gates, Inverters, and Buffers. These four logic gates form the basis of almost all combinational logic circuits as well as **flip flops**.



Sequential Logic

- Has **memory**; the circuit stores the result of the previous set of inputs. The current output depends on inputs **in the past** as well as present inputs.
 - The basic element in sequential logic is the **bistable latch** or **flip-flop**, which acts as a **memory** element for one bit of data.



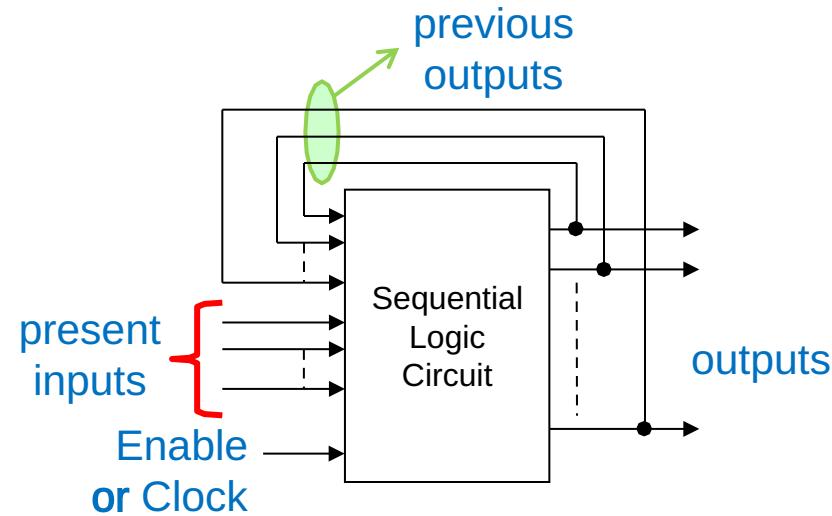
Sequential circuit = Combinational logic + Memory Elements

Digital Circuits

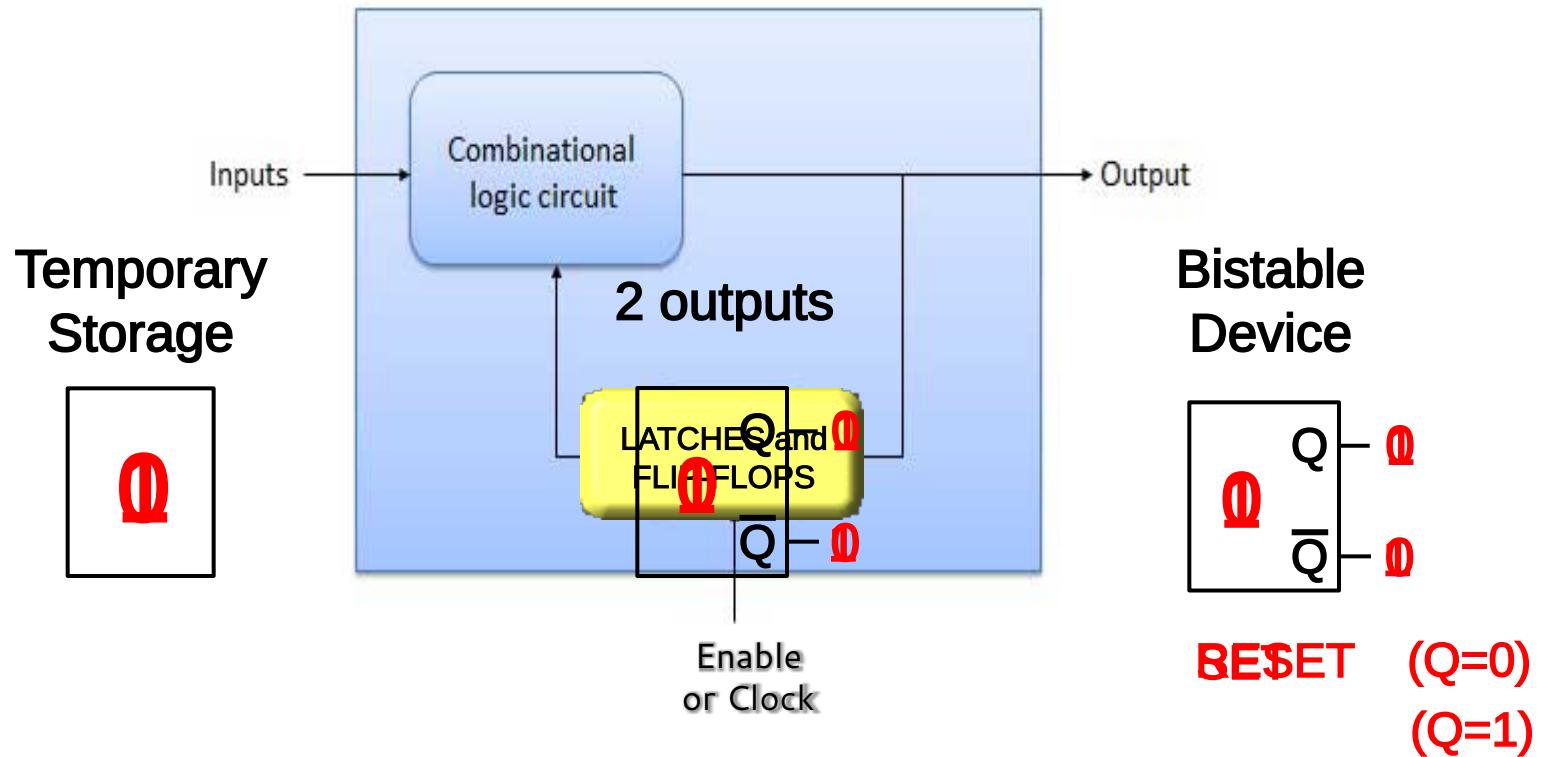
Combinational Logic Circuit

- output depends on present inputs
- consisted of logic gates and combinational logic subsystems (multiplexer, etc)

Sequential Logic Circuit



- output depends on present inputs and previous outputs
- enable or clock signal is used to synchronize the output change with time



Some Applications:

1	1	0	1
---	---	---	---

Memory

0	0	0	0
---	---	---	---

Counters

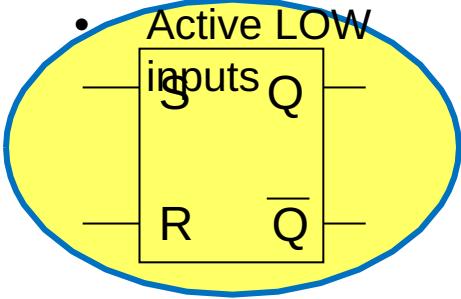
1	→	0	0	1	0
---	---	---	---	---	---

Shift Register
-cover in DF2

Latches

§ SR Latch

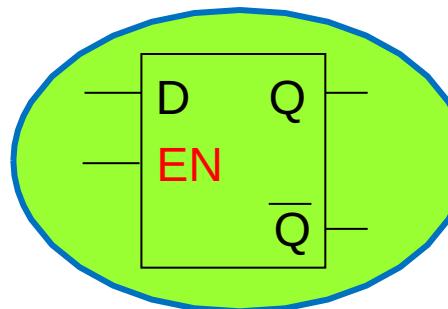
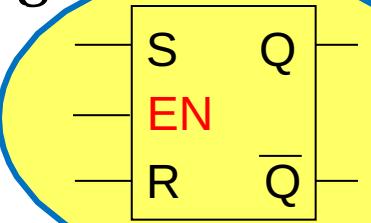
- Active HIGH inputs
- Active LOW inputs



Gated Latches

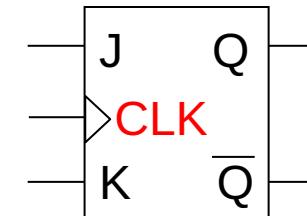
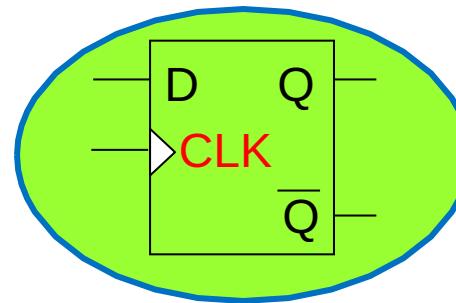
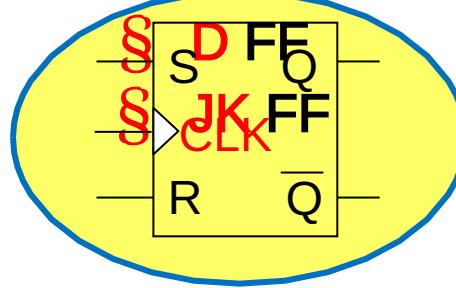
§ Gated SR Latch

§ Gated D Latch



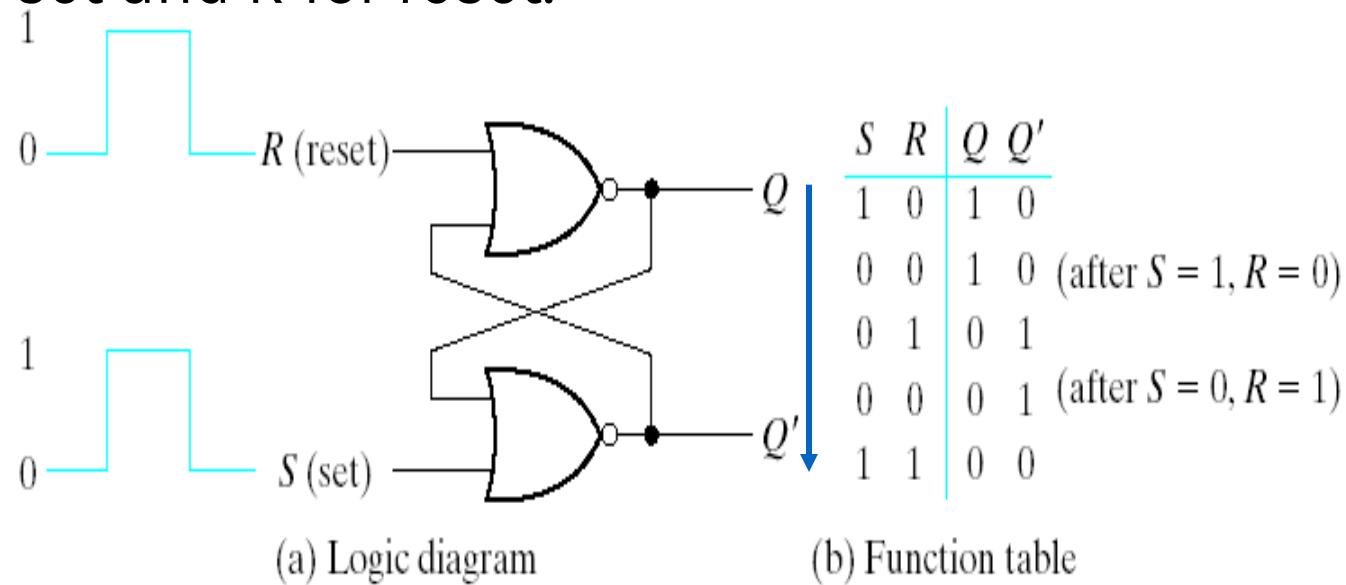
Flipflops (FF)

§ SR FF



Latches --SR Latch

The **SR latch** is a circuit with two cross-coupled **NOR gates** or two cross-coupled **NAND gates**. It has two inputs labeled S for set and R for reset.



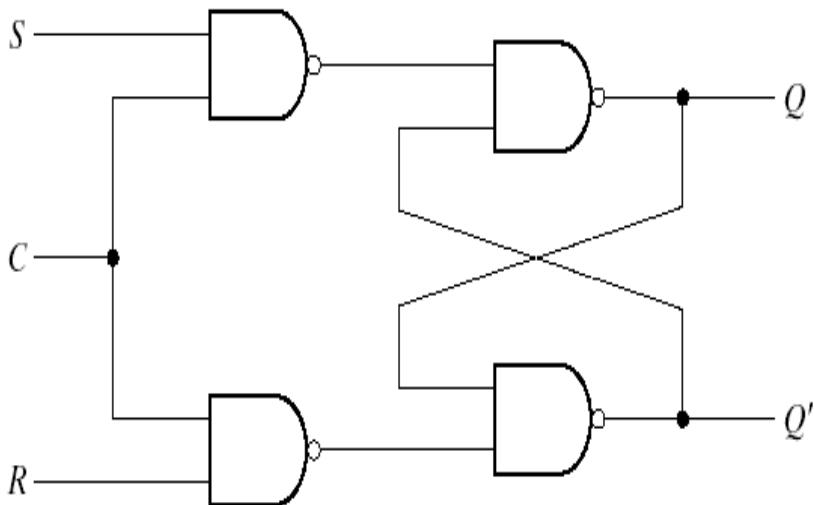
(a) Logic diagram

(b) Function table

Fig. 5-3 SR Latch with NOR Gates

SR Latch with Control Input

The operation of the basic SR latch can be modified by providing an additional control input that determines when the state of the latch can be changed. In Fig. 5-5, it consists of the **basic SR latch** and **two additional NAND gates**.



(a) Logic diagram

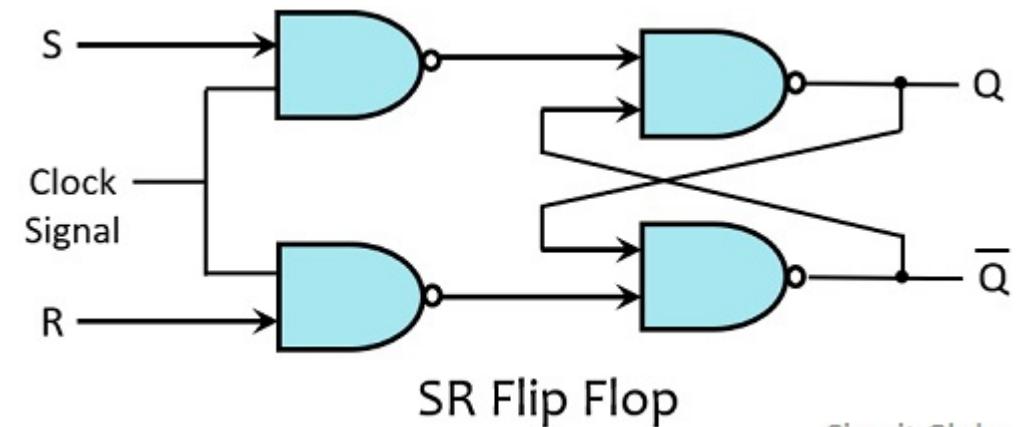
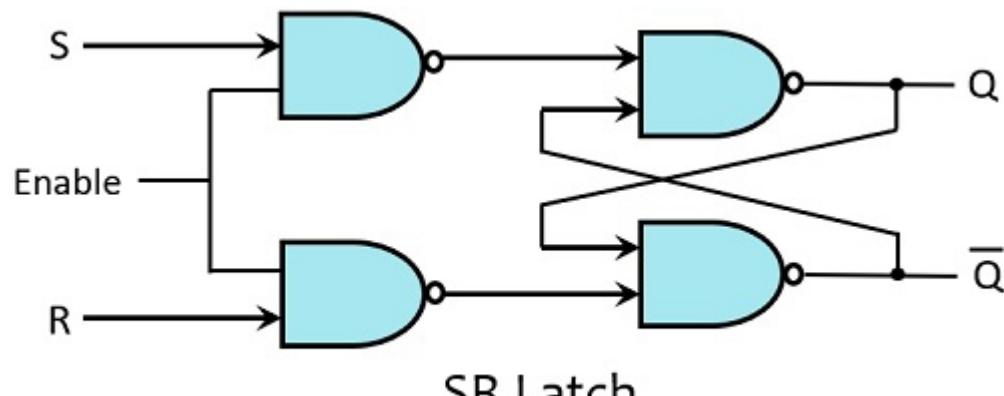
C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

Fig. 5-5 SR Latch with Control Input

Flip Flops Vs Latches

- A flip flop is an electronic circuit with two stable states that can be used to store binary data.
- The stored data can be changed by applying varying inputs.
- **Latches and flip-flops** are circuit elements whose output depends not only on the current inputs, but also on previous inputs and outputs.
- **The difference between a latch and a flip-flop is that a latch does not have a clock signal, whereas a flip-flop always does.**



Circuit Globe

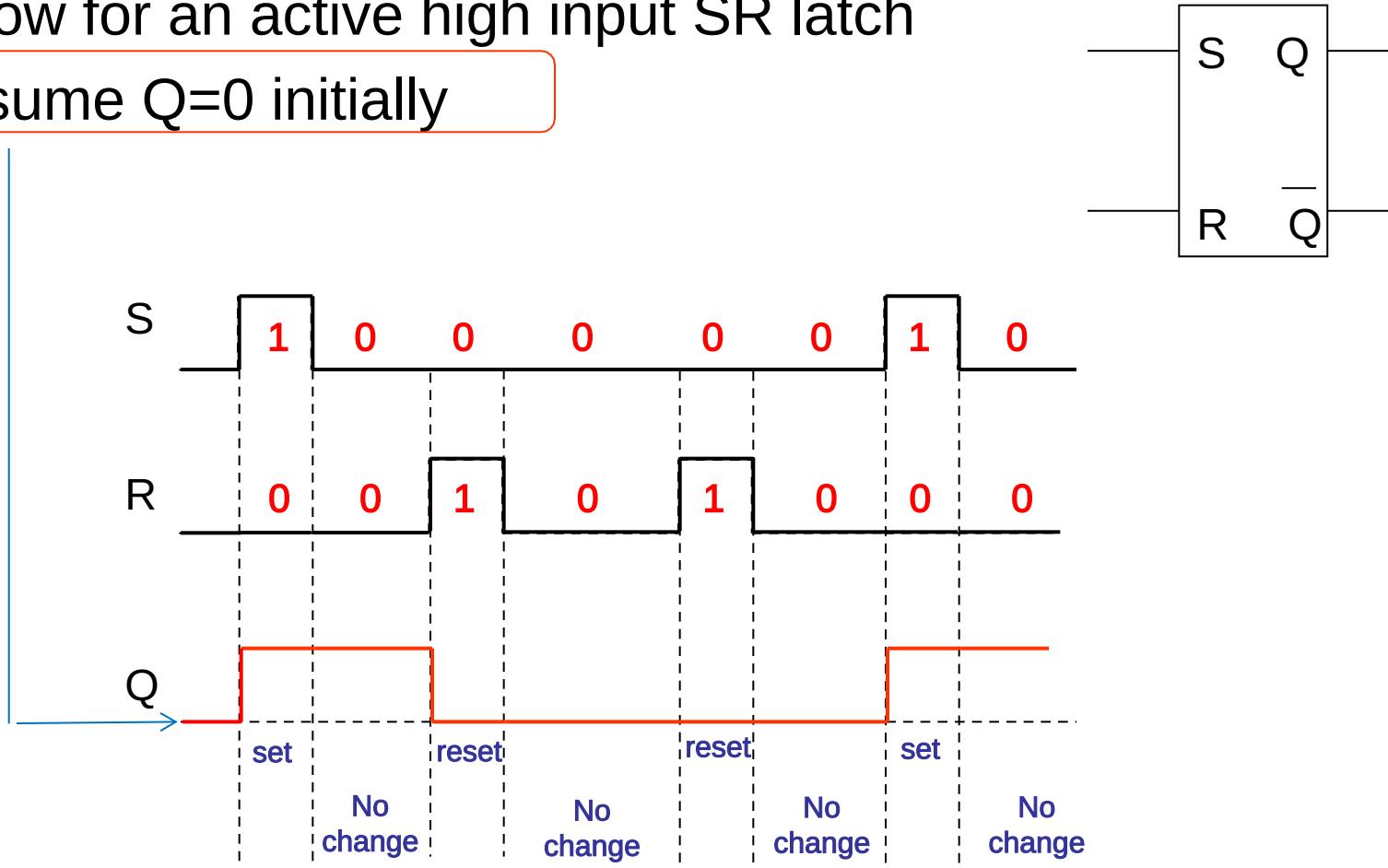
Circuit Globe

Latch VS Flipflop

Latches	Flip Flops
Latches are building blocks of sequential circuits and these can be built from logic gates	Flip flops are also building blocks of sequential circuits. But, these can be built from the latches.
Latch continuously checks its inputs and changes its output correspondingly.	Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal
The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on	Flipflop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip flops are used as a register.
It is based on the enable function input	It works on the basis of clock pulses
It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.	It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.

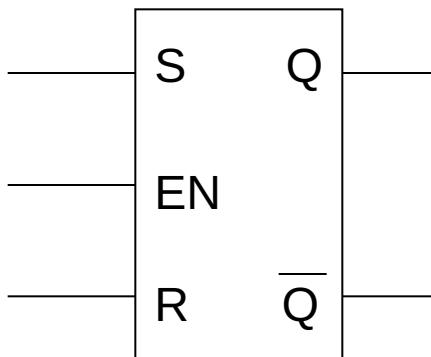
Exercise 1

- Draw the output waveform for the S, R inputs shown below for an active high input SR latch
- Assume Q=0 initially

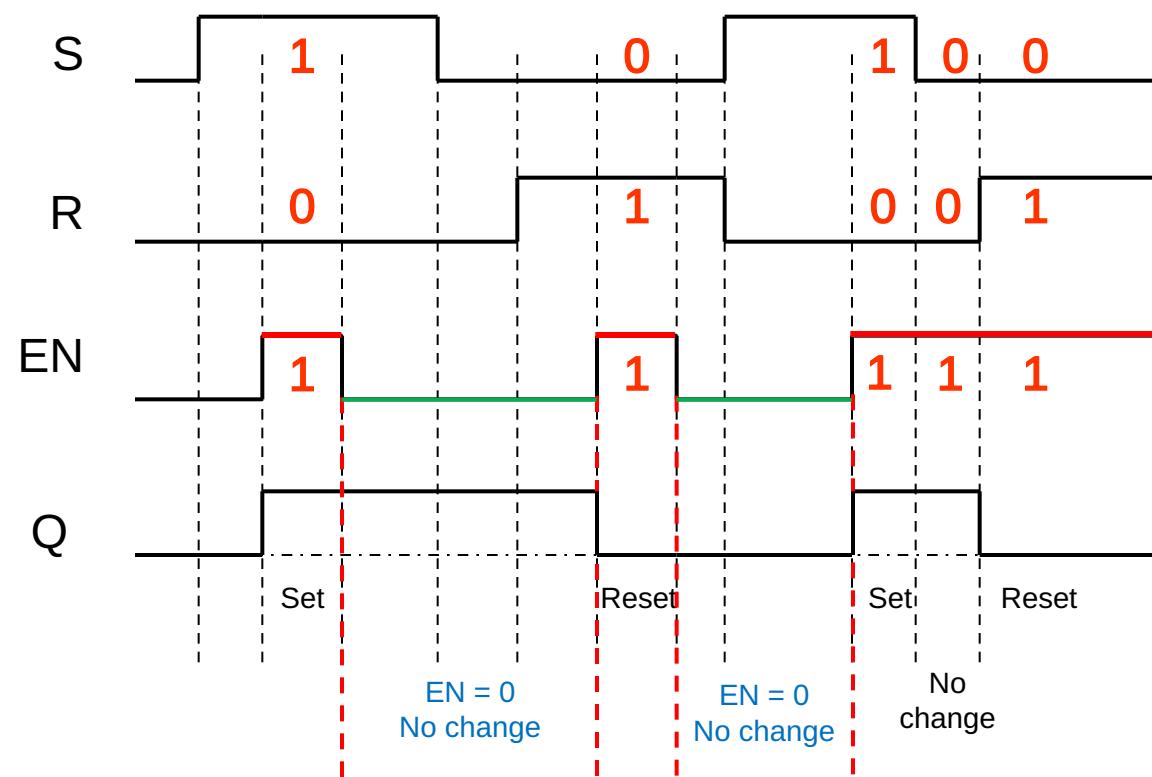


Gated Latches

1. Gated SR Latch



EN	S	R	Q
0	x	x	No change
1	0	0	No change
1	0	1	0 (Reset)
1	1	0	1 (Set)
1	1	1	Invalid



Assume Q=0 initially

Flipflops

q A Flip Flop is a memory element that is capable of storing one bit of information.

v A flip flop can maintain a binary state for an unlimited period of time as long as-

- (i) Power is supplied to the circuit.
- (ii) or until it is directed by an input signal to switch states

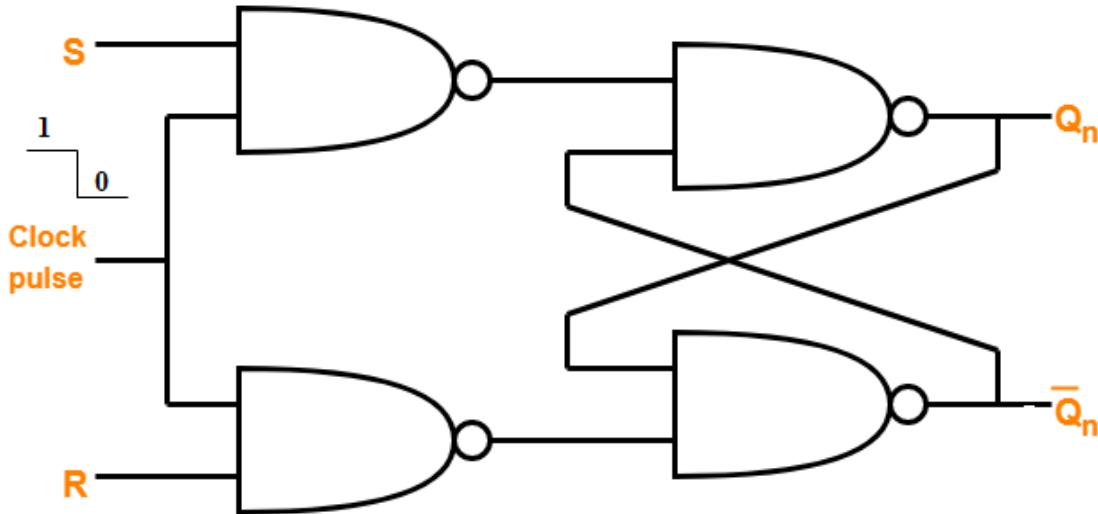
Types of Flipflops

- SR Flip Flop
- JK Flip Flop
- D Flip Flop

Steps to design of Flipflops

- Circuit diagram using universal gates
- Truth Table
- Characteristics Equation
- Excitation Table
- State Diagram
- Timing (or) Switching (or) Waveform Diagram

S-R Flip flop



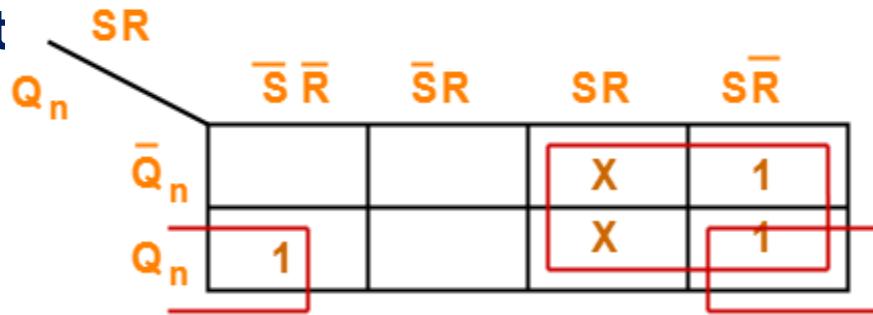
(i) Circuit
diagram

(ii) Truth
Table

C	S	R	Q_n	Q_{n+1}	State of Operation
1	0	0	0	0	hold
1	0	0	1	1	
1	0	1	0	0	clear (reset)
1	0	1	1	0	
1	1	0	0	1	set
1	1	0	1	1	
1	1	1	0	?	indeterminate
1	1	1	1	?	— avoid

(iii) Characteristic Equat

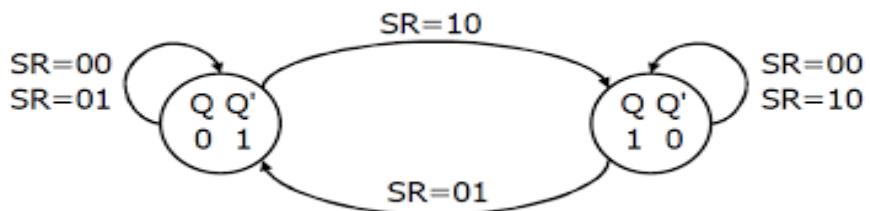
$$Q_{n+1} = S + Q_n R'$$



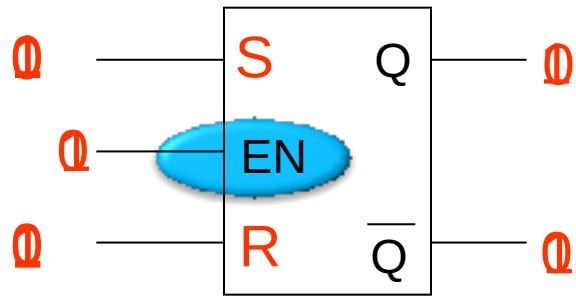
(iv) Excitation Table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

(v) State Diagram



Gated Latch

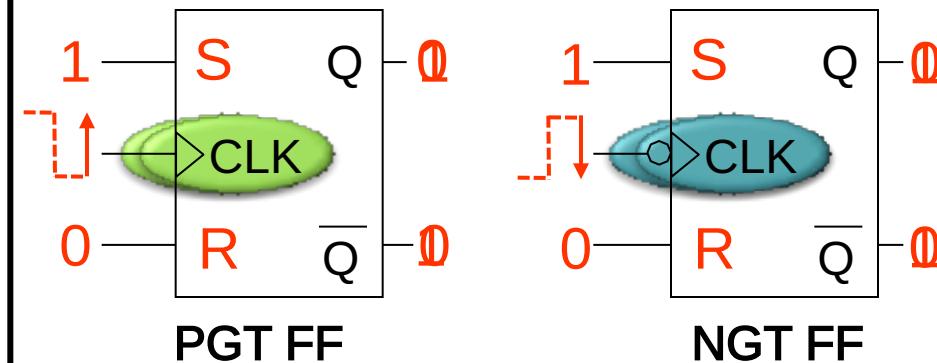


Level enabled

EN = 1, normal latch operation

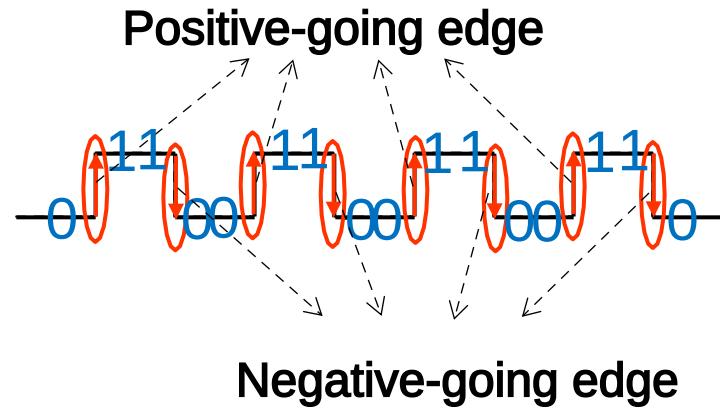
EN = 0, no change in output even
when inputs change

Flip-flop



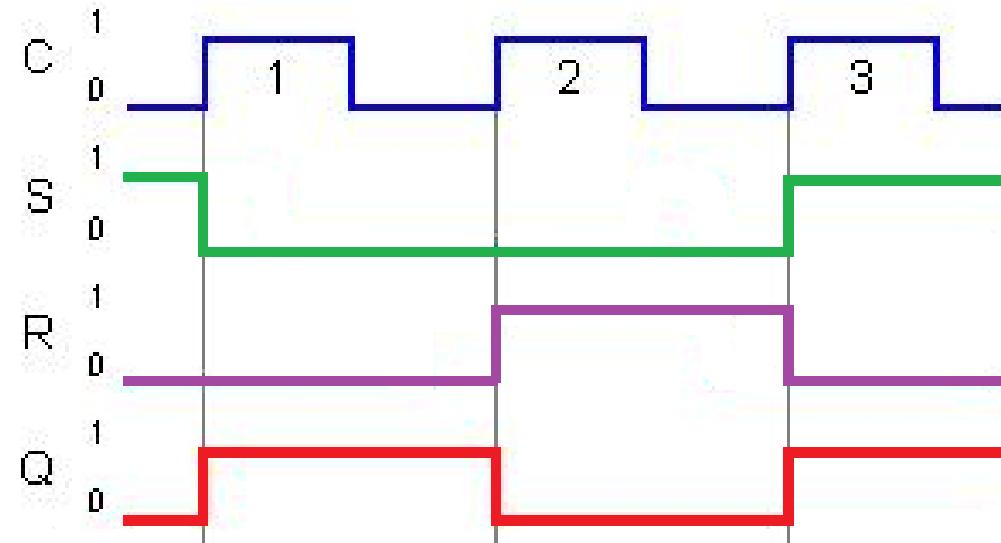
Edge-triggered

CLOCK (CLK) signal



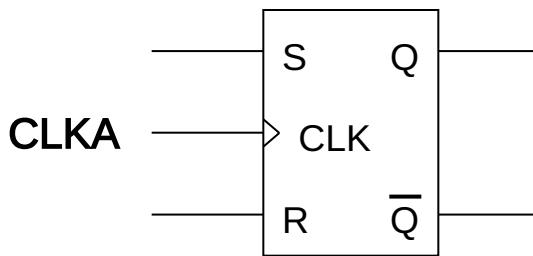
(V) Timing (or) Switching (or) Waveform Diagram

When $Q_n=1$

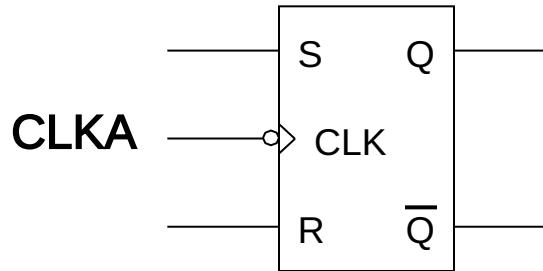
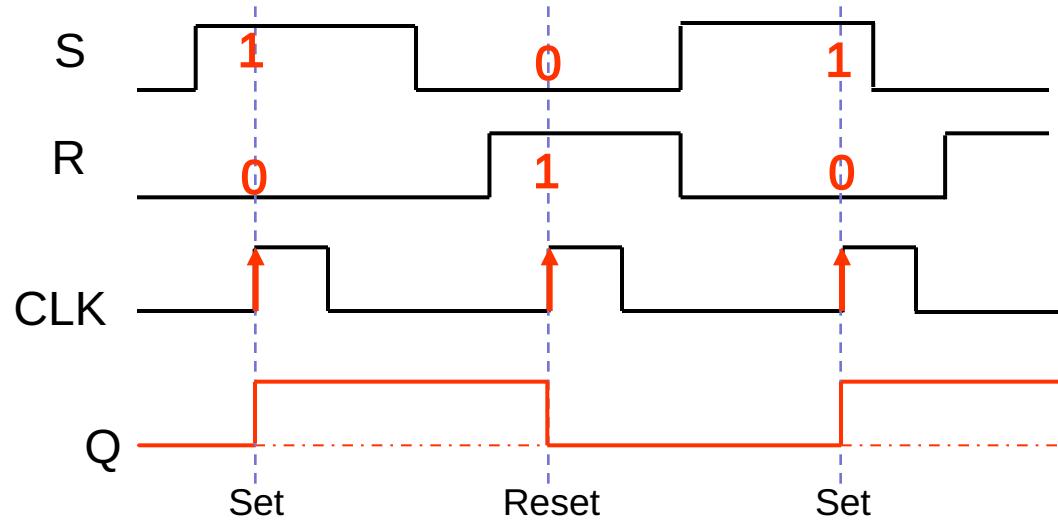


C	S	R	Q_n	Q_{n+1}
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	?
1	1	1	1	?

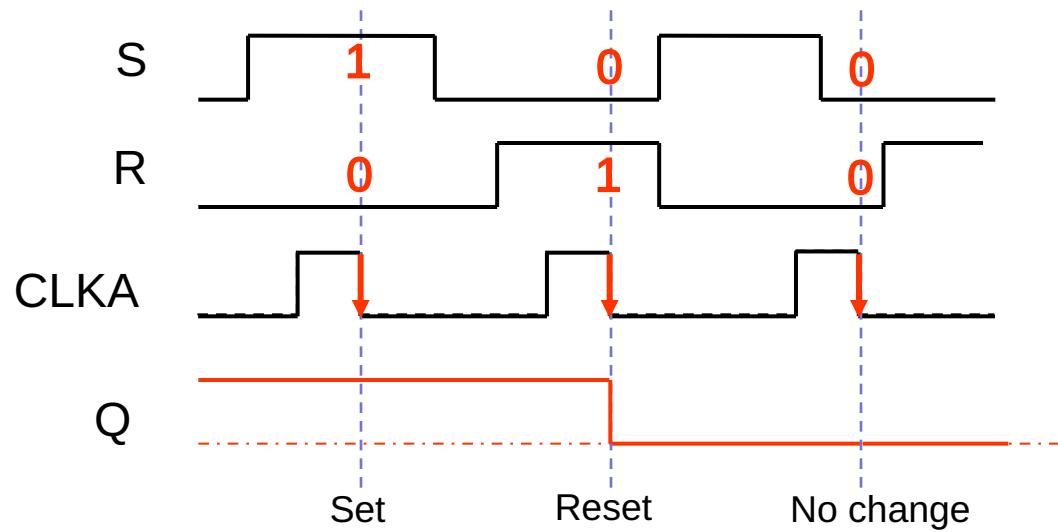
Complete the timing diagrams shown below



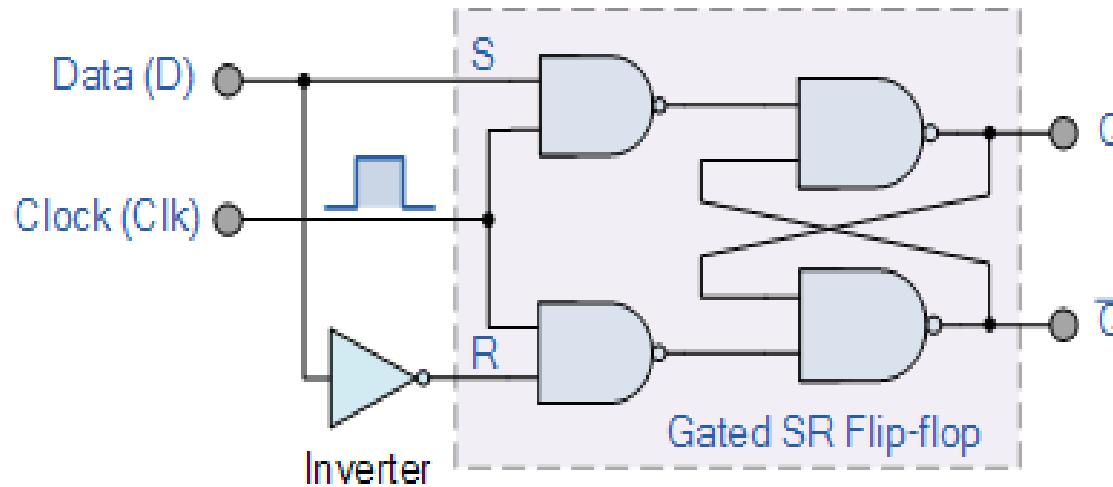
Assume Q=0 initially



Assume Q=1 initially



D - Flip flop



(i) Circuit
diagram

(ii) Truth
Table

C	D	Q_n	Q_{n+1}	State of Operation
1	0	0	0	Clear (reset)
1	0	1	0	
1	1	0	1	
1	1	1	1	Set

(iii) Characteristic Equation

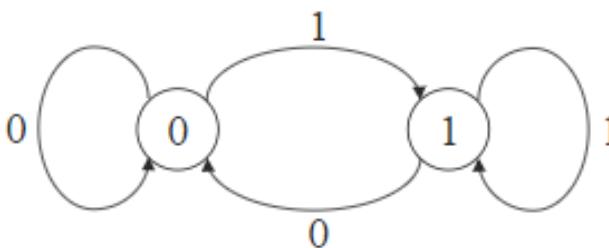
$$Q_{n+1} = D$$

	$Q_{n'}$	Q_n
D'	0	0
D	1	1

(iv) Excitation Table

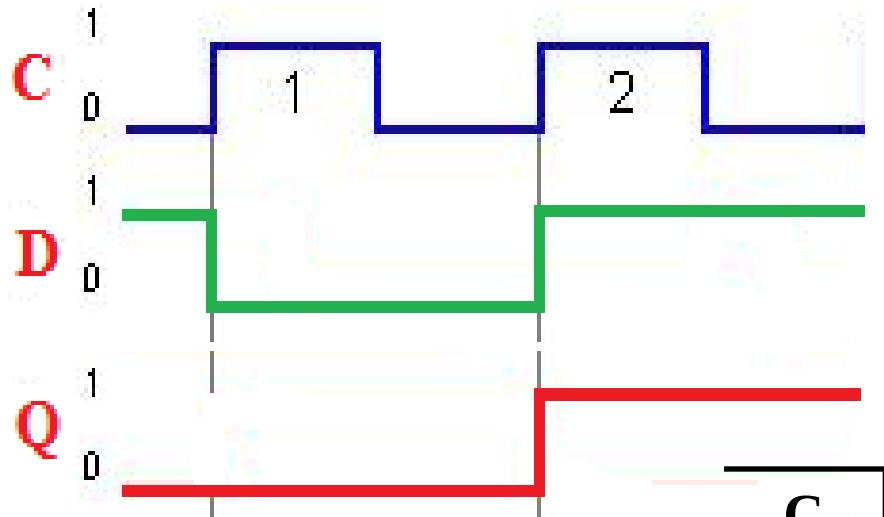
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

(v) State Diagram



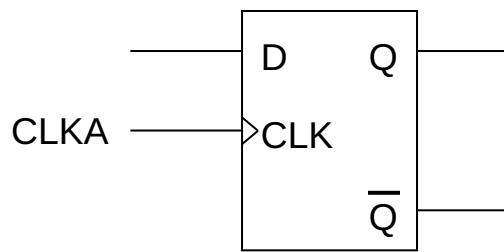
(V) Timing (or) Switching (or) Waveform Diagram

When $Q_n=1$

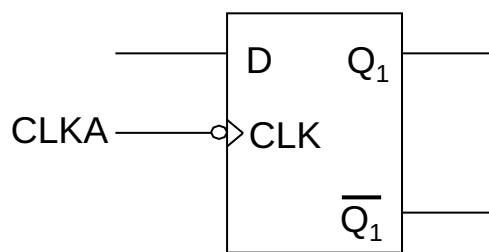
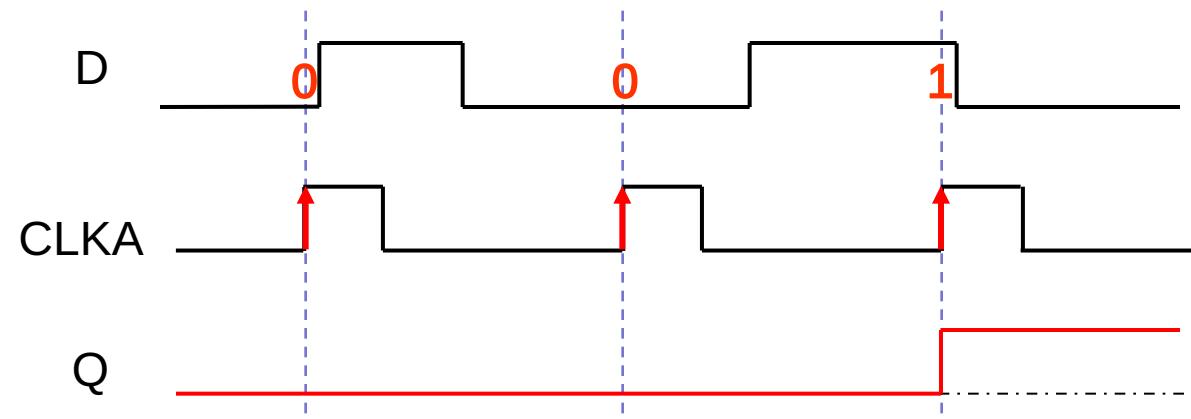


C	D	Q_n	Q_{n+1}	State of Operation
1	0	0	0	Clear (reset)
1	0	1	0	
1	1	0	1	
1	1	1	1	Set

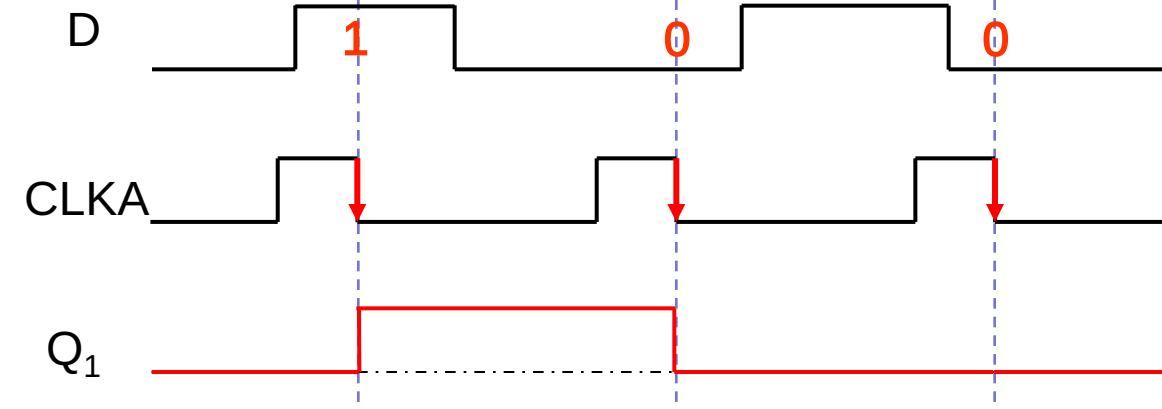
Complete the timing diagrams shown below



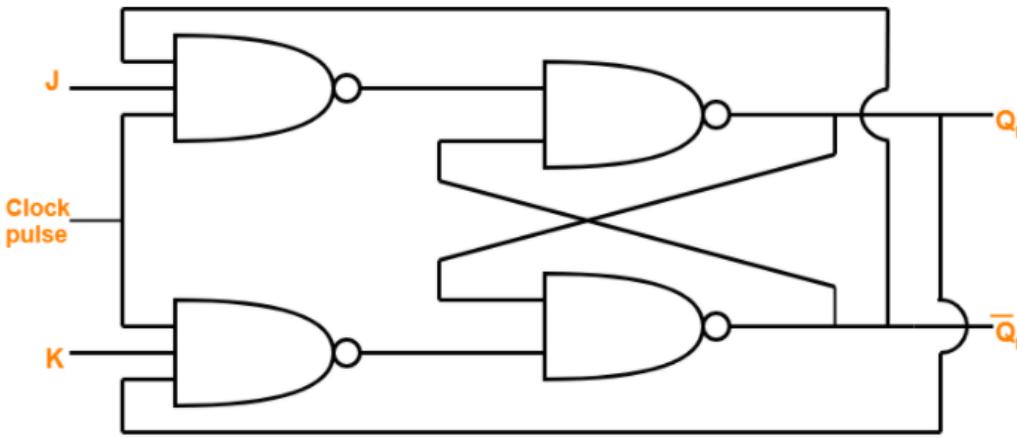
Assume Q=0 initially



Assume $Q_1=0$ initially



J-K Flip flop



(i) Circuit diagram

(ii) Truth Table

C	J	K	Q_n	Q_{n+1}	State of Operation
1	0	0	0	0	hold
1	0	0	1	1	
1	0	1	0	0	clear (reset)
1	0	1	1	0	
1	1	0	0	1	set
1	1	0	1	1	
1	1	1	0	1	Toggle
1	1	1	1	0	

(iii) Characteristic Equat

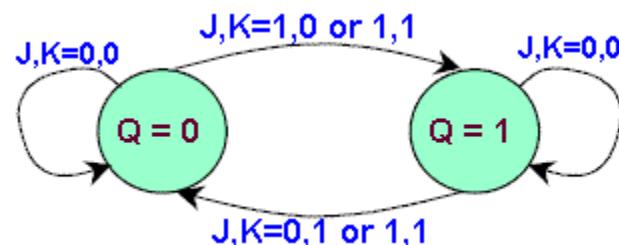
$$Q_{n+1} = Q'_n J + Q_n K'$$

Q_n	$\bar{J}K$	$\bar{J}K$	JK	$J\bar{K}$
\bar{Q}_n			1	1
Q_n	1			1

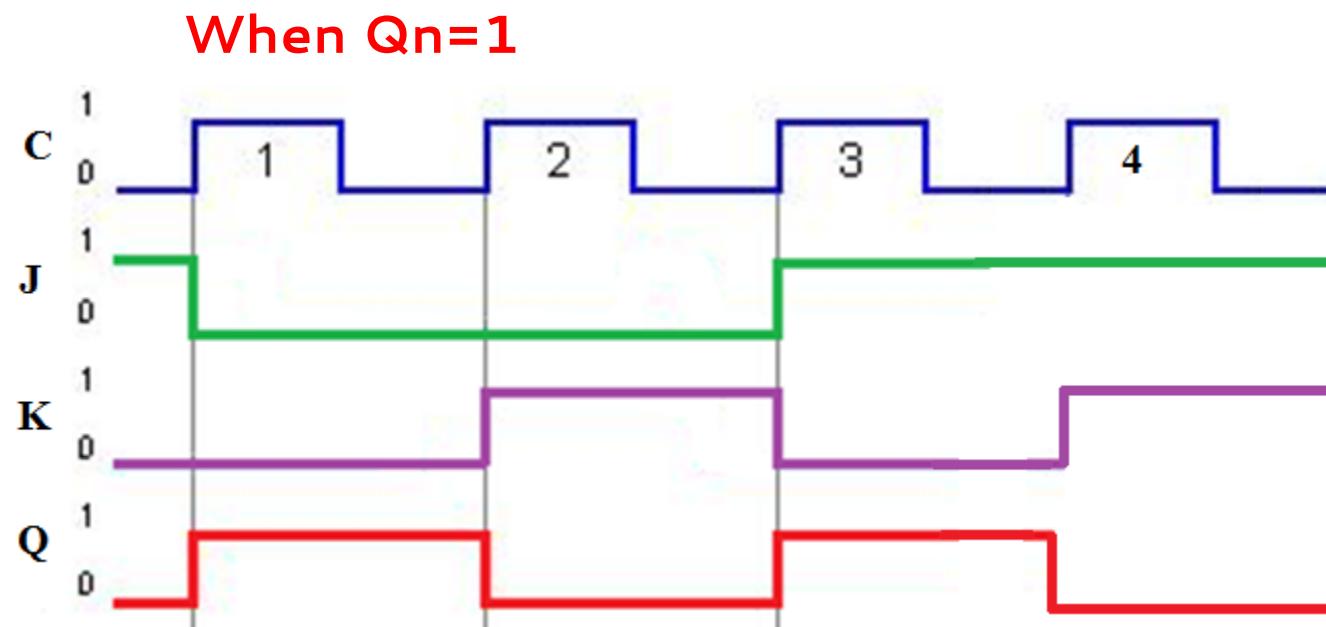
(iv) Excitation Table

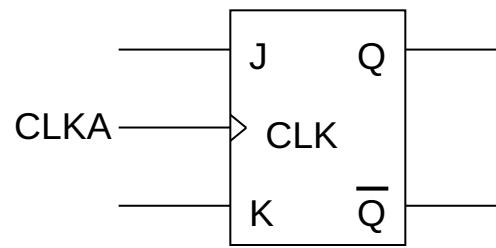
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(v) State Diagram

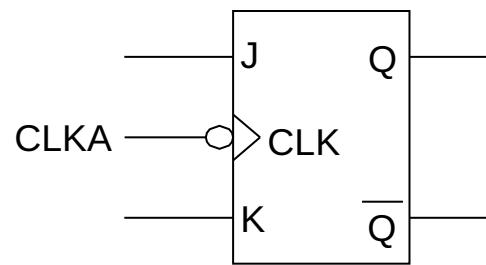
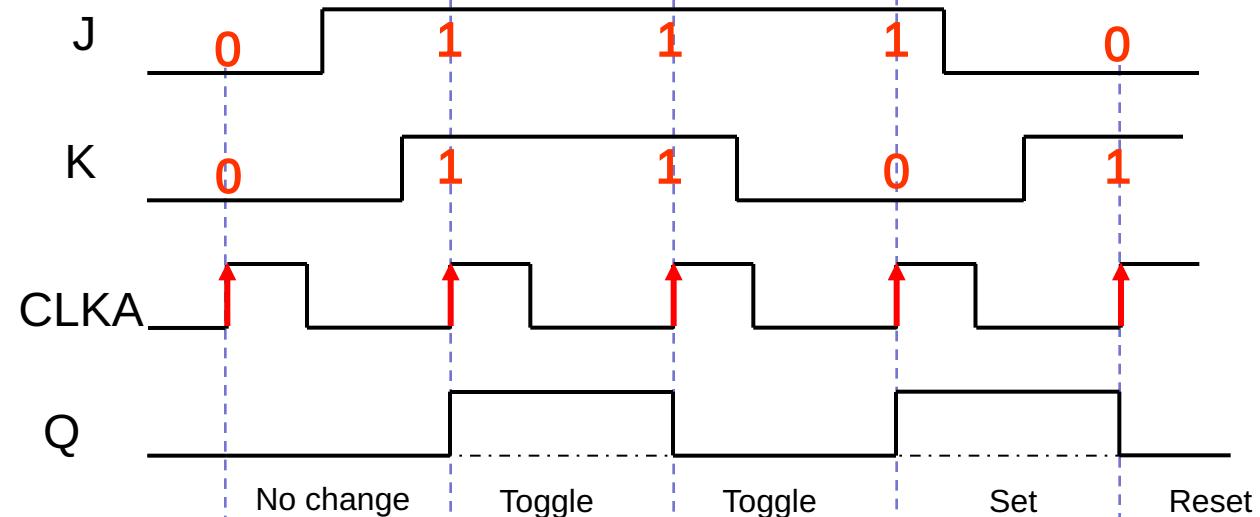


(V) Timing (or) Switching (or) Waveform Diagram

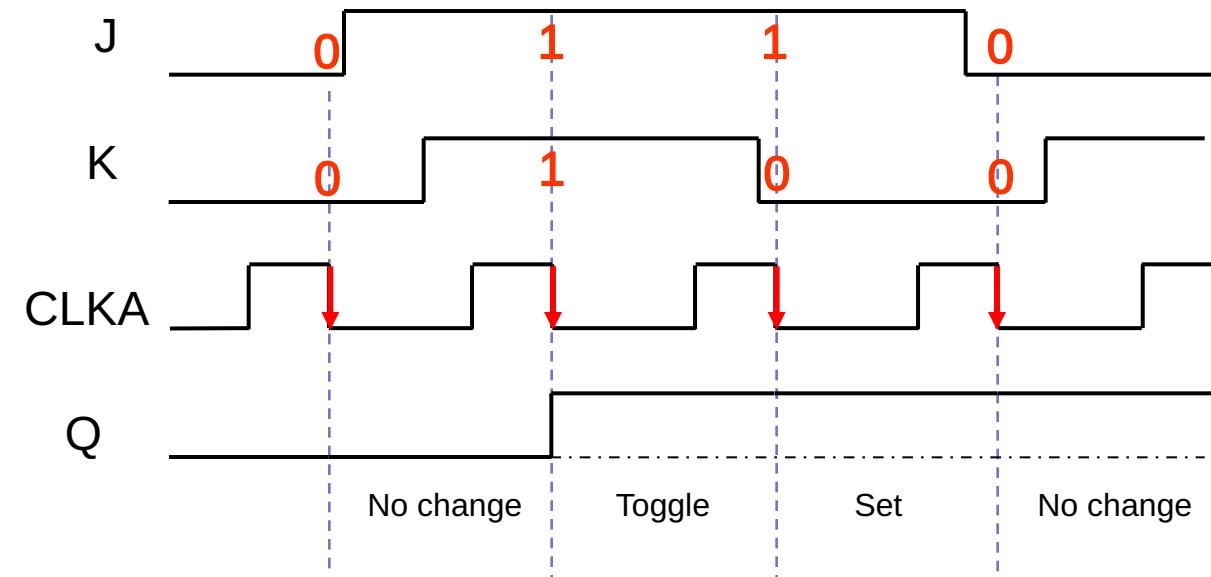




Assume Q=0 initially

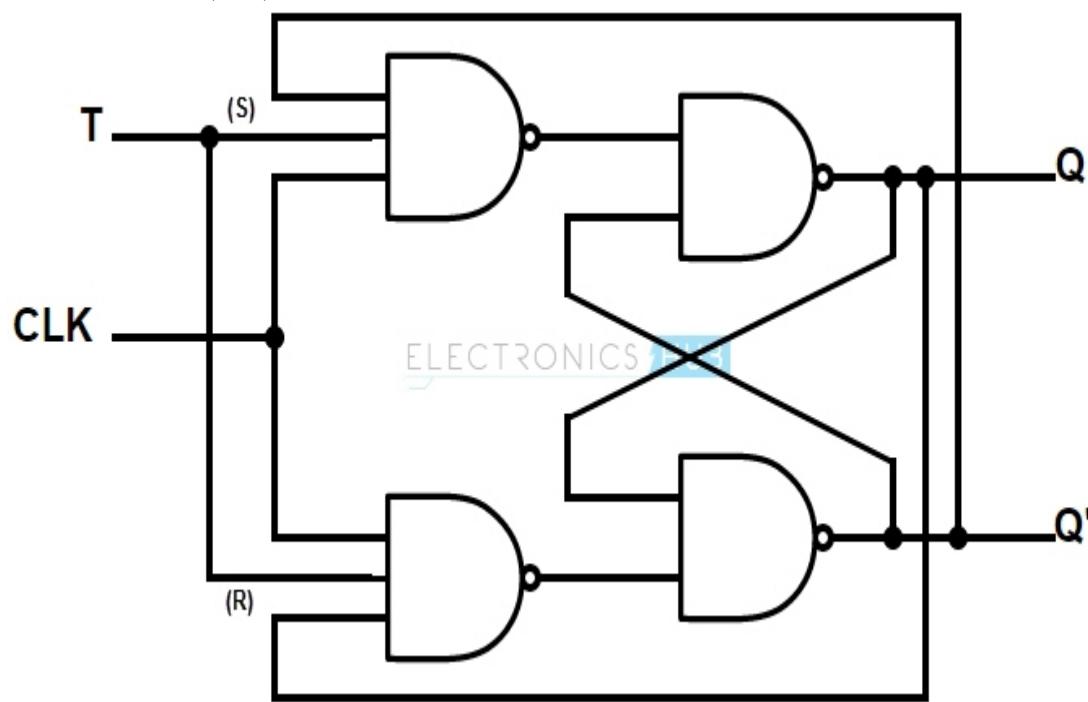


Assume Q=0 initially



T Flipflop

- (i) Circuit Diagram
- (ii) Truth Table



	Previous		Next	
T	Q_{Prev}	Q'_{Prev}	Q_{Next}	Q'_{Next}
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	0	1

(iii) Characteristic Equation

Q_p	0	1
0	0	1
1	1	0

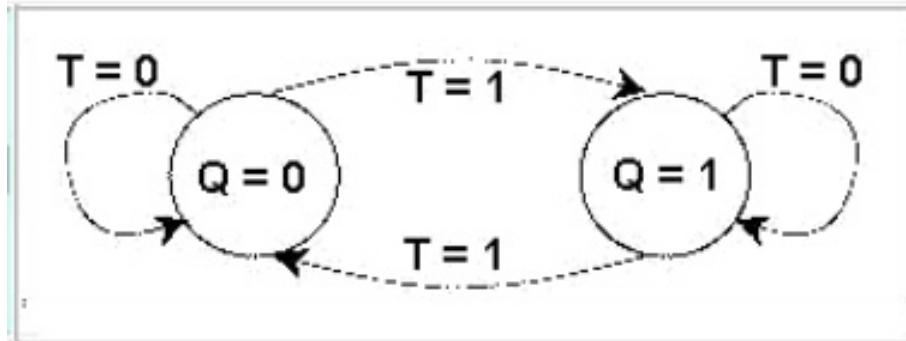
The Equation we get is

$$\begin{aligned} Q &= T Q_p' + T' Q_p \\ &= T \text{ XOR } Q_p \end{aligned}$$

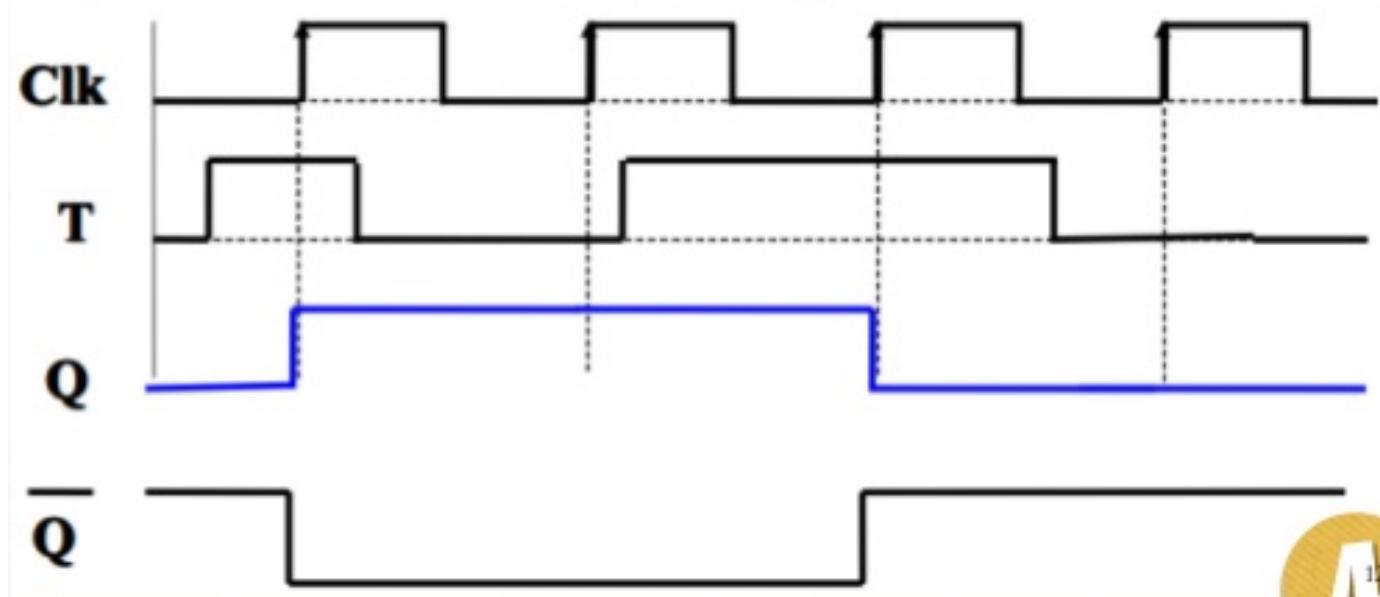
(iv) Excitation Table

Q	Q'	T
0	0	0
0	1	1
1	0	1
1	1	0

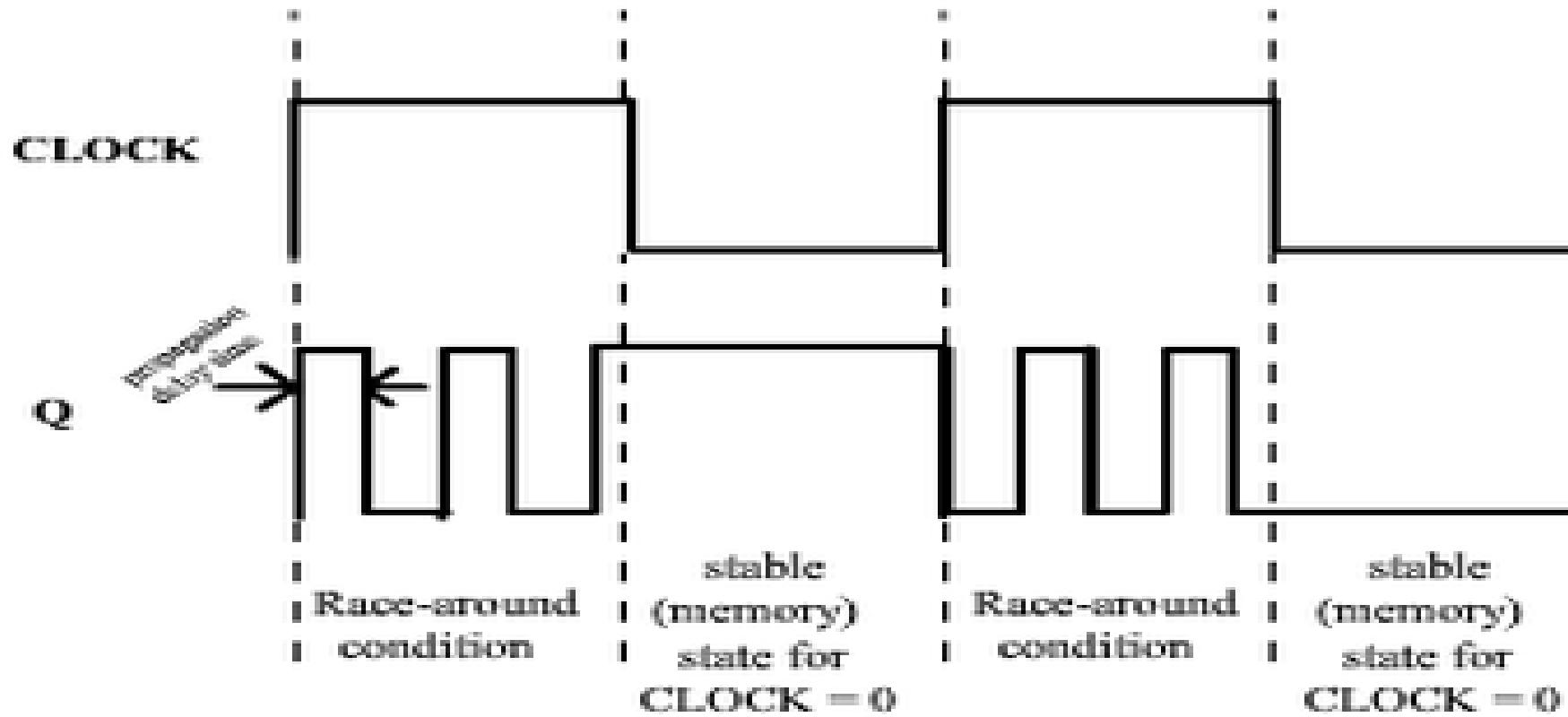
(v) State Diagram



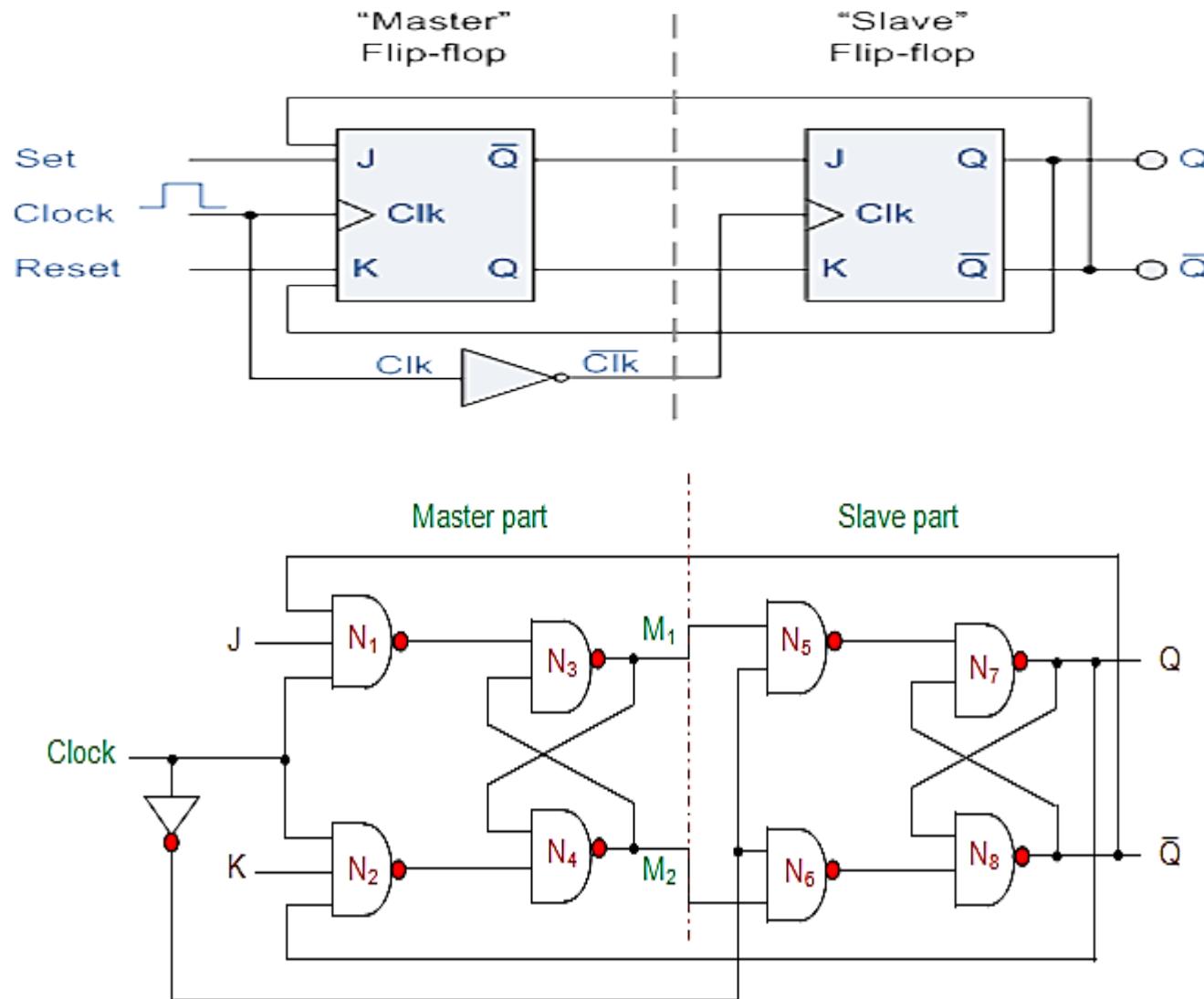
(vi) Timing Diagram



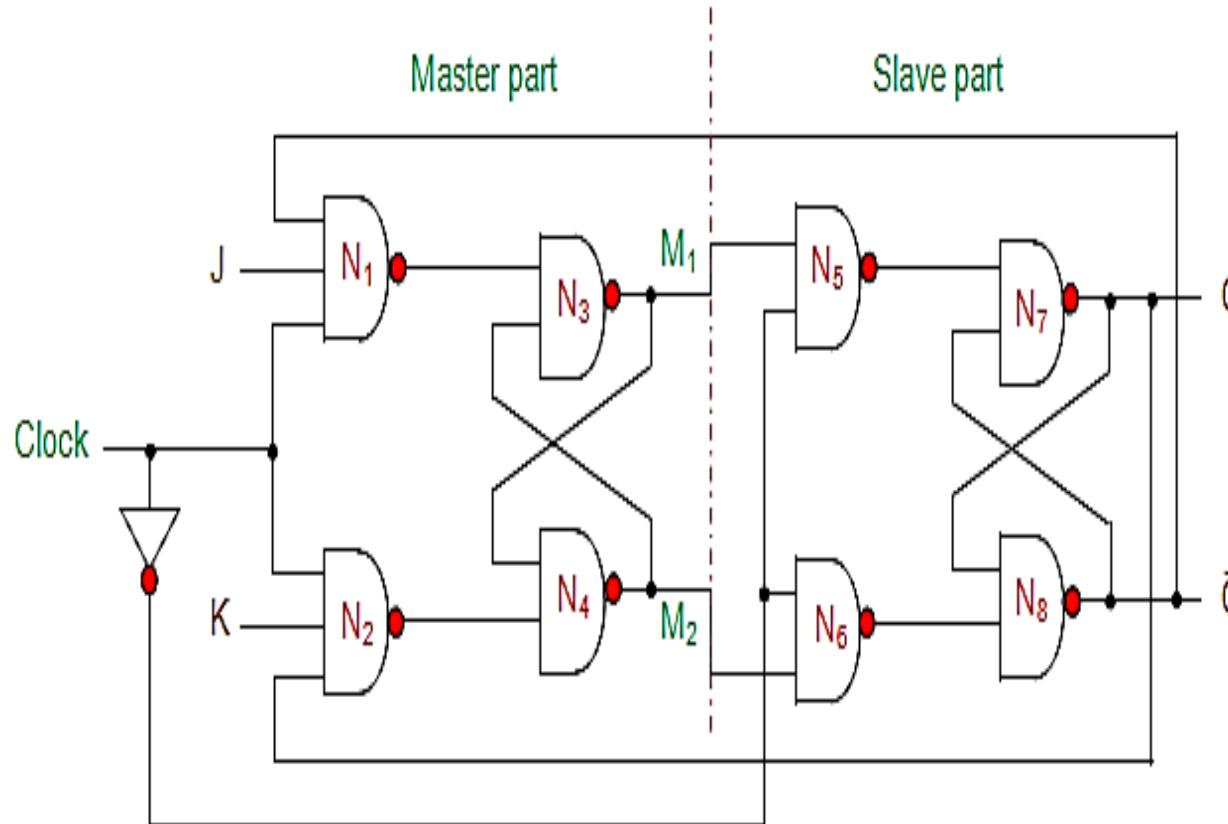
Race around condition in JK FF



Master slave JK flipflop



Master slave JK flipflop



Trigger	Inputs		Output						Inference
			Present State		Intermediate		Next State		
CLK	J	K	Q	\bar{Q}	M_1	M_2	Q	\bar{Q}	
↑	0	0	0	1	0	1	0	1	Latched
↓			0	1	Latched		0	1	
↑	0	1	1	0	1	0	1	0	Latched
↓			1	0	Latched		1	0	
↑	1	0	0	1	0	1	0	1	Latched
↓			0	1	Latched		0	1	
↑	1	1	1	0	0	1	0	1	Latched
↓			1	0	Latched		1	0	
↑	0	0	0	1	1	0	1	0	Latched
↓			0	1	Latched		1	0	
↑	0	1	1	0	1	0	1	0	Latched
↓			1	0	Latched		1	0	
↑	1	0	0	1	1	0	0	1	Latched
↓			0	1	Latched		1	0	
↑	1	1	1	0	0	1	1	0	Latched
↓			1	0	Latched		0	1	

Table I Truth table for master-slave JK flip-flop

Master slave JK flipflop

Trigger	Inputs		Output						Inference
			Present State		Intermediate		Next State		
CLK	J	K	Q	\bar{Q}	M_1	M_2	Q	\bar{Q}	
↑	0	0	0	1	0	1	Latched		No Change
↓			0	1	Latched		0	1	
↑			1	0	1	0	Latched		
↓			1	0	Latched		1	0	
↑	0	1	0	1	0	1	Latched		Reset
↓			0	1	Latched		0	1	
↑			1	0	0	1	Latched		
↓			1	0	Latched		0	1	
↑	1	0	0	1	1	0	Latched		Set
↓			0	1	Latched		1	0	
↑			1	0	1	0	Latched		
↓			1	0	Latched		1	0	
↑	1	1	0	1	1	0	Latched		Toggles
↓			0	1	Latched		1	0	
↑			1	0	0	1	Latched		
↓			1	0	0	1	Latched		

Table I Truth table for master-slave JK flip-flop

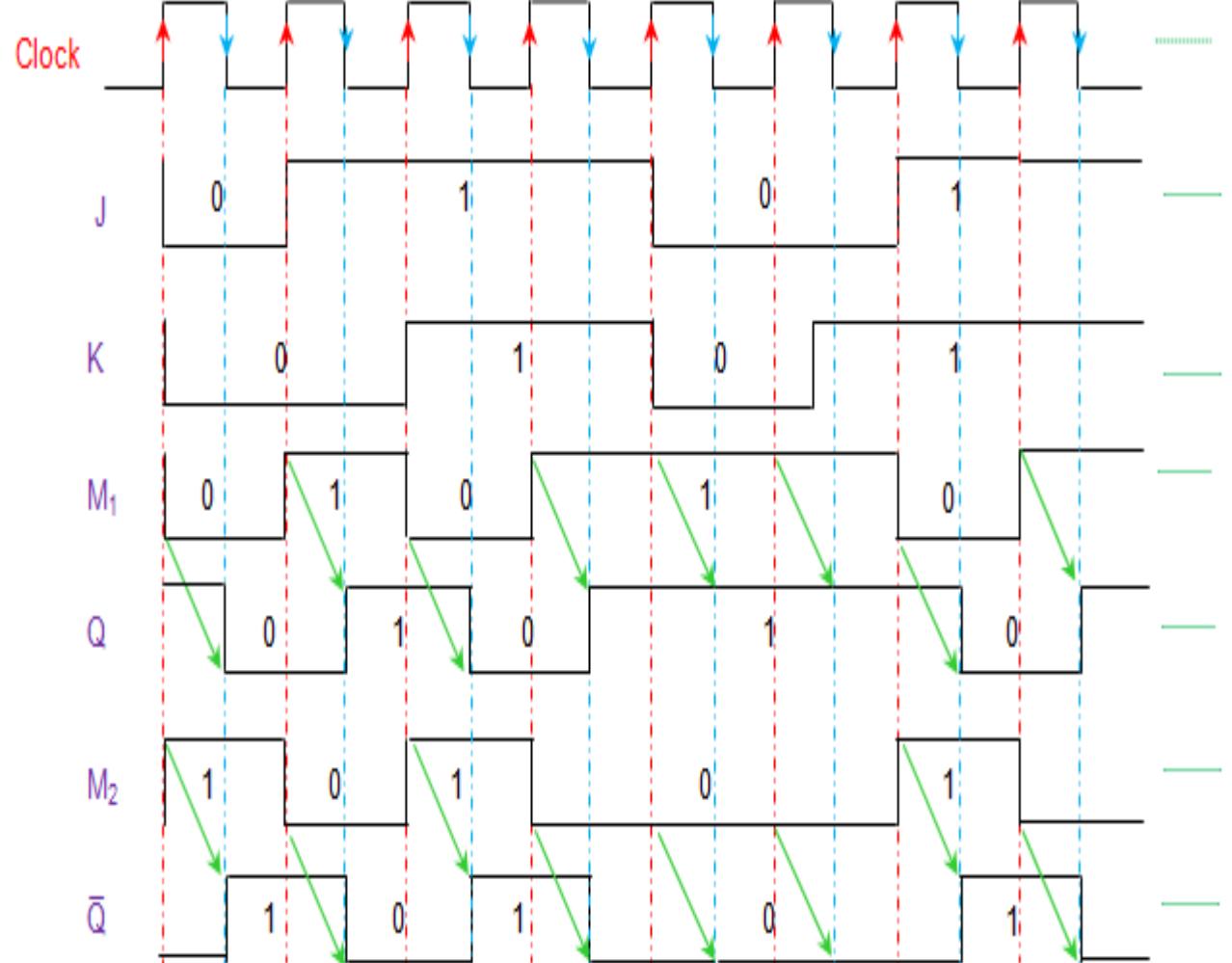


Figure 3 Timing diagram for master-slave JK flip-flop

Excitation Tables

RS FLIP FLOP			
Truth Table		Excitation Table	
S	R	Q_{n+1}	
0	0	Q_n	
0	1	0	
1	0	1	
1	1	X	

Q _n	Q _{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

JK FLIP FLOP			
Truth Table		Excitation Table	
J	K	Q_{n+1}	
0	0	Q_n	
0	1	0	
1	0	1	
1	1	Q_n'	

Q _n	Q _{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D FLIP FLOP			
Truth Table		Excitation Table	
D	Q_n	Q_{n+1}	
0	0	0	
0	1	0	
1	0	1	
1	1	1	

Q _n	Q _{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

T FLIP FLOP			
Truth Table		Excitation Table	
T	Q_n	Q_{n+1}	
0	0	0	
0	1	1	
1	0	1	
1	1	0	

Q _n	Q _{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

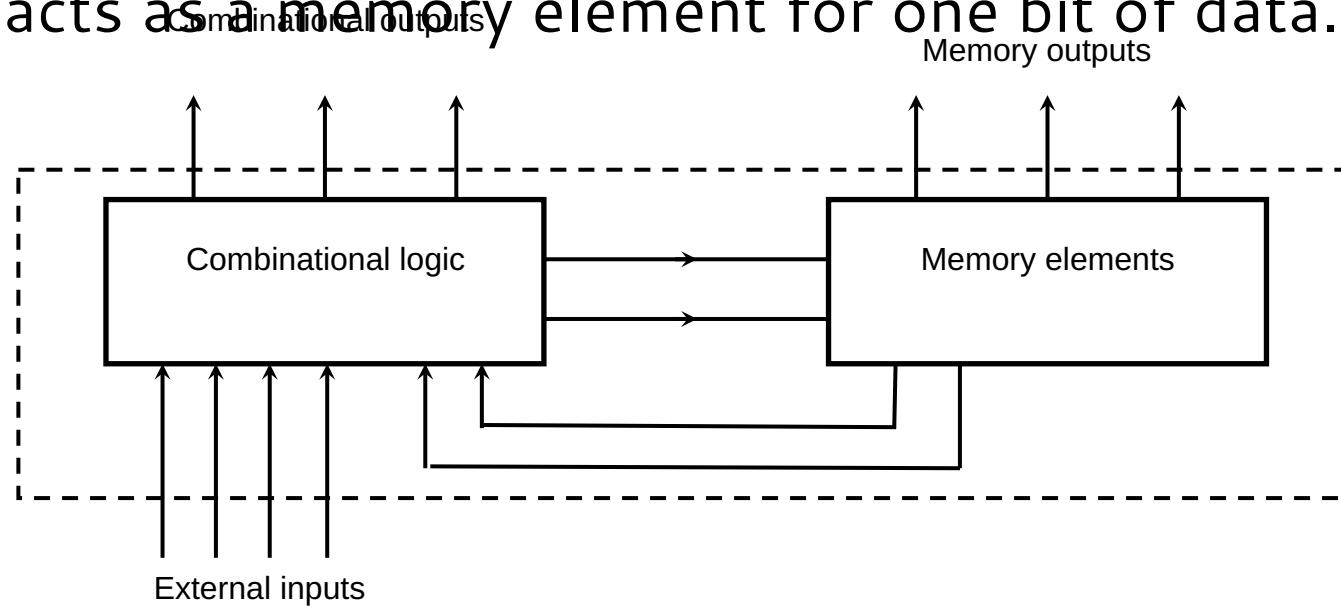
NAME	STATE DIAGRAM
SR	<p>State Diagram for SR:</p> <ul style="list-style-type: none"> States: $Q = 0$, $Q = 1$ Transitions: <ul style="list-style-type: none"> $S, R = 0, 0$: $Q = 0 \rightarrow Q = 0$ $S, R = 1, 0$: $Q = 0 \rightarrow Q = 1$ $S, R = 0, 1$: $Q = 1 \rightarrow Q = 0$ $S, R = 0, 0$: $Q = 1 \rightarrow Q = 1$
JK	<p>State Diagram for JK:</p> <ul style="list-style-type: none"> States: $Q = 0$, $Q = 1$ Transitions: <ul style="list-style-type: none"> $J, K = 0, 0$: $Q = 0 \rightarrow Q = 0$ $J, K = 1, 0 \text{ or } 1, 1$: $Q = 0 \rightarrow Q = 1$ $J, K = 0, 1 \text{ or } 1, 1$: $Q = 1 \rightarrow Q = 0$ $J, K = 0, 0$: $Q = 1 \rightarrow Q = 1$
D	<p>State Diagram for D:</p> <ul style="list-style-type: none"> States: $Q = 0$, $Q = 1$ Transitions: <ul style="list-style-type: none"> $D = 0$: $Q = 0 \rightarrow Q = 0$ $D = 1$: $Q = 0 \rightarrow Q = 1$ $D = 1$: $Q = 1 \rightarrow Q = 1$ $D = 0$: $Q = 1 \rightarrow Q = 0$
T	<p>State Diagram for T:</p> <ul style="list-style-type: none"> States: $Q = 0$, $Q = 1$ Transitions: <ul style="list-style-type: none"> $T = 0$: $Q = 0 \rightarrow Q = 0$ $T = 1$: $Q = 0 \rightarrow Q = 1$ $T = 1$: $Q = 1 \rightarrow Q = 0$ $T = 0$: $Q = 1 \rightarrow Q = 1$

Unit - 4

Sequential circuits

Sequential Logic

- Has **memory**; the circuit stores the result of the previous set of inputs. The current output depends on inputs **in the past** as well as present inputs.
 - The basic element in sequential logic is the **bistable latch** or **flip-flop**, which acts as a **memory** element for one bit of data.



Sequential circuit = Combinational logic + Memory Elements

Excitation Tables

RS FLIP FLOP			
Truth Table		Excitation Table	
S	R	Q_{n+1}	
0	0	Q_n	
0	1	0	
1	0	1	
1	1	X	

Q _n	Q _{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

JK FLIP FLOP			
Truth Table		Excitation Table	
J	K	Q_{n+1}	
0	0	Q_n	
0	1	0	
1	0	1	
1	1	Q_n'	

Q _n	Q _{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D FLIP FLOP			
Truth Table		Excitation Table	
D	Q_n	Q_{n+1}	
0	0	0	
0	1	0	
1	0	1	
1	1	1	

Q _n	Q _{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

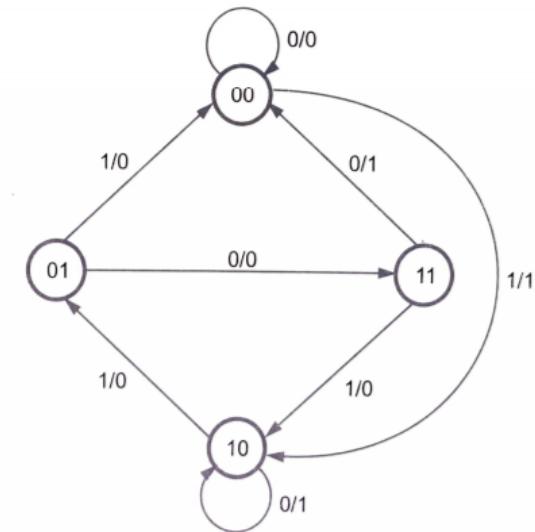
T FLIP FLOP			
Truth Table		Excitation Table	
T	Q_n	Q_{n+1}	
0	0	0	
0	1	1	
1	0	1	
1	1	0	

Q _n	Q _{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

NAME	STATE DIAGRAM
SR	<p>State Diagram for SR:</p> <ul style="list-style-type: none"> States: $Q = 0$, $Q = 1$ Transitions: <ul style="list-style-type: none"> $S, R = 0, 0$: $Q = 0 \rightarrow Q = 0$ $S, R = 1, 0$: $Q = 0 \rightarrow Q = 1$ $S, R = 0, 1$: $Q = 1 \rightarrow Q = 0$ $S, R = 0, 0$: $Q = 1 \rightarrow Q = 1$
JK	<p>State Diagram for JK:</p> <ul style="list-style-type: none"> States: $Q = 0$, $Q = 1$ Transitions: <ul style="list-style-type: none"> $J, K = 0, 0$: $Q = 0 \rightarrow Q = 0$ $J, K = 1, 0 \text{ or } 1, 1$: $Q = 0 \rightarrow Q = 1$ $J, K = 0, 1 \text{ or } 1, 1$: $Q = 1 \rightarrow Q = 0$ $J, K = 0, 0$: $Q = 1 \rightarrow Q = 1$
D	<p>State Diagram for D:</p> <ul style="list-style-type: none"> States: $Q = 0$, $Q = 1$ Transitions: <ul style="list-style-type: none"> $D = 0$: $Q = 0 \rightarrow Q = 0$ $D = 1$: $Q = 0 \rightarrow Q = 1$ $D = 1$: $Q = 1 \rightarrow Q = 1$ $D = 0$: $Q = 1 \rightarrow Q = 0$
T	<p>State Diagram for T:</p> <ul style="list-style-type: none"> States: $Q = 0$, $Q = 1$ Transitions: <ul style="list-style-type: none"> $T = 0$: $Q = 0 \rightarrow Q = 0$ $T = 1$: $Q = 0 \rightarrow Q = 1$ $T = 1$: $Q = 1 \rightarrow Q = 0$ $T = 0$: $Q = 1 \rightarrow Q = 1$

DESIGN PROBLEMS

- A sequential circuit has one input and one output. The state diagram is shown in figure. Design the sequential circuit with a) D-FF b) T-FF c) RS-FF d) JK-FF



- a) D-FF

Present state		Next state		Output	
		X = 0	X = 1	X = 0	X = 1
A	B	AB	AB	Y	Y
0	0	0 0	1 0	0	1
0	1	1 1	0 0	0	0
1	0	1 0	0 1	1	0
1	1	0 0	1 0	1	0

Present state		Next state		Output	
		X = 0	X = 1	X = 0	X = 1
A	B	AB	AB	Y	Y
0	0	00	10	0	1
0	1	11	00	0	0
1	0	10	01	1	0
1	1	00	10	1	0

For flip - flop A

X	0	1
AB	00	0
	01	(1)
	11	0
	10	(1)

For flip - flop B

X	0	1
AB	00	0
	01	(1)
	11	0
	10	(1)

For output

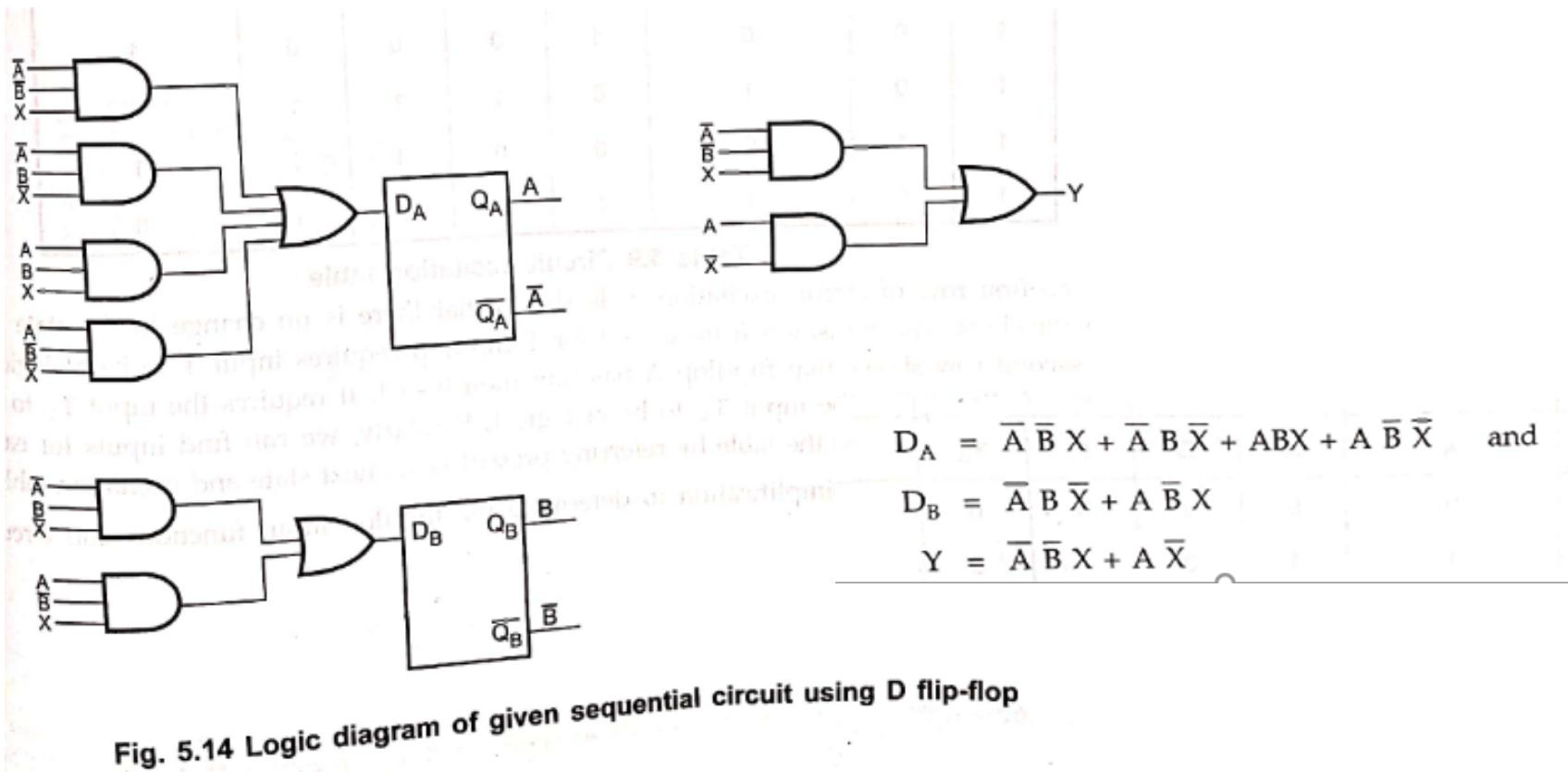
X	0	1
AB	00	0
	01	0
	11	1
	10	1

Fig. 5.13

$$D_A = \overline{A} \overline{B} X + \overline{A} B \overline{X} + ABX + A \overline{B} \overline{X} \quad \text{and}$$

$$D_B = \overline{A} B \overline{X} + A \overline{B} X$$

$$Y = \overline{A} \overline{B} X + A \overline{X}$$



$$D_A = \overline{A} \overline{B} X + \overline{A} B \overline{X} + ABX + A \overline{B} \overline{X} \quad \text{and}$$

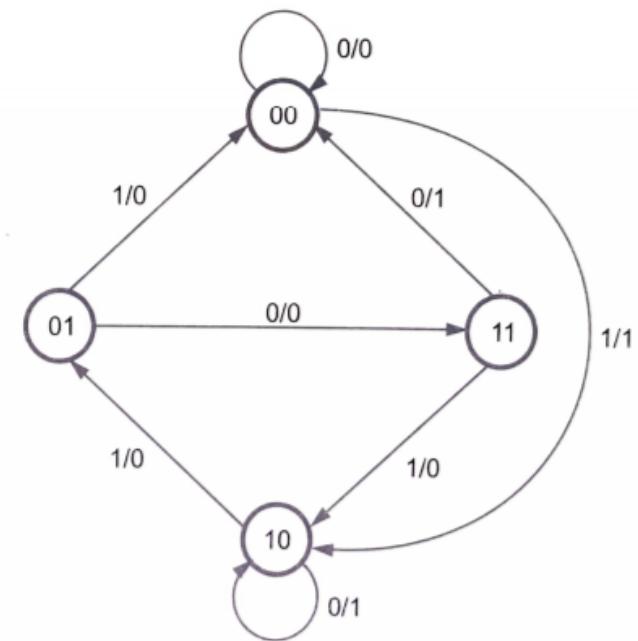
$$D_B = \overline{A} B \overline{X} + A \overline{B} X$$

$$Y = \overline{A} \overline{B} X + A \overline{X}$$

- A sequential circuit has one input and one output. The state diagram is shown in figure. Design the sequential circuit with a) D-FF b) T-FF c) RS-FF d) JK-FF

- a) T-FF

Present state		Input	Next state		Flip-flop inputs		Out
A	B	X	A	B	T _A	T _B	Y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	1	1	0	0
0	1	1	0	0	0	1	0
1	0	0	1	0	0	0	1
1	0	1	0	1	1	1	0
1	1	0	0	0	1	1	1
1	1	1	1	0	0	1	0



	X	AB	0	1
00	0	0	1	0
01	1	0	0	1
11	1	1	1	0
10	0	1	0	1

(a) For flip-flop A

	X	AB	0	1
00	0	0	0	0
01	0	1	1	0
11	1	1	1	1
10	0	1	0	1

(b) For flip-flop B

	X	AB	0	1
00	0	0	1	0
01	0	1	0	0
11	1	1	1	0
10	1	0	0	1

(c) For output

Present state		Input	Next state		Flip-flop inputs		Output
A	B		A	B	T _A	T _B	
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	1	1	0	0
0	1	1	0	0	0	1	0
1	0	0	1	0	0	0	1
1	0	1	0	1	1	1	0
1	1	0	0	0	1	1	1
1	1	1	1	0	0	1	0

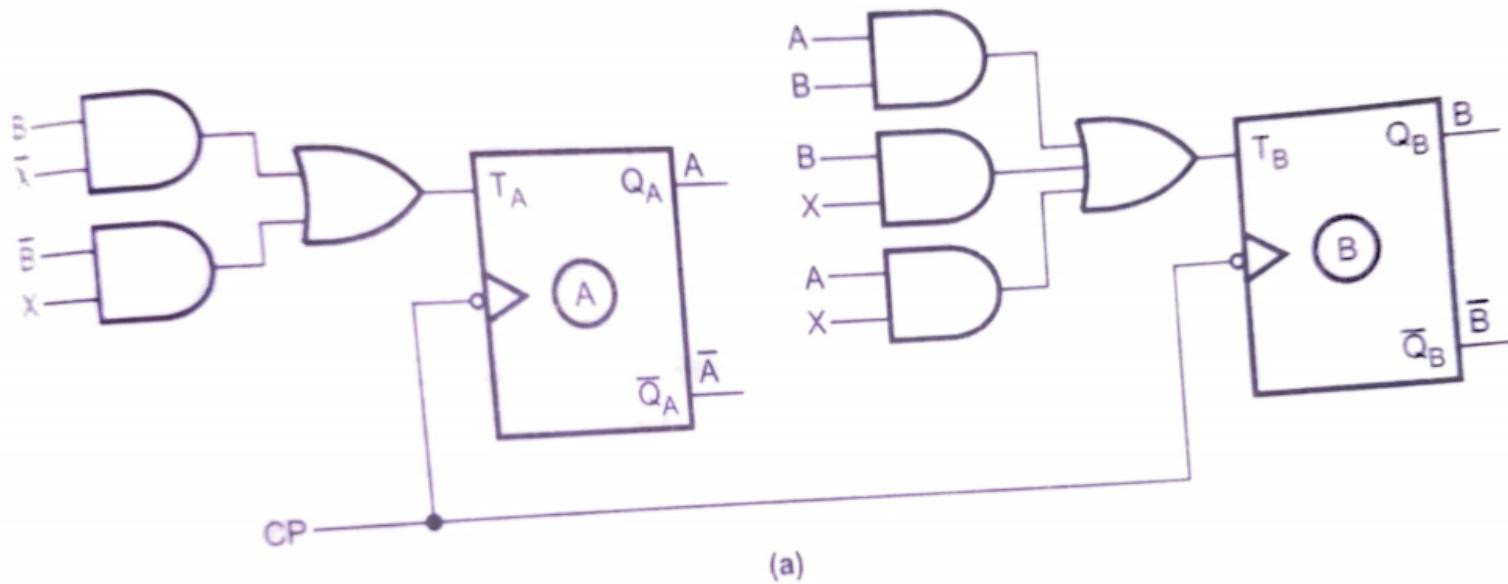
Fig. 5.15

fore, input function for

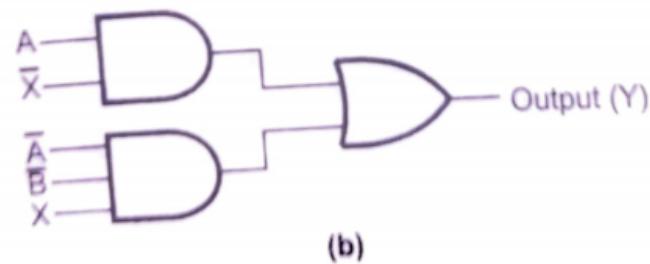
$$T_A = B\bar{X} + \bar{B}X,$$

$$T_B = AB + BX + AX, \text{ and}$$

$$\text{Circuit output function} = A\bar{X} + \bar{A}\bar{B}X$$



(a)



(b)

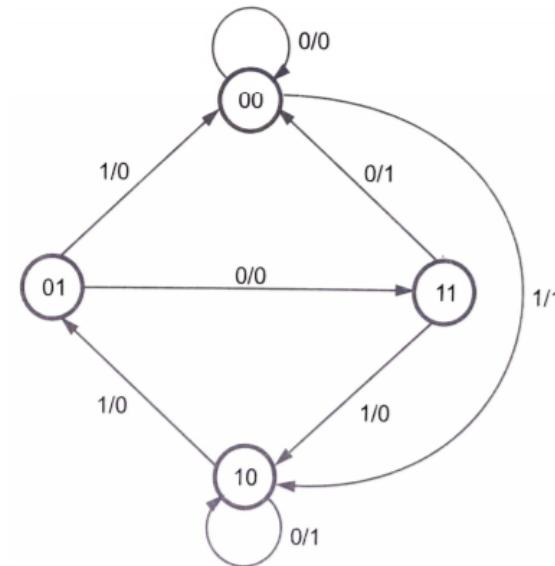
Fig. 5.15 Realization of a function by a sequential circuit.

$$T_A = B\bar{X} + \bar{B}X,$$

$$T_B = AB + BX + AX, \text{ and}$$

$$\text{function } = A\bar{X} + \bar{A}\bar{B}X$$

- A sequential circuit has one input and one output. The state diagram is shown in figure. Design the sequential circuit with a) D-FF b) T-FF c) RS-FF d) JK-FF



- a) RS-FF

Present state		Input	Next state		Flip-flop inputs				Output
A	B		A	B	R _A	S _A	R _B	S _B	
0	0	0	0	0	X	0	X	0	0
0	0	1	1	0	0	1	X	0	1
0	1	0	1	1	0	1	0	X	0
0	1	1	0	0	X	0	1	0	0
1	0	0	1	0	0	X	X	0	1
1	0	1	0	1	1	0	0	1	0
1	1	0	0	0	1	0	1	0	1
1	1	1	1	0	0	X	1	0	0

Table 5.44

Present state		Input X	Next state		Flip-flop inputs				Output Y
A	B		A	B	R _A	S _A	R _B	S _B	
0	0	0	0	0	X	0	X	0	0
0	0	1	1	0	0	1	X	0	1
0	1	0	1	1	0	1	0	X	0
0	1	1	0	0	X	0	1	0	0
1	0	0	1	0	0	X	X	0	1
1	0	1	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	0	1
1	1	1	1	0	0	X	1	0	0

Table 5.14

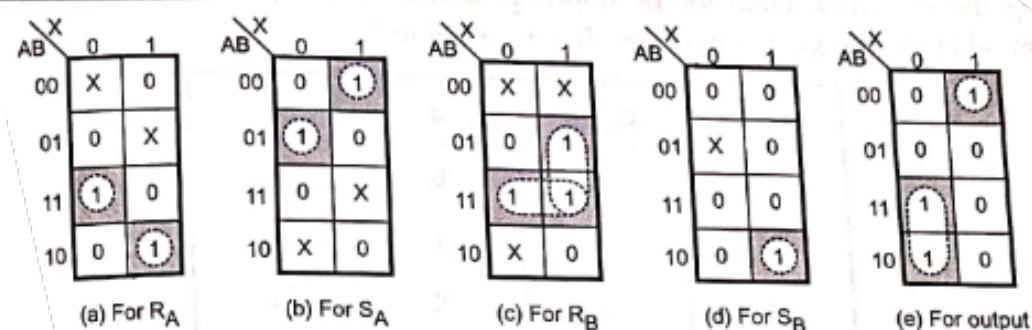


Fig. 5.17

input function for

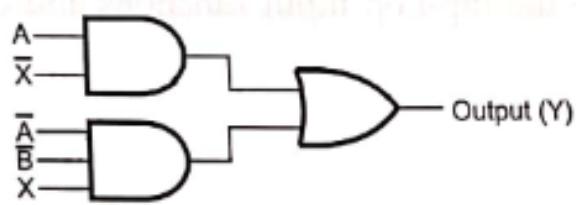
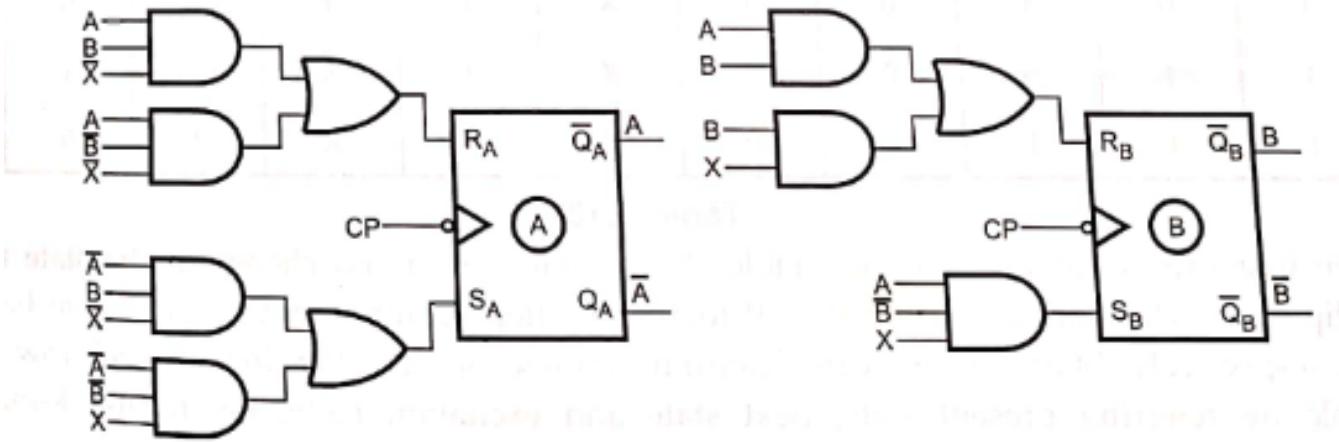
$$R_A = AB\bar{X} + A\bar{B}\bar{X}$$

$$S_A = \bar{A}B\bar{X} + \bar{A}\bar{B}X$$

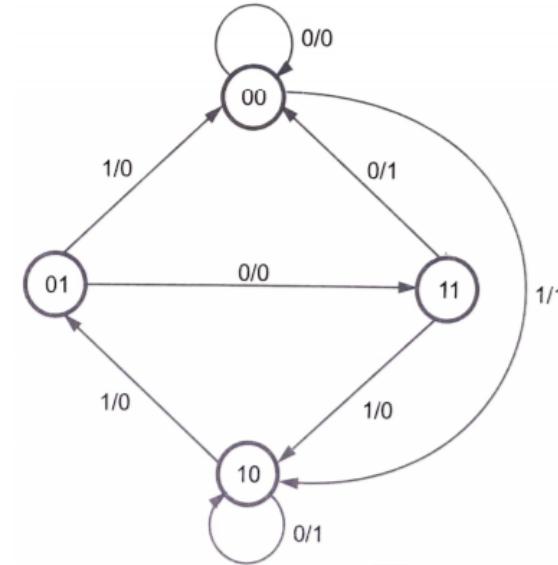
$$R_B = AB + BX$$

$$S_B = A\bar{B}X \text{ and,}$$

$$\text{Circuit output function} = A\bar{X} + \bar{A}\bar{B}X$$



- A sequential circuit has one input and one output. The state diagram is shown in figure. Design the sequential circuit with
a) D-FF b) T-FF c) RS-FF d) JK-FF



- a) JK-FF

Present state		Input	Next state		Flip-flop inputs				Output
A	B		A	B	J _A	K _A	J _B	K _B	
0	0	0	0	0	0	X	0	X	0
0	0	1	1	0	1	X	0	X	1
0	1	0	1	1	1	X	X	0	0
0	1	1	0	0	0	X	X	1	0
1	0	0	1	0	X	0	0	X	1
1	0	1	0	1	X	1	1	X	0
1	1	0	0	0	X	1	X	1	1
1	1	1	1	0	X	0	X	1	0

Table - 5.4

Present state		Input X	Next state		Flip-flop inputs				Output Y
A	B		A	B	J _A	K _A	J _B	K _B	
0	0	0	0	0	0	X	0	X	0
0	0	1	1	0	1	X	0	X	1
0	1	0	1	1	1	X	X	0	0
0	1	1	0	0	0	X	X	1	0
1	0	0	1	0	X	0	0	X	1
1	0	1	0	1	X	1	1	X	0
1	1	0	0	0	X	1	X	1	1
1	1	1	1	0	X	0	X	1	0

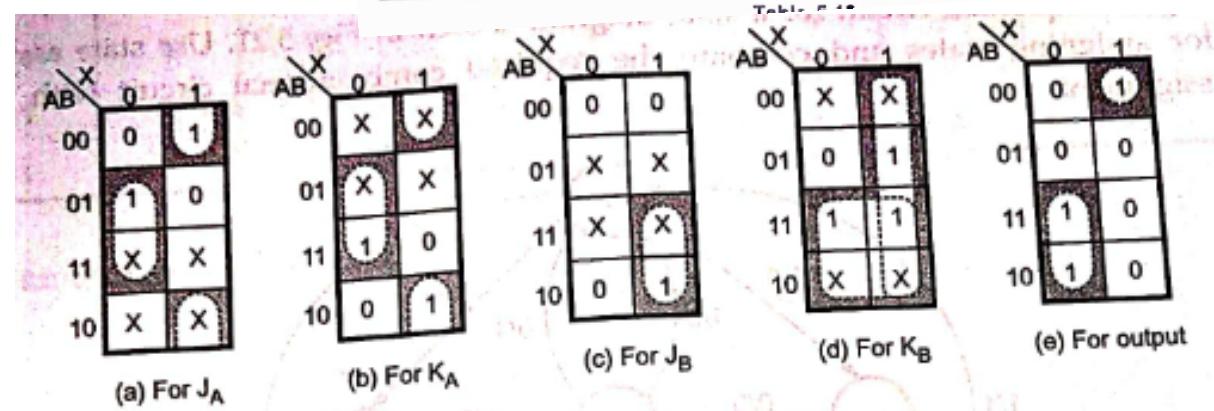


Fig. 5.19

$$J_A = \overline{BX} + \overline{B}X$$

$$K_A = \overline{B}\overline{X} + \overline{B}X$$

$$J_B = AX$$

$$K_B = A + X$$

Circuit output function = $A\overline{X} + \overline{A}\overline{B}X$

input function for

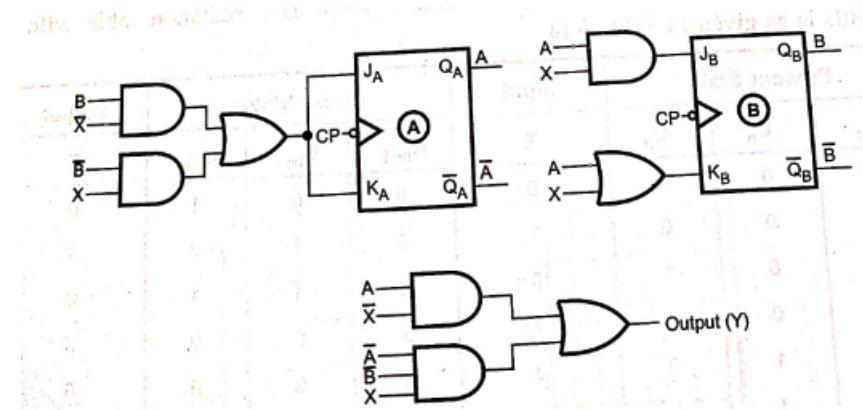
$$J_A = B\bar{X} + \bar{B}X$$

$$K_A = \bar{B}\bar{X} + \bar{B}X$$

$$J_B = AX$$

$$K_B = A+X$$

Circuit output function = $A\bar{X} + \bar{A}\bar{B}X$



states.

Example 5.2 : Design the sequential circuit for the state diagram shown in Fig. 5.26 use JK flip-flops.

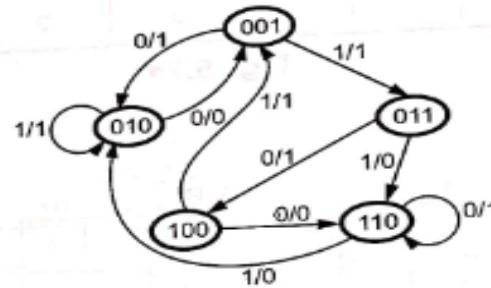


Fig. 5.26

Solution : The state table for given state diagram is as follows

Present State			Input X	Next State			Flip-flop inputs						Output Y
A	B	C		A	B	C	J _A	K _A	J _B	K _B	J _C	K _C	
0	0	1	0	0	1	0	0	X	1	X	X	1	1
0	0	1	1	0	1	1	0	X	1	X	X	0	1
0	1	0	0	0	0	1	0	X	X	1	1	X	0
0	1	0	1	0	1	0	0	X	X	0	0	X	1
0	1	1	0	1	0	0	1	X	X	1	X	1	1
0	1	1	1	1	1	0	1	X	X	0	X	1	0
1	0	0	0	1	1	0	X	0	1	X	0	X	0
1	0	0	1	0	0	1	X	1	0	X	1	X	1
1	1	0	0	1	1	0	X	0	X	0	0	X	1
1	1	0	1	0	1	0	X	1	X	0	0	X	0

- The unused states are taken as don't cares

		For J_A				
		AB	00	01	11	10
CX		00	X	X	0	0
CX		01	0	0	1	1
CX		11	X	X	X	X
CX		10	X	X	X	X

		For K_A				
		AB	00	01	11	10
CX		00	X	X	1	1
CX		01	X	X	X	X
CX		11	X	X	X	X
CX		10	1	0	X	X

		For J_B				
		AB	00	01	11	10
CX		00	X	X	X	X
CX		01	X	X	X	X
CX		11	0	1	X	X
CX		10	0	1	X	X

		For K_B				
		AB	00	01	11	10
CX		00	X	X	X	X
CX		01	1	0	0	1
CX		11	0	0	X	X
CX		10	X	X	X	X

		For J_C				
		AB	00	01	11	10
CX		00	X	X	X	X
CX		01	1	0	X	X
CX		11	0	0	X	X
CX		10	0	1	X	X

		For K_C				
		AB	00	01	11	10
CX		00	X	X	1	0
CX		01	X	X	1	1
CX		11	X	X	X	X
CX		10	X	X	X	X

		For Output				
		AB	00	01	11	10
CX		00	X	X	1	1
CX		01	0	1	0	1
CX		11	1	0	X	X
CX		10	0	1	X	X

input functions for

$$J_A = BC$$

$$K_A = \bar{X} + C$$

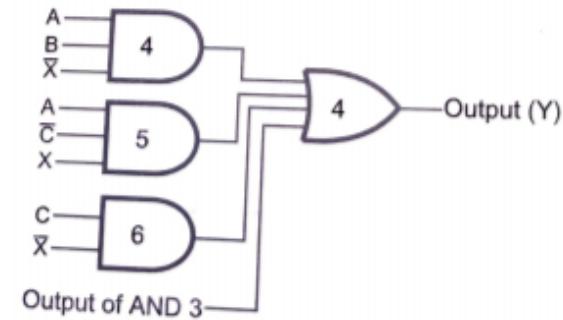
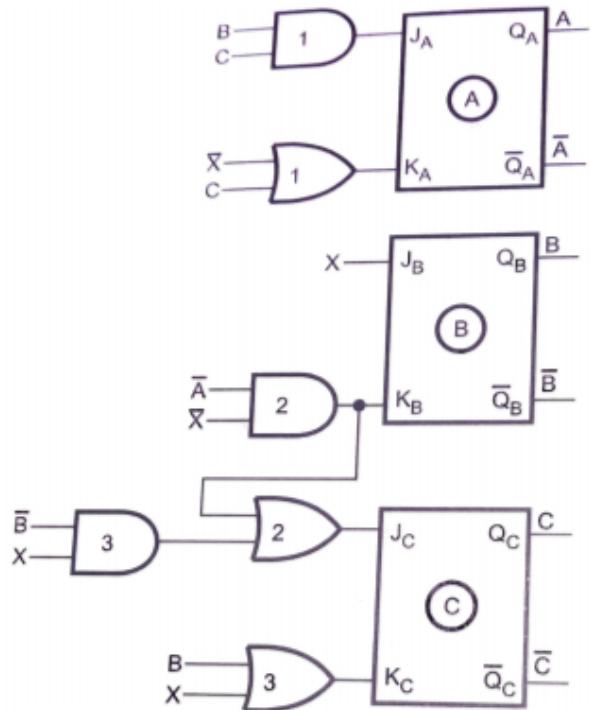
$$J_B = X$$

$$K_B = \bar{A} \bar{X}$$

$$J_C = \bar{A} \bar{X} + \bar{B}X \quad \text{and}$$

$$K_C = B + X$$

$$\text{output function } Y = AB\bar{X} + A\bar{C}X + \bar{B}BX + C\bar{X}$$



input functions for

$$J_A = BC$$

$$K_A = \bar{X} + C$$

$$J_B = X$$

$$K_B = \bar{A} \bar{X}$$

$$J_C = \bar{A} \bar{X} + \bar{B} X \quad \text{and}$$

$$K_C = B + X$$

$$\text{output function } Y = AB\bar{X} + A\bar{C}X + \bar{B}X + C\bar{X}$$

► **Example 5.5 :** Realize the sequential circuit for the state diagram shown in Fig. 5.44.

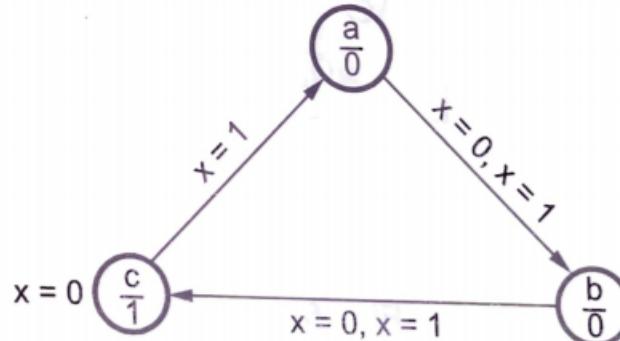


Fig. 5.44

Solution : Since the state diagram shows 3 states we required 2 flip-flops to implement the given sequential circuit. The Table 5.21 shows the state table for the given state diagram.

Present State	Next state				Output	
	X = 0		X = 1			
	A	B	A_{+1}	B_{+1}		
a	0	0	0	1	0	0
b	0	1	1	0	1	0
c	1	0	1	0	0	1

Table 5.21

		For D_A		For D_B	
		AB		AB	
AB	X	00	0	00	1
01		1	1	01	0
11		X	X	11	X
10		1	0	10	0

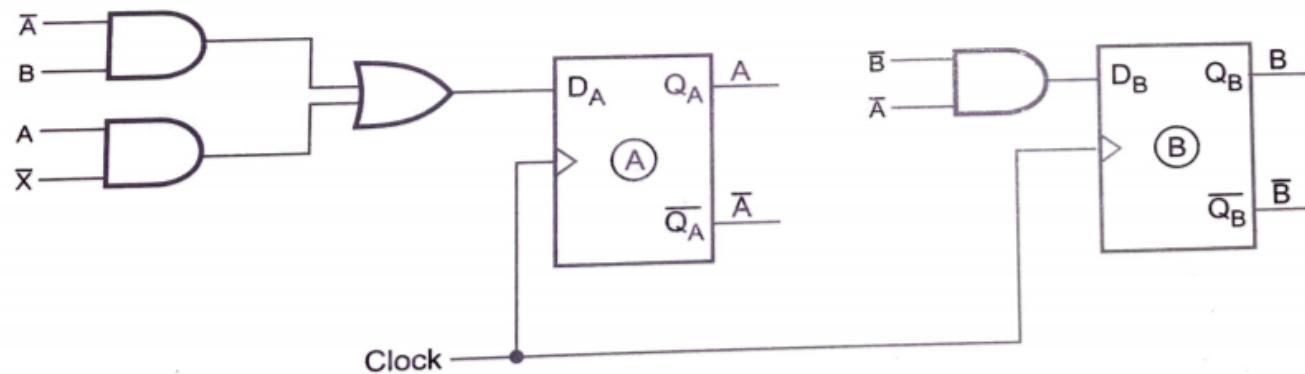
$D_A = \bar{A}B + A\bar{X}$

		For D_A		For D_B	
		AB		AB	
AB	X	00	1	00	1
01		0	0	01	0
11		X	X	11	X
10		0	0	10	0

$D_B = \bar{A}\bar{B}$

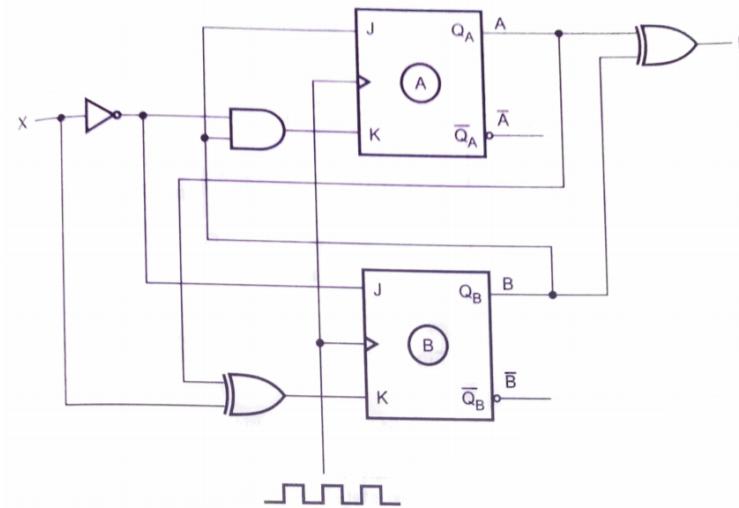
Fig. 5.45

Logic Diagram



ANALYSIS PROBLEMS

- Construct the transition table, state table, state diagram for the Moore sequential circuit given



Solution : 1. Determine the flip-flop input equations and the output equations from the sequential circuit.

$$F = A \oplus B$$

$$J_A = B \quad K_A = \bar{X}B$$

$$J_B = \bar{X} \quad K_B = X \oplus A$$

Solution : 1. Determine the flip-flop input equations and the output equations from the sequential circuit.

$$F = A \oplus B$$

$$J_A = B \quad K_A = \bar{X}B$$

$$J_B = \bar{X} \quad K_B = X \oplus A$$

2. Derive the transition equations.

The transition equations for JK flip-flops can be derived from the characteristic equation of JK flip-flop as follows :

We know that for JK flop-flop

$$Q^+ = J\bar{Q} + \bar{K}Q$$

$$\therefore A^+ = Q_A^+ = J_A \bar{Q}_A + \bar{K}_A Q_A = B\bar{Q}_A + \bar{\bar{X}}B Q_A = B\bar{Q}_A + (X + \bar{B}) Q_A$$

$$= B\bar{A} + (X + \bar{B}) A$$

and $B^+ = Q_B^+ = J_B \bar{Q}_B + \bar{K}_B Q_B = \bar{X} \bar{Q}_B + \overline{X \oplus A} Q_B$

$$= \bar{X} \bar{B} + \overline{X \oplus A} \cdot B$$

The next-state maps are :

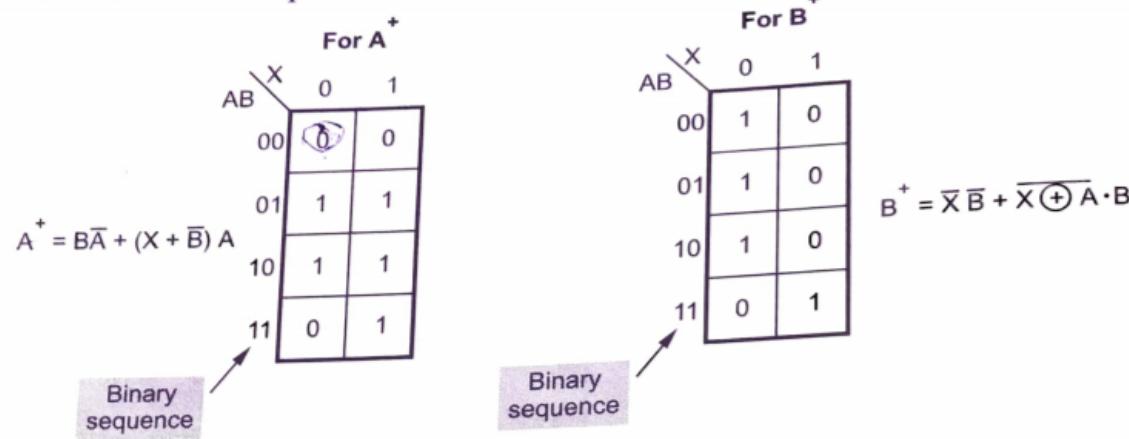


Fig. 5.42 (b)

4. Plot the transition table.

The transition table can be formed by combining the above two maps. The Table 5.19 shows the transition table.

Present state		Next state				Output
		X = 0		X = 1		
A	B	A ⁺	B ⁺	A ⁺	B ⁺	F = (A ⊕ B)
0	0	0	1	0	0	0
0	1	1	1	1	0	1
1	0	1	1	1	0	1
1	1	0	0	1	1	0

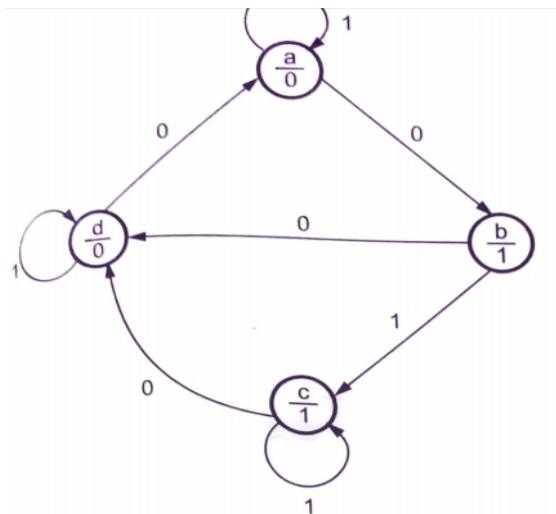
Table 5.19 Transition table

Note : For Moore sequential circuit output only depends on present state and not on the input.

5. Draw the state table

By assigning $a = 0\ 0$, $b = 01$, $c = 10$ and $d = 11$ we can write state table from the transition table as shown.

Present State A B	Next State		Output F
	X = 0	X = 1	
	A ⁺ B ⁺	A ⁺ B ⁺	
a	b	a	0
b	d	c	1
c	d	c	1
d	a	d	0



- Construct the transition table, state table, state diagram for the sequential circuit given

1. Determine the flip-flop input equations and the output equation for the sequential circuit.

$$Z = \alpha Q$$

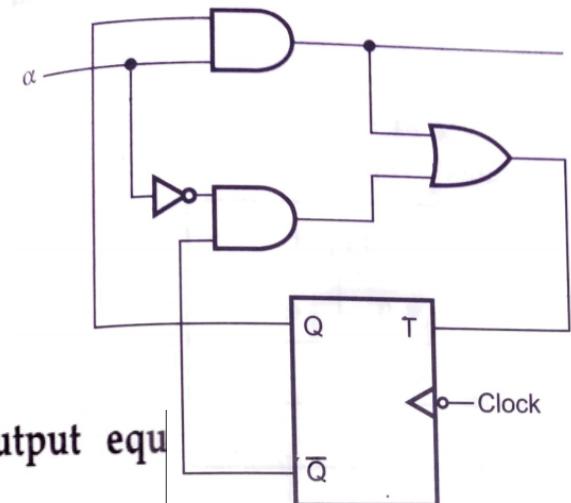
$$T = \alpha Q + \bar{\alpha} \bar{Q}$$

2. Derive the transition equation.

The transition equation for T flip-flop is

$$Q^+ = T \oplus Q$$

$$Q^+ = (\alpha Q + \bar{\alpha} \bar{Q}) \oplus Q$$



3. Plot the next step map for each flip-flop

For Q^+

$\alpha \backslash Q$	0	1
0	1	0
1	1	0

$$Q^+ = (\alpha Q + \bar{\alpha} \bar{Q}) \oplus Q$$

4. 1

Fig. 5.10

Present State	Next State		Output	
	$\alpha = 0$	$\alpha = 1$	$\alpha = 0$	$\alpha = 1$
Q	Q^+	Q^+	Z	Z
0	1	0	0	0
1	1	0	0	1

Table 5.17 Transition table

Draw the state table

The transition table shown in Table 5.17 can be converted into state table as shown in Table 5.18. Here, new symbols to binary codes are assigned. They are $a = 0$, $b = 1$.

Present State	Next State		Output	
	$\alpha = 0$	$\alpha = 1$	$\alpha = 0$	$\alpha = 1$
$a(0)$	b	a	0	0
$b(1)$	b	a	0	1

Table 5.18 State table

Draw state diagram

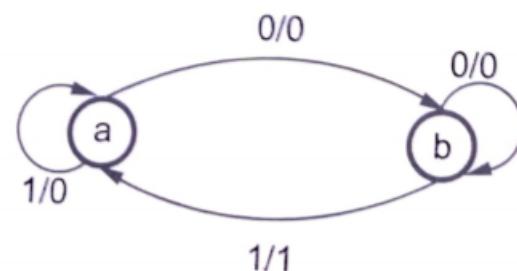


Fig. 5.41 State diagram

Analysis of Asynchronous Sequential Circuit

Types:

According to how input variables are to be considered, there are two types

- ④ Fundamental mode circuit
- ④ Pulse mode circuit.

Fundamental mode circuit assumes that:

- ✗ The input variables change only when the circuit is stable.
- ✗ Only one input variable can change at a given time.
- ✗ Inputs are levels (0, 1) and not pulses.

Pulse mode circuit assumes that:

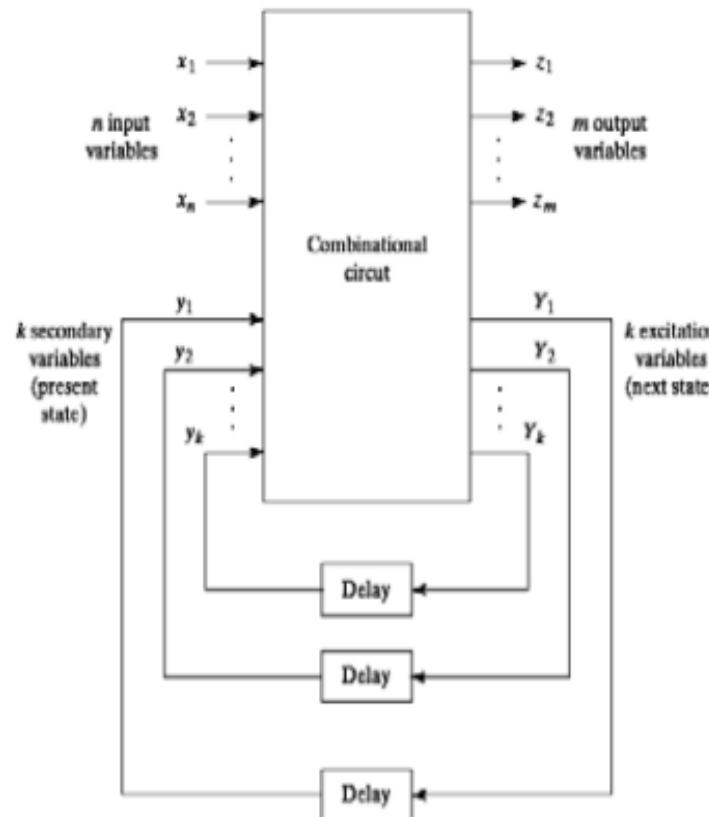
- ✗ The input variables are pulses (True, False) instead of levels.
- ✗ The width of the pulses is long enough for the circuit to respond to the input.
- ✗ The pulse width must not be so long that it is still present after the new state is reached.

Why Asynchronous Circuits ?

- Used when speed of operation is important
 - Response quickly without waiting for a clock pulse
- Used in small independent systems
 - Only a few components are required
- Used when the input signals may change independently of internal clock
 - Asynchronous in nature
- Used in the communication between two units that have their own independent clocks
 - Must be done in an asynchronous fashion

Definitions of Asyn. Circuits

- Inputs / Outputs
- Delay elements:
 - Only a short term memory
 - May not really exist due to original gate delay
- Secondary variable:
 - Current state (small y)
- Excitation variable:
 - Next state (big Y)
 - Have some delay in response to input changes





Operational Mode

- Steady-state condition:
 - Current states and next states are the same
 - Difference between Y and y will cause a transition
- Fundamental mode:
 - No simultaneous changes of two or more variables
 - The time between two input changes must be longer than the time it takes the circuit to a stable state
 - The input signals change one at a time and only when the circuit is in a stable condition

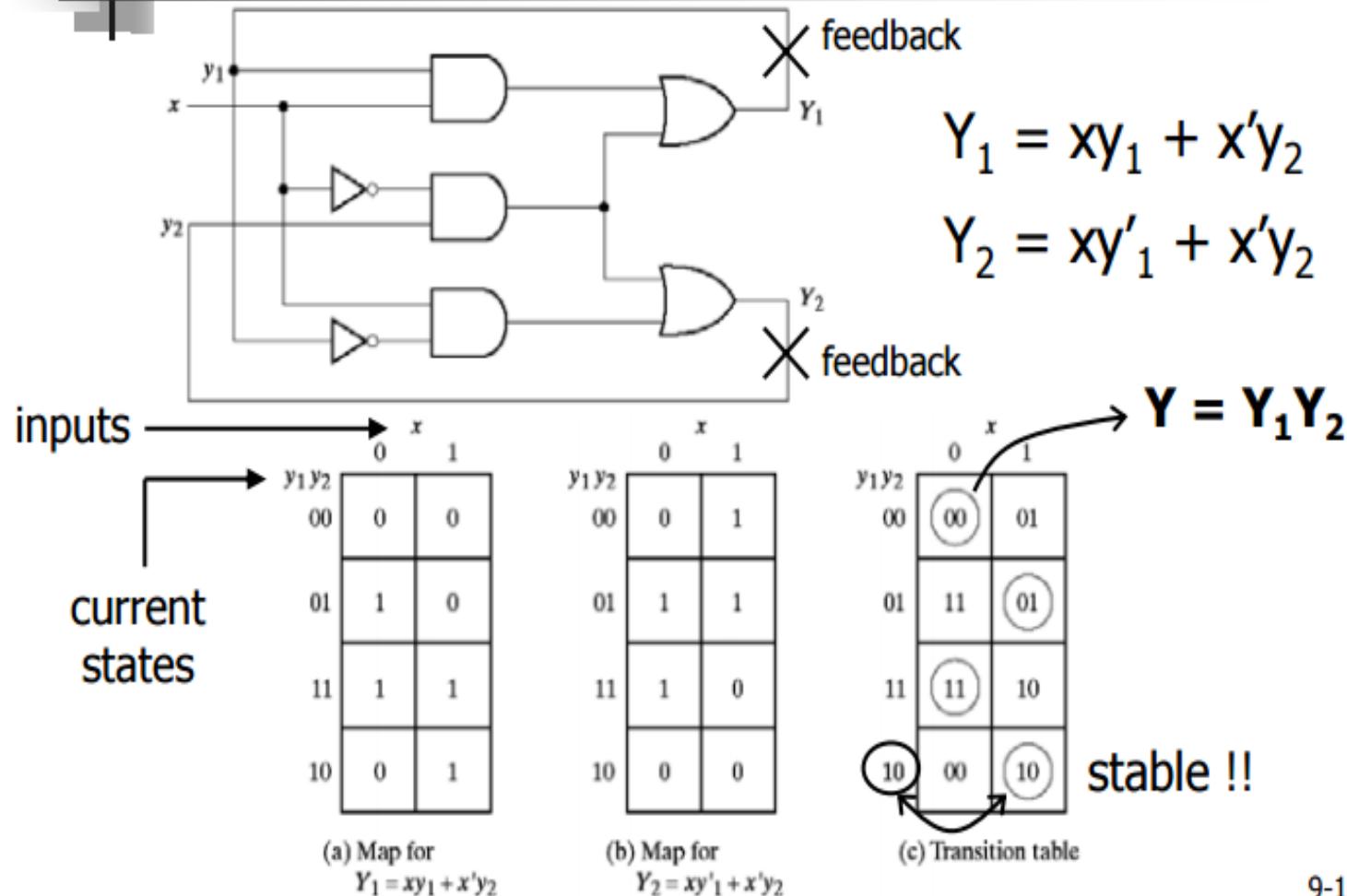
Comparisons

S.No	Synchronous sequential circuits	Asynchronous sequential circuits
1	Memory elements are clocked flip-flops	Memory elements are either unclocked flip-flops or time delay elements.
2	The change in input signals can affect memory element upon activation of clock signal.	The change in input signals can affect memory element at any instant of time.
3	The maximum operating speed of clock depends on time delays involved. Therefore synchronous circuits can operate slower than asynchronous.	Because of the absence of clock, it can operate faster than synchronous circuits.
4	Easier to design	More difficult to design

Transition Table

- Transition table is useful to analyze an asynchronous circuit from the circuit diagram
- Procedure to obtain transition table:
 1. Determine all feedback loops in the circuits
 2. Mark the input (y_i) and output (Y_i) of each feedback loop
 3. Derive the Boolean functions of all Y 's
 4. Plot each Y function in a map and combine all maps into one table
 5. Circle those values of Y in each square that are equal to the value of y in the same row

An Example of Transition Table



State Table

- When input x changes from 0 to 1 while $y=00$:
 - Y changes to 01 → unstable
 - y becomes 01 after a short delay → stable at the second row
 - The next state is $Y=01$
- Each row must have ***at least one*** stable state
- Analyze each state in this way can obtain its state table

		x	0	1
		y_1y_2	00	01
y_1y_2	00	(00)	01	
01	11	(01)		
11	(11)	10		
10	00	(10)		

(c) Transition table

		Present State		Next State	
		X=0		X=1	
y_1y_2	y_1y_2	0	0	0	1
00	00	0	0	0	1
01	11	0	1	1	0
11	(11)	1	1	0	1
10	10	1	0	1	0

y_1y_2x :
total state
4 stable
total states:
000,011,
110,101

Flow Table

- Similar to a transition table except the states are represented by **letter symbols**
- Can also include the output values
- Suitable to obtain the logic diagram from it
- Primitive flow table:

only one stable state in each row
(ex: 9-4(a))

Equivalent to 9-3(c) if
 $a=00$, $b=01$, $c=11$, $d=10$

		x	
		0	1
a	0	a	b
	1	c	b
	0	c	d
	1	a	d

(a) Four states with one input

		$x_1 x_2$			
		00	01	11	10
a	00	a , 0	a , 0	a , 0	b , 0
	01	a , 0	a , 0	b , 1	b , 0

(b) Two states with two inputs and one output

Definitions:

State Table:

The relationship that exists among the inputs, outputs, present **states** and next **states** can be specified by either the **state table** or the **state** diagram

Transition Table:

Transition table is table of states and transition, useful to analyze an asynchronous circuit from the circuit diagram

Flow Table:

In a flow table the states are named by letter symbols

1. An asynchronous sequential circuit is described by the following excitation and output function,

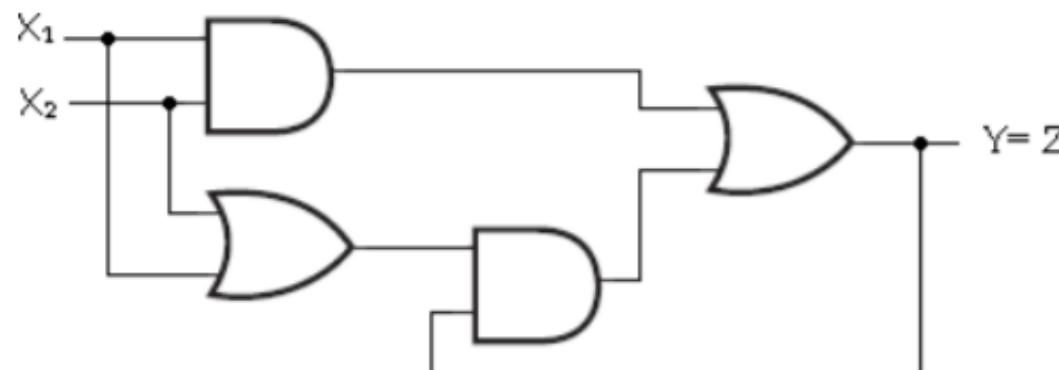
$$Y = x_1 x_2 + (x_1 + x_2) y$$

$$Z = Y$$

- Draw the logic diagram of the circuit.
- Derive the transition table, flow table and output map.
- Describe the behavior of the circuit.

Soln:

- The logic diagram is shown as,



Logic diagram

y	x_1	x_2	x_1x_2	$(x_1+x_2)y$	$Y = x_1x_2 + (x_1+x_2)y$	\downarrow	$Z = Y$
0	0	0	0	0	0	Y	0
0	0	1	0	0	0	Y	0
0	1	0	0	0	0	Y	0
0	1	1	1	0	1	N	1
1	0	0	0	0	0	N	0
1	0	1	0	1	1	Y	1
1	1	0	0	1	1	Y	1
1	1	1	1	1	1	Y	1

STABLE

$$Y = x_1x_2 + (x_1+x_2)y$$

$$Z = Y$$

Output map:

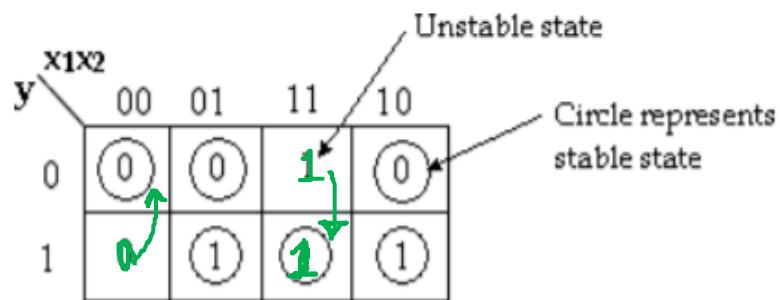
Output is mapped for all stable states. For unstable states output is mapped unspecified.

$y \backslash x_1x_2$	00	01	11	10
0	0	0	-	0
1	-	1	1	1

Flow table:

Assign $a=0$; $b=1$

Transition table:



$y \backslash x_1x_2$	00	01	11	10
0	a	a	b	a
1	a	b	b	b

2. Design an asynchronous sequential circuit that has two internal states and one output. The excitation and output function describing the circuit are as follows:

$$Y_1 = \underline{x}_1 \underline{x}_2 + \underline{x}_1 \underline{y}_2 + \underline{x}_2 \underline{y}_1$$

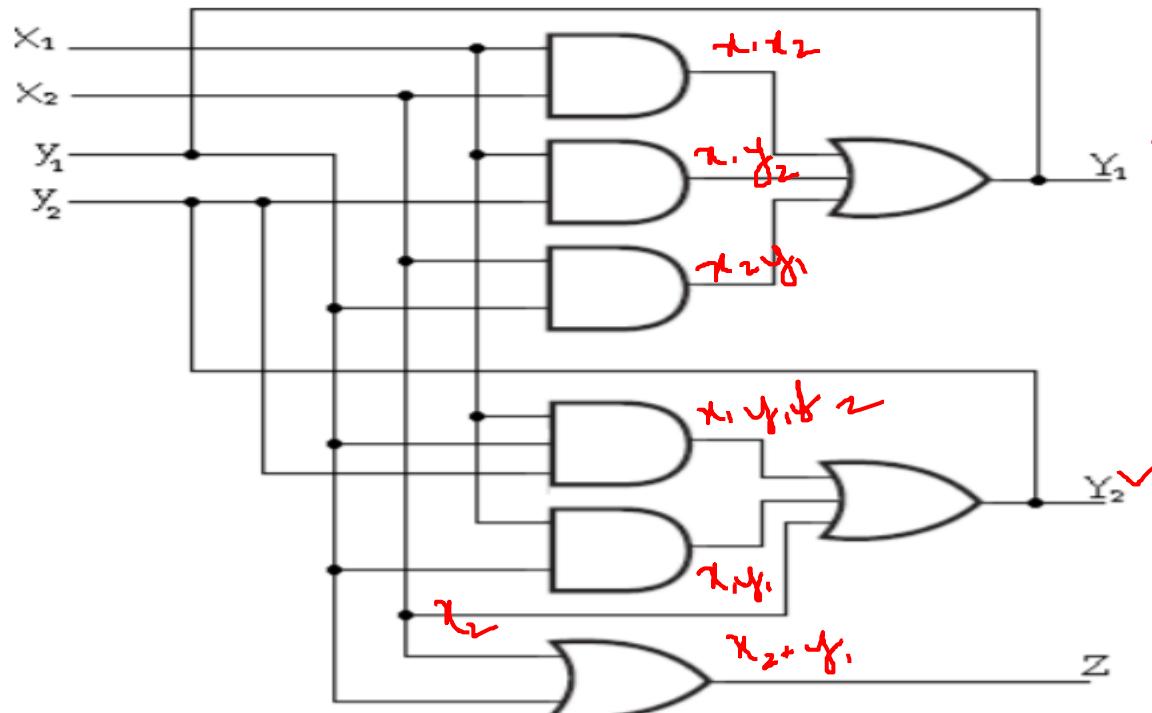
$$Y_2 = \underline{x}_2 + \underline{x}_1 \underline{y}_1 \underline{y}_2 + \underline{x}_1 \underline{y}_1$$

$$Z = \underline{x}_2 + \underline{y}_1.$$

- Draw the logic diagram of the circuit.
- Derive the transition table, output map and flow table.

Soln:

- The logic diagram is shown as,



Logic Diagram

Transition table and Output map

		Map for Y ₁ Y ₂			
		00	01	11	10
y ₁ y ₂	x ₁ x ₂	00	01	11	10
	00	(00)	01	11	(00)
01	00	(01)	11	10	
11	00	(11)	(11)	(11)	
10	00	11	11	01	

Transition table

		x_1x_2	00	01	11	10
y_1y_2		00	0	-	-	0
		01	-	1	-	-
11		-	1	1	1	1
		-	-	-	-	-

Output map

$$\begin{aligned}Y_1 &= x_1x_2 + x_1y_2 + x_2y_1 \\Y_2 &= x_2 + x_1y_1y_2 + x_1y_1 \\Z &= x_2 + y_1.\end{aligned}$$

y_1	y_2	x_1	x_2	x_1x_2	x_1y_2	x_2y_1	$x_1y_1y_2$	x_1y_1	y_1	y_2	$Z = x_2 + y_1$	y_1	PS	NP	Stable
0	0	0	0	0	0	0	0	0	0	0	0	0	Y		
0	0	0	1	0	0	0	0	0	0	0	1	1	N		
0	0	1	0	0	0	0	0	0	0	0	0	0	N		
0	0	1	1	1	0	0	0	0	1	1	1	1	N		
0	1	0	0	0	0	0	0	0	0	0	0	0	N		
0	1	0	1	0	0	0	0	0	0	0	1	1	N		
0	1	1	0	0	1	0	0	0	1	0	0	0	N		
0	1	1	1	1	1	0	0	0	1	1	1	1	N		
1	0	0	0	0	0	0	0	0	0	0	0	1	N		
1	0	0	1	0	0	1	0	0	1	1	1	1	N		
1	0	1	0	0	0	0	0	1	0	1	1	1	N		
1	0	1	1	1	0	1	0	1	1	1	1	1	N		
1	1	0	0	0	0	0	0	0	0	0	0	1	N		
1	1	0	1	0	0	1	0	0	1	1	1	1	N		
1	1	1	0	0	1	0	1	1	1	1	1	1	N		
1	1	1	1	1	1	1	1	1	1	1	1	1	N		

		Map for Y ₁ Y ₂			
		00	01	11	10
y ₁ y ₂	00	(00)	01	11	(00)
	01	00	(01)	11	10
11	00	(11)	(11)	(11)	(11)
10	00	11	11	11	01

Transition table

Primitive Flow table

Let

$$\square \square = a$$

$$\square 1 = b$$

$$11 = c$$

$$10 = d$$

		x ₁ x ₂			
		00	01	11	10
y ₁ y ₂	a	(a)	b	c	(a)
	b	a	(b)	c	d
c	a	(c)	(c)	(c)	(c)
d	a	c	c	b	

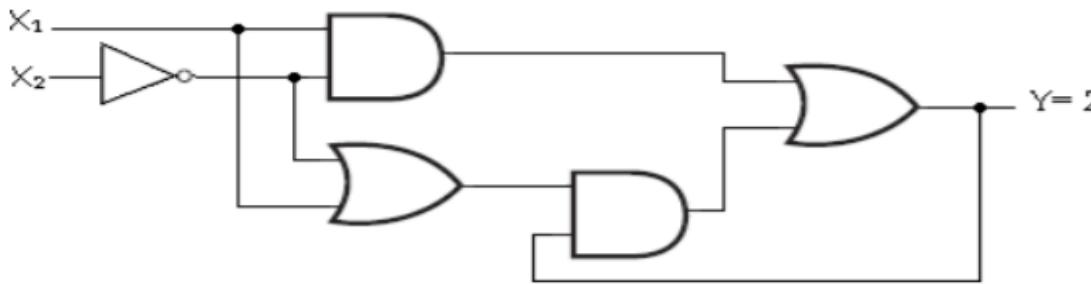
3. An asynchronous sequential circuit is described by the excitation and output functions,

$$Y = x_1 x_2' + (x_1 + x_2') y$$

$$Z = Y$$

- a) Draw the logic diagram of the circuit.
- b) Derive the transition table, output map and flow table.

Soln:



Logic diagram

ii)

y	x ₁	x ₂	x _{2'}	x ₁ x _{2'}	(x ₁ +x _{2'})y	Y = x ₁ x _{2'} + (x ₁ +x _{2'})y	Z = Y
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	1	0	1	1	0	1	1
0	1	1	0	0	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	0	0	0
1	1	0	1	1	1	1	1
1	1	1	0	0	1	1	1

Transition table:

		x ₁ x ₂			
		00	01	11	10
y	0	(0)	(0)	(0)	1
	1	(1)	0	(1)	(1)

Transition Table

Output map:

Output is mapped for all stable states. For unstable states output is mapped unspecified.

		x ₁ x ₂			
		00	01	11	10
y	0	0	0	0	-
	1	1	-	1	1

Output map

Flow table:

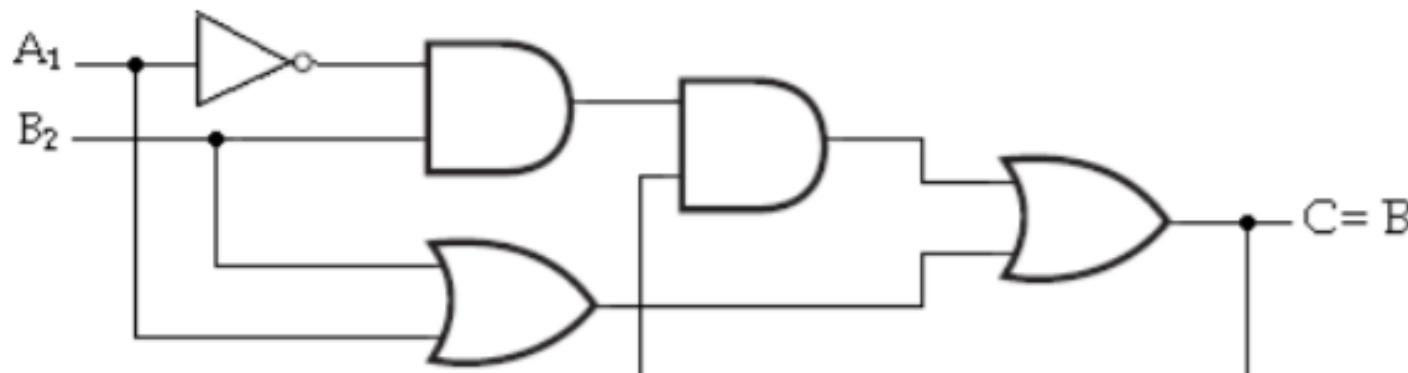
Assign a= 0; b= 1

		x ₁ x ₂			
		00	01	11	10
y	0	(a)	(a)	(a)	b
	1	(b)	a	(b)	(b)

4. An asynchronous sequential circuit is described by the excitation and output functions, $B = (A_1'B_2) + (A_1+B_2)$ $C = B$

- Draw the logic diagram of the circuit.
- Derive the transition table, output map and flow table.

Soln:



Logic Diagram

b	A ₁	B ₂	A _{1'}	(A _{1'} B ₂)b	A ₁ +B ₂	B= (A _{1'} B ₂) b+ (A ₁ +B ₂)	C= B
0	0	0	1	0	0	0	0
0	0	1	1	0	1	1	1
0	1	0	0	0	1	1	1
0	1	1	0	0	1	1	1
1	0	0	1	0	0	0	0
1	0	1	1	1	1	1	1
1	1	0	0	0	1	1	1
1	1	1	0	0	1	1	1

Transition table

		A ₁ B ₂			
		00	01	11	10
b	0	0	1	1	1
	1	0	1	1	1

Output map

Output is mapped for all stable states.

		A ₁ B ₂			
		00	01	11	10
b	0	0	-	-	-
	1	-	1	1	1

Flow table

Assign a= 0; b= 1

		A ₁ B ₂			
		00	01	11	10
b	0	(a)	b	b	b
	1	a	(b)	(b)	(b)