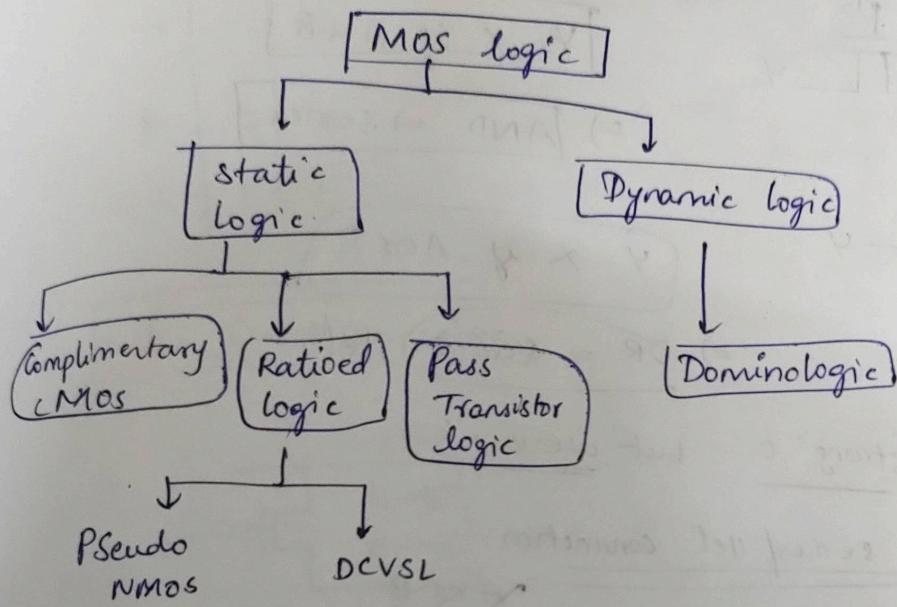


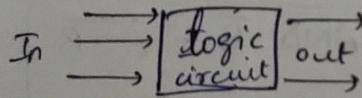
$\frac{1}{2}$  to other  
P-blocks

## Unit - 4

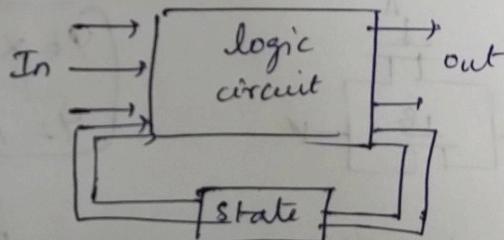
### \* logic style classification:



### • Combinational vs. sequential logic:



$$\text{output} = f(\text{In}) \\ (\text{Combinational})$$



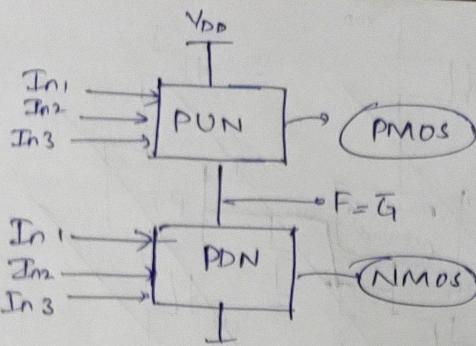
$$\text{output} = f(\text{In}, \text{previousIn})$$

### \* static CMOS circuit: • At every point in time

(except during the switching) each gate o/p is connected  
+ transients

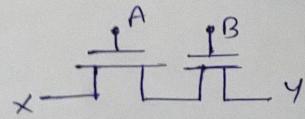
to either VDD (or) VSS via a low-resistive path.

- The o/p of gates assume at all times the value of boolean function, implemented by the circuit.

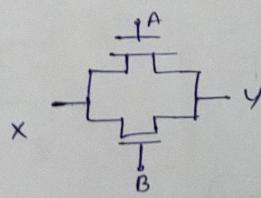


\* NMOS transistors in series / IIel connection:

- transistors can be thought as switch controlled by gate signal. NMOS  $\Rightarrow$  closes when switch control I/P is high



$$Y = X \text{ if } A \neq B$$



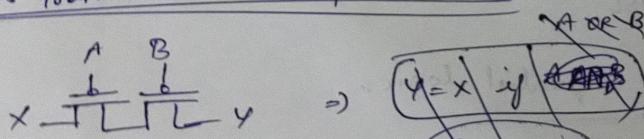
$$\Rightarrow \text{AND} \Rightarrow \text{series}$$

$$Y = X \text{ if } A \otimes B$$

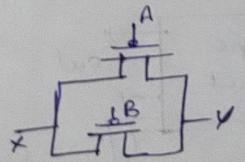
$$\Rightarrow \text{OR} \Rightarrow \text{IIel}$$

NMOS pass a "strong" 0 but "weak" 1

\* PMOS transistors in series / IIel connection:



$$Y = X \text{ if } \overline{A} \otimes \overline{B}$$



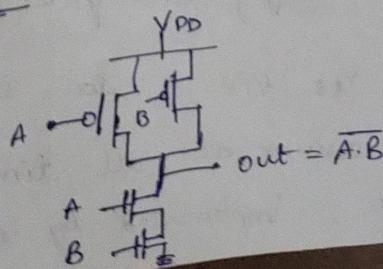
$$Y = X - \text{if } \overline{A} \text{ AND } \overline{B} = \overline{A} + B$$

$$Y = X \text{ if } \overline{A} \text{ or } \overline{B} = \overline{A} \overline{B}$$

PMOS transistors pass strong 1 but weak 0.

\* CMOS construction :-

① NAND gate:-



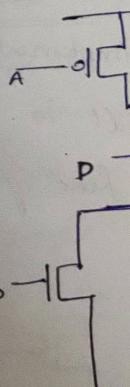
$$\text{out} = \overline{A} \cdot \overline{B}$$

A	B	out
0	0	1
0	1	1
1	0	1
1	1	0

② NOR gate:-

A	B	out
0	0	1
0	1	0
1	0	0
1	1	0

③  $\text{out} = \overline{D} + A$



\* properties of

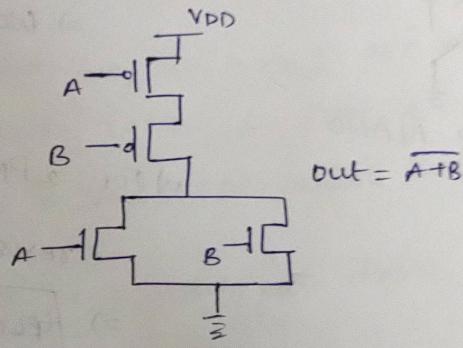
- High noise respectively
- No static direct state con-

A	B	out
0	0	1
0	1	1
1	0	1
1	1	0

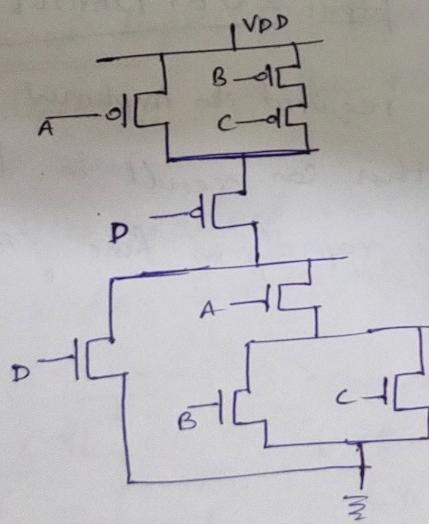
by gate  
V<sub>P</sub> is high

② NOR gate :-  $(\overline{A+B})$

A	B	out
0	0	1
0	1	0
1	0	0
1	1	0



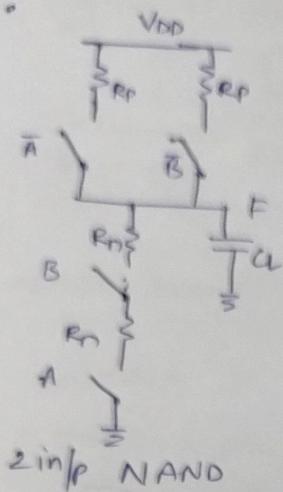
③  $[out = \overline{D+A(B+C)}]$



\* properties of CMOS gates :-

- High noise margins : V<sub>OH</sub> & V<sub>OL</sub> are at V<sub>DD</sub> & GND respectively
- No static power consumption: There never exists a direct path b/w V<sub>DD</sub> & V<sub>SS</sub> (GND) in steady state consumption

## \* Propagation delay analysis - the switch model



Assume  $R_N = R_P$  = resistance of min-sized CMOS inverter

determine "worst case t<sub>PP</sub>" transition  
(delay depends on i/p values)

Ex: t<sub>PLH</sub> for 2-i/p NAND

⇒ Worst case when only one PMOS pulls up the o/p node.

⇒ For 2 PMOS devices in ||sel, the resistance is lower

$$\Rightarrow t_{PLH} = 0.69 R_P C_L$$

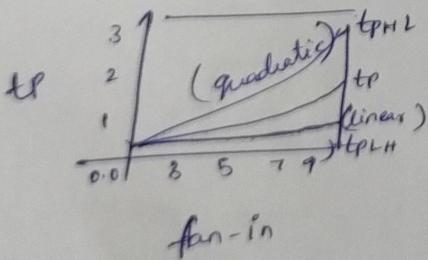
Ex: t<sub>PHL</sub> for 2-i/p NAND

Worst Case: 2-nmos in series

$$t_{PHL} = 0.69 (2R_N) C_L$$

Limitations: ① No. of transistors required to implement an i/p fan-in gate is  $2^n$ , this can result in large area.

② propagation delay is deteriorate rapidly as func. of fan-in



## \* Ratioed logic

- Attempt to reduce no. of transistor to implement a logic func. at cost of reduced robustness and extra power dissipation
- No. of transistor required to N-i/p design
- No. of logic is  $N+1$ .

The o/p or NMOS ratioed to R

⇒ Ratio-les

are inde  
transistor

Ex: Compli

- V

f rela

limitation

function

• Signif

devices

• Propaga

⇒ Ratioed

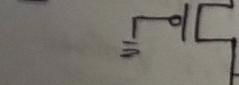
are depend

PDN dev

• In this

by single

Ex: V



z*n*  
*In*2  
*In*3

PD

• This result  
Static po

The o/p voltage swing + overall functionality of ckt depends on NMOS & PMOS size because ratioed logic  $\Rightarrow$  ratio  $\Rightarrow$  size  $= \frac{W}{L}$  of that this logic is called

Ratio-less logic: The high & low voltage levels at the o/p are independent of ratio b/w sizes of PMOS & NMOS transistors

Ex: Complementary CMOS.

- Voltage levels ( $V_{OH} = V_{DD}$ ,  $V_{OL} = V_{SS}$ ) are independent of relative transistors aspect ratios in PUN & PDN.

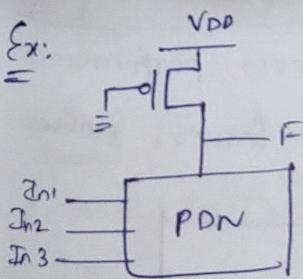
Limitation:- 2N transistors to realize N-variable Boolean function

- Significant load capacitance, each gate drives two devices (PMOS & NMOS) per fanout.

- Propagation delay  $\uparrow$  rapidly as function of fan-in.

Ratioed logic:- A logic style in which o/p voltage levels are dependent upon the relative aspect ratios of PUN & PDN devices.

In this ratioed logic, the entire PUN is replaced by single unconditional load device (that is always on).



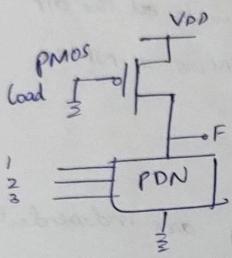
This is called pseudo NMOS.

- The clear advantage of pseudo NMOS is reduced no. of transistors.
- The nominal high o/p voltage ( $V_{O(H)}$ ) for gate is  $V_{DD}$  but nominal low o/p voltage is not (0V) because there is a connection b/w devices in PDN & grounded PMOS.

- This results in reduced noise margin & more importantly static power dissipation. The sizing of load device

relative to Pull-down devices can used to trade off parameters such as noise-margin, propagation delay.

### \* Pseudo-NMOS logic:-



#### Calculation of $V_{OL}$ :-

①  $V_{OL}$  can be obtained by equating the current through driver & load devices for  $V_{in} = V_{DD}$ .

• PMOS load is in saturation mode.

• NMOS device is in linear mode.

$$\Rightarrow \frac{W_n}{L} C_{ox} \left( \frac{W}{L} \right)_n \left( (V_{DD} - V_{tN}) V_{OL} - \frac{V_{OL}^2}{2} \right) + \frac{W_p}{L} C_{ox} \left( \frac{W}{L} \right)_p \left( (-V_{DD} - V_{tSP}) V_{DSATP} - \frac{V_{DSATP}^2}{2} \right) = 0.$$

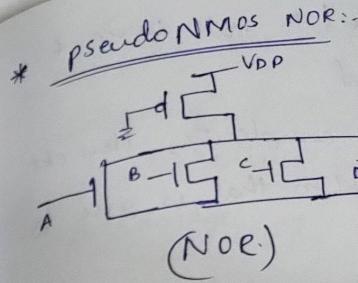
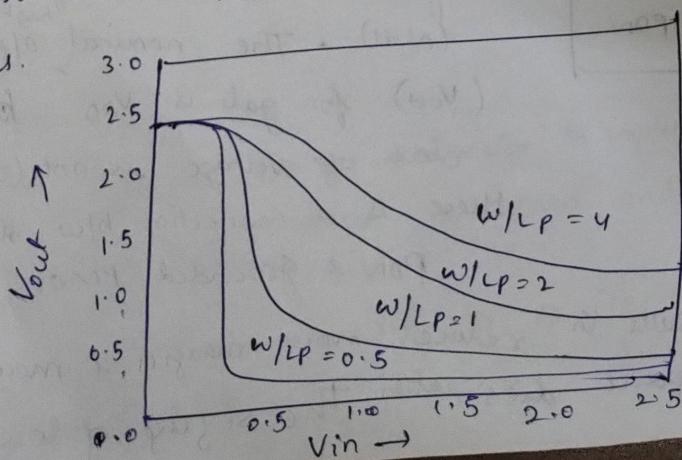
$$\Rightarrow V_{OL} = \frac{W_p W_p}{W_n W_n} \cdot V_{DSATP}$$

• In order to make  $V_{OL}$  small, PMOS load width must be very small as compared to NMOS. But this has a -ve impact on propagation delay for charging up the o/p node.

#### Static power consumption in low o/p mode:-

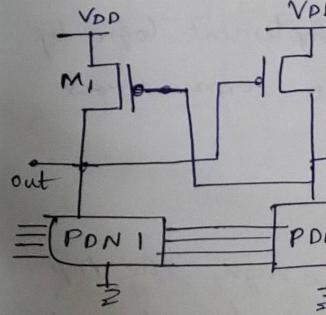
$$P_{low} = V_{DD} I_{low} \approx V_{DD} / k_p \left( C - V_{DD} - V_{tP} \right) V_{DSATP} - \frac{V_{DSATP}^2}{2}$$

• A larger pull-up device not only improves performance but also ↑ static power dissipation & lowers noise margins.



How to build better  
• It is possible to completely eliminate rail swing. Such logic & positive feedback that the load needed. An example

Differential cascode



Working :- . Assume

and  $PDN_1$  i

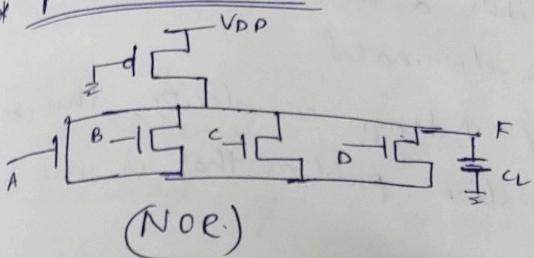
• Turning  $PDN_1$  to 0. When

$N_2$  transistor

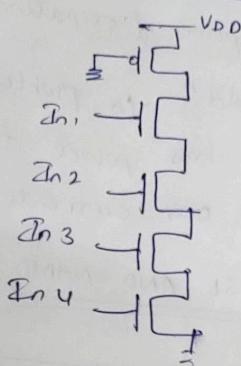
to  $V_{DD}$ . Event

to discharge to  $V_{DD}$

\* pseudo NMOS NOR:-

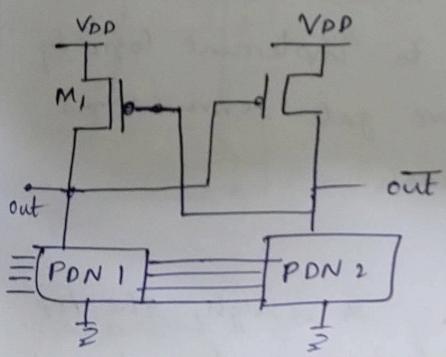


\* pseudo-NMOS N AND



How to build better loads:-

It is possible to create a ratiored logic style that completely eliminates static currents & provides rail-to-rail swing. Such a gate combines 2 concepts: differential logic & positive feedback. The feedback mechanism ensures that the load device is turned off when not needed. An example of such a logic family is called Differential Cascode Voltage Switch Logic (DCVSL).



- The PDN<sub>1</sub> & PDN<sub>2</sub> are NMOS devices.
- PDN<sub>1</sub> & PDN<sub>2</sub> are mutually exclusive. The required function and its complement are simultaneously implemented with PDN<sub>1</sub> & PDN<sub>2</sub>.

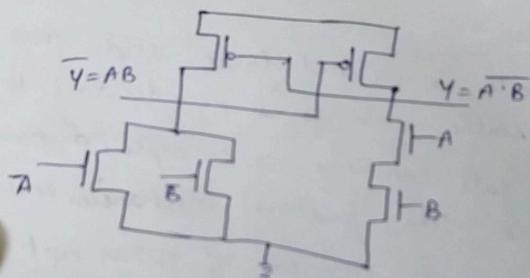
Working :- Assume for given set of i/p, PDN<sub>1</sub> is on

and PDN<sub>2</sub> is off + out=1,  $\overline{OUT}=0$  initially.

Turning PDN<sub>1</sub> ON, causes out to be discharged to 0. When out reaches below  $V_{DD} - V_{TP}$ , the  $N_2$  transistor conducts & causes  $\overline{OUT}$  to start charging to  $V_{DD}$ . Eventually  $M_1$  turns OFF. This enables out to discharge completely to 0 &  $\overline{OUT}$  to charge completely to  $V_{DD}$ .

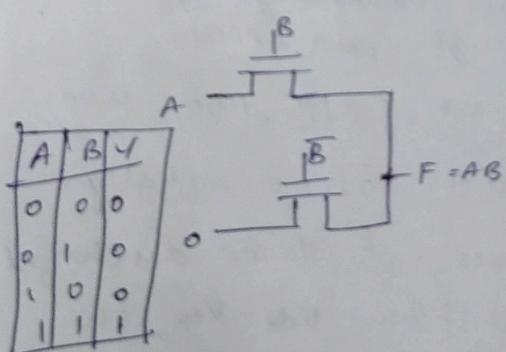
- The resulting circuit exhibits a rail-to-rail swing & static power dissipation is eliminated.
- In add'ly style has to problem of ↑ design complexity, this ckt cross over currents.

\* D'CVSL AND-NAND gate :-



\* Pass-Transistor logic:-

- A popular & widely used alternative to complementary CMOS is pass-transistor logic, which attempts to reduce the no of transistors required to implement logic by allowing memory o/p to drive gate terminals as well as source-drain terminals.
- AND function implementation:-



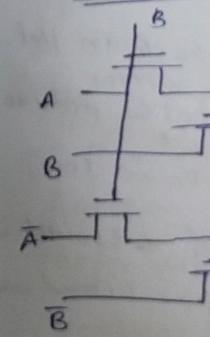
If B is high, the top transistor is turned on & copies the i/p A to o/p F.  
When B is low, bottom pass transistor is turned on & passes a 0.

- The switch driven by B seems to be redundant at 1st glance. Its presence is essential to ensure that gate is static.

So, the including implementation advantage

\* Different  
For high performance logic  
The basic and comp o/p

① AND / N



\* Limitations

• Threshold consumption

\* Robust  
Refer

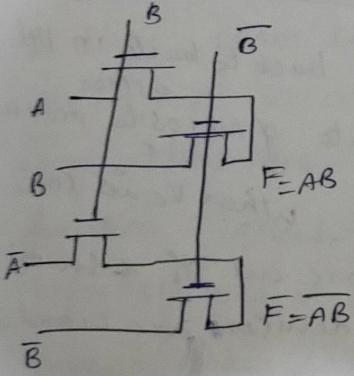
So, the implementation of AND gate requires 4 transistors including inverters for  $\bar{B}$ . While complementary CMOS implementation requires 6 transistors. This has an advantage of lower capacitance.

#### \* Differential pass-transistor logic:-

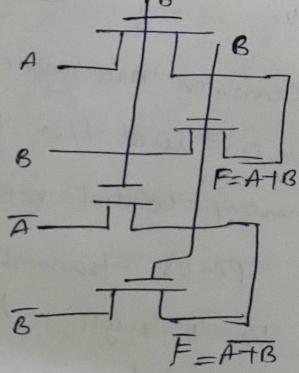
For high performance design, a differential pass-transistor logic family called CPL / DPL is commonly used.

The basic idea (similar to DCVSL) is to accept true and complementary i/p & produce true + complementary o/p

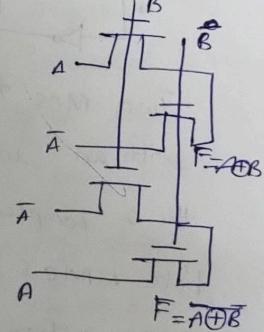
#### ① AND / NAND:-



#### ② OR / NOR:-



#### ③ XOR / XNOR:-



#### \* Limitations of PTL:-

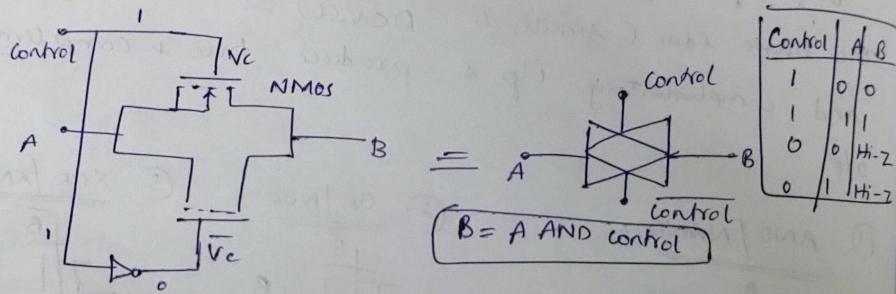
- Threshold voltage loss causes static power consumption.

#### \* Robust & efficient pass-transistor logic design:-

Refer pg - 274

### \* CMOS - transmission gate :-

- The most widely used soln to deal with voltage drop problem is the use of transmission gates. This technique builds on complementary prop. of NMOS + PMOS transistors.
- The ideal approach is to use an NMOS to pull down & PMOS to pull up. The txrn gate combines the best of both device flavors by placing an NMOS device in lvel with PMOS device.

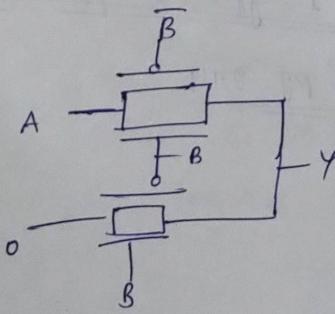


- Two MOS transistors are connected back-to-back in lvel with an inverter used b/w the gate of NMOS & PMOS to provide the 2 complementary control voltages. When V<sub>C</sub> is low, both NMOS & PMOS transistors are cut-off & switch is open. When V<sub>C</sub> is high, both devices are biased into conduction & switch is closed.

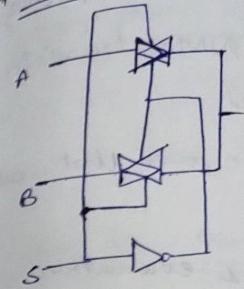
- Thus txrn gate acts as closed switch when V<sub>C</sub> = 1 and acts as open switch when V<sub>C</sub> = 0. This acts as bi directional switch.

Ex: Q/R AND gate :-

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



### \* 2 - i/p mux :-

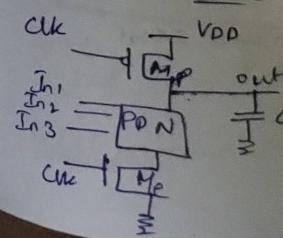


- disadvantage
- chain of propagation
- with no of

### \* dynamic CMOS

- In static CMOS devices, a no. of transistors function in unfortunatly reverse bias.
- An alternate Presented + avoiding sta of clock if Conditional eva

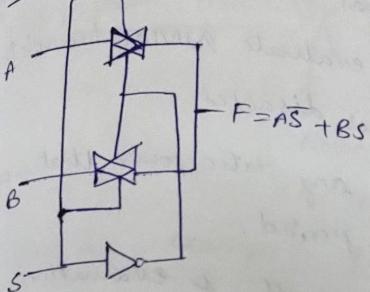
### \* Basic concept



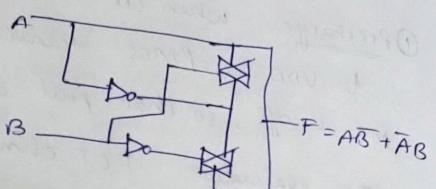
voltage drop  
This technique  
PMOS transistors  
to pull  
combines the  
NMOS device

Control	A	B
1	0	0
1	1	1
0	0	Hi-Z
0	1	Hi-Z

\* 2-1IP mux:-



\* XOR:-



- disadvantage of Txn gate:- delay associated with chain of txn gates.
- propagation delay is prop. to  $n^2 n$  and ↑ rapidly with no. of switches in the chain.

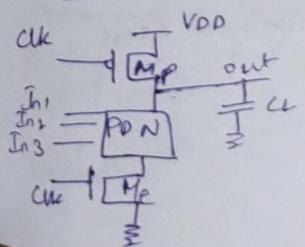
\* dynamic CMOS design:-

In static CMOS logic, with fanIN of N requires  $2N$  devices. A variety of approaches were presented to reduce no. of transistors req. to implement a given logic function including pseudo-nmos, PFL etc. but unfortunately it has static power dissipation due to reverse bias leakage b/w diffusion regions + substrate

An alternate logic style called dynamic logic is presented that obtains a similar result while avoiding static power consumption. With the add' of clock 1IP, it uses a sequence of precharge + conditional evaluation phases.

\* Basic concept of

dynamic gate:-

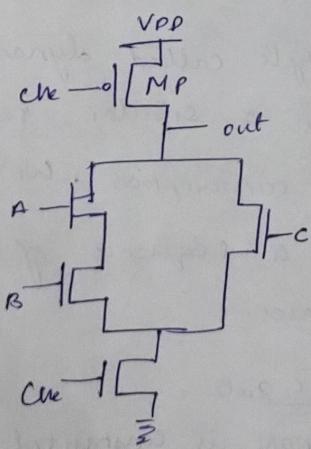


The PDN is constructed exactly as in complementary CMOS. The operation of this ckt is divided into precharge and evaluation phases

With mode of operation determined by CLK

- ① Precharge:- When  $CLK = 0$ , during that time "Out" is precharged to  $VDD$  by PMOS transistor & evaluate NMOS transistors  $M_E$  is off, so that pull-down is disabled.
  - The evaluation FET eliminates any static power that would be consumed during precharge period.
- ② Evaluation:- When  $CLK = 1$ ,  $M_P$  is off & evaluation transistor  $M_E$  is ON. The o/p is conditionally discharged based on  $i_{LP}$  values & pull-down topology.
  - If  $i_{LP}$  are such that PDN conducts, then low resistance path exists b/w Out & GND and the o/p is discharged to GND. If PDN is OFF, precharged value remains stored on o/p capacitance  $C_L$ , which is a combination of junction capacitances.
  - During evaluation phase, the only possible path b/w o/p node & a supply rail is to GND.

Ex:-  $F' = \frac{1}{2} (A \cdot B + C)$  using dynamic logic



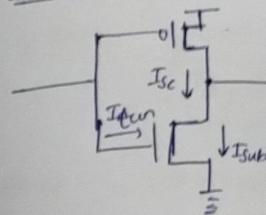
Issue in dynamic logic:-

#### Cascading problem:-

- If several stages of previous CMOS dynamic logic circuit are cascaded together using same clock  $\phi$ , a problem in evaluation involves a built-in race condition will exist.

\* CMOS power dissipation  
• Why power matters  
N  
En

Consider example



Components of CMOS

- ① dynamic power
- ② short circuit
- ③ static current
- ④ leakage current

⇒ Brief MOSFET

① saturation:  $I_S$

② Triode:  $I_D$

③ Subthreshold:-

\* CMOS delay &

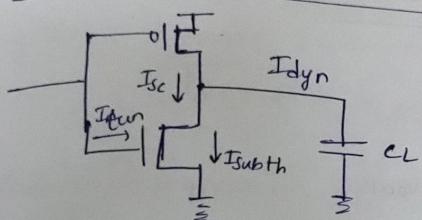
Delay:  $\Delta t = \frac{L}{V_D}$

Total power:-

\* CMOS power dissipation & trends:-

- Why power matters?
  - packaging costs
  - power supply rail design
  - chip & system cooling costs
  - Noise immunity & system reliability.
  - Environmental concern.

Consider example of a CMOS inverter.



Components of CMOS power dissipation:- (Pg - 213, 214 --)

- ① dynamic power  $\Rightarrow$  charging & discharging load capacitances
- ② Short circuit (overlap) current  $\Rightarrow$  occurs when PMOS & NMOS devices on simultaneously
- ③ static current  $\Rightarrow$  Bias circuitry in analog circuits.
- ④ leakage current
  - $\rightarrow$  reverse biased - diode leakage
  - $\rightarrow$  Subthreshold leakage
  - $\rightarrow$  tunneling through gate oxide

⇒ Brief MOSFET review:-

$$\textcircled{1} \text{ saturation: } I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \frac{V_{DS}}{V_{GS}})$$

$$\textcircled{2} \text{ Triode: } I_D = \mu C_{ox} \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$\textcircled{3} \text{ Subthreshold: } I_D = I_S e^{\frac{V_{GS}}{nKT/q}} \left( 1 - e^{-\frac{V_{DS}}{KT/q}} \right)$$

\* CMOS delay & power dissipation :-

$$\text{Delay: } \Delta t = \frac{C \Delta V}{I} = \frac{C_L V_{dd}}{I_D}$$

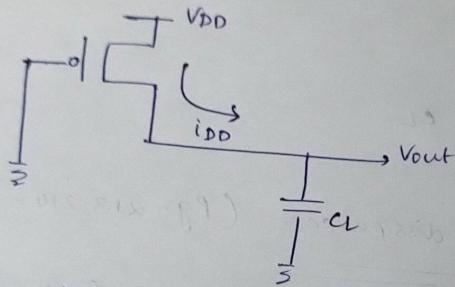
Total power:-

$$P_{\text{tot}} = P_{\text{dyn}} + P_{\text{sc}} + P_{\text{stat}} + P_{\text{leak}}$$

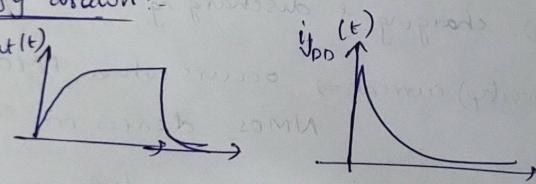
$$= C_L V_{DD}^2 f + V_{DD} I_{\text{peak}} \left( \frac{t_r + t_f}{2} \right) f + V_{DD} I_{\text{static}} + V_{DD} I_{\text{leak}}$$

⇒ To reduce power, minimise each term - starting with the biggest! (dynamic power)

\* Low-to-High Transition Equivalent circuit :-



Energy drawn :-



$$\begin{aligned} E_{VDD} &= \int_0^\infty P_{VDD}(t) dt = \int_0^\infty i_{VDD}(t) V_{DD} dt \\ &= V_{DD} \int_0^\infty C_L \frac{dV_{out}}{dt} dt = C_L V_{DD} \int_0^\infty dV_{out} \end{aligned}$$

$$(E_{VDD} = C_L V_{DD}^2)$$

Energy stored on load capacitor :-

$$\begin{aligned} E_C &= \int_0^\infty i_{VDD}(t) V_{out} dt \\ &= \int_0^\infty C_L \frac{dV_{out}}{dt} V_{out} dt = \frac{1}{2} C_L^2 V_{DD}^2 \end{aligned}$$

Compared to  $E_{VDD}$ , we see that  $\frac{C_L^2 V_{DD}^2}{2}$  is dissipated

: Same amount is dissipated when capacitor is discharged.

- \* deriving diff
- each charge
- to compute frequency
- Typically the power together, do

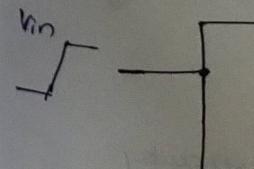
\* Finer litho  
but we have reliability  
voltages to r

\* Minimising

- Voltage +  
— run
- performance
- reduce
- relax

- reduce
- reduce

\* CMOS Inve



expressed as the sum of it  
 $t_s f_0 \rightarrow V_{DD} I_{\text{leak}}$   
y far the dominant factor.  
design, and thus should no  
n the not-too-distant future  
ct (PDP) as a quality m

urrent from the units ( $W$ )  
rate of  $f_{\max} = 1/(2t_p)$ , an  
e power consumption, r  
 $t_p = \frac{C_L V_{DD}^2}{2}$

$I_{\text{Static}} + V_{\text{H}} + I_{\text{Leak}}$

ing with the

#### \* Deriving dynamic power:-

- each charge / discharge cycle dissipates total energy  $E_{\text{VDD}}$
- to compute power, account for switching the ckt at frequency  $f$ .
- Typically DLP does not switch every cycle, so we scale the power by probability of transition " $\alpha$ ." Putting it all together, dynamic power component

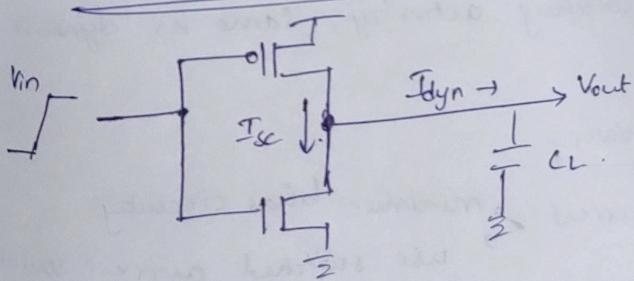
$$P_{\text{dyn}} = \alpha C_L V_{\text{DD}}^2 f$$

\* Finer lithography & thinner oxides imply faster devices but we have to scale the supply voltage to maintain reliability. So, in turn, we have to decrease threshold voltages to maintain performance.

#### \* Minimising dynamic power:-

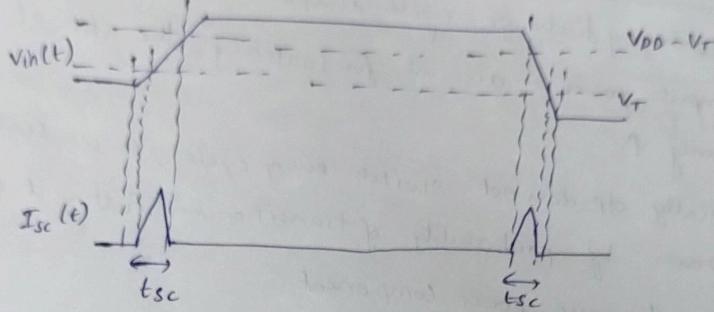
- voltage & frequency scaling (lower  $V_{\text{DD}}, f$ )
  - run high speed circuits at lower voltage to meet performance constraint
  - reduce clock freq. with NCL functional units
  - relax critical path constraints by pipelining
- reduce capacitive load (lower  $C_L$ )
- reduce activity factor (lower  $\alpha$ ).

#### \* CMOS Inverter short circuit current:-



dissipated  
capacitor is

Short circuit current AVE approx.



$$\text{derivation: } E_{sc} = \int_0^\infty I_{sc}(t) V_{dd}(t) dt$$

$$= V_{dd} \frac{I_{peak} t_{sc}}{2} + V_{dd} \frac{I_{peak} t_{sc}}{2}$$

$$E_{sc} = t_{sc} V_{dd} I_{peak}$$

Similar to deriving dynamic power, we must account for switching freq & probability of charge & discharge cycle.

$$\Rightarrow P_{sc} = t_{sc} V_{dd} I_{peak} \times f = C_{sc} V_{dd}^2 f$$

⇒ Duration of both devices conducting:-

$$t_{sc} = \frac{V_{dd} - 2V_T}{V_{dd}} t_{0-100\%} \approx \frac{V_{dd} - 2V_T}{V_{dd}} \times t_{rf}(f)$$

If  $V_T = 0.1 V_{dd}$ , then  $t_{sc} \approx t_{rf}$ .

$$\Rightarrow P_{sc} = V_{dd} I_{peak} \left( \frac{t_{rf} + t_f}{2} \right) f$$

• proportional to switching activity, same as dynamic power.

\* Lowering static power:-

- ① reduce static current  $\hookrightarrow$  minimise bias circuitry  
use switched current sources
- ② reduce Subthreshold leakage.

③ reduce gate

\* Power-delay product

$$PDP = \text{Particular}$$

product of

is generally

• Assume that

2)

$$\Rightarrow PDP = C$$

Adv of PDP:-

gate which

\* Energy-delay

$$\Rightarrow EDP = PDP$$

• weight per

• higher vo

⇒ Putting all

$$P_{tot} = P_{dy}$$

$$P_{tot} = (C_L$$

③ reduce gate tunneling leakage

\* Power-delay product (PDP)

$$PDP = P_{avg} t_{pd}$$

product of average power & propagation delay  $t_{pd}$   
is generally a constant

• Assume that dynamic power dominates

$$\Rightarrow f_{fast} = \frac{1}{2t_{pd}}$$

$$\Rightarrow PPP = C_L V_{DD}^2 f_{fast} t_{pd} = \frac{C_L V_{DD}^2}{2}$$

Adv of PDP:- → Measures energy needed for switching  
gate which is important.

\* Energy-delay product Pg (226) :-

$$\Rightarrow EDP = PDP \times t_{pd} = P_{avg} t_{pd}^2 = \frac{C_L V_{DD}^2}{2} t_{pd}$$

- weight performance more heavily than PDP
- higher voltages decrease delay but ↑ energy

2) Putting all together

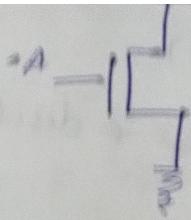
$$P_{tot} = P_{dyn} + P_{dp} + P_{stat}$$

$$P_{tot} = \left( C_L V_{DD}^2 + V_{DD} \cdot \frac{\text{peak } t_s}{f_{osc}} \right) + V_{DD} \cdot I_{leak}$$

$\times t_{pd}$   
0.8

as dynamic

circuit  
current sources



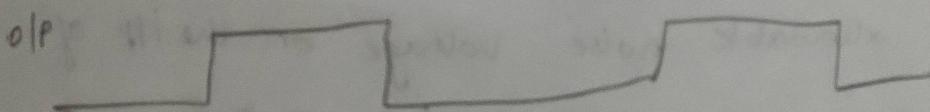
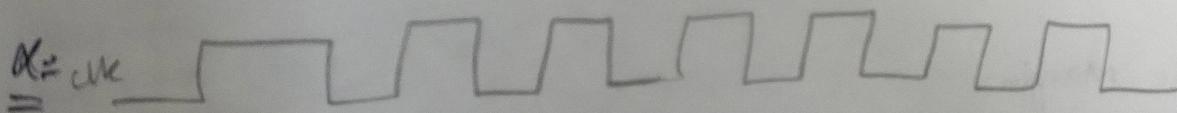
## Power dissipation in CMOS:- Unit - 4

$P_{tot} = \text{dynamic switching}$  + static power dissipation + leakage power dissipation  
 (dynamic power dissipation) (short circuit) (leakage power dissipation)

$$P_{tot} = C V_{dd}^2 f \alpha + I_{sc} V_{dd} + I_{leak} V_{dd}$$

Golden eqn

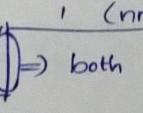
load capacitance → 40-70%  
 supply voltage → 20-40%  
 freq of operation → 10%  
 switching factor → 10%



$\alpha = 2/7$

- Design goal: Design low power system  $\Rightarrow$  reduce the power dissipation
  - Adv:
    - ① Extending battery life
    - ② Green environment
    - ③ Less packing cost (heat sink  $\Rightarrow$  dissipates the heat)
    - ④ Reliability

- We can use Gray code for decoding circuit design.  
 $\Rightarrow$  reduces power  $\Rightarrow$  since it reduces switching activity.  
 Because in Gray code, only bit changes can be occurred.
- Power supply  $\downarrow \Rightarrow$  power dissipation  $\downarrow$  (adv)
  - $\Rightarrow$  delay  $\uparrow$  (drawback).  
 (Because  $V_{DD} \downarrow$ , charging + discharging becomes slow)

$\Rightarrow$   (NMOS on, PMOS off)  
 both are (on) for a short span of time.  
 nmos (off)  $\Downarrow$  produces static current  
 pmos (on)

- leakage:
  - ① Subthreshold leakage
  - ② Gate oxide leakage
- If threshold voltage  $\uparrow$ , subthreshold  $\downarrow$   
 But nowadays / recent times, due to short channel effect, leakage current  $\uparrow$

#### \* Noise Margin:

defines the allowable noise voltage on the I/O of gate so that O/P will not be affected

High noise  
 Low noise  
 $\Rightarrow N_{ML} = V_I$   
 $N_{MH} =$   
 $V_{IL} =$

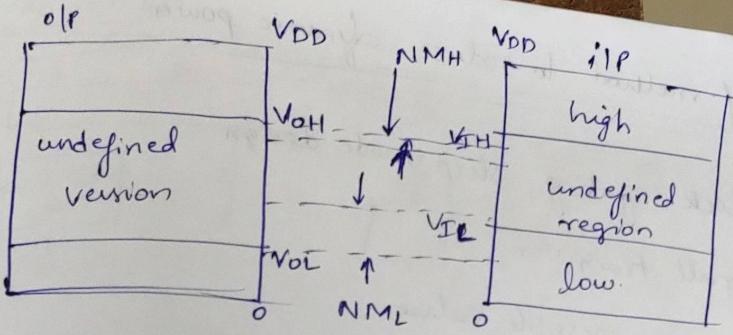
#### Calculation:

$$K_R = \frac{k}{k}$$

$$\Rightarrow V_{IH} =$$

CMOS in V variation.

$V_{out}$   
 Good NMOS bad PMOS



High noise margin  $NM_H$

Low noise margin  $NM_L$ .

$$\Rightarrow NM_H = |V_{IH} - V_{OH}| \quad \text{Value high is good.}$$

$$NM_L = V_{IL} - V_{OL}$$

Calculation:

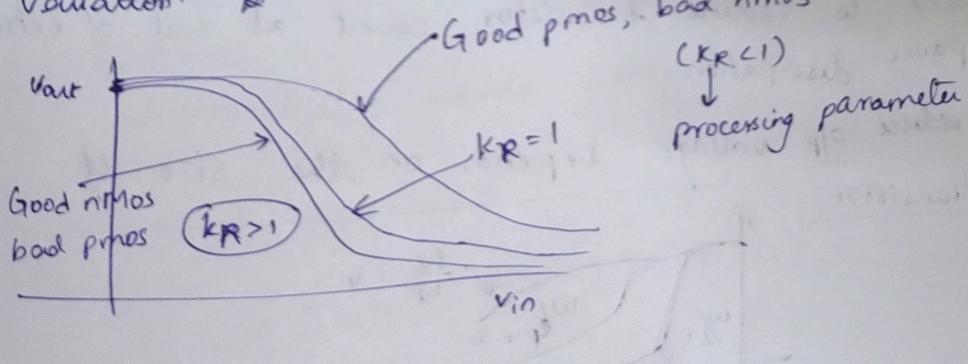
$$V_{IL} = \frac{2V_{out} + V_{TP} - V_{DD} + K_R V_{TN}}{1 + K_R}$$

$$K_R = \frac{k_n}{k_p} = \frac{\mu_n C_{ox} (w/l)_n}{\mu_p C_{ox} (w/l)_p}$$

$$\Rightarrow V_{IH} = \frac{V_{DD} + V_{TP} + K_R (2V_{out} + V_{in})}{1 + K_R}$$

(CMOS inverter) - VTC w.r.t process parameters

Variation:



Some of method to reduce dynamic power:

$\alpha \rightarrow$  clock gating, sleep mode design

$C \rightarrow$  small transistor

$V_{DD} \rightarrow$  lowest possible value

$f \rightarrow$  " frequency "

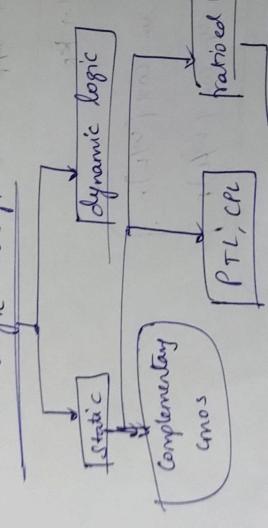
Methods to static power:

\* use ratioed cell

\* use low  $V_T$  device

\* low temp, body bias method

\* CMOS logic design:



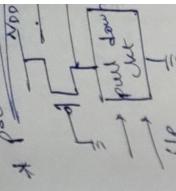
\* ratioed logic:

used to reduce transistor count at cost of extra power dissipation

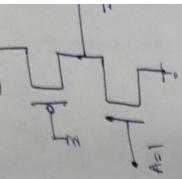
• reduce op voltage depends on the size of transistor

is now expressed

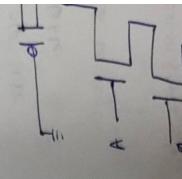
$\frac{W}{L} = 4$



pseudo NMOS:



pseudo NMOS:



pseudo NMOS:

pseudo NMOS:

pseudo NMOS:

DCL

di-

(5.5)

per Operation ( $P_O$ )

$\times V_{DD}^2 f_o^{-1}$

+  $V_{DD}^2 f_o^{-1}$  per unit time

is determined by design.

careful in the no-

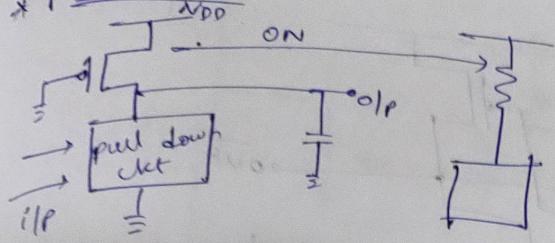
change in

as the rate of consumption.

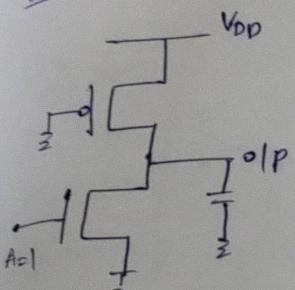
$P_O = P_O^{1/2}$

$\times f_o^{1/2}$

\* pseudo-nmos:



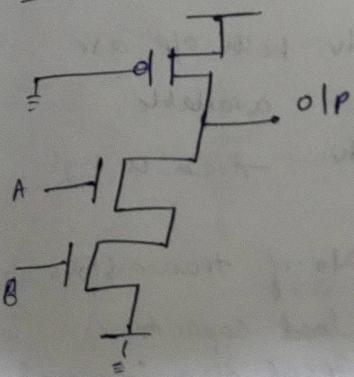
pseudo nmos:- inverter:-



when  $A=1$ ,  $\text{O/P}=0$

when  $A=0$ ,  $\text{O/P}=1$

pseudo nmos : NAND gate:-



$A=1, B=1 \quad \text{O/P}=0$

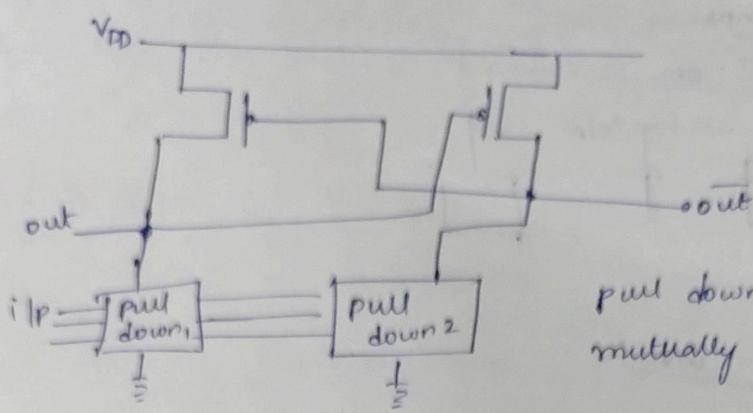
$A=0, B=0 \quad \text{O/P}=1$

$A=0, B=1 \quad \text{O/P}=1$

2) Adv: no. of transistors = 3.

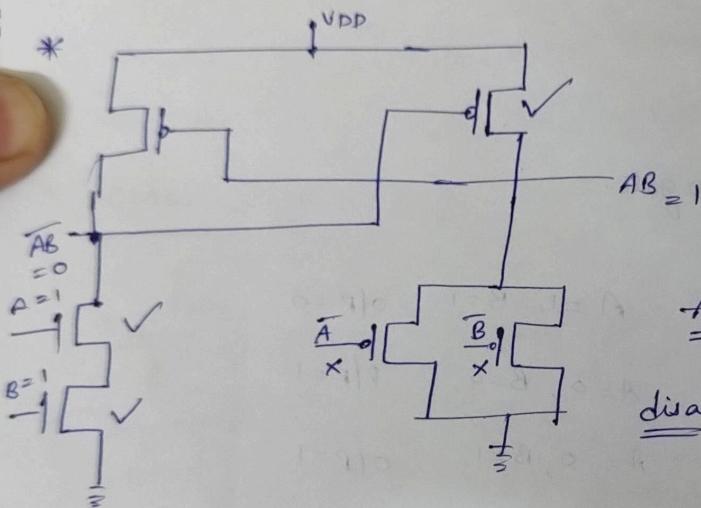
\* for better load,

DCVSL,  
differential cascode voltage switch logic



pull down 1, 2 are mutually exclusive.

Adv: avoid static power dissipation



Adv: both o/p are available  
disadv: Area is high

\* Dynamic CMOS logic design:

No. of transistors = less  
load capacitance.  
Speed also improved

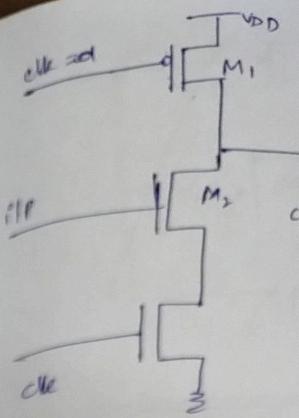
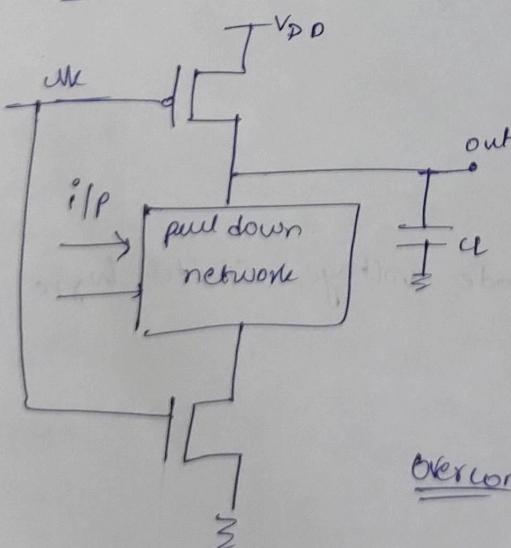
Mode:-

- ① Pre-processing  $clk = 0$
- ② Evaluation  $clk = 1$

Disadvantage:

- ① Cascadelp issue
- ② Race problem (unwanted delay)

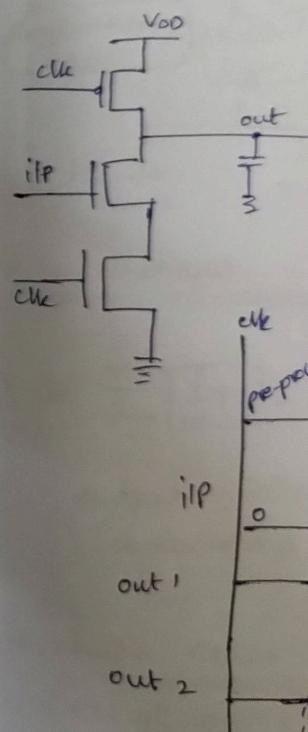
Overcome: Domino CMOS logic  
NORA logic.

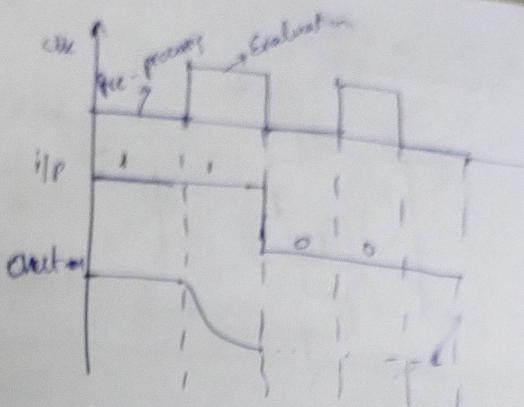
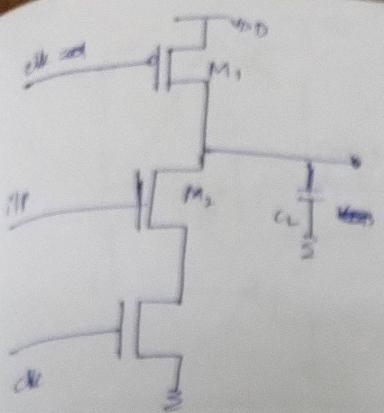


clk = 0:

$$\begin{cases} M_1 = ON \\ M_2 = ON \\ M_3 = OFF \end{cases} \quad \left| \begin{array}{l} C_L = V_{DD} \\ \end{array} \right.$$

\* Cascadelp problem

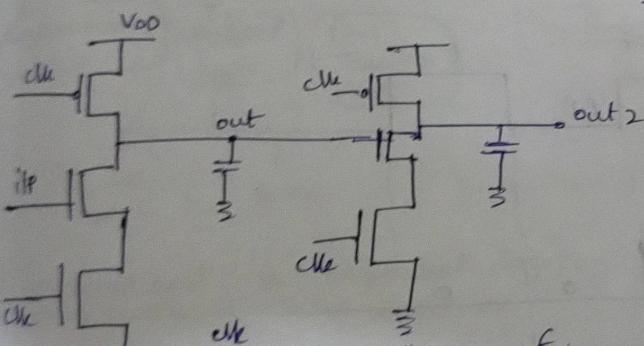




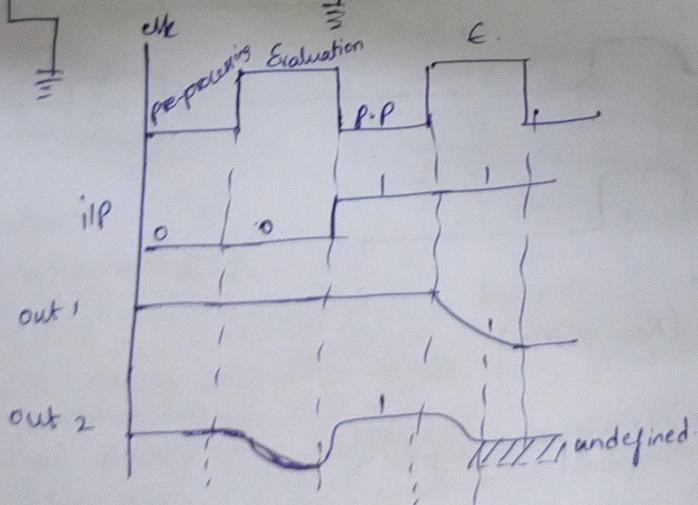
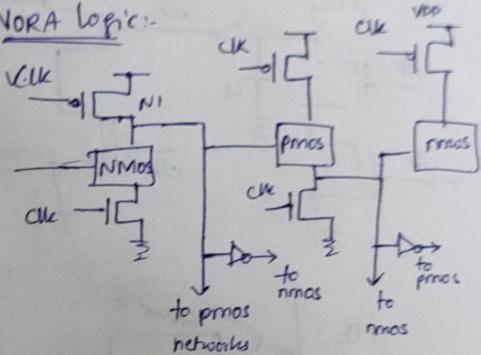
CLL = 0:

$$\begin{array}{l|l} M_1 = \text{ON} & C_L = V_{DD} \\ M_2 = \text{ON} & \\ M_3 = \text{OFF} & \end{array}$$

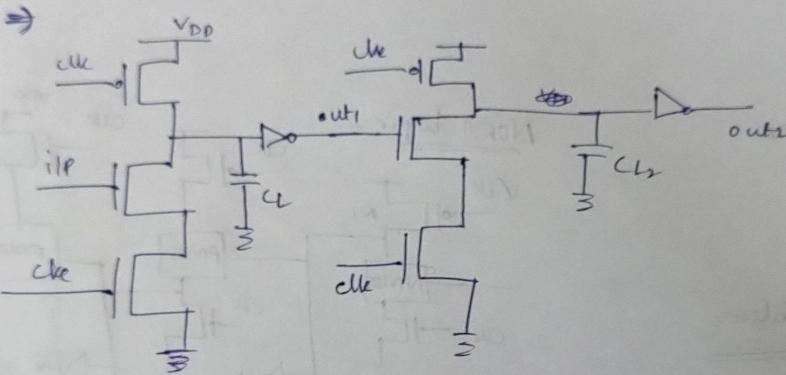
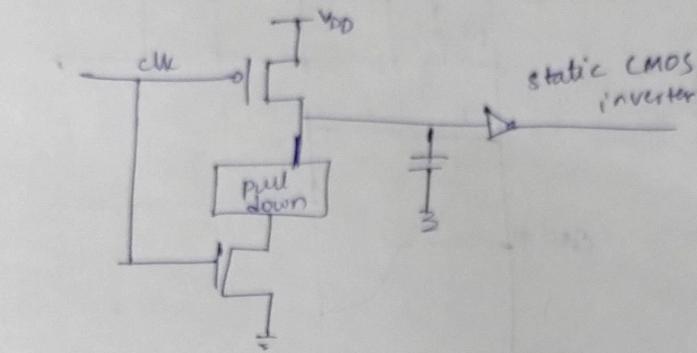
### \* Cascading problem:



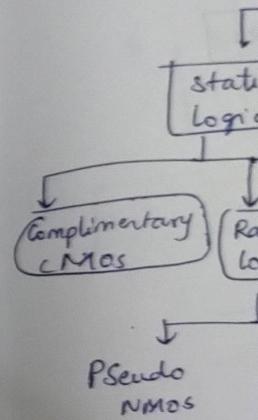
### NORA logic:-



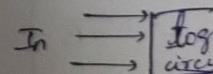
### \* Domino logic:-



### \* logic style



### \* Combinational

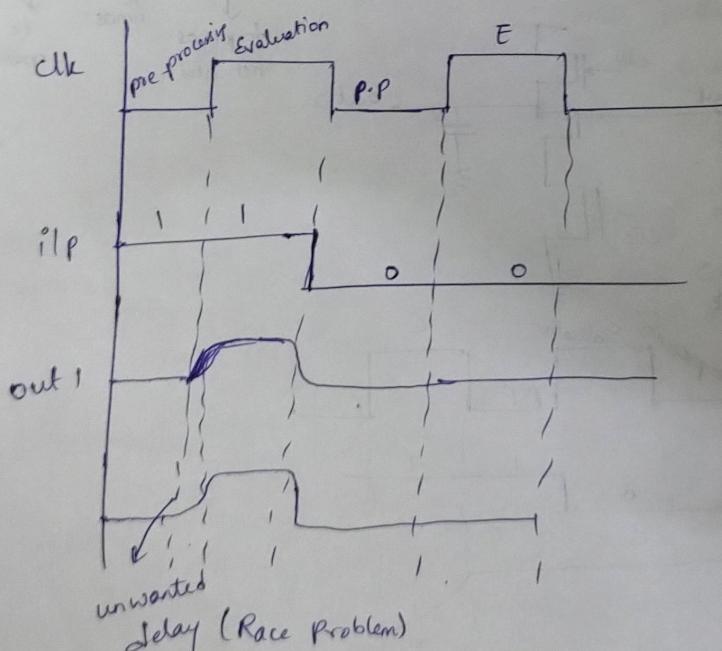


output =  
(Combinational)

### \* static CMOS

(except d  
transis  
to either

The o/p  
of both



### \* NORA (logic) (No-race logic):-

Diagram:-