Unit-5 IC Biasing & Active Load

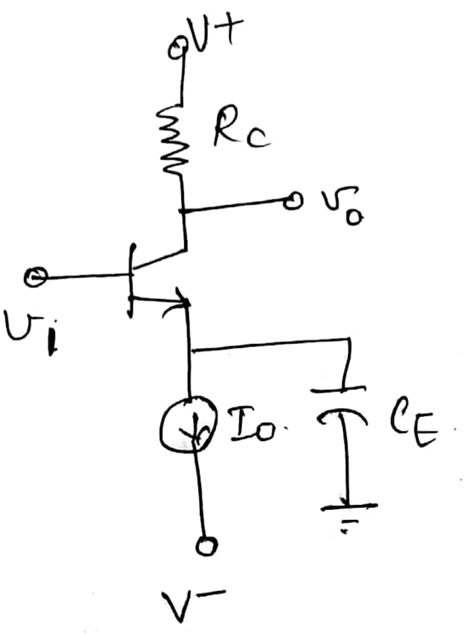
(2) Current Source & Current Mirror

Introduction :-

* The biasing techniques for BJT and FET amplifiers for the most part used voltage-divider resistor networks.
* For IC, this is not possible.
* Resistors require large areas on an IC compared to transistors; therefore a resistor intensive circuit would necessiate a large chip area.
* Also the resistor biasing technique uses coupling & bypass capacitors which is almost impossible to fabricate in uf range.
* Biasing IC involves the use of constant current source.
* Transistors are also used as load instead of R_C & R_D. These are called active loads.

Bipolar Transistor Current Sources

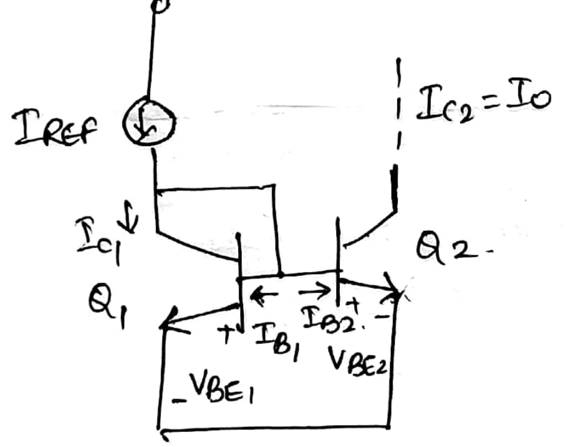
The circuit shown can be designed to establish the bias current I_O.

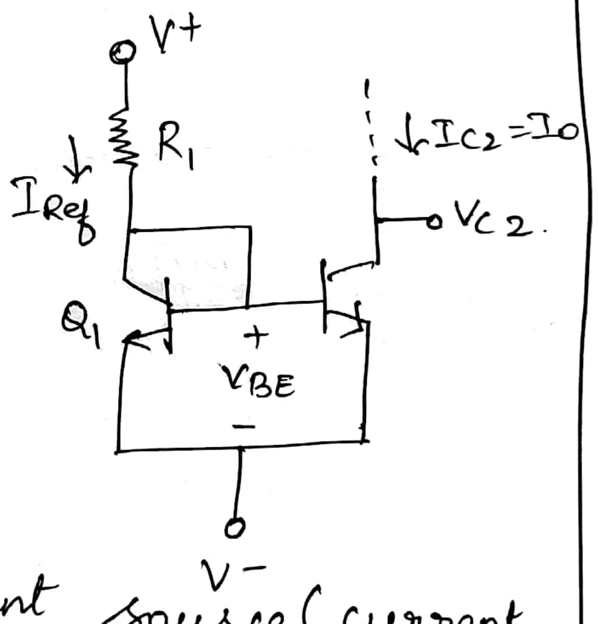


Two transistor Current Source :-

2(b)

2(a)





* The 2 transistor current source (current mirror), is the basic building block in the design of IC current source.
* Q_1 & Q_2 are matched transistors.
* $V_{BE1} = V_{BE2}$.
* base & emitter of two transistors are

connected together.

* Q_1 is connected as a diode, when supply voltages are applied, B-E junction of Q_1 is forward biased, I_{Ref} is established.
* Once V_{BE1} is established it is applied to the base of Q_2 & generates I_o which is used to bias a transistor.

$$\boxed{I_{Ref} = \frac{V^+ - V_{BE} - V^-}{R_1}}$$

* Connecting base & collector terminal produces a 2 terminal device with I-V characteristics identical to i_c vs V_{BE} of BJT.

Current Relationships

$I_{B1} = I_{B2}$

$I_{C1} = I_{C2}$.

Sum of currents at the collector of Q_1

$$I_{Ref} = I_{C1} + I_{B1} + I_{B2} = I_{C1} + 2I_{B2}$$

$$I_{B2} = \frac{I_{C2}}{\beta}$$

$$\therefore I_{Ref} = I_{C1} + \frac{2I_{C2}}{\beta} = I_{C2}\left(1 + \frac{2}{\beta}\right).$$

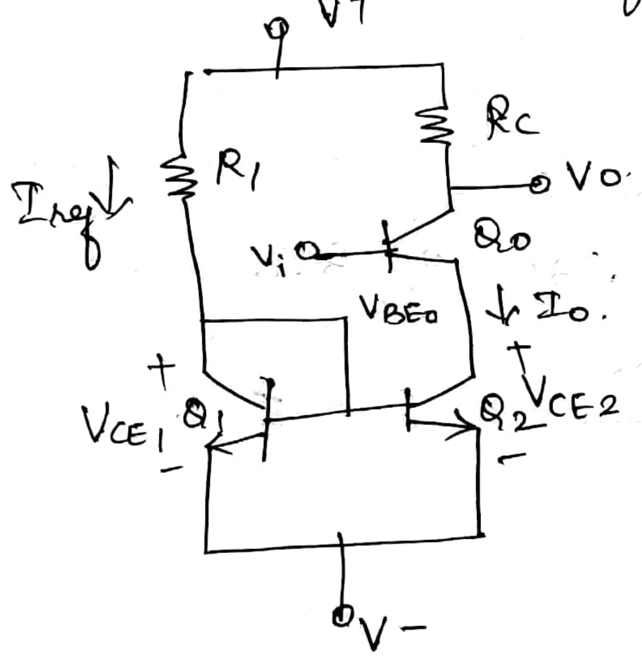
$$\boxed{I_{C2} = \frac{I_{Ref}}{1+\frac{2}{\beta}} = I_o}$$

Q_2 is biased in f/w active region &

$V_A = \infty$.

<u>Output Resistance</u>

* Early effect is finite
Collector current is a function of V_{CE}.



$$\frac{I_o}{I_{ref}} = \frac{1}{1+\frac{2}{\beta}} \frac{\left(1+\frac{V_{CE2}}{V_A}\right)}{\left(1+\frac{V_{CE1}}{V_A}\right)}$$

ratio of load current to reference current taking into a/c early effect.

$V_{CE1} = V_{BE}$ and $V_{CE2} = V^+ - V_{BEo} - V^-$.

* If V_i changes then V_{CE2} changes.
* A change in dc bias conditions in the load circuit affects the collector emitter voltage of Q_2.

SRM

$$\frac{dI_o}{dV_{CE2}} = \frac{I_{ref}}{1+\frac{2}{\beta}} \frac{1}{V_A} \frac{1}{1+\frac{V_{BE}}{V_A}}$$

If $V_{BE} << V_A$

$$\frac{dI_o}{dV_{CE2}} \simeq \frac{I_o}{V_A} = \frac{1}{r_o}.$$

r_o = small signal o/p resistance looking into the collector of Q_2.

Mismatched transistors

Q_1 & Q_2 may not be exactly identical.
If $\beta >> 1$, we can neglect base currents.
The current-voltage relationship for the circuit in Fig. 2(b).

$$I_{Ref} = I_{C1} \simeq I_{S1} e^{V_{BE}/V_T} \rightarrow (1)$$

and

$$I_o = I_{C2} = I_{S2} e^{V_{BE}/V_T} \rightarrow (2)$$

I_{S1} & I_{S2} contain both electrical & geometric parameters of Q_1 & Q_2.
If Q_1 & Q_2 are not identical $I_{S1} \neq I_{S2}$,

$$\frac{I_o}{I_{ref}} = \frac{I_{S2} e^{\cancel{V_{BE}}/V_T}}{I_{S1} e^{\cancel{V_{BE}}/V_T}}$$

$$I_O = I_{ref}\left[\frac{I_{S2}}{I_{S1}}\right] \leftarrow$$ reverse bias saturation current

Any deviation in bias current from the ideal, as a function of mismatch b/w Q_1 & Q_2, is directly related to the ratio of (I_{S2}/I_{S1}).

$I_S \rightarrow$ strong function of temperature.

Q_1 & $Q_2 \rightarrow$ must have the same temperature so should be placed close in the circuit.

Improved Current Source Circuits

Improved load current stability against changes in β & changes in O/P collector current.

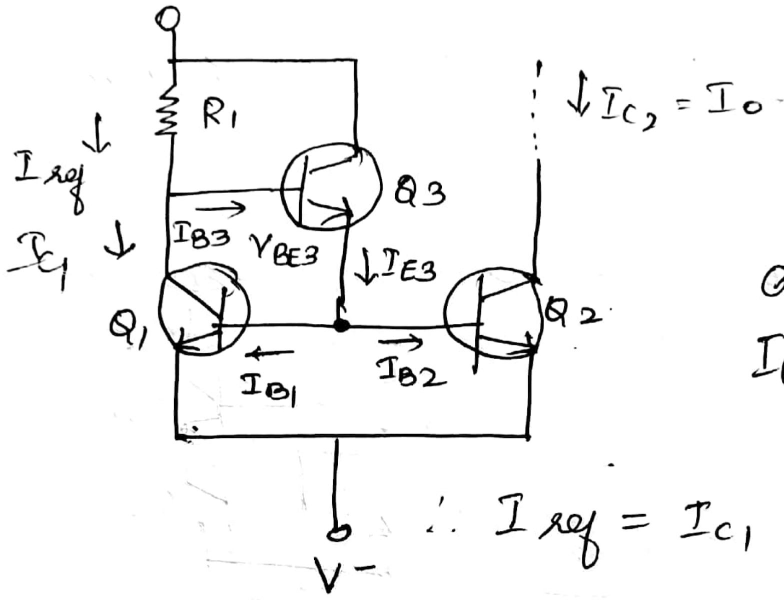
Basic 3 transistor Current Source

all transistors are identical

$I_{B1} = I_{B2}$ & $I_{C1} = I_{C2}$.

Q_3 supplies the base current of Q_1 & Q_2, so these base currents are less dependant on I_{ref}.

Current gain of $Q_1 = Q_2 = \beta$ & current gain of Q_3 is β_3. Summing the currents at the collector node of Q_1, we have,



$$I_{Ref} = I_{C1} + I_{B3}$$

Since

$$I_{B1} + I_{B2} = 2I_{B2} = I_{E3}$$

and

$$I_{E3} = (1+\beta_3) I_{B3}$$

$$\therefore I_{ref} = I_{C1} + \frac{I_{E3}}{1+\beta_3}$$

(or)

$$I_{ref} = I_{C1} + \frac{2I_{B2}}{1+\beta_3} \qquad \left[\begin{array}{l} I_1 = I_{C2} \\ I_{B2} = \frac{I_{C2}}{\beta} \end{array} \right]$$

$$I_{ref} = I_{C2} + \frac{2I_{C2}}{\beta(1+\beta_3)}$$

$$= I_{C2}\left[1 + \frac{2}{\beta(1+\beta_3)}\right]$$

$$\therefore I_o = I_{C2} = \frac{I_{ref}}{\left[1 + \frac{2}{\beta(1+\beta_3)}\right]}$$

SRM

where

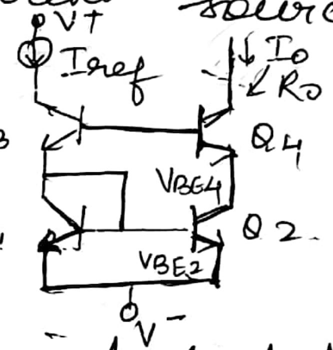
$$I_{ref} = \frac{V^+ - V_{BE3} - V_{BE} - V^-}{R_1} \simeq \frac{V^+ - 2V_{BE} - V^-}{R_1}$$

Compared to 2 transistor current source $I_0 \simeq I_{ref}$ is better for 3 transistor current source.

O/P resistance

Same as 2 transistor current source

$$\frac{dI_o}{dV_{CE2}} = \frac{1}{r_{o2}}.$$



Cascode Current source

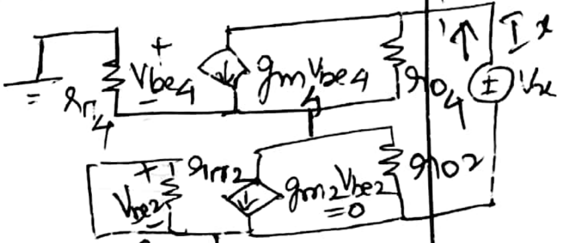
* Current sources can be designed such that the resistance is much greater than that of 2-transistor current source.
* In cascode current source if the transistors are matched, then the load & reference currents are essentially equal.
* We may calculate the o/p resistance R_o by considering the small signal equivalent transistor circuits.
* For a constant reference current V_{BE} of Q_1

and Q_4 are constant, which implies that these terminals are at signal ground.

Since $g_{m2}V_{be2} = 0$ $\quad V_{be4} = -I_x (r_{o4} \| r_{\pi 4})$

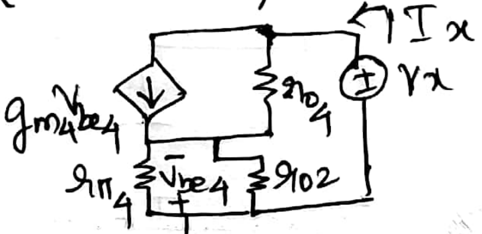
Summing currents at o/p node yields :-

$$I_x = g_{m4} V_{be4} + \left(\frac{V_x - I_x (r_{o2} \| r_{\pi 4})}{r_{o4}} \right)$$



$$I_x = -g_{m4} I_x (r_{o2} \| r_{\pi 4}) + \left(\frac{V_x - I_x (r_{o2} \| r_{\pi 4})}{r_{o4}} \right)$$

$$R_o = \frac{V_x}{I_x}$$



$$I_x + g_{m4} I_x (r_{o2} \| r_{\pi 4}) + \frac{I_x}{r_{o4}} (r_{o2} \| r_{\pi 4}) = \frac{V_x}{r_{o4}}$$

$$I_x \left[1 + g_{m4} (r_{o2} \| r_{\pi 4}) + \frac{1}{r_{o4}} (r_{o2} \| r_{\pi 4}) \right] = \frac{V_x}{r_{o4}}$$

$$\frac{V_x}{I_x} = r_{o4} + g_{m4} r_{o4} (r_{o2} \| r_{\pi 4}) + (r_{o2} \| r_{\pi 4})$$

$$\simeq r_{o4} + g_{m4} r_{o4} r_{\pi 4} + r_{\pi 4}$$

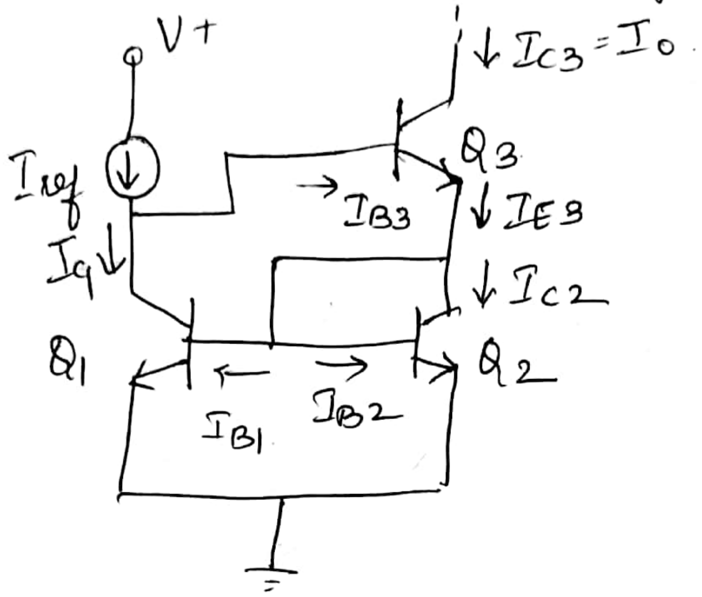
$$= r_{o4} (1 + \beta r_{o4}) + r_{\pi 4} \simeq \beta r_{o4}$$

$$R_o = \frac{V_x}{I_x} \simeq \beta r_{o4}$$

The o/p resistance has increased by a factor of β.

Wilson Current Source

* Has large o/p resistance.
* $I_{B1} = I_{B2}$ & $I_{C1} = I_{C2}$ & current gain of these transistors are equal.



$$I_{ref} = I_{C1} + I_{B3}$$

$$I_{E3} = I_{C2} + I_{B1} + I_{B2} = I_{C2} + 2I_{B2}.$$

$$I_{E3} = I_{C2} + \frac{2I_{C2}}{\beta} = I_{C2}\left(1 + \frac{2}{\beta}\right).$$

$$I_{C2} = \frac{I_{E3}}{1 + 2/\beta}.$$

$$I_{ref} = I_{C2} + I_{B3}. = \frac{I_{E3}}{1+2/\beta} + \frac{I_{E3}}{1+\beta}. \rightarrow (1)$$

$$I_{E3} = (1+\beta) I_{B3}$$

$$I_{E3} = \frac{1+\beta}{\beta} I_{C3}.$$

Sub in (1)

$$I_{Ref} = I_{C3} \frac{1+\beta}{\beta(1+2/\beta)} + I_{C3} \frac{\cancel{1+\beta}}{\beta(\cancel{1+\beta})}$$

$$= I_{C3} \left[\frac{1+\beta}{2+\beta}\right] + \frac{I_{C3}}{\beta}.$$

$$= I_{C3} \left[\frac{1+\beta}{2+\beta} + \frac{1}{\beta}\right].$$

$$\boxed{I_{C3} = \frac{I_{ref}}{\left(\frac{1+\beta}{2+\beta} + \frac{1}{\beta}\right)} = I_o}$$

O/p resistance $\simeq \frac{\beta r_{o3}}{2} \simeq \beta/2.$

Widlar Current Source

* The load & reference currents are nearly equal in other current sources. Hence the Resistor value required is large.

To limit the value of 'R' we use Widlar current source.

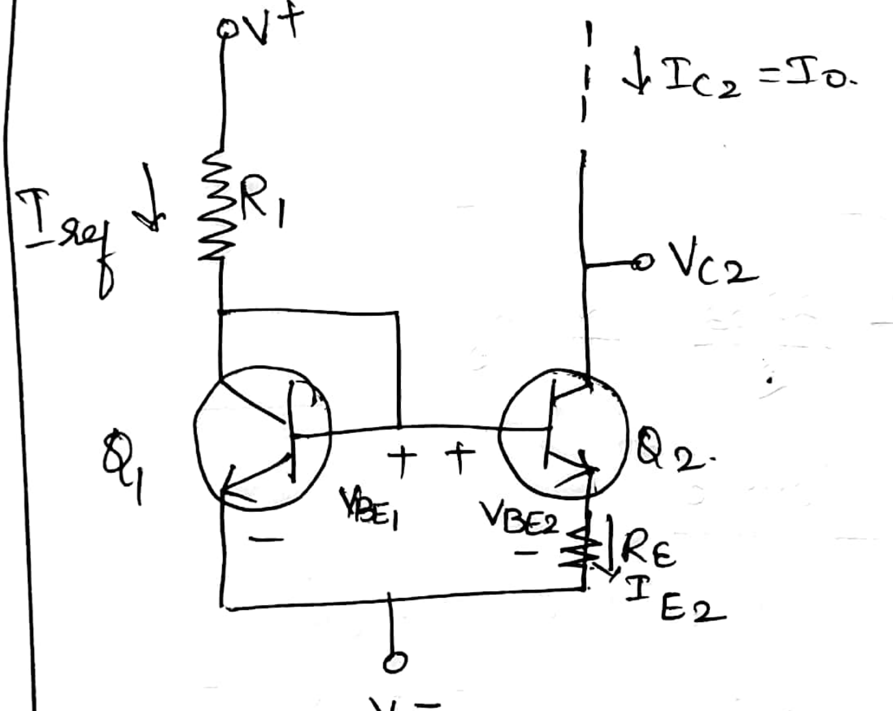
SRM

* A voltage difference is produced across R_E which means B-E voltage of Q_2 is less than B-E voltage of Q_1 hence I_O is smaller than I_{ref}.

<u>Current Relationship</u>

$$I_{ref} \simeq I_{C1} = I_S e^{V_{BE1}/V_T} \rightarrow (1)$$

$$I_O \simeq I_{C2} = I_S e^{V_{BE2}/V_T} \rightarrow (2)$$



From (1) $V_{BE1} = V_T \ln\left(\frac{I_{ref}}{I_S}\right) \rightarrow (3)$

From (2) $V_{BE2} = V_T \ln\left(\frac{I_O}{I_S}\right) \rightarrow (4)$

~~Div~~. From 3 & 4

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{ref}}{I_o}\right).$$

But from fig

$$V_{BE1} = V_{BE2} + I_{E2}R_E$$

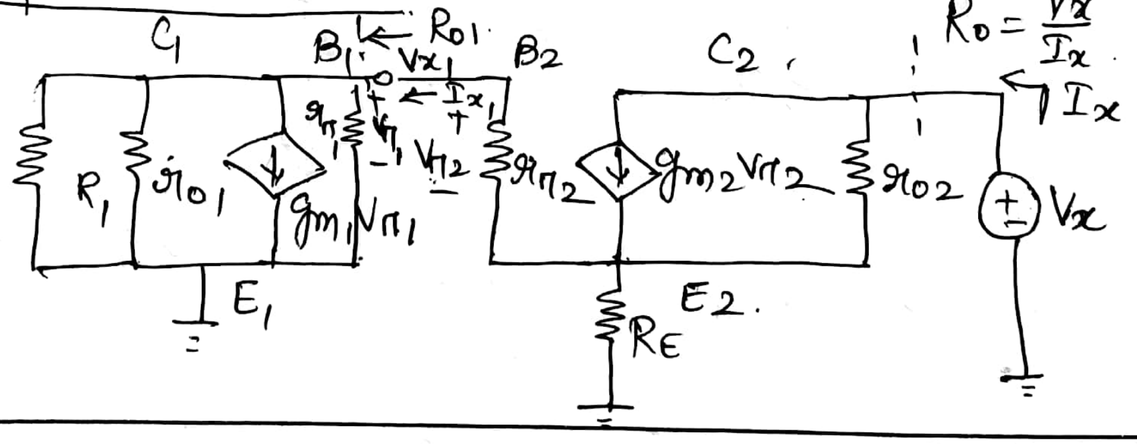
$$\therefore \quad V_{BE1} - V_{BE2} = I_{E2}R_E \simeq I_o R_E$$

$$I_o R_E = V_T \ln\left(\frac{I_{ref}}{I_o}\right).$$

The above equation gives the relationship between I_o & I_{ref}.

With small change in V_{BE} large change in I_c occurs. Maintaining equal temperature is important.

Output Resistance



$$I_x = -g_{m2} I_x (R_E \| r_{\pi 2}) + \frac{V_x}{r_{o2}} - \frac{I_x}{r_{o2}} (R_E \| r_{\pi 2})$$

$$I_x + I_x g_{m2} R_E' + \frac{I_x}{r_{o2}} R_E' = \frac{V_x}{r_{o2}}.$$

$$I_x \left[1 + g_{m2} R_E' + \frac{R_E'}{r_{o2}} \right] = \frac{V_x}{r_{o2}}$$

$$I_x \left[1 + \left(g_{m2} + \frac{1}{r_{o2}} \right) R_E' \right] = \frac{V_x}{R_{o2}}.$$

$$\frac{V_x}{I_x} = r_{o2} \left[1 + R_E' \left(g_{m2} + \frac{1}{r_{o2}} \right) \right].$$

If $1/r_{o2} << g_{m2}$

$$\boxed{R_o \simeq r_{o2} (1 + R_E' g_{m2})}$$

The o/p resistance of Widlar current source is larger than other current sources.

Multitransistor Current Mirrors

B-E voltage of Q_1 can be applied to additional transistors to generate multiple load currents.

$$I_x = -g_{m2} I_x (R_E \| r_{\pi 2}) + \frac{V_x}{r_{o2}} - \frac{I_x}{r_{o2}} (R_E \| r_{\pi 2})$$

$$I_x + I_x g_{m2} R_E' + \frac{I_x}{r_{o2}} R_E' = \frac{V_x}{r_{o2}}.$$

$$I_x \left[1 + g_{m2} R_E' + \frac{R_E'}{r_{o2}} \right] = \frac{V_x}{r_{o2}}$$

$$I_x \left[1 + \left(g_{m2} + \frac{1}{r_{o2}} \right) R_E' \right] = \frac{V_x}{R_{o2}}.$$

$$\frac{V_x}{I_x} = r_{o2} \left[1 + R_E' \left(g_{m2} + \frac{1}{r_{o2}} \right) \right].$$

If $1/r_{o2} << g_{m2}$

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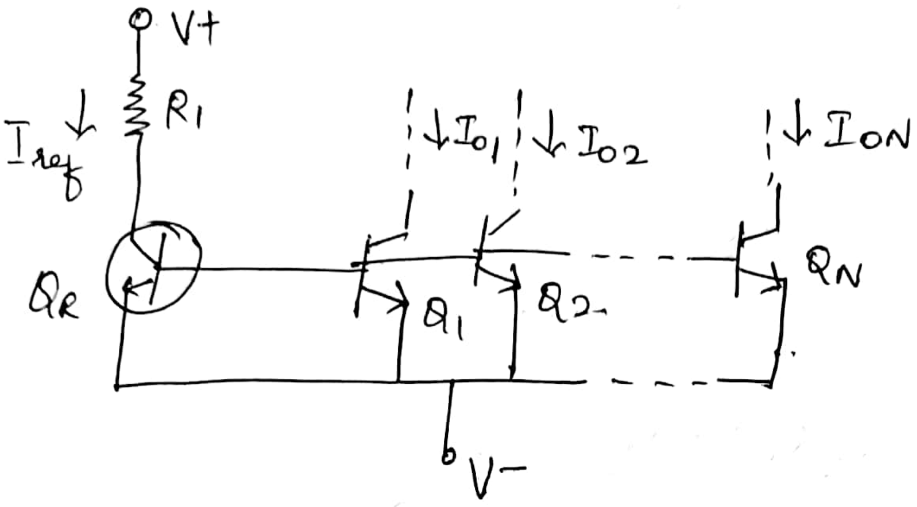
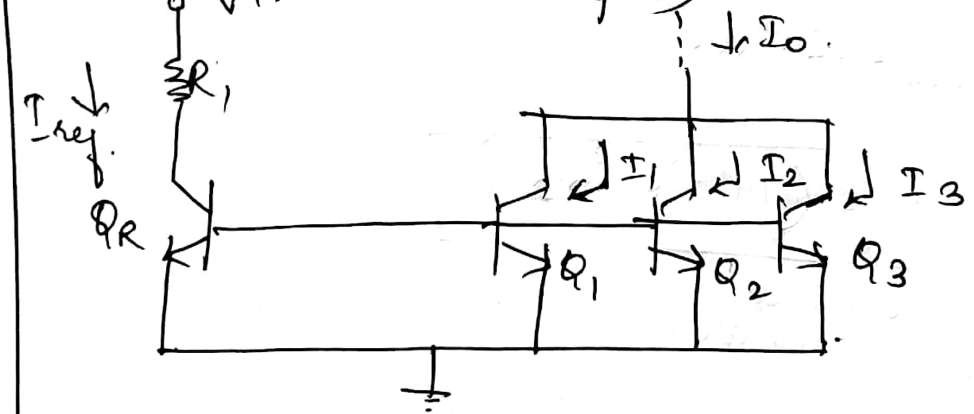


* Q_R is the reference transistor, connected as a diode.
* The Base-Emitter voltage of Q_R is applied to N o/p transistors, creating N load currents. The transistors are matched.

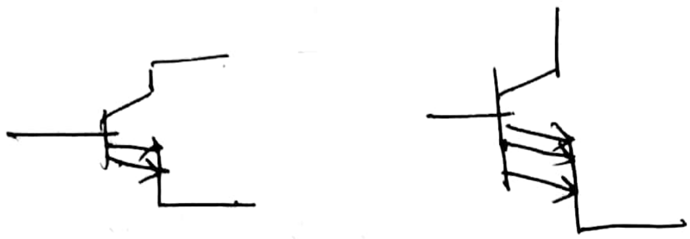
$$I_{o1} = I_{o2} = I_{ON} = \frac{I_{ref}}{1 + \left(\frac{1+N}{\beta}\right)}$$



$$I_o = 3 I_{ref}.$$

* The collectors of multiple transistors can be connected together.

* This increases the B-E area of the device.



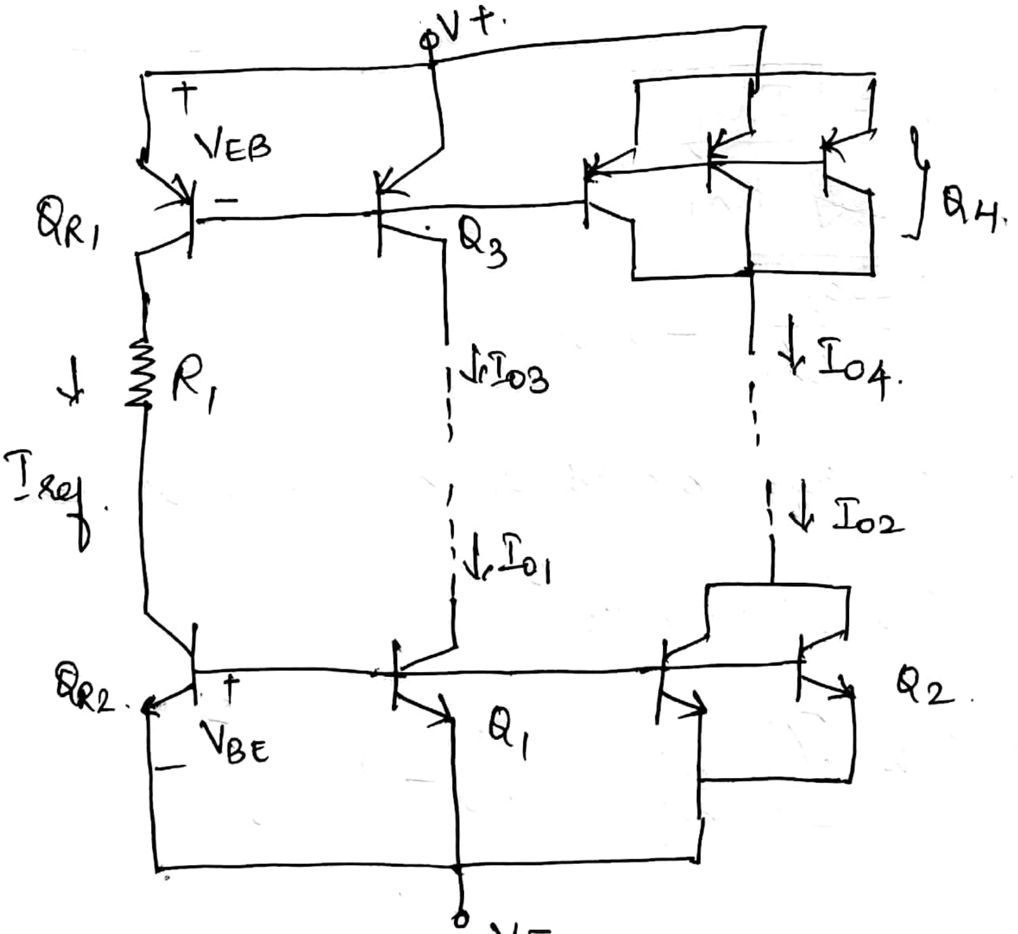
Circuit symbols.

Current Mirror:

$$I_{ref} = \frac{V^+ - V_{EB}(Q_{R1}) - V_{BE}(Q_{R2}) - V^-}{R_1}$$

Q_{R1} & Q_{R2} are connected as diodes.

The reference current is established by Q_{R1} & Q_{R2}.



$I_{O1} = I_{O3} = I_{ref}$ $\quad$ $I_{O2} = 2I_{ref}$

$I_{O4} = 3I_{ref}$

If the aspect ratios of 2 transistors are not same then

$$I_0 = \frac{(W/L)_2}{(W/L)_1} I_{ref}$$

Output resistance

Taking into account the finite output resistance of the transistors, we can write the load & reference currents as,

$$I_0 = K_{n2}(V_{GS} - V_{TN2})^2 (1 + \lambda_2 V_{DS2})$$

&

$$I_{ref} = k_{n1}(V_{GS} - V_{TN1})^2 (1 + \lambda_1 V_{DS1})$$

All the physical parameters are same for both the transistors. hence,

$$\frac{I_0}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1} \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})}$$

$$\frac{1}{R_0} = \lambda I_{ref}$$

3-transistor Current Source

The reference current in bipolar current source circuits is usually established by bias voltage & resistor.

If the aspect ratios of 2 transistors are not same then

$$I_0 = \frac{(W/L)_2}{(W/L)_1} I_{ref}$$

Output resistance

Taking into account the finite output resistance of the transistors, we can write the load & reference currents as,

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&

$$I_{ref} = K_{n1}(V_{GS} - V_{TN1})^2(1 + \lambda_1 V_{DS1})$$

All the physical parameters are same for both the transistors. hence,

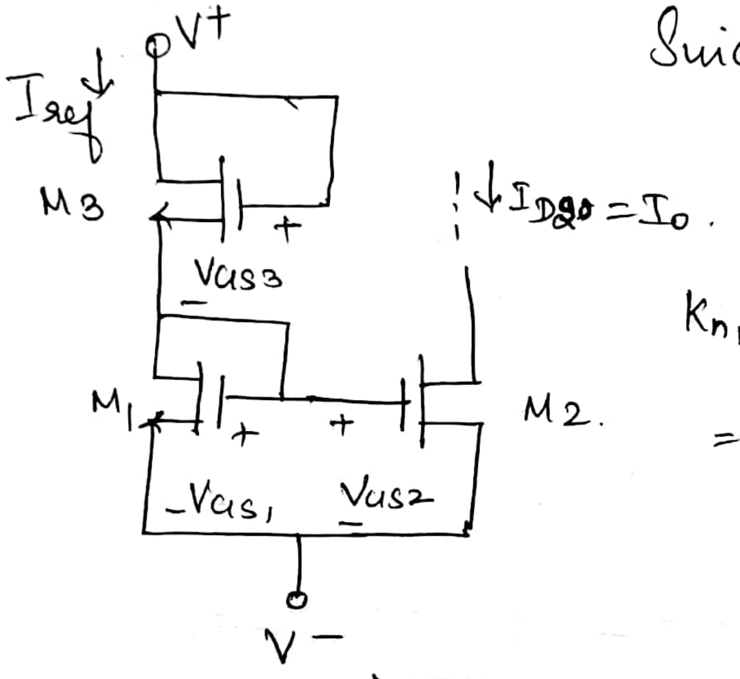
$$\frac{I_0}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1} \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})}$$

$$\frac{1}{R_0} = \lambda I_{ref}$$

3-transistor Current Source

The reference current in bipolar current source circuits is usually established by bias voltage & resistor.

* Since MOSFET can be configured to act like resistor, the reference current is MOSFET current mirror is usually established by using additional transistor.



Since M_1 & M_3 are in series

$$K_{n1}(V_{GS1} - V_{TN1})^2 = K_{n3}(V_{GS3} - V_{TN3})^2$$

$$V_{GS1} - V_{TN1} = \sqrt{\frac{K_{n3}}{K_{n1}}}\,(V_{GS3} - V_{TN3})$$

$$V_{GS1} = \sqrt{\frac{K_{n3}}{K_{n1}}}\,(V_{GS3} - V_{TN3}) + V_{TN1}.$$

$$= \sqrt{\frac{K_{n3}}{K_{n1}}}\cdot V_{GS3} - \sqrt{\frac{K_{n3}}{K_{n1}}}\,V_{TN3} + V_{TN1}.$$

Let $V_{TN3} = V_{TN1} = V_{TN}$ then

$$V_{GS1} = \sqrt{\frac{K_{n3}}{K_{n1}}}\,V_{GS3} + \left(1 - \sqrt{\frac{K_{n3}}{K_{n1}}}\right)V_{TN} \rightarrow (1)$$

Also $V^+ - V^- = V_{GS1} + V_{GS3}. \rightarrow (2)$

Substituting the eqn for V_{GS3} from (2) in (1)

$$V_{GS1} = \sqrt{\frac{(W/L)_3}{(W/L)_1}}\,(V^+ - V^- - V_{GS1}) + \left(1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right) V_{TN}.$$

$$\left[\sqrt{\frac{(W/L)_3}{(W/L)_1}}\,V_{GS1} + V_{GS1}\right] = \sqrt{\frac{(W/L)_3}{(W/L)_1}}\,(V^+ - V^-) + \left(1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right) V_{TN}.$$

$$V_{GS1}\left[1 + \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right] = \sqrt{\frac{(W/L)_3}{(W/L)_1}}\,(V^+ - V^-) + \left(1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right) V_{TN}$$

$$V_{GS1} = \frac{\sqrt{\frac{(W/L)_3}{(W/L)_1}}}{1 + \sqrt{\frac{(W/L)_3}{(W/L)_1}}}\,(V^+ - V^-) + \left(\frac{1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}}{1 + \sqrt{\frac{(W/L)_3}{(W/L)_1}}}\right) V_{TN}$$

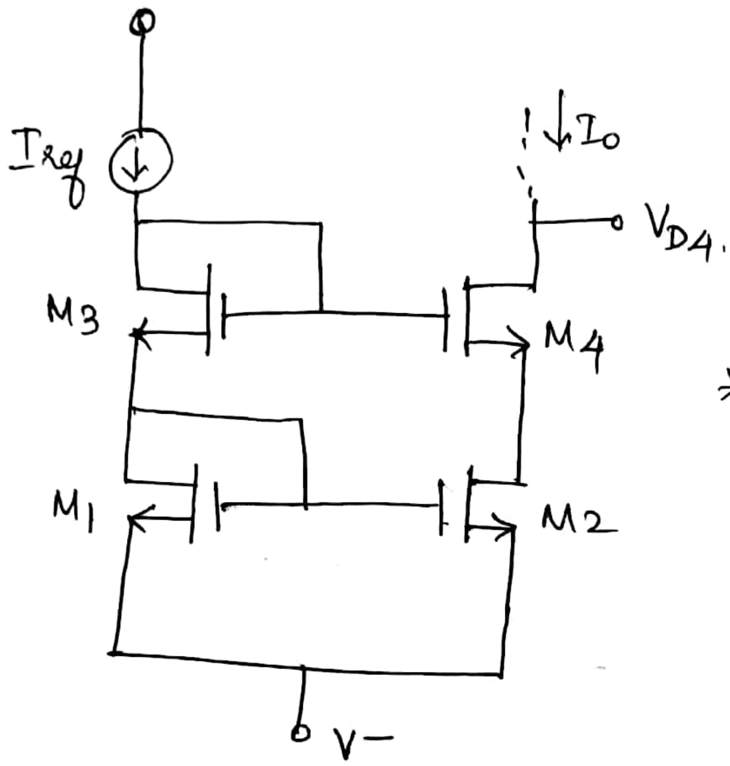
$$= V_{GS2}.$$

The load current

$$I_O = \left(\frac{W}{L}\right)_2 \left(\frac{1}{2}\mu_n C_{ox}\right)\left(V_{GS2} - V_{TN}\right)^2.$$

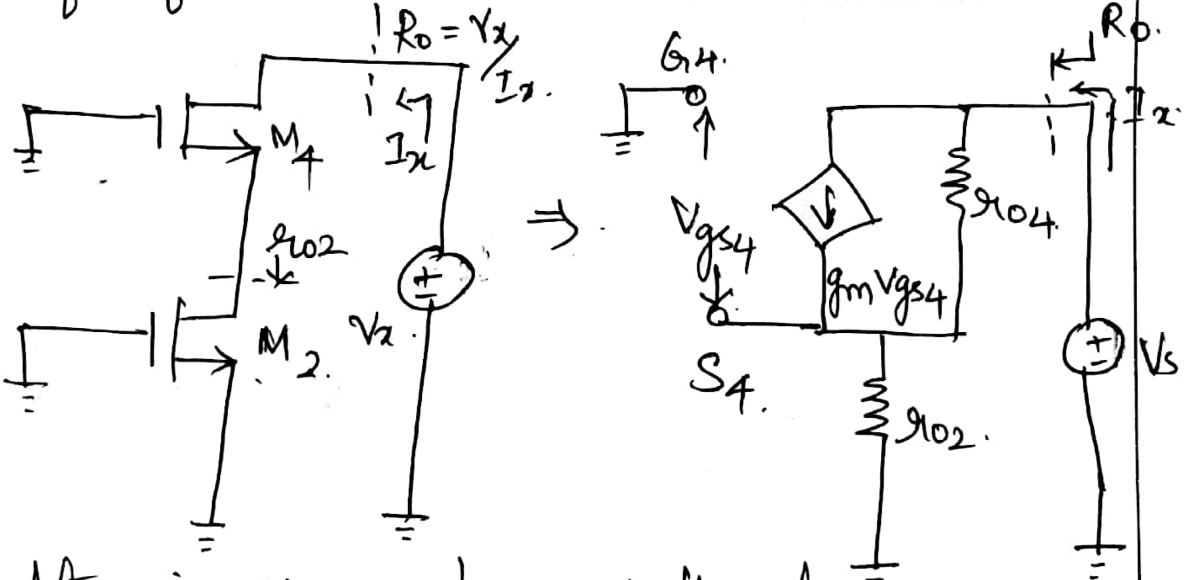
Since the designer has control over W/L of the transistors there is considerable flexibility in the design of MOSFET current sources.

CASCODE Current Mirror



* O/P resistance is a measure of stability with respect to changes in O/P voltage.
* O/P resistance can be increased by modifying the circuit.

* I_{ref} is established by including another MOSFET in the reference branch.
* $I_0 = I_{ref}$ if all transistors are identical.



To determine O/P resistance at the drain of M_4.

Since I_{ref} is constant, the gate voltage to M_1 & M_3 & M_2 & M_4 are constant.

$$I_x = g_m V_{gs4} + \frac{(V_x + V_{gs4})}{r_{o4}}$$

$$V_{gs4} = -I_x r_{o2}$$

$$\therefore I_x = -g_m I_x r_{o2} + \frac{V_x}{r_{o4}} - \frac{I_x r_{o2}}{r_{o4}}$$

$$I_x\left[1 + g_m r_{o2} + \frac{r_{o2}}{r_{o4}}\right] = \frac{V_x}{r_{o4}}$$

$$\frac{V_x}{I_x} = R_o = r_{o4} + \cancel{r_{o4}}\left(\frac{g_m r_{o2} r_{o4} + r_{o2}}{\cancel{r_{o4}}}\right)$$

$$R_o = r_{o4} + r_{o2}(1 + g_m r_{o4})$$

$$g_m r_{o4} >> 1$$

$$\therefore \boxed{R_o = r_{o4} + r_{o2} r_{o4} g_m}$$

R_o is Much larger than 2-transistor current source.

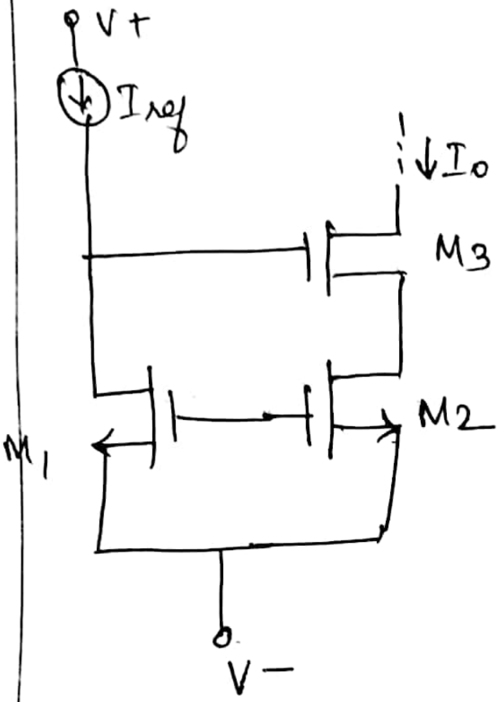
<u>Wilson Current Source</u>:

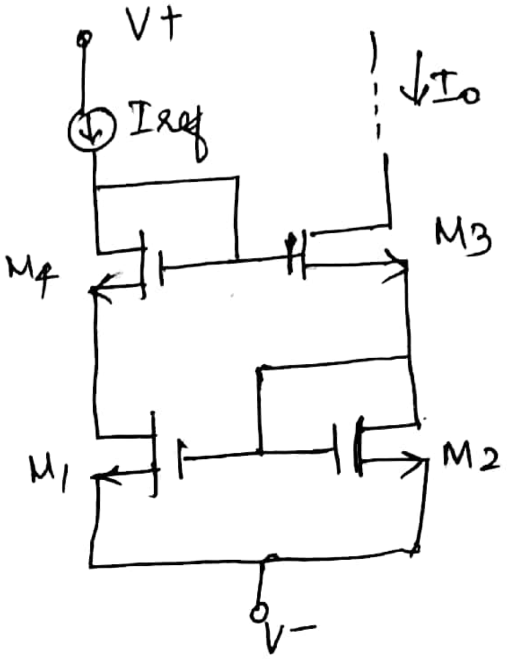
The primary advantage of these circuits is that it increases the o/p resistance which stabilizes the load current.

The

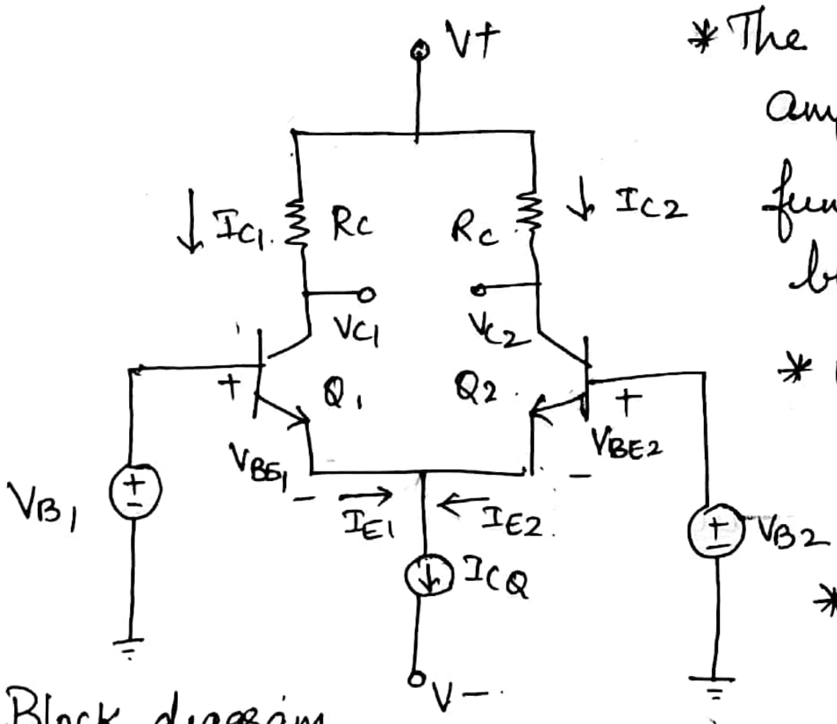
Modified Circuit

MOSFET Wilson Current Source





THE DIFFERENTIAL AMPLIFIER



* The differential amplifier is the fundamental building block of analog circuits.
* i/p stage in every op-amp.
* basis of ECL.

Block diagram

SRM

The difference amplifier amplifies the difference b/w 2 i/p signals.

$$V_o = A_d (V_1 - V_2).$$

If $V_1 = V_2$ o/p voltage $= 0$

If $V_1 \neq V_2$ o/p voltage $\neq 0$.

Differential mode i/p voltage

$$V_d = V_1 - V_2$$

Common mode i/p voltage

$$V_{cm} = \frac{V_1 + V_2}{2}.$$

The o/p voltage due to both differential & common mode i/p is

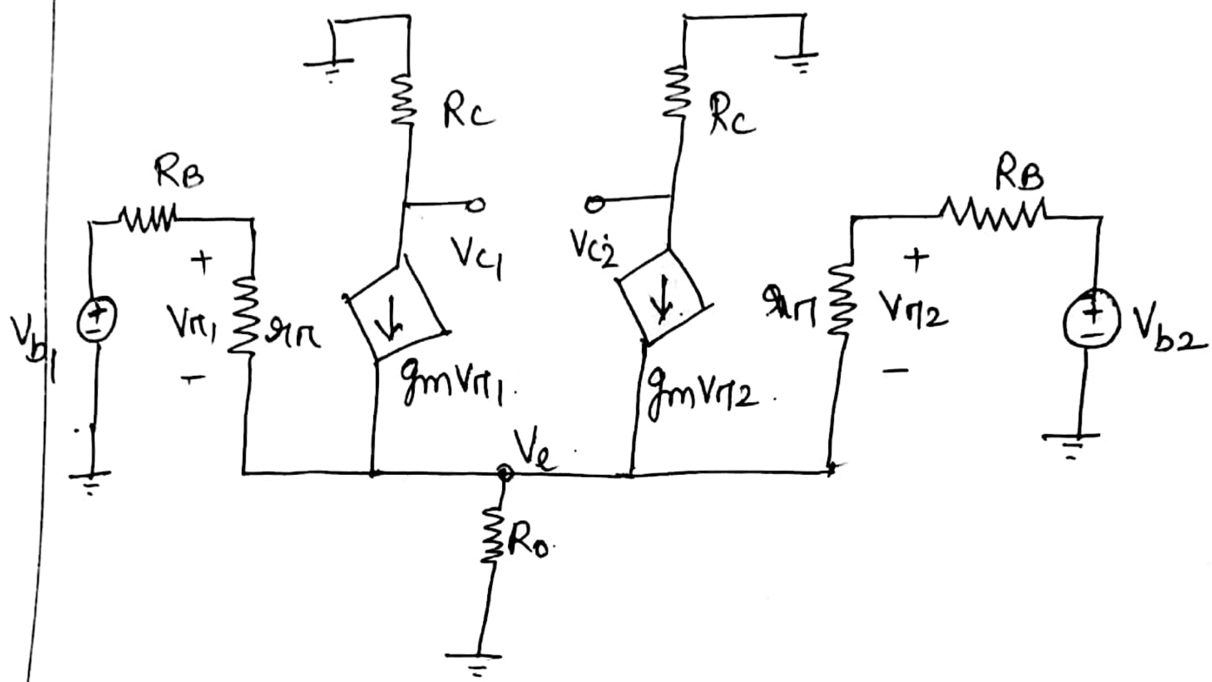
$$V_o = \underbrace{A_d}_{\text{differential mode gain}} V_d + \underbrace{A_{cm}}_{\text{common mode gain}} V_{cm}$$

CMRR Common Mode rejection ratio

The ability of a diff-amp to reject common mode signal

$$CMRR = \left| \frac{A_d}{A_{cm}} \right|. \quad \text{in dB} \quad 20 \log \left| \frac{A_d}{A_{cm}} \right|$$

Small signal Equivalent Circuit Analysis



* Assume Early effect is infinite.
* Constant Current source can be represented by a finite o/p impedance Ro. & RB is also not neglected.

Since the 2 transistors are biased at the same quiescent current we have,

$r_{\pi 1} = r_{\pi 2} = r_\pi$ & $g_{m1} = g_{m2} = g_m$.

Writing a KCL at V_e:-

$$g_m V_{\pi 1} + \frac{V_{\pi 1}}{r_\pi} + g_m V_{\pi 2} + \frac{V_{\pi 2}}{r_\pi} = \frac{V_e}{R_o}.$$

Now $V_{\pi 1}\left(\frac{g_m r_\pi + 1}{r_\pi}\right) + V_{\pi 2}\left(\frac{g_m r_\pi + 1}{r_\pi}\right) = \frac{V_e}{R_o}$

SRM

$$\boxed{V_e = \frac{V_{b1} + V_{b2}}{2 + \frac{r_\pi + R_B}{R_o(1+\beta)}}} \rightarrow (5)$$

If we consider one sided o/p at the collector of Q_2 Then

$$V_o = V_{c2} = -g_m v_{\pi 2} R_C \longrightarrow (6)$$

Sub the eqn for $v_{\pi 2}$ from (3) into (6);

$$V_o = V_{c2} = -g_m r_\pi \left(\frac{V_{b2} - V_e}{r_\pi + R_B}\right) R_C$$

$$V_o = \frac{-\beta R_C}{r_\pi + R_B}(V_{b2} - V_e). \longrightarrow (7)$$

Sub the eqn for V_e from (5) in (7)

$$V_o = -\frac{\beta R_C}{r_\pi + R_B}\left[V_{b2} - \left(\frac{V_{b1} + V_{b2}}{2 + \frac{r_\pi + R_B}{R_o(1+\beta)}}\right)\right]$$

$$= \frac{-\beta R_C}{r_\pi + R_B}\left[\frac{V_{b2}\left(2 + \frac{r_\pi + R_B}{R_o(1+\beta)}\right) - V_{b1} - V_{b2}}{2 + \frac{r_\pi + R_B}{R_o(1+\beta)}}\right]$$

$$= \frac{-\beta R_C}{r_\pi + R_B}\left[\frac{2V_{b2} + V_{b2}\left(\frac{r_\pi + R_B}{R_o(1+\beta)}\right) - V_{b1} - V_{b2}}{2 + \frac{r_\pi + R_B}{R_o(1+\beta)}}\right]$$

$$V_{\pi 1}\left(\frac{1+\beta}{r_\pi}\right) + V_{\pi 2}\left(\frac{1+\beta}{r_\pi}\right) = \frac{V_e}{R_o} \rightarrow (1)$$

$$V_{\pi 1} = \left[\frac{V_{b1} - V_e}{r_\pi + R_B}\right] r_\pi \rightarrow (2)$$

$$V_{\pi 2} = \frac{(V_{b2} - V_e) r_\pi}{r_\pi + R_B} \rightarrow (3)$$

Sub (2) & (3) in (1)

$$\left(\frac{V_{b1} - V_e}{r_\pi + R_B}\right) \cancel{r_\pi} \left(\frac{1+\beta}{\cancel{r_\pi}}\right) + \frac{(V_{b2} - V_e)}{r_\pi + R_B} \cancel{r_\pi} \left(\frac{1+\beta}{\cancel{r_\pi}}\right) = \frac{V_e}{R_o}$$

$$\frac{(V_{b1} - V_e)(1+\beta) + (V_{b2} - V_e)(1+\beta)}{r_\pi + R_B} = \frac{V_e}{R_o}$$

$$(V_{b1} + V_{b2} - 2V_e)\frac{(1+\beta)}{r_\pi + R_B} = \frac{V_e}{R_o} \rightarrow (4)$$

Solving for Ve

$$V_{b1} + V_{b2} - 2V_e = \frac{V_e(r_\pi + R_B)}{R_o(1+\beta)}$$

$$V_{b1} + V_{b2} = \frac{V_e(r_\pi + R_B)}{R_o(1+\beta)} + 2V_e$$

$$V_{b1} + V_{b2} = V_e\left[2 + \frac{r_\pi + R_B}{R_o(1+\beta)}\right]$$

SRM

$$V_0 = \frac{-\beta R_C}{r_\pi + R_B}\left\{\frac{V_{b2}\left(1+\frac{r_\pi+R_B}{R_O(1+\beta)}\right) - V_{b1}}{2+\frac{r_\pi+R_B}{R_O(1+\beta)}}\right\} \rightarrow (8)$$

In an ideal current source $R_O = \infty$ [in (8)]

$$\therefore V_0 = \frac{-\beta R_C}{r_\pi + R_B}\left[\frac{V_{b2}(1+0) - V_{b1}}{2+0}\right)$$

$$V_0 = \frac{-\beta R_C (V_{b2} - V_{b1})}{2(r_\pi + R_B)} \rightarrow (9)$$

$$\therefore V_{b2} - V_{b1} = -V_d \text{ (or) } \boxed{V_d = V_{b1} - V_{b2}} \rightarrow (10)$$

Sub (10) in (9)

$$V_0 = \frac{\beta R_C V_d}{2(r_\pi + R_B)}$$

$$\frac{V_0}{V_d} = \frac{\beta R_C}{2(r_\pi + R_B)} = A_d. \rightarrow (11)$$

We. k.t $V_{cm} = \frac{V_{b1} + V_{b2}}{2}$ & $V_d = V_{b1} - V_{b2}$.

In terms of V_d

$$\therefore V_{b1} = V_{cm} + \frac{V_d}{2}. \text{ and } \rightarrow (12)$$

$$V_{b2} = V_{cm} - \frac{V_d}{2} \rightarrow (13)$$

The two i/p signals can be written as the sum of differential mode i/p signal component & a common mode i/p signal component.

Sub (12) & (13) into (8)

$$V_0 = \frac{-\beta R_C}{r_\pi + R_B} \left[\frac{V_{cm} - \frac{V_d}{2}\left(1 + \frac{r_\pi + R_B}{R_O(1+\beta)}\right) - \left(V_{cm} + \frac{V_d}{2}\right)}{2 + \frac{r_\pi + R_B}{(1+\beta)R_O}} \right] \longrightarrow (14)$$

Solving for Vd only:

$$\Rightarrow \frac{\frac{\beta R_C V_d}{2(r_\pi + R_B)}\left(1 + \frac{r_\pi + R_B}{R_O(1+\beta)}\right) + \frac{V_d}{2(r_\pi + R_B)}\beta R_C}{2 + \frac{r_\pi + R_B}{R_O(1+\beta)}}$$

$$\Rightarrow \frac{V_d \beta R_C}{2(r_\pi + R_B)} \left[\frac{1 + \frac{r_\pi + R_B}{R_O(1+\beta)} + 1}{2 + \frac{r_\pi + R_B}{R_O(1+\beta)}} \right]$$

$$\Rightarrow V_d \frac{\beta R_C}{2(r_\pi + R_B)} \left[\cancel{\frac{2 + \frac{r_\pi + R_B}{R_O(1+\beta)}}{2 + \frac{r_\pi + R_B}{R_O(1+\beta)}}} \right]$$

SRM

$$\Rightarrow V_d \frac{\beta R_C}{2(r_\pi + R_B)} \longrightarrow (15)$$

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For Vcm

$$\Rightarrow V_{cm}\left[\frac{-\beta R_C}{r_\pi+R_B}\left(\frac{\cancel{1}+\frac{r_\pi+R_B}{R_o(1+\beta)}\cancel{-1}}{2+\frac{r_\pi+R_B}{(1+\beta)R_o}}\right)\right]$$

$$\Rightarrow \frac{-V_{cm}\beta R_C}{r_\pi+R_B}\left[\frac{\frac{r_\pi+R_B}{R_o\cancel{(1+\beta)}}}{\frac{2(1+\beta)R_o+r_\pi+R_B}{\cancel{(1+\beta)}R_o}}\right]$$

$$\Rightarrow \frac{-\beta R_C V_{cm}}{r_\pi+R_B}\left[\frac{r_\pi+R_B}{2(1+\beta)R_o+r_\pi+R_B}\right]$$

~~neglect~~ gm.

$$\Rightarrow \frac{-\beta R_C V_{cm}}{r_\pi}\left[\frac{1}{1+\frac{2R_o(1+\beta)}{r_\pi+R_B}}\right]$$

$$\Rightarrow \frac{-g_m R_C V_{cm}}{1+\frac{2R_o(1+\beta)}{r_\pi+R_B}} \longrightarrow (16)$$

Combining (15) & (16)

$$V_o=\frac{\beta R_C}{2(r_\pi+R_B)}V_d-\frac{g_m R_C}{1+\frac{2R_o(1+\beta)}{r_\pi+R_B}}V_{cm}.$$

$$= A_d V_d + A_{cm} V_{cm}$$

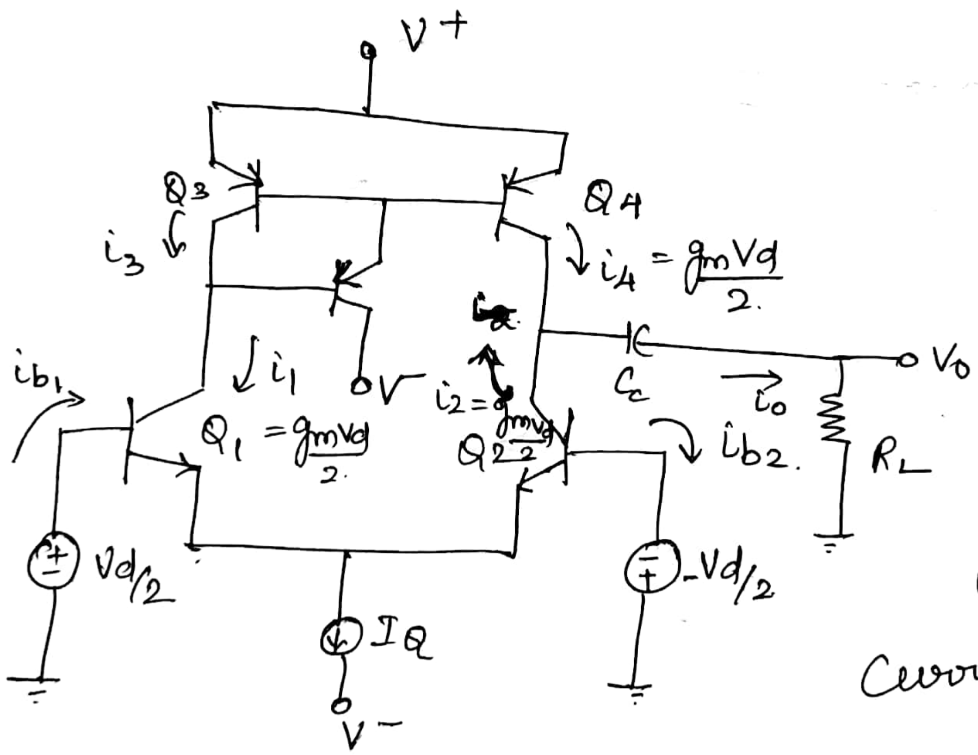
$$Ad = \frac{\beta R_C}{2(r_\pi + R_B)} \quad \& \quad A_{cm} = -\frac{g_m R_C}{1 + \frac{2(1+\beta)R_O}{r_\pi + R_B}}$$

If $R_O = \infty$

then $A_{cm} = 0$

Small signal analysis of BJT Active load.

* R_L represents the small signal i/p resistance of the gain stage.
* Differential mode i/p is applied.



$i_3 = i_1$

$i_1 = \frac{g_m V_d}{2}$

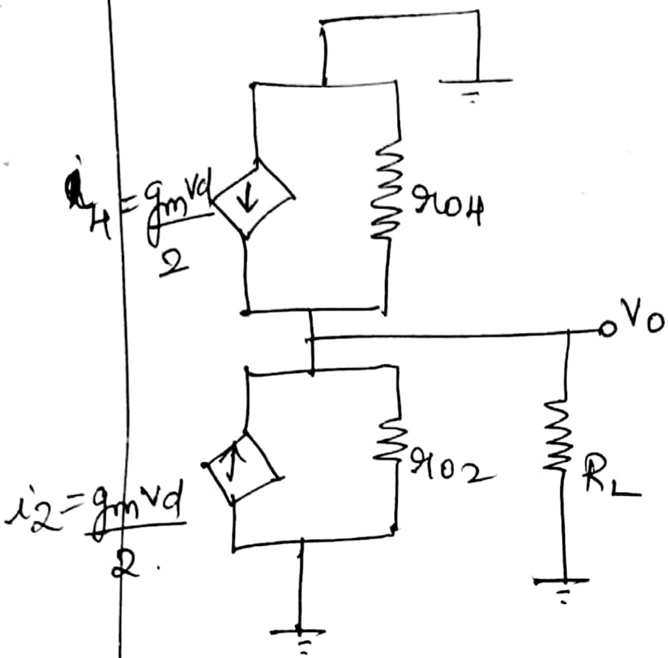
$i_2 = \frac{g_m V_d}{2}$

$i_4 = i_3$

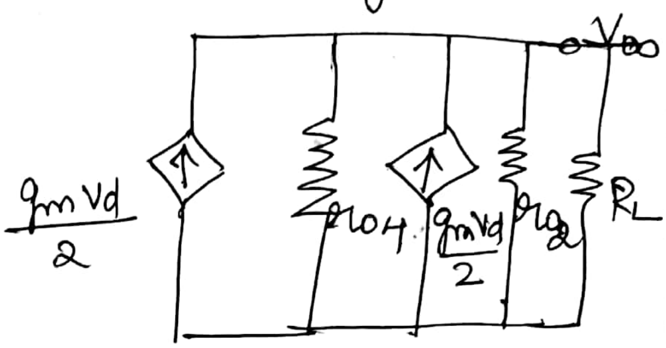
Current mirror

$i_2 + i_4 = i_L$

Small signal Equivalent circuit



rearranged circuit



$$V_o = \left(\frac{g_m v_d}{2} + \frac{g_m v_d}{2}\right)(r_{o4} \| r_{o2} \| R_L)$$

$$= \cancel{2}\left(\frac{g_m v_d}{\cancel{2}}\right)(r_{o4} \| r_{o2} \| R_L)$$

$$\boxed{A_d = \frac{V_o}{V_d} = g_m(r_{o4} \| r_{o2} \| R_L)}$$

or $A_d = \dfrac{g_m}{\frac{1}{r_{o4}} + \frac{1}{r_{o2}} + \frac{1}{R_L}} = \dfrac{g_m}{g_{o2} + g_{o4} + G_L}$

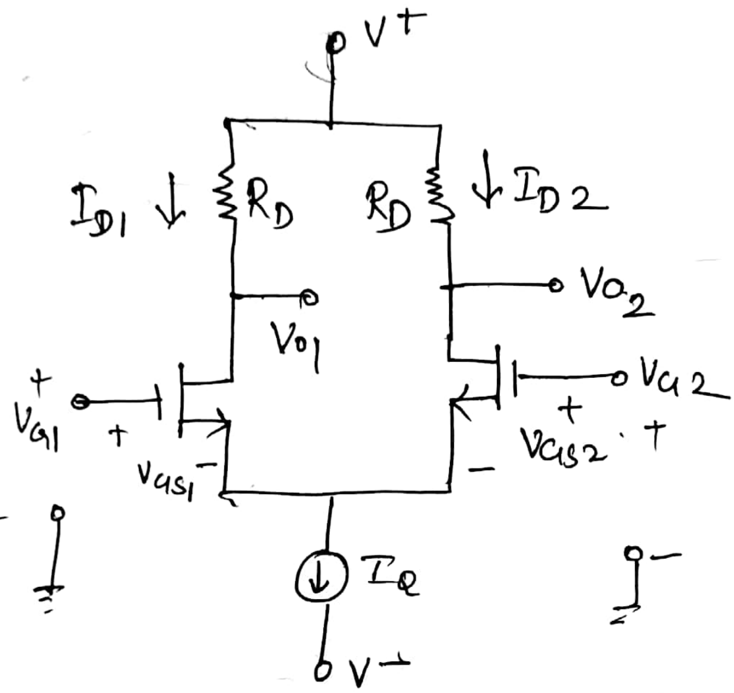
w.r.t $g_m = \dfrac{I_Q}{2V_T}$, $r_{o2} = \dfrac{V_{A2}}{I_2}$ and $r_{o4} = \dfrac{V_{A4}}{I_4}$

$I_2 = I_4 = I_Q/2$

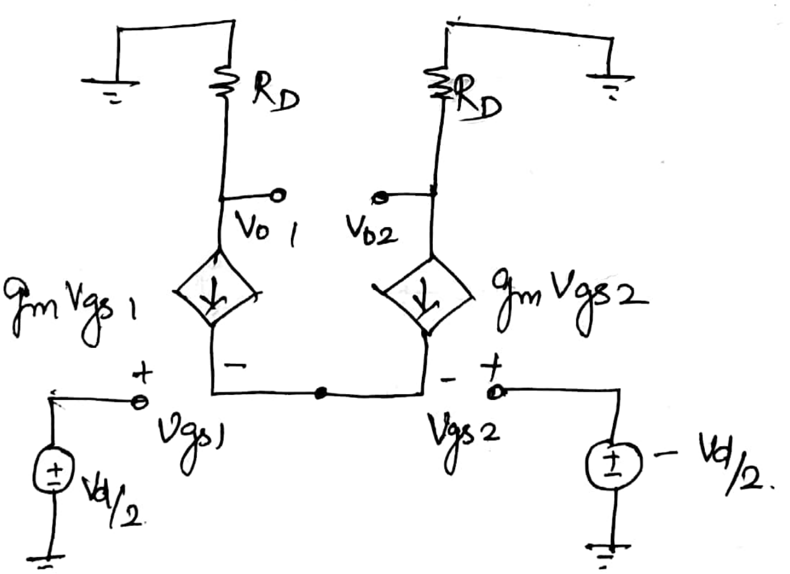
$$A_d = \frac{I_Q/2V_T}{\frac{I_Q}{2V_{A2}} + \frac{I_Q}{2V_{A4}} + \frac{1}{R_L}}$$

This is similar to that of a single amplifier with an active load.

Basic FET Differential pair



Small signal Analysis of FET diff-amp



Applying KCL to the common source node:

$g_m V_{gs1} + g_m V_{gs2} = 0$.

$\cancel{g_m} V_{gs1} = -\cancel{g_m} V_{gs2} \Rightarrow V_{gs1} = -V_{gs2} \rightarrow (1)$

The differential mode i/p voltage is

$V_d = V_1 - V_2 = V_{gs1} - V_{gs2} \rightarrow (2)$

(1) in (2)

$\therefore V_d = -V_{gs2} - V_{gs2} = -2V_{gs2}$.

A one sided O/P at V_{o2} is given by

$V_{o2} = -g_m V_{gs2} R_D = -g_m\left(\frac{-V_d}{2}\right) R_D$

$A_d = \frac{V_{o2}}{V_d} = +\frac{g_m R_D}{2}$

$\boxed{A_d = \frac{g_m R_D}{2}}$

If constant current source & O/P resistance is finite, then the JFET amplifier will have a non zero common mode gain.

MOSFET Differential Amplifier with Active load :-

M_1 & M_2 are n-channel devices and form differential pair biased with I_Q. The load circuit consists of M_3 & M_4, both p-channel devices.

$$i_{D1} = i_{D2} = \frac{I_Q}{2}$$

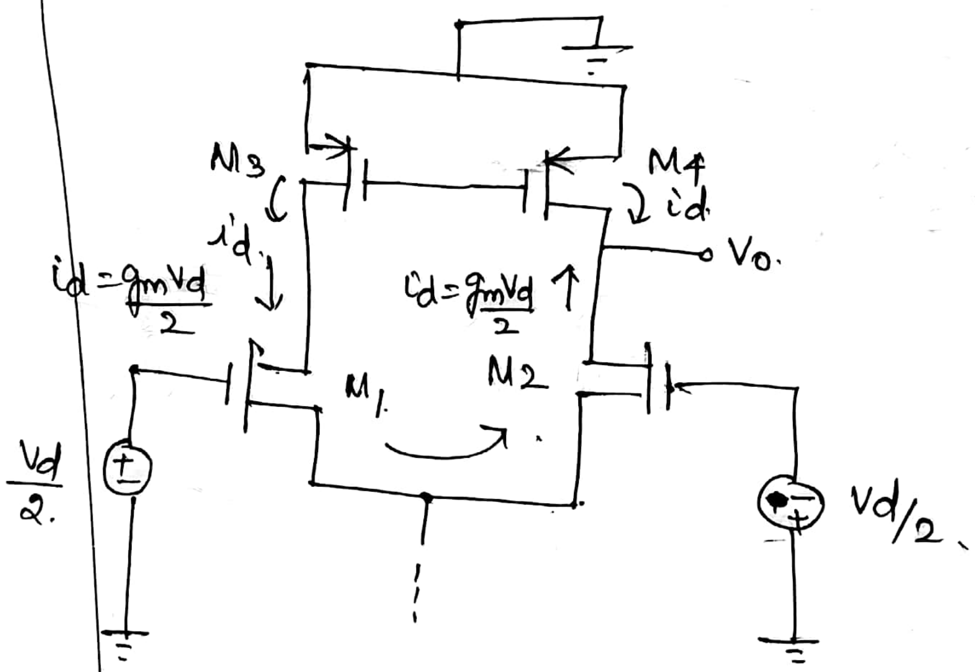
There are no gate currents therefore

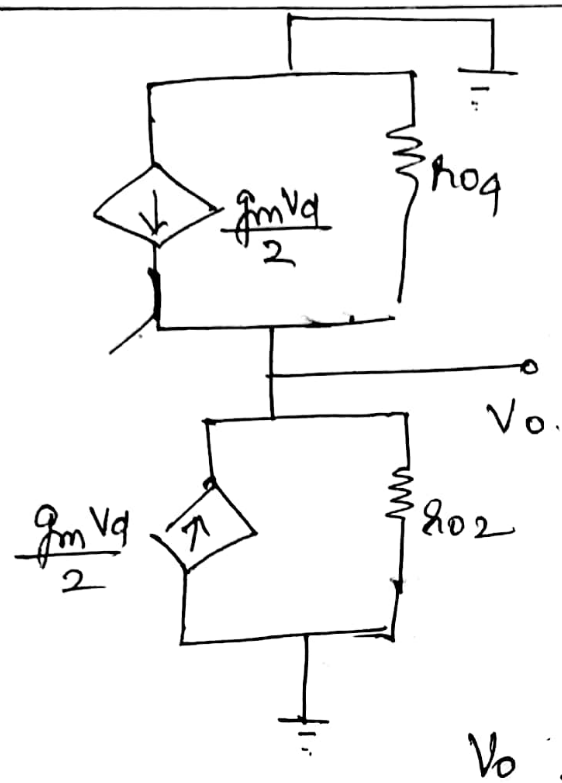
$i_{D3} = i_{D1}$ & $i_{D4} = i_{D2}$.

If $v_d = v_1 - v_2$ is applied, then ~~from~~

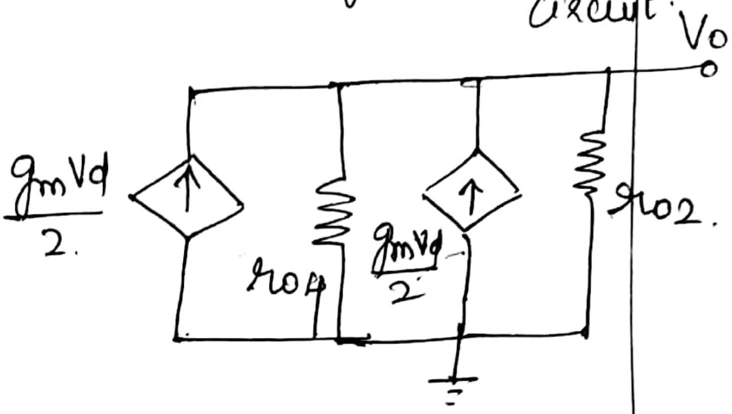
$$i_{D1} = \frac{I_Q}{2} + i_d \quad \& \quad i_{D2} = \frac{I_Q}{2} - i_d.$$

$$i_{D1} = i_{D3} = \frac{I_Q}{2} + i_d \quad \& \quad i_{D4} = i_{D3} = \frac{I_Q}{2} + i_d.$$





The small signal equivalent circuit:



$$V_o = 2\left(\frac{g_m V_d}{2}\right)(r_{o2} \| r_{o4})$$

$$\frac{V_o}{V_d} = A_d = g_m (r_{o2} \| r_{o4}).$$

$$A_d = \frac{g_m}{\frac{1}{r_{o2}} + \frac{1}{r_{o4}}} = \frac{g_m}{g_{o2} + g_{o4}}.$$

$$g_m = 2\sqrt{K_n I_D} = \sqrt{2 k_n I_Q}$$

$$g_{o2} = \lambda_2 I_{DQ2} = (\lambda_2 I_Q / 2) \quad \&$$

$$g_{o4} = \lambda_4 I_{DQ4} = (\lambda_4 I_Q / 2) \quad \text{then}$$

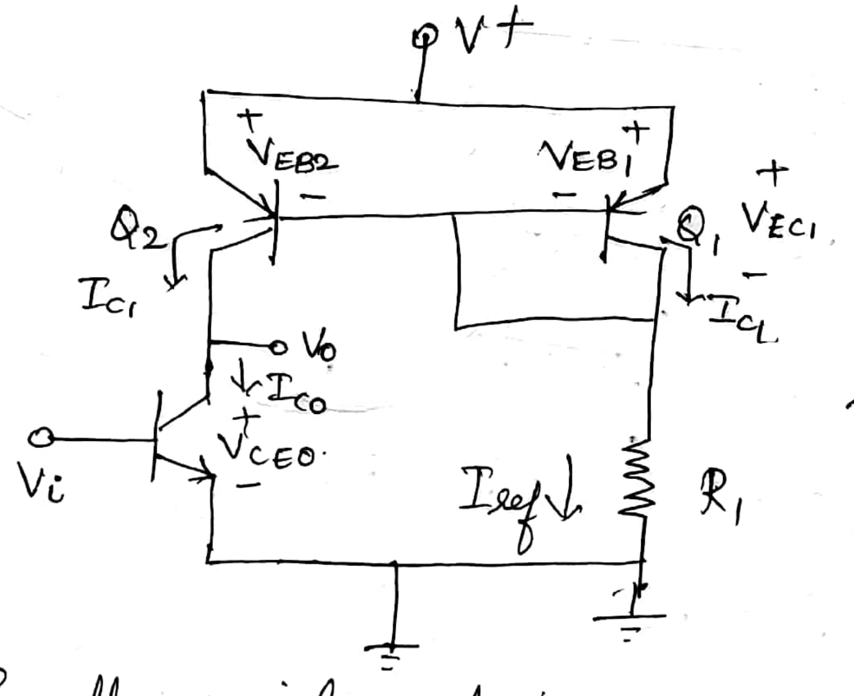
$$A_d = \frac{2\sqrt{2 k_n I_Q}}{I_Q(\lambda_2 + \lambda_4)} = 2\sqrt{\frac{2k_n}{I_Q}} \cdot \frac{1}{\lambda_2 + \lambda_4}.$$

Circuits with active load:-

The In bipolar amplifiers, Small signal voltage gain is directly proportional to the collector resistor R_C. To increase the gain, we need to increase R_C value, and hence V_{CC} has to be increased. In practice, there is a limited range of values of R_C & V_{CC} that are ~~seen~~ reasonable.

* We use a load device that is a transistor.
* Active loads produce much larger small signal gain than discrete resistors.

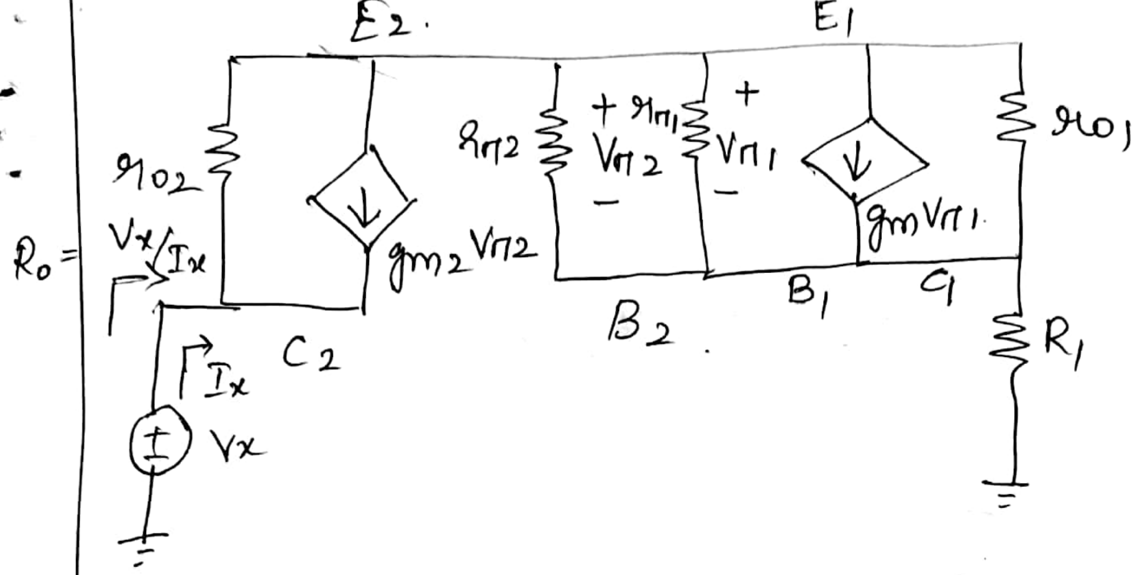
DC Analysis : BJT Active Load



The elements R_1, Q_1 and Q_2 form the active load & Q_2 is refered as the active load device for Q_0.

Small signal analysis

We must determine the resistor looking into the collector of the active load.



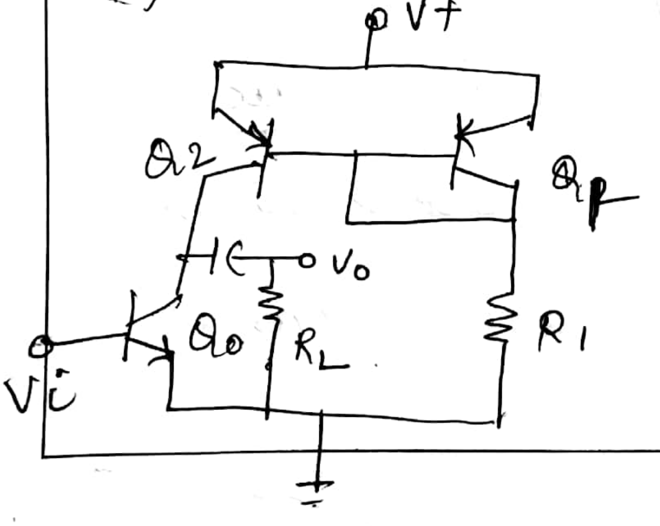
In the Q_1 portion of equivalent circuit, there are no independent ac sources to excite any currents or voltages. $\therefore V_{\pi 1} = V_{\pi 2} = 0$

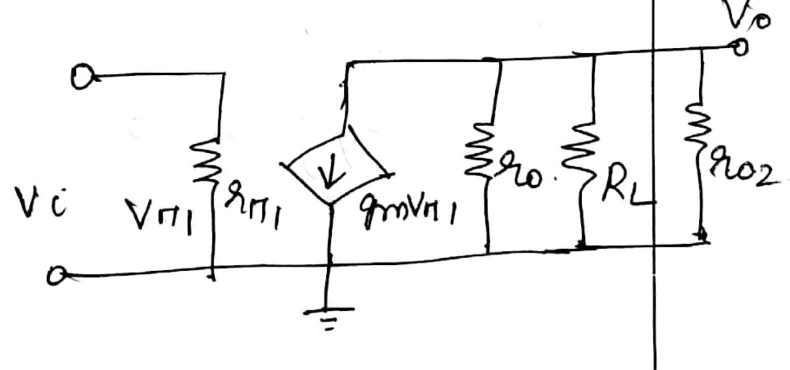
$g_m V_{\pi 2} = 0$

$R_o = r_{o2}$ ← resistance looking into the collector of Q_2

We will use this equivalent resistance to calculate the small signal voltage gain of the amplifier.

<u>Simple BJT with active load & load resistance.</u>





The o/p voltage is

$$V_o = -g_m V_{\pi 1}\,(r_o \| R_L \| r_{o2})$$

$$V_{\pi 1} = V_i$$

$$\therefore \frac{V_o}{V_i} = A_V = -g_m\,(r_o \| R_L \| r_{o2})$$

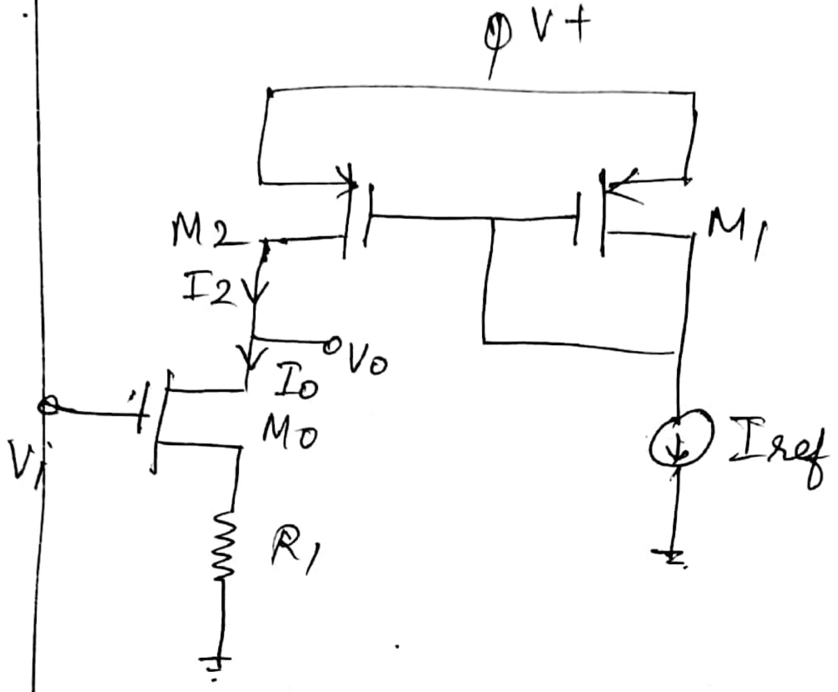
$$A_V = \frac{-g_m}{\frac{1}{r_o} + \frac{1}{R_L} + \frac{1}{r_{o2}}}$$

$$\boxed{A_V = \frac{-g_m}{g_o + g_L + g_{o2}}}$$ or

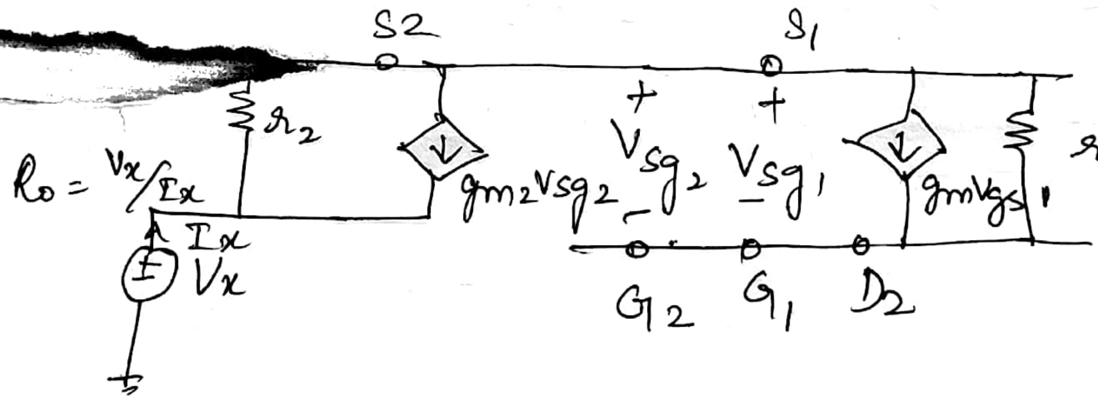
$$A_V = \frac{-\left(\frac{I_{CO}}{V_T}\right)}{\frac{I_{CO}}{V_{AN}} + \frac{1}{R_L} + \frac{I_{CO}}{V_{AP}}}$$

<u>Small Signal Analysis of CS with Active load</u>

M_1 & M_2 form a PMOS active load circuit & M_2 is the active load device.



Small signal equivalent



To find Ro:

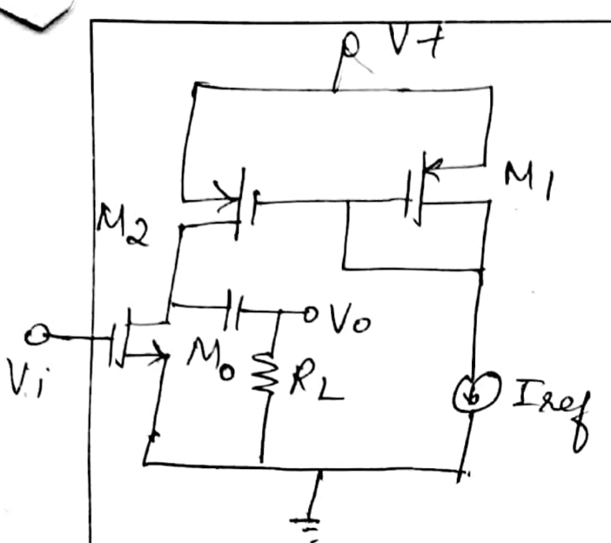
No independant ac source is supplied for M2 $\therefore V_{gs1} = V_{gs2} = 0$

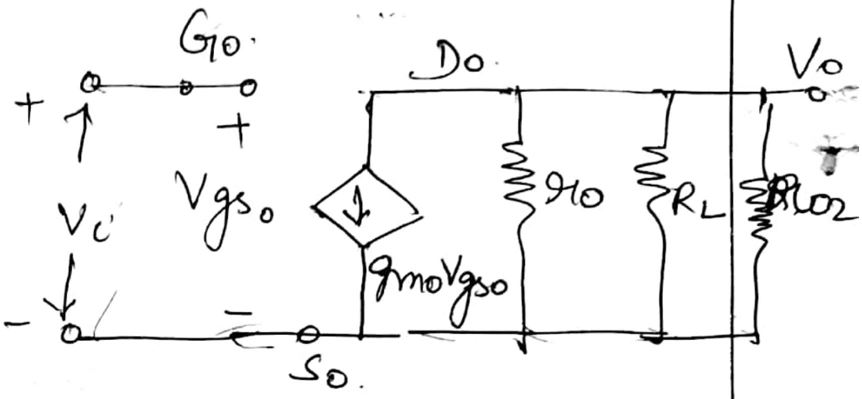
$$g_m V_{gs1} = g_m V_{gs2} = 0$$

$$R_o = r_{o2}$$

A <u>simple MOSFET CS with an active load & R_L</u>

Small signal equivalent ckt.





To find Av:-

$$V_o = -g_{m0}V_{gs0}\,(r_o \| R_L \| r_{o2}) \qquad V_{gs0} = V_i$$

$$\frac{V_o}{V_i} = -g_{m0}(r_o \| R_L \| r_{o2})$$

$$A_V = \frac{-g_m}{\frac{1}{r_o} + \frac{1}{R_L} + \frac{1}{r_{o2}}} = \frac{-g_m}{g_o + g_L + g_{o2}}$$