

Unit - VMos Field Effect Transistor

MOSFET is the common term for Insulated Gate Field Effect Transistor (IGFET). There are two basic forms of MOSFET:

- (i) Enhancement MOSFET
- (ii) Depletion MOSFET.

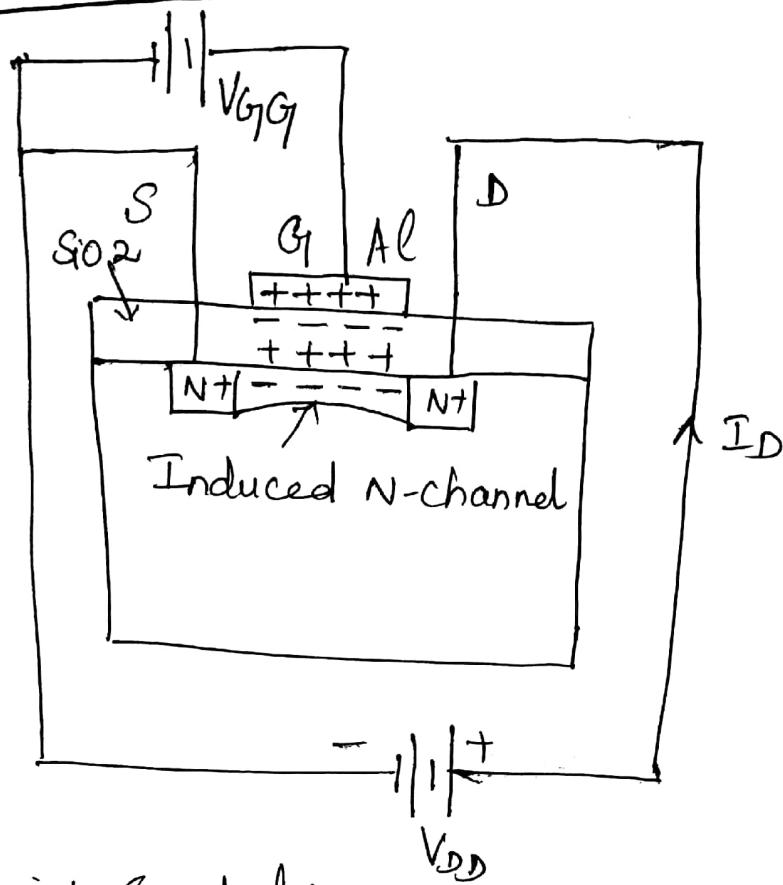
Principle: By applying a transverse electric field across an insulator, deposited on the semiconductor material, the thickness and hence the resistance of a conducting channel of semiconductor material can be controlled.

Depletion MOSFET → controlling field reduces the number of majority carriers available for conduction.

Enhancement MOSFET → application of electric field causes an increase in the majority carrier density in the majority carrier density in the conducting regions of the transistor.

# ENHANCEMENT MOSFET

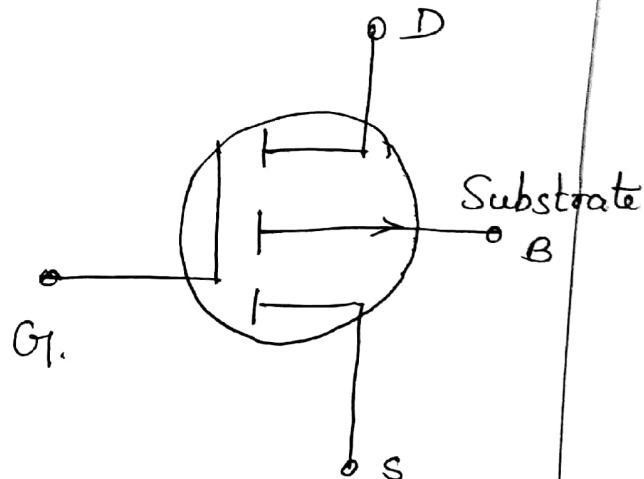
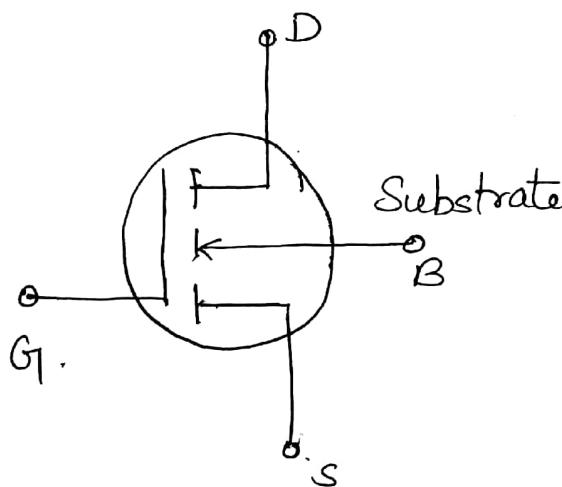
## N-channel enhancement MOSFET



Circuit Symbol:

N-Channel

P-Channel



Construction :-

- \* Two highly doped N+ regions are diffused in a lightly doped substrate of P-type

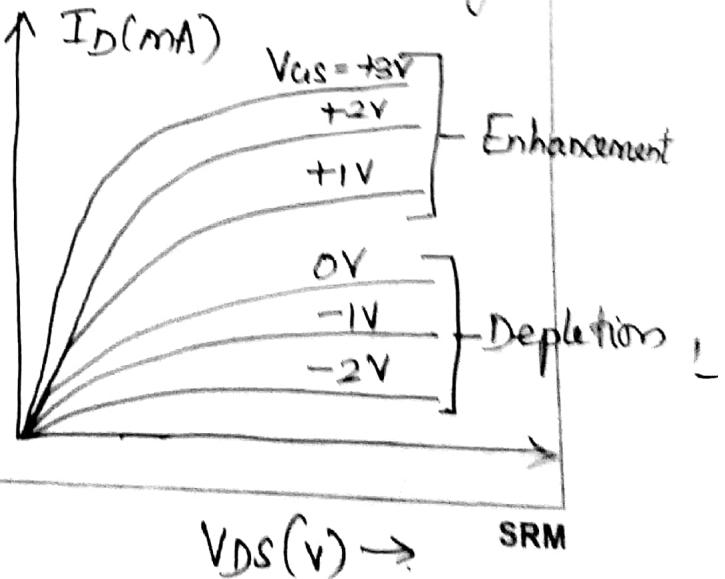
SRM

silicon substrate.

- \* One  $N^+$  region is called source & the other one is called drain (D).
  - \* They are separated by 1 mil ( $10^{-3}$  inch).
  - \* A thin layer of  $SiO_2$  is grown over the surface of the structure & holes are cut into the oxide layer allowing contact with source & drain.
  - \* Then a thin layer of metal aluminium is formed over  $SiO_2$  layer. This covers the entire channel region & it forms the gate.
  - \* The metal area of the gate, in conjunction with the insulating oxide layer of  $SiO_2$  and the semiconductor channel forms a parallel plate capacitor.
  - \* This device is called the insulated gate FET because of insulating layer of  $SiO_2$ .
  - \* This layer gives an extremely high input impedance for the MOSFET.
- Operation:
- \* If the substrate is grounded & a positive voltage is applied at the gate, the positive

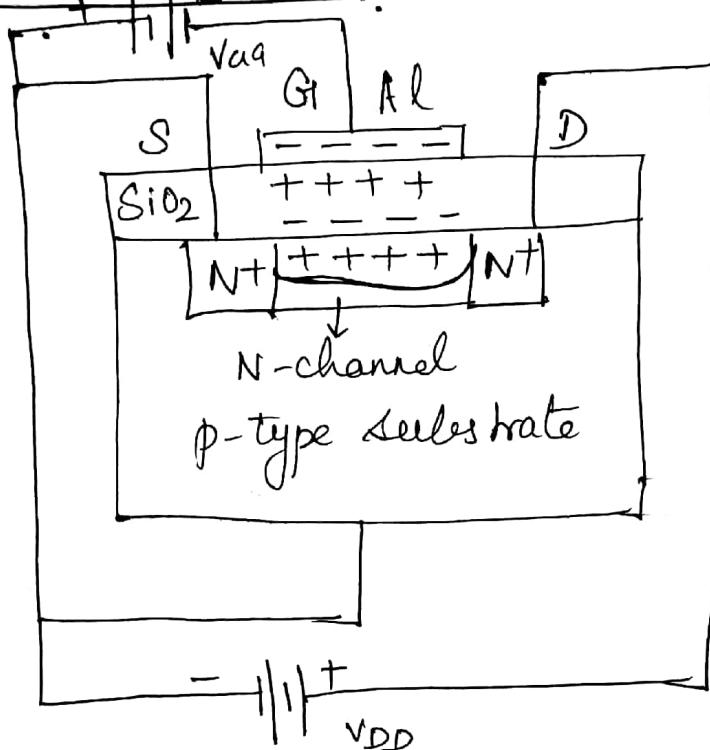
Charge on G induces an equal negative charge on the substrate between the source and drain regions.

- \* Thus an electric field is produced between the source and drain regions.
- \* The direction of electric field is perpendicular to the plates of the capacitor through the oxide.
- \* The negative charge of electrons which are minority carriers in P-type substrate forms an inversion layer.
- \* As the positive voltage on the gate increases, the induced negative charge in the semiconductor increases.
- \* Hence the conductivity increases & current flows from source to drain through the induced channel.
- \* Thus the drain current is enhanced by the positive gate voltage.



③

## Depletion MOSFET

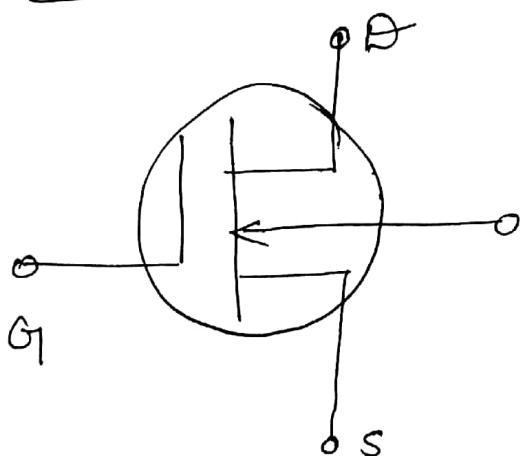


ⓐ N-channel depletion MOSFET

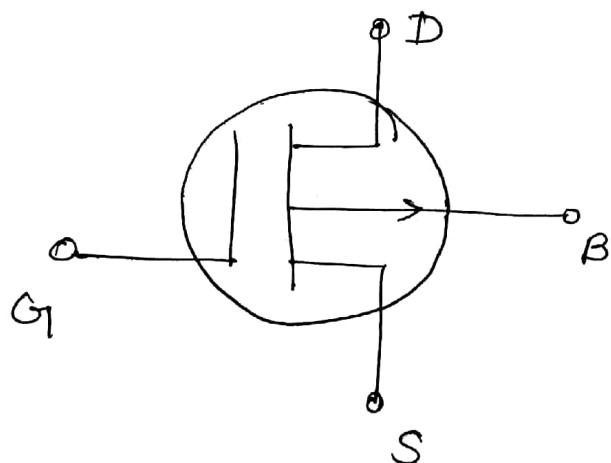
ⓑ

## Circuit Symbol

N-channel



P-channel



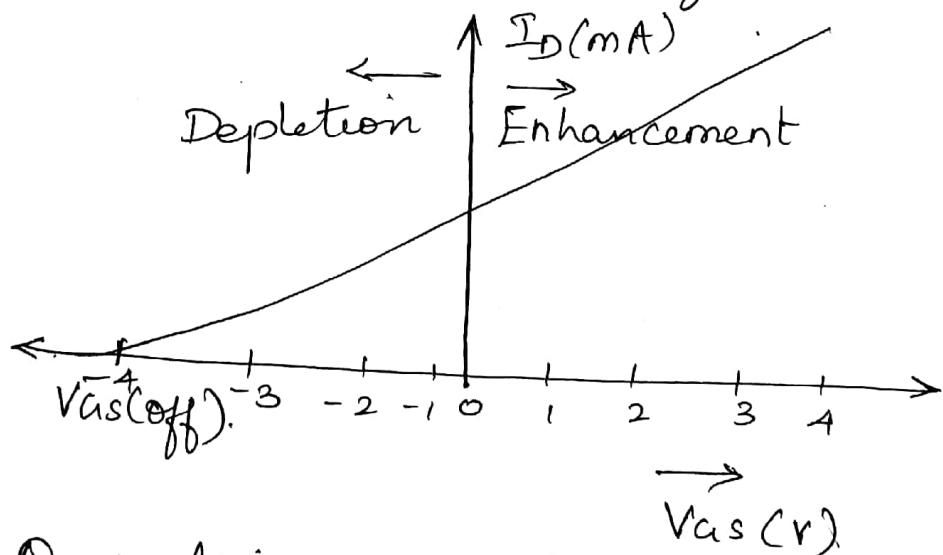
- \* With  $V_{GS}=0$  and the drain D at a positive potential with respect to the source, the electrons flow through the

N-channel from S to D.

- \* Therefore, the conventional current  $I_D$  flows through the channel D to S.
- \* If the gate voltage is made negative, positive charge consisting of holes is induced in the channel through  $\text{SiO}_2$  of the gate channel capacitor.
- \* The introduction of positive charge causes depletion of mobile electrons in the channel. Thus depletion region is produced in the channel.
- \* Shape of depletion region depends on  $V_{GS}$  &  $V_{DS}$ .
- \* Channel  $\rightarrow$  wedge shaped.
- \* When  $V_{DS}$  is increased,  $I_D$  increases & becomes constant for certain value of  $V_{DS}$ , called the pinch off voltage.
- \* Drain current  $I_D$  gets saturated beyond the pinch off voltage.
- \* Since the current in an FET is due to majority carriers, the induced positive charges make the channel less conductive, and  $I_D$  drops as  $V_{DS}$  is made negative.
- \* The depletion MOSFET may also be

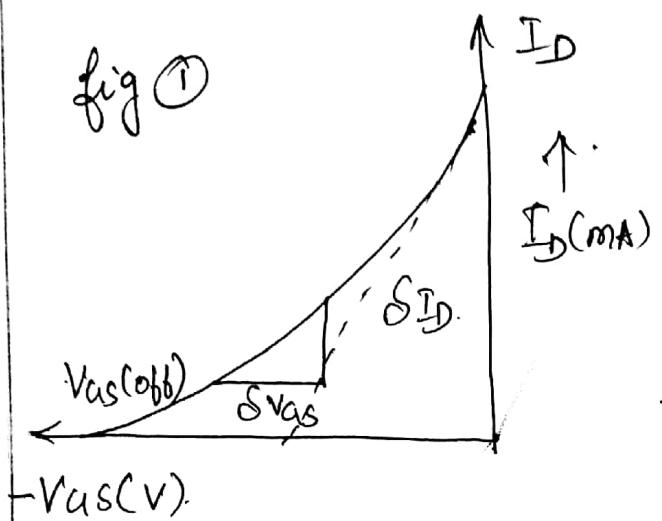
- \* Operated in an enhancement mode.
- \* It is only necessary to apply a positive gate voltage so that negative charges are induced into N-type channel. Hence the conductivity of channel increases and  $I_D$  increases.
- \* As depletion MOSFET can be operated with bipolar input signals irrespective of doping of the channel, it is also called as dual mode MOSFET.

### Transfer Characteristics of MOSFET



Derivation for Saturation Drain Current & transconductance :-

fig ①



Characteristics is represented by a parabola.

$$I_{DS} = I_{DSS} \left(1 - \frac{V_{ds}}{V_p}\right)^2 \quad ①$$

$I_{DS}$   $\rightarrow$  saturation drain current

$I_{DSS}$  is  $I_D$  when  $V_{ds}=0$  &  $V_p$  is the pinch off voltage.

Differentiating ① w.r.t.  $V_{ds}$

$$\frac{\partial I_{DS}}{\partial V_{ds}} = I_{DSS} \times 2 \left(1 - \frac{V_{ds}}{V_p}\right) \left(-\frac{1}{V_p}\right)$$

$$g_m = \frac{\partial I_{DS}}{\partial V_{ds}} \rightarrow V_{ds} \text{ constant}$$

$$g_m = -2 \frac{I_{DSS}}{V_p} \left(1 - \frac{V_{ds}}{V_p}\right) \rightarrow ②$$

From ①

$$1 - \frac{V_{ds}}{V_p} = \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

Substituting in eqn ②

$$g_m = -2 \frac{\sqrt{I_{DSS}}}{V_p} \left(\sqrt{\frac{I_{DS}}{I_{DSS}}}\right)$$

(5)

$$g_m = -\frac{2 \sqrt{I_{DS} I_{DSS}}}{V_p} \rightarrow ③$$

Suppose  $g_m = g_{m0}$ ,  $V_{GS} = 0$  then  $I_{DS} = I_{DSS}$ .

$$g_{m0} = -\frac{2 I_{DSS}}{V_p}$$

From eqn ②

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_p}\right)$$

### Slope of Transfer Characteristics

from ③

$$g_m = -\frac{2 \sqrt{I_{DS} I_{DSS}}}{V_p}$$

$$\text{or } \frac{\partial I_D}{\partial V_{GS}} = -\frac{2 \sqrt{I_D I_{DSS}}}{V_p}$$

Substituting  $I_{DS} = I_{DSS}$

$$\frac{\partial I_D}{\partial V_{GS}} = -\frac{2 I_{DSS}}{V_p} = \frac{I_{DSS}}{(-V_{p/2})}$$

This equation shows that the tangent to the curve at  $I_{DS} = I_{DSS}$ ,  $V_{GS} = 0$  will

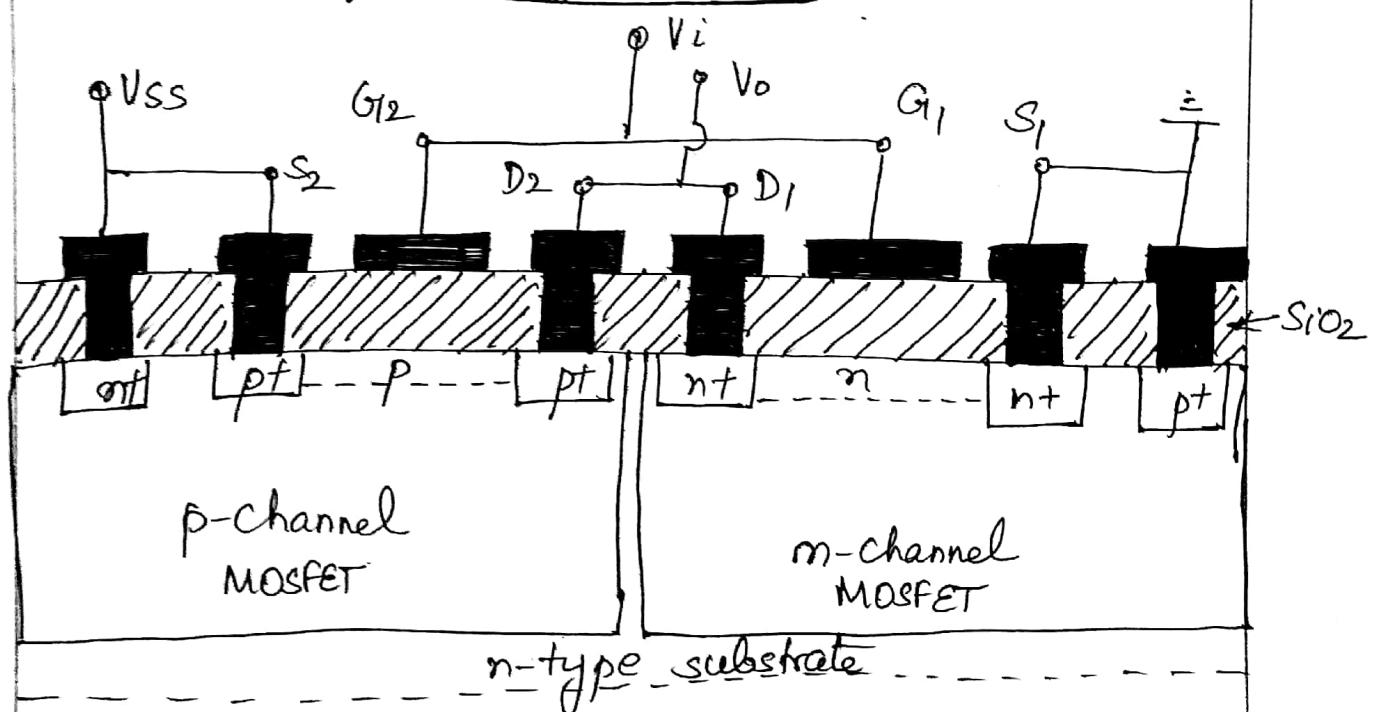
intercept at  $-V_{p/2}$  on the axis of  $V_{AS}$  as shown in fig. ①. Therefore the value of  $V_p$  can be found by drawing the tangent at  $I_{DS} = I_{DSS}$ ,  $V_{AS} = 0$

The  $V_{AS(off)}$  on transfer characteristics is equal to  $V_p$  on the drain characteristics

$$(ii) V_p = [V_{AS(off)}].$$

$$\therefore I_D = I_{DSS} \left(1 - \frac{V_{AS}}{V_{AS(off)}}\right)^2.$$

### CMOS : Complementary MOSFET



- \* A very effective logic circuit can be established by connecting p & n-channel

MOSFET on the same substrate.

\* referred to as CMOS  $\rightarrow$  complementary MOSFET.

\* Applications  $\rightarrow$  computer logic design.  
Advantages

- $\hookrightarrow$  high input impedance
- $\hookrightarrow$  fast switching speeds
- $\hookrightarrow$  lower operating power levels.

### CMOS Inverter :-

$\rightarrow$  logic element that inverts the applied signal.

I/P	O/P
0V	5V
5V	0V

~~when~~ Both gates are connected to  $V_o$ .

\* Source of p-channel MOSFET connected to  $V_{ss}$ .

\* Source of n-channel MOSFET connected to ground.

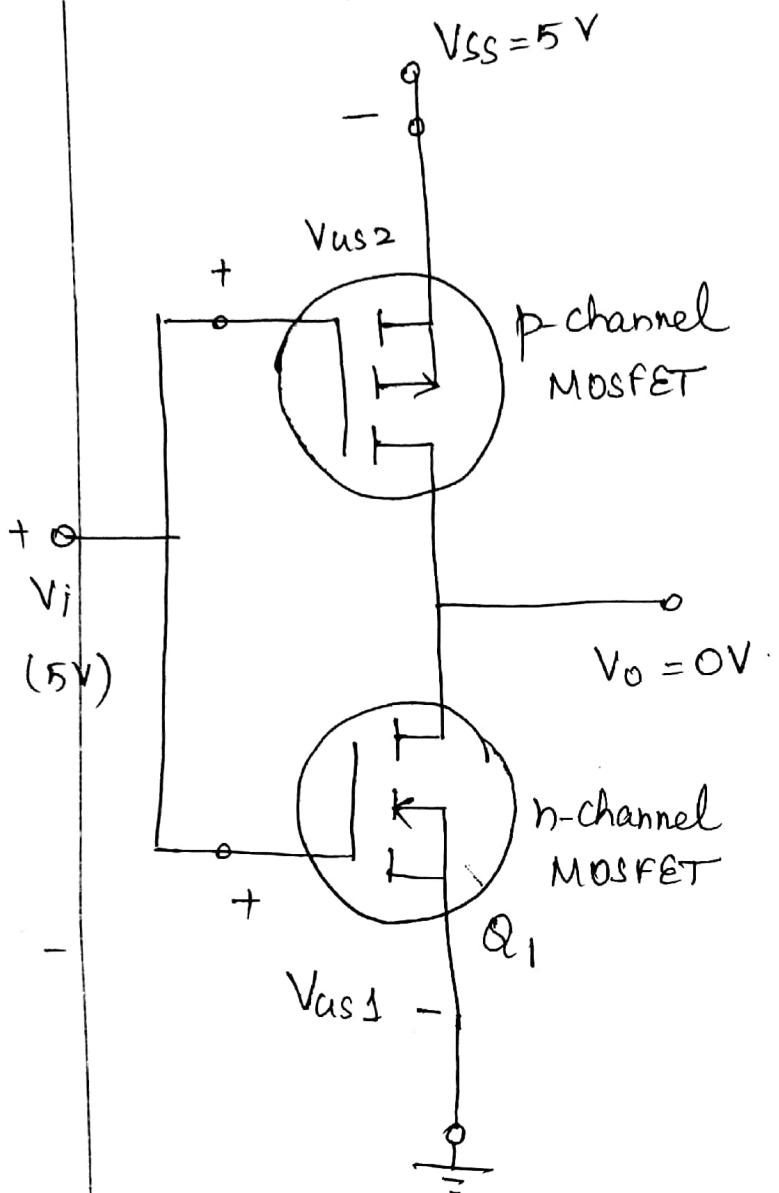
\* With  $V_i = 0V$ ,

$Q_1$  is ON &  $Q_2$  is OFF.  $\therefore V_o = 0$

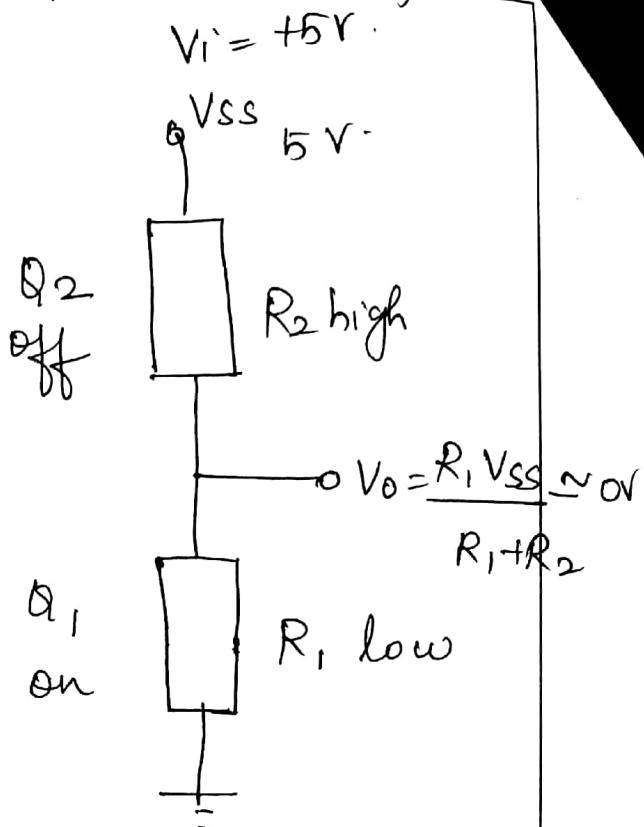
With  $V_i = 5V$

$Q_1$  is OFF &  $Q_2$  is ON  $\therefore V_o = V_{ss} = 5V$

## Cmos Inverter



Resistance levels for

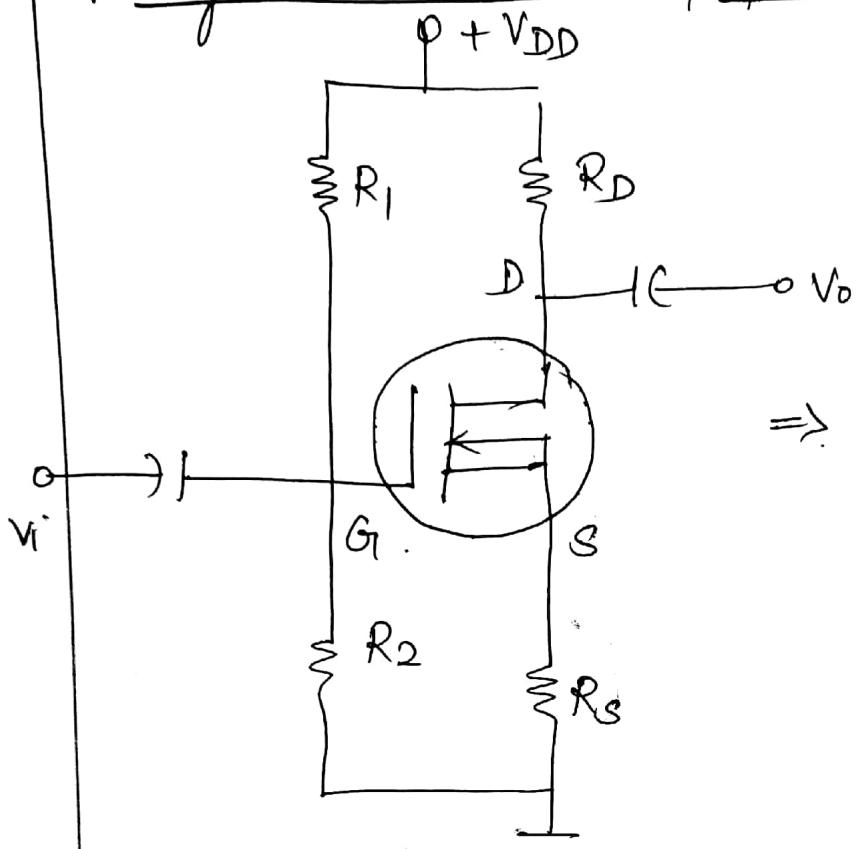


Biasing of MOSFET

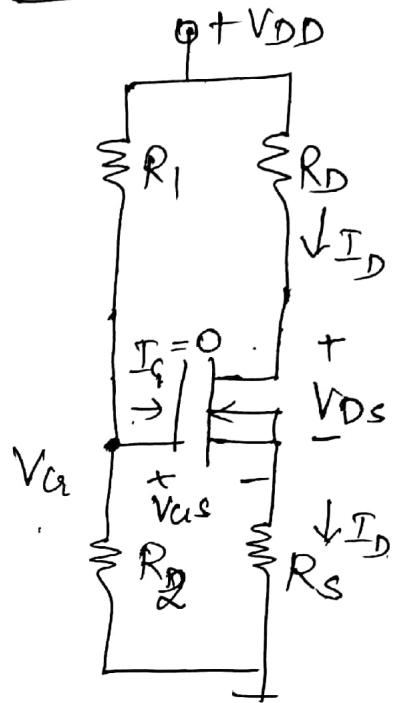
Depletion MOSFET :-

- ① Voltage divider bias
- ② Self bias

Voltage Divider Bias : popular biasing technique :



DC equivalent



Equivalent Circuit

To find  $I_D$ :

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2$$

To find  $V_{GS}$  :-  $I_P$  loop:

$$V_G - V_{GS} - I_D R_S = 0$$

$$V_{GS} = V_G - I_D R_S$$

To find  $V_{DS}$ : off Loop

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

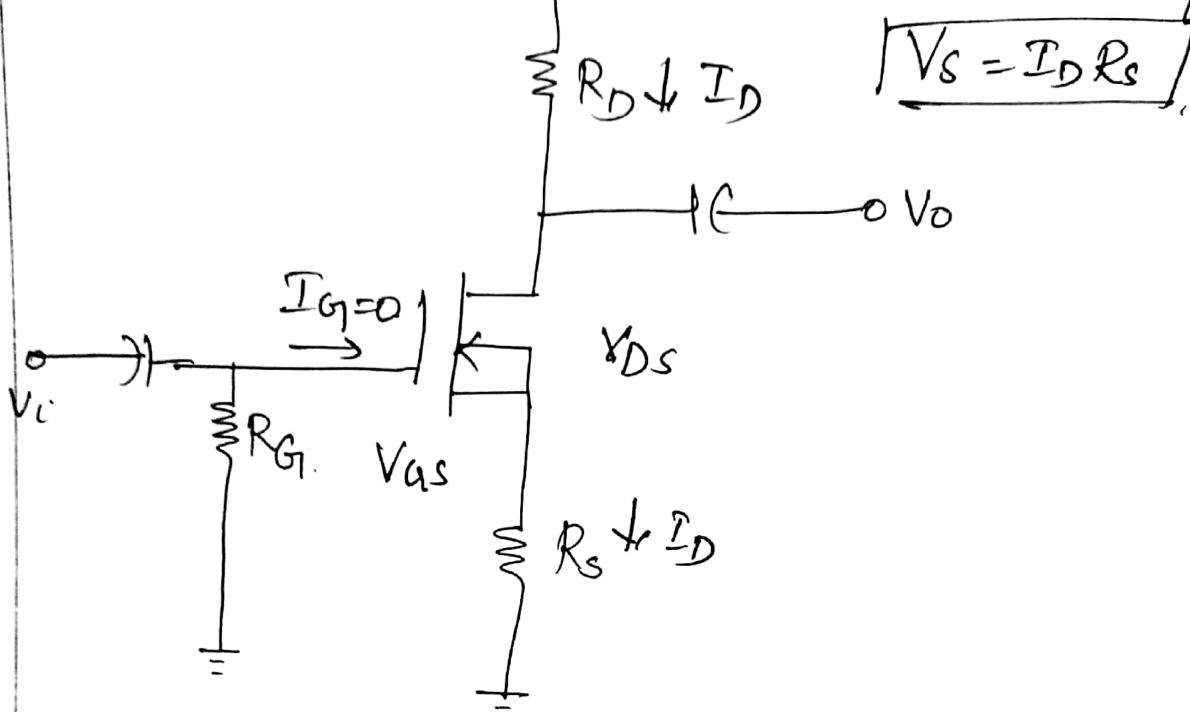
$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$V_G = \frac{R_2 \times V_{DD}}{R_1 + R_2}$$

$$V_D = V_{DD} - I_D R_D$$

If  $V_G G_s$  is very large compared to  $V_{GS}$ , the  $I_D$  is constant.

Self Bias in depletion MOSFET :- When the drain voltage  $V_D$  is applied,  $I_D$  flows even in the absence of  $V_G$ .



DC equivalent circuit

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

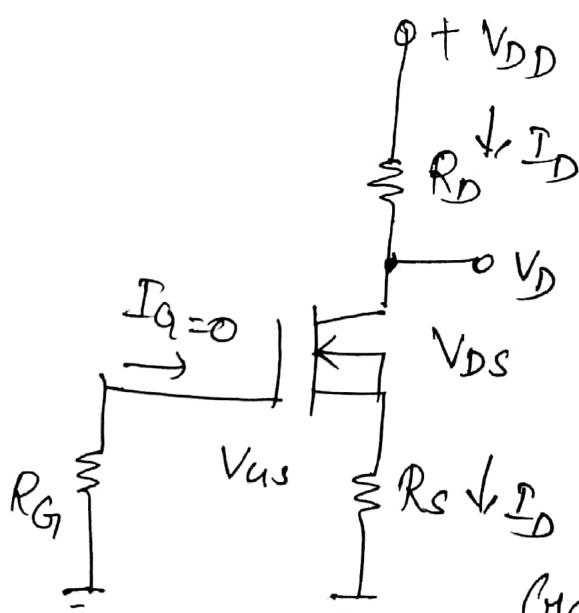
The drain voltage

$$V_D = V_{DD} - I_D R_D$$

Q/P Loop:

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$



Gate to source voltage  $V_{GS}$  is

$$V_{GS} = V_{GSG1} - V_S = 0 - I_D R_S$$

$$V_{GS} = -I_D R_S$$

(8)

When the drain current increases, the voltage drop across  $R_s$  increases. The increased voltage drop increases the reverse gate to source voltage, which decreases the effective width of the channel & hence  $I_D$  decreases.

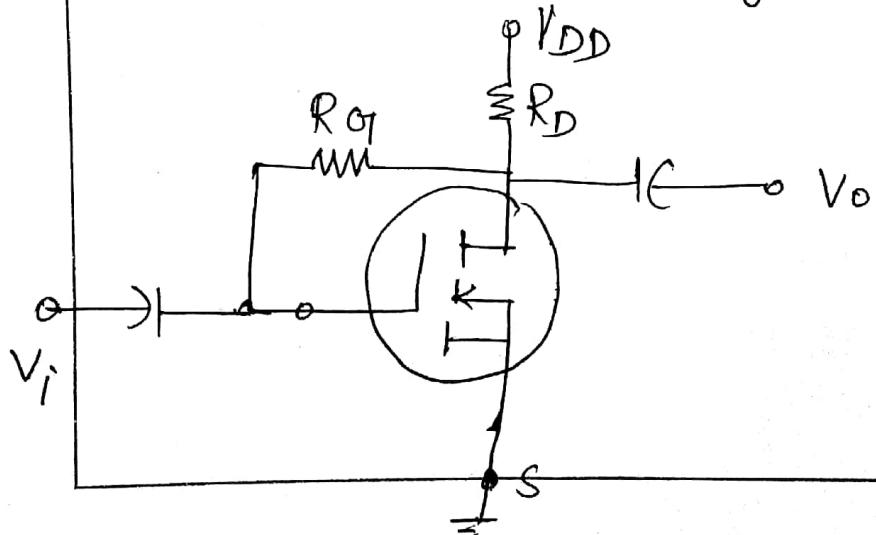
- \* Now the reduced  $I_D$  ~~decreases~~ decreases  $V_{GS}$  & hence width of the channel increases increasing  $I_D$ .

### Enhancement MOSFET Biasing Techniques

$$I_D = K (V_{GS} - V_{GS(Th)})^2$$

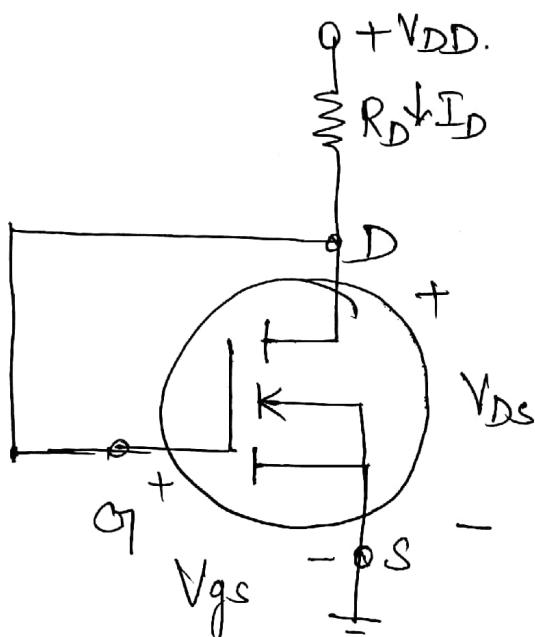
$$K = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

### Feedback Biasing Arrangement



SRM

The resistor  $R_D$  brings large voltage to the gate to drive the MOSFET "on". A direct connection exists b/w gate & drain since  $I_{G_s} = 0 \text{ mA}$  &  $V_{G_s} = 0 \text{ V}$ .



$$V_D = V_{G_s}$$

$$\text{and } V_{DS} = V_{G_s}$$

For o/p circuit

$$V_{DS} = V_{DD} - I_D R_D$$

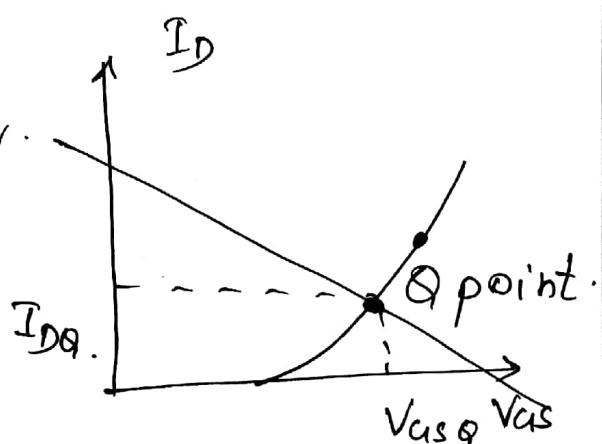
$$\therefore V_{GS} = V_{DD} - I_D R_D \rightarrow \textcircled{1}$$

If  $V_{GS} = 0$  in eqn \textcircled{1}

$$I_D = \frac{V_{DD}}{R_D} / V_{GS} = 0 \text{ V}$$

If  $I_D = 20 \text{ mA}$  in \textcircled{1}

$$V_{GS} = V_{DD}$$

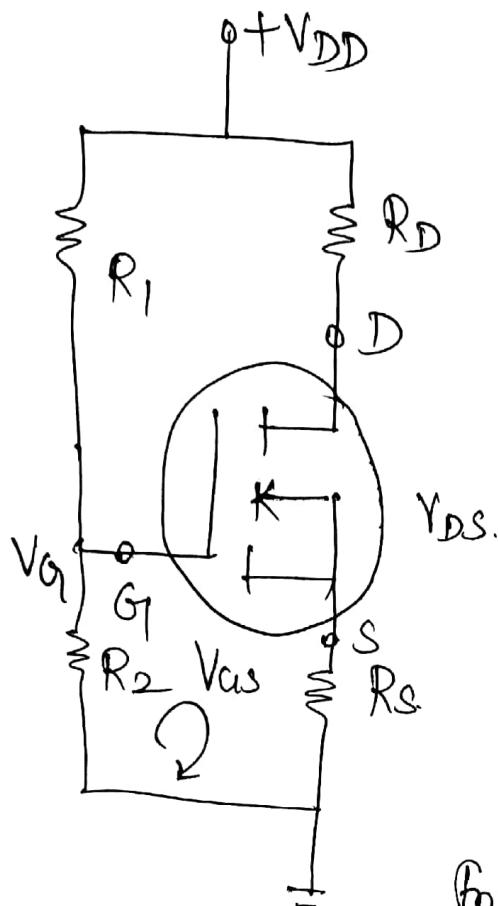


\textcircled{2}

Voltage divider biasing:

The fact that  $I_Q \approx 0$  results in

9



$$V_{G_1} = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Apply KVL to i/p loop

$$V_{G_1} - V_{GS} - I_D R_S = 0$$

$$\boxed{V_{GS} = V_{G_1} - I_D R_S}$$

for o/p section

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)}$$

MOSFET Models:-