

18ECC103J Digital Electronics Principles

SEMESTER III

YEAR : 2021-2022

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COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

(Under section 3 of UGC Act, 1956)

SRM Nagar, Kattankulathur-603203



SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SRM Nagar, Kattankulathur-603203.

BONAFIDE CERTIFICATE

Register No: RA2011004010051

Certified to be the bonafide record of work done by S. KUNAL KESHAN of
ECE - B.Tech Degree course in the Practical **18ECC103J Digital Electronic
Principles** in **SRM INSTITUTE OF SCIENCE AND TECHNOLOGY**, Kattankulathur during the
Academic year **2021-2022 (odd Semester)**.

Date:

Lab In-charge

Date:

YEAR COORDINATOR

Submitted for University Examination held in _____ in

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY, Kattankulathur

Date:

Examiner I

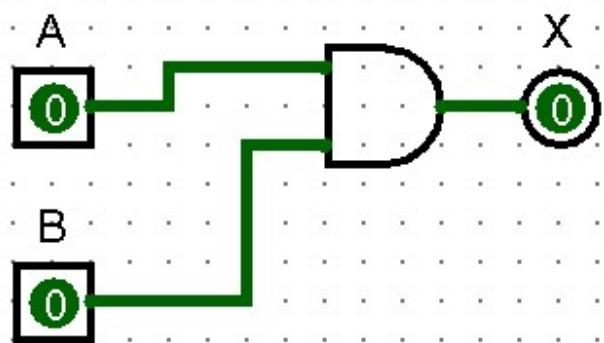
Examiner II

Name : S KUNAL KESHAN
 Reg. No : RA2011004010051

Class : II Year
 Branch : ECE - A

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AND GATE

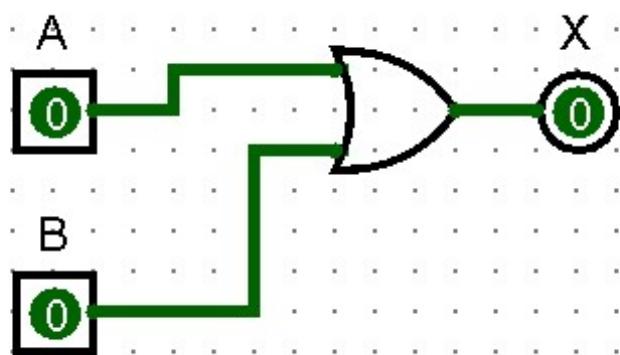
Combinational Analysis

File Edit Project Simulate Window Help

Inputs Outputs Table Expression Minimized

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

Build Circuit



OR GATE

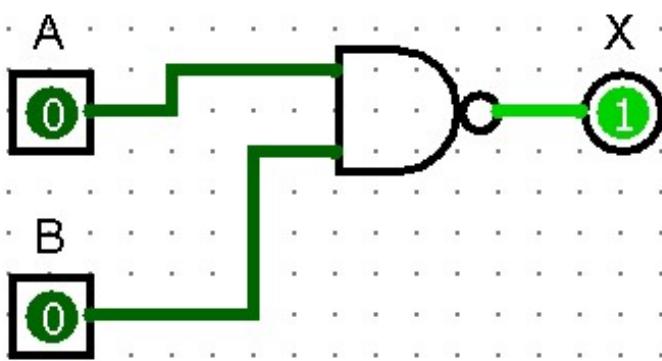
Combinational Analysis

File Edit Project Simulate Window Help

Inputs Outputs Table Expression Minimized

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

Build Circuit



NAND GATE

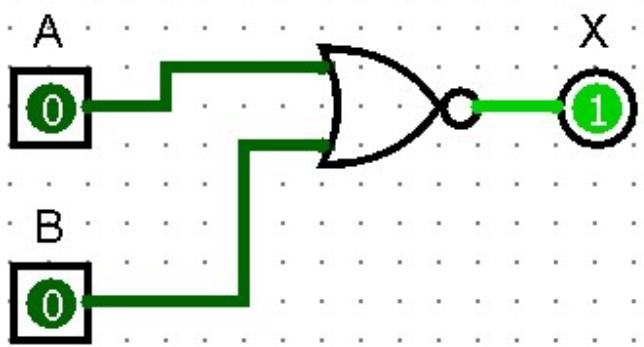
Combinational Analysis

File Edit Project Simulate Window Help

Inputs Outputs Table Expression Minimized

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

Build Circuit



NOR GATE

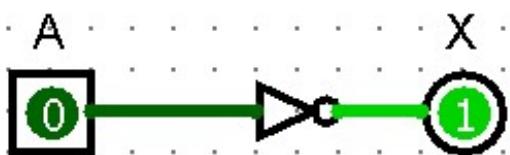
Combinational Analysis

File Edit Project Simulate Window Help

Inputs Outputs Table Expression Minimized

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

Build Circuit



NOT GATE

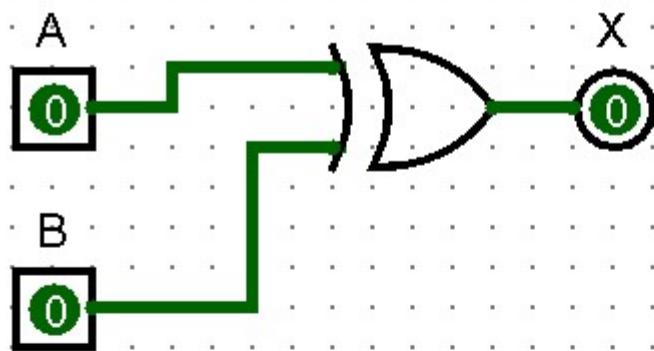
Combinational Analysis

File Edit Project Simulate Window Help

Inputs Outputs Table Expression Minimized

A	X
0	1
1	0

Build Circuit



XOR GATE

Combinational Analysis

File Edit Project Simulate Window Help

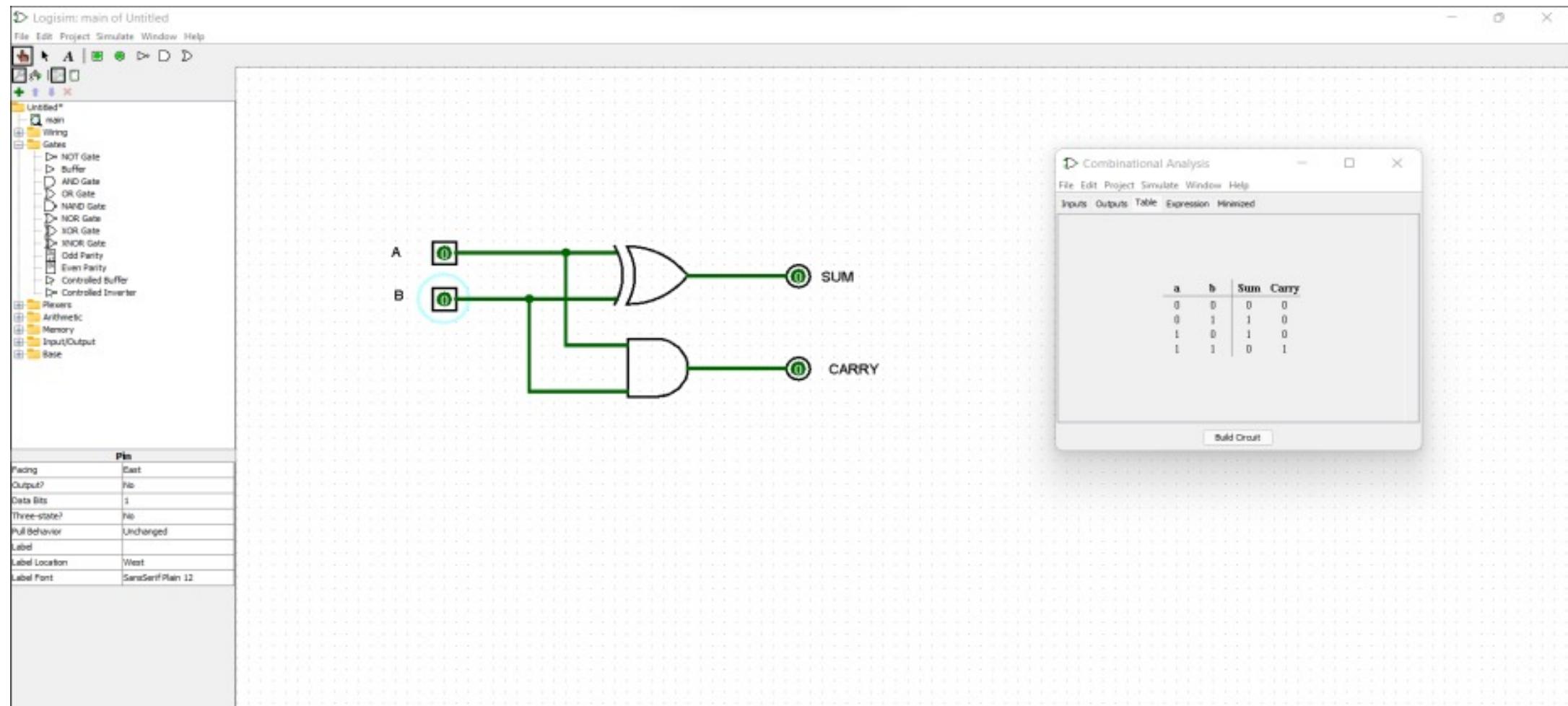
Inputs Outputs Table Expression Minimized

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

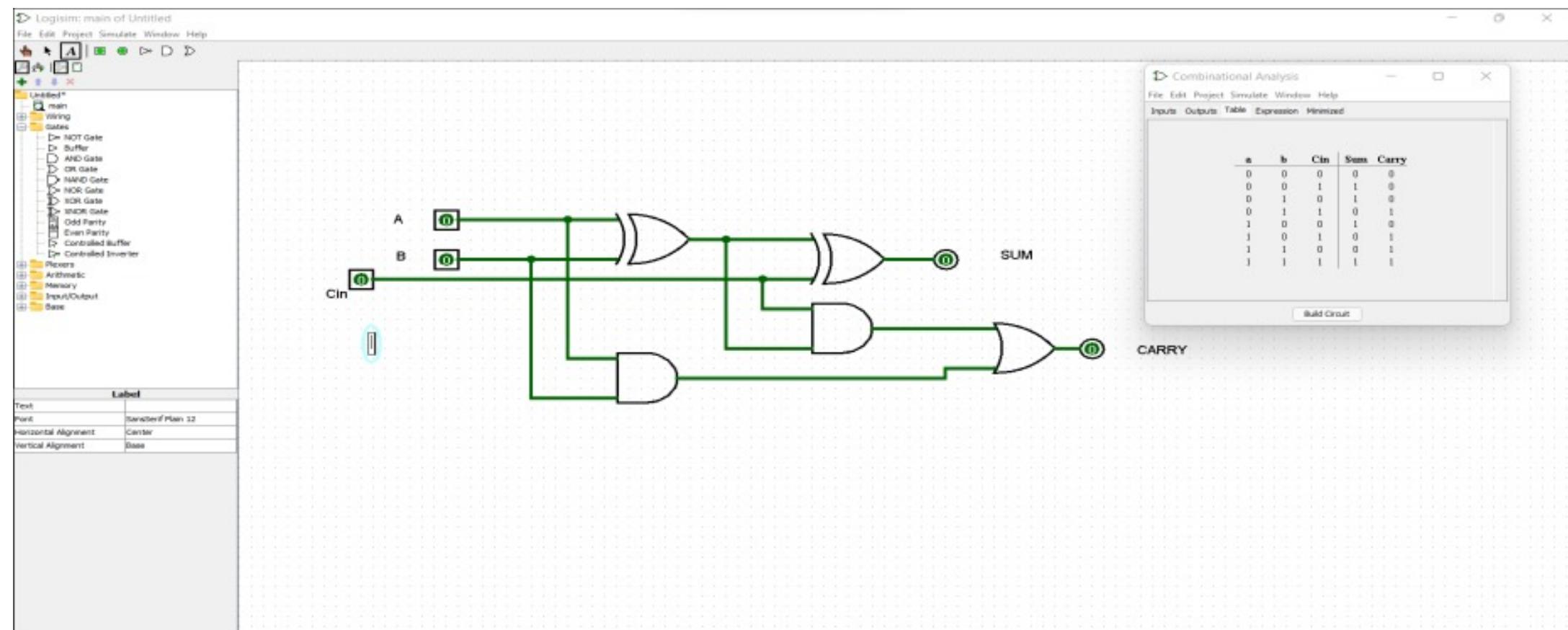
Build Circuit

Experiment 2

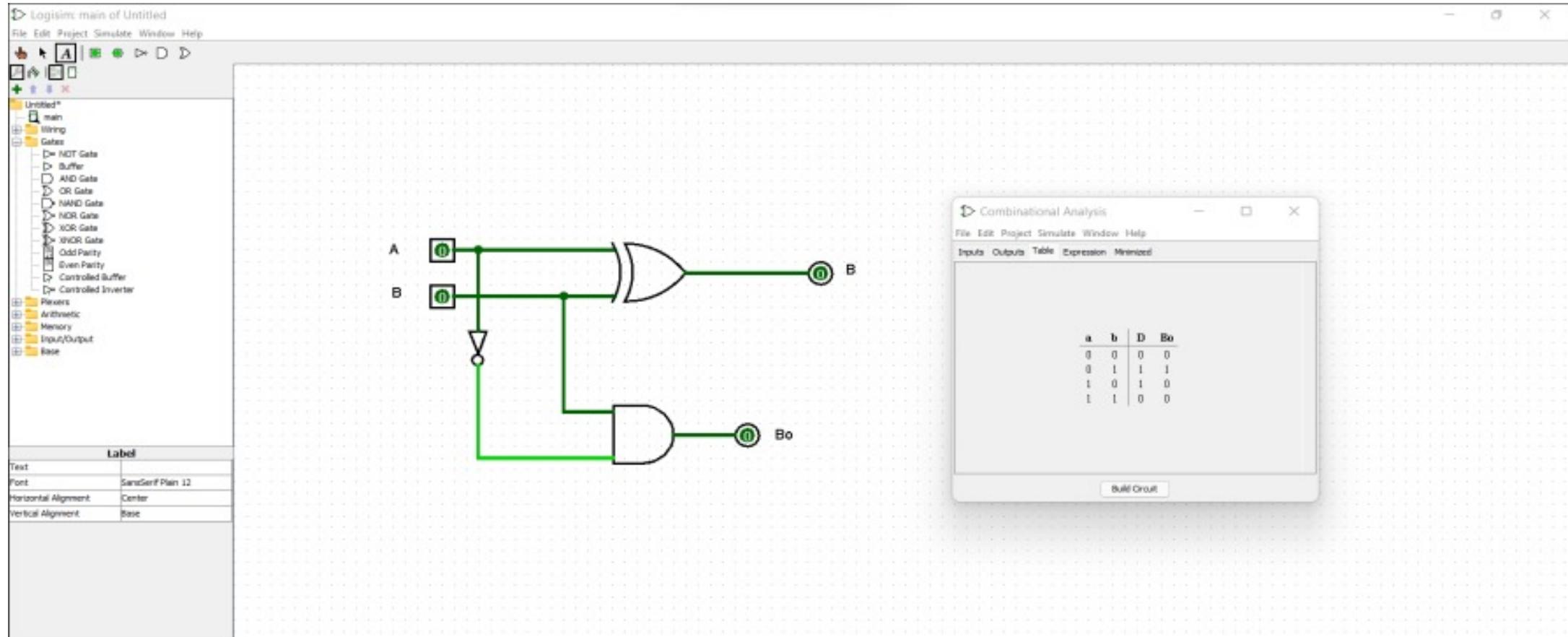
Half Adder



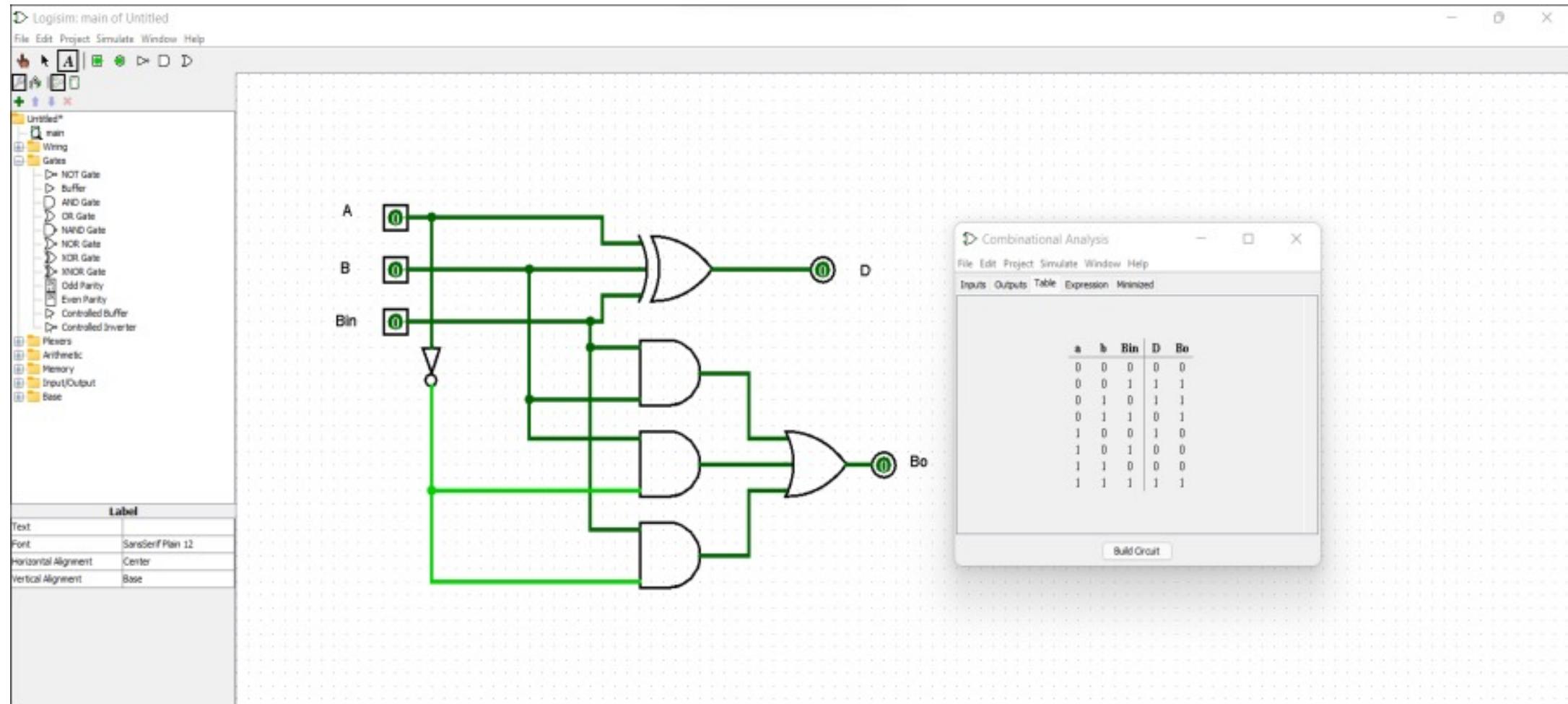
Full Adder

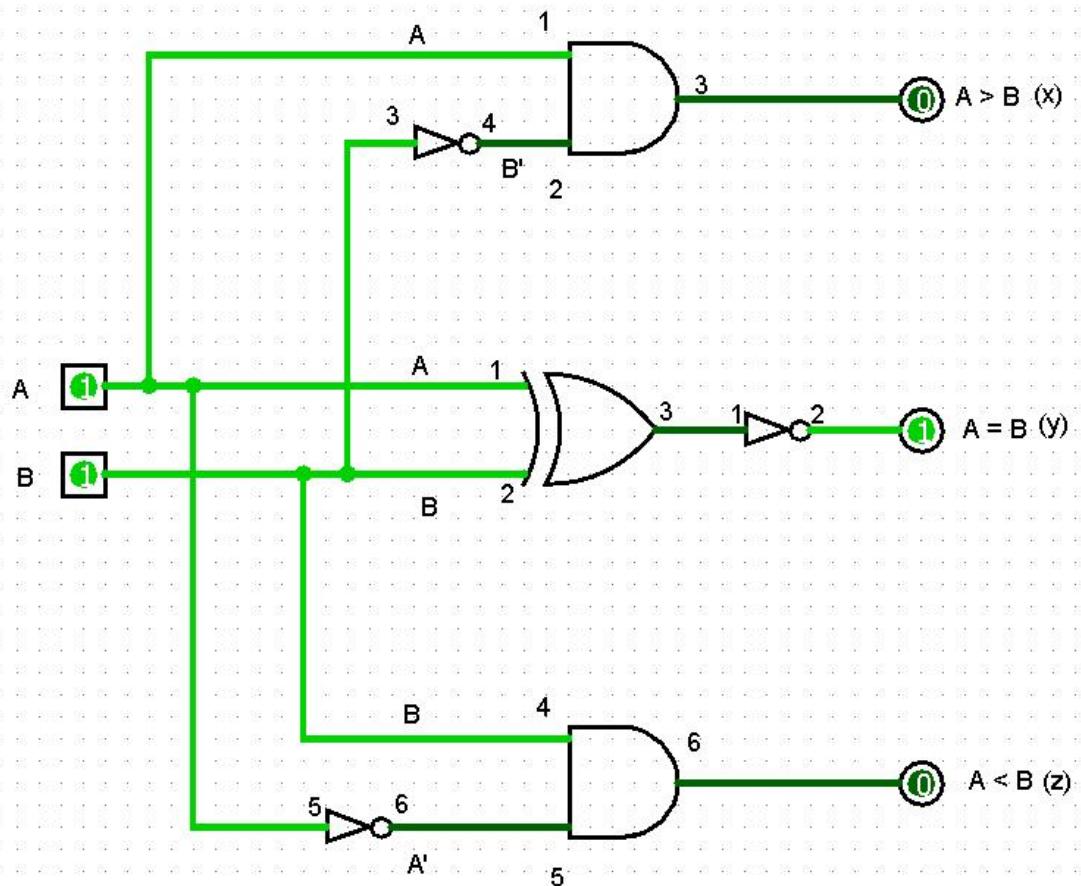


Half Subtractor



Full Subtractor

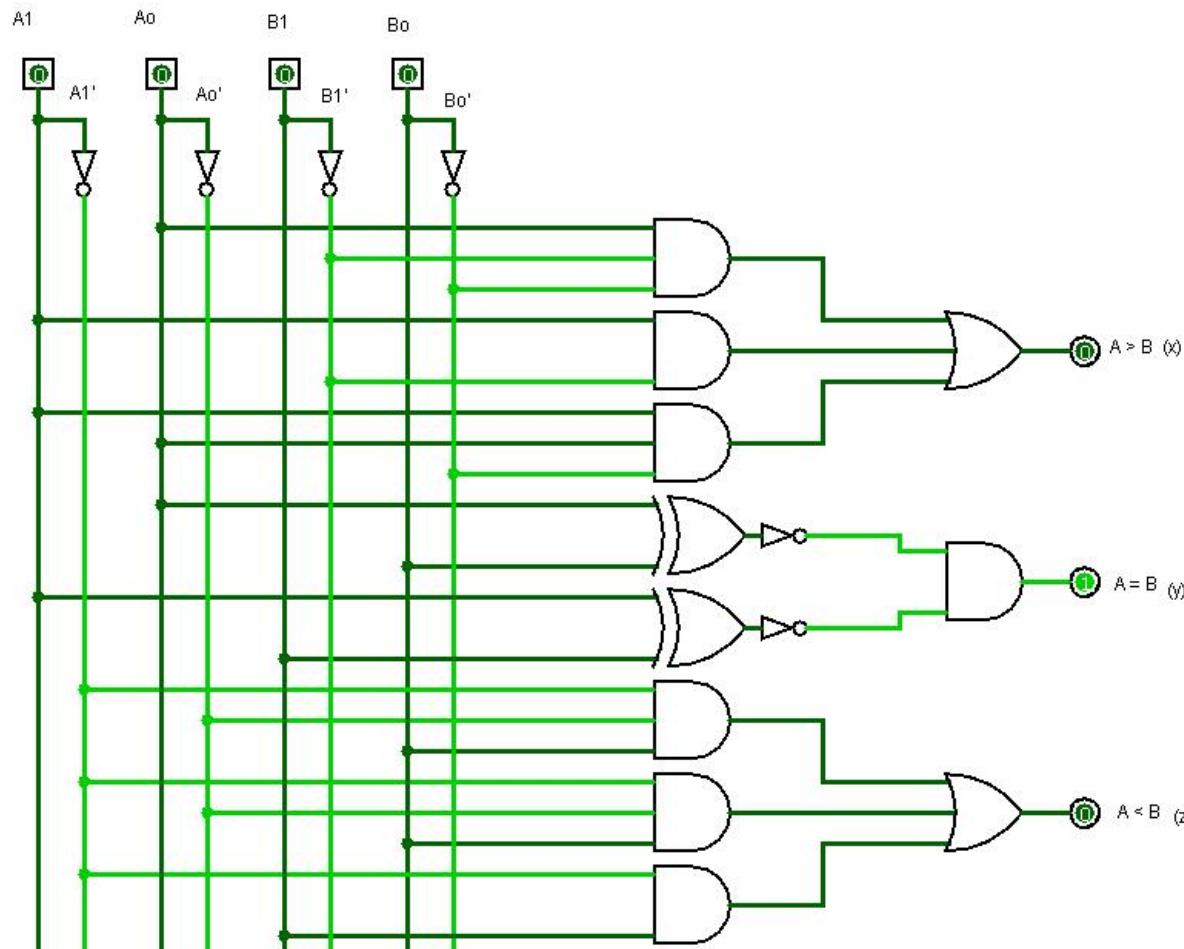




Combinational Analysis

File	Edit	Project	Simulate	Window	Help
Inputs	Outputs	Table	Expression	Minimized	
a 0 0 1 1	b 0 1 0 1	x 0 1 0 0	y 1 0 0 1	z 0 0 1 0	

Build Circuit

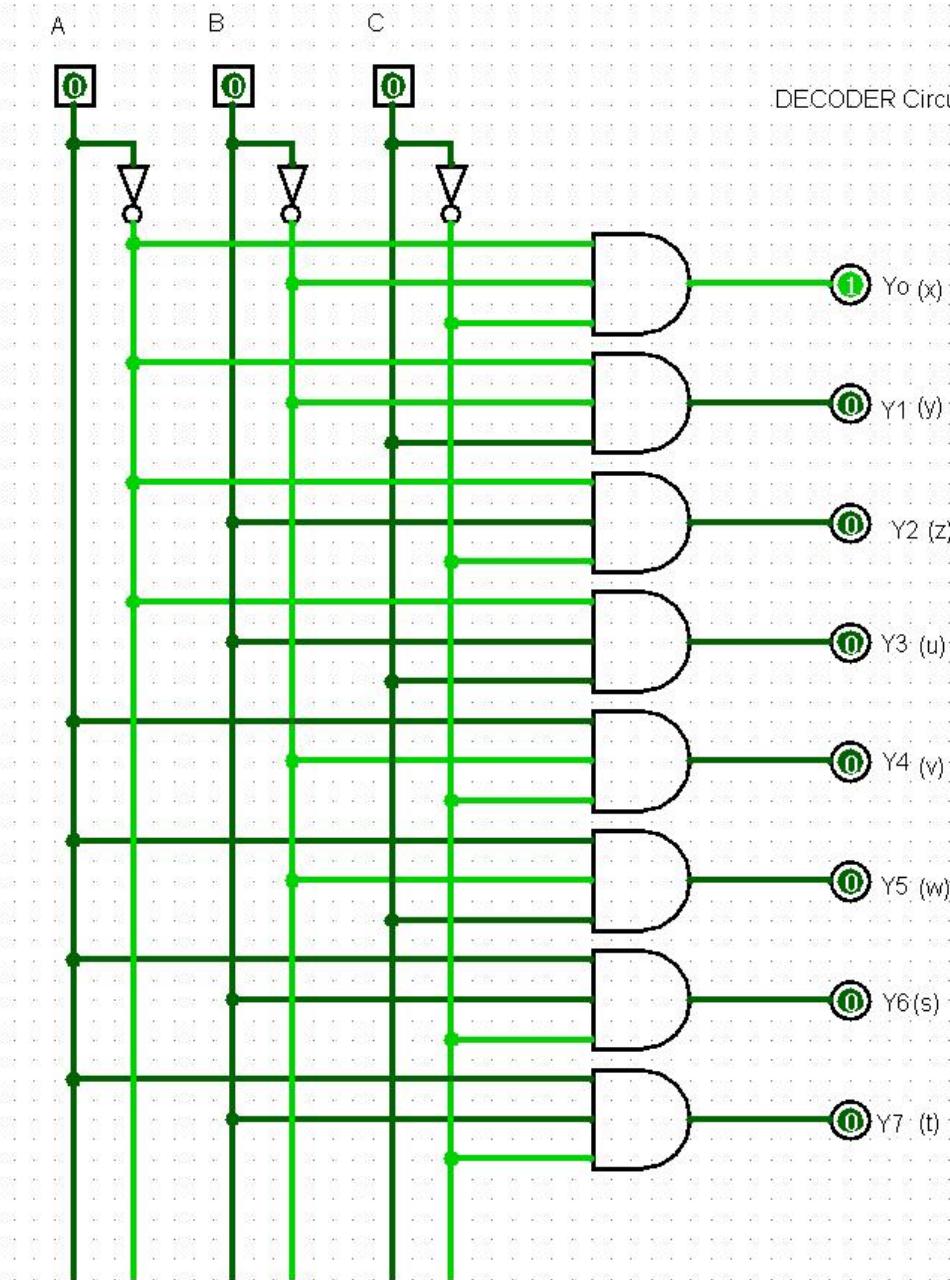


Combinational Analysis

File Edit Project Simulate Window Help

	Inputs	Outputs	Table	Expression	Minimized	
a	b	c	d	x	y	z
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Build Circuit

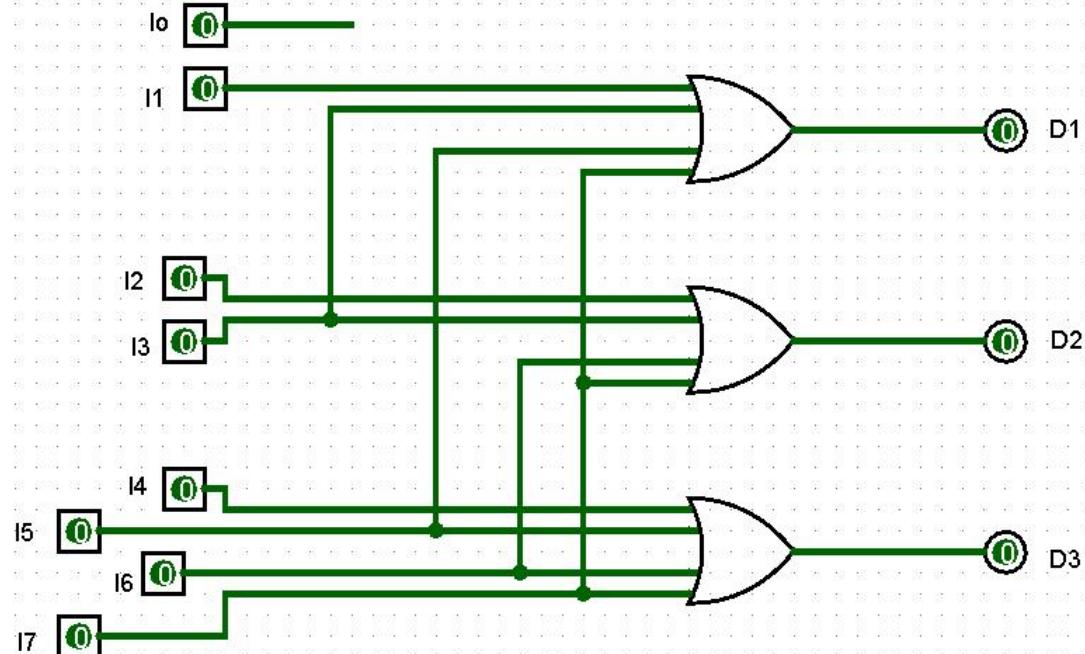


Combinational Analysis

	a	b	c	x	y	z	u	v	w	s	t
0	0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	0	1

Build Circuit

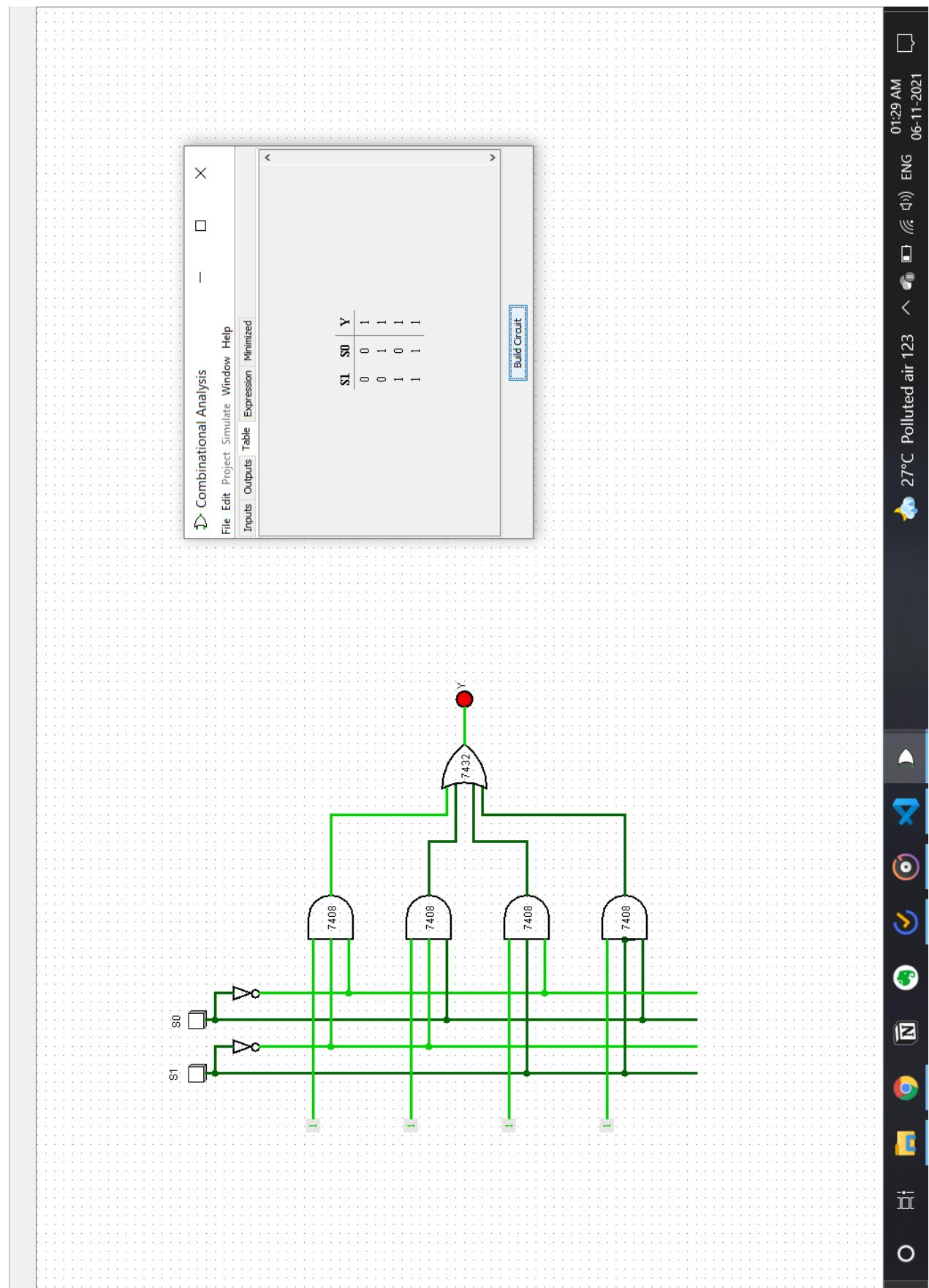
ENCODER CIRCUIT



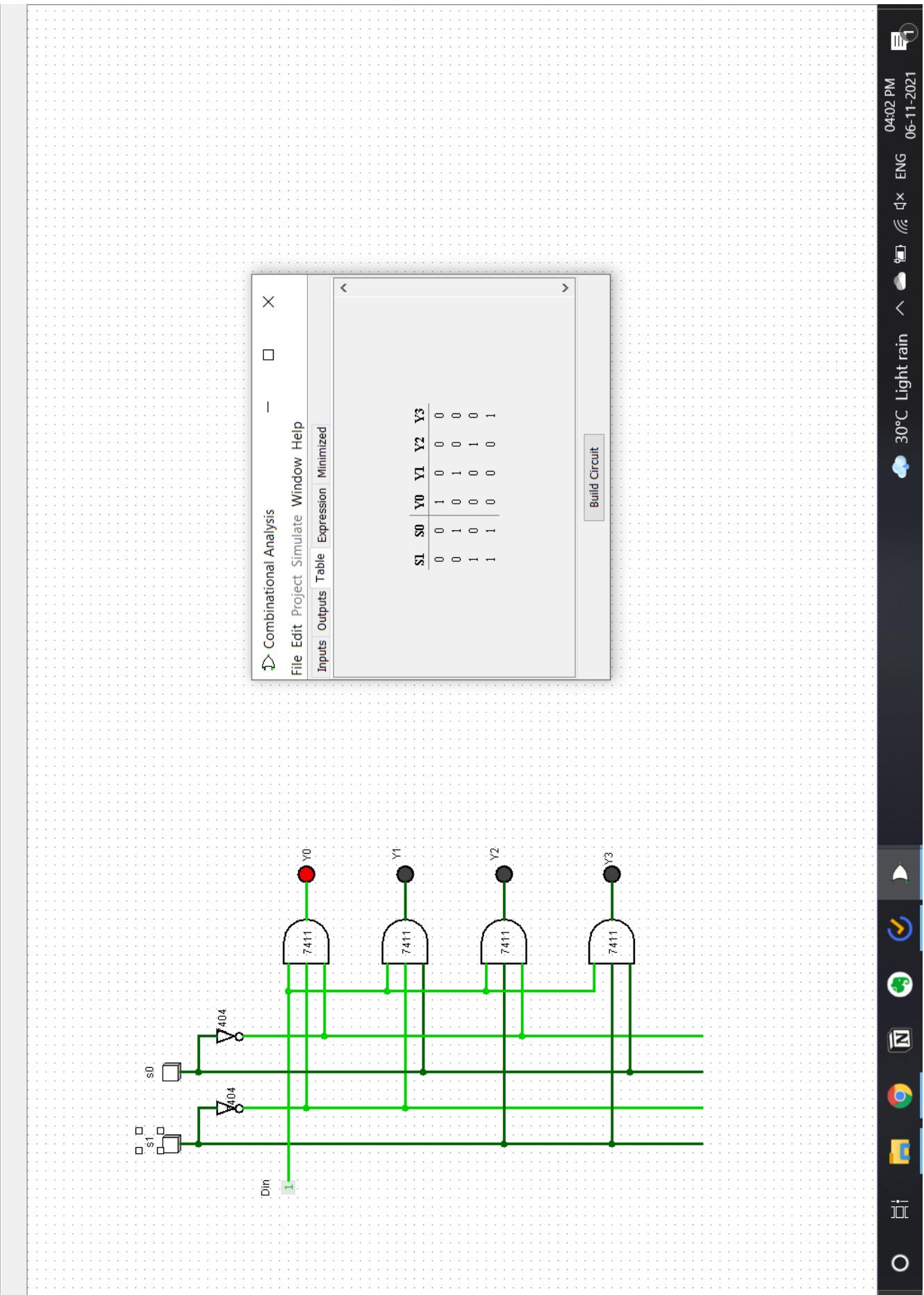
INPUT								OUTPUT			
I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	D ₃	D ₂	D ₁	
1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1	1

Experiment 4

4:1 MUX CIRCUIT

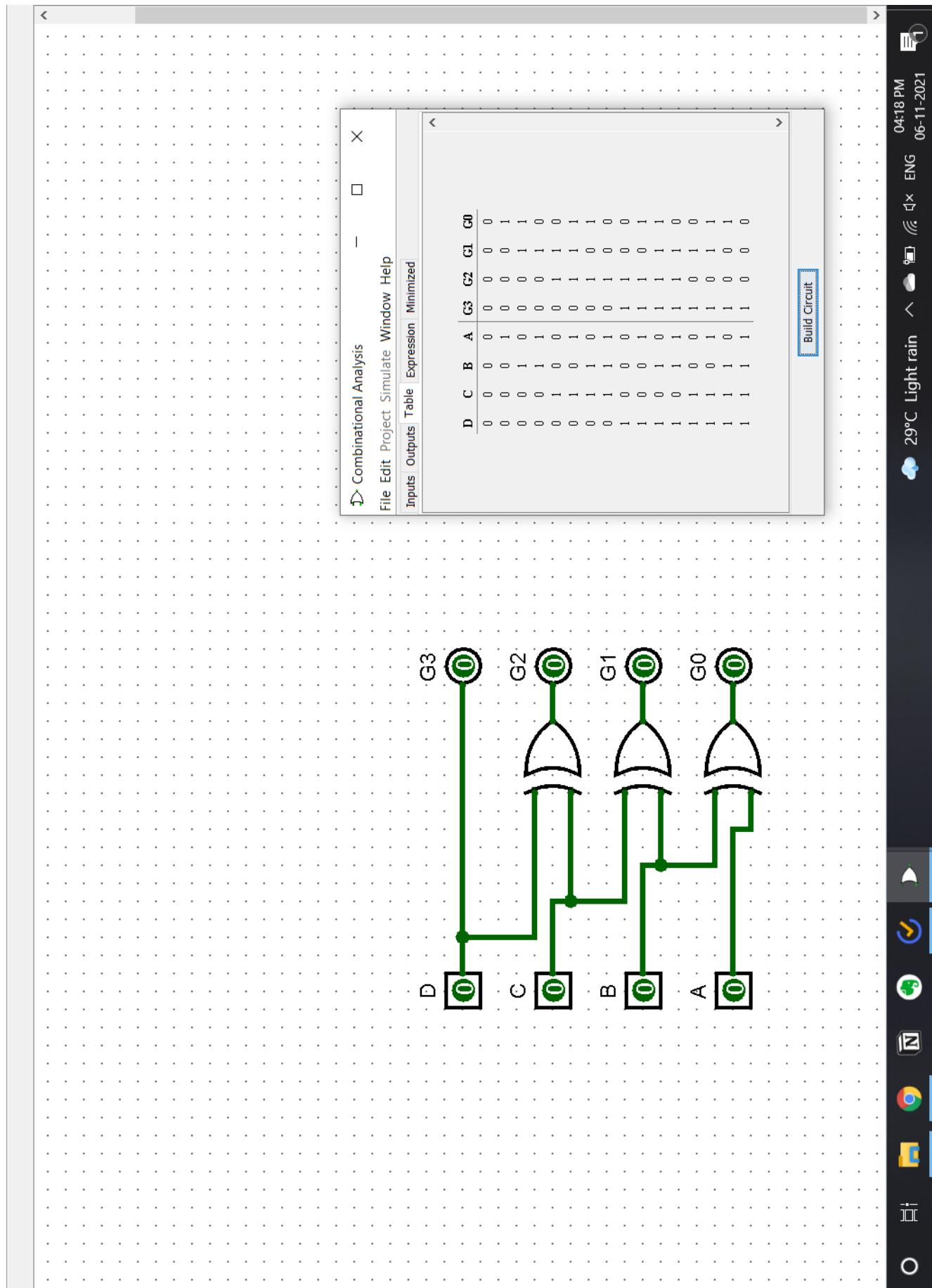


1:4 DeMUX CIRCUIT



Experiment 5

BINARY TO GRAY CONVERTER CIRCUIT



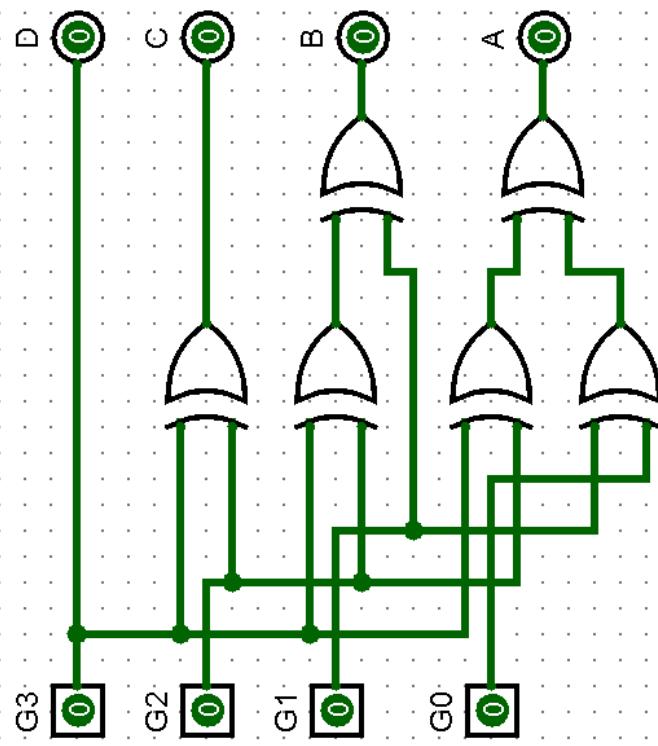
GRAY TO BINARY CIRCUIT

Combinational Analysis

Inputs Outputs Table Expression Minimized

G3	G2	G1	G0	D	C	B	A
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
1	0	0	0	1	1	1	0
1	0	0	1	1	1	0	0
1	0	1	0	0	0	0	1
1	0	1	1	1	0	0	1
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	0	1	0	0
1	1	1	1	1	1	0	0

Build Circuit

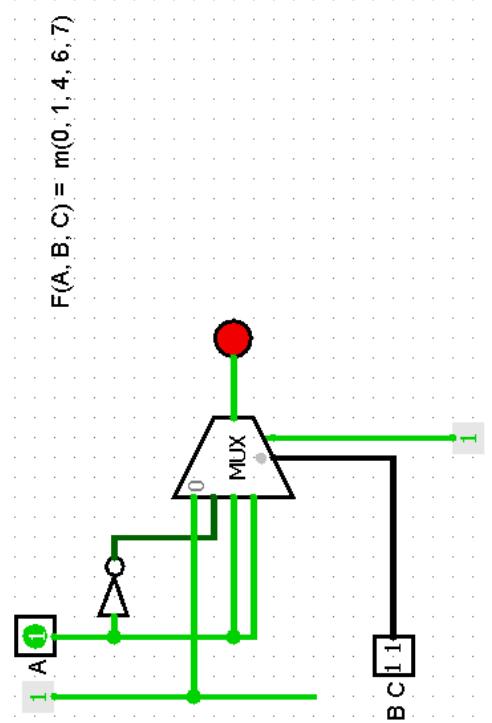


29°C Light rain ~ ☁ 04:32 PM 06-11-2021

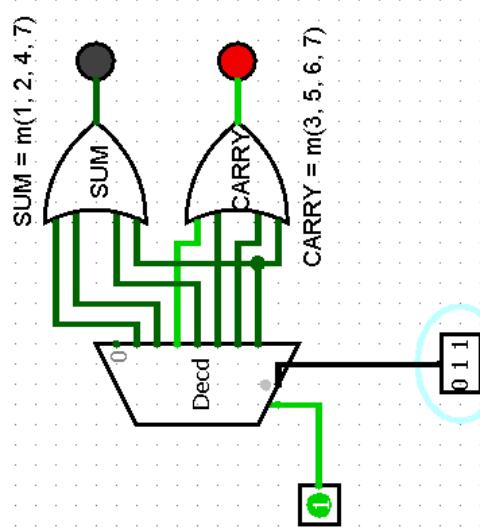


Experiment 7

MUX SOP Operation

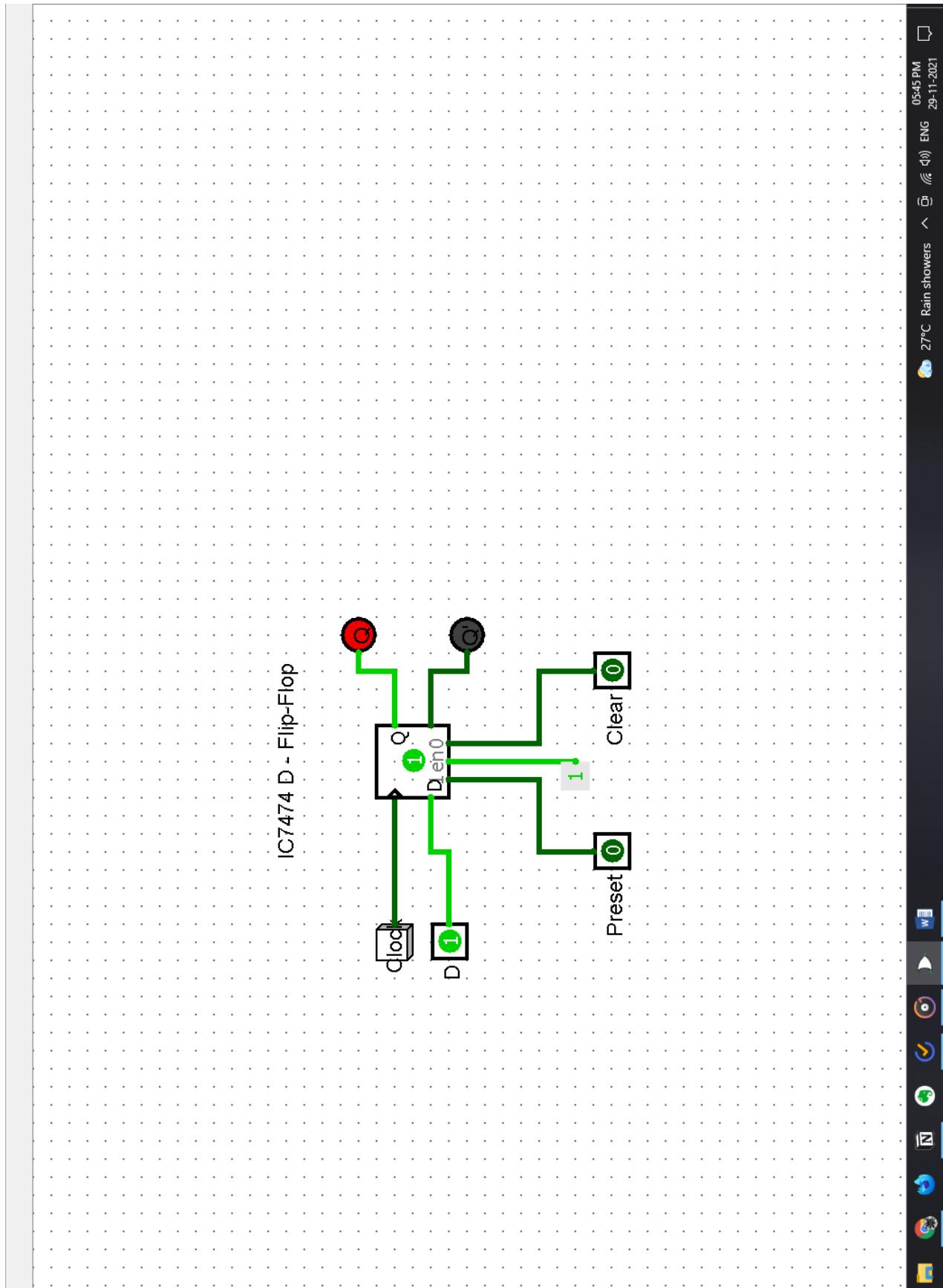


Decoder SOP Operation

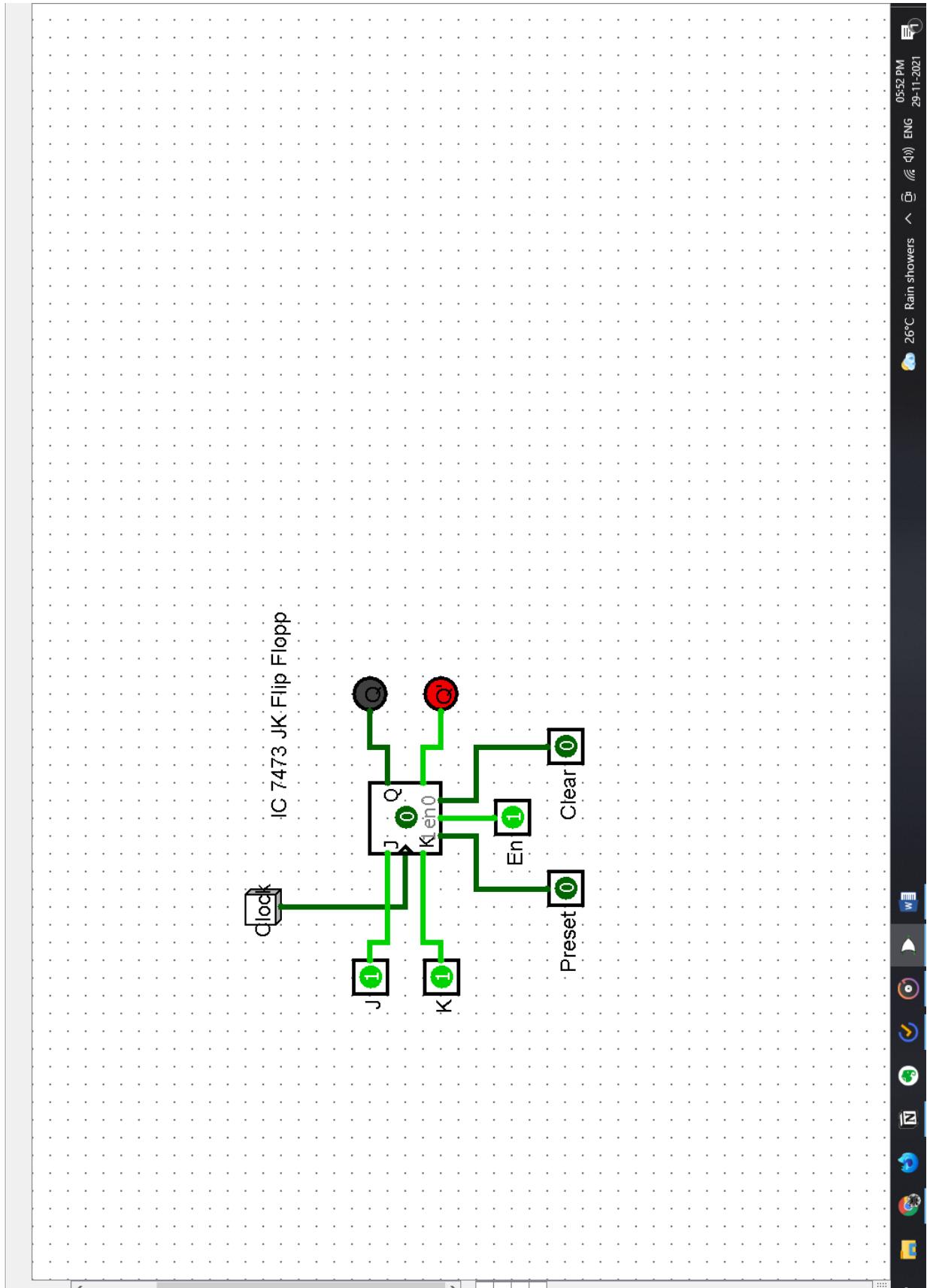


Experiment 8

IC 7474 D Flip-Flop Logism Circuit

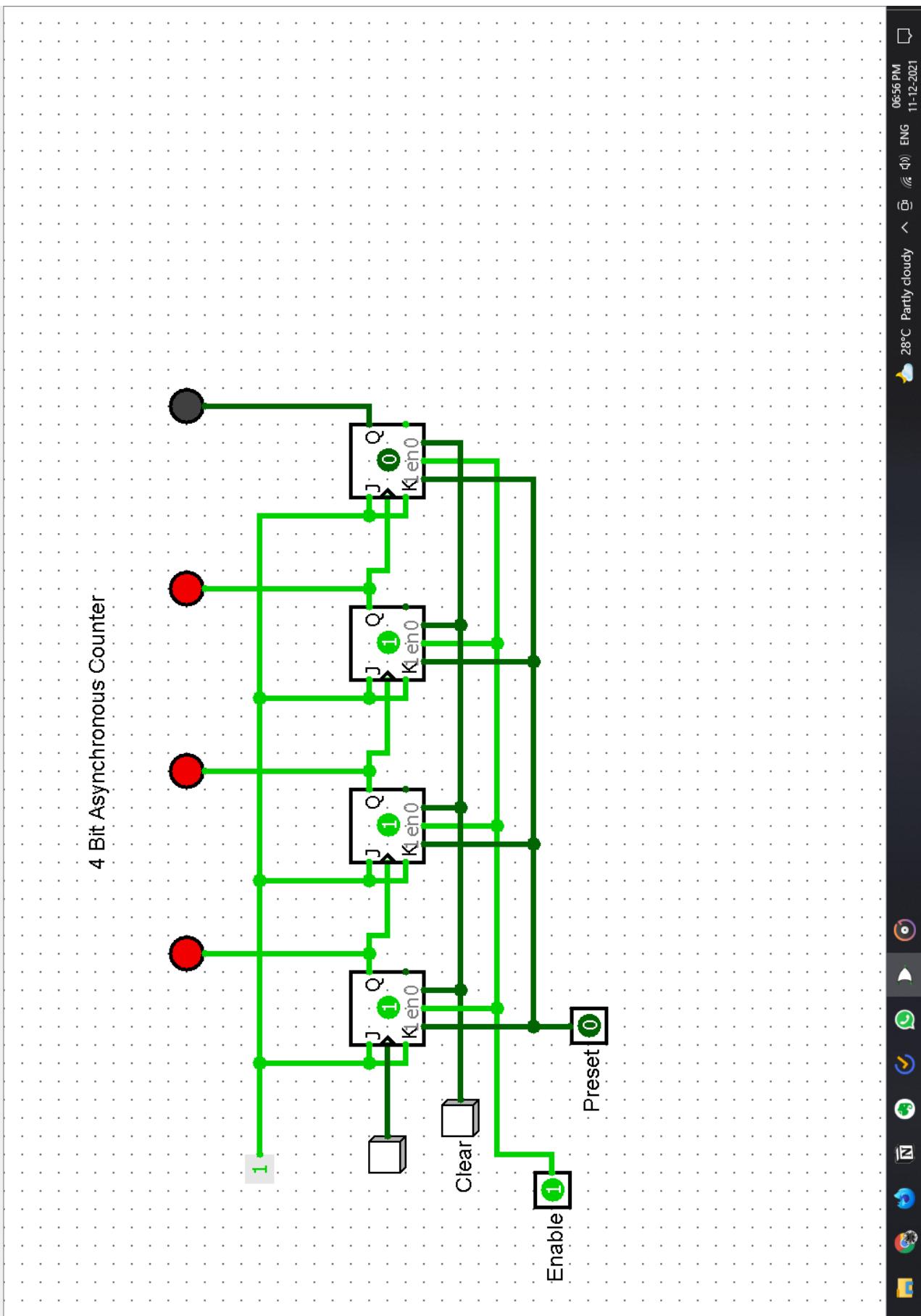


IC7473 J-K Flip-Flop Logism Circuit

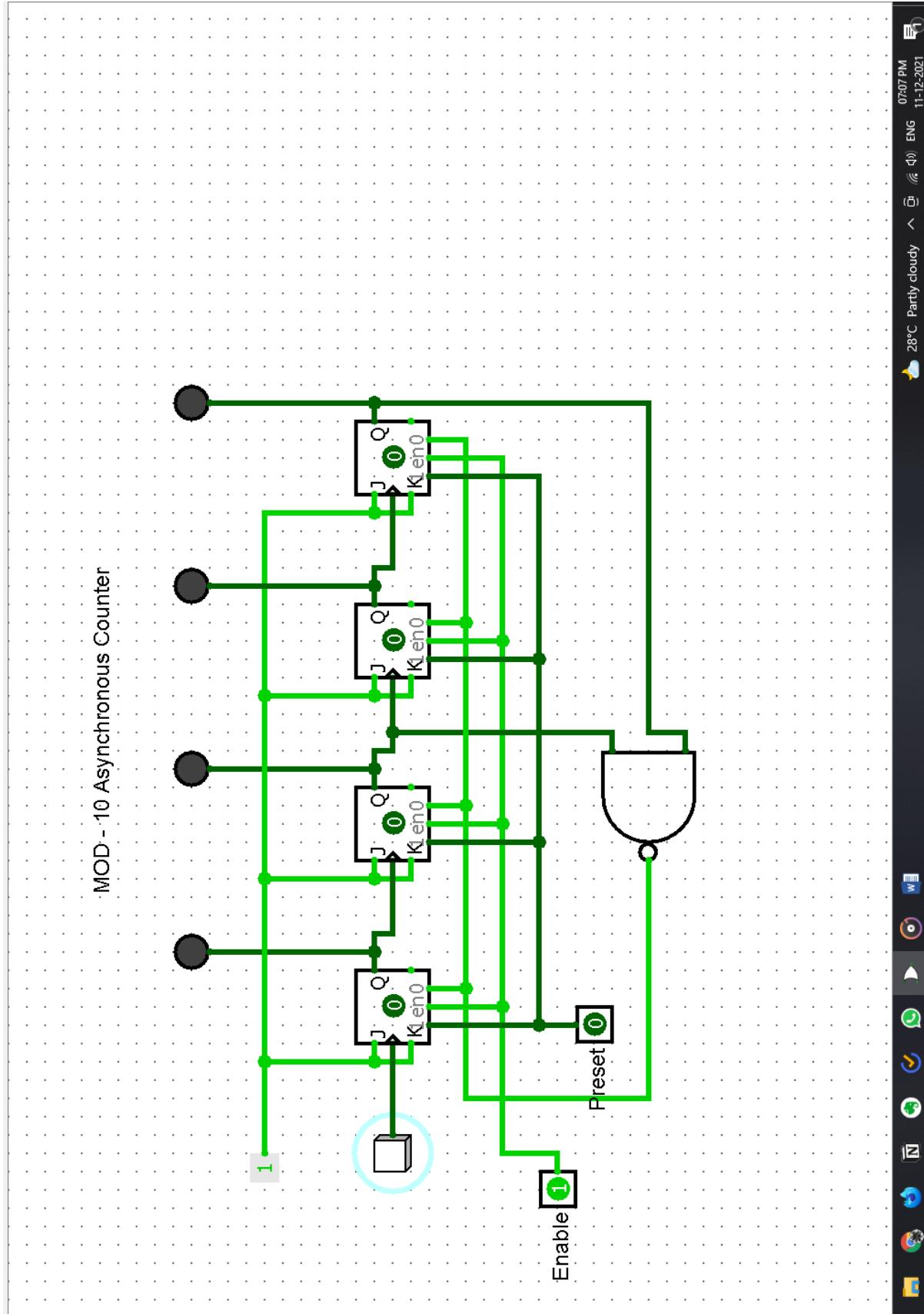


Experiment 9 Design Of Counters

4 Bit Asynchronous Counter



MOD 10 Asynchronous Counter



1

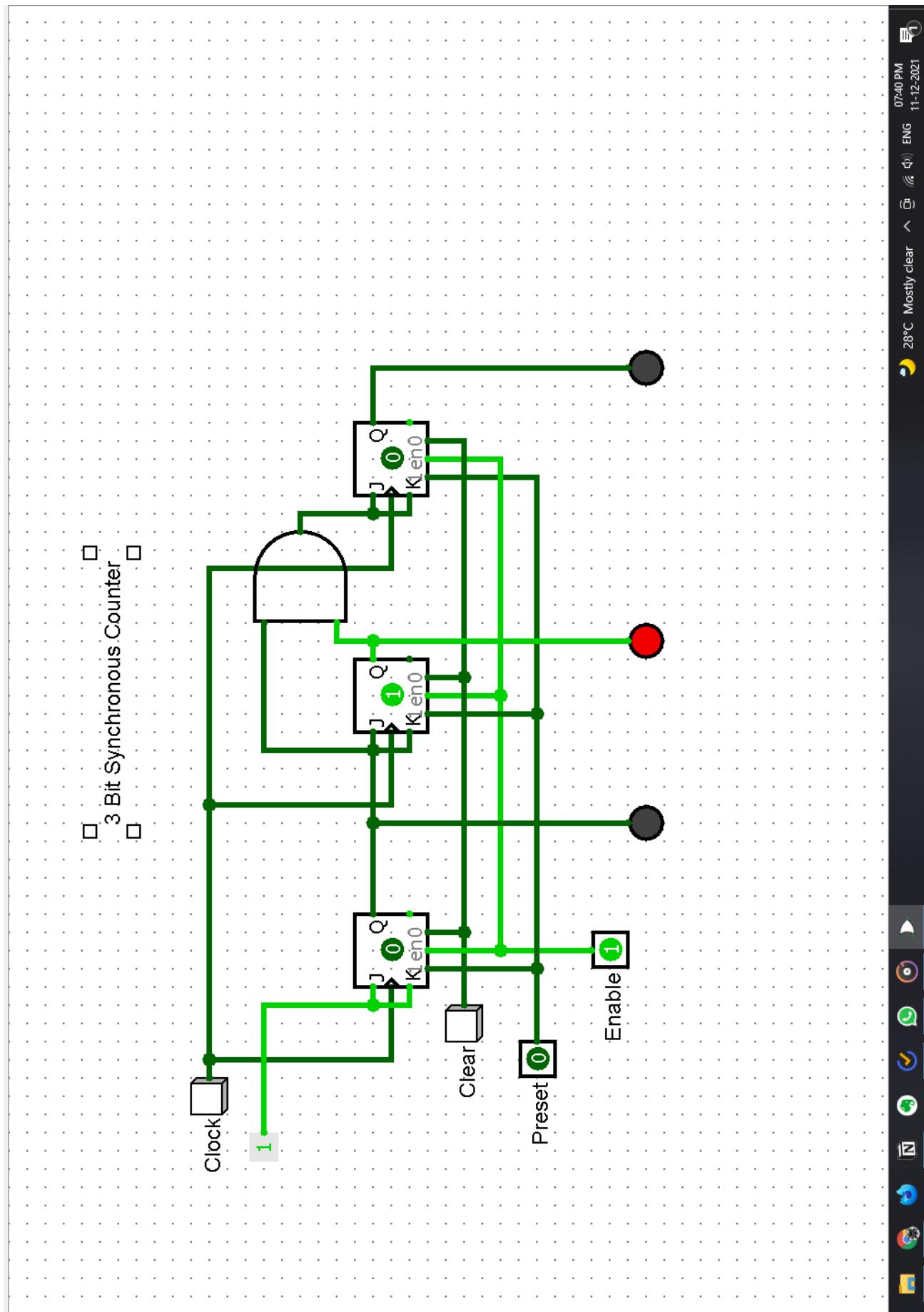
07:07 PM
11-12-2021

28°C Partly cloudy



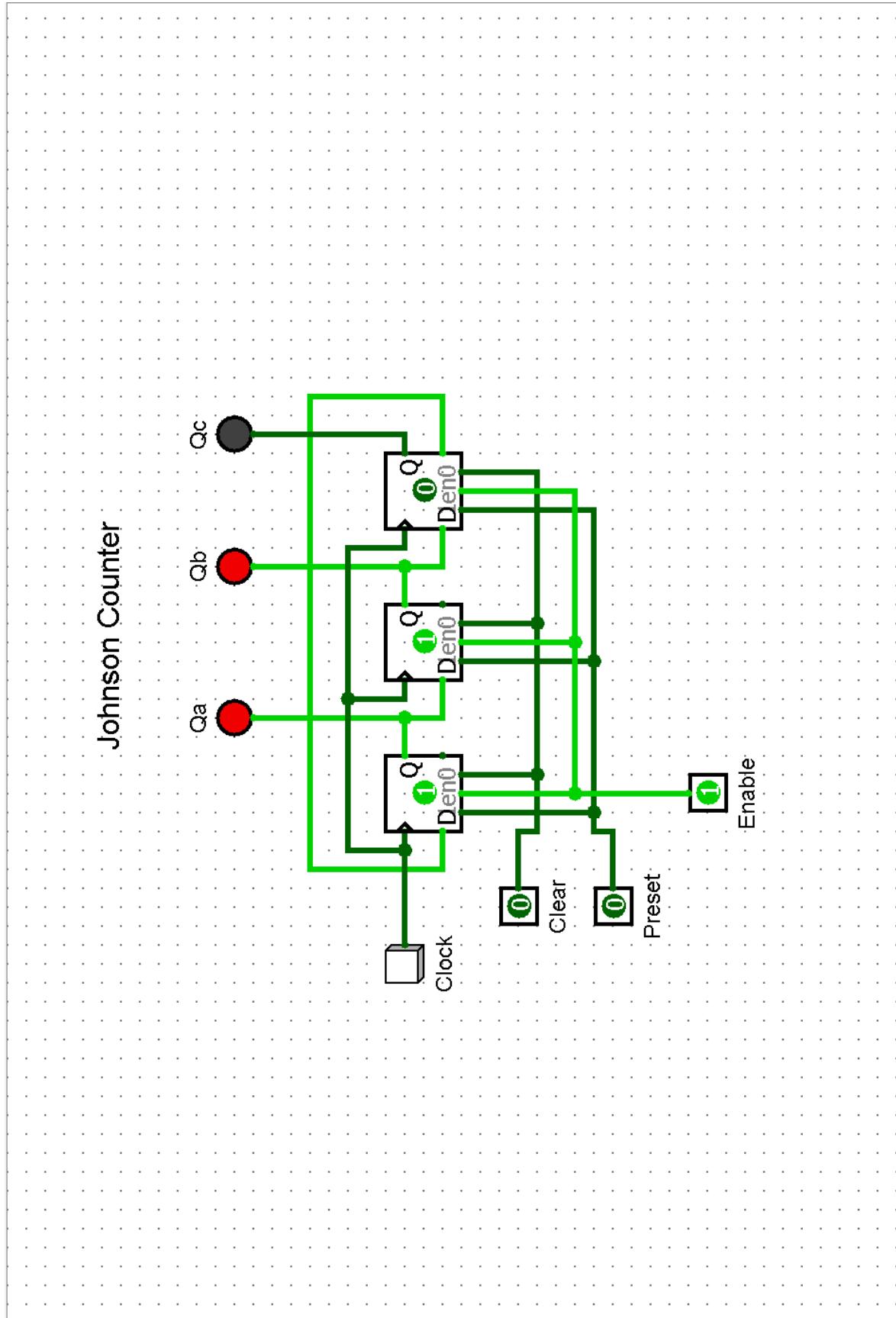
Experiment 10

3 Bit Synchronous Counter



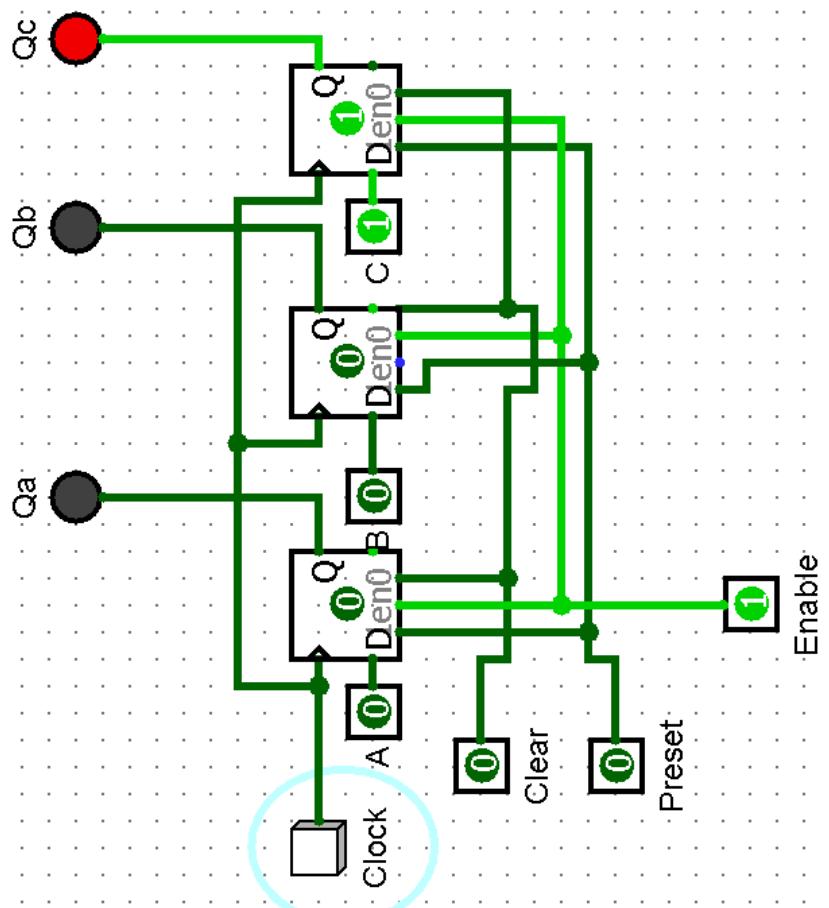
Experiment 11

Johnson Counter



Parallel In Parallel Out Shift Register

Parallel In Parallel Out Shift Register



Serial In Serial Out Shift Register

Serial In Serial Out Shift Register

