

## **Laboratory Report Cover Sheet**

SRM Institute of Science and Technology

Faculty of Engineering and Technology

Department of Electronics and Communication Engineering

**18ECC103J Digital Electronic Principles**

Third Semester, 2021-22(Odd semester)

**Name** :

**Register No.** :

**Day / Session** :

**Venue** :

**Title of Experiment** :

**Date of Conduction** :

**Date of Submission** :

<b>Particulars</b>	<b>Max. Marks</b>	<b>Marks Obtained</b>
Pre-lab questions	10	
In-lab experiment	20	
Post-lab questions	10	
Total	40	

### **REPORT VERIFICATION**

**Date** :

**Staff Name** :

**Signature** :

## **Lab 7. Implementation of SOP function using Multiplexer and Decoder**

**7.1 Aim:** To implement the SOP function using MUX and Decoder

### **7.2 Hardware Requirement**

1. IC74151 - 8:1 Multiplexer
2. IC74LS138 - 3:8 Decoder
3. IC trainer kit
4. Connecting wires

### **7.3 Software Requirement**

5. Logisim

### **7.4 Theory:**

#### **IC74151 8:1 Multiplexer IC**

##### **IC Description:**

74151 is a 8 line-to-1 line multiplexer. It has the schematic representation shown in Fig 1. Selection lines S<sub>2</sub>, S<sub>1</sub> and S<sub>0</sub> select the particular input to be multiplexed and applied to the output.

Strobe S acts as an enable signal. If strobe =1, the chip 74151 is disabled and output y = 0. If strobe = 0 then the chip 74151 is enabled and functions as a multiplexer. Table 1 shows the multiplex function of 74151 in terms of select lines.

#### **3x8 Decoder using IC74LS138**

Decoder is the combinational circuit which contains ‘n’ input lines to  $2^n$  output lines. The decoder is used for converting the binary code into the octal code. The IC74138 is the 3\*8 decoder which contains three inputs and eight outputs and also three enables out of them two are active low and one is active high. Decoders are used in the circuit where required to get more outputs than that of the inputs which also used in the chip designing process for reducing the IC chip area.

#### **Implementation of SOP function using multiplexer**

There are certain steps involved in it:

Step 1: Draw the truth table for the given number of variable function.

Step 2: Consider one variable as input and remaining variables as select lines.

Step 3: Form a matrix where input lines of MUX are columns and input variable and its compliment are rows.

Step 4: Find common between both rows on the basis of the truth table.

Step 5: Hence whatever is found is considered as input of MUX.

### Example:

Given SOP function  $f(A, B, C) = m(0, 1, 4, 6, 7)$  and MUX is

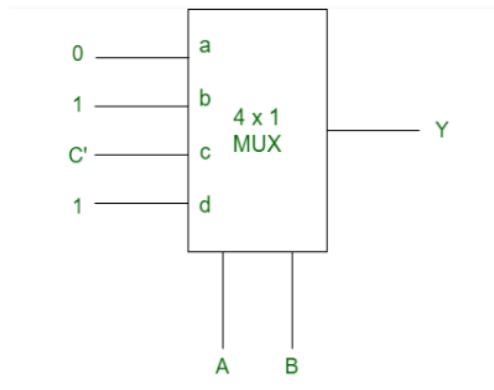


Fig 7.1 mux implementation

### Logisim connection

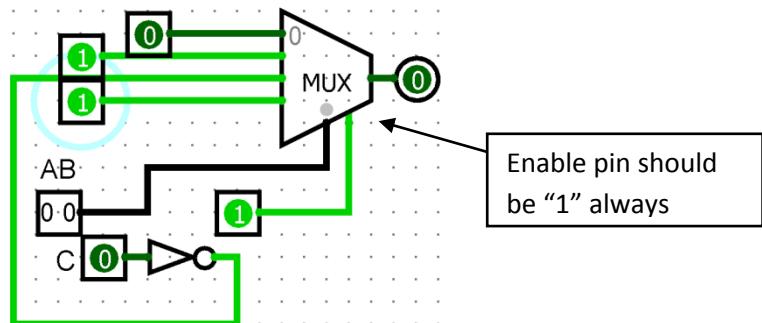


Fig 7.2 MUX Logisim Implementation

1. Take the mux from the plexers in the menu bar.
2. By changing the “select bits” 2x1 will be converted to any variant.
3. Inputs A,B are clubbed by changing the data bits when picking the input pin.
4. Now change the value of inputs and verify the SOP function in the truth table.

### Combinational Logic Implementation using Decoder:

A decoder takes N input lines and  $2^N$  has output lines. These output lines can provide the  $2^N$  min terms of N input variables.

Since any Boolean function can be expressed as a sum of min terms, a decoder that can generate these min terms along with external OR gates that form their logical sums, can be used to form a circuit of any boolean function.

For example, if we need to implement the logic of a full adder, we need a 3:8 decoder and OR gates. The input to the full adder, first and second bits and carry bit, are used as input to the decoder. Let x, y and z represent these three bits. The SOP functions of Sum and Carry outputs of a full adder as in figure 7.3 S= $\sum m(1,2,4,7)$ , C= $\sum m(3,5,6,7)$

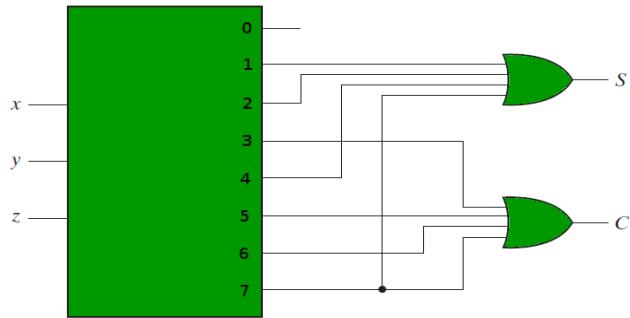


Fig 7.3 Full-adder

### Logisim connection

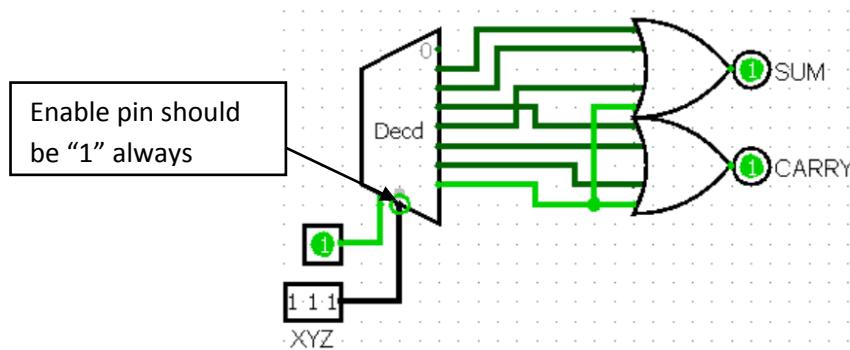


Fig 7.4 Decoder Logisim Implementation

1. Take the Decoder from the plexers in the menu bar.
2. By changing the “select bits” get the suitable decoder.
3. Inputs A,B,C are clubbed by changing the data bits when picking the input pin.
4. Now change the value of inputs and verify the SOP function in the truth table.

### MULTIPLEXER

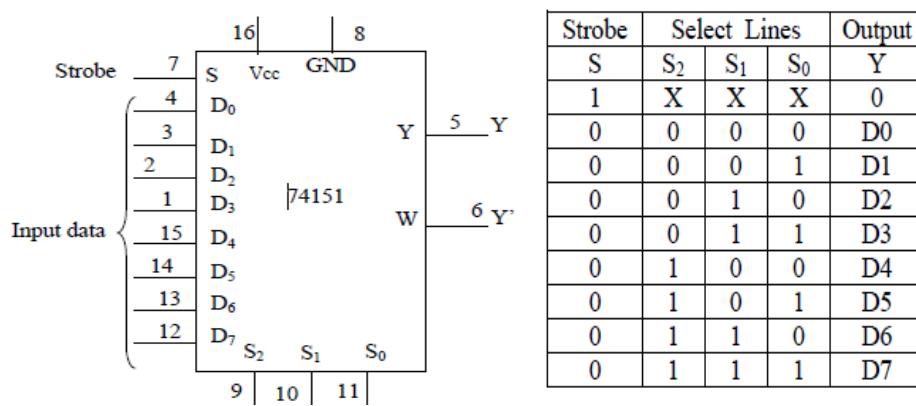


Fig 7.5. IC74151 Pin Description.

## DECODER

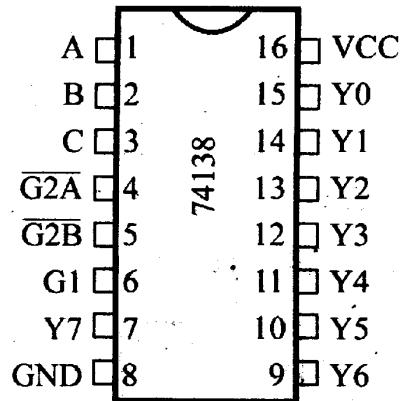


Fig 7.6: IC74138 Pin Description

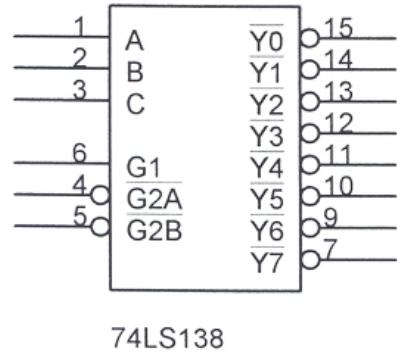


Fig 7.7: IC74138 Circuit connection

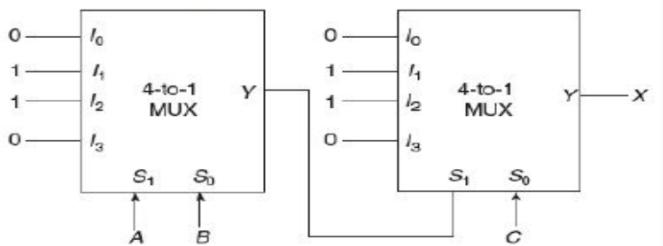
Truth table of Decoder

G1	$\overline{G2}^*$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

$$* \overline{G2} = \overline{G2A} + \overline{G2B}$$

## 7.5 Pre lab Questions

1. Find the output boolean expression X for the given figure?



2. Design 4-bit parity generator using Multiplexer IC.  
 3. What are the difference between Decoder and Demultiplexer?  
 4. Give some examples for standard combinational circuit ICs.

## 7.6 Procedure:

### Software

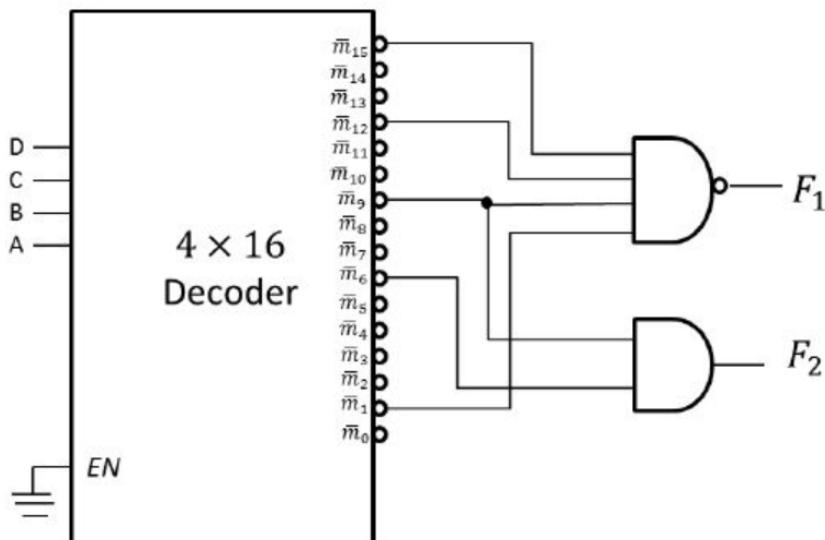
1. Connect the given SOP function for the given example in Multiplexer and Decoder as shown in the figure 7.2 and 7.4 respectively.
2. **Here each faculty can assign different SOP Functions suitable for Decoder and Multiplexer**

### Hardware

1. Connect the IC74151 and IC74138 in trainer kit and connect the inputs and outputs.
2. Give proper logic values to enable and strobe pin , And verify the truth table.

## 7.7 Post Lab Questions

1. Implement  $F(W,X,Y,Z) = \Sigma m(1,2,5,7,9,12,15)$  using suitable IC74151.
2. The 3x8 decoder shown has active low outputs. Find SOP terms for  $F_1$  and  $F_2$  from the given figure.



3. Implement the function  $F(A,B,C,D) = \Sigma m(1,3,4,11,12,13,14,15)$  using MUX. Draw its truth table and its logic symbol.
4. Realize the SOP expression  $y = \Sigma m(1,4,5)$  using 74LS138 decoder.
5. Realize the POS expression  $y = \prod m(0,2,3,6,7)$  using 74LS138 decoder.

## 7.8 Result: