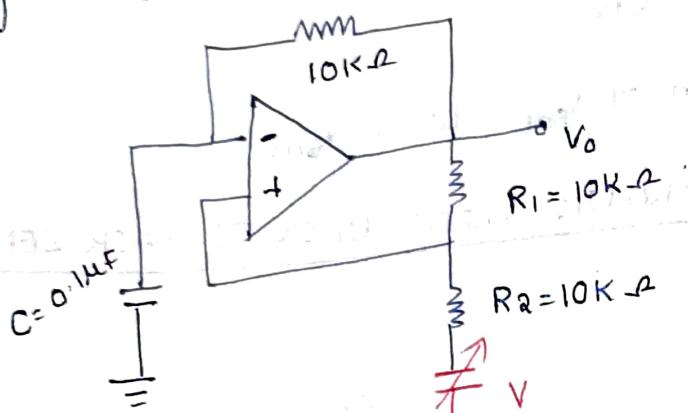


→ wave
a lesser
amplitude
over R_2

Asymmetric square wave can also be generated by using following circuit



Adding DC voltage source V_{in}

series with R_2
can generate Asy. Squ. wave
If V_{in} is varied,
freq. conversion
can be achieved

TRIANGULAR WAVE GENERATOR

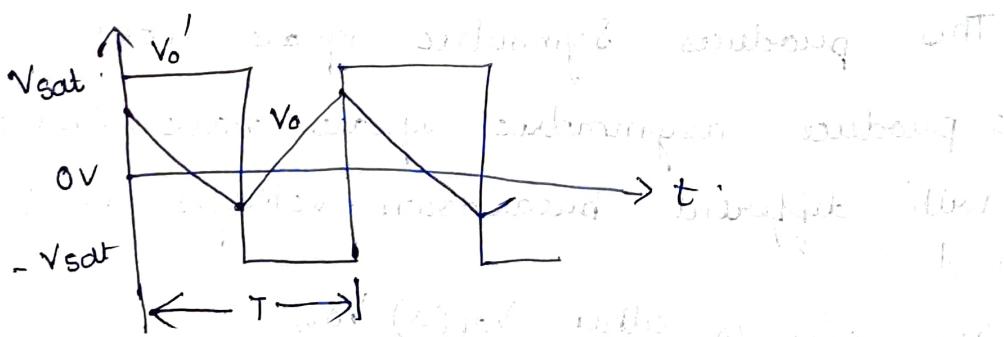
integrating square wave \rightarrow Triangle wave

To generate square wave \rightarrow Astable multivibrator
To generate triangle wave \rightarrow Astable multivibrator + integrator

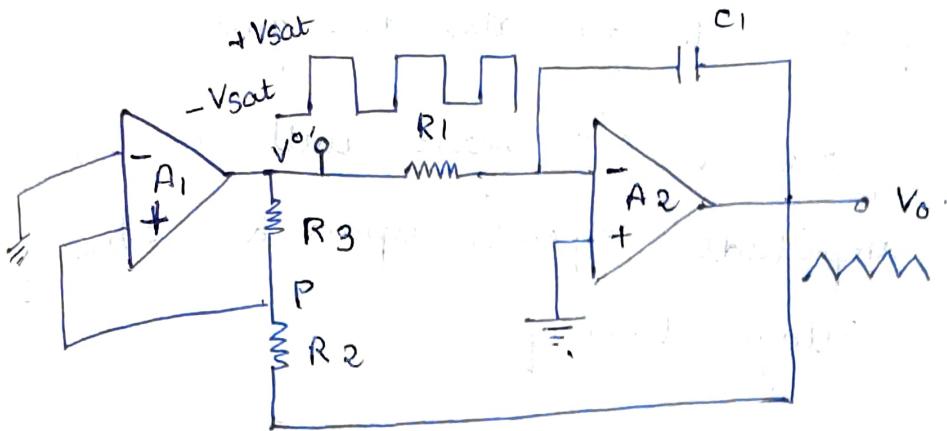
(astable multivibrator + integrator)

(ckt comb of both)

output waveform is as shown below.



Another triangular wave generator with lesser no. of components is shown below.



It consists of two level comparators followed by integrators. O/p of comparator A_1 is square wave of amplitude $\pm V_{sat}$. It is applied to (-) terminal of integrator A_2 produces a triangular wave. This is fed back as i/p to A_1 through voltage divider R_2, R_3 .

$$\text{If } \text{o/p of } A_1 = +V_{sat} \quad \text{ramp} + \text{quint} - \\ \text{o/p of } A_2 = -\text{ve going ramp}$$

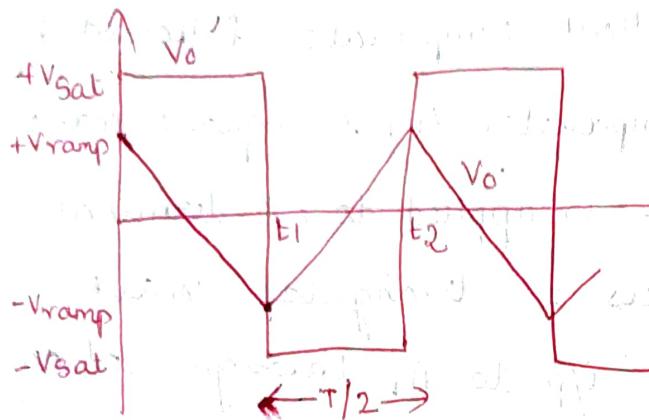
\therefore one end of voltage divider R_2, R_3 is at the voltage $+V_{sat}$ and other at negative going ramp of A_2 .

At $t = t_1$, (negative) ramp attains a value of $-V_{ramp}$. \therefore effective voltage at P becomes less than 0V. This switches o/p of A_1 from +ve saturation to -ve saturation level $-V_{sat}$.

At this time o/p of A_2 increases in +ve direction.

At this instant when $t = t_2$, voltage at $P > 0V$ \therefore o/p of A_1 switches from $-V_{sat}$ to $+V_{sat}$.

cycle repeats and generates triangular waveform
 freq of square & triangle wave will be same.
 however, amplitude depends upon RC value of A₂ & o/p voltage level of A₁.



effective voltage at P when o/p of A₁ is at $+V_{sat}$
 is

$$-V_{ramp} + \frac{R_2}{R_2 + R_3} [+V_{sat} - (-V_{ramp})] = 0 \quad (1)$$

At $t = t_1$, voltage at P becomes equal to zero

∴ from eqn (1)

$$-V_{ramp} = -\frac{R_2}{R_3} (+V_{sat}).$$

Similarly at $t = t_2$, o/p of A₁ switches from $-V_{sat}$ to $+V_{sat}$

$$\therefore V_{ramp} = +\frac{R_2}{R_3} (-V_{sat})$$

$$= \frac{R_2}{R_3} (V_{sat})$$

peak to peak amplitude of Δ^{1st} wave is

$$V_o(PP) = +V_{ramp} - (-V_{ramp}).$$

$$\therefore \frac{2R_2}{R_3} V_{sat}$$

o/p switches from $-V_{ramp}$ to $+V_{ramp}$ in half time period $T/2$. putting values in basic integrator eqn.

$$V_o = -\frac{1}{R_1 C_1} \int V_i dt$$

$$V_o(PP) = -\frac{1}{R_1 C_1} \int (-V_{sat}) dt$$

$$dt = \frac{\pi A}{2} = \left(\frac{\pi A}{2} \right) \frac{T/2}{R_1 C_1} = \frac{V_{sat}}{R_1 C_1} \left(\frac{T}{2} \right)$$

$$\therefore T = 2 R_1 C_1 \cdot \frac{V_o(PP)}{V_{sat}}$$

$$Sub \quad o(PP) = \frac{2R_2}{R_3} V_{sat}$$

$$\therefore T = \frac{4 R_1 C_1 R_2}{R_3}$$

freq of oscillation

$$f_o = \frac{1}{T} = \frac{R_3}{4 R_1 C_1 R_2}$$

$$-V_{ramp} = -\frac{R_2}{R_2+R_3} [V_{sat} + V_{ramp}]$$

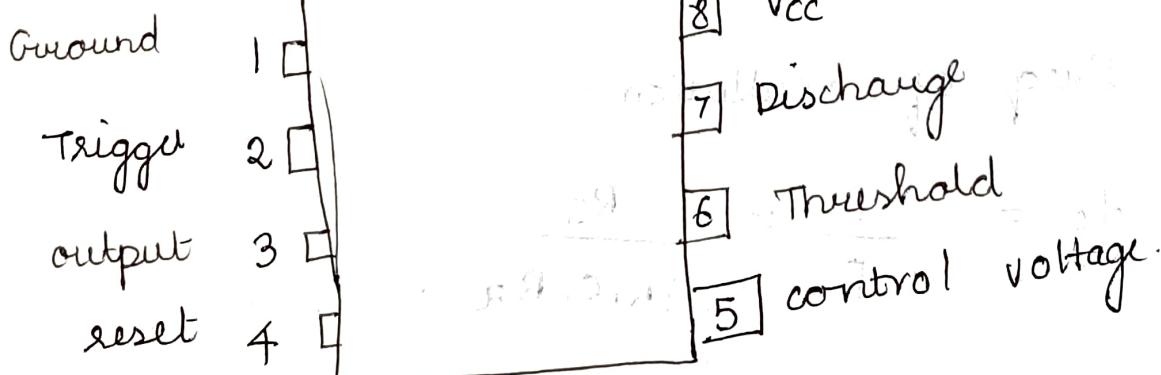
$$-V_{ramp} = -\frac{R_2}{R_2+R_3} V_{sat} - \frac{R_2}{R_2+R_3} V_{ramp}$$

$$V_{ramp} \frac{R_2}{R_2+R_3} - V_{ramp} = -\frac{R_2}{R_2+R_3} V_{sat}$$

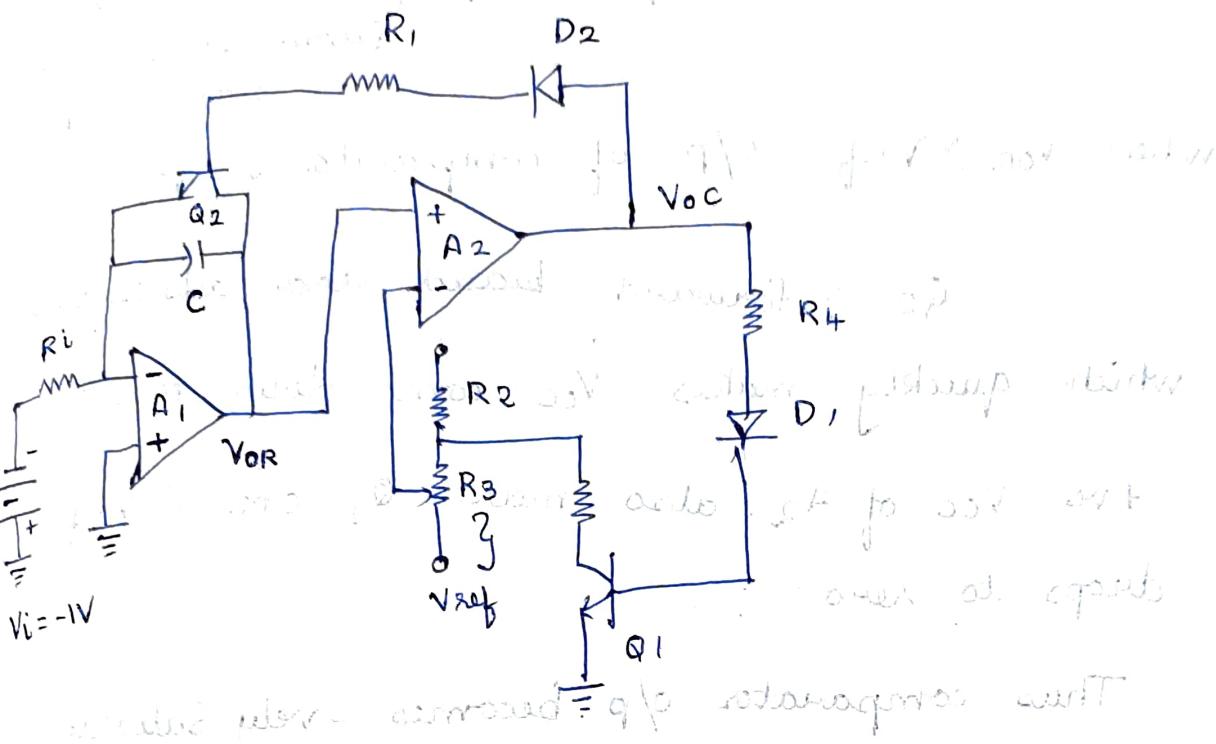
$$V_{ramp} \left(\frac{R_2}{R_2+R_3} - 1 \right) = -\frac{R_2}{R_2+R_3} V_{sat}$$

$$V_{ramp} \left(\frac{R_2 - R_2 - R_3}{R_2+R_3} \right) = -\frac{R_2}{R_2+R_3} V_{sat}$$

$$-V_{ramp} = -\frac{R_2}{R_2+R_3} V_{sat}$$



SAWTOOTH WAVE GENERATOR



sawtooth wave refers to waveform with its rise time being many times longer than fall time

$A_1 \rightarrow$ ramp generator

$A_2 \rightarrow$ comparator

V_i is less than '0' and is connected to inverting input of op amp.

Since $V_i = -ve$, o/p of A_1 ramp up.

o/p V_{OR} of A_1 is connected to non inverting terminal of A_2 . & V_{ref} (reference voltage) set by potentiometer V_{ref} is connected to inverting i/p of A_2

When $V_{OR} < V_{ref}$, o/p of comparator is -ve.

Q_1 & Q_2 do not conduct.

diodes D_1 and D_2 protect transistor from excessive reverse bias voltage.

when $V_{OR} > V_{ref}$, o/p of comparator is +ve.

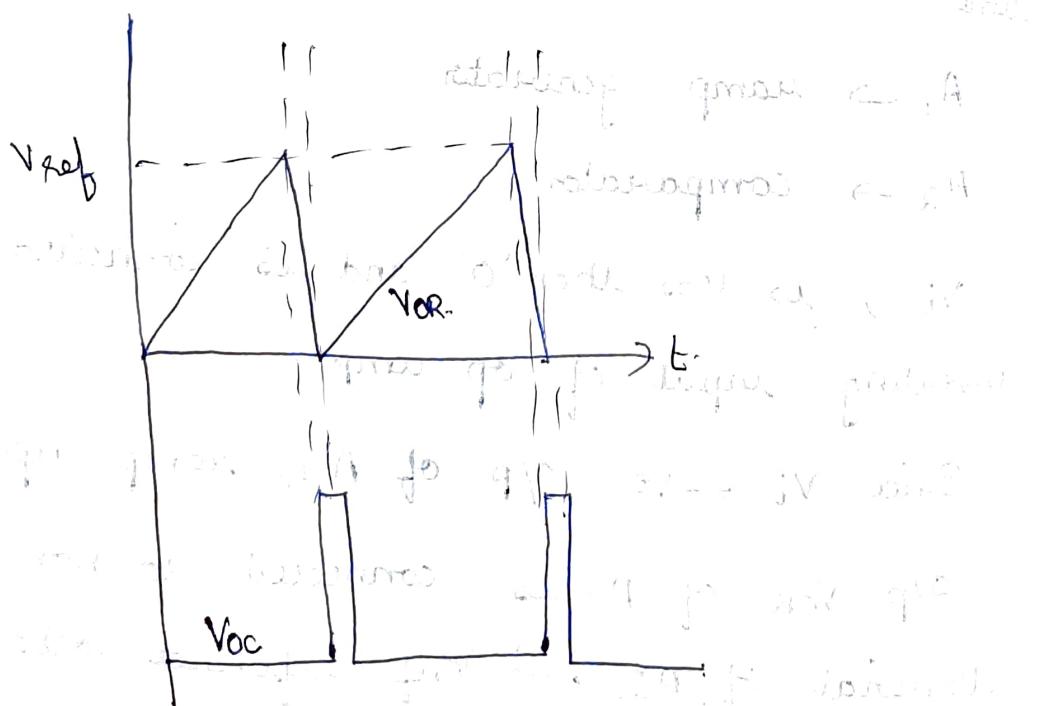
$Q_2 \rightarrow$ forward biased and acts as sink.

which quickly makes V_{oc} come down to 0V.

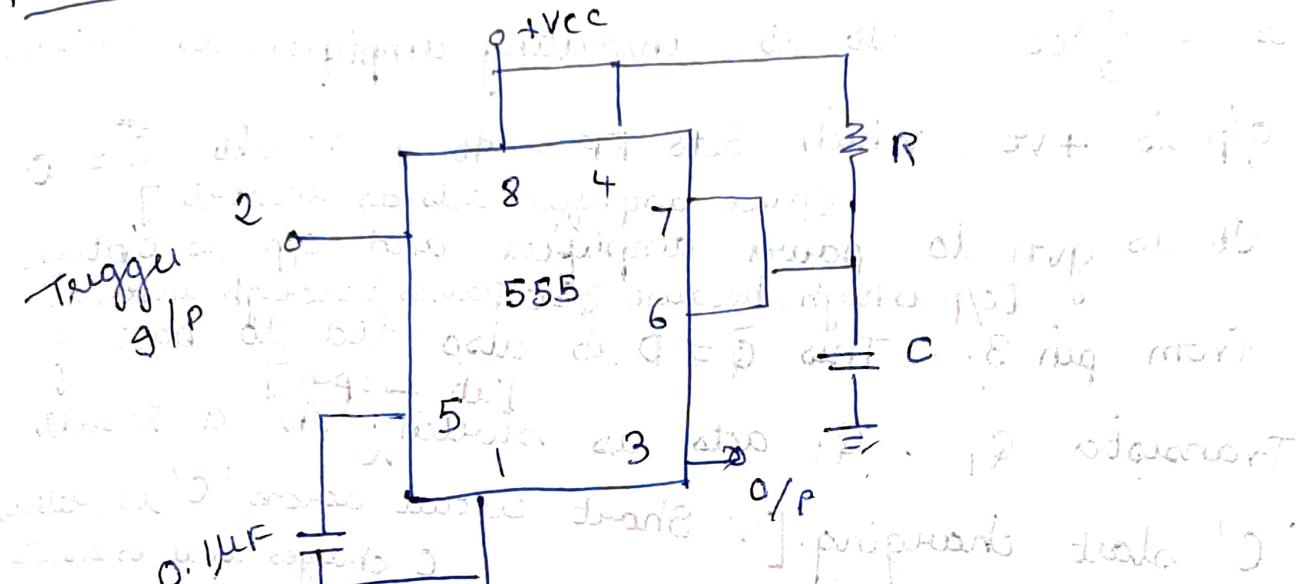
+ve V_{oc} of A_2 also makes Q_1 ON & V_{ref} drops to zero.

Thus comparator o/p becomes -vely saturated.

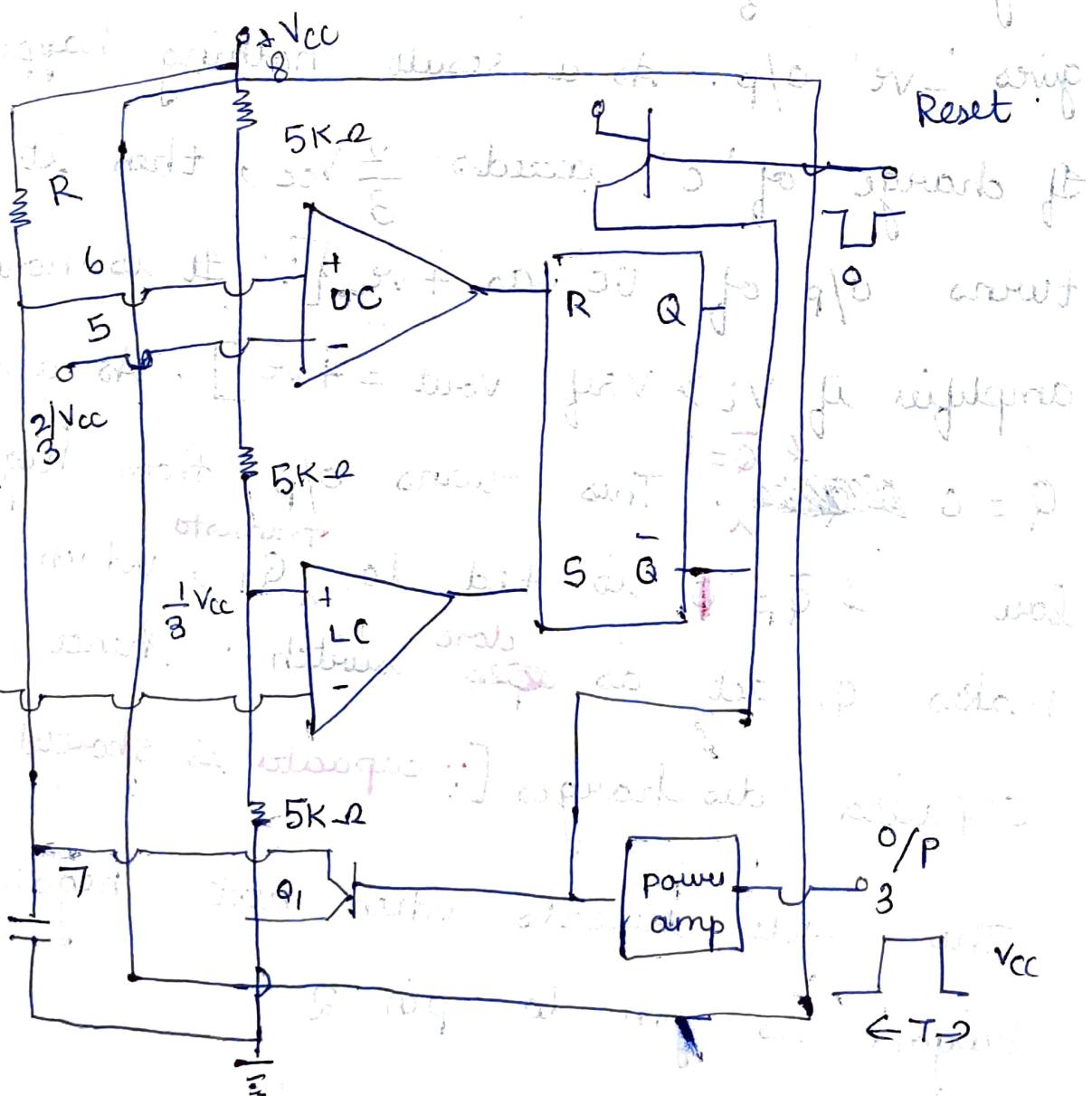
This switches off Q_2 OFF & C begins charging linearly & cycle repeats.



MONOSTABLE OPERATION



Monostable multivibrator circuit diagram



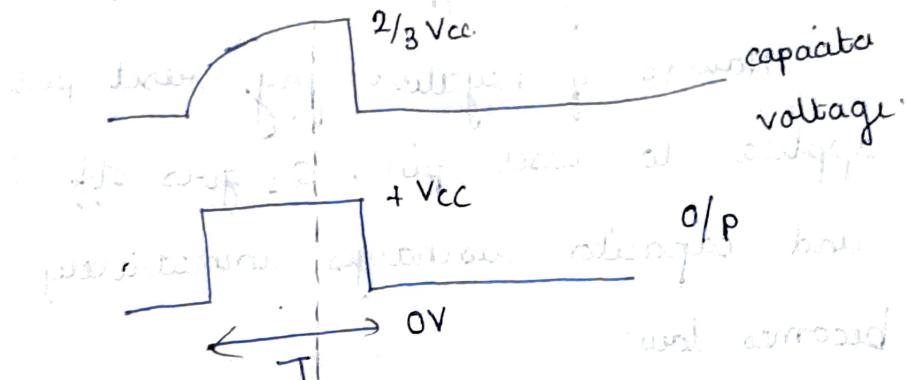
Negative trigger is given as i/p to LC. Its value is $< \frac{1}{3} V_{cc}$. It is inverting amplifier as a result $\bar{Q} = 0$. O/p is +ve, which sets FF. As a result [power amplifier acts as inverter] it is given to power amplifier and o/p is obtained from pin 3. This $\bar{Q} = 0$ is also fed to base of Transistor Q_1 . Q_1 acts as switch. As a result 'C' starts charging. [it is open] Short circuit across 'C' is released. C charges as it is connected to $+V_{cc}$.

Any value $< \frac{2}{3} V_{cc}$ fed to upper comparator gives '-ve' o/p. As a result nothing happens if charge of 'C' exceeds $\frac{2}{3} V_{cc}$, then it turns o/p of V_C as +ve. [It is noninverting amplifier if $V_i > V_{ref}$ $v_{out} = +ve$]. As a result $Q = 0$ & $\bar{Q} = 1$. This turns o/p from high to low. & $\bar{Q} = 0$ is fed to Q_1 , which makes Q_1 act as close switch. hence capacitor discharges. [capacitor is shorted by Q_1]

The cycle repeats when next negative trigger is given to pin 2.

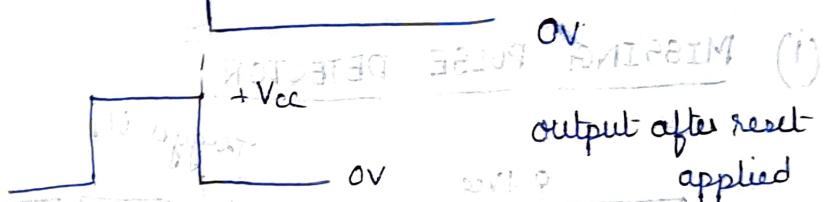
The output wave will be as shown below

Trigger



Reset

[EQUATION 199A]



voltage across the capacitor

$$V_C = V_{CC} \left(1 - e^{-t/RC} \right)$$

At $t = T$;

$$\frac{2}{3} V_{CC} = V_C$$

$$\frac{2}{3} V_{CC} = V_{CC} \left(1 - e^{-T/RC} \right)$$

$$\frac{2}{3} = 1 - e^{-T/RC}$$

$$e^{-T/RC} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$-T/RC = \ln(1/3)$$

$$-T = RC \ln(1/3)$$

$$T = RC \ln(3)$$

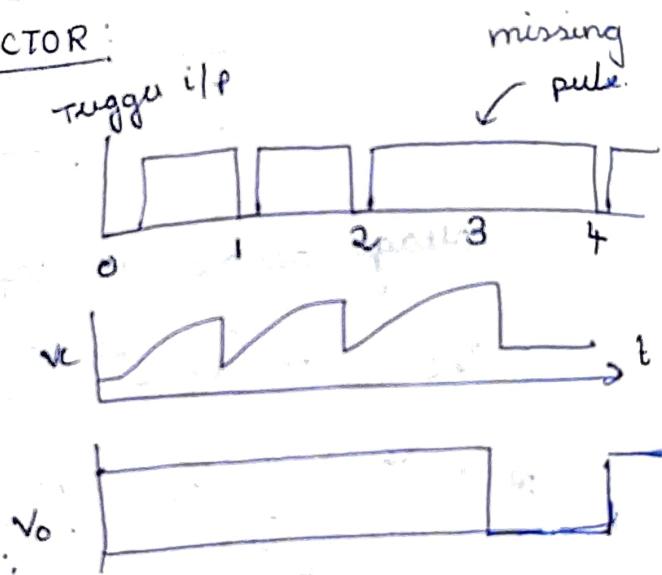
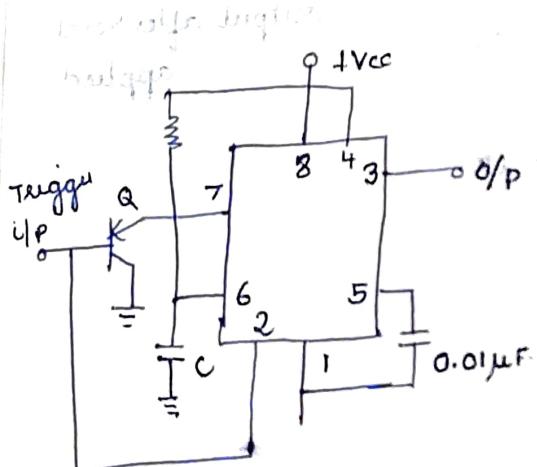
$$\boxed{T = 1.1 RC}$$

o/p remains high until T elapses, which depends on R and C . Any additional trigger will not change o/p state.

However if negative going reset pulse is applied to reset pin, Q_2 goes off & Q_1 on and capacitor discharges immediately & o/p becomes low.

APPLICATIONS

(1) MISSING PULSE DETECTOR



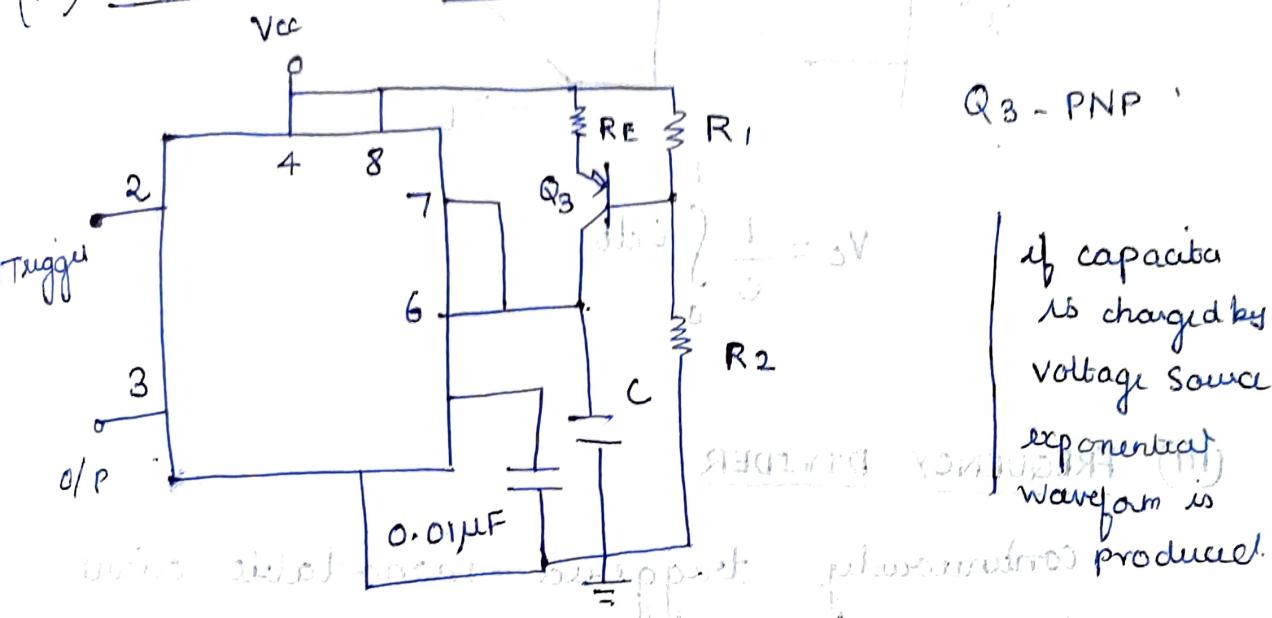
It detects a missing pulse or abnormally long period between two pulses in train of pulses.

When i/p (trigger) goes low, it turns on a transistor which quickly drains the capacitor. When i/p trigger goes high, capacitor recharges but doesn't quite make it to the threshold voltage before the i/p goes low again.

If S/P stays high capacitor is allowed to charge fully and 555 timing interval ends, bringing O/P low.

Application: used to detect missing heartbeat

(ii) LINEAR RAMP GENERATOR:



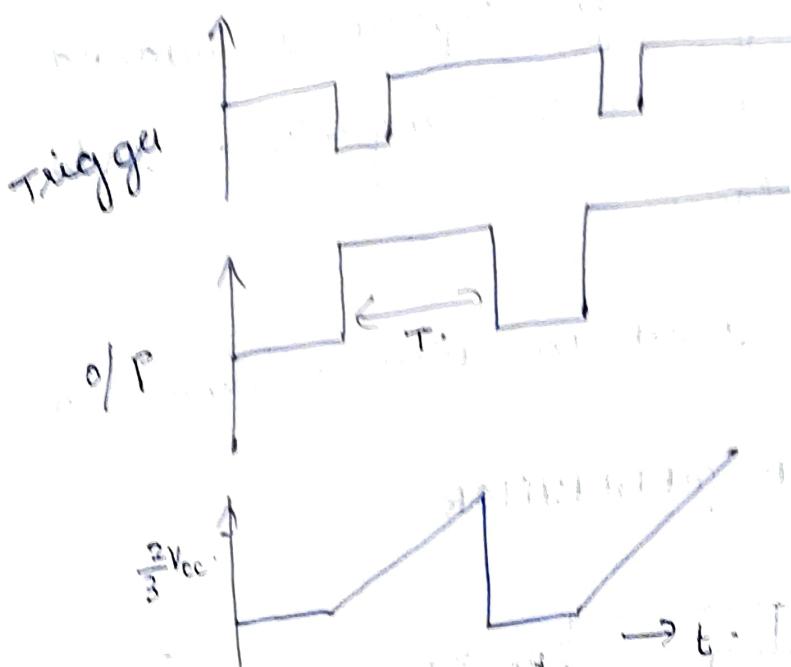
Q₃ - PNP

If capacitor is charged by voltage source exponential waveform is produced.

When trigger starts, constant current source produces a ramp. This is fed behind the circuit.

When trigger starts, PNP current source forces constant charging into the capacitor C. When voltage across the capacitor reaches $\frac{2}{3} V_{cc}$, the upper comparator triggers.

Capacitor discharges as soon as its voltage reaches $\frac{2}{3} V_{cc}$ which is threshold of upper comparator in monostable circuit. Capacitor voltage remains zero till another trigger is applied.



$$V_c = \frac{1}{C} \int_0^t i dt$$

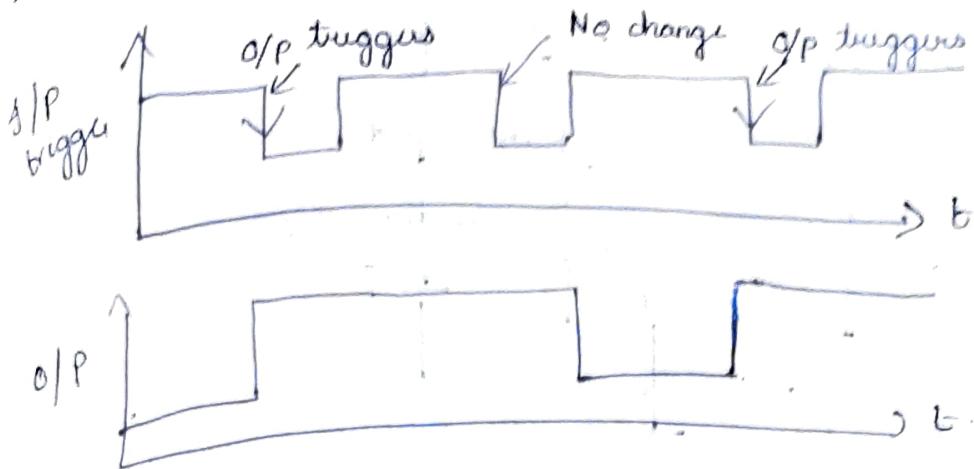
(iii) FREQUENCY DIVIDER

continuously triggered monostable circuit when triggered by square wave generator can be used as frequency divider. If timing interval is adjusted to be longer than period of triggering square wave input signal.

Monostable multivibrator will be triggered by first negative going edge of square wave if o/p remains high (because of greater timing interval) for next -ve going edge of i/p square wave.

o/p triggers again on third negative going input, depending on choice of time delay.

In this way, o/p can be made integral fractions of the frequency of i/p triggering square wave.



(iv) PULSE WIDTH MODULATION

modulating i/p is applied at pin 5.

continuous trigger is applied at pin 2.

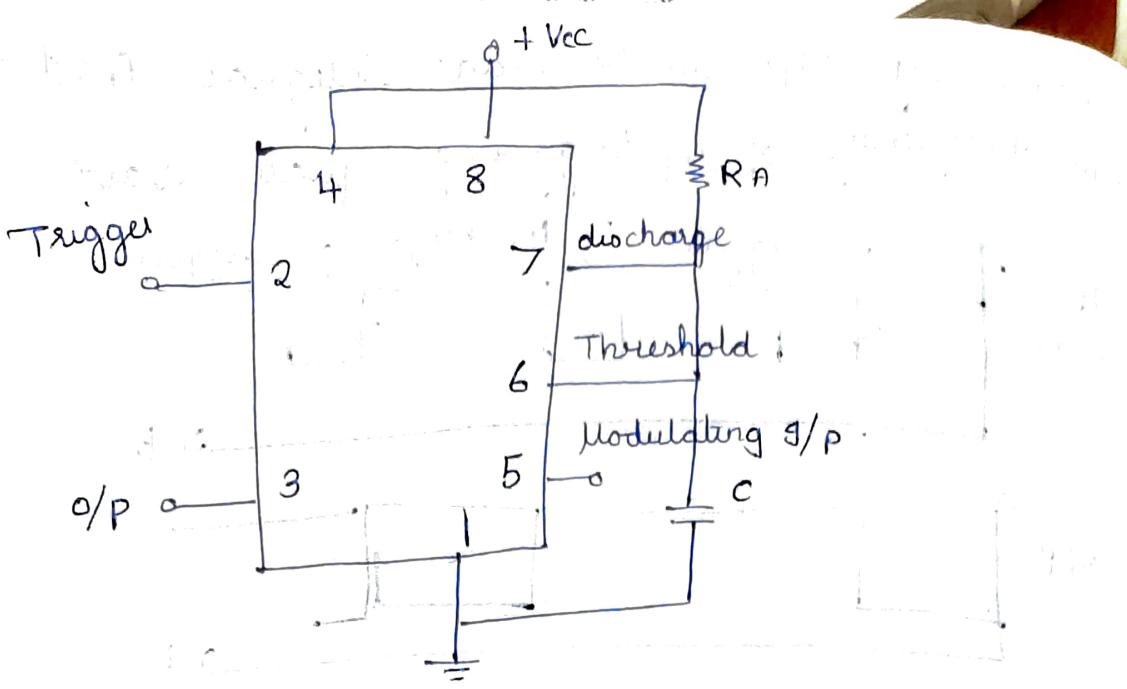
o/p is obtained from pin 3, the duration of which depends on modulating i/p.

modulating i/p at pin 5 gets superimposed upon already existing $\left(\frac{2}{3}\right)V_{cc}$ at inverting i/p of UC.

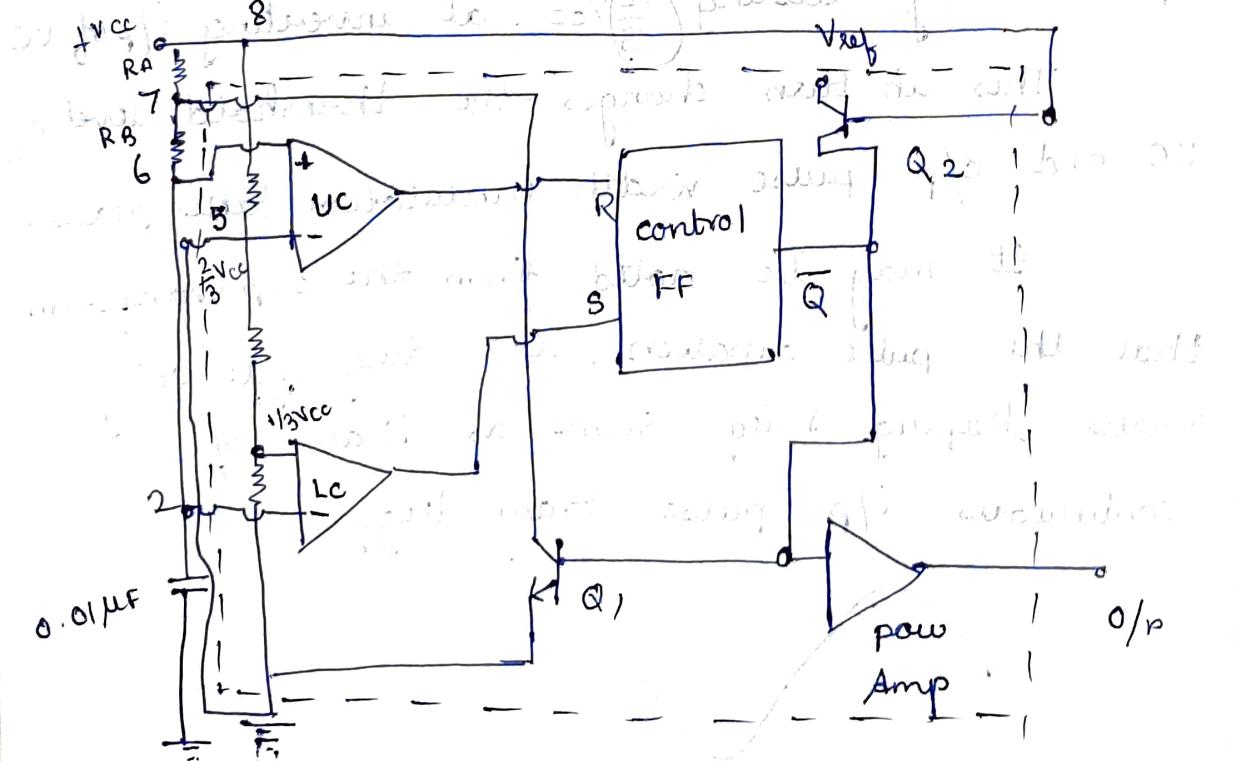
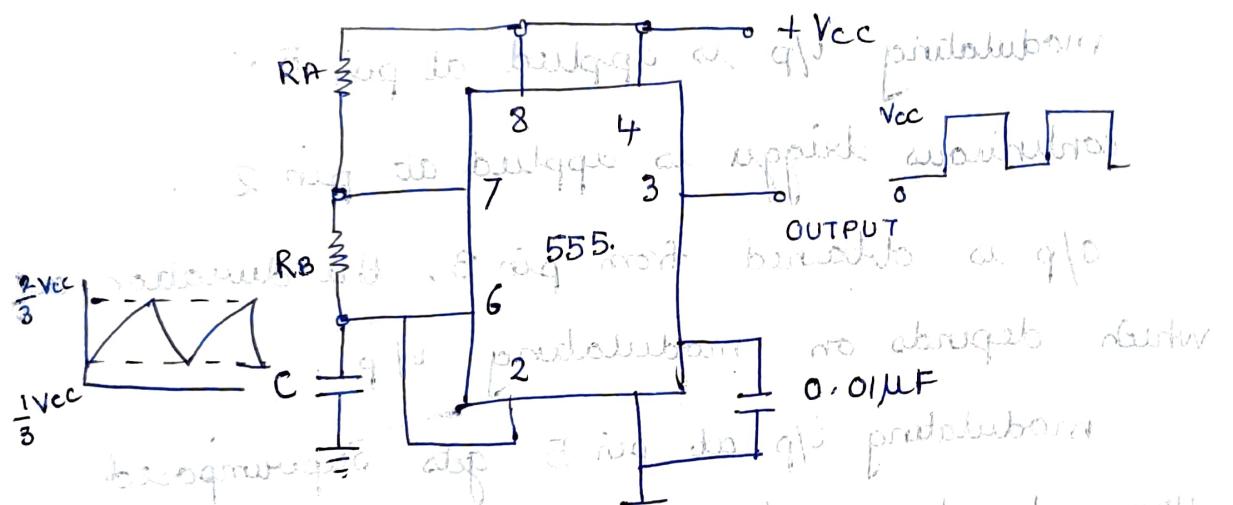
This in turn changes the threshold level of UC and o/p pulse width modulation takes place.

It may be noted from the o/p waveform that the pulse duration, i.e. duty cycle only varies, keeping freq same as that of continuous i/p pulse train trigger.





ASTABLE OPERATION



Timing resistor is split into two sections R_A and R_B .
 discharging transistor Q_1 is connected to junction of
 R_A and R_B .

When the power supply V_{cc} is connected, external
 capacitor C charges towards V_{cc} with time constant

$$(R_A + R_B)C$$

during this time, output is high (equals V_{cc})
 as reset $R = 0$, set $S = 1$ & this combination makes

$$\bar{Q} = 0$$

when capacitor voltage equals $(\frac{2}{3})V_{cc}$, the upper
 comparator triggers F.F. $\boxed{\bar{Q} = 1 \text{ if } \bar{Q} = 0}$

$\because V_{in} > V_{ref}$; for +ve comp, $V_{out} = +ve$
 Resets, $\bar{Q} = 0$ $\boxed{\bar{Q} = 1}$

$$o/p = 0 \quad [\text{at pin 3}]$$

This makes Q_1 on and C discharges

during discharge of capacitor C , as it reaches
 less than $\frac{1}{3}V_{cc}$, lower comparator is triggered
 and at this stage $S = 1$, $R = 0$ which turns $\bar{Q} = 0$

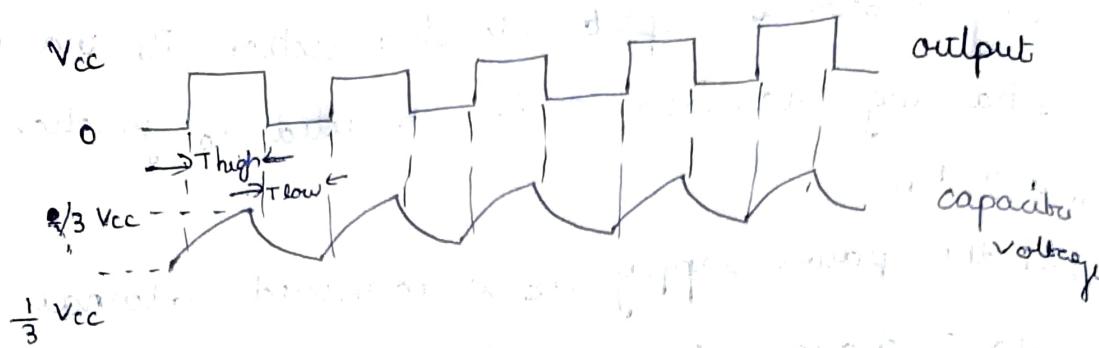
Now Q_1 - OFF & C charges.

$L \cdot C \quad V_{in} < \frac{1}{3}V_{cc}$; for -ve comp

$$V_{out} = +ve$$

$$S = 1; \bar{Q} = 0; Q = 1$$

Thus capacitor is periodically charged & discharged
 b/w $\frac{2}{3}V_{cc}$ & $\frac{1}{3}V_{cc}$



capacitor voltage is given by

$$V_C = V_{CC} \left(1 - e^{-t/RC} \right)$$

At t_1 , capacitor charge from 0 to $(2/3)V_{CC}$

$$\frac{2}{3}V_{CC} = V_{CC} \left(1 - e^{-t_1/RC} \right)$$

$$t_1 = 1.09 RC$$

At t_2 , capacitor charge from 0 to $(1/3)V_{CC}$

$$\frac{1}{3}V_{CC} = V_{CC} \left(1 - e^{-t_2/RC} \right)$$

$$t_2 = 0.405 RC$$

$$[t_2 - t_1] = 0.69 RC$$

time to charge from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$ is

$$t_{HIGH} = t_1 - t_2$$

$$= 1.09 RC - 0.405 RC$$

$$= 0.69 RC$$

for given circuit

$$t_{HIGH} = 0.69(R_A + R_B)C$$

O/p is low when capacitor discharges from $(2/3)V_{CC}$ to $(1/3)V_{CC}$. Therefore voltage across

capacitor is given by

$$\frac{1}{3} V_{cc} = \frac{2}{3} V_{cc} e^{-t/RC}$$

$$t = 0.69 RC$$

$$t_{low} = 0.69 R_B C$$

$$\text{Total time} = t_{HIGH} + t_{low}$$

$$= 0.69 (R_A + 2R_B) C$$

$$\therefore f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B) C}$$

approximate values for standard 555 timer

Duty cycle:

Duty cycle is defined as ratio of ON time

$$\text{to total time period } T = \frac{t_{ON}}{T} = \frac{t_{low}}{(R_B C + R_A C)}$$

$$\text{D}\% = \frac{t_{low}}{T} \times 100$$

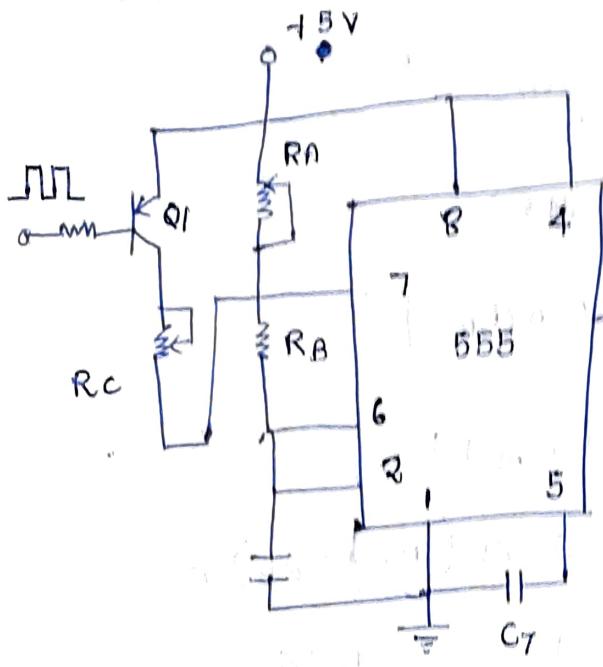
$$= \frac{R_B}{R_A + 2R_B} \times 100$$

$$= \frac{RB}{(RA + RB)} \times 100$$

APPLICATIONS

i) FSK Generator

A 555 timer in astable mode can be used to generate FSK signal. The circuit is shown below.



$Q_1 = \text{PNP}$
Transistor

when input is high, Q_1 is off and 555 timer works in normal astable mode of operation.

freq of o/p waveform is given by $f_o = \frac{1.45}{(R_A + 2R_B)C}$

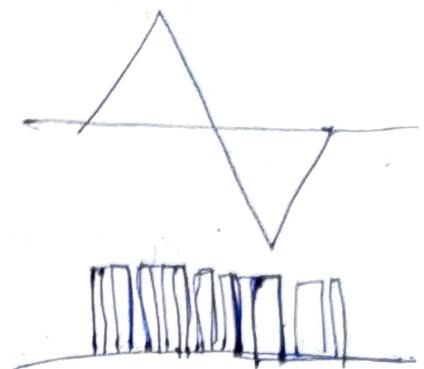
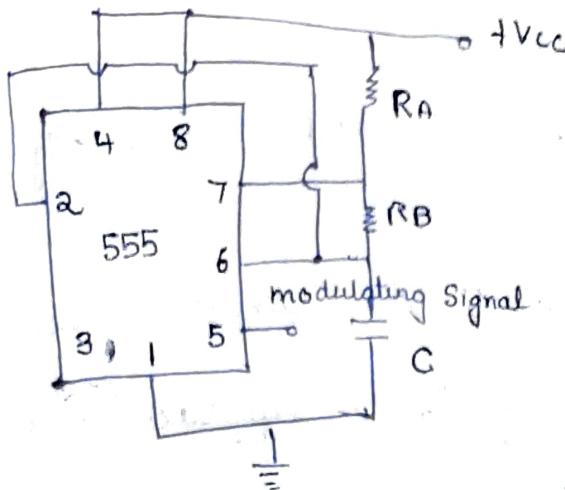
when i/p is low, Q_1 is ON & connects R_C across R_A . The o/p freq is now given by

$$f_o = \frac{1.45}{(R_A || R_C) + 2R_B}$$

FSK is one of modulation scheme which is used to transmit digital data using high freq carrier signal. bit 1 is transmitted using one carrier signal and bit 0 is transmitted using another carrier signal.

carrier freq is switched between two frequencies according to binary i/p

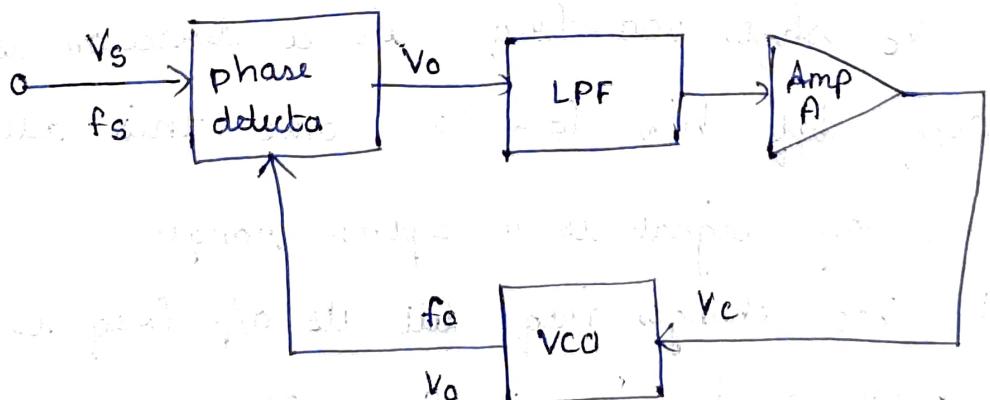
PULSE POSITION MODULATOR



- (i) here modulating signal is Δ^{tar} wave. It is applied to pin 5 of 555 timer
- (ii) o/p pulse position varies with modulating signal, since the threshold voltage and hence the time delay is varied.

PHASE LOCKED LOOP

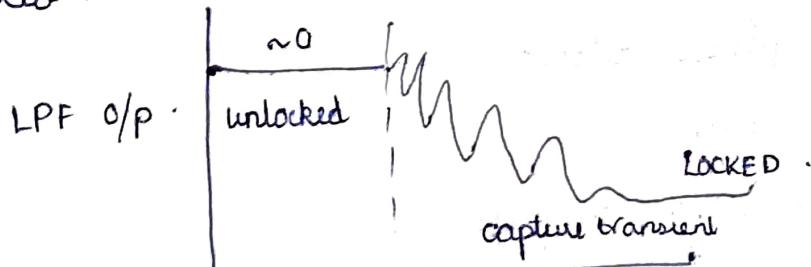
OPERATION OF BASIC PLL



The S/m consists of

- (i) phase detector
- (ii) LPF
- (iii) error Amplifier
- (iv) VCO (voltage controlled osc)

- (i) VCO operates at set frequency f_0 called free running freq. The freq is determined by external capacitor & resistor.
- (ii) It can be shifted to either side by applying dc control voltage V_c .
freq deviation \propto dc control voltage.
- (iii) If i/p sigl of freq f_s is applied to PLL, the phase detector compares phase & freq of incoming sigl to output V_o of VCO.
- (iv) If signals differ in frequency / phase, error voltage V_e is generated.
- (v) phase detector is basically a multiplier & produces the sum ($f_s + f_0$) & difference ($f_s - f_0$) at its o/p.
- (vi) high freq component ($f_s + f_0$) is removed by LPF & difference component is amplified and then applied as control voltage V_c to VCO.
- (vii) V_c shifts VCO freq in a direction to reduce freq diff b/w f_s & f_0 , once this action starts we say signal is in capture range.
- (viii) VCO changes freq till its o/p freq is exactly same as i/p signal freq. Then circuit is said to be locked.



(ix) As capture starts small sine wave appears.
This is due to difference freq b/w VCO & S/P
sgnl.

Each successive cycle causes VCO frequency to
move closer to S/P signal freq.

If VCO freq is far away, the beat freq
will be too high to pass through the filter. Hence
PLL will not respond.

lock in range:

range of freq over which PLL can
maintain lock with the incoming signal

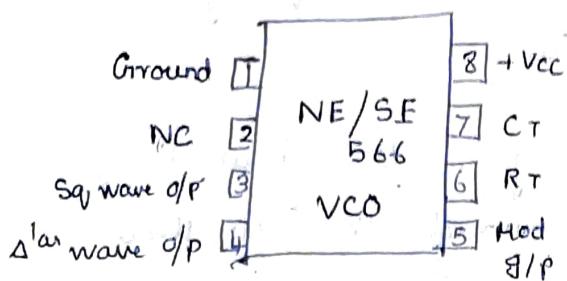
capture range

The range of frequencies over which PLL
can acquire lock with an input Sgnl.

pull-in time

The total time taken by PLL to establish
lock is called pull-in time

VOLTAGE CONTROLLED OSCILLATOR



VCO is type of oscillator where freq of output oscillation can be varied by varying amplitude of g/p voltage. Hence freq is set by external Resistor & cap & then varied by dc voltage.

C_T is linearly charged or discharged by constant current source/sink.

Amount of current can be controlled by changing V_C applied at pin 5 or by changing R_T [pin 6]. External to IC chip voltage at pin 6 is held at same voltage as

pin 5. Thus if modulating i/p at 5 is ↑, voltage at pin 6 also ↑, resulting in less current across R_T thereby ↓ the charging current. VCO's is commonly used in converting low freq signals such as EEGs, EKGs into audio freq range.

voltage across C_T is applied to inverting g/p of Schmitt trigger A_2 via buffer Amplifier A_1 . o/p voltage of Schmitt trigger is designed to swing ~~between~~ to V_{CC} & $0.5 V_{CC}$

If $R_a = R_b$, voltage at non inverting terminal of A_2 swings from $0.5 V_{CC}$ to $0.25 V_{CC}$

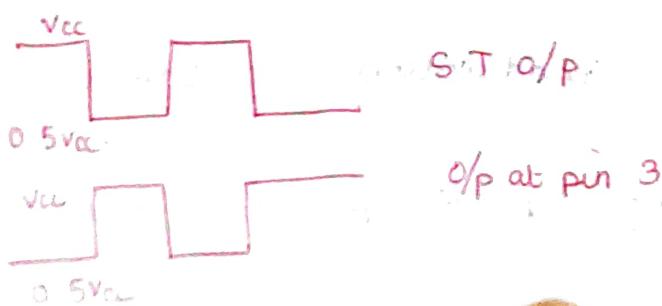
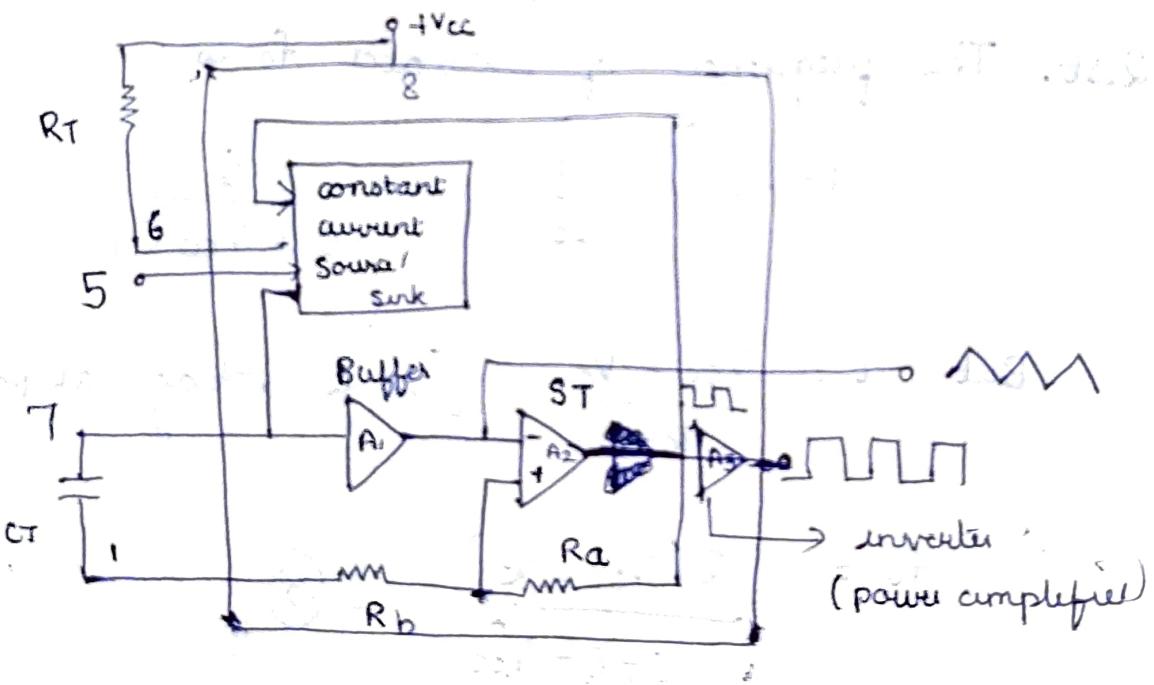
when voltage on capacitor C_T exceeds $0.5V_{CC}$
during charging o/p of schmitt trigger goes low
($0.5V_{CC}$)

capacitor now discharges & when it is at
 $0.25V_{CC}$, o/p of schmitt trigger goes high.

Since source & sink currents are equal,
capacitor charges & discharges for same amount of time.

This gives rectangular voltage waveform
across C_T [pin 4] which is available at

The square wave o/p of S.T is inverted
by inverter A3 & is available at pin 3 of ST



OUTPUT FREQUENCY OF VCO

$$i \Delta t = C_T \Delta V$$

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_T} \quad \text{--- (1)}$$

$$\begin{aligned} i &= q/t \\ V &= C_V \\ it &= C_V \end{aligned}$$

The total voltage on capacitor changes from $0.25 V_{cc}$ to $0.5 V_{cc}$

$$\therefore \Delta V = 0.5 V_{cc} - 0.25 V_{cc}$$

$$\boxed{\Delta V = 0.25 V_{cc}} \quad \text{Sub in (1)}$$

$$\frac{0.25 V_{cc}}{\Delta t} = \frac{i}{C_T}, \quad \Delta t = \frac{0.25 V_{cc} C_T}{i} \quad \text{--- (2)}$$

The Time period T of the Δ waveform = $2\Delta t$. The frequency of oscillation f_0 is

$$f_0 = \frac{1}{T} = \frac{1}{2\Delta t} \quad \boxed{T = \frac{1 \cdot i}{0.5 V_{cc} C_T}}$$

$$\text{But } i = \frac{V_{cc} - V_c}{R_T} \quad [V_c \text{ is voltage at pin 5}]$$

$$f_0 = \frac{2(V_{cc} - V_c)}{C_T R_T V_{cc}} \quad \text{--- (3)}$$

The output freq of vco can be changed by

(i) R_T

(ii) C_T

(iii) V_c at modulating i/p terminal 5.

If modulating i/p at pin 5 is biased at

$$\left(\frac{7}{8}\right)V_{cc}$$

then

$$f_0 = \frac{2(V_{cc} - (7/8)V_{cc})}{C_T R_T V_{cc}} = \frac{V_{cc}/4}{C_T R_T V_{cc}}$$

$$\Rightarrow \frac{1}{4 R_T C_T} = 0.25$$

(4)

voltage to frequency conversion factor

Important parameter for V_{cc} is voltage to frequency conversion & is defined as

$$K_V = \frac{\Delta f_0}{\Delta V_C} ; \Delta V_C \rightarrow \text{modulation voltage required to produce frequency shift } \Delta f_0$$

Let original freq = f_0 & new freq = f_1

$$\Delta f_0 = f_1 - f_0$$

: duplo percept

$$\text{new freq} = \frac{2(V_{cc} - V_C + \Delta V_C)}{C_T R_T V_{cc}} - f_0 \frac{2(V_{cc} - V_C)}{C_T R_T V_{cc}}$$

$$= 2 \Delta V_C$$

$$\therefore \Delta V_C = \frac{\Delta f_0 C_T R_T V_{cc}}{2} - (6)$$

Sub $C_T R_T$ from (4)

$$\Delta V_C = \frac{\Delta f_0 (0.25) V_{cc}}{2}$$

$$K_V = \frac{\Delta f_0}{\Delta V_C} = \frac{2 f_0}{0.25 V_{cc}} = \frac{2 f_0}{(\frac{1}{4}) V_{cc}} = \frac{8 f_0}{V_{cc}}$$

PLL APPLICATIONS

O/p of PLL system can either be

(i) voltage signal $V_c(t)$ corresponding to error voltage

(ii) frequency signal at VCO output

voltage output used in frequency discriminator application

frequency output used in Signal conditioning

frequency Synthesis or clock recovery

voltage output

when PLL is locked to input freq,

error voltage $V_c(t) \propto (f_s - f_o)$

If f_s is varied, V_c will also vary to maintain lock

$$\omega_t - \omega_o = \omega_d$$

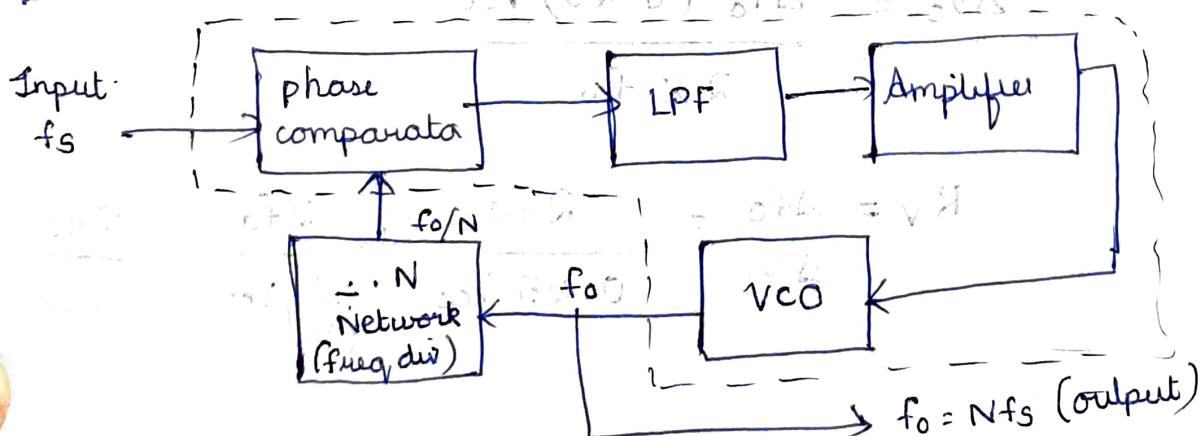
Frequency output:

($f_s - \omega_o$) SAW - filter signal - comprises of many

frequencies (including noise & other disturbances), the PLL can be made to lock to particular frequency

The output of VCO would regenerate that particular frequency & attenuate other freq. Thus used for regenerating or reconditioning desired frequency Sgnl. out of many undesirable freq.

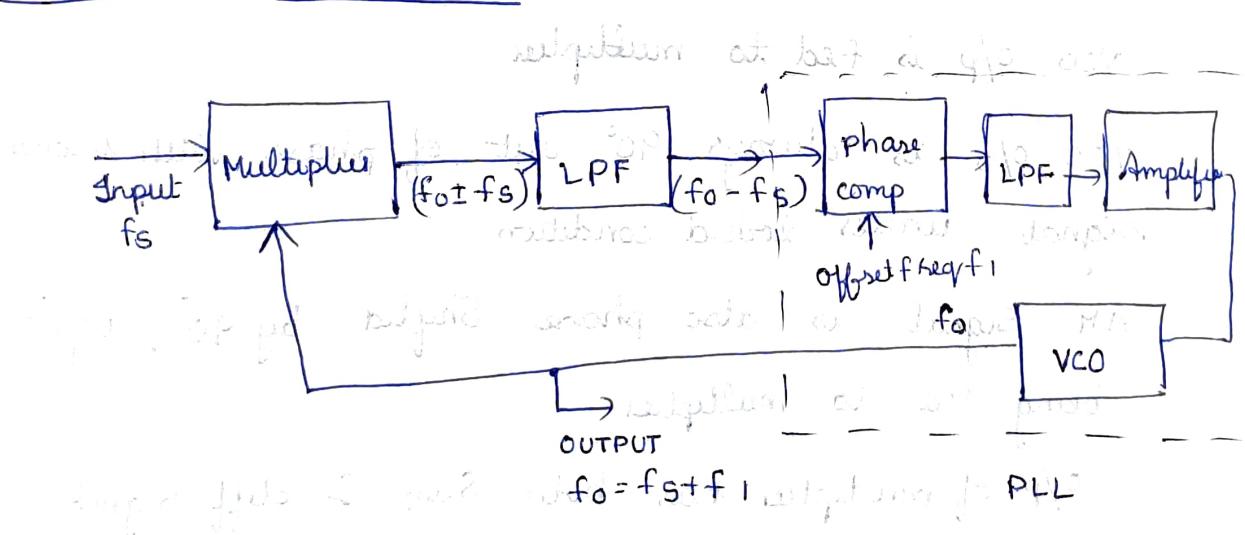
FREQUENCY MULTIPLICATION / DIVISION.



- i) frequency divider is inserted between o/p of vco & phase comparator so that loop signal to pc is f_o while o/p of vco is Nf_o .
- ii) o/p is multiple of input frequency as long as the loop is in lock.
- iii) desired amount of multiplication can be obtained by selecting proper divide by N n/w where N is integer.
- iv) freq multiplication can also be obtained using PLL in harmonic locking mode.
- v) if g/p signal is such in harmonics, VCO can be directly locked to n^{th} harmonic of i/p signal without connecting any frequency divider in between.
- vi) effective locking may not take place, if amplitude of high order harmonics are less than 10%.

FREQUENCY TRANSLATION

as specified above and given



- Multiplexer & LPF is connected externally to PLL.
- Signal f_s which has been shifted & o/p freq f_o of the VCO are applied as g/p to mixer.

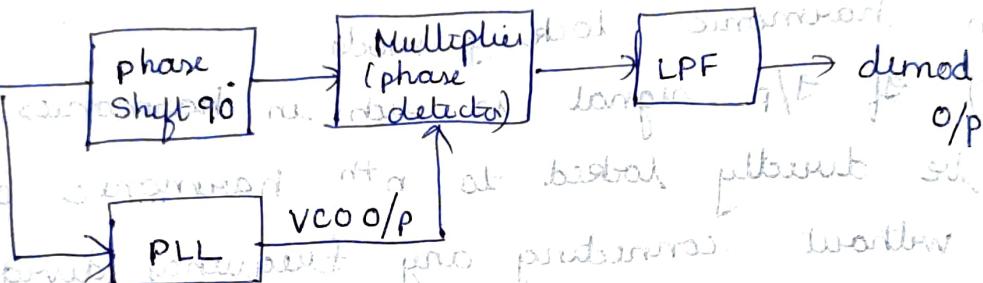
- (III) o/p of mixer contains sum & diff of f_s & f_o
- (IV) o/p of LPF contains only difference signal ($f_o - f_s$)
- (V) Translation or offset freq. is applied to PC.

when PLL is in lock state

$$f_o - f_s = f_1$$

$$f_o = f_s + f_{\text{offset}}$$

AM DETECTION



PLL is used to demodulate AM Signal

VCO has same freq as carrier but it is unmodulated

VCO o/p is fed to multiplier

VCO o/p is always 90° out of phase with incoming signal under locked condition

AM Signal is also phase shifted by 90° , before being fed to multiplier

O/p of multiplier has both sum & diff signals, demodulated o/p is obtained after filtering high freq. sigl. by LPF and rectifying it

Since PLL responds only to carrier freq., it exhibits high degree of selectivity & noise immunity

Demodulation

if PLL is locked to FM signal- vco tracks instantaneous frequency of I/p signal . The filtered error voltage which controls vco & maintains lock with i/p signal is demodulated FM o/p .

FSK demodulator binary data can be retrieved using FSK demod.
As signal appears at I/p , the loop locks ^{at receive} _{2nd} to i/p freq & tracks it b/w two freq corresponding to dc shift at o/p .

Three stage filter removes carrier component and o/p signal is made logic compatible by comparators.

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OSCILLATORS

To build oscillator, we use amplifier with +ve f/b. The idea is to use f/b signal in phase with input signal.

for +ve f/b

$$A_{fb} = \frac{A}{1 - AB} \quad \text{when } AB = 1 ; \quad A_{fb} = \infty = \frac{V_o}{V_i}$$

This will happen when $V_i = 0$.

This is when we get o/p wth out an i/p. This is called oscillator.