SRM Institute of Science and Technology
College of Engineering and Technology

SET A

DEPARTMENT OF ECE

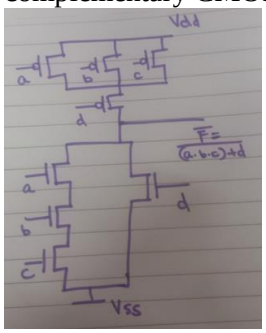
SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

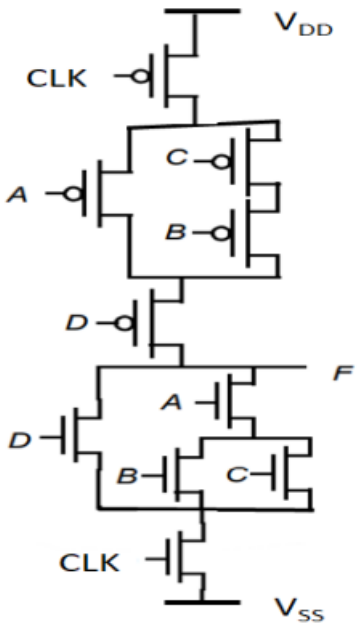
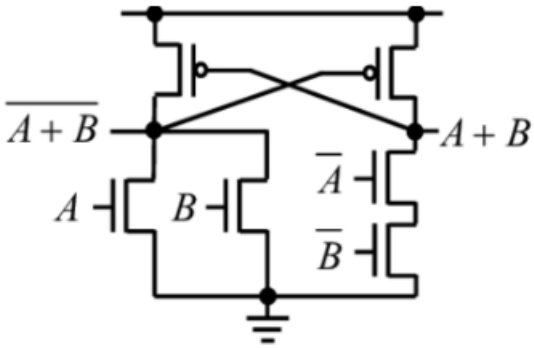
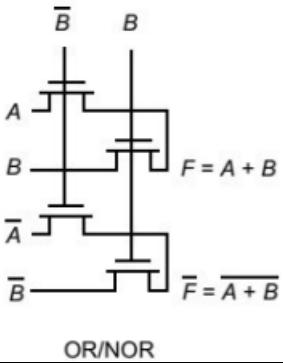
Academic Year: 2022-2023 (EVEN)

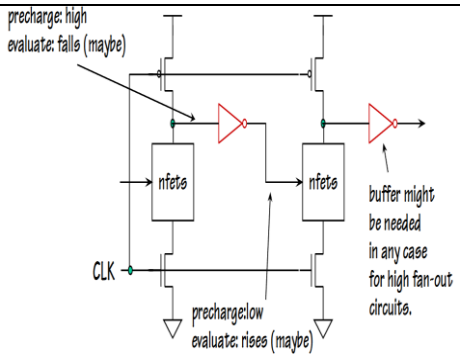
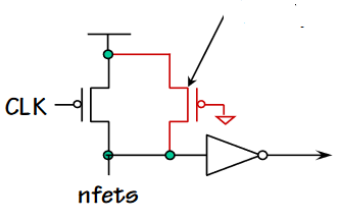
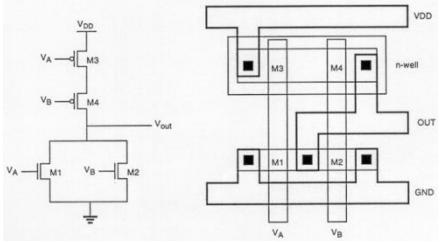
Test: CLAT- 3 **Date:** 02.05.2023
Course Code & Title: 18ECC206J - VLSI Design **Time:** 8.00 to 9.40 AM
Year & Sem: III & VI **Max. Marks:** 50

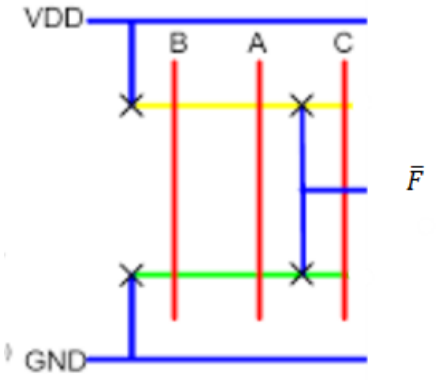
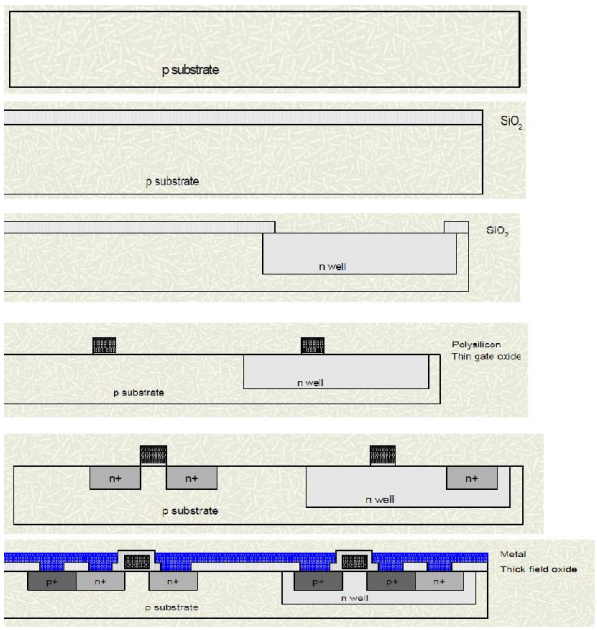
Course Articulation Matrix:

18ECC206J - VLSI Design		Program Learning Outcomes (POs)														
		Graduate Attributes												PSO		
S. No.	Course Outcomes (COs)	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
1	Design and implement digital circuits using Verilog HDL to simulate and verify the designs.	-	3	3	-	3	-	-	-	-	-	-	-	2	-	-
2	Design general VLSI system components, adder cells and multipliers to address the design of data path subsystem.	-	3	3	-	3	-	-	-	-	-	-	-	2	-	-
3	Examine the characteristics of MOS transistors	3	2	-	-	-	-	-	-	-	-	-	-	2	-	-
4	Analyze CMOS inverter and other complex logic gates designed using different logic styles	-	2	2	-	-	-	-	-	-	-	-	-	2	-	-
5	Explain how the transistors are built, and understand the physical implementation of circuits.	-	1	1	-	-	-	-	-	-	-	-	-	2	-	-

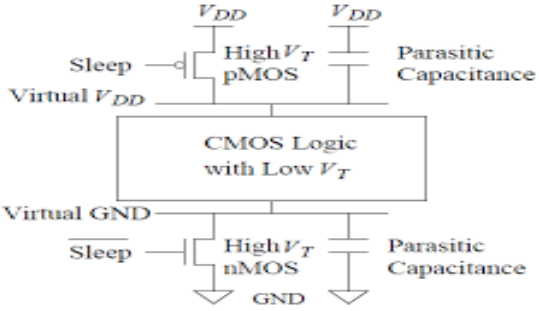
	Answer any 5 Five Questions				
Q.No	Question	Marks	BL	CO	PO
1a	If nMOS-transistor conducts and has large voltage between source and drain, then it is said to be in _____region b) saturation	1	2	CO4	PO2
1b	i) Implement the Boolean function $\bar{F} = \overline{(a.b.c)+d}$ using complementary CMOS Logic  	4	4	CO4	PO3
	ii) Design the Boolean function $\bar{F} = \overline{(d + a.(b + c)}$ using dynamic CMOS logic	5	4	CO4	PO3

					
2a	Which one of the following is dynamic logic _____ c. NORA logic	1	2	CO4	PO3
2b	Implement OR/NOR logic using Differential cascade voltage switch logic and Complementary Pass transistor logic **OR/NOR logic using Differential cascade voltage switch logic:**  **OR/NOR logic using Complementary Pass transistor logic** 	9	3	CO4	PO3
3a	In Pseudo-nMOS logic, nMOS transistor operates in b. saturation region	1	2	CO4	PO2
3b	Analyze the operation of DOMINO logic	9	2	CO4	PO2

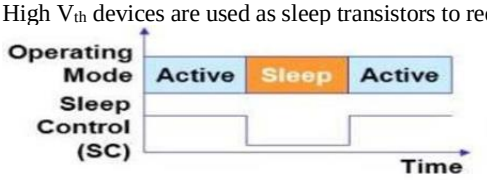
	 • When CLK is low, dynamic node is pre-charged high and buffer inverter output is low. • NFETs in the next logic block will be off. • When CLK goes high, dynamic node is conditionally discharged and the buffer output will conditionally go high. • Since discharge can only happen once, buffer output can only make one low-to-high transition. • When domino gates are cascaded, as each gate "evaluates", if its output rises, it will trigger the evaluation of the next stage, and so on... like a line of dominos falling. • Like dominos, once the internal node in a gate "falls", it stays "fallen" until it is "picked up" by the pre-charge phase of the next cycle. • Thus many gates may evaluate in one eval cycle.  • Weak pFET "keeper" keeps dynamic node pulled high during evaluate phase if it's not being pulled down through nfets => gate is static in both clock phases. • "latching" pFET acts like keeper above unless dynamic node gets pulled down during evaluate phase. When buffer output goes high it switches keeper off saving static power. Good for leakage current problems.. • Note that you can put an even number of static gates after the inverter and before the next domino gate. **Disadvantages:** • "charge sharing" between nodes in the pulldown network and the dynamic node can unintentionally reduce the voltage of the dynamic node enough to switch output buffer. • The addition of the output inverter makes domino gates non-inverting. One can often design around this limitation, but some circuits cannot be implemented solely using domino logic unless both polarities (true and complement) of the inputs are available. If both polarities of inputs are available then we can generate both polarities of internal signals with two domino gates so subsequent stages will have both polarities of their inputs available too.				
4a	Design rules does not specify _____ d) colours	1	1	CO5	PO2
4b	**i)** Draw 2 -input NOR gate using CMOS layout  **ii)** Implement the boolean expression using stick diagram	4 5	3 4	CO5 CO5	PO2 PO2

	$\bar{F} = \overline{(a+b)c}$  				
5a	In nMOS fabrication, etching is done using _____ a. plasma	1	1	CO5	PO2
5b	Illustrate n-well CMOS fabrication process Fabrication Process (Theory) - 5 Marks Fabrication Process (Diagram) - 4Marks  	9	2	CO5	PO2
6a	Silicon oxide is patterned on a substrate using: b) Photolithography	1	1	CO5	PO2
6b	Discuss how enhancement in CMOS technology can be achieved using Multiple threshold voltage and high k dielectric **CMOS Process Enhancements:** • For real time Analog, Digital or RF CMOS integrated circuits along with transistors, other elements such as interconnects, resistors, capacitors are to be integrated on chip. • In order to achieve this, enhancements in CMOS process technology is required. The main goals of adding CMOS enhancements are • To provide on chip capacitors for analog circuits. • To provide on chip resistors. • To provide routing of interconnects **Multi-threshold CMOS** (**MTCMOS**) is a variation of CMOS chip technology which has transistors with multiple threshold voltages (V_{th}) in order to optimize delay or power. • Low V_{th} devices switch faster, and are therefore useful on critical delay paths to minimize clock periods.	9	3	CO5	PO2

- The penalty is that low V_{th} devices have substantially higher static leakage power.
- High V_{th} devices are used on non-critical paths to reduce static leakage power without incurring a delay penalty. Typical high V_{th} devices reduce static leakage by 10 times compared with low V_{th} devices.



- One method of creating devices with multiple threshold voltages is to apply different bias voltages (V_b) to the base or bulk terminal of the transistors.
- Other methods involve adjusting the gate oxide thickness, gate oxide dielectric constant (material type), or dopant concentration in the channel region beneath the gate oxide.
- The most common implementation of MTCMOS for reducing power makes use of sleep transistors.
- Logic is supplied by a virtual power rail.
- Low V_{th} devices are used in the logic where fast switching speed is important.
- High V_{th} devices connecting the power rails and virtual power rails are turned on in active mode, off in sleep mode.
- High V_{th} devices are used as sleep transistors to reduce static leakage power.



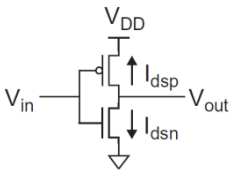
High k-dielectric

- The dielectric constant k, is a parameter defining ability of material to store charge.
- In Si technology the reference value of k of silicon di-oxide, SiO_2, which is 3.9.
- Dielectrics featuring k > 3.9 are referred to as "high"-k dielectric while dielectric featuring k<3.9 are defined as "low"-k dielectrics.
- In cutting edge silicon nano-electronics both high- and low-k dielectrics are needed to implement fully functional very high-density integrated circuit, although, for drastically different reasons.

Need for high-k dielectric:

- Silicon di-oxide (SiO_2) has been used as a gate oxide material for decades.
- As transistors have decreased in size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current, raising device performance.
- As the thickness scales below 2 nm, leakage currents due to tunneling increase drastically, leading to high power consumption and reduced device reliability.
- Replacing the silicon dioxide gate dielectric with a high-k material allows increased gate capacitance without the associated leakage effects.
- In digital circuits, insulating dielectrics separate the conducting parts (wire interconnects and transistors) from one another.
- As components have scaled and transistors are closer together, the insulating dielectrics have thinned to the point where charge build-up and crosstalk adversely affect the performance of the device.
- Replacing the silicon di-oxide with a low-k dielectric of the same thickness reduces parasitic capacitance, enabling faster switching speeds and lower heat dissipation.

7a	In stick diagram, which color is used for n-diffusion? d) yellow	1	1	CO5	PO2
7b	i) Analyze DC characteristics of CMOS Inverter	5	2	CO4	PO2

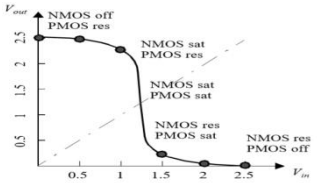


As the source of the nMOS* transistor is grounded, *Vgsn = Vin and Vdsn = Vout

As the source of the pMOS transistor is tied to *VDD*, ***Vgsp = Vin – VDD and Vdsp = Vout – VDD***

$I_{dsn} = -I_{dsp} = |I_{dsp}|$

Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \|V_{tp}\|$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \|V_{tp}\|$	cutoff	linear	$V_{out} = 0$



	ii) Discuss the interconnect layers involved in CMOS process	4	2	CO5	PO2

The interconnect layers involved in process are :

(1) Metal interconnect
(2) Poly-silicon interconnect
(3) Local interconnect.

Metal Interconnect

- The second layer of metal interconnect (Metal 2) is required for digital Integrated circuits.
- The connection between first metal layer (Metal 1) and second metal layer (Metal 2) is established with the help of via.
- For high speed chips third metal layer (Metal 3) is also required.

Poly-silicon Interconnect

- Poly-silicon Interconnect layers are used in ICs because of its high melting points as compare to Aluminium (Al).
- But the major problem with poly-silicon interconnect is it has high sheet resistance because of this for long distance interconnects this provides significant delay.

Local Interconnect

- If silicide is used as a interconnect layer for connecting different cells then it is called as local interconnect.
- The important advantage of local interconnect is it allows direct connection between poly-silicon and diffusion regions.
- Due to this metal contacts are eliminated which reduces the chip area.