SRM Institute of Science and Technology
College of Engineering and Technology

SET B

DEPARTMENT OF ECE

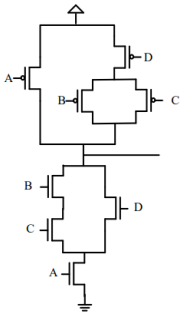
SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

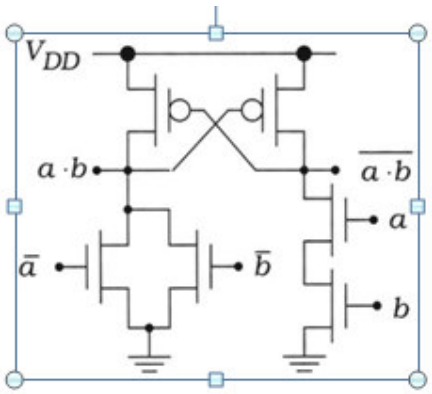
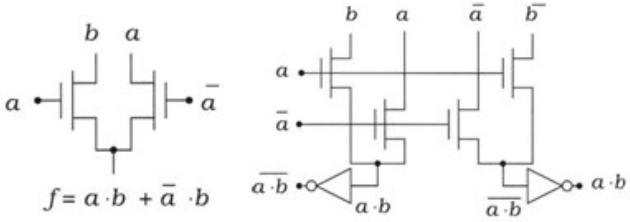
Academic Year: 2022-2023 (EVEN)

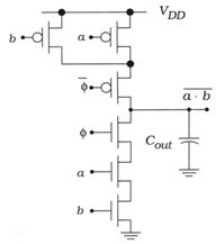
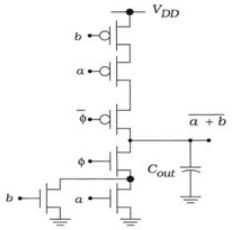
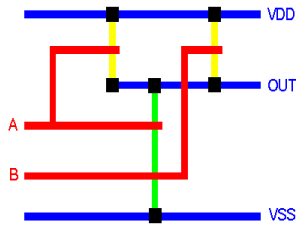
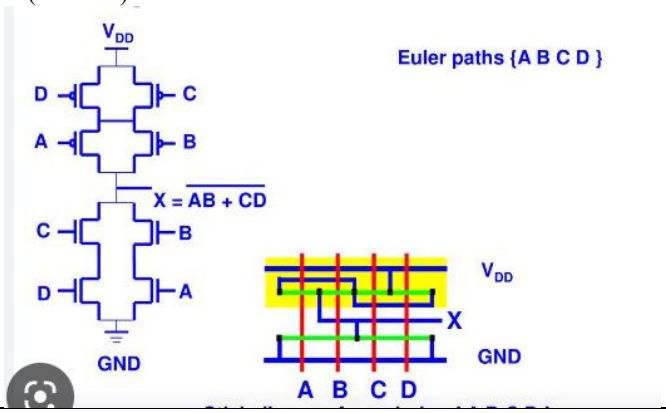
Test: CLAT- 3 **Date:** 2.05.2023
Course Code & Title: 18ECC206J - VLSI Design **Time:** 10:30-12:10 PM
Year & Sem: III & VI **Max. Marks:** 50

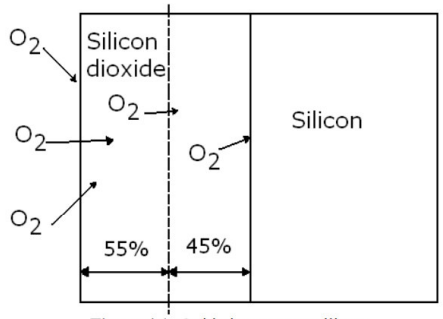
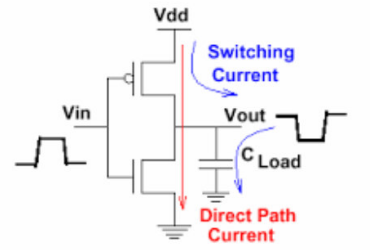
Course Articulation Matrix:

18ECC206J - VLSI Design		Program Learning Outcomes (POs)														
		Graduate Attributes												PSO		
S. No.	Course Outcomes (COs)	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
1	Design and implement digital circuits using Verilog HDL to simulate and verify the designs.	-	3	3	-	3	-	-	-	-	-	-	-	2	-	-
2	Design general VLSI system components, adder cells and multipliers to address the design of datapath subsystem.	-	3	3	-	3	-	-	-	-	-	-	-	2	-	-
	Examine the characteristics of MOS transistors	3	2	-	-	-	-	-	-	-	-	-	-	2	-	-
4	Analyze CMOS inverter and other complex logic gates designed using different logic styles	-	2	2	-	-	-	-	-	-	-	-	-	2	-	-
5	Explain how the transistors are built, and understand the physical implementation of circuits.	-	1	1	-	-	-	-	-	-	-	-	-	2	-	-

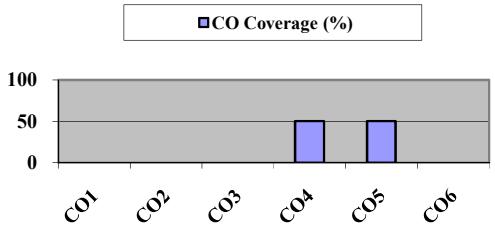
Answer any five questions					
Q. No	**Question**	**Marks**	**BL**	**CO**	**PO**
1	a. If the n-MOS and p-MOS of the CMOS inverters are interchanged the output is measured at: i) **Source of both transistor** ii) Drains of both transistor iii) Drain of n-MOS and source of p-MOS iv) Source of n-MOS and drain of p-MOS	1+4+5	2	CO4	PO2
	b. Implement the Boolean function F= (A (B C + D))' using complementary CMOS Logic.  		4		PO3
	c. Find the Inverter switching threshold for long channel devices with proper expressions.		4		PO3

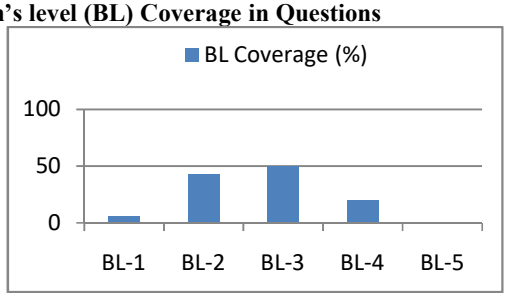
	The above expressions were derived under the assumption that the transistors are velocity-saturated. When the PMOS and NMOS are long-channel devices, or when the supply voltage is low, velocity saturation does not occur ($V_M - V_T < V_{DSAT}$). Under these circumstances, Eq. (5.6) holds for V_M. Derive. $$V_M = \frac{V_{Tn} + r(V_{DD} + V_{Tp})}{1 + r} \quad \text{with } r = \sqrt{\frac{k_p}{k_n}} \qquad (5.6)$$				
2	a. When the input of the CMOS inverter is equal to Inverter Threshold Voltage V_{th}, the transistors are operating in: i) N-MOS is cutoff, p-MOS is in Saturation ii) P-MOS is cutoff, n-MOS is in Saturation iii) Both the transistors are in linear region iv) **Both the transistors are in saturation region** b. Implement AND/NAND logic using Differential cascade voltage switch logic and Complementary Pass transistor logic DCVS:  (a) AND/NAND CPT:  (a) AND gate (b) AND/NAND array	1+9	2 3	CO4	PO3 PO3
3	a. In CMOS logic circuit the p-MOS transistor acts as: i) Pull down network ii) **Pull up network** iii) Load iv) Short to ground b. Implement and analyze the NOR and NAND logic using Clocked CMOS network.	1+9	2 2	CO4	PO2

	 (a) NAND2  (b) NOR2				
4	a. NMOS devices are formed in i) p-type substrate of high doping level ii) n-type substrate of low doping level iii) **p-type substrate of moderate doping level** iv) n-type substrate of high doping level b. Draw 2 -input NAND gate using CMOS layout  c.Implement the boolean expression using stick diagram F=(AB+CD)' 	1+4+5	1 3 4	CO5	PO2
5	a . Which is used for the interconnection? i) boron ii) oxygen iii) **aluminium** iv) silicon b. Illustrate p-well CMOS fabrication process.	1+9	1 2	CO5	PO2
6	a. Oxidation process is carried out using i) **hydrogen and oxygen** ii) low purity oxygen iii) sulphur iv) nitrogen b. Describe the Si oxidation mechanisms. What are the uses of SiO_2	1+9	1	CO5	PO2

	in VLSI circuits? Classify the SiO_2 layer formation techniques and discuss them in brief.  **Figure 4.1:** Oxidation process silicon There are many applications for silicon dioxide. One of them is as diffusion mask. Dopant such as phosphorus and boron have lower diffusion rate in silicon dioxide than in silicon. Therefore, any etching windows on the masking oxide layer, one can dope silicon substrate at the designated area by dopant diffusion process Semiconductor can be oxidized by various methods that include thermal oxidation, electrochemical anodization, and plasma enhanced chemical vapor deposition PECVD.		3		
7	a. Stick diagrams are those which convey layer information through i) thickness ii**) color** iii) shapes iv) layers b. Analyze and describe the static and dynamic power consumption for CMOS Inverter.  **Figure 1. Dynamic power consumption** c. Discuss the plasma etching process. Plasma etching is a form of plasma processing used to fabricate integrated circuits. It involves a high-speed stream of glow discharge (plasma) of an appropriate gas mixture being shot (in pulses) at a sample. The plasma source, known as etch species, can be either charged (ions) or neutral (atoms and radicals).	1+5+4	1 2 2		PO2

Course Outcome (CO) and Bloom's level (BL) Coverage in Questions





Approved by the Course Coordinator **Signature of the Question paper setter**

Evaluation Sheet

Name of the Student: **Register No.:**

Answer any 5 Five Questions					
Q. No	**CO**	**PO**	**Maximum Marks**	**Marks Obtained**	**Total**
1a	**CO4**	**PO2**	**1**		
1b (i)	**CO4**	**PO3**	**4**		
1b (ii)	**CO4**	**PO3**	**5**		
2a	**CO4**	**PO3**	**1**		
2b	**CO4**	**PO3**	**9**		
3a	**CO4**	**PO2**	**1**		
3b	**CO4**	**PO2**	**9**		
4a	**CO5**	**PO2**	**1**		
4b(i)	**CO5**	**PO2**	**4**		
4b(ii)	**CO5**	**PO2**	**5**		
5a	**CO5**	**PO2**	**1**		
5b	**CO5**	**PO2**	**9**		
6a	**CO5**	**PO2**	**1**		
6b	**CO5**	**PO2**	**9**		
7a	**CO5**	**PO2**	**1**		
7b(i)	**CO4**	**PO2**	**5**		
7b)ii)	**CO5**	**PO2**	**4**		

Consolidated Marks:

CO	Maximum Marks	Marks Obtained
4	35	
5	35	
Total		

PO	Maximum Marks	Marks Obtained
PO2	51	
PO3	19	
Total		

Signature of Course Teacher

Signature of the Course Coordinator

Signature of the Academic Advisor