LINEAR INTEGRATED CIRCUITS

Unit- 2
Op–Amp Applications

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Inverting amplifier

The inverting amplifier is shown in Fig. 12.
Here, $R_1 = input\ resistance$,
R_f = feedback resistance
As we have considered 2 assumption for closed loop configuration
(i)$V_d = 0 \Rightarrow V_1 - V_2 = 0$,
As V_1=0, So, $V_2 = 0$. This is known as virtual ground.
(ii) The current drawn by either of input terminals (non-inverting and inverting) is negligible.

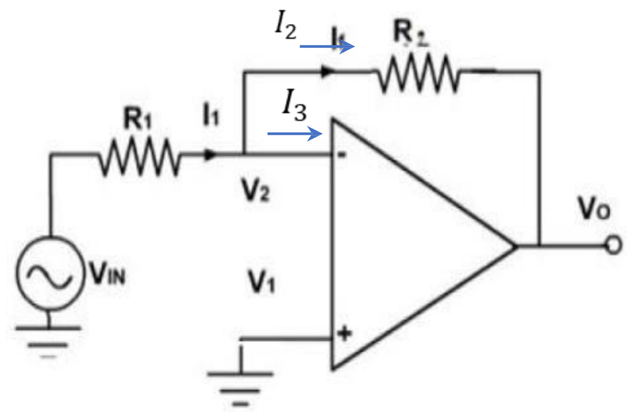


Fig.12. Inverting amplifier

Inverting amplifier (Cont.)

Applying KCL at point V_2

$I_1 = I_2 + I_3$ As $I_3 = 0$

$\Rightarrow \frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_0}{R_f}$ As $V_2 = 0$

$\Rightarrow \frac{V_{in}}{R_1} = \frac{-V_0}{R_f} \Rightarrow V_0 = \frac{-R_f}{R_1} V_{in}$

$\Rightarrow$So, Output voltage= $V_0 = \frac{-R_f}{R_1} V_{in}$

- Closed loop gain of inverting amplifier

$= A_{CL} = \frac{V_0}{V_{in}} = \frac{-R_f}{R_1}$

- The negative sign indicate phase shift of 180^0.
- To avoid loading effect, R_1 should be large.

Non-inverting amplifier

The noninverting amplifier is shown in Fig. 13.

Here, $R_1 = input\ resistance$,

R_f = feedback resistance

As we have considered 2 assumption for closed loop configuration

$(i) V_d = 0 \Rightarrow V_1 - V_2 = 0$,

As $V_1 = V_{in}$, So, $V_2 = V_{in}$.

(ii) The current drawn by either of input terminals (non-inverting and inverting) is negligible. So, $I_3 = 0$.

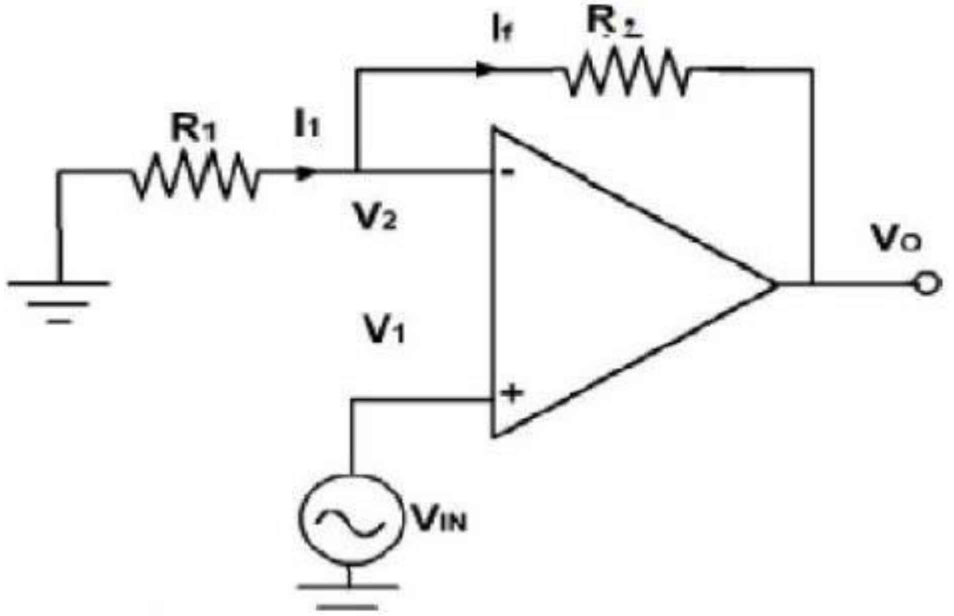


Fig.13. Non-inverting amplifier

Non-inverting amplifier (Cont.)

Applying KCL at point V_2

$I_2 = I_1 + I_3$ As $I_3 = 0$

$\Rightarrow \frac{V_0 - V_2}{R_f} = \frac{V_2 - 0}{R_1}$ As $V_2 = V_{in}$

$\Rightarrow \frac{V_0 - V_{in}}{R_f} = \frac{V_{in}}{R_1}$ => $V_0 = (1 + \frac{R_f}{R_1})\, V_{in}$

$\Rightarrow$So, Output voltage= $V_0 = (1 + \frac{R_f}{R_1})\, V_{in}$

- Closed loop gain of noninverting amplifier

$= A_{CL} = \frac{V_0}{V_{in}} = (1 + \frac{R_f}{R_1})$

Voltage follower

The voltage follower circuit is shown in Fig. 14.

In this circuit, $R_f = 0, R_i = \infty$.

Voltage across A is V_2 and B is V_1

As $V_d = 0 \Rightarrow V_1 - V_2 = 0,$

As $V_1 = V_{in}$, So, $V_2 = V_{in}$.

So, $V_0 = V_2 = V_{in}$

$\Rightarrow$So, Output voltage= $V_0 = V_{in}$

Closed loop gain of voltage follower

$= A_{CL} = \frac{V_0}{V_{in}} = 1$

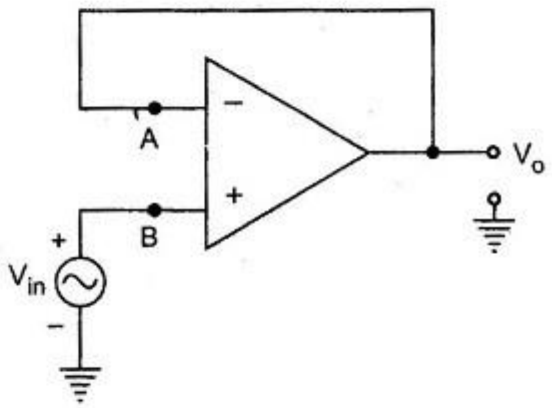


Fig.14. Voltage follower

Summing amplifier

I. <u>Inverting configuration:</u>

R_{comp} is used to nullify the offset input current, so $I_B^- = 0$,

$$V_I = V_n = 0.$$

Applying KCL at V_I

$I_1 + I_2 + I_3 = I_4 + I_B^-$

$\Rightarrow \frac{V_1 - V_I}{R_1} + \frac{V_2 - V_I}{R_2} + \frac{V_3 - V_I}{R_3} = \frac{V_I - V_0}{R_f}$

$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_0}{R_f}$

$\Rightarrow V_0 = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$

$\Rightarrow V_0 = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$ ------Eqn (1)

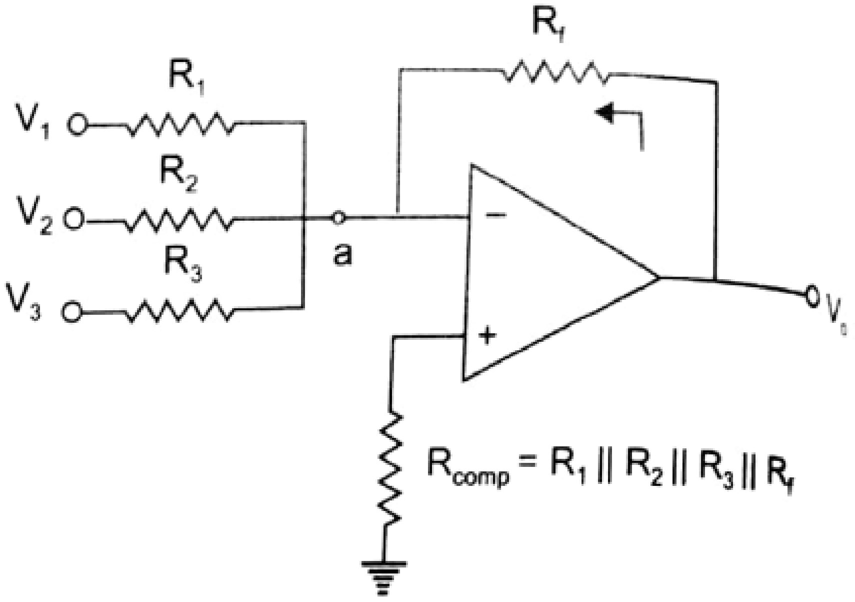


Fig.1. Inverting configuration

Inverting configuration (Cont.)

(i) <u>Summing amplifier (inverting amplifier)</u>

In the Fig.1, if $R_1 = R_2 = R_3 = R$

$$V_0 = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

Then above equation becomes

$$V_0 = -\left(\frac{R_f}{R}V_1 + \frac{R_f}{R}V_2 + \frac{R_f}{R}V_3\right)$$

$\Rightarrow V_0 = -\frac{R_f}{R}(V_1 + V_2 + V_3)$

The output of fig.1 is sum of the Voltages, for $R_1 = R_2 = R_3 = R$

Inverting configuration (Cont.)

<u>(ii) Scaling or weighted amplifier</u>

If each input voltage is amplified by a different vector or weighted differently called scaling or weighted amplifier (Using Fig.1).

Here, $R_1 \neq R_2 \neq R_3$

So, output of the inverting scaling amplifier is

$$V_0 = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

Inverting configuration (Cont.)

(iii) Average circuit amplifier:- The Fig.1. can be used as an averaging circuit, in which output voltage is equal to the average value of all input voltages.

Here, $R_1 = R_2 = R_3 = R$

and $\frac{R_f}{R} = \frac{1}{n}$

Where, n is number of input voltage sources. Putting these values in equation (1)

$$V_0 = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

$=> V_0 = -\left(\frac{R_f}{R}V_1 + \frac{R_f}{R}V_2 + \frac{R_f}{R}V_3\right)$

$\Rightarrow V_0 = -\frac{R_f}{R}(V_1 + V_2 + V_3) = \frac{-1}{n}(V_1 + V_2 + V_3) = \frac{-(V_1+V_2+V_3)}{3}$

$\Rightarrow V_0 = \frac{-(V_1+V_2+V_3)}{3}$

Summing, scaling, and averaging amplifiers

II. Non-inverting configuration

In ideal case, $I_B^- = I_B^+ = 0$,

Applying KCL at V_n

$I_1 + I_2 + I_3 = I_B^+$

$$=> \frac{V_1 - V_n}{R_1} + \frac{V_2 - V_n}{R_2} + \frac{V_3 - V_n}{R_3} = 0$$

$$=> \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{V_n}{R_1} + \frac{V_n}{R_2} + \frac{V_n}{R_3}$$

$$=> V_n = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \quad \text{-----Equation(2)}$$

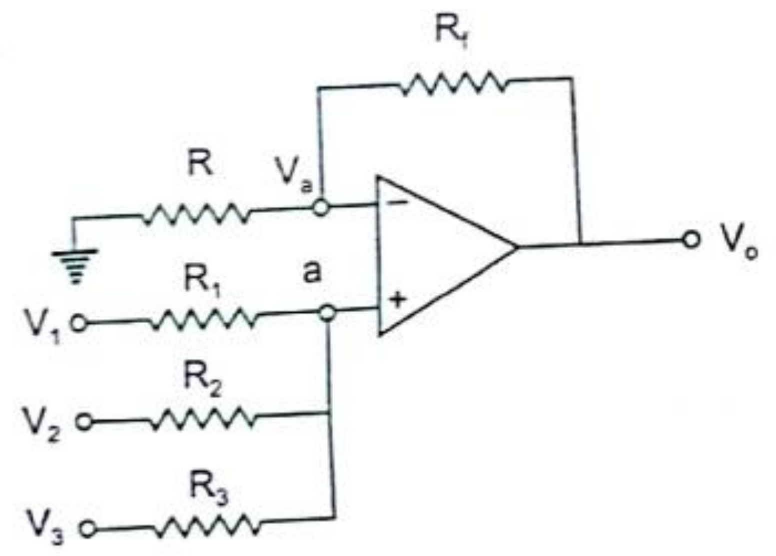


Fig.2. Non-inverting configuration

Non-inverting configuration

- Applying KCL at V_I

$$I_4 = I_B^- + I_5$$

$$\Rightarrow \frac{0-V_I}{R} = \frac{V_I - V_0}{R_f} \Rightarrow V_0 = V_I(1+\frac{R_f}{R})$$

$$\text{As, } V_I = V_n = \frac{\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}}$$

$$=> V_0 = \frac{\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}}(1+\frac{R_f}{R}) \qquad \text{--Equation(3)}$$

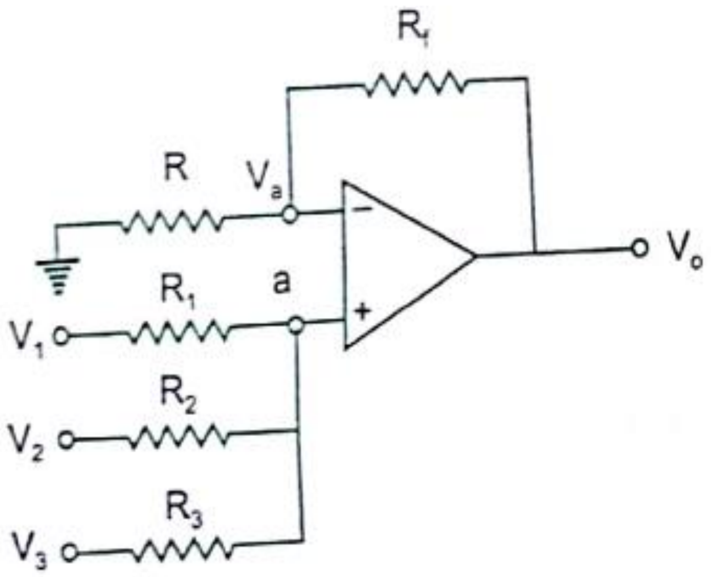


Fig.2. Non-inverting configuration

Non-inverting configuration (Cont.)

(i) <u>Summing amplifier (non-inverting configuration)</u>

Here $R_1 = R_2 = R_3 = R$, $R = \frac{R_f}{2}$

$$V_0 = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \left(1 + \frac{R_f}{R}\right)$$

Then, output voltage of summing non-inverting amplifier is:

$$V_0 = \frac{\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R}}{\frac{1}{R} + \frac{1}{R} + \frac{1}{R}} \left(1 + \frac{2R}{R}\right) = \frac{\frac{1}{R}(V_1 + V_2 + V_3)}{\frac{3}{R}}(3)$$

$= (V_1 + V_2 + V_3)$ (output of non-inverting summing amplifier)

Non-inverting configuration (Cont.)

(ii) Average amplifier:

Here, $R_1 = R_2 = R_3 = R$

The output of non-inverting average amplifier is:

$$V_0 = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}\left(1 + \frac{R_f}{R}\right)$$

Then, output voltage of averaging non-inverting amplifier is:

$$V_0 = \frac{\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R}}{\frac{1}{R} + \frac{1}{R} + \frac{1}{R}}\left(1 + \frac{R_f}{R}\right) = \frac{\frac{1}{R}(V_1 + V_2 + V_3)}{\frac{3}{R}}\left(1 + \frac{R_f}{R}\right) = \frac{(V_1 + V_2 + V_3)}{3}\left(1 + \frac{R_f}{R}\right)$$

=> $V_0 = \frac{(V_1 + V_2 + V_3)}{3}\left(1 + \frac{R_f}{R}\right)$ (Output of non-inverting average amplifier)

Differential Configuration

- Using differential op-amp configuration, a subtractor and a adder-subtractor (summing) amplifier may be constructed.

(i) <u>A subtractor</u>

Applying KCL at V_n

$I_1 = I_2 + I_B^+$ $\qquad\qquad I_B^+ = 0$

$=> \frac{V_1 - V_n}{R} = \frac{V_n}{R} => V_n = \frac{V_1}{2}$

$V_I = V_n = \frac{V_1}{2}$

Applying KCL at V_I

$I_3 = I_4 + I_B^-$ $\qquad\qquad I_B^- = 0$

$\Rightarrow \frac{V_2 - V_I}{R} = \frac{V_I - V_0}{R} => V_0 = -V_2 + 2\,V_I$

$\Rightarrow V_0 = -V_2 + 2\frac{V_1}{2} = V_1 - V_2$

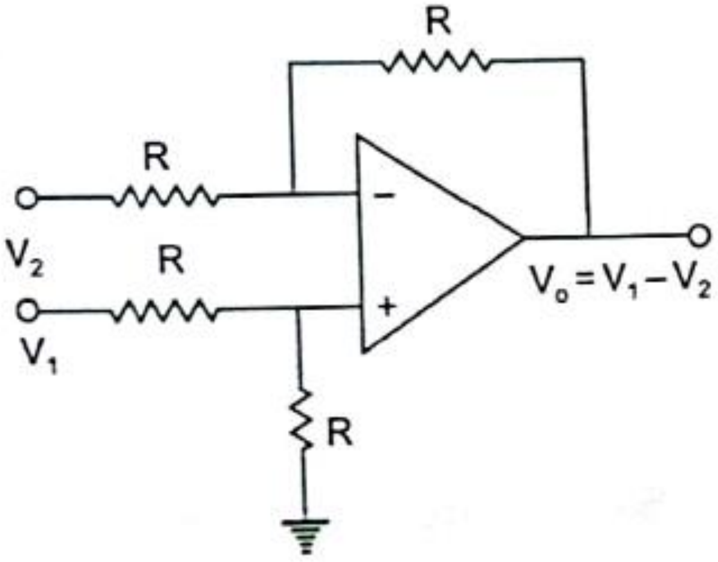


Fig.3. Subtractor

Differential Configuration

(ii) Adder-subtractor

Applying KCL at V_n

$I_1 + I_2 = I_3 + I_B^+$ $\qquad I_B^+ = 0$

$=> \frac{V_3 - V_n}{R} + \frac{V_4 - V_n}{R} = \frac{V_n}{R} => V_n = \frac{V_3 + V_4}{3}$

$V_I = V_n = \frac{V_3 + V_4}{3}$

Applying KCL at V_I

$I_4 + I_5 = I_6 + I_B^-$ $\qquad I_B^- = 0$

$=> \frac{V_1 - V_I}{R} + \frac{V_2 - V_I}{R} = \frac{V_I - V_0}{R}$

$\Rightarrow V_0 = 3V_I - V_1 - V_2$

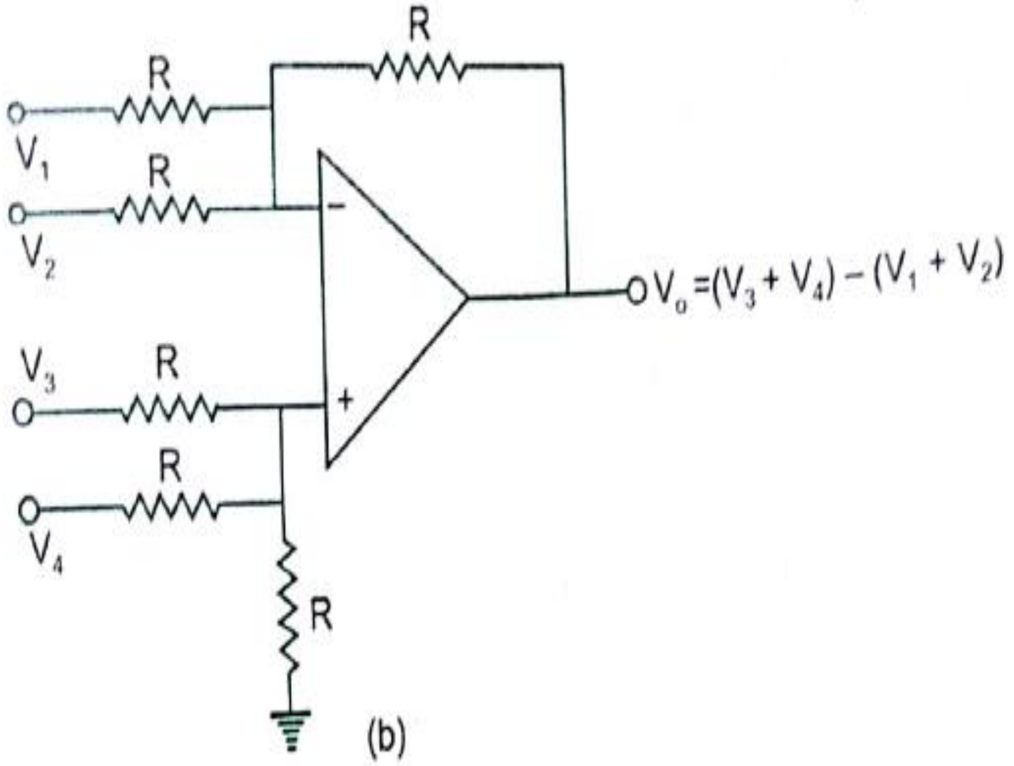


Fig.4. Adder-subtractor

Adder-subtractor

$\Rightarrow V_0 = 3V_I - V_1 - V_2$

$V_I = V_n = \frac{V_3 + V_4}{3}$

$\Rightarrow V_0 = \frac{3(V_3 + V_4)}{3} - V_1 - V_2$

$\Rightarrow V_0 = V_3 + V_4 - V_1 - V_2$

It is the output of adder-subtractor circuit.

Problem

1.Q. Design an adder circuit using an op-amp to get the output expression as

$$V_0 = -(0.1V_1 + V_2 + 10V_3)$$

Ans:- $V_0 = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$

Given, $V_0 = -(0.1V_1 + V_2 + 10V_3)$

$\frac{R_f}{R_1}$=0.1=> R_1=10 R_f , $\frac{R_f}{R_2}$=1=> R_f= R_2

$\frac{R_f}{R_3}$=10=> R_3=0.1 R_f

Let, R_f =10 KΩ

So, R_1= 100 KΩ, R_2= 10 KΩ, R_3= 1 KΩ

AC amplifier

- To get the AC frequency response of an op-amp or if the ac input signal is superimposed with dc level, it becomes essential to block the dc component.
- Coupling capacitor is used for blocking the dc component of ac amplifier.

Types of AC amplifier

(i) Inverting AC amplifier

(ii) Non-inverting AC amplifier

Inverting AC amplifier

- Applying KCL at V_2

$$I_1 + I_2 = I_B^-, \qquad I_B^- = 0$$

$$\frac{V_i - V_2}{R_1 + \frac{1}{sc}} + \frac{V_0 - V_2}{R_f} = 0, \qquad V_2 = 0$$

$$\Rightarrow \frac{V_i}{R_1 + \frac{1}{sc}} + \frac{V_0}{R_f} = 0$$

$$\Rightarrow \frac{V_i}{R_1 + \frac{1}{sc}} = \frac{-V_0}{R_f}$$

$$\Rightarrow A_{CL} = \frac{V_0}{V_i} = \frac{-R_f}{R_1 + \frac{1}{sc}} = \frac{-R_f}{R_1(1 + \frac{1}{sR_1c})}$$

$$\Rightarrow A_{CL} = \frac{-R_f}{R_1} \frac{sR_1c}{1 + sR_1c}$$

Let $R_1 c = \tau$

$$\Rightarrow A_{CL} = \frac{-R_f}{R_1} \frac{s\tau}{1 + s\tau}$$

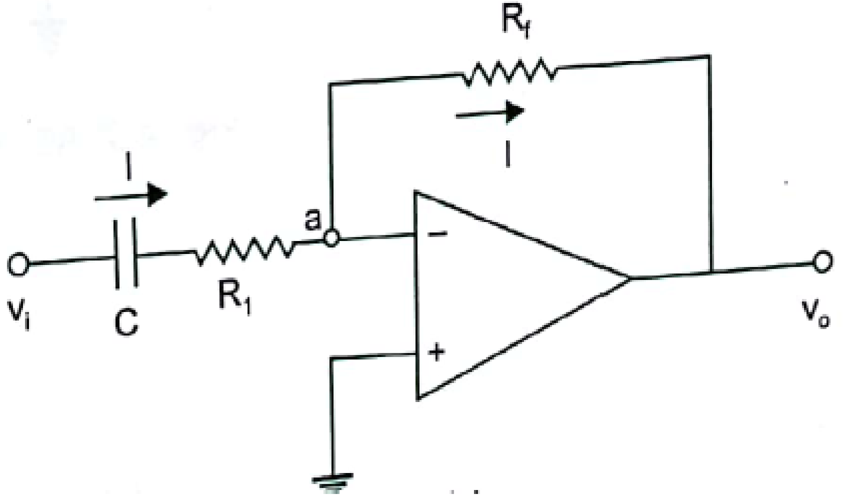


Fig.5. Inverting AC amplifier

Inverting AC amplifier (Cont.)

A_{CL} is at low frequency

So, lower cut-off frequency=$f_L = \frac{1}{2\pi\tau} = \frac{1}{2\pi R_1 c}$

At mid-band range, the capacitor behaves as a short circuit,

So $A_{CL} = \frac{-R_f}{R_1}$

Non-inverting AC amplifier

- Resistor R_2 is added to provide a dc return to ground as shown in Fig.6 .
- This reduces the overall input impedance of the amplifier (R_2).
- This problem of low input impedance is eliminated by connecting capacitor c_3 as shown in Fig.7.

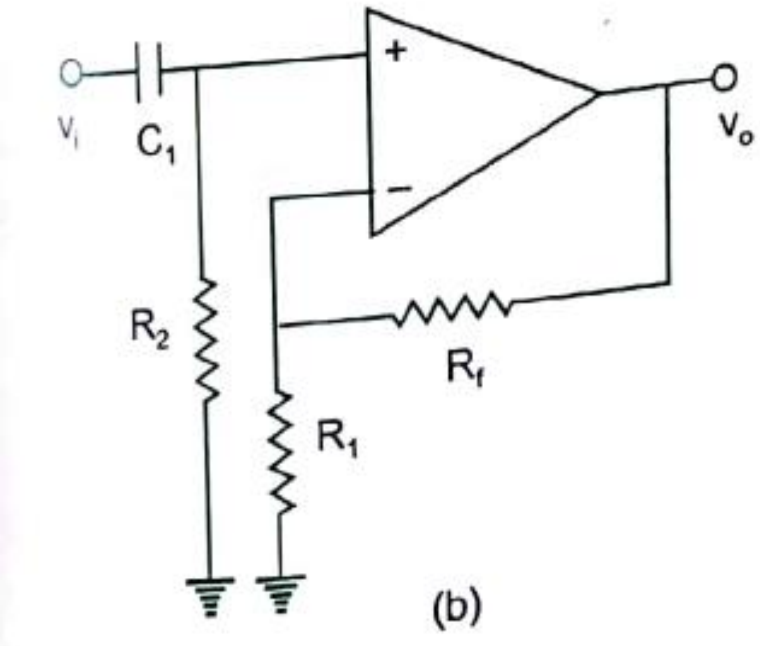


Fig.6. Non-inverting AC amplifier

Non-inverting AC amplifier (Cont.)

- This problem of low input impedance is eliminated by connecting capacitor c_3 as shown in Fig.
- Capacitor c_3 is large enough to act as short circuit to ac signal.
- Node ‘n’ and non-inverting terminal are almost the same potential, so R_2 carries almost no current.
- So, the circuit will have extremely high input impedance

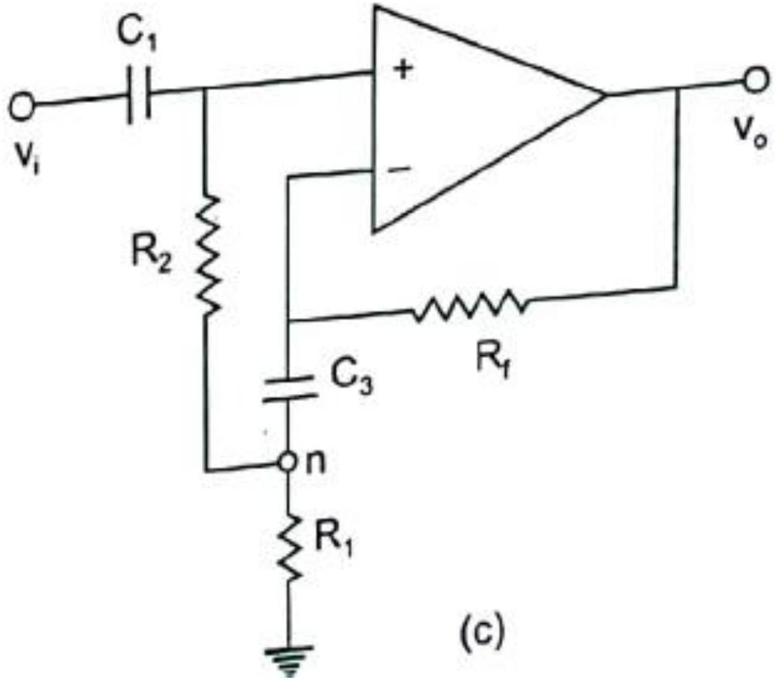


Fig.7. High input impedance non-inverting ac amplifier

AC voltage follower

- The circuit of practical ac voltage follower is shown in Fig.8.
- The circuit is used as a buffer to connect a high impedance signal source to a low impedance load, which may even be capacitive.
- c_1, c_2 are chosen high so that they are short circuit at all frequencies of operation.
- Resistor R_1, R_2 provide a path for dc input current into the non-inverting terminal.
- c_2 act as a bootstrapping capacitor and connects the resistance R_1 to the output terminal for AC operation.
- It has very high input impedance.

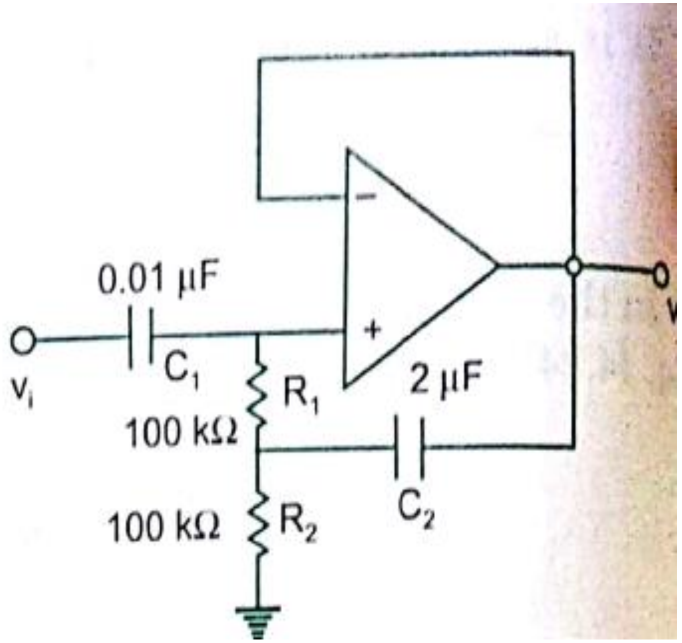


Fig.8. AC Voltage follower

Voltage to current converter(V to I converter) (transconductance amplifier)

- In many application, voltage signal need to be converted to a proportional output current.
- There are 2 types of circuits are possible

(i) V to I converter with floating load

(ii) V to I converter with grounded load

V to I converter with floating load

Fig.9. shows V to I converter with floating load.

According to assumption, $I_B^- = 0$

$V_1 = V_i, V_1 = V_2$

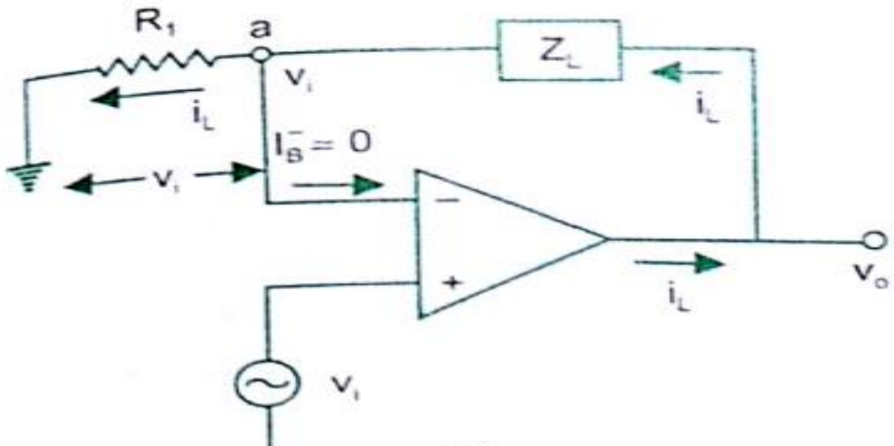
Applying KCL at V_2

$I_1 + I_B^- = I_L, I_B^- = 0$

$\Rightarrow \frac{V_1}{R_1} = I_L,$ As $V_1 = V_i$

$\Rightarrow I_L = \frac{V_i}{R_1}$

So, here input voltage V_i is converted to output current $\frac{V_i}{R_1}$



(a)

Note : It may be seen that the same current flows through the signal source and the load and therefore, the signal source should be capable of providing this load current.

- This circuit is also called a *current-series negative feedback amplifier* because the feedback voltage across R_1 (applied to the inverting terminal) depends on the output current I_L and is in series with the input difference voltage V_{id}.

V to I converter with grounded load

Fig. 10 shows V to I converter with grounded load

Applying KCL at node V_1

$I_1 + I_2 = I_B^+ + I_L, \quad I_B^+ = 0$

$\Rightarrow I_1 + I_2 = I_L$

$\Rightarrow \frac{V_i - V_1}{R} + \frac{V_0 - V_1}{R} = I_L$

$\Rightarrow V_i - 2V_1 + V_0 = I_L \mathrm{R}$

$\Rightarrow V_1 = \frac{V_i + V_0 - I_L \mathrm{R}}{2}$

Applying KCL at node V_2

$I_5 + I_B^- = I_6, \quad$ as $I_B^- = 0$

$=> \frac{V_2}{R} = \frac{V_0 - V_2}{R}$

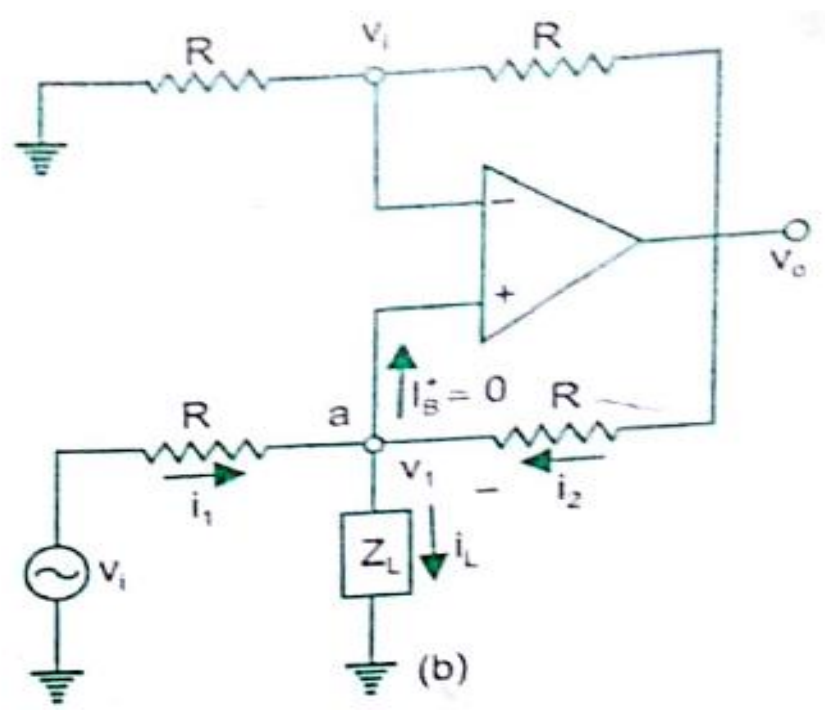


Fig. 10

V to I converter with grounded load (Cont.)

$$\frac{V_2}{R} = \frac{V_0 - V_2}{R}$$

$\Rightarrow V_0 = 2\, V_2$

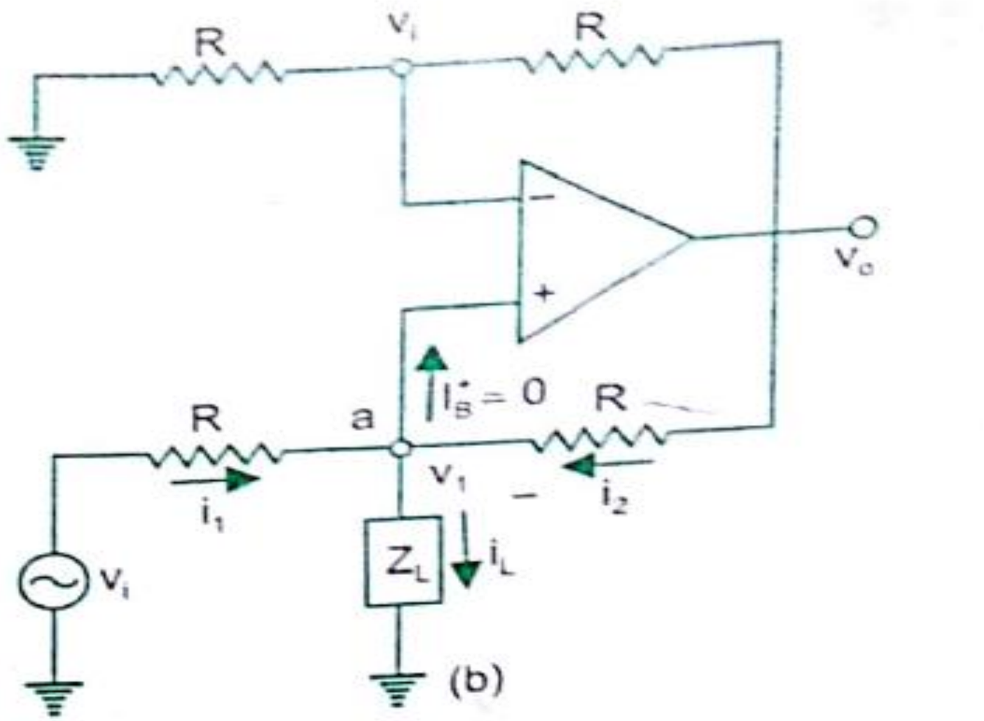
As, $V_2 = V_1$

As, $V_1 = \frac{V_i + V_0 - I_L \mathrm{R}}{2}$

$\Rightarrow V_0 = 2\, (\frac{V_i + V_0 - I_L \mathrm{R}}{2})$

$\Rightarrow V_0 = V_i + V_0 - I_L \mathrm{R}$

$\Rightarrow I_L = \frac{V_i}{R}$



V to I converter with grounded load (Cont.)

- As the input impedance of a non-inverting amplifier is very high, this circuit has the advantage of drawing little current from the source.
- A voltage to current converter is used for low voltage dc, and ac voltmeter, LED, and Zener diode tester.

Current to voltage converter (trans-resistance amplifier)

- Photocell, photodiode and photovoltaic cell give an output current that is proportional to an incident radiant energy light.
- The current through the device can be converted to voltage by current to voltage converter, and there by amount of light or radiant energy incident on the photo device can be measured.

Current to voltage converter (Cont.)

- According to ideal characteristic, $V_2 = V_1$
- As, V_1=0

$I_s = \frac{V_1 - V_0}{R_f}$

=> $V_0 = - I_s R_f$

- R_f is shunted with a capacitor c_f to reduce the high frequency noise and possibility of oscillations.

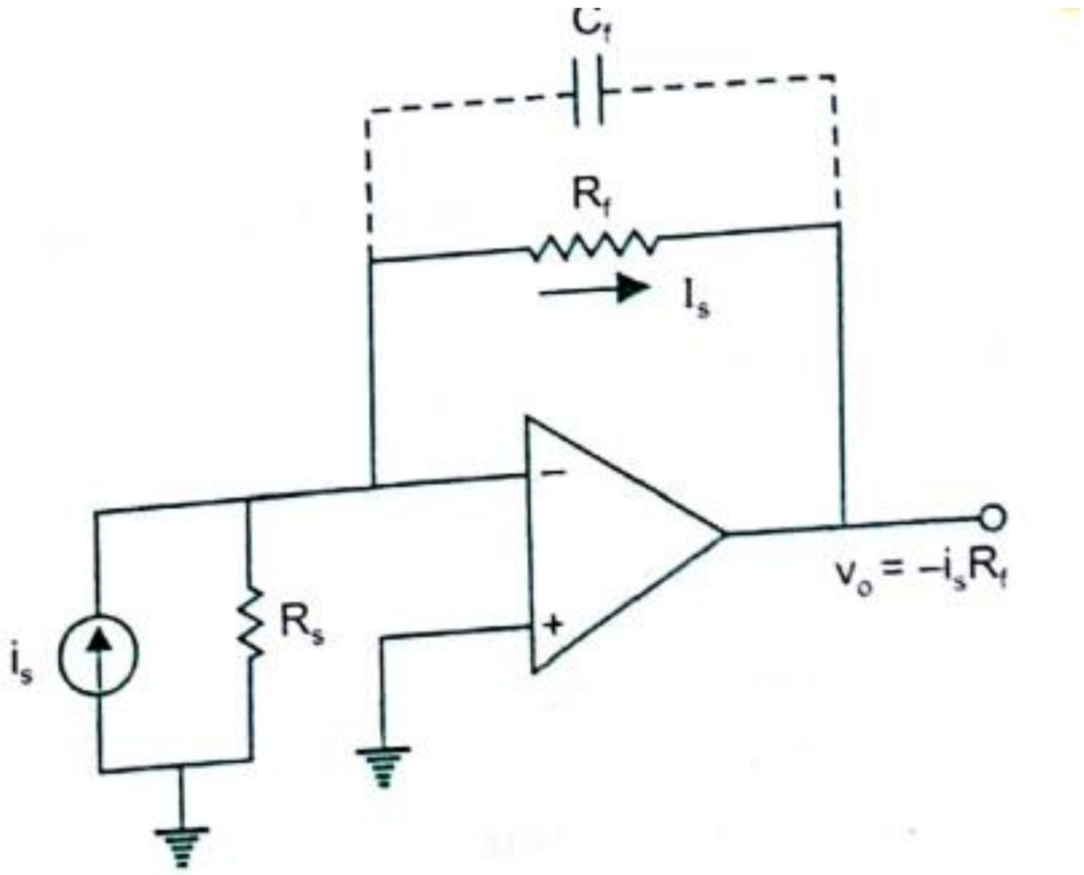


Fig. 11. I to V converter

Instrumentation amplifier

- In a number of industrial and consumer application measurement and control of physical quantities is needed.
- Some examples are measurement and control of temperature, humidity, light intensity, waterflow etc.
- These physical quantities are usually measured with the help of transducers.
- The output of transducer has to be amplified so that it can drive the indicator or display system.
- This function is performed by an instrumentation amplifier.

Instrumentation amplifier (Cont.)

- The important features of an instrumentation amplifier are:

(i) High gain accuracy

(ii) High CMRR

(iii) High gain stability with low temperature coefficient

(iv) Low dc offset

(v) Low output impedance

There are specially designed op-amps such as μA725 to meet the above stated requirements of a good instrumentation amplifier.

Instrumentation amplifier (Cont.)

Applying KCL at V_n

$$I_1 = I_B^+ + I_7$$

As I_B^+=0

$$\frac{V_1 - V_n}{R_3} = \frac{V_n}{R_4} => (V_1 - V_n)\, R_4 = V_n\, R_3$$

$$\Rightarrow V_n = \frac{R_4}{R_3 + R_4}\, V_1$$

Applying KCL at V_I

$$I_3 = I_B^- + I_4$$

As I_B^-=0

$$\frac{V_2 - V_I}{R_1} = \frac{V_I - V_0}{R_2}$$

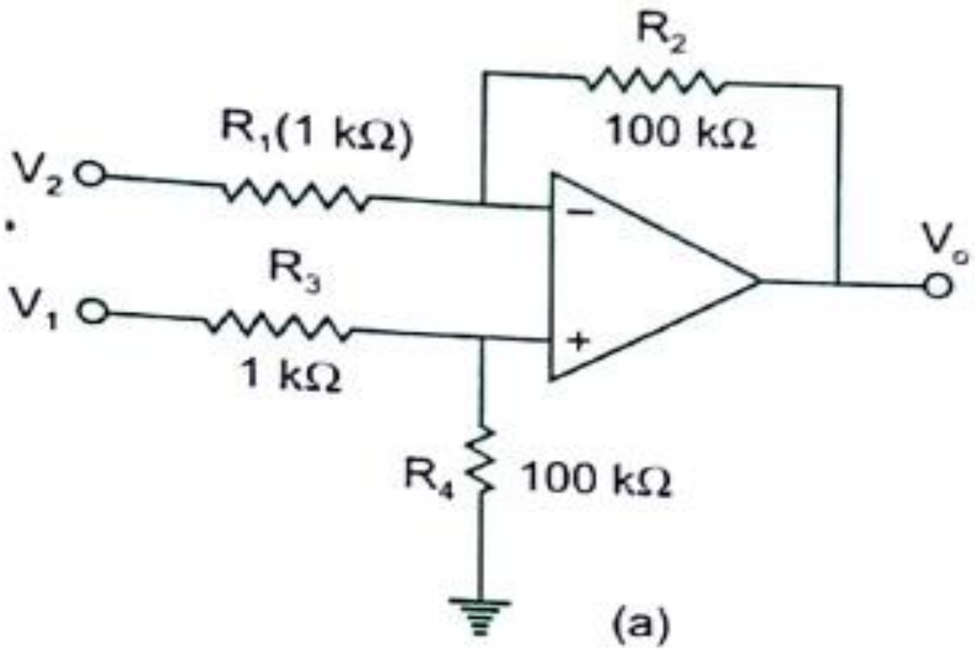


Fig.12. Differential amplifier using single op-amp

Instrumentation amplifier (Cont.)

$$\frac{V_2 - V_I}{R_1} = \frac{V_I - V_0}{R_2}$$

$$V_n = V_I = \frac{R_4}{R_3 + R_4} V_1$$

$$\Rightarrow (V_2 - V_I)\, R_2 = (V_I - V_0)\, R_1$$

$$\Rightarrow V_0 = \frac{-V_2 R_2}{R_1} + \left(\frac{R_2 + R_1}{R_1}\right) V_I$$

$$\Rightarrow V_0 = \frac{-V_2 R_2}{R_1} + \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_3 + R_4} V_1$$

For $\frac{R_1}{R_2} = \frac{R_3}{R_4}$

$$\Rightarrow V_0 = \frac{-V_2 R_2}{R_1} + \left(1 + \frac{R_2}{R_1}\right) \frac{1}{\frac{R_3}{R_4} + \frac{R_4}{R_4}} V_1$$

Instrumentation amplifier (Cont.)

- $V_0 = \frac{-V_2 R_2}{R_1} + (1 + \frac{R_2}{R_1}) \frac{1}{\frac{R_3}{R_4} + \frac{R_4}{R_4}} V_1$

$=> V_0 = \frac{-V_2 R_2}{R_1} + (\frac{R_1 + R_2}{R_1}) \frac{1}{\frac{R_1}{R_2} + \frac{R_2}{R_2}} V_1$

$=> V_0 = \frac{-V_2 R_2}{R_1} + \frac{V_1 R_2}{R_1} = \frac{R_2}{R_1}(V_1 - V_2)$

If in the figure-12, the source V_1 sees an input impedance $R_3 + R_4$ (1 KΩ+100 KΩ), And V_2 sees an input impedance R_1 (1 KΩ). This low impedance may load the signal source heavily.

So, High resistance buffer is used proceeding each input to avoid this loading effect as shown in figure-13

Instrumentation amplifier (Cont.)

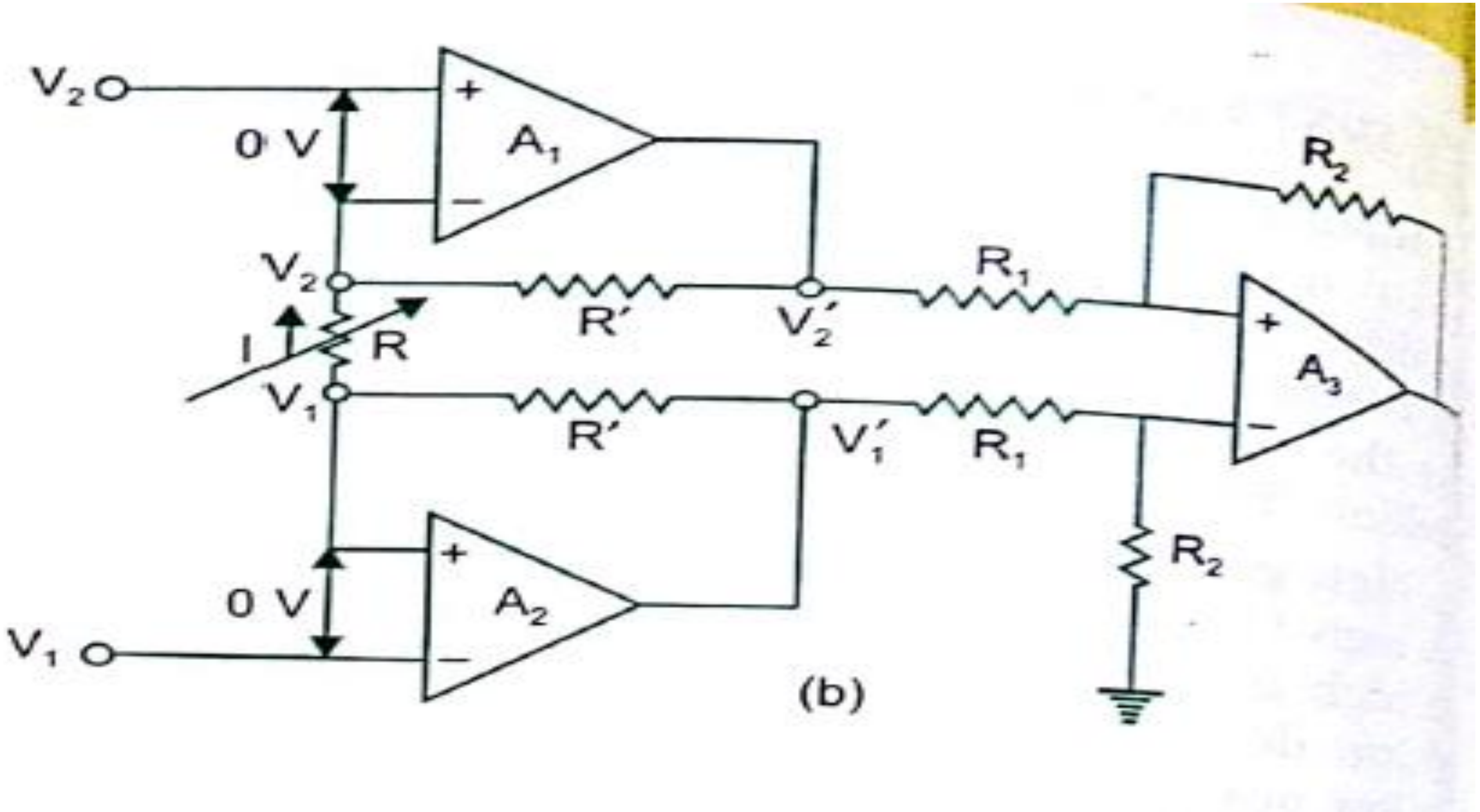


Figure :13 Instrumentation amplifier

Instrumentation amplifier (Cont.)

- The op-amp $A_{1,}\, A_2$ have differential input voltage zero.
- For $V_1 = V_2$ (Under common mode condition), the voltage across R =0,
- As no current flows through R and R' the non-inverting op-amp A_1 and A_2 act as a voltage follower.
- So $V_2' = V_2, V_1' = V_1$

Instrumentation amplifier using transducer bridge

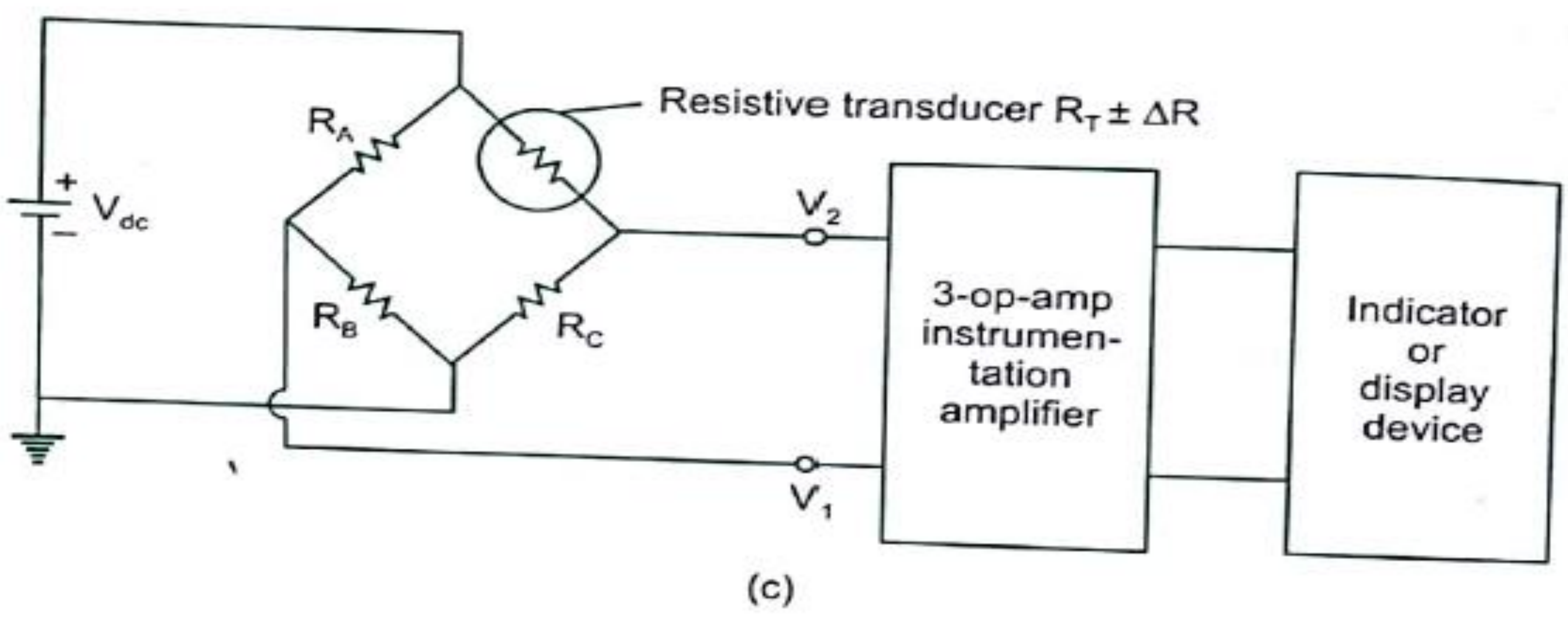
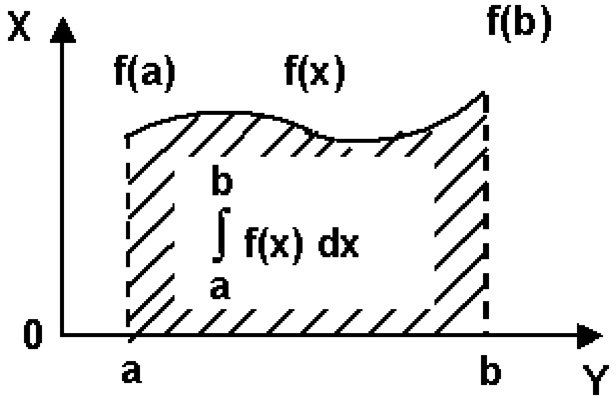


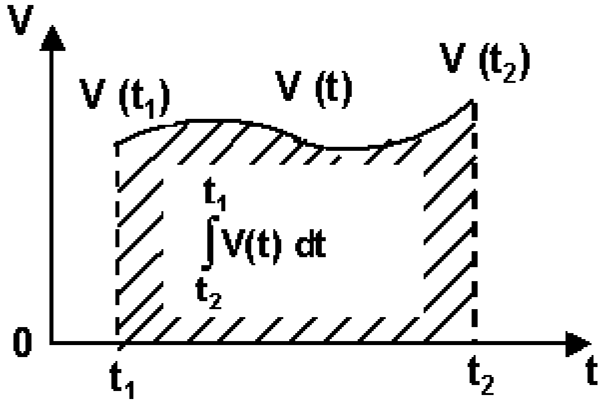
Figure.14 Instrumentation amplifier using transducer bridge

Integrator

- ✓Useful on control circuits / networks wherever a differential equation must be solved or the integral of a voltage is needed.
- ✓ Useful for generating saw tooth and triangular waveforms.
- ✓ Integration can be thought of as determining the area under a curve.
- ✓ op-amp integrator operates over a period of time

The integral as an area





Integrator

- A circuit in which output voltage waveform is the integration of the input voltage waveform is integrator integration amplifier.
- The integrator circuit is shown in Fig

$V_1 = 0$, as $V_1 = V_2$=> $V_2 = 0$

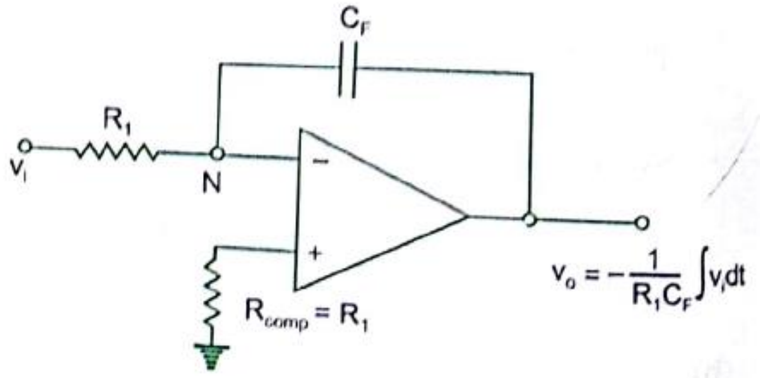
(assumption-ii)

I_3=0 (assumption-i)

- Applying KCL at point at A

$I_1 = I_2 + I_3$

=>$\frac{V_{in}-V_2}{R_1}$=$c_F \frac{d(V_2-V_0)}{dt}$=> $\frac{V_{in}}{R_1}$ = -$c_F \frac{d(V_0)}{dt}$



Integrator

Integrator (Cont.)

$\Rightarrow \frac{V_{in}}{R_1} = -c_F \frac{d(V_0)}{dt}$

Integrating both sides

$$\frac{1}{R_1} \int_0^t V_{in}\, dt = -c_F V_0 + V_0|_{t=0}$$

$=> V_0 = \frac{-1}{R_1 c_F} \int_0^t V_{in}\, dt + \mathrm{C}$

C is the integration constant and is proportional to the value of output voltage at time=t=0.

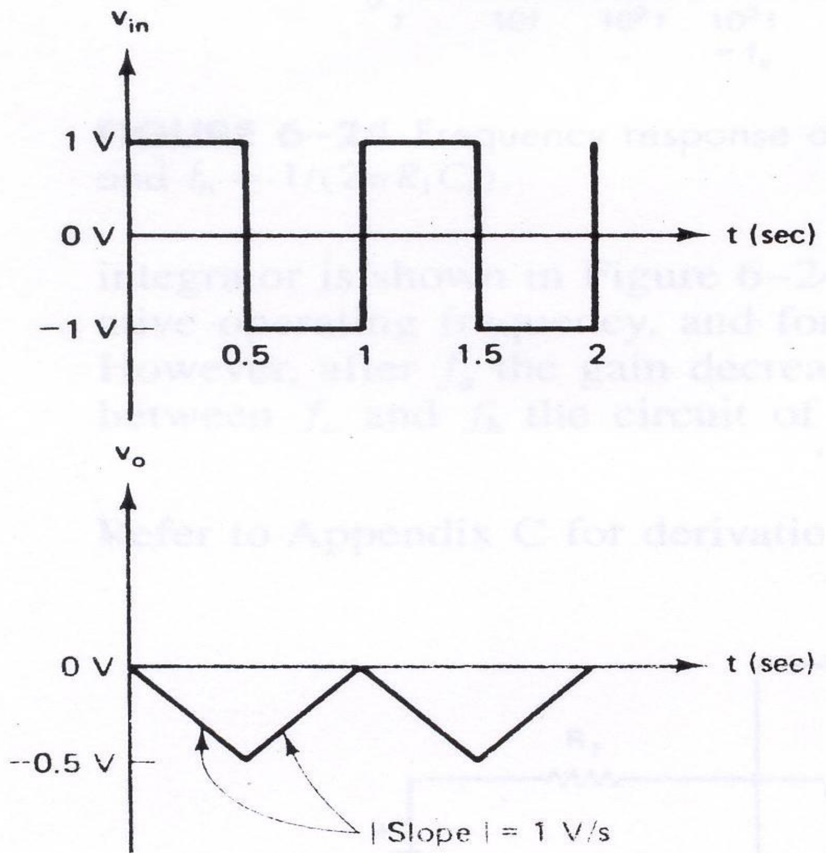
Observation:

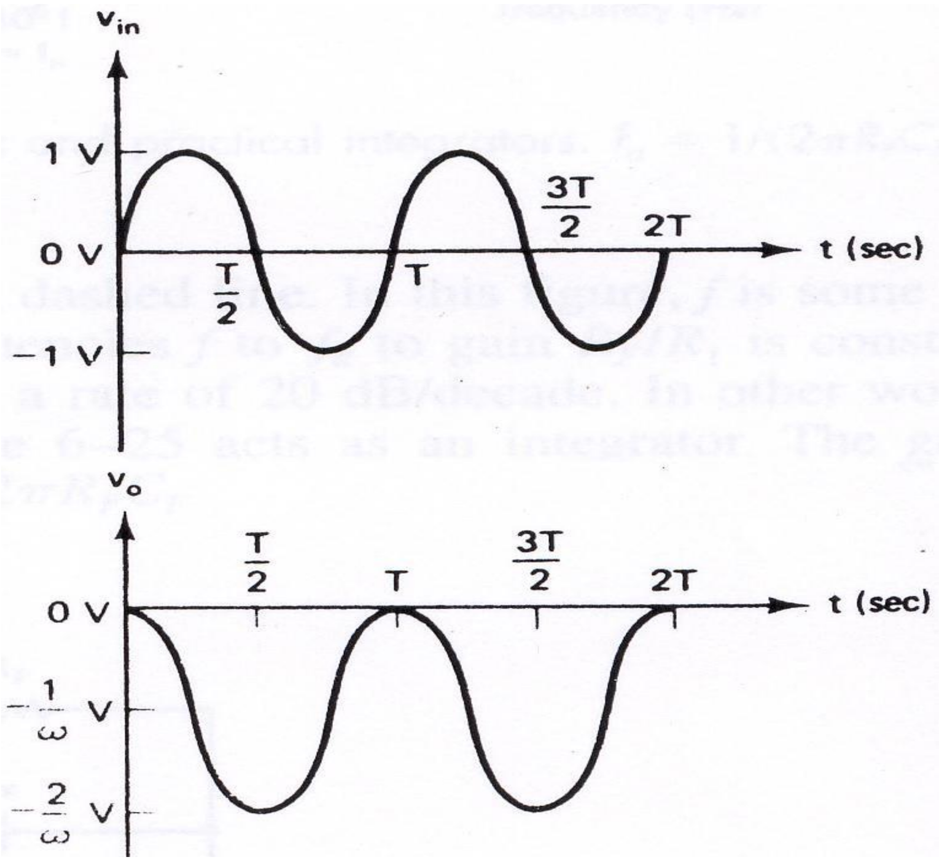
1. Output voltage is directly proportional to negative integral of input signal.
2. Output voltage is inversely proportional to time constant $R_1 c_F$

Integrator (Cont.)

- For sinewave input, output will be cosine wave.
- If input is square wave, output will be triangular wave.

<u>Input and Output waveforms</u>





Integrator (Cont.)

- In phasor notation, considering impedance value of C_F is $\frac{1}{sC_F}$

$V_1 = 0$, as $V_1 = V_2 \Rightarrow V_2 = 0$

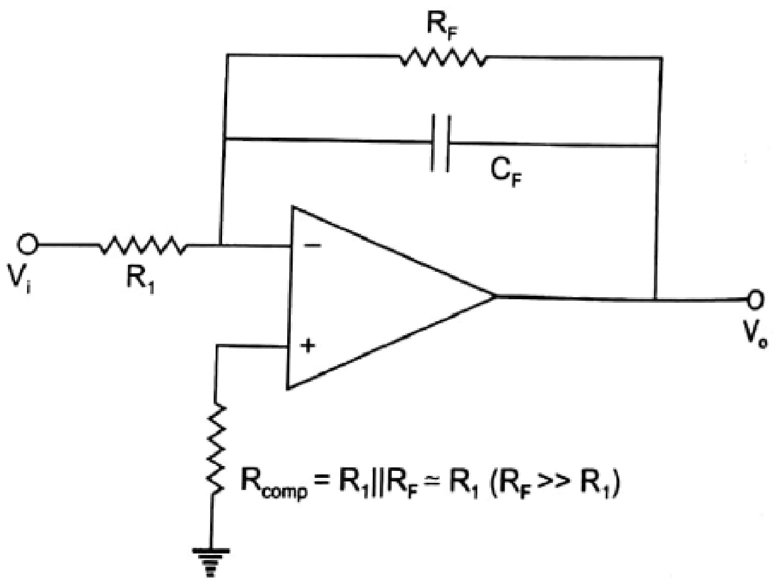
(assumption-ii)

I_3=0 (assumption-i)

- Applying KCL at point at A

$I_1 = I_2 + I_3$

$\Rightarrow \frac{V_{in} - V_2}{R_1} = \frac{(V_2 - V_0)}{\frac{1}{sC_F}} \Rightarrow \frac{V_{in}}{R_1} = -sc_F V_0$



Integrator

Integrator (Cont.)

$\frac{V_{in}}{R_1} = -sc_F V_0$

$\Rightarrow V_0(\mathrm{s}) = \frac{-1}{sc_F R_1} V_{in}(\mathrm{s})$

$\Rightarrow V_0(jw) = \frac{-1}{jwc_F R_1} V_{in}(jw)$

$\Rightarrow \mathrm{Gain} = |\mathrm{A}| = \frac{V_0(jw)}{V_{in}(jw)} = \left|\frac{-1}{jwc_F R_1}\right| = \frac{1}{wc_F R_1}$

The frequency at which gain of the integrator is 0 dB is $f_b = \frac{1}{2\pi R_1 C_F}$

When, w=0, |A|=∞.

In practical, output never becomes ∞.

Integrator (Cont.)

- For proper integration, RC has to be much greater than the time period of the input signal.
- It can be seen that the gain of the integrator decreases with the increasing frequency so, the integrator circuit does not have any high frequency problem.
- However, at low frequencies such as at dc, the gain becomes infinite.
- Hence the op-amp saturates (ie., the capacitor is fully charged and it behaves like an open circuit).
- A practical integrator circuit is shown in Fig. 17.
- Both stability and the low frequency roll off problems can be corrected by addition of the resistor R_F

Integrator (Cont.)

$V_1 = 0$, as $V_1 = V_2 \Rightarrow V_2 = 0$

(assumption-ii)

$I_B^- = 0$ (assumption-i)

- Applying KCL at point at V_2

$I_1 = I_2 + I_3 + I_B^-$

$$\Rightarrow \frac{V_{in} - V_2}{R_1} = \frac{(V_2 - V_0)}{\frac{1}{sC_F}} + \frac{(V_2 - V_0)}{R_F}$$

$$\Rightarrow \frac{V_{in}}{R_1} = -V_0\, sC_F - \frac{V_0}{R_F}$$

$$\Rightarrow \frac{V_{in}}{R_1} = -V_0 \left(\left(\frac{1 + sC_F R_F}{R_F}\right)\right.$$

$$\Rightarrow \frac{V_0(s)}{V_{in}(s)} = \frac{-R_F}{R_1}\left(\frac{1}{1 + sC_F R_F}\right)$$

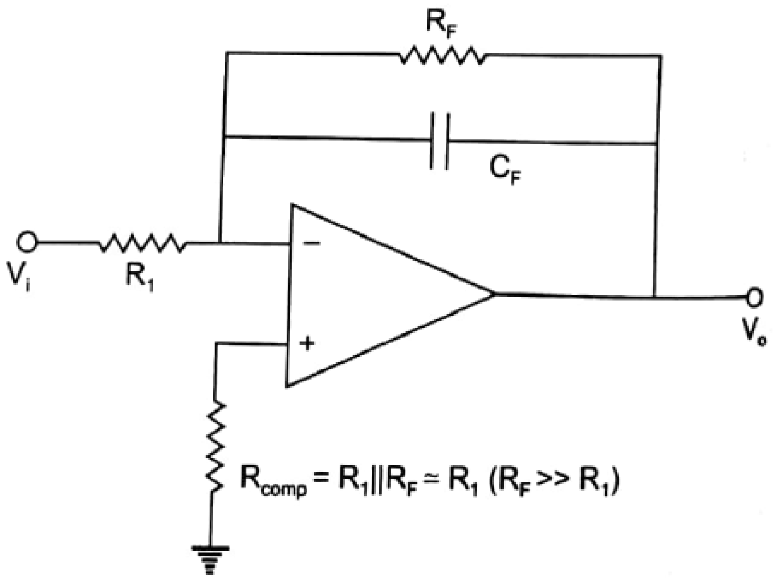


Fig. Practical integrator

Integrator (Cont.)

$$\frac{V_0(s)}{V_{in}(s)} = \frac{-R_F}{R_1}\left(\frac{1}{1+sC_FR_F}\right)$$

$$=> \frac{V_0(jw)}{V_{in}(jw)} = \frac{-R_F}{R_1}\left(\frac{1}{1+jwC_FR_F}\right)$$

$$=> |A| = \left|\frac{V_0(jw)}{V_{in}(jw)}\right| = \frac{R_F}{R_1}\left(\frac{1}{\sqrt{1+(wC_FR_F)^2}}\right)$$

At -3 dB cut off frequency, the gain is 0.707 $\frac{R_F}{R_1}$

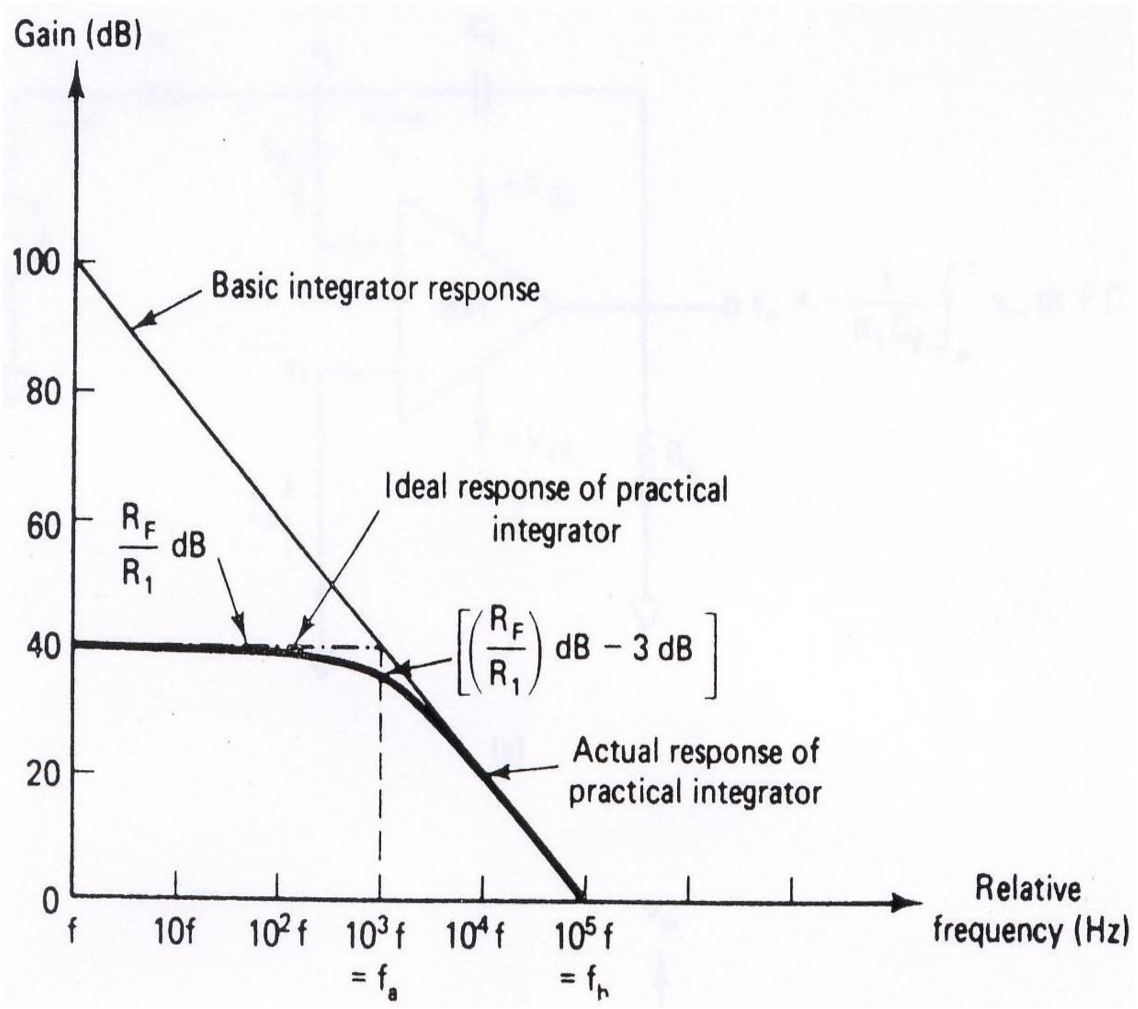
$$\Rightarrow \sqrt{1+(wC_FR_F)^2} = \sqrt{2}$$

$$\Rightarrow wC_FR_F = 1 => 2\pi f_a\, C_FR_F = 1$$

$$\Rightarrow f_a = \frac{1}{2\pi C_FR_F}$$

Integrator (Cont.)

- At input frequency is equal to f_a, 50% accuracy results.
- If input frequency 10 times f_a, then 99% accuracy can result.



Frequency response of integrator

Differentiator

- A circuit in which output voltage waveform is the differentiation of the input voltage waveform is differentiator.
- The differentiator circuit is shown in Fig

$V_1 = 0$, as $V_1 = V_2 \Rightarrow V_2 = 0$

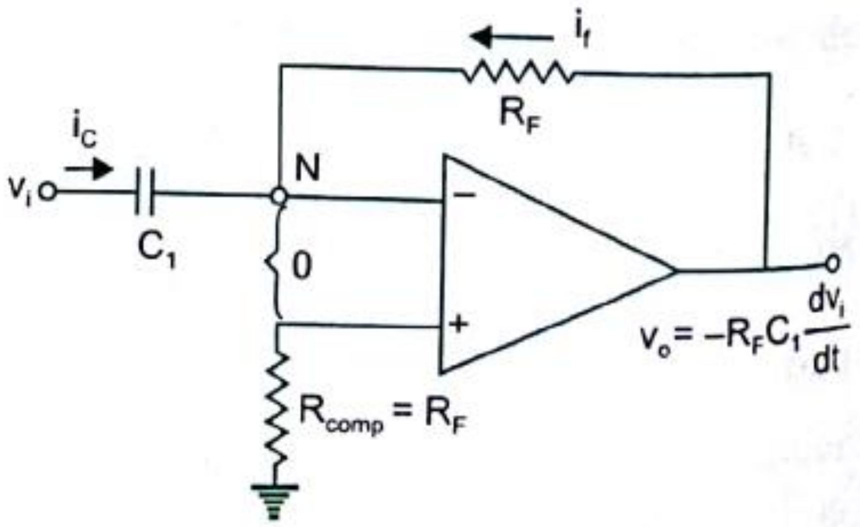
(assumption-ii)

I_3=0   (assumption-i)

- Applying KCL at point at A

$I_1 = I_2 + I_3$

$$\Rightarrow c_1 \frac{d(V_{in}-V_2)}{dt} = \frac{V_2 - V_0}{R_F} \Rightarrow V_0 = -c_1 R_F \frac{d(V_{in})}{dt}$$

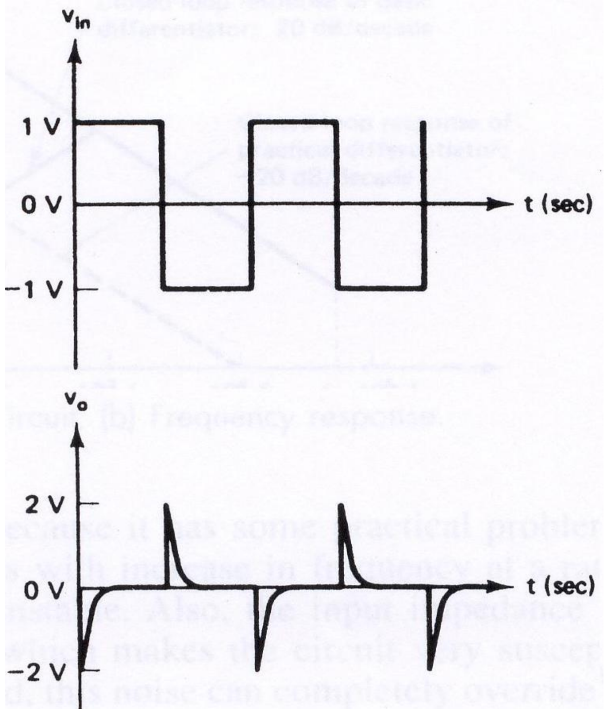


Differentiator

Differentiator (Cont.)

- For sinewave input, output will be cosine wave.
- If input is square wave, output will be spike.

Input and Output waveforms



Differentiator (Cont.)

- In phasor notation, considering impedance value of C_1 is $\frac{1}{sC_1}$

$V_1 = 0$, as $V_1 = V_2 \Rightarrow V_2 = 0$ (assumption-ii)

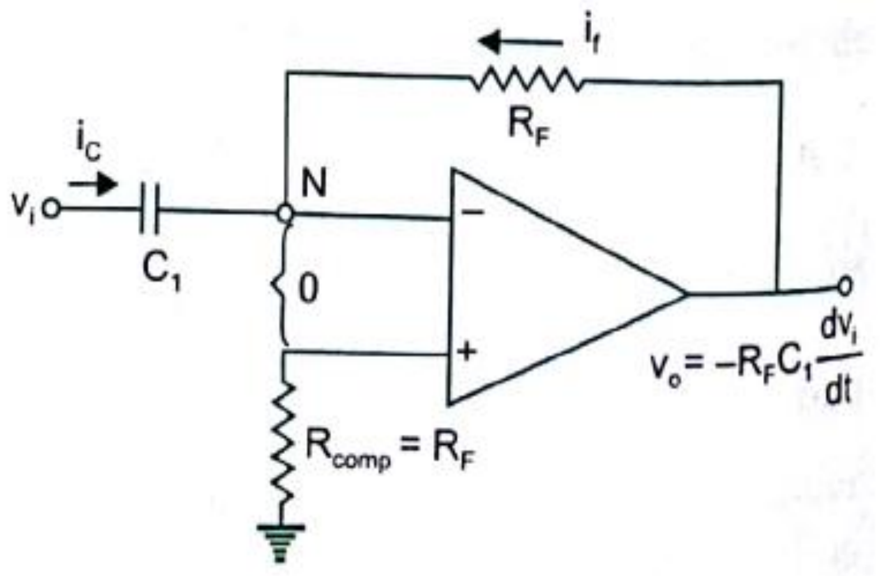
$I_3=0$ (assumption-i)

- Applying KCL at point at A

$I_1 = I_2 + I_3$

$\Rightarrow \frac{(V_{in} - V_2)}{\frac{1}{sc_1}} = \frac{V_2 - V_0}{R_F}$

$\Rightarrow V_0 = -sc_1 R_F V_{in}$



Differentiator

Differentiator (Cont.)

=> $V_0 = -sc_1 R_F V_{in}$

=> $\frac{V_0(s)}{V_{in}(s)} = -sc_1 R_F$

$\Rightarrow \frac{V_0(jw)}{V_{in}(jw)} = A = -jwc_1 R_F$

=> $|A| = |-jwc_1 R_F| = wc_1 R_F$

As, $w = 2\pi f_c$

$\Rightarrow 2\pi f_c \; c_1 R_F = |A|$

$\Rightarrow f_c = \frac{|A|}{2\pi \; c_1 R_F}$

Differentiator (Cont.)

- The frequency at which gain 0 dB, Here |A|=1.

$$\Rightarrow f_a = \frac{1}{2\pi\, c_1 R_F}$$

- For proper differentiation, RC has to be much smaller than the time period of the input signal.
- It can be seen that at high frequencies a differentiator may become unstable and break into oscillation.
- Also, the input impedance of the differentiator decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.
- So, in order to limit the gain of the differentiator at high frequencies, the input capacitor is connected in series with a resistance R_1 and hence avoiding high frequency noise and stability problems.

Differentiator (Cont.)

$V_1 = 0$, as $V_1 = V_2 \Rightarrow V_2 = 0$

(assumption-ii)

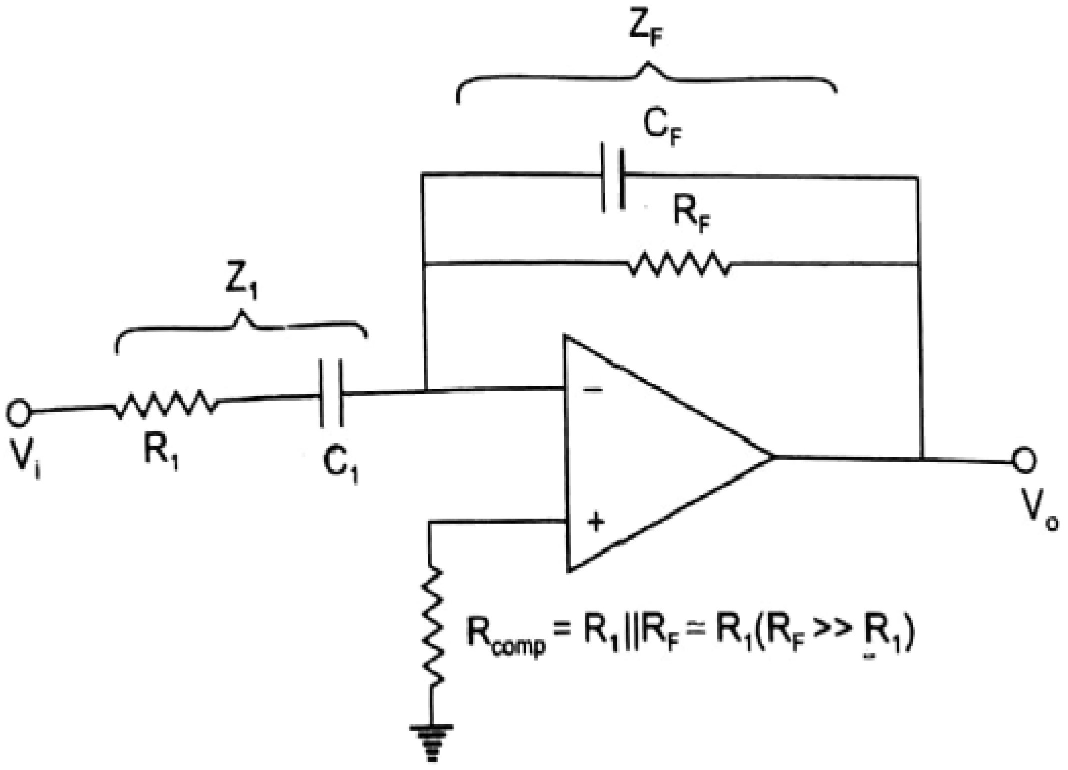
$I_B^- = 0$ (assumption-i)

- Applying KCL at point at V_2

$I_1 = I_2 + I_3 + I_B^-$

$$\Rightarrow \frac{(V_{in} - V_2)}{R_1 + \frac{1}{sc_1}} = \frac{V_2 - V_0}{R_F} + \frac{V_2 - V_0}{\frac{1}{sc_F}}$$

$$\Rightarrow \frac{V_{in}}{\frac{R_1 sc_1 + 1}{sc_1}} = -V_0\left(\frac{1 + sR_F C_F}{R_F}\right)$$



Practical differentiator

Differentiator (Cont.)

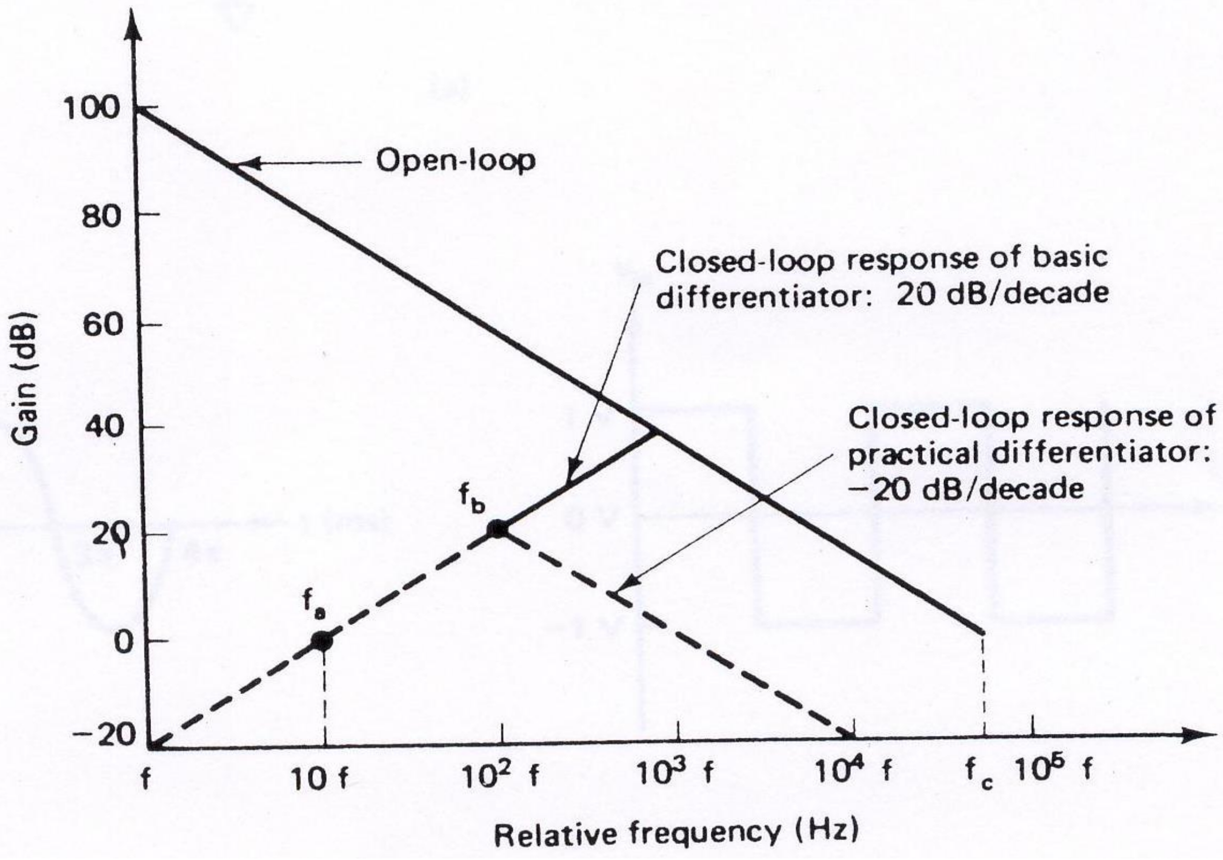
$$\frac{V_0(s)}{V_{in}(s)} = \frac{-R_F s c_1}{(1+\frac{jf}{f_b})^2}$$

So, gain increases at 20 dB/decade for $f < f_b$

And decreases -20 dB/decade for $f > f_b$

For good differentiation, time period T of the input signal is larger than or equal to $R_F c_1$

$T \geq R_F c_1$

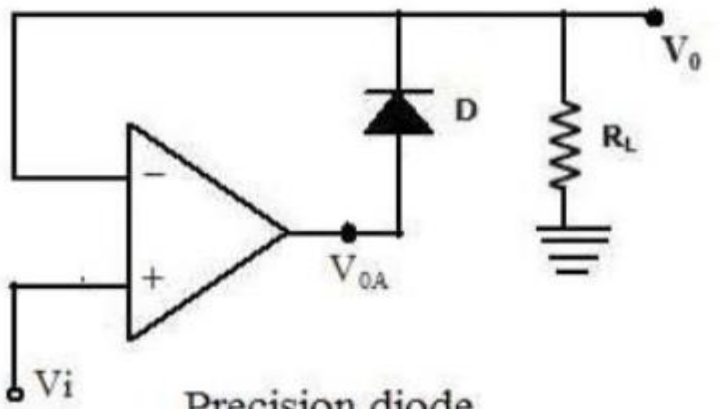


Frequency Response of Practical Differentiator Circuit

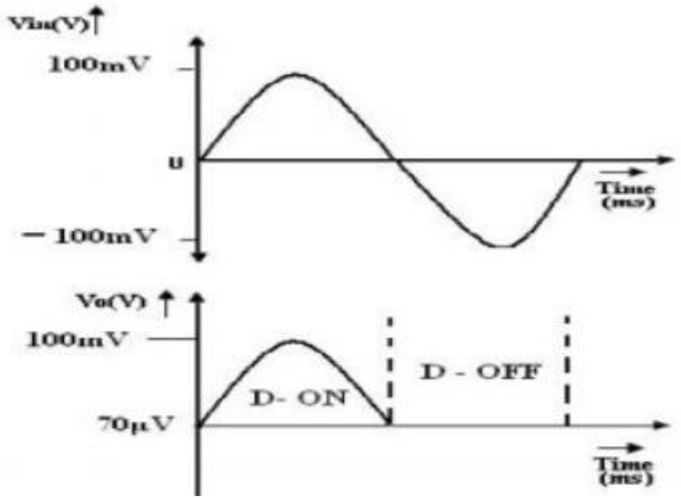
Unit II Part II

Precision Diode

- The ordinary diodes cannot rectify voltages below the cut-in -voltage of the diode. A circuit which can act as an ideal diode or precision signal – processing rectifier circuit for rectifying voltages which are below the level of cut-in voltage of the diode can be designed by placing the diode in the feedback loop of an op-amp
- Figure shows the arrangement of a precision diode. It is a single diode arrangement and functions as a non-inverting precision half– wave rectifier circuit. If V_1 in the circuit of figure is positive, the op-amp output V_{OA} also becomes positive. Then the closed loop condition is achieved for the op-amp and the output voltage V_0 = Vi . When Vi < 0, the voltage V_{0A} becomes negative and the diode is reverse biased. The loop is then broken and the output $V_0 = 0$.



Precision diode



- Consider the open loop gain AOL of the op-amp is approximately 10^4 and the cut-in voltage Vγ for silicon diode is ≈ 0.7V. When the input voltage Vi > Vγ / AOL, the output of the op-amp V_{OA} exceeds Vγ and the diode D conducts.
- Then the circuit acts like a voltage follower for input voltage level $V_i >$ V_γ / AOL ,(i.e. when $V_i > 0.7/10^4 = 70\mu V$), and the output voltage V_0 follows the input voltage during the positive half cycle for input voltages higher than 70μV as shown in figure.
- When Vi is negative or less than V_γ / A_{OL}, the output of op-amp V_{OA} becomes negative, and the diode becomes reverse biased. The loop is then broken, and the op-amp swings down to negative saturation. However, the output terminal is now isolated from both the input signal and the output of the op-amp terminal thus V_0 =0.
- No current is then delivered to the load RL except for the small bias current of the op-amp and the reverse saturation current of the diode.
- This circuit is an example of a non-linear circuit, in which linear operation is achieved over the remaining region ($V_i < 0$). Since the output swings to negative saturation level when $V_i < 0$, the circuit is basically of saturating form. Thus the frequency response is also limited.

Applications: The precision diodes are used in

Half wave rectifier,

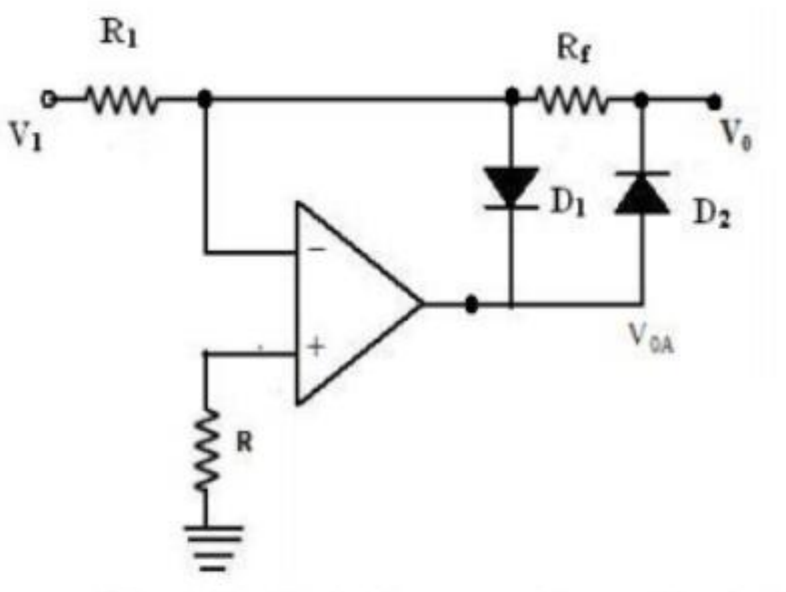
Full-wave rectifier,

Peak value detector,

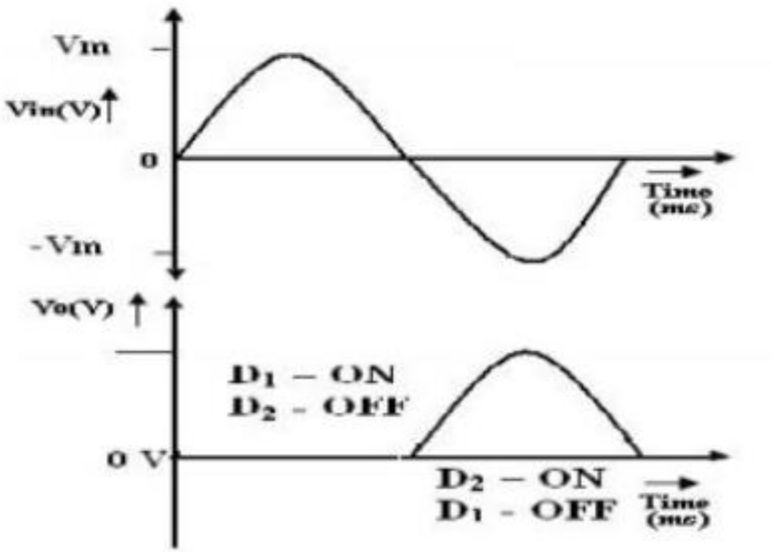
Clipper and clamper circuits.

Half wave Rectifier

- A non-saturating half wave precision rectifier circuit is shown in figure. When $V_i > 0V$, the voltage at the inverting input becomes positive, forcing the output V_{OA} to go negative. This results in forward biasing the diode D_1 and the op-amp output drops only by $\approx 0.7V$ below the inverting input voltage. Diode D_2 becomes reverse biased. The output voltage V_0 is zero when the input is positive.
- When $V_i > 0$, the op-amp output V_{OA} becomes positive, forward biasing the diode D_2 and reverse biasing the diode D_1. The circuit then acts like an inverting amplifier circuit with a non-linear diode in the forward path. The gain of the circuit is unity when $R_f = R_i$.



Non - Saturating half - wave precision rectifier circuit



Input and Output Waveforms

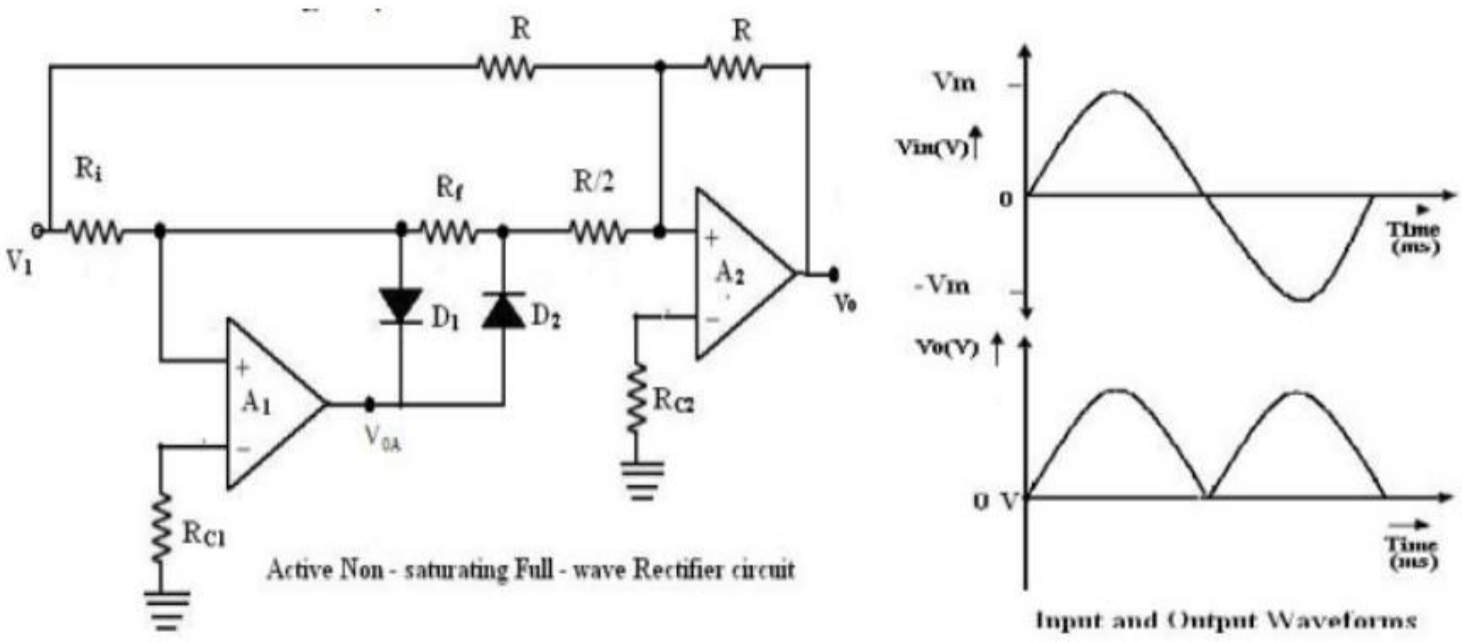
- The circuit operation can mathematically be expressed as
- $V_0 = 0$ when $V_i > 0$ and
- $V_0 = R_f/R_i V_1$ for$V_i < 0$
- The voltage V_{oA} at the op amp output is $V_{OA} = -0.7V$ for $V_i>0$
- $V_{OA}= R_f/R_i\ V_1 + 0.7V$ for$V_i<0$

Advantages:

- It is a precision half wave rectifier and
- It is a non saturating one.
- The inverting characteristics of the output V0 can be circumvented by the use of an additional inversion for achieving a positive output.

Full wave Rectifier

- The first part of the Full wave circuit is a half wave rectifier circuit. The second part of the circuit is an inverting amplifier.



Active Non - saturating Full - wave Rectifier circuit

Input and Output Waveforms

For positive input voltage V_i > 0V and assuming that R_F =R_i = R, the output voltage V_{OA}=V_i. The voltage V_0 appears as (-) input to the summing op-amp circuit formed by A_2, The is R/(R/2), as shown in figure.

- The input Vi also appears as an input to the summing amplifier. Then, the net output is V_0=-V_i -2V_0= -V_i -2(-V_i) = Vi. Since V_i > 0V, V_0 will be positive, with its input output characteristics in first quadrant. For negative input Vi < 0V, the output V‘0 of the first part of rectifier circuit is zero. Thus, one input of the summing circuit has a value of zero. However, Vi is also applied as an input to the summer circuit formed by the op-amp A2.
- The gain for this input id (-R/R) = -1, and hence the output is V_0 = -Vi. Since Vi is negative, V_0 will be inverted and will thus be positive. This corresponds to the second quadrant of the circuit.
- To summarize the operation of the circuit,
- $V_0 = V_i$ when $V_i < 0V$ and
- $V_0 = V_i$ for $V_i > 0V$, and hence
- $V_0 = |V_i|$

Wave Shaping Circuits
(Clipper and Clampers)

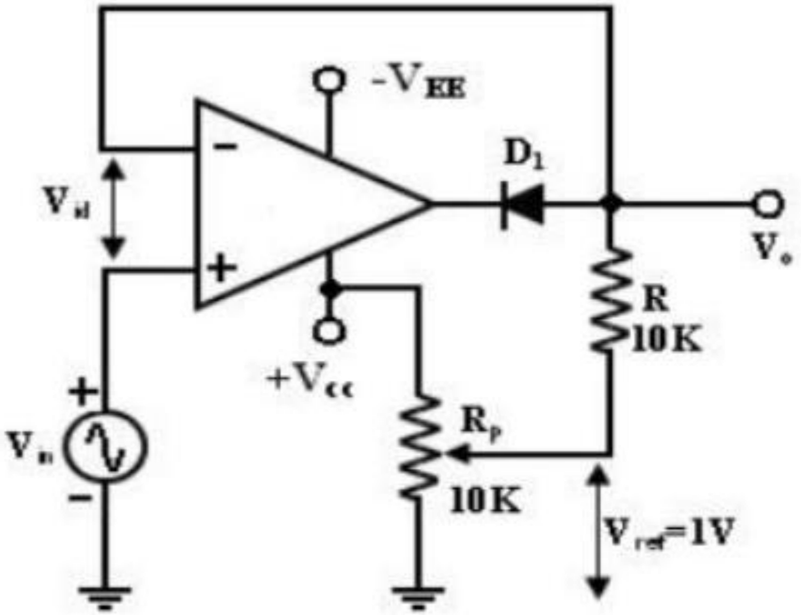
- Wave shaping circuits are commonly used in digital computers and communication such as TV and FM receiver.
- Wave shaping technique include clipping and clamping.
- In op-amp clipper circuits a rectifier diode may be used to clip off a certain portion of the input signal to obtain a desired o/p waveform.
- The diode works as an ideal diode (switch) because when on, the voltage drop across the diode is divided by the open loop gain of the op-amp. When off (reverse biased) the diode is an open circuit. In an op-amp clamper circuits, however a predetermined dc level is deliberately inserted in the o/p volt. For this reason, the clamper is sometimes called a dc inverter.

Clipper: Positive Clipper

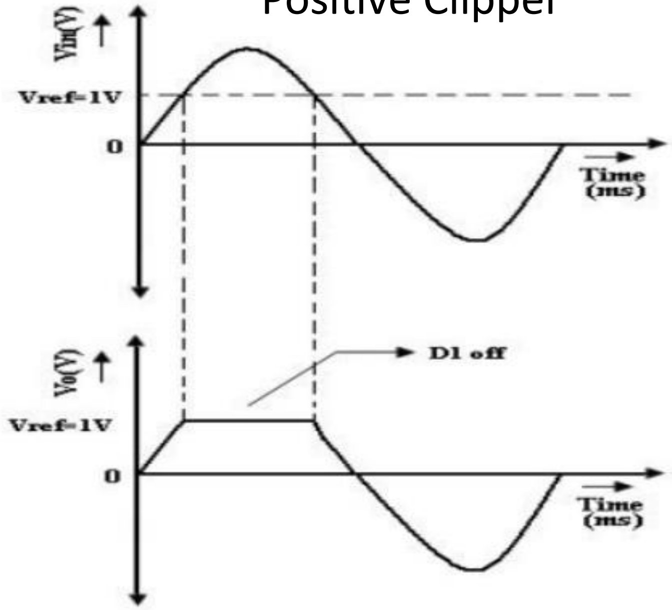
- A circuit that removes positive parts of the input signal can be formed by using an op-amp with a rectifier diode. T he clipping level is determined by the reference voltage V_{ref}, which should less than the i/p range of the op-amp ($V_{ref} < V_{in}$). The Output voltage has the portions of the positive half cycles above Vref clipped off.

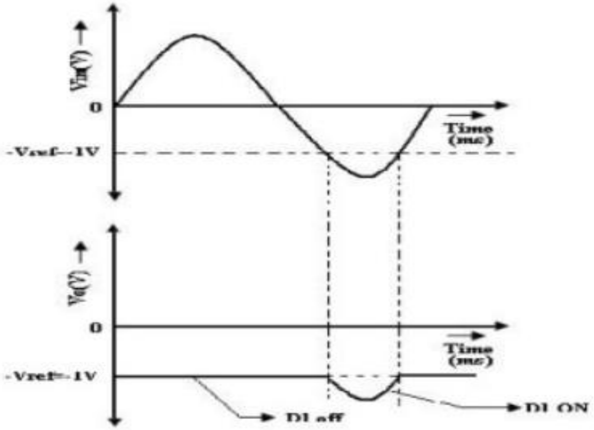
WORKING

- During the positive half cycle of the input, the diode D_1 conducts only until $V_{in} = V_{ref}$. This happens because when $V_{in} < V_{ref}$, the output volts V_0 of the op-amp becomes negative to device D_1 into conduction when D_1 conducts it closes feedback loop and op-amp operates as a voltage follower. (i.e.) Output V0 follows input until $V_{in} = V_{ref}$.
- When $V_{in} > V_{ref}$ => the V_0 becomes +ve to derive D_1 into off. It opens the feedback loop and op- amp operates open loop. When V_{in} drops below V_{ref} ($V_{in}<V_{ref}$) the o/p of the op-amp V_0 again becomes –ve to device D_1 into conduction. It closes the feedback path. (o/p follows the i/p).
- Thus diode D_1 is on for $v_{in}<V_{ref}$ (o/p follows the i/p) and D_1 is off for $V_{in}>V_{ref}$.
- The op-amp alternates between open loop (off) and closed loop operation as the D_1 is turned off and on respectively. For this reason the op-amp used must be high speed and preferably compensated for unity gain.



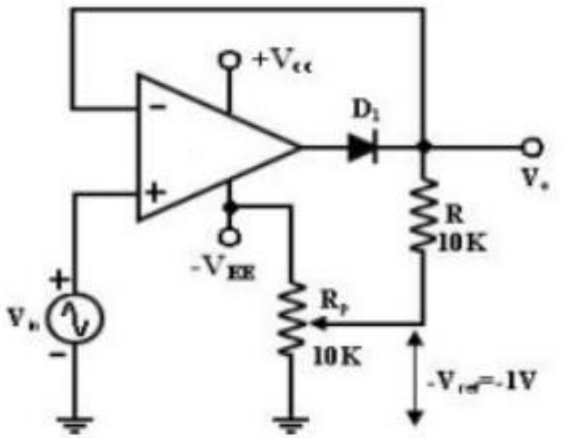
Positive Clipper



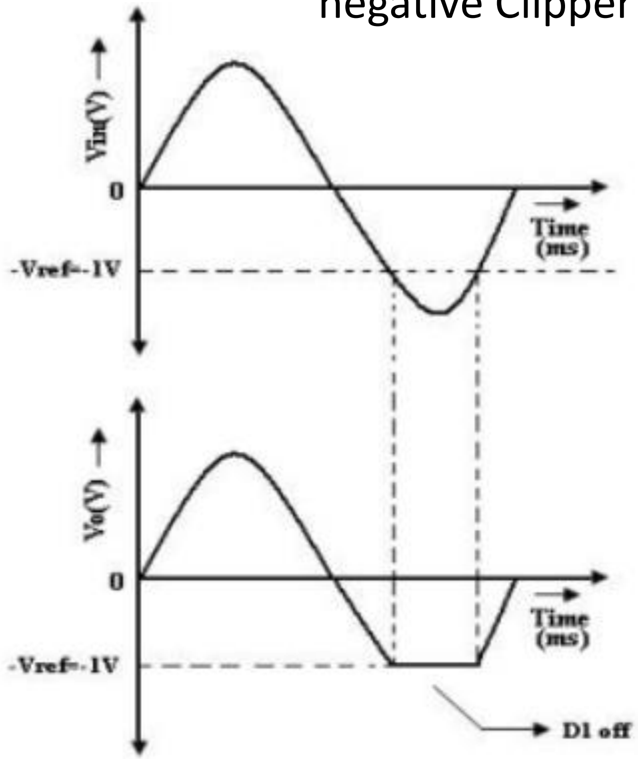


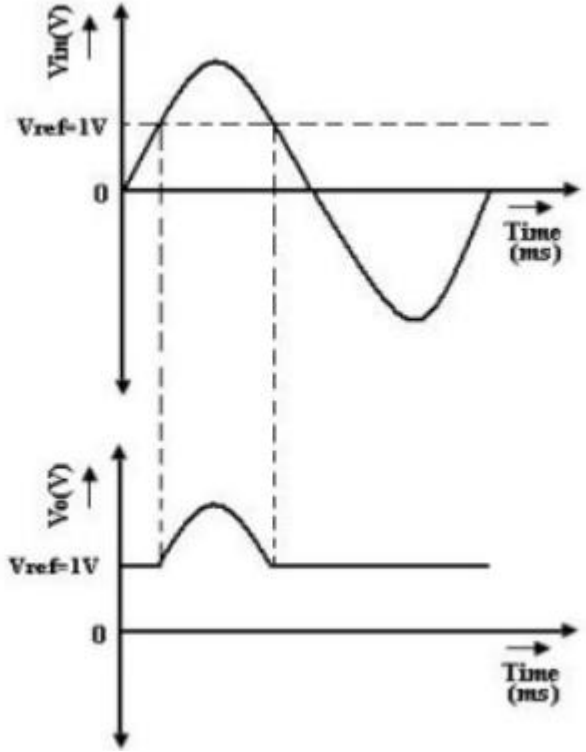
Negative Clipper

- The positive clipper is converted into a –ve clipper by simply reversing diode D_1 and changing the polarity of V_{ref} voltage. The negative clipper clips off the –ve parts of the input signal below the reference voltage.
- Diode D_1 conducts -> when $V_{in} > -V_{ref}$ and therefore during this period o/p volt V0 follows the i/p volt Vin.
- The –Ve portion of the output volt below –Vref is clipped off because (D_1 is off) $V_{in}<-V_{ref}$. If $-V_{ref}$ is changed to $-V_{ref}$ by connecting the potentiometer R_p to the $+V_{cc}$, the V_0 below $+V_{ref}$ will be clipped off.
- The diode D1 must be on for $V_{in} > V_{ref}$ and off for V_{in}.



negative Clipper





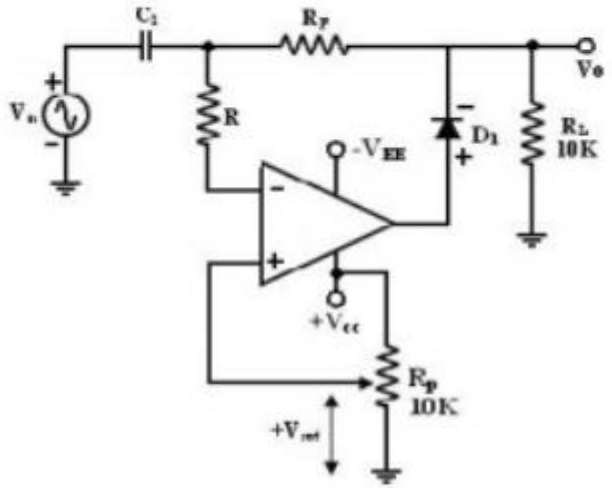
Clampers

- In clamper circuits a predetermined dc level is added to the output voltage. (or) The output is clamped to a desired dc level.

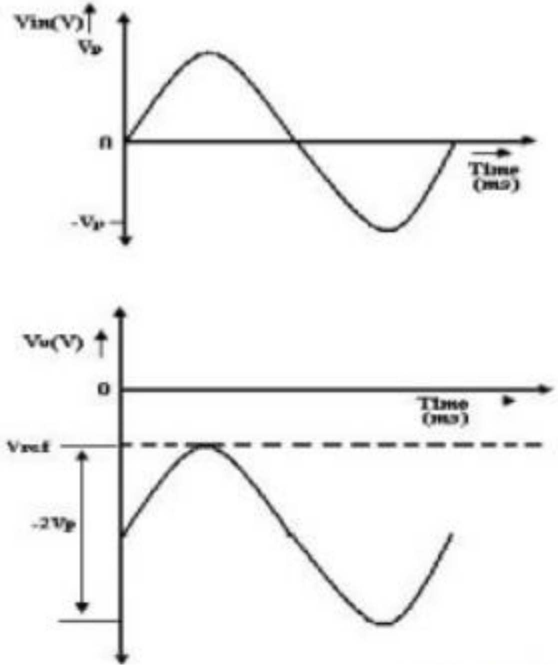
1. If the clamped dc level is +ve, the clamper is positive clamper

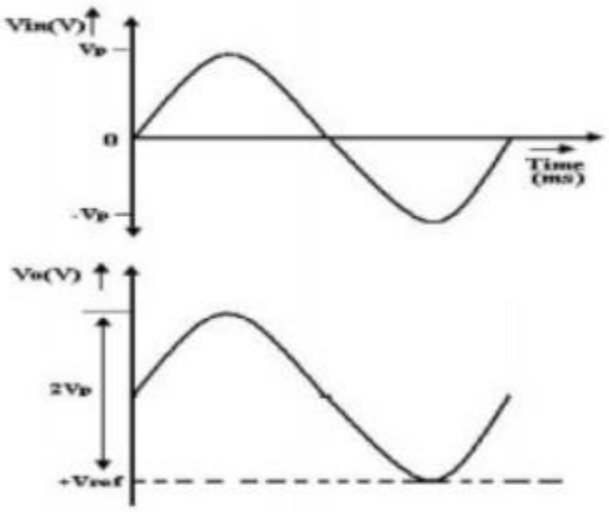
2. If the clamped dc level is –ve, the clamper is negative clamper.

Other equivalent terms used for clamper are dc inserter or restorer. Inverting and Non-Inverting that uses this technique.


C1
Rf
Vo
R
Vs
-VEE
D1
RL
10K
+Vcc
Rp
10K
+Vref

Clamper


Vin(V)
Vp
0
-Vp
Time
(ms)
Vo(V)
0
Time
(ms)
Vref
-2Vp


Vin(V)
Vp
0
-Vp
Time
(ms)
Vo(V)
2Vp
+Vref

- In this circuit, the input waveform peak is clamped at Vref. For this reason, the circuit is called the peak clamper.
- First consider the input voltage Vref at the (+) input: since this volt is +ve, V‘0 is also +ve which forward biases D_1. This closed the feedback loop.
- Voltage V_{in} at the (-) input: During its –ve half cycle, diode D_1 conducts, charging c; to the –ve peak value of V_p. During the +ve half cycle, diode D1 in reverse biased. Since this voltage Vp is in series with the +ve peak volt Vp the o/p volt V0 = 2 Vp. Thus the nett o/p is Vref plus 2 Vp. So the – ve peak of 2 Vp is at Vref. For precision clamping, $C_i R_d << T/2$

Where R_d = resistance of diode D_1 when it is forward biased.

T = time period of the input waveform.

- Resistor R is used to protect the op-amp against excessive discharge currents from capacitor Ci especially when the dc supply voltages are switched off. A +ve peak clamping is accomplished by reversing D1 and using –ve reference voltage ($-V_{ref}$).

Log and Antilog Amplifiers

- There are several applications of log and antilog amplifiers. Antilog computation may require functions such as *ln x, log x or sinh x*.

- These can be performed continuously with log-amps. Log-amp can easily perform this function.

Log Amplifier

- The fundamental log-amp circuit is shown in Fig.a where a grounded base resistor is placed in the feedback path.
- The transistor's voltage-current relationship is given by,

$$I_E = I_s(e^{qV_E/kT} - 1)$$

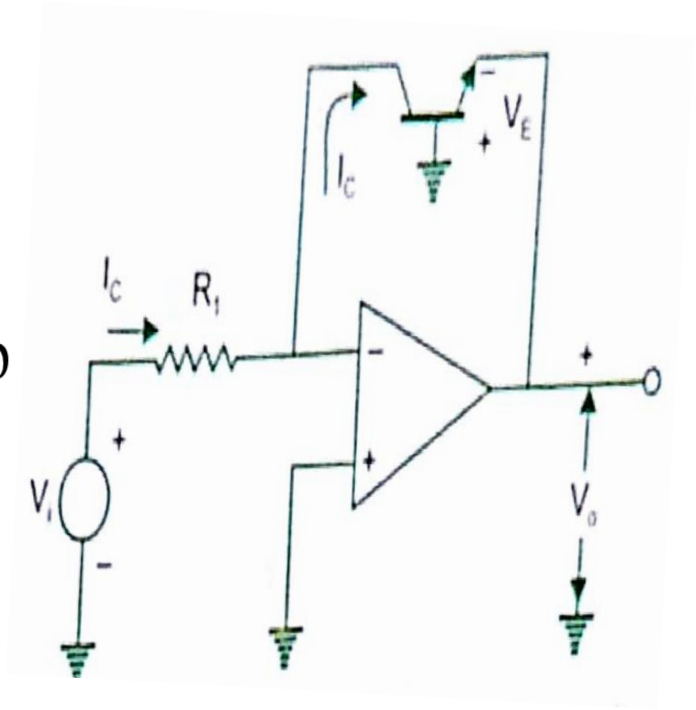


Fig.(a) Fundamental log-amp circuit

Since, $I_C = I_E$ for a grounded base transistor,

$$I_C = I_s(e^{qV_E/kT} - 1)$$

I_s = emitter saturation current $= 10^{-13}$ A

k = Boltzmann's Constant

T = absolute temperature (in $^\circ$K)

Therefore,

$$\frac{I_C}{I_S} = (e^{qV_E/kT} - 1)$$

Or

$$e^{qV_E/kT} = \frac{I_C}{I_S} + 1$$

$$= \frac{I_C}{I_S} \qquad [\text{as } I_s \approx 10^{-13}\ A, I_c \gg I_s]$$

Taking natural log on both sides, we get

$$V_E = \frac{kT}{q}\ln\left(\frac{I_c}{I_s}\right)$$

Also in Fig.a, $I_c = \frac{V_i}{R_1}$

$$V_E = -V_o$$

So, $V_o = -\frac{kT}{q}\ln\left(\frac{V_i}{R_1 I_s}\right) = -\frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$

Where

$$V_{ref} = R_1\, I_s$$

- The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log (ln), one can find log_{10} by proper scaling

$$log_{10}X = 0.4343 \ln X$$

- The circuit, however, has one problem. The emitter saturation current I_s varies from transistor to transistor and with temperature. Thus a stable reference voltage V_{ref} cannot be obtained. This is eliminated by the circuit given in Fig.b.

- The input is applied to one log-amp, while a reference voltage is applied to another log-amp.

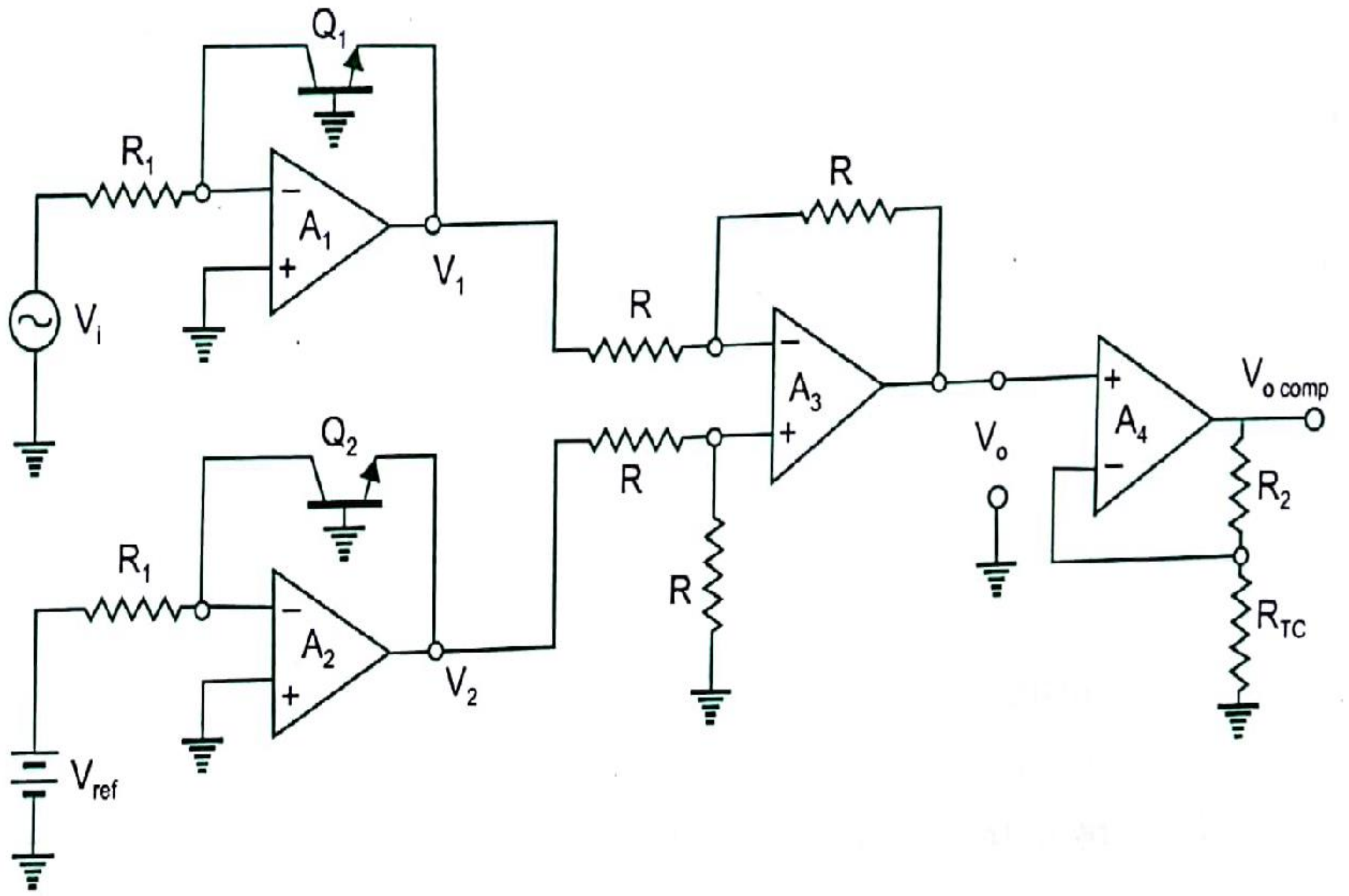


Fig.(b) Log-amp with saturation current and temperature compensation

Assume, $$I_{s1} = I_{s2} = I_s$$

and then, $$V_1 = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right)$$

and $$V_2 = -\frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

Now, $$V_o = V_2 - V_1 = \frac{kT}{q} \left[\ln\left(\frac{V_i}{R_1 I_s}\right) - \ln\left(\frac{V_{ref}}{R_1 I_s}\right)\right]$$

or, $$V_o = \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

- Thus reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed. The voltage V_o is still dependent upon temperature and is directly proportional to T.
- This is compensated by the last op-amp stage A_4 which provides a non-inverting gain of $\left(1 + \frac{R_2}{R_{TC}}\right)$. Now, the output voltage is,

$$V_{o\,comp} = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

where R_{TC} is a temperature-sensitive resistance with a positive coefficient of temperature (sensistor) so that the slope of the equation becomes constant as the temperature changes.

- The circuit in Fig.b requires four op-amps, and becomes expensive if FET op-amps are used for precision. The same output (with an inversion) can be obtained by the circuit of Fig.c using two op-amps only.

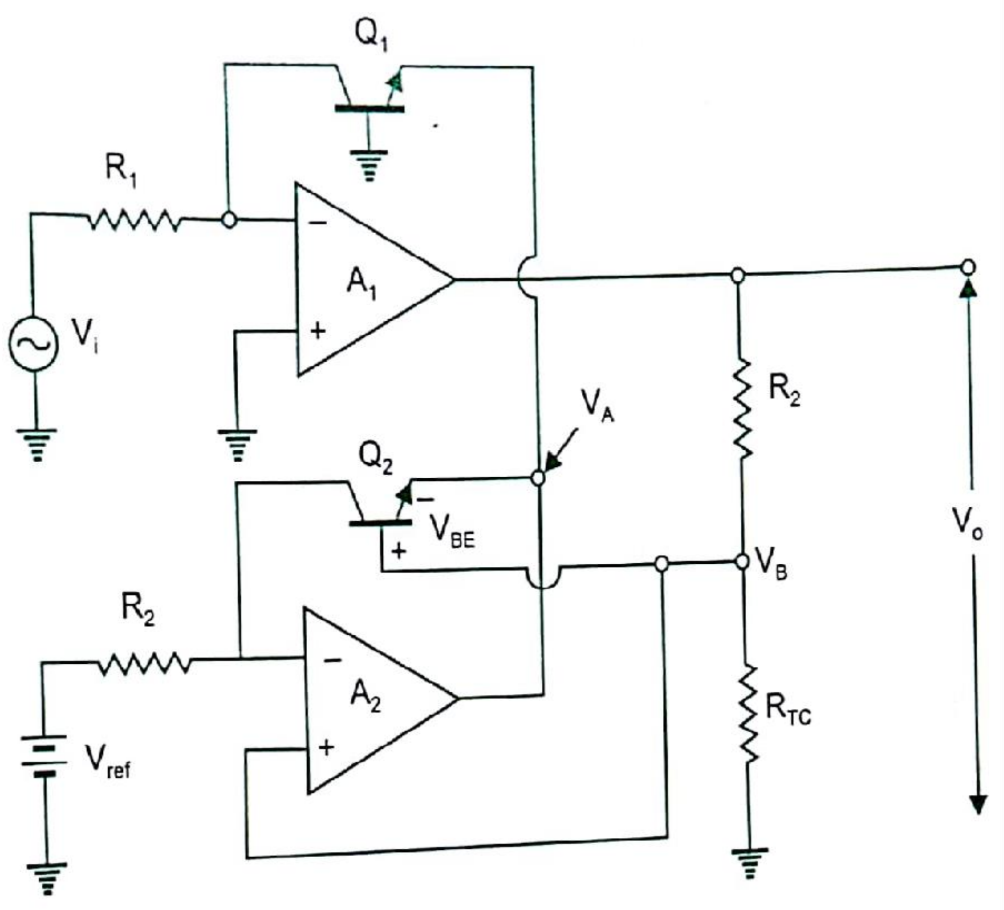


Fig.(c) Log-amp using two op-amps only

Antilog Amplifier

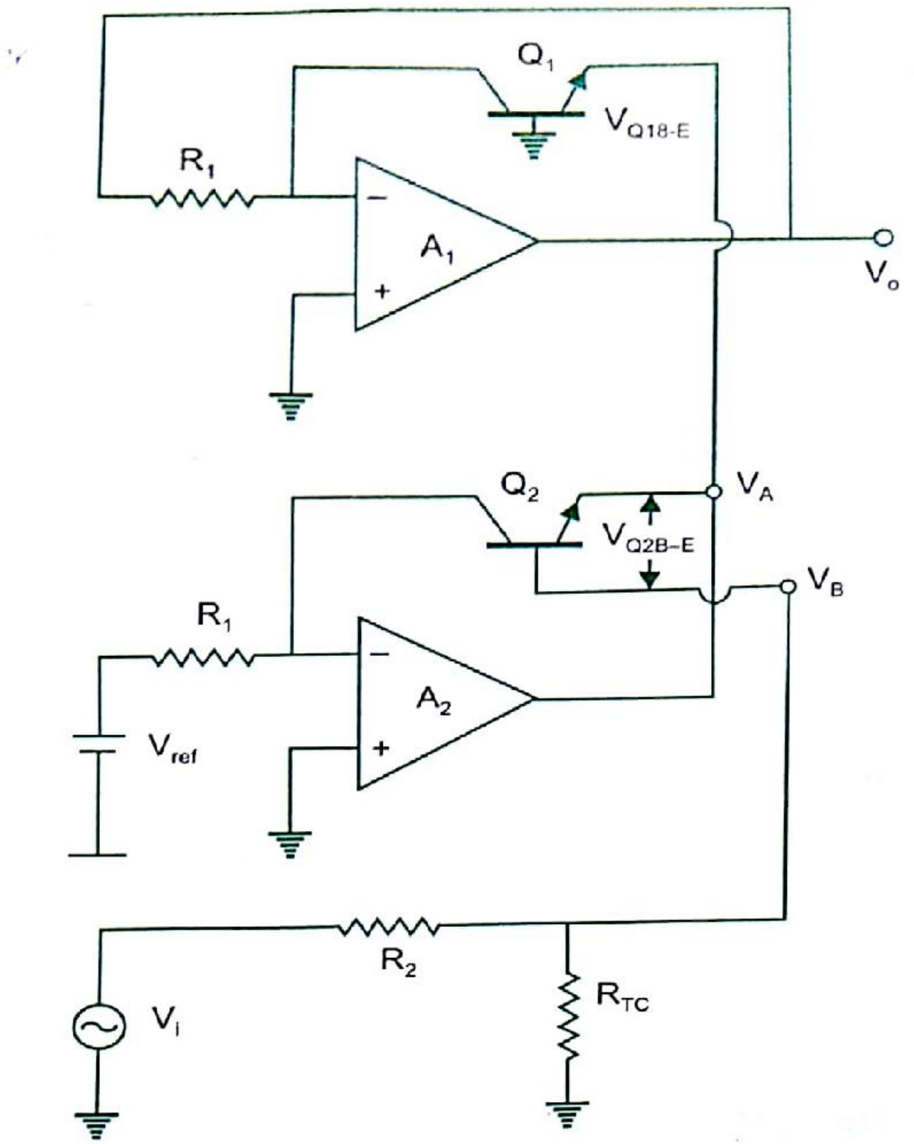


Fig.(d). Antilog Amplifier

- The antilog amplifier circuit is shown in Fig.d. The input V_i for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2.
- The output V_o of the antilog-amp is fed back to the inverting input of A_1 through the resistor R_1.
- The base to emitter voltage of transistors Q_1 and Q_2 can be written as

$$V_{Q1\ B\text{–}E} = \frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right)$$

$$V_{Q2\ B\text{–}E} = \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

Since the base of Q_1 is tied to ground, we get

$$V_A = -V_{Q1\ B\text{–}E} = -\frac{kT}{q}\ln\left(\frac{V_o}{R_1 I_s}\right)$$

The base voltage V_B of Q_2 is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i$$

The voltage at the emitter of Q_2 is

$$V_{Q2\ B\text{-}E} = V_B + V_{Q2\ E\text{-}B}$$

or,

$$V_{Q2\ B\text{-}E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i - \frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

But the emitter voltage of Q_2 is V_A, that is,

$$V_A = V_{Q2\ \text{B-E}}$$

or,

$$-\frac{kT}{q}\ln\frac{V_o}{R_1 I_s} = \frac{R_{TC}}{R_2 + R_{TC}}V_i - \frac{kT}{q}\ln\frac{V_{ref}}{R_1 I_s}$$

or,

$$\frac{R_{TC}}{R_2 + R_{TC}}V_i = -\frac{kT}{q}\left(\ln\frac{V_o}{R_1 I_s} - \ln\frac{V_{ref}}{R_1 I_s}\right)$$

or,

$$-\frac{q}{kT}\frac{R_{TC}}{R_2+R_{TC}}V_i = \ln\left(\frac{V_o}{V_{ref}}\right)$$

Changing natural log, i.e., ln to log_{10} using $log_{10}X = 0.4343 \ln X$ we get

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i = 0.4343 \times \ln\left(\frac{V_o}{V_{ref}}\right)$$

or, $$-K'V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

or, $$\frac{V_o}{V_{ref}} = 10^{-K'V_i}$$

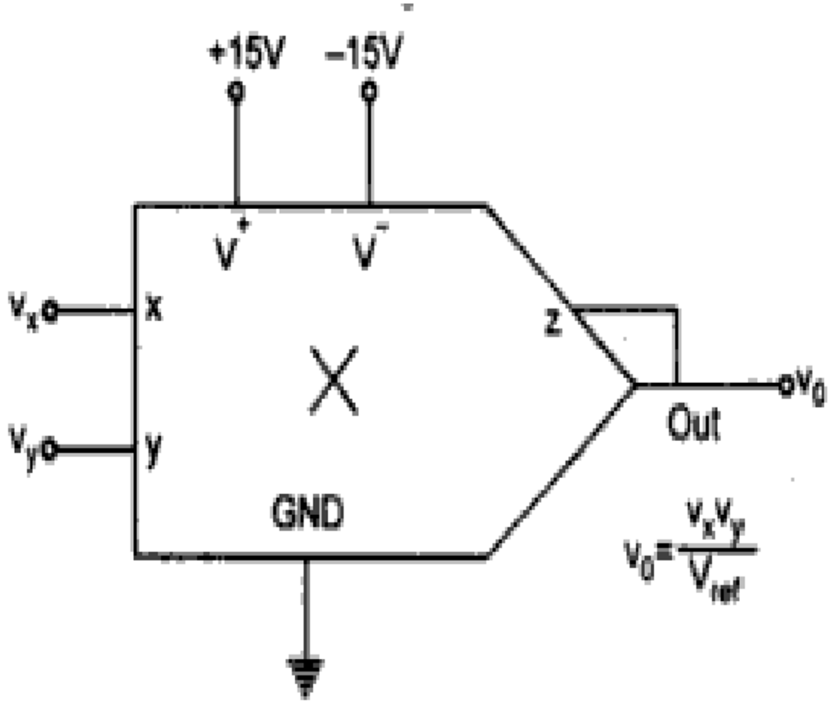
or, $$V_o = V_{ref}\,(10^{-K'V_i})$$

where $$K' = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

Hence an increase of input by one volt causes the output to decrease by a decade. The 755 log/antilog amplifier IC chip is available as a functional module which may require some external components also to be connected to it.

Analog voltage multiplier circuit and its applications

- There are a number of applications of analog multiplier such as frequency doubling, frequency shifting, phase angle detection, real power computation, multiplying two signals, dividing and squaring of signals.
- A basic multiplier symbol is shown in Fig.e. Two signal inputs (v_x and v_y) are provided. The output is the product of the two inputs divided by a reference voltage V_{ref}.



$$v_o = \frac{v_x v_y}{V_{ref}}$$

Fig.e. Multiplier Schematic Symbol

Normally, V_{ref} is internally set to 10 volts. So,

$$v_o = \frac{v_x v_y}{10}$$

As long as

$v_x < V_{ref}$ and $v_y < V_{ref}$

the output of the multiplier will not saturate.

- If both inputs are positive, the IC is said to be a one quadrant multiplier. A two quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative.
- If both inputs may be either positive or negative, the IC is called a four quadrant multiplier.

- There can be several ways to make a circuit which will multiply according to equation, $v_o = \frac{v_x v_y}{V_{ref}}$. One commonly used technique is log-antilog method.

- The log-antilog method relies on the mathematical relationship that the sum of the log of two numbers equals the log of the product of those numbers.

$$\ln v_x + \ln v_y = \ln(v_x v_y)$$

- Fig.f. shows the block diagram of a log-antilog multiplier IC. Log-amps requires the input and reference voltages to be of the same polarity. The two applications of multiplier IC will be discussed in the next section.

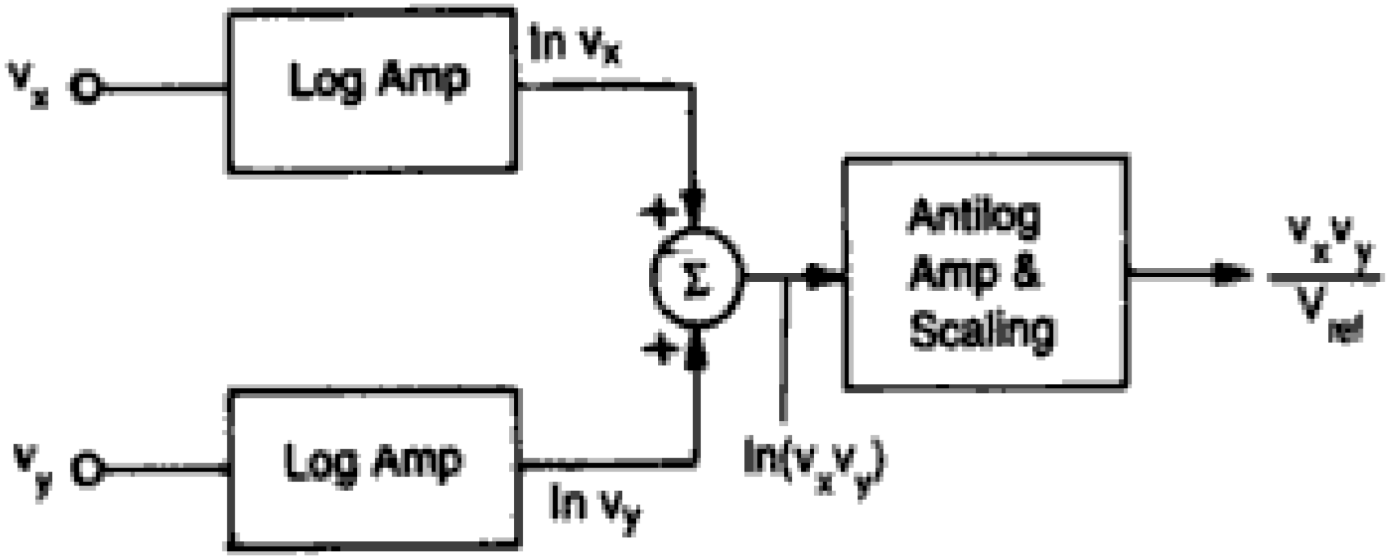


Fig.f. Block diagram of a log-antilog

(i) Frequency Doubling

The multiplication of two sine waves of the same frequency, but of possibly different amplitudes and phase allows to double a frequency and to directly measure real power. Let

$$v_x = V_x \sin \omega t$$

$$v_y = V_y \sin(\omega t + \theta)$$

where θ is the phase difference between the two signals. Applying these two signals to the inputs of a four quadrant multiplier will yield an output as,

$$v_o = \frac{V_x \sin \omega t \, V_y \sin(\omega t + \theta)}{V_{ref}}$$

$$v_o = \frac{V_x V_y}{V_{ref}} \sin \omega t \, (\sin \omega t \cos \theta + \sin \theta \cos \omega t)$$

$$= \frac{V_x V_y}{V_{ref}} (\sin^2 \omega t \cos \theta + \sin \theta \sin \omega t \cos \omega t)$$

But $$\sin^2 a = 1 - \cos^2 a$$

and $$\cos^2 a = 2 \cos^2 a - 1$$

so $$\cos^2 a = \frac{1}{2} + \left(\frac{1}{2}\right) \cos 2a$$

$$\sin^2 a = 1 - \frac{1}{2} - \left(\frac{1}{2}\right) \cos 2a = \frac{1}{2} - \left(\frac{1}{2}\right) \cos 2a$$

so $$v_o = \frac{V_x V_y}{V_{ref}} \left[\cos \theta \left(\frac{1}{2} - \left(\frac{1}{2}\right) \cos 2\, \omega t \right) + \sin \theta \sin \omega t \cos \omega t \right]$$

But, $$\sin a \cos a = \left(\frac{1}{2}\right) \sin 2a$$

Hence, $$v_o = \frac{V_x V_y}{2 V_{ref}} (\cos\theta - \cos\theta \cos 2\omega t + \sin\theta \sin 2\omega t)$$

or, $$v_o = \frac{V_x V_y}{2V_{ref}} \cos\theta + \frac{V_x V_y}{2V_{ref}} (\sin\theta \sin 2\,\omega t - \cos\theta \cos 2\,\omega t)$$

- The first term is a DC and is set by the magnitude of the signals and their phase difference. The second term varies with time, but at twice the frequency of the inputs (2ω).

(ii) Divider

- Division, the complement of multiplication, can be accomplished by placing the multiplier circuit element in the op-amp's feedback loop. The output voltage from the divider in Fig.g with input signals v_z and v_x as dividend and divisor respectively, is given by

$$v_o = -V_{ref}\frac{v_z}{v_x}$$

The result can be derived as follows. The op-amps inverting terminal is at virtual ground. Therefore,

$$I_z = I_A$$

and

$$I_z = \frac{v_z}{R}$$

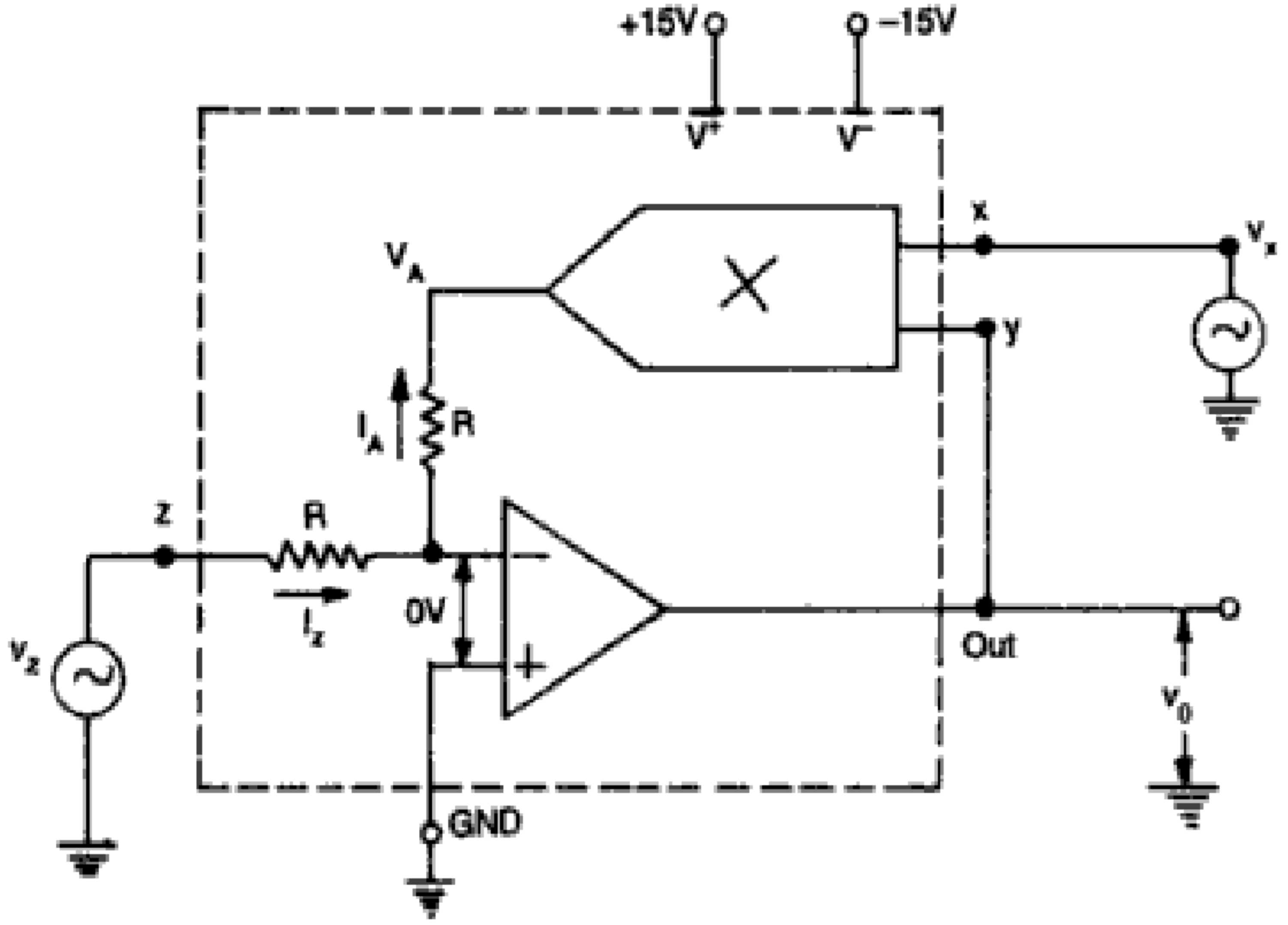


Fig.g. Multiplier IC configured as divider

The output voltage V_A of the multiplier is determined by the multiplication of v_x and v_y

$$V_A = \frac{v_x\, v_y}{V_{ref}} = \frac{v_x\, v_o}{V_{ref}}$$

$$V_A = -I_A R$$

$$I_A = -V_A/R = -\frac{v_x\, v_o}{V_{ref}\, R}$$

$$I_z = I_A$$

$$I_z = -\frac{v_x\, v_o}{V_{ref}\, R}$$

$$v_z = I_z R = -\frac{v_x v_o}{V_{ref}}$$

$$v_o = -V_{ref}\frac{v_z}{v_x}$$

- Division by zero is, of course, prohibited. Multiplier IC can be used for squaring a signal. Similarly, divider circuit can be used to take the square root of a signal.

Operational Transconductance Amplifier (OTA)

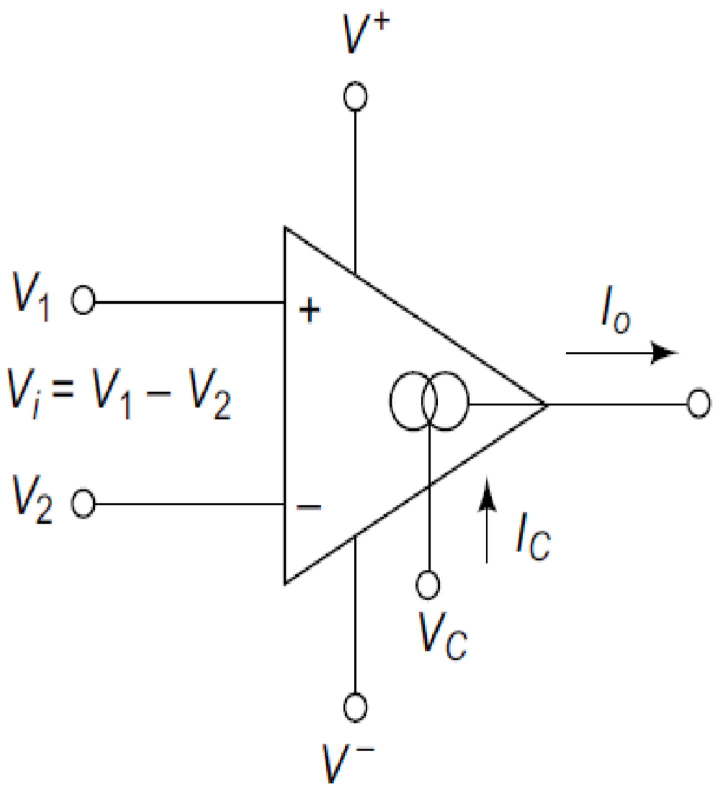


Fig.h. Schematic representation of an OTA

- A voltage to current converter is inherently an amplifier that is capable of producing a current proportional to an applied input voltage. Thus, a voltage to current converter using op-amp is an amplifier which produces an output current that is dependent on the input voltage.
- The proportionality constant of the circuit is called the transconductance of the amplifier circuit, and hence, such circuits are called transconductance amplifiers.
- Due to their wide use in a variety of applications, they are normally called programmable transconductance or operational transconductance amplifiers (PTA or OTA).
- Specially designed single chip transconductance amplifier ICs are available in the market.

- These ICs are widely used in the design of programmable amplifiers and integrators in audio processing and electronic music synthesis applications.
- They also find use as current switches in sample-and-hold applications.
- The widely used OTAs are CA3080 from RCA, LMI3600/3700 from National Semiconductor and NE5517 from Signetics.
- Fig.h shows the schematic representation of an OTA. The constant of proportionality or the transconductance is expressed as

$$I_o = g_m V_i = g_m (V_1 - V_2)$$

- In the programmable transconductance amplifier, the transconductance can be varied by changing the voltage V or current I.

Circuit diagram of OTA

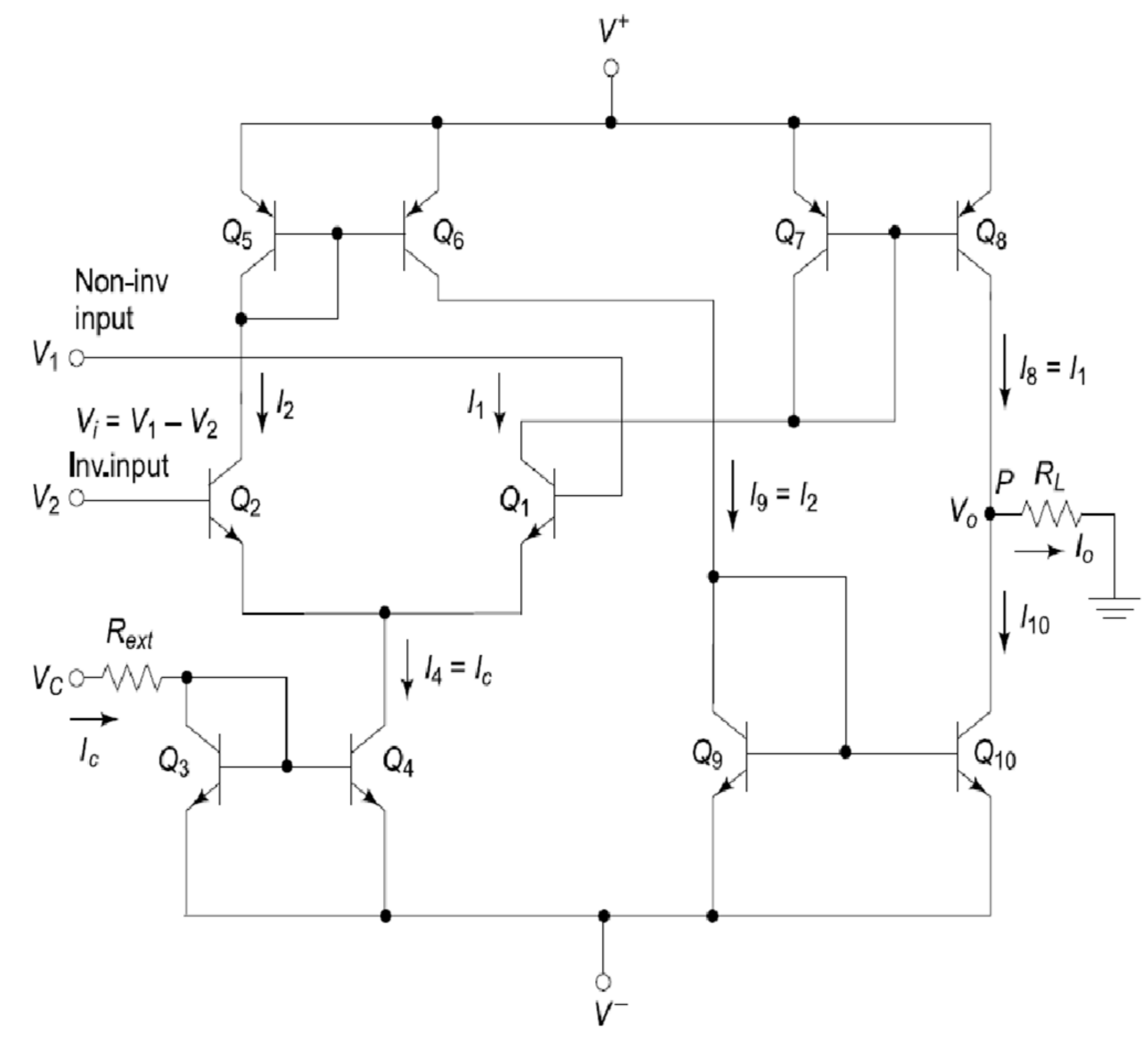


Fig.i. Simplified schematic diagram of OTA

A simplified circuit schematic of an OTA is shown in Fig.i. Using Kirchhoff 's Current Law at output node P, we get

$$I_o = I_8 - I_{10} = I_1 - I_2$$

Thus, the voltage gain A_v can be expressed as

$$A_v = \frac{V_o}{V_i} = \frac{I_o R_L}{V_i} = g_m R_L$$

The transconductance g_m of the circuit can be calculated as follows:

$$I_1 = I_S \exp\left(\frac{V_1}{V_T}\right)$$

$$I_2 = I_S \exp\left(\frac{V_2}{V_T}\right)$$

where I_S is reverse saturation current transistors Q1 and Q2 assumed to be equal and V_T is thermal voltage of the junction.

$$I_c = I_1 + I_2 = I_S\left[\exp\left(\frac{V_1}{V_T}\right) + \exp\left(\frac{V_2}{V_T}\right)\right]$$

$$I_S = \frac{I_C}{\exp\left(\frac{V_1}{V_T}\right) + \exp\left(\frac{V_2}{V_T}\right)}$$

$$I_1 = I_S \exp\left(\frac{V_1}{V_T}\right) = \frac{I_C \exp\left(\frac{V_1}{V_T}\right)}{\exp\left(\frac{V_1}{V_T}\right) + \exp\left(\frac{V_2}{V_T}\right)}$$

$$I_2 = I_S \exp\left(\frac{V_2}{V_T}\right) = \frac{I_C \exp\left(\frac{V_2}{V_T}\right)}{\exp\left(\frac{V_1}{V_T}\right) + \exp\left(\frac{V_2}{V_T}\right)}$$

$$I_1 - I_2 = \frac{I_C\left[\exp\left(\frac{V_1}{V_T}\right) - \exp\left(\frac{V_2}{V_T}\right)\right]}{\exp\left(\frac{V_1}{V_T}\right) + \exp\left(\frac{V_2}{V_T}\right)}$$

Multiplying both numerator and denominator by exp $\left[-\left(\frac{V_1 - V_2}{2}\right)\right]$

$$I_o = I_1 - I_2 = \frac{I_C\left[\exp\left(\frac{V_1 - V_2}{2V_T}\right) - \exp\left(\frac{V_1 - V_2}{2V_T}\right)\right]}{\exp\left(\frac{V_1 - V_2}{2V_T}\right) + \exp\left(\frac{V_1 - V_2}{2V_T}\right)}$$

$$= I_C \tan h\left(\frac{V_1 - V_2}{2V_T}\right)$$

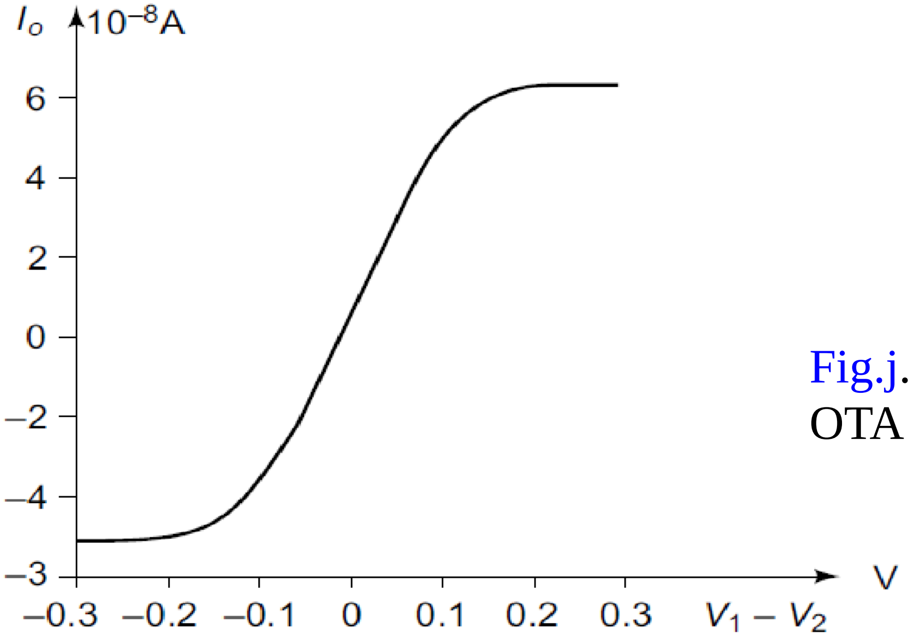


Fig.j. Transfer characteristics of OTA

A plot of output current I_o as a function of (V1 – V2) is shown in Fig.j. A transconductance amplifier basically computes a tan-hyperbolic. It operates linearly for a very small range of inputs and smoothly transits to saturation. The transconductance is given by

$$g_m = \left| \frac{\partial I_o}{\partial V_{\text{in}}} \right| = \frac{I_c}{2\,V_T}$$

with the assumption that for small difference of V1 – V2,

$$\tan h\left(\frac{V_1 - V_2}{2V_T} \right) \approx \frac{V_1 - V_2}{2V_T}$$

Then, the voltage gain A_v becomes

$$A_v = g_m R_L = \frac{I_C R_L}{2\, V_T}$$

Thus, the voltage gain of the OTA circuit can be externally controlled by the control current I_C .

Op-Amp Comparators

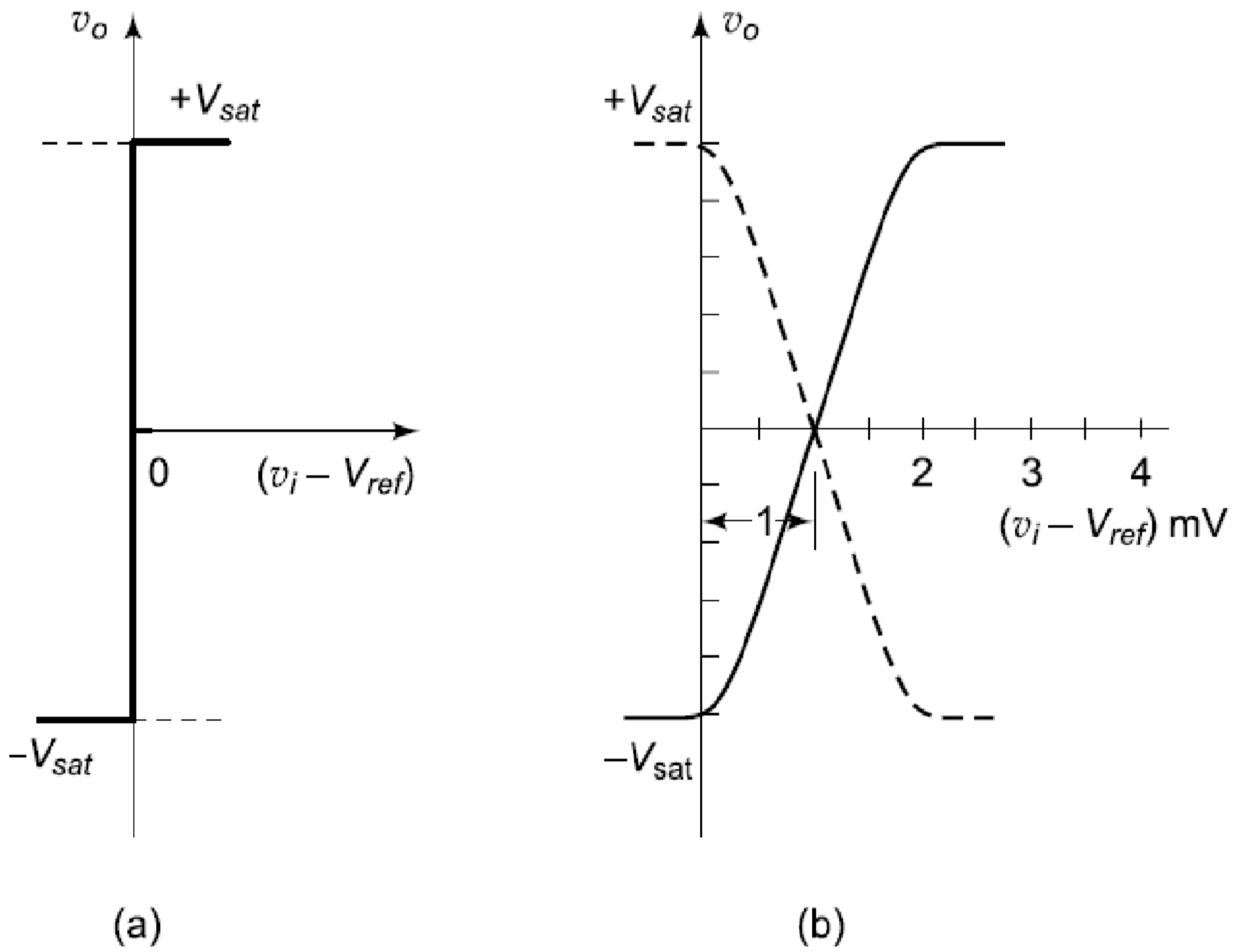


Fig.k. Transfer characteristics of a) Ideal Comparator b) Practical Comparator

Two types of comparators, viz.

(i) Non-inverting comparator, and
(ii) Inverting comparator

can be constructed using op-amps

(i) Non-Inverting Comparator

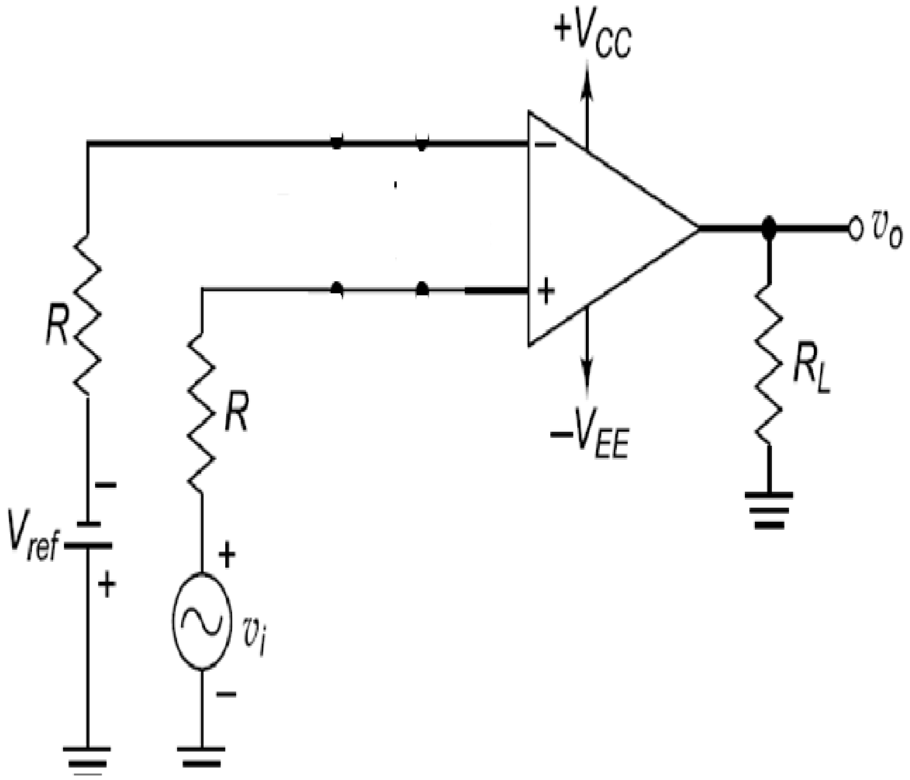


Fig.L. (a) Non-Inverting Comparator

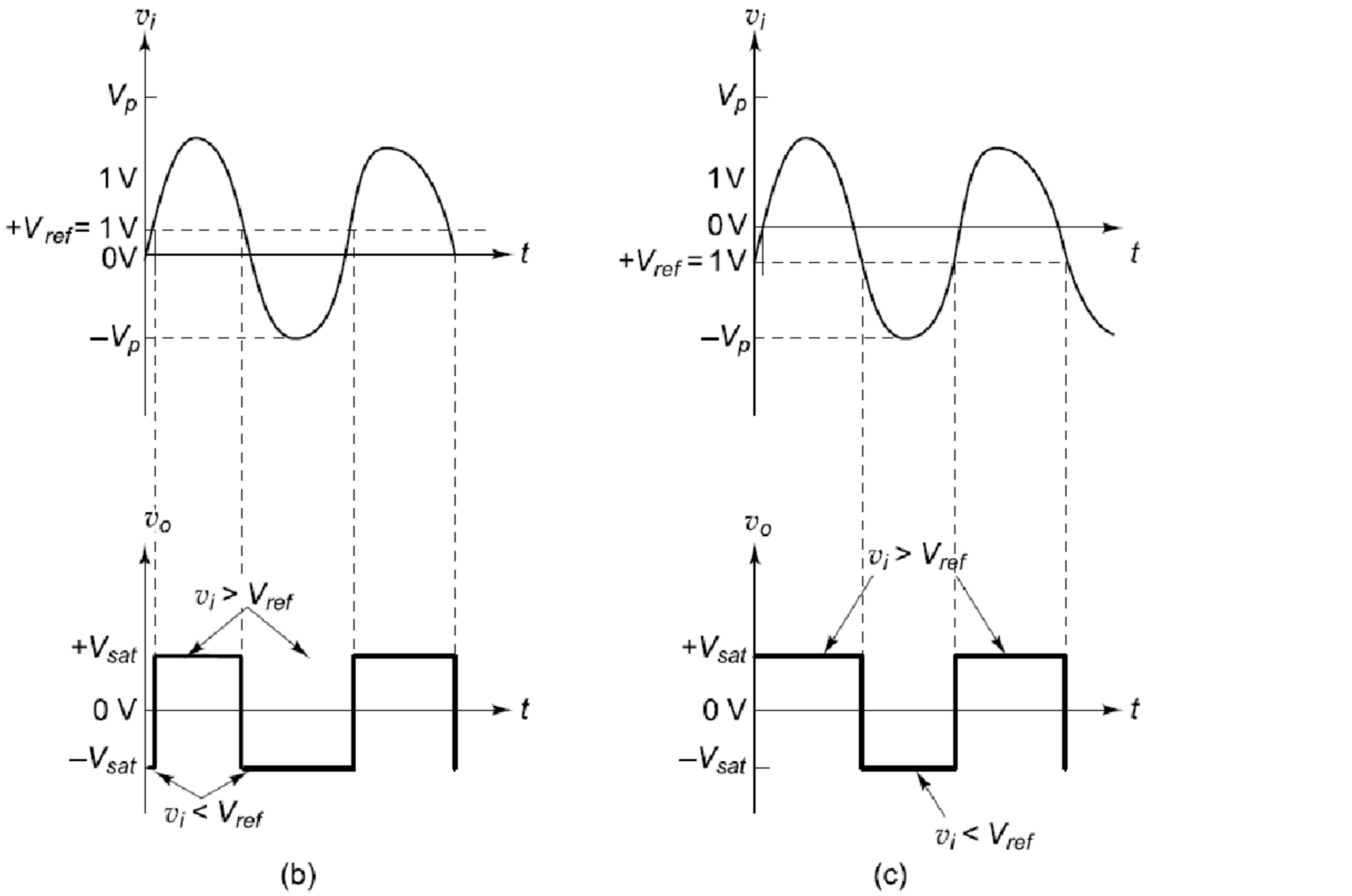


Fig.L. (b) Input and Output Waveforms when V_{ref} is +ve

Fig.L. (c) Input and Output Waveforms when V_{ref} is -ve

(ii) Inverting Comparator

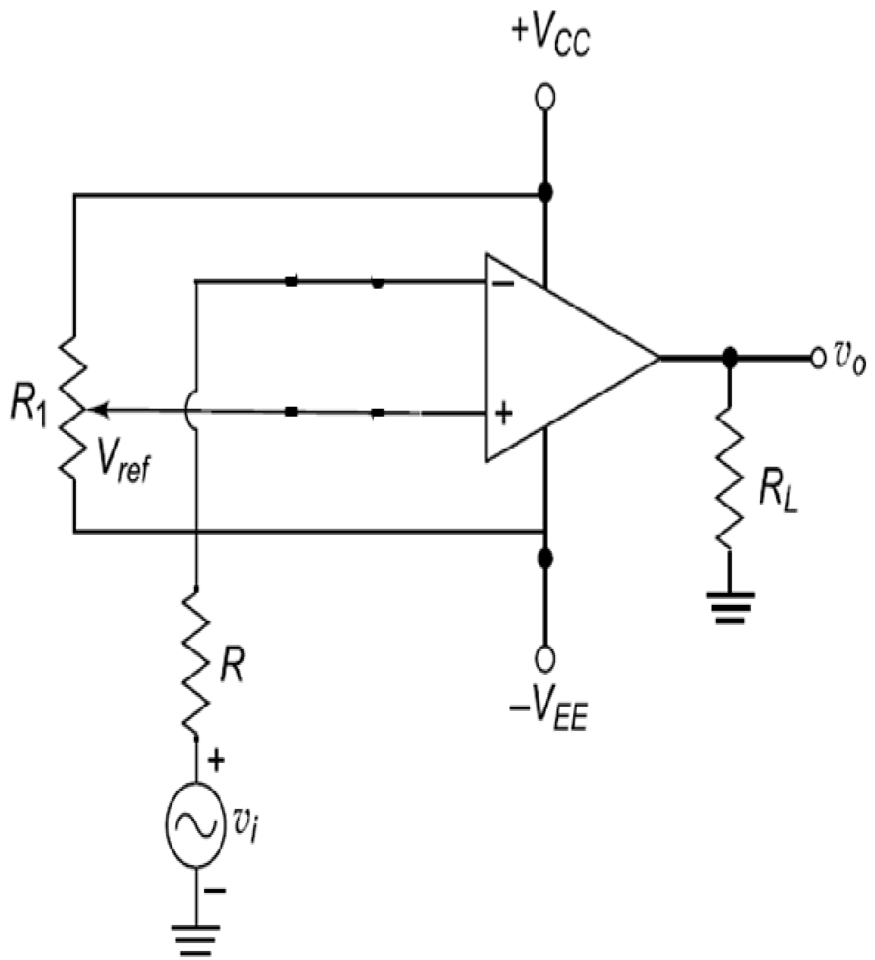


Fig.m. (a) Inverting Comparator

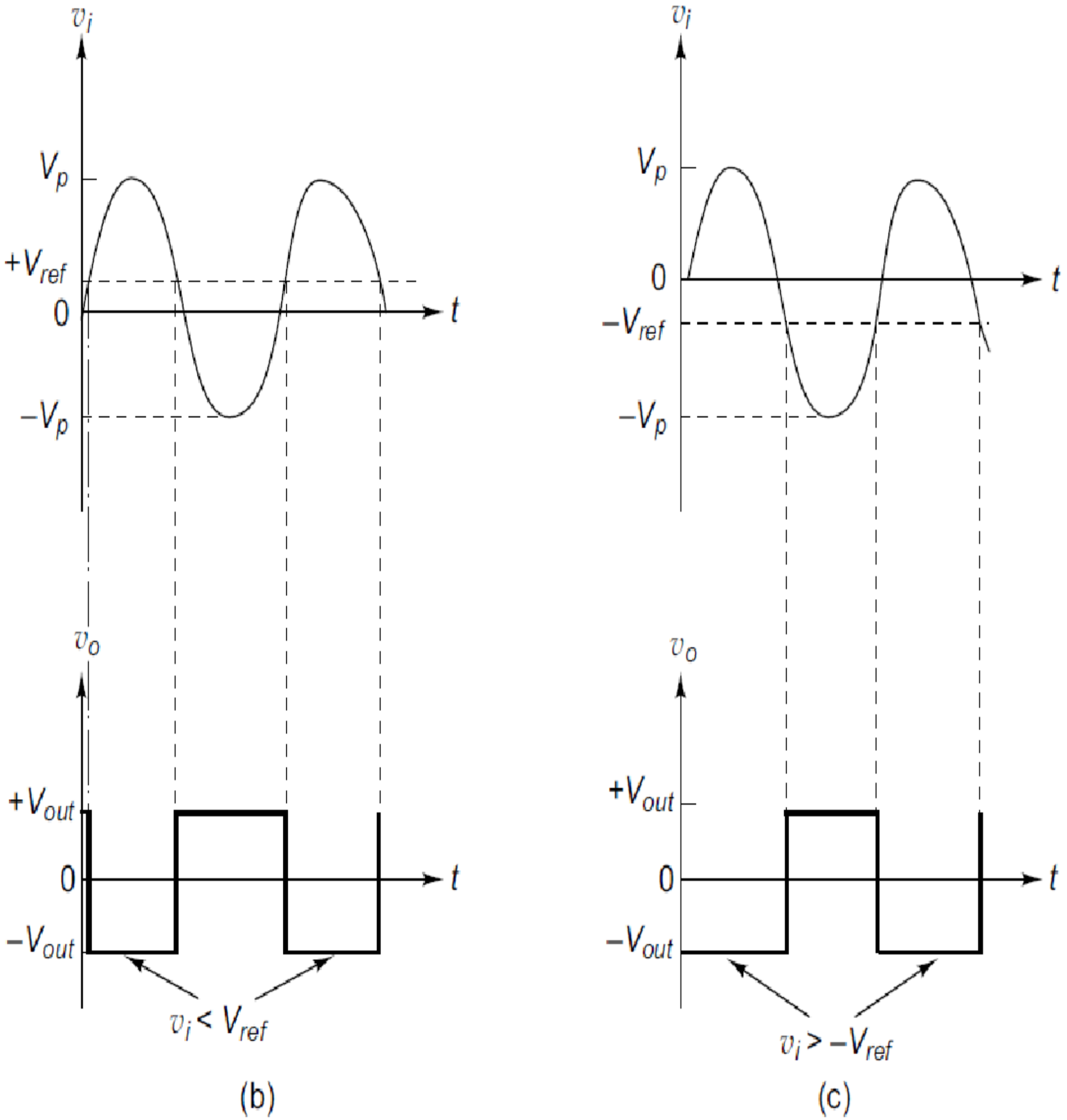


Fig.m. (b) Input and Output Waveforms when V_{ref} is +ve

Fig.m. (c) Input and Output Waveforms when V_{ref} is -ve

Applications of Comparator

The important applications of comparator are:

(i) Zero crossing detector (sine wave to square wave converter)

(ii) Window detector

(iii) Timing marker signal generator

(iv) Phase detector

(i) Zero crossing detector (sine wave to square wave converter)

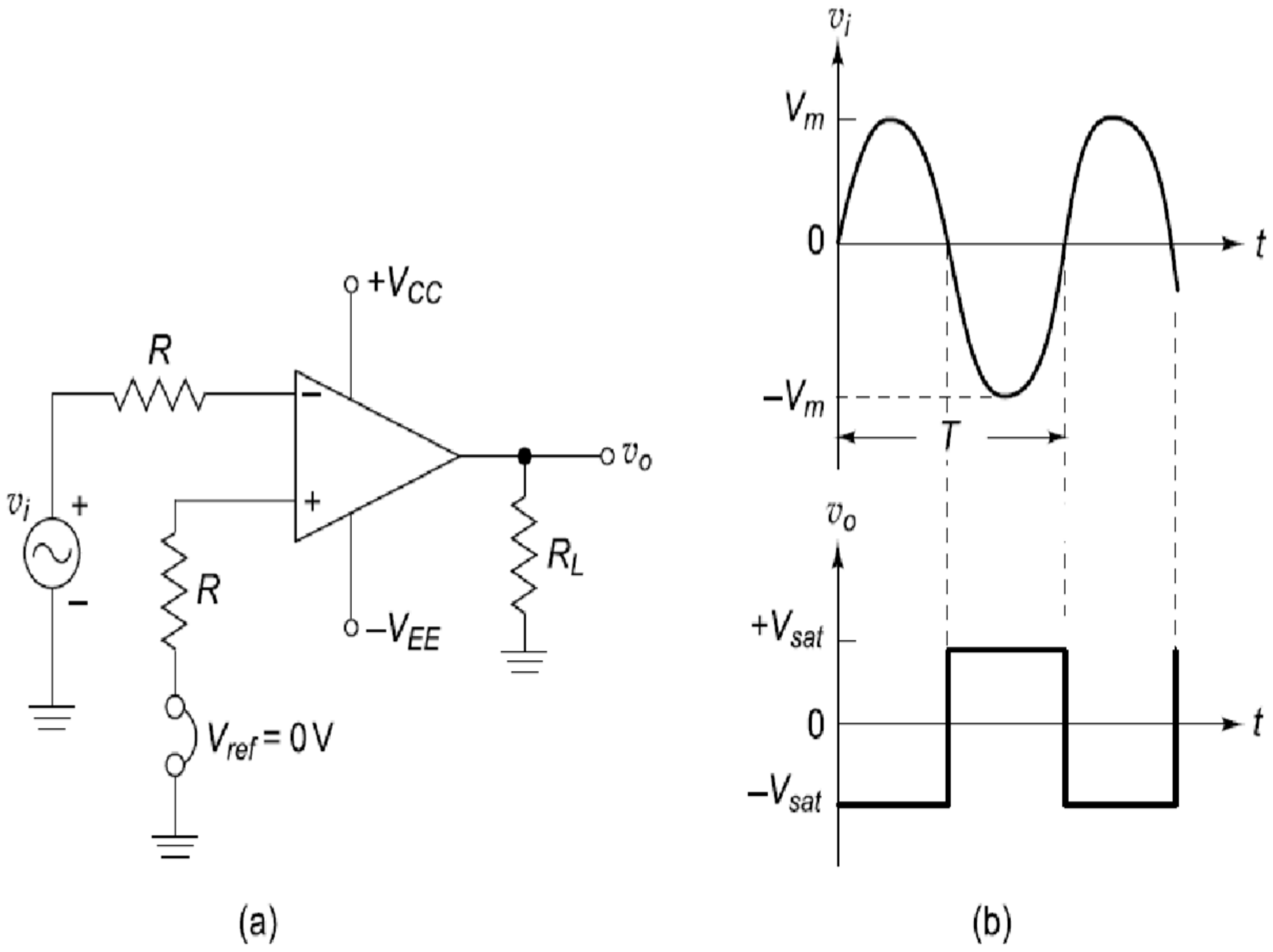


Fig.n. (a) Zero crossing detector (b) Input and Output Waveforms

(ii) Window detector

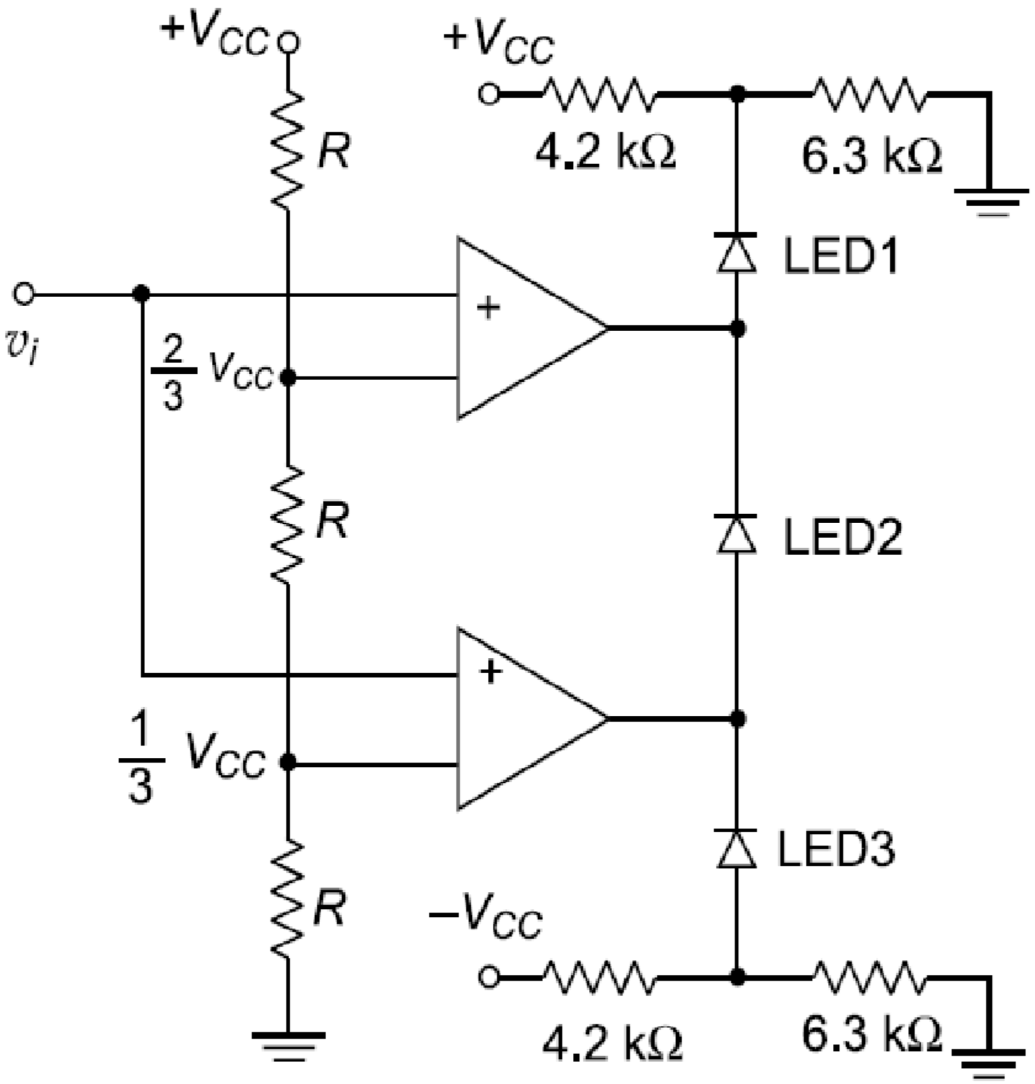
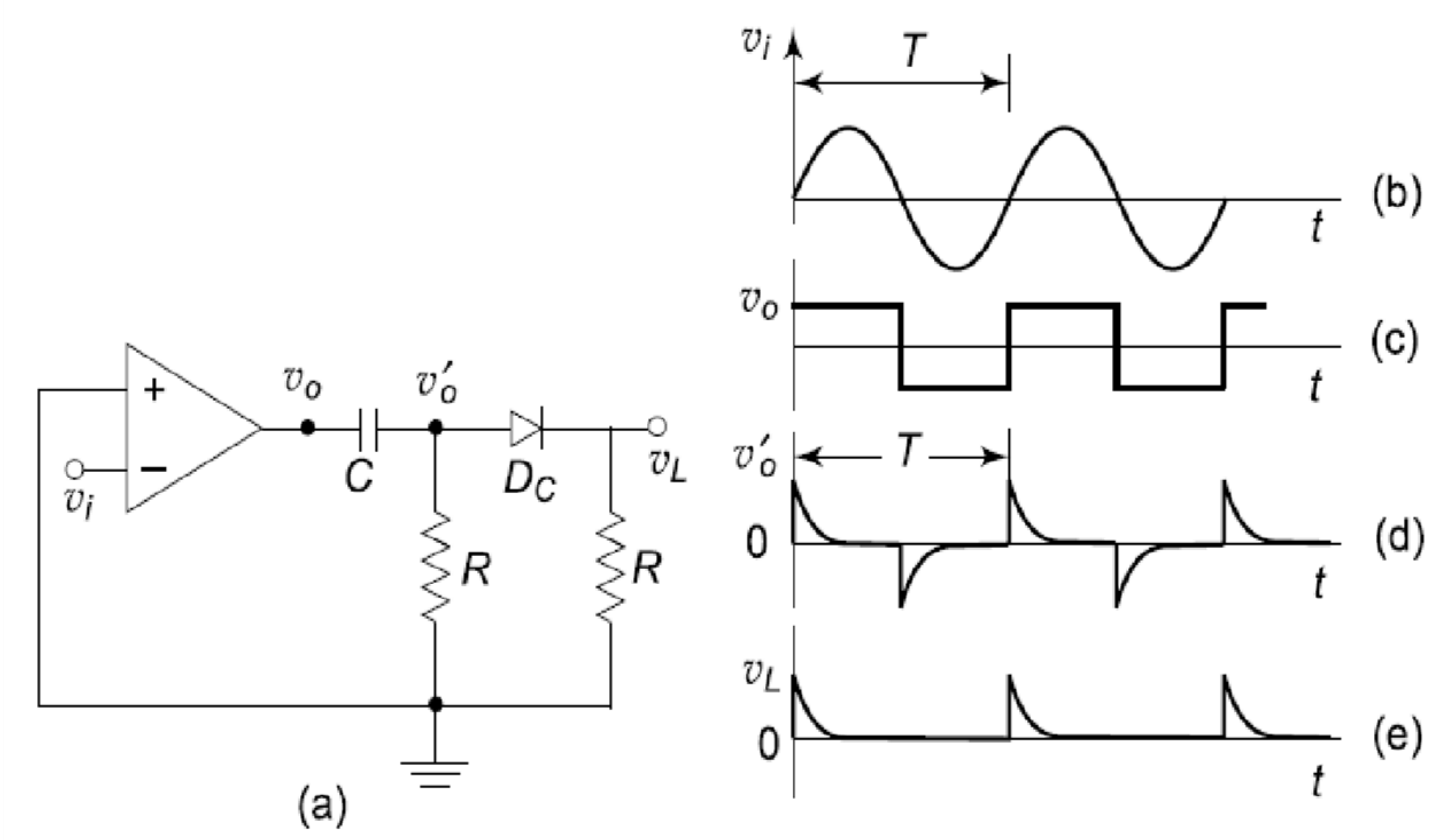


Fig.o. Three level comparator

Table.1. Three level comparator LED specifications

Input (Volts)	*LED3*	*LED2*	*LED1*
Less than 2 V	ON	OFF	OFF
Less than 4 V and more than 2 V	OFF	ON	OFF
More than 4 V	OFF	OFF	ON

(iii) Time marker signal generator



(a) Time marker signal generator circuit
(b) Input waveform, (c) Output v_o of op-amp
(d) Differentiated output v'_o
(e) Pulses across R, v_L

Fig.p. Time Market Circuit

(iv) Phase detector

- The phase angle between two time varying voltages can be measured using the circuit of Fig. p (a).
- The two voltages are converted into spikes using the time marker circuit shown in Fig. p (e).
- The time interval between the pulse spikes is then measured, and it is an indication of the phase difference between the two signals.
- The phase angle difference from 0° to 360° can be detected using such a circuit.

Sample and Hold Circuit

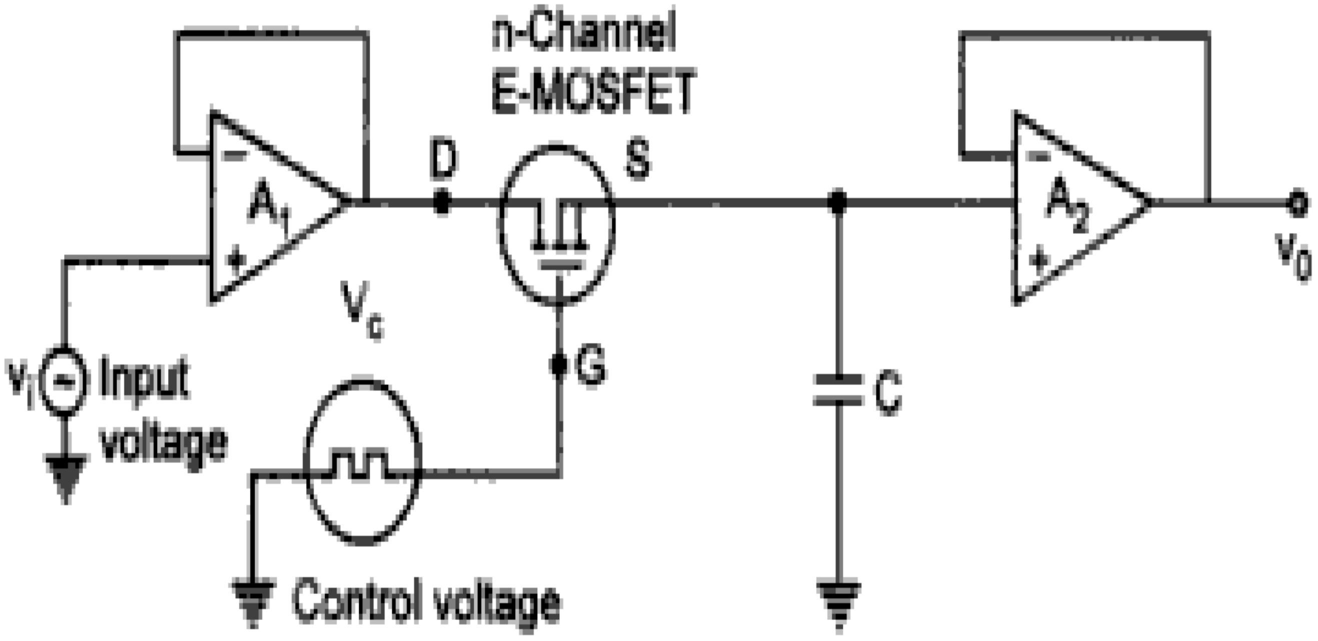


Fig.q. (a) Sample and Hold Circuit

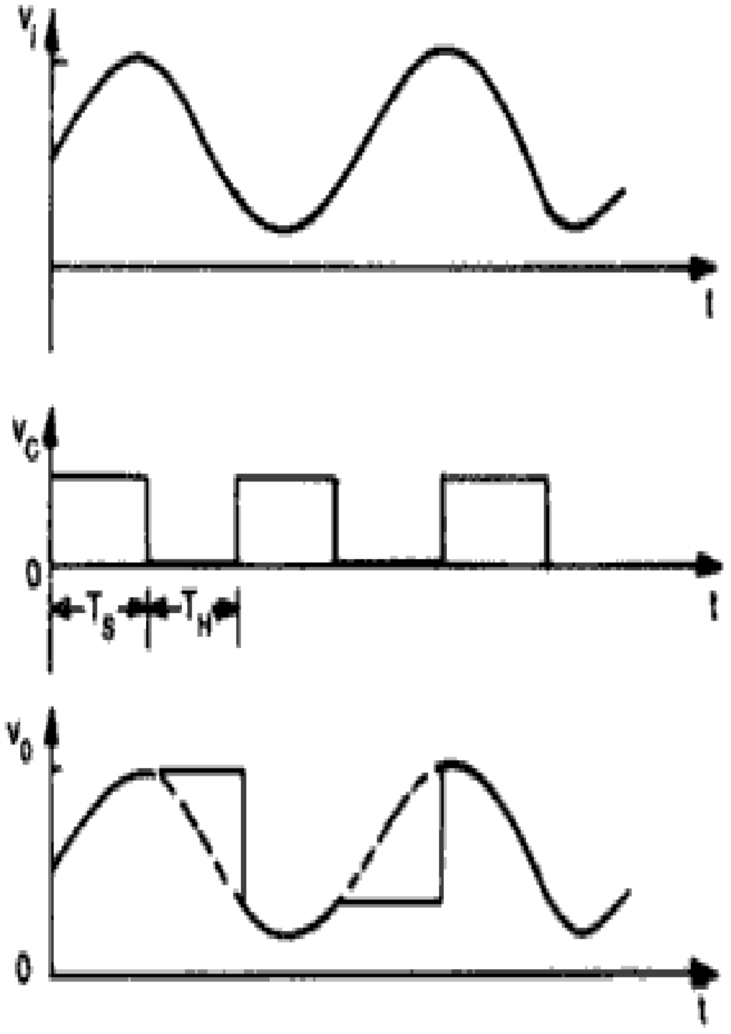


Fig.q. (b) Input and Output Waveforms

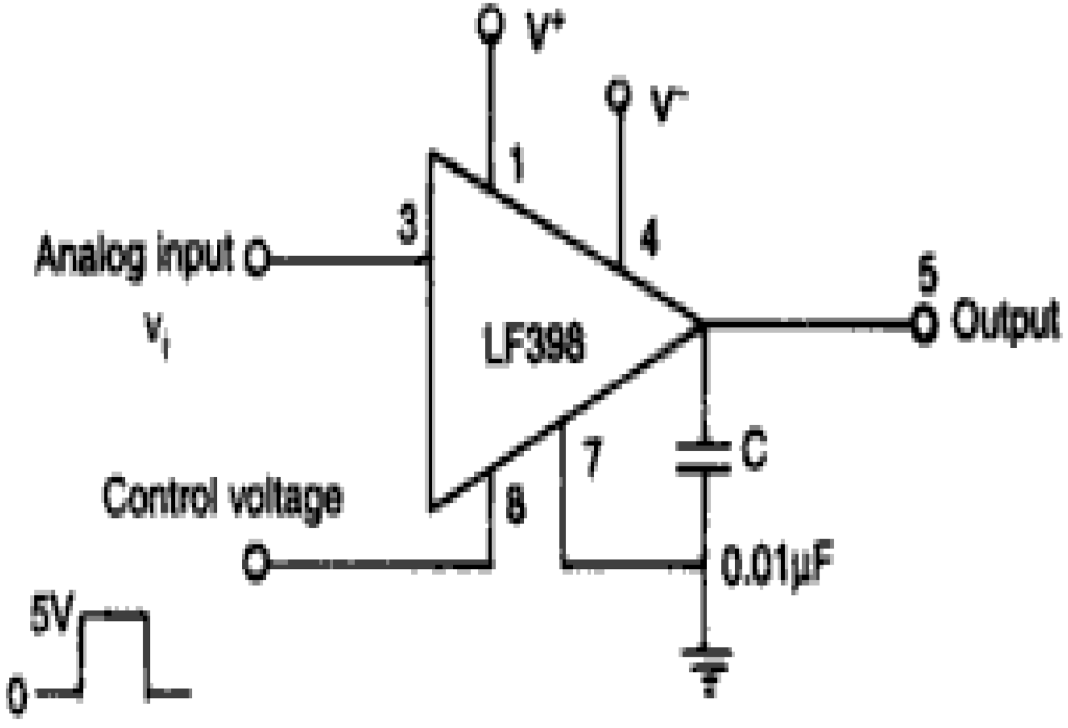


Fig.q. (c) Sample and Hold ICs LF398 Connection Diagram