

## **Unit- III: Field-Effect Transistor (FET) and Power Devices**

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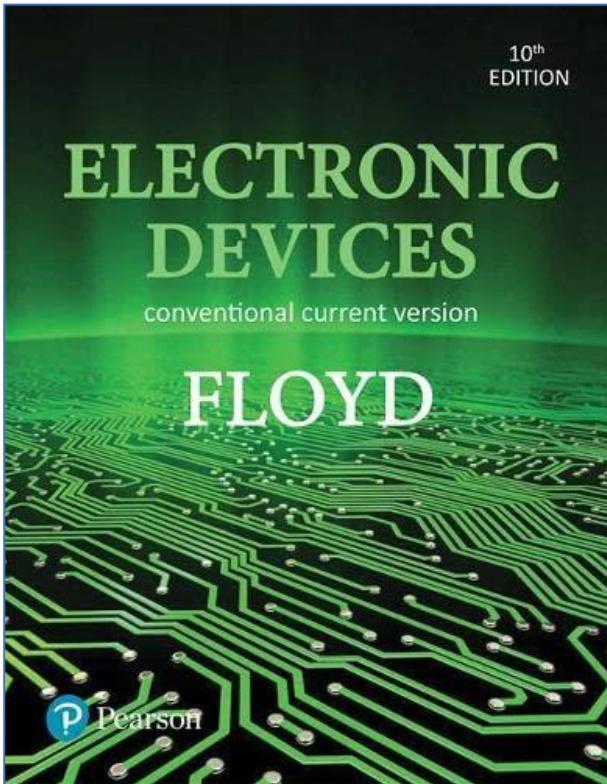
(An Autonomous Institute affiliated to Savitribai Phule Pune University)  
(NBA and NAAC accredited, ISO 9001:2015 certified)

# Teaching Scheme

Topics	<b>Unit- III: Field-Effect Transistor (FET) and Power Devices</b>
1	Introduction of FET
2	Types of MOSFET, construction and working of n-channel and p-channel E-MOSFET
3	V-I characteristics. MOSFET biasing circuit
4	MOSFET amplifier configurations- Common-Source (CS) amplifier, Common-Drain (CD) amplifier (source follower), and Common-Gate (CG) amplifier
5	Power Devices- Construction, working, characteristics and applications of Silicon-Controlled Rectifier (SCR),
6	Power Devices- Construction, working, characteristics and applications of TRIAC.

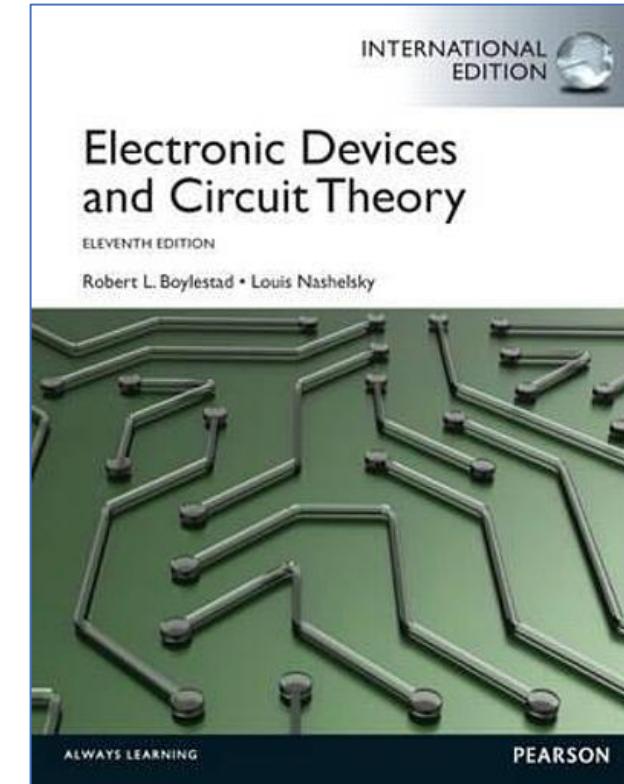
On completion of the course UNIT III, students will be able to:  
**Understand the working of MOSFET and power devices for various electronics applications.**

# Acknowledgment



## Acknowledgment

Figures and text in this presentation are taken from book  
**“Electronic Devices – Conventional Current Version,”** ,by  
Thomas L. Floyd.



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Figures and text in this presentation are taken from book :-  
**“Electronic Devices and Circuit Theory”,** Boylestad and  
Nashelsky, 11th Edition

# Text/Reference Books

Text Books			
Sr. No.	Title	Authors	Publication
T1	Electronic Devices and Circuits.	Floyd	9 <sup>TH</sup> Edition, Pearson Education
T2	Electronic Devices and Circuit Theory	Robert L. Boylestad, Louis Nashelsky	Prentice Hall
T3	Electronic Devices and Circuits	David A. Bell	5th Edition, Oxford press.
T4	Electronic Devices and Circuits	N.P. Deshpande	McGraw-Hill Education (India) Pvt Ltd.

Text Books			
R1	Electronic principles	Albert Malvino	7thEd,TataMc-Graw-Hill
R2	Linear Integrated Circuits	Ramakant Gaikwad	Pearson Education.
R3	Electronic Circuits Analysis and Design	Donald Neamen	3 <sup>rd</sup> Edition, TMH.
R4	Electronics Analog And Digital System	Jacob Millman, Christos C. Halkias	5th Edition Integrated McGraw-Hill

# FIELD-EFFECT TRANSISTORS ( FET'S)

- FET's are the unipolar devices because, unlike BJT's that use both electron and hole current, they operate only with one type of charge carrier.
- The two main types of FET's are the
- Junction field effect transistor (JFET) and
- The metal oxide semiconductor field effect transistor (MOSFET)

- Types of MOSFET:
  - Depletion D-MOSFET
  - Enhancement E-MOSFET
- In FET: An electric field control the conduction path of the output current
- The MOSFETs are popular in the design and construction of integrated circuits (ICs) for digital computers.
- Its thermal stability and low power dissipation makes it extremely popular in computer circuit design and in VLSI technology

# Comparison between BJT, JFET and MOSFET

Types	BJT	JFET	MOSFET
Device	Current controlled device	Voltage controlled	Voltage controlled
Flow of current	Bipolar	Unipolar	Unipolar
Mode of Operation	No modes	Only Depletion	In Depletion and Enhancement mode
Input Impedance	Low	High	Very High
Thermal Durability	Low	Better than BJT	High

# JUNCTION FIELD-EFFECT TRANSISTORS ( JFET'S) BASIC STRUCTURE

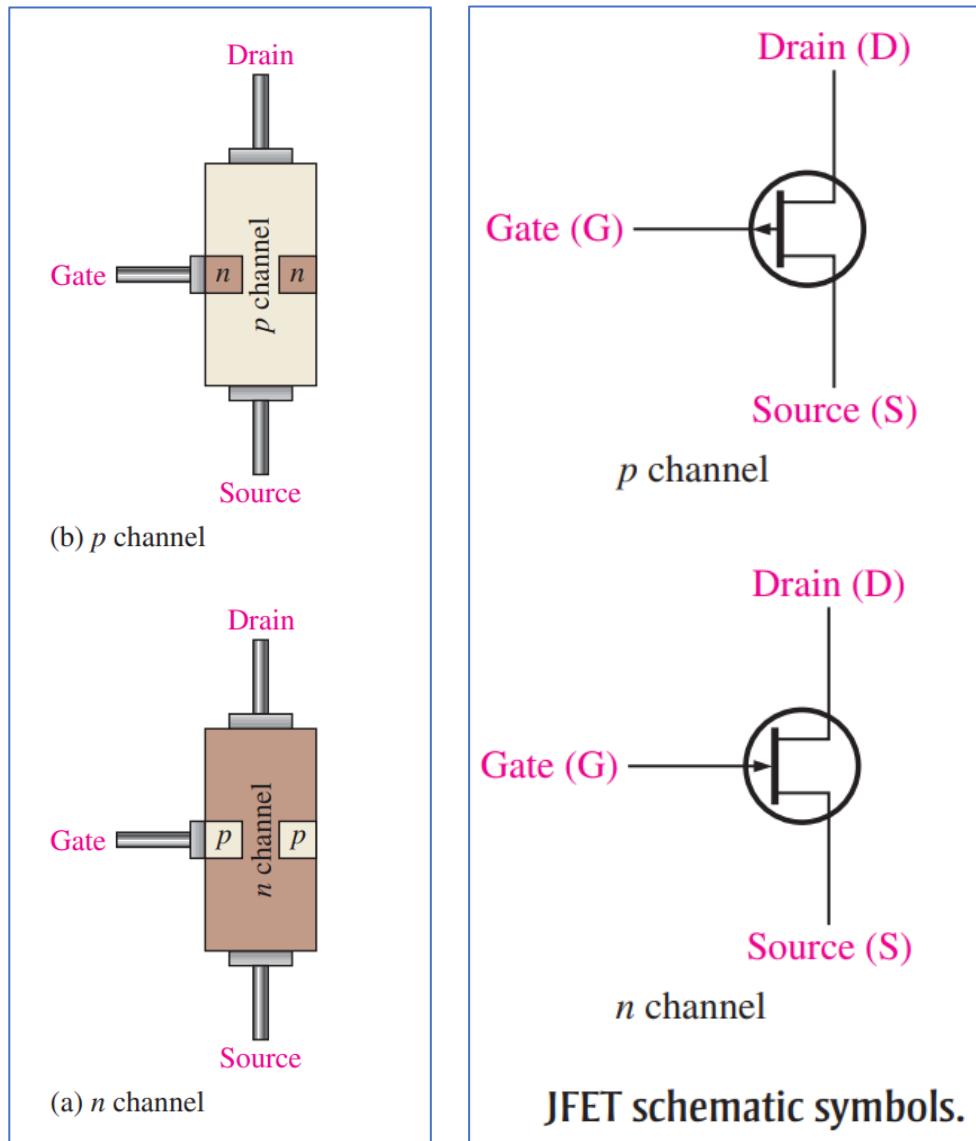
- Figure (a) shows the basic structure of an n-channel JFET (junction field-effect transistor).
- Wire leads are connected to each end of the n-channel; the drain is at the upper end, and the source is at the lower end.
- Two p-type regions are diffused in the n-type material to form a channel, and both p-type regions are connected to the gate lead.
- For simplicity, the gate lead is shown connected to only one of the p regions.
- A p-channel JFET is shown in Figure (b).

## JFET Symbols

- The schematic symbols for both n-channel and p-channel JFETs are shown in Figure.
- Notice that the arrow on the gate points “in” for n channel and “out” for p channel.

3 terminal:

- Drain** – Top
- Source** – Bottom
- Gate** – 2 p/n-type regions are diffuse in the n/p-type material to form a channel.

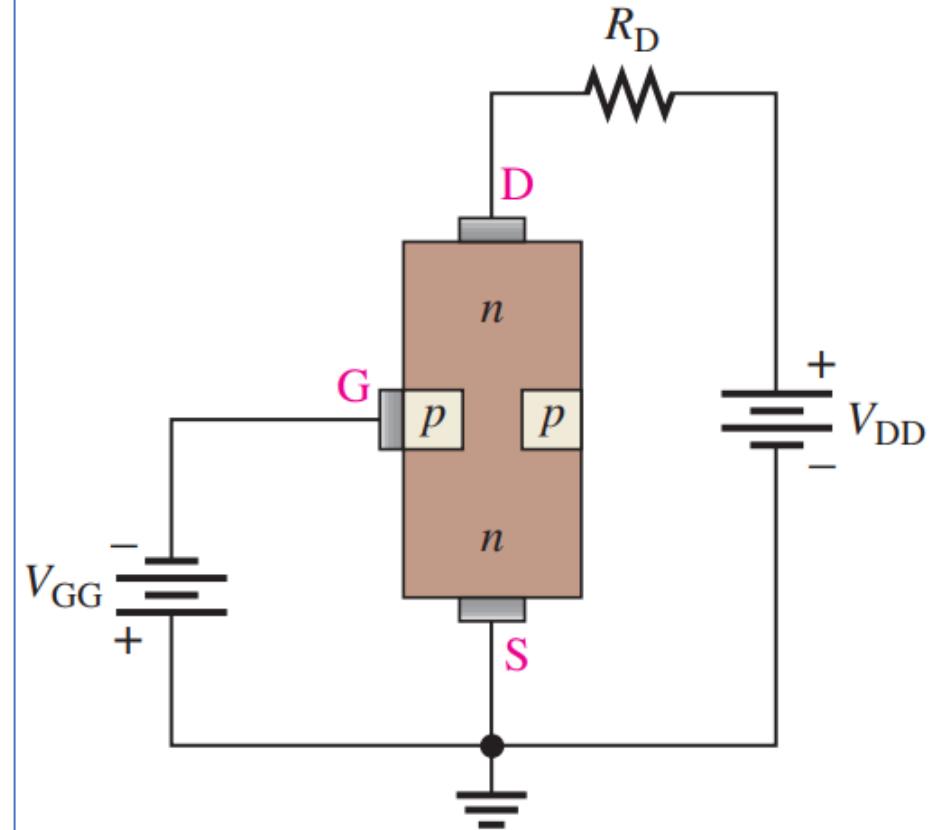


Acknowledgment:-Thomas L. Floyd Electronic Devices, Electron Flow Version, Ninth Edition

# JUNCTION FIELD-EFFECT TRANSISTORS ( JFET'S) BASIC OPERATION

- To illustrate the operation of a JFET, Figure shows dc bias voltages applied to an n-channel device.
- $V_{DD}$  provides a drain-to-source voltage and supplies current from drain to source.
- $V_{GG}$  sets the reverse-bias voltage between the gate and the source, as shown.

- The JFET is always operated with the gate-source pn junction reverse-biased.
- Reverse biasing of the gate-source junction with a negative gate voltage produces a depletion region along the pn junction, which extends into the n channel and thus increases its resistance by restricting the channel width.



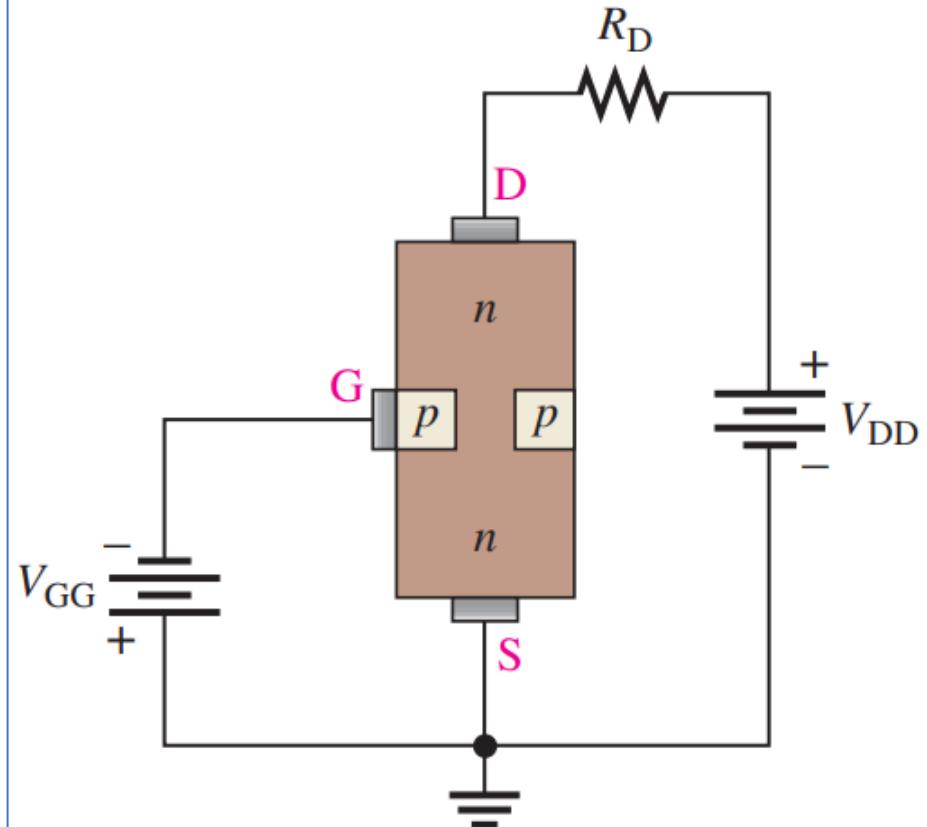
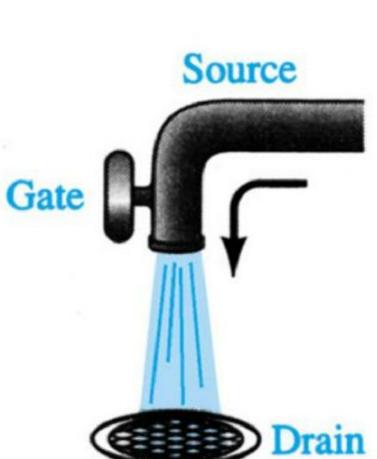
A biased n-channel JFET.

# JUNCTION FIELD-EFFECT TRANSISTORS ( JFET'S) BASIC OPERATION

- To illustrate the operation of a JFET, Figure shows dc bias voltages applied to an n-channel device.
- $V_{DD}$  provides a drain-to-source voltage and supplies current from drain to source.
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JFET operation can be compared to a water spigot.

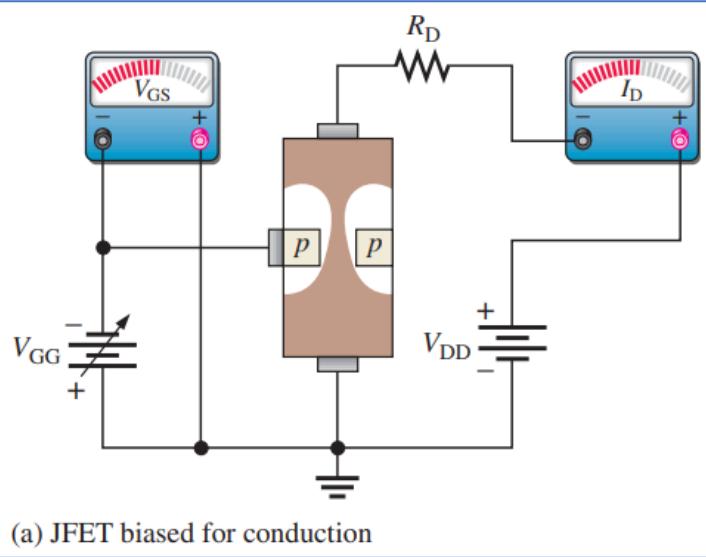
- The Source** of water pressure is the accumulation of electrons at the negative pole of the drain-source voltage.
- The Drain** of water is the electron deficiency (or holes) at the positive pole of the applied voltage.
- The Gate (control)** of flow of water is the gate voltage that controls the width of the n-channel and, therefore, the flow of charges from source to drain.



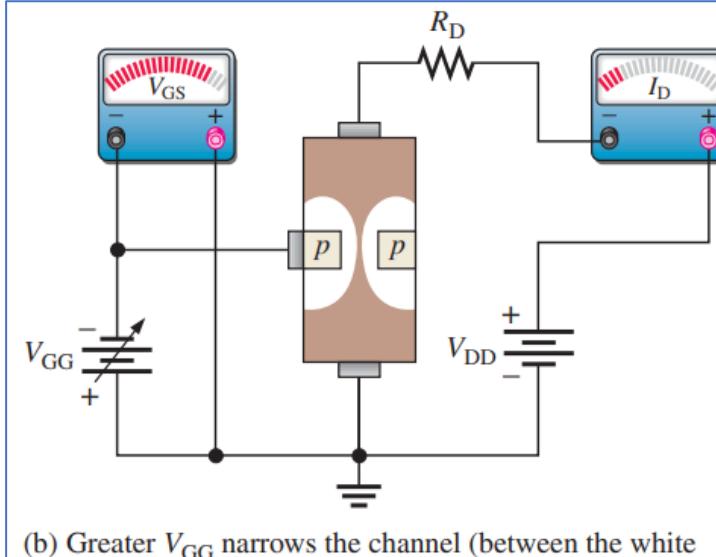
A biased n-channel JFET.

# JUNCTION FIELD-EFFECT TRANSISTORS ( JFET'S) BASIC OPERATION

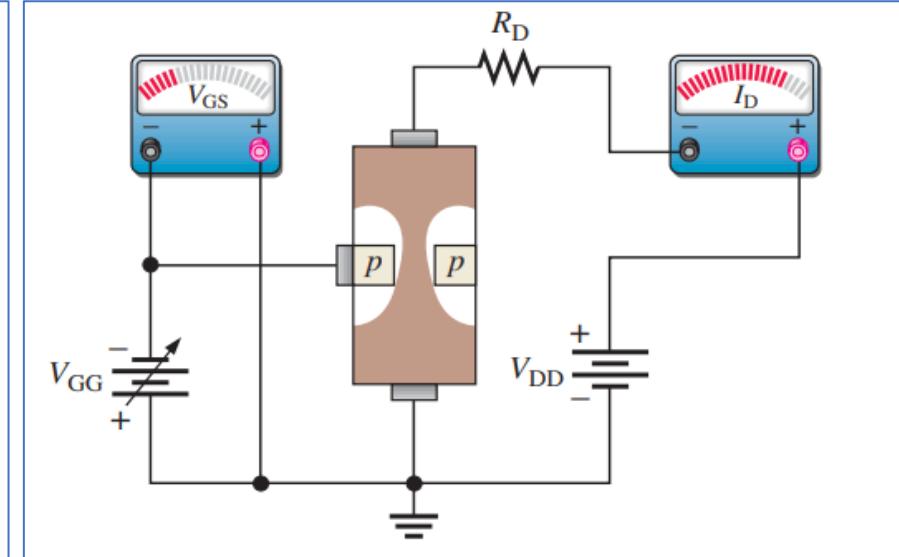
- The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current,  $I_D$ .
- Figure illustrates this concept.
- The white areas represent the depletion region created by the reverse bias.
- It is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source.



(a) JFET biased for conduction



(b) Greater  $V_{GG}$  narrows the channel (between the white areas) which increases the resistance of the channel and decreases  $I_D$ .



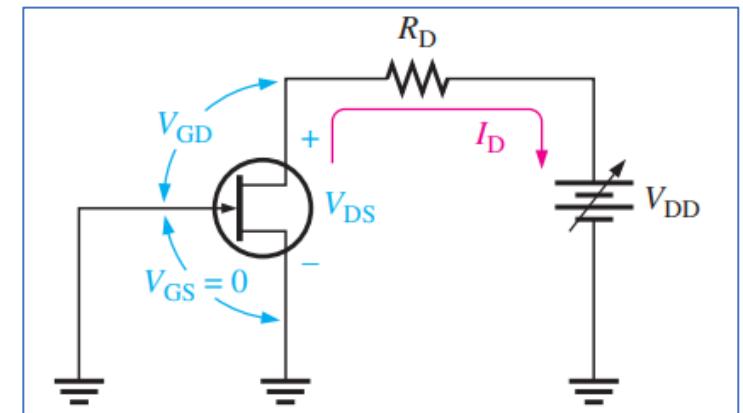
(c) Less  $V_{GG}$  widens the channel (between the white areas) which decreases the resistance of the channel and increases  $I_D$ .

# JFET'S CHARACTERISTICS AND PARAMETERS

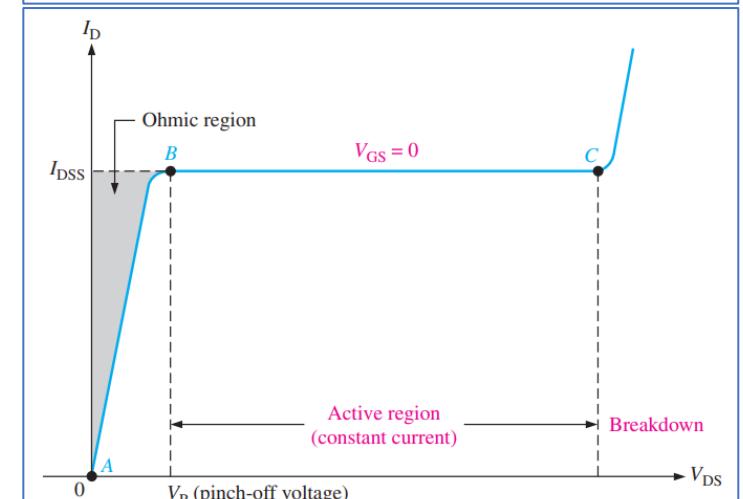
## • Drain Characteristic Curve

- Consider the case when the gate-to-source voltage is zero ( $V_{GS} = 0$  V).
- This is produced by shorting the gate to the source, as in Figure (a) where both are grounded. As  $V_{DD}$  (and thus  $V_{DS}$ ) is increased from 0 V,  $I_D$  will increase proportionally, as shown in the graph of Figure(b) between points A and B.
- In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect.
- This is called the ohmic region because  $V_{DS}$  and  $I_D$  are related by Ohm's law.

- At point B in Figure (b), the curve levels off and enters the active region where  $I_D$  becomes essentially constant.
- As  $V_{DS}$  increases from point B to point C, the reverse-bias voltage from gate to drain ( $V_{GD}$ ) produces a depletion region large enough to offset the increase in  $V_{DS}$ , thus keeping  $I_D$  relatively constant



(a) JFET with  $V_{GS} = 0$  V and a variable  $V_{DS}$  ( $V_{DD}$ )



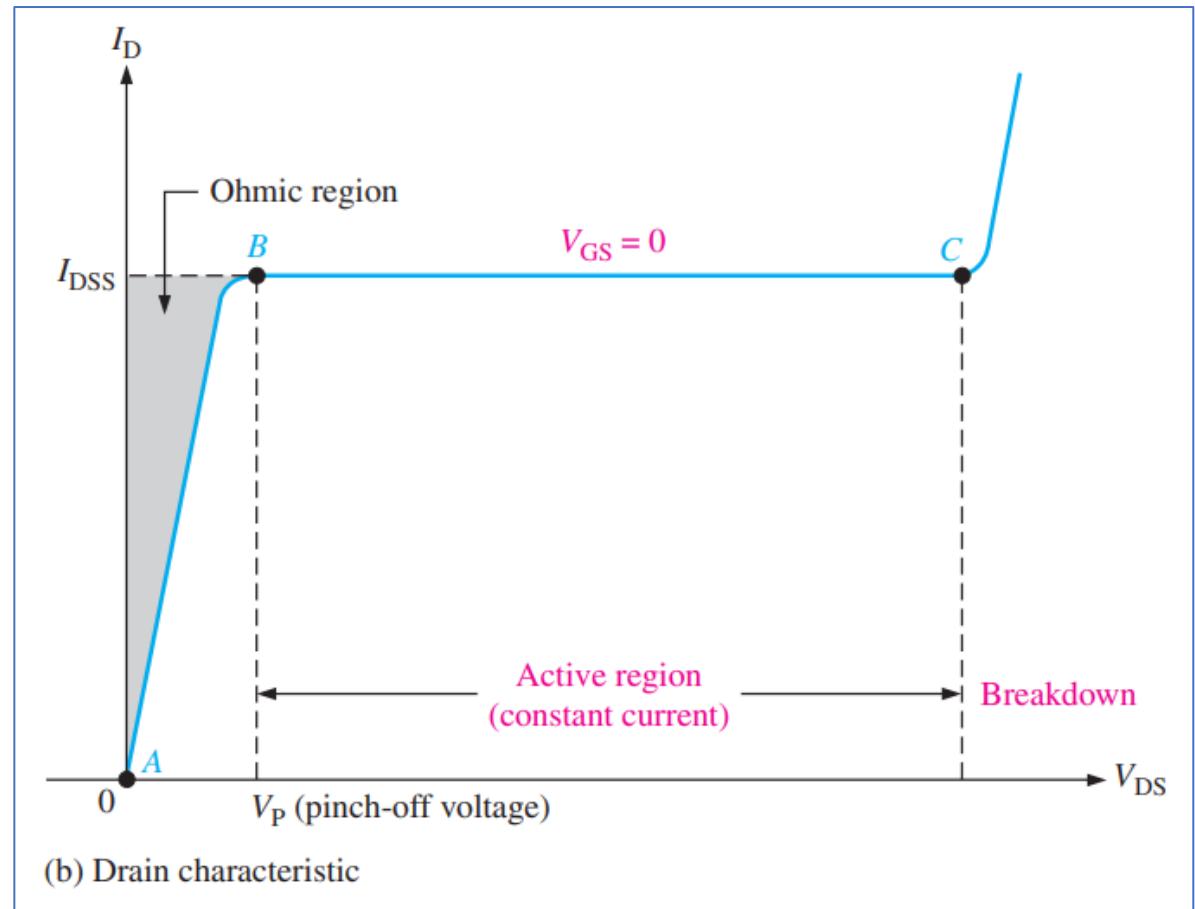
The drain characteristic curve of a JFET for  $V_{GS} = 0$  showing pinch-off voltage

Acknowledgment:-Thomas L. Floyd Electronic Devices, Electron Flow Version, Ninth Edition

# JFET'S CHARACTERISTICS AND PARAMETERS

- Drain Characteristic Curve

- ***Pinch-Off Voltage***
- For  $V_{GS} = 0$  V, the value of  $V_{DS}$  at which  $I_D$  becomes essentially constant (point B on the curve in Figure (b)) is the pinch-off voltage,  $V_P$ .
- For a given JFET,  $V_P$  has a fixed value.
- As you can see, a continued increase in  $V_{DS}$  above the pinch-off voltage produces an almost constant drain current.
- This value of drain current is  $I_{DSS}$  (Drain to Source current with gate Shorted) and is always specified on JFET datasheets.
- $I_{DSS}$  is the maximum drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition,  $V_{GS}= 0$  V



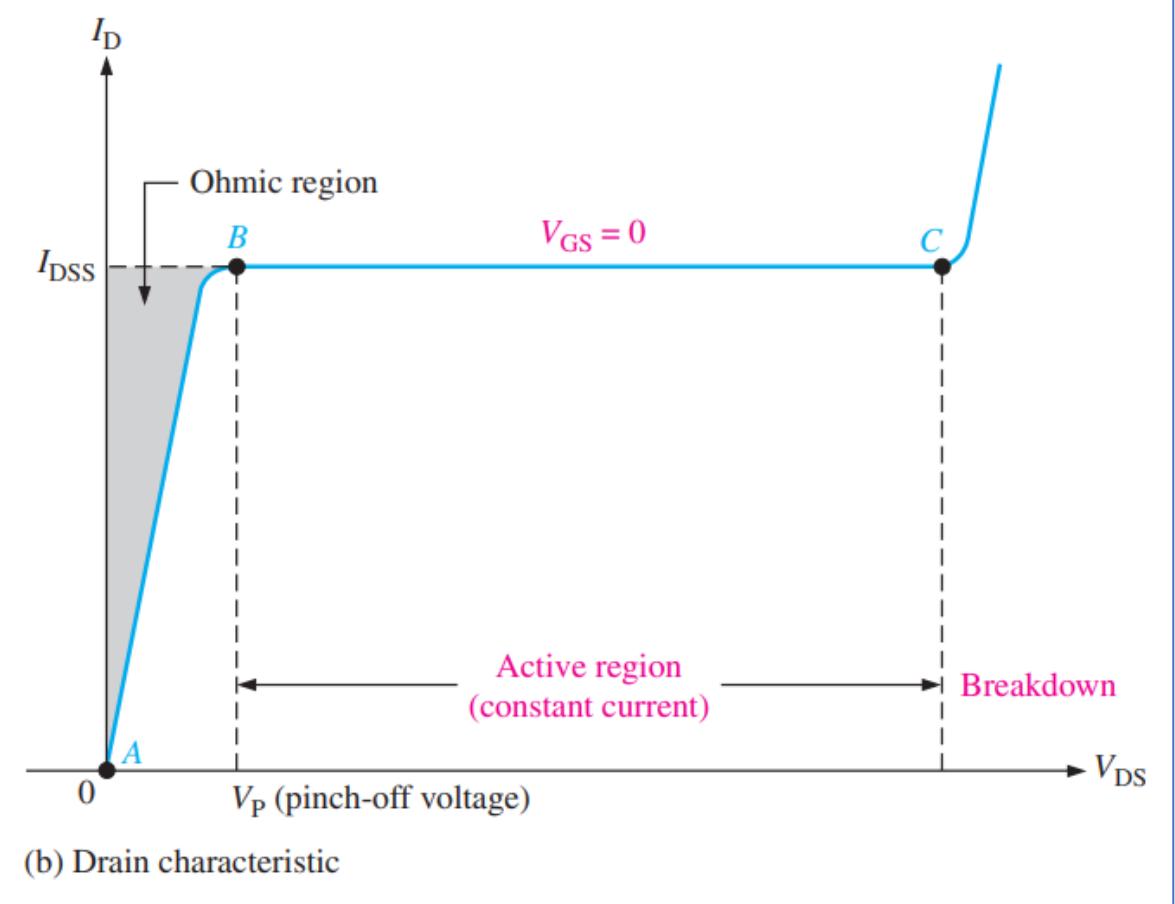
The drain characteristic curve of a JFET for  $V_{GS} = 0$  showing pinch-off voltage

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# JFET'S CHARACTERISTICS AND PARAMETERS

- Drain Characteristic Curve

- ***Breakdown***
- As shown in the graph in Figure (b), breakdown occurs at point C when  $I_D$  begins to increase very rapidly with any further increase in  $V_{DS}$ .
- Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the active region (constant current) (between points B and C on the graph).

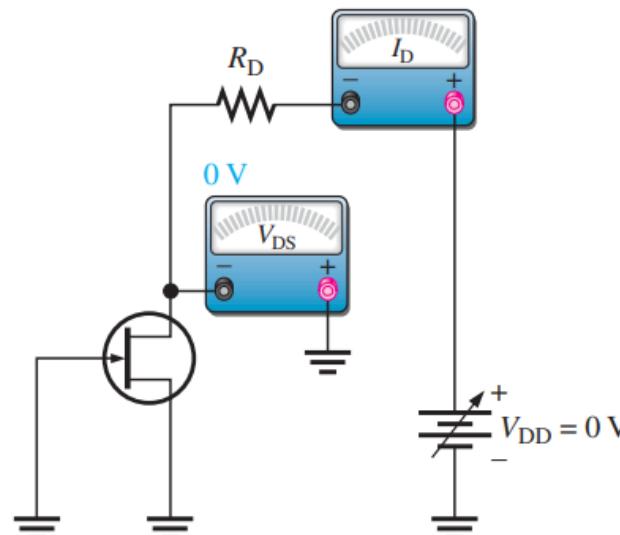


The drain characteristic curve of a JFET for  $V_{GS} = 0$  showing pinch-off voltage

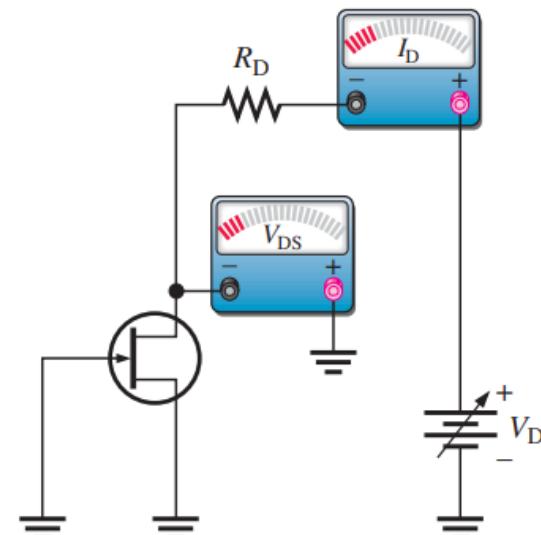
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# JFET'S CHARACTERISTICS AND PARAMETERS

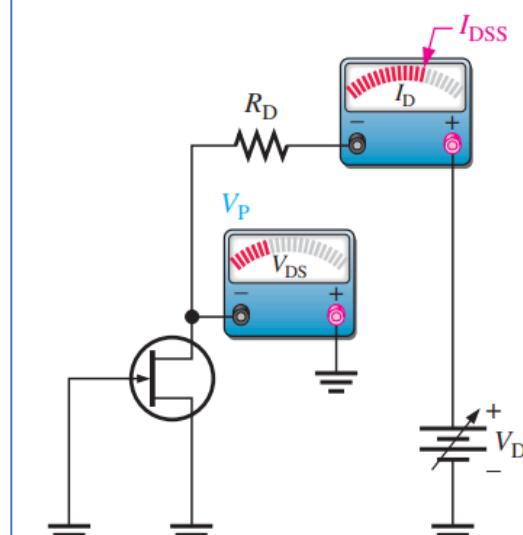
- **Drain Characteristic Curve**
- The JFET action that produces the drain characteristic curve to the point of breakdown for  $V_{GS} = 0$  V is illustrated in Figure.



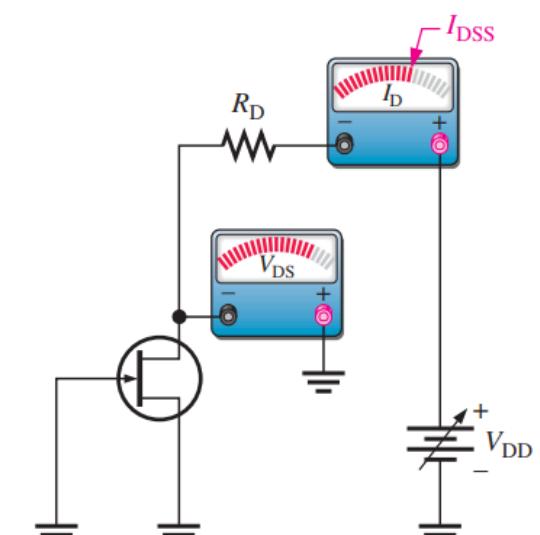
(a) When  $V_{DS} = 0$ ,  $I_D = 0$ .



(b)  $I_D$  increases proportionally with  $V_{DS}$  in the ohmic region.



(c) When  $V_{DS} = V_P$ ,  $I_D$  is constant and equal to  $I_{DSS}$ .



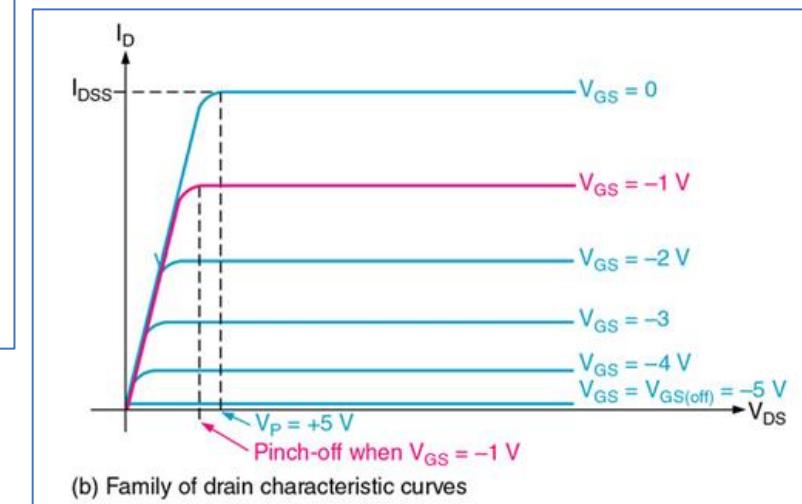
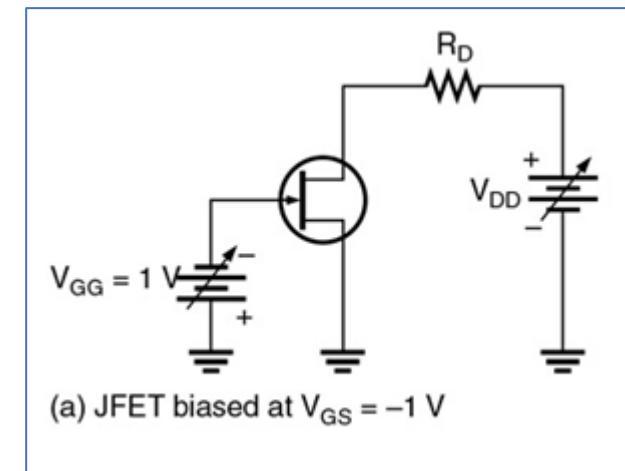
(d) As  $V_{DS}$  increases further,  $I_D$  remains at  $I_{DSS}$  until breakdown occurs.

JFET action that produces the characteristic curve for  $V_{GS} = 0$  V

# JFET'S CHARACTERISTICS AND PARAMETERS

## • Drain Characteristic Curve

- **V<sub>GS</sub> Controls I<sub>D</sub>**
- Let's connect a bias voltage,  $V_{GG}$ , from gate to source as shown in Figure (a).
- As  $V_{GS}$  is set to increasingly more negative values by adjusting  $V_{GG}$ , a family of drain characteristic curves is produced, as shown in Figure (b).
- Notice that  $I_D$  decreases as the magnitude of  $V_{GS}$  is increased to larger negative values because of the narrowing of the channel.
- Also notice that, for each increase in  $V_{GS}$ , the JFET reaches pinch-off (where constant current begins) at values of  $V_{DS}$  less than  $V_p$ .
- The term pinch-off is not the same as pinch-off voltage,  $V_p$ .
- Therefore, the amount of drain current is controlled by  $V_{GS}$ , as illustrated in Figure .



Pinch-off occurs at a lower  $V_{DS}$  as  $V_{GS}$  is increased to more negative values

# JFET'S CHARACTERISTICS AND PARAMETERS

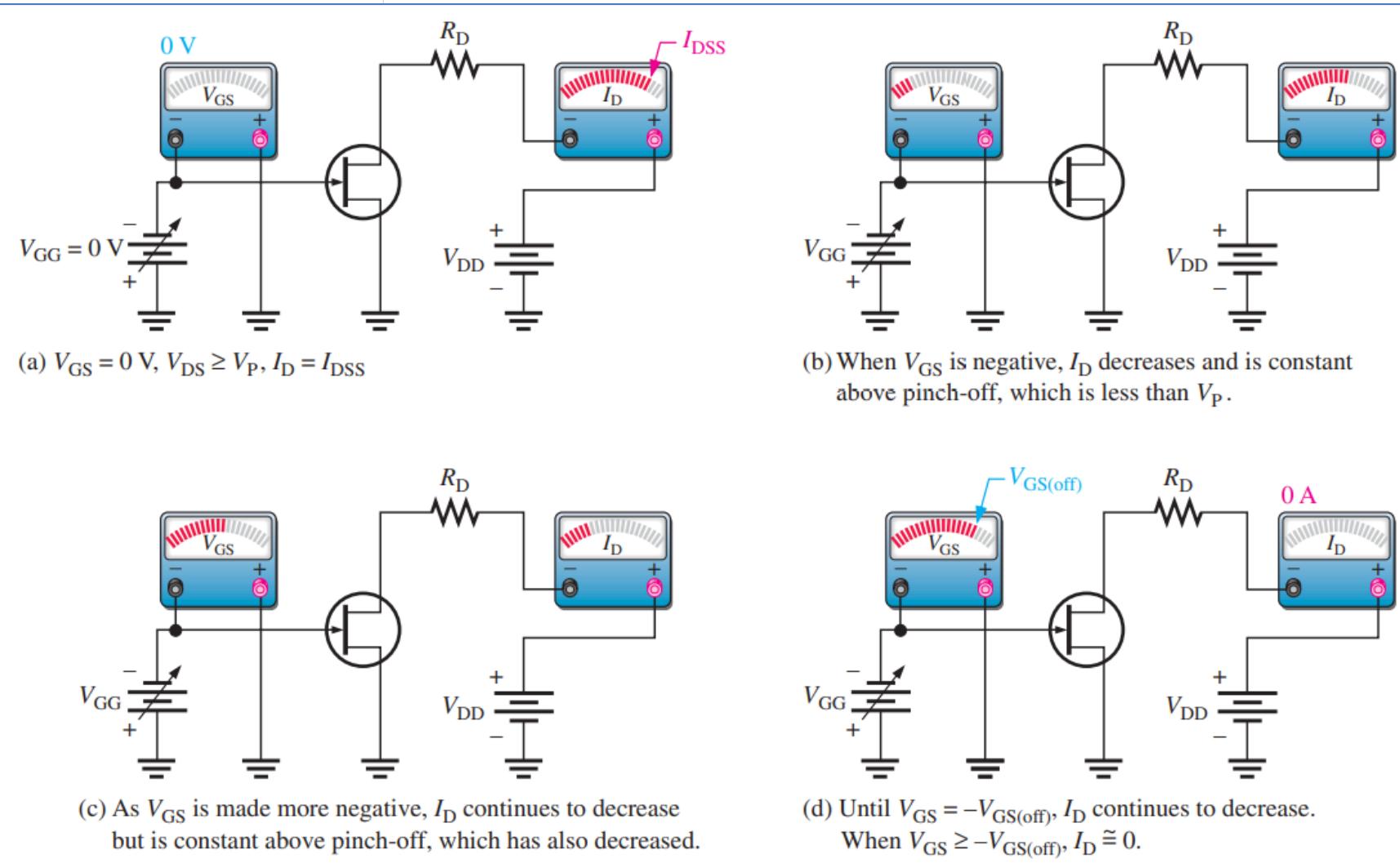
- **Drain Characteristic Curve**

- **V<sub>GS</sub> Controls I<sub>D</sub>**

- The amount of drain current is controlled by  $V_{GS}$ , as illustrated in Figure .

- **Cutoff Voltage**

- The value of  $V_{GS}$  that makes  $I_D$  approximately zero is the cutoff voltage,  $V_{GS(off)}$ , as shown in Figure(d).
- The JFET must be operated between  $V_{GS}=0$  V and  $V_{GS(off)}$ .
- For this range of gate-to-source voltages,  $I_D$  will vary from a maximum of  $I_{DSS}$  to a minimum of almost zero.



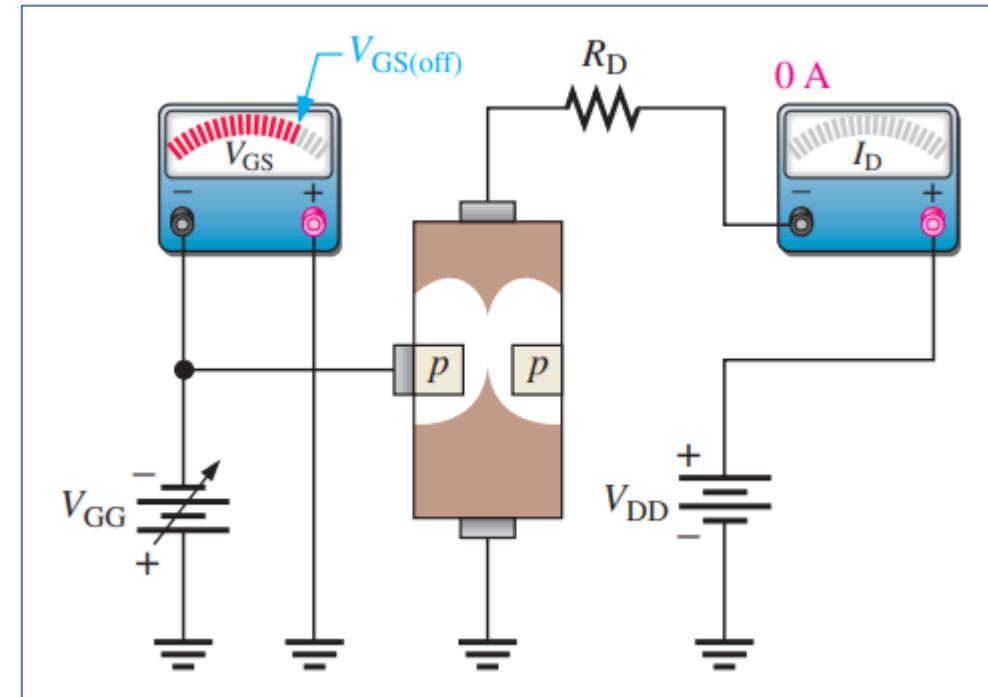
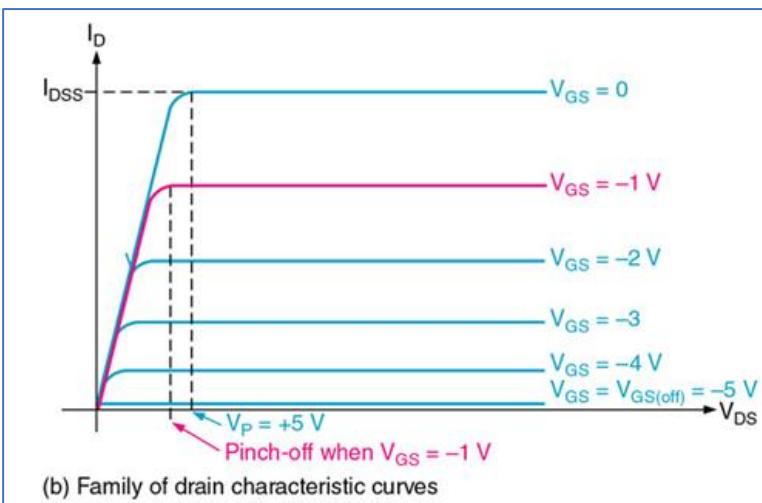
$V_{GS}$  controls  $I_D$ .

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# JFET'S CHARACTERISTICS AND PARAMETERS

## • Drain Characteristic Curve

- As you have seen, for an n-channel JFET, the more negative  $V_{GS}$  is, the smaller  $I_D$  becomes in the active region.
- When  $V_{GS}$  has a sufficiently large negative value,  $I_D$  is reduced to zero.
- This cutoff effect is caused by the widening of the depletion region to a point where it completely closes the channel, as shown in Figure.

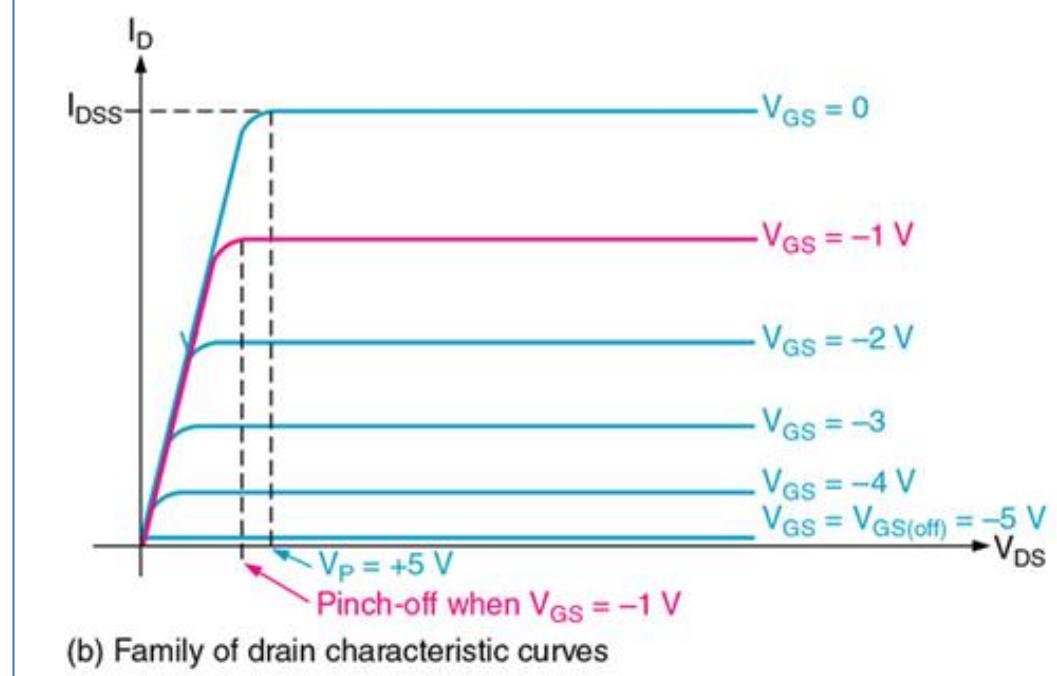


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# JFET'S CHARACTERISTICS AND PARAMETERS

## • Comparison of Pinch-Off Voltage and Cutoff Voltage

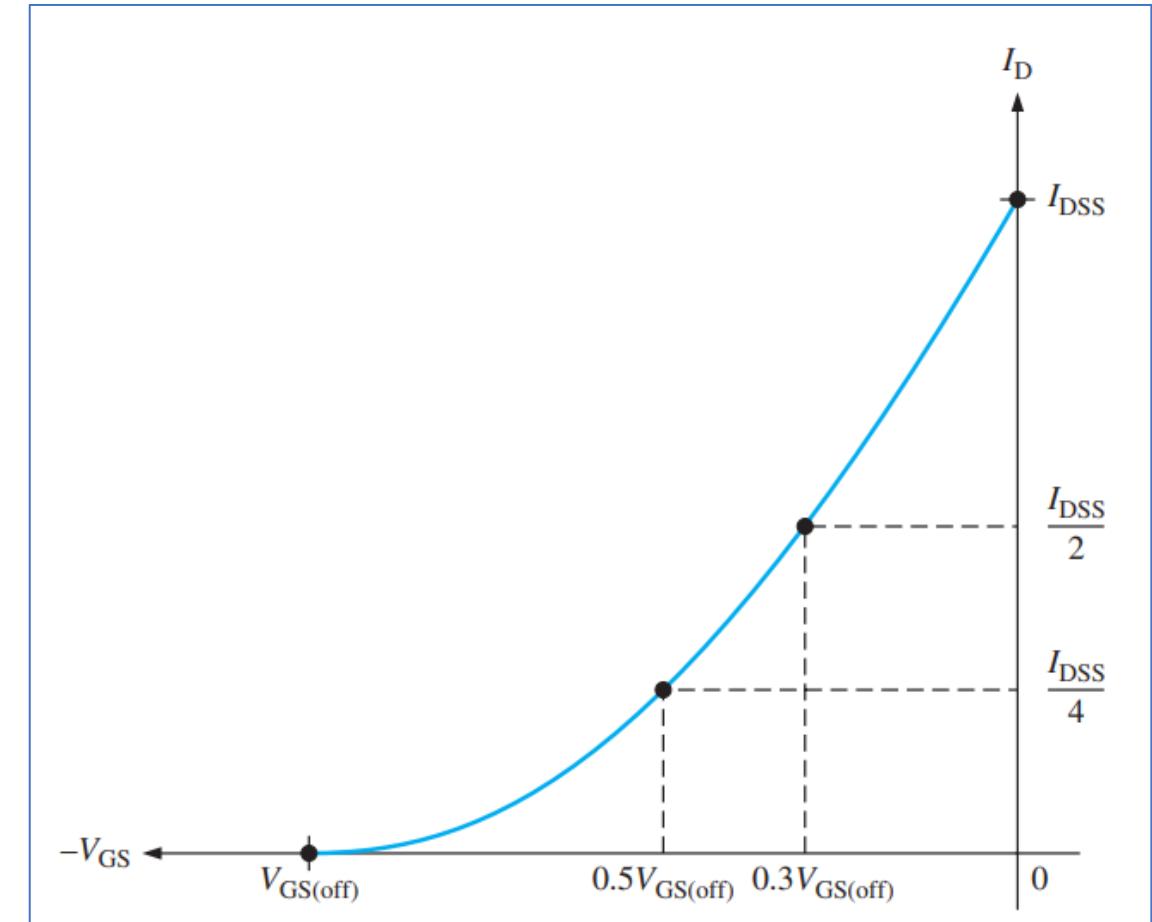
- The pinch-off voltage  $V_P$  is the value of  $V_{DS}$  at which the drain current becomes constant and equal to  $I_{DSS}$  and is always measured at  $V_{GS} = 0$  V.
- However pinch-off occurs for  $V_{DS}$  values less than  $V_P$  when  $V_{GS}$  is nonzero.
- So, although  $V_P$  is a constant, the minimum value of  $V_{DS}$  at which  $I_D$  becomes constant varies with  $V_{GS}$ .
- $V_{GS(off)}$  and  $V_P$  are always equal in magnitude but opposite in sign.
- A datasheet usually will give either  $V_{GS(off)}$  or  $V_P$ , but not both.
- However, when you know one, you have the other. For example, if  $V_{GS(off)} = -5$  V,  $V_P = +5$  V, as shown in Figure (b).



# JFET'S CHARACTERISTICS AND PARAMETERS

- JFET Universal Transfer Characteristic**

- A range of  $V_{GS}$  values from zero to  $V_{GS(off)}$  controls the amount of drain current.
- For an n-channel JFET,  $V_{GS(off)}$  is negative, and for a p-channel JFET,  $V_{GS(off)}$  is positive. Because  $V_{GS}$  does control  $I_D$ , the relationship between these two quantities is very important.
- Figure is a general transfer characteristic curve that illustrates graphically the relationship between  $V_{GS}$  and  $I_D$ .
- This curve is also known as a transconductance curve.



# JFET'S CHARACTERISTICS AND PARAMETERS

- JFET Universal Transfer Characteristic**

- Notice that the bottom end of the curve is at a point on the  $V_{GS}$  axis equal to  $V_{GS(off)}$ ,
- and the top end of the curve is at a point on the  $I_D$  axis equal to  $I_{DSS}$ . This curve shows that

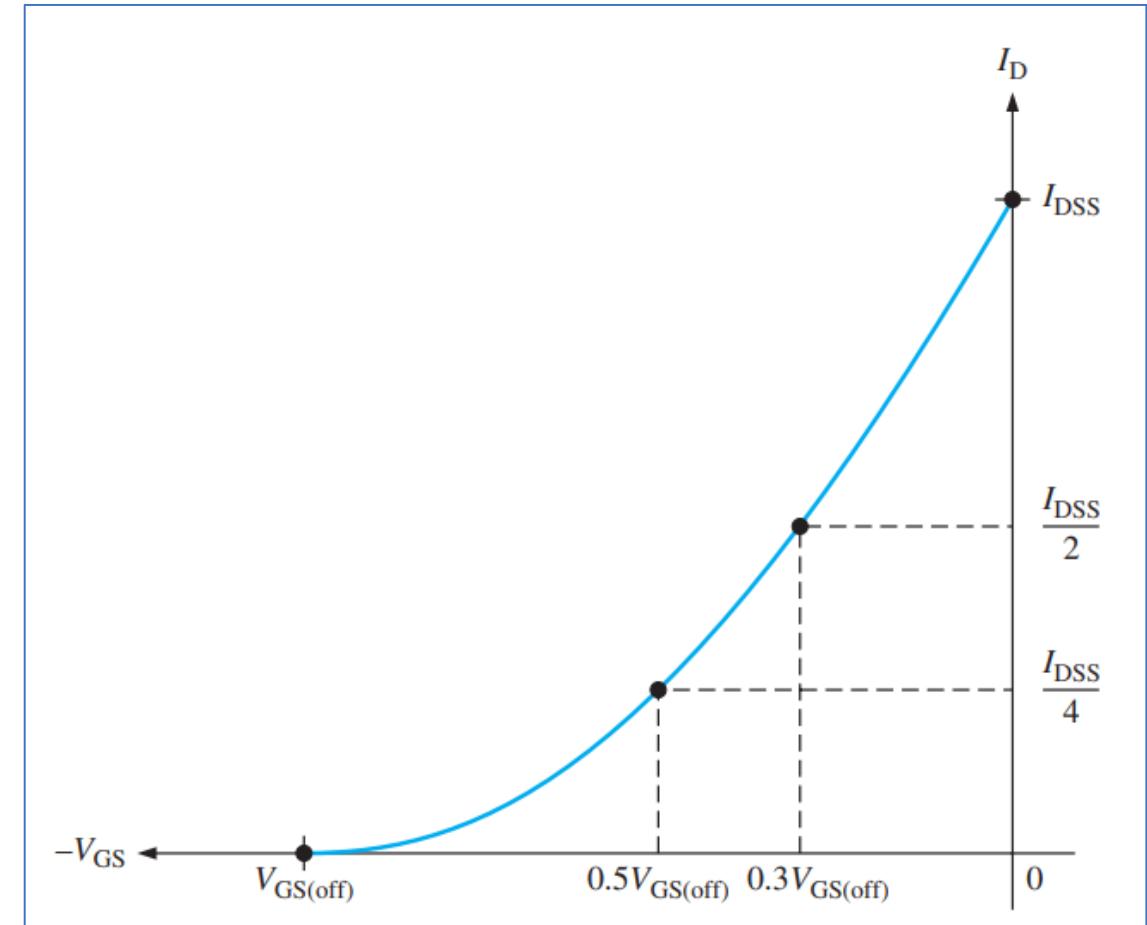
$$I_D = 0 \quad \text{when } V_{GS} = V_{GS(off)}$$

$$I_D = \frac{I_{DSS}}{4} \quad \text{when } V_{GS} = 0.5V_{GS(off)}$$

$$I_D = \frac{I_{DSS}}{2} \quad \text{when } V_{GS} = 0.3V_{GS(off)}$$

and

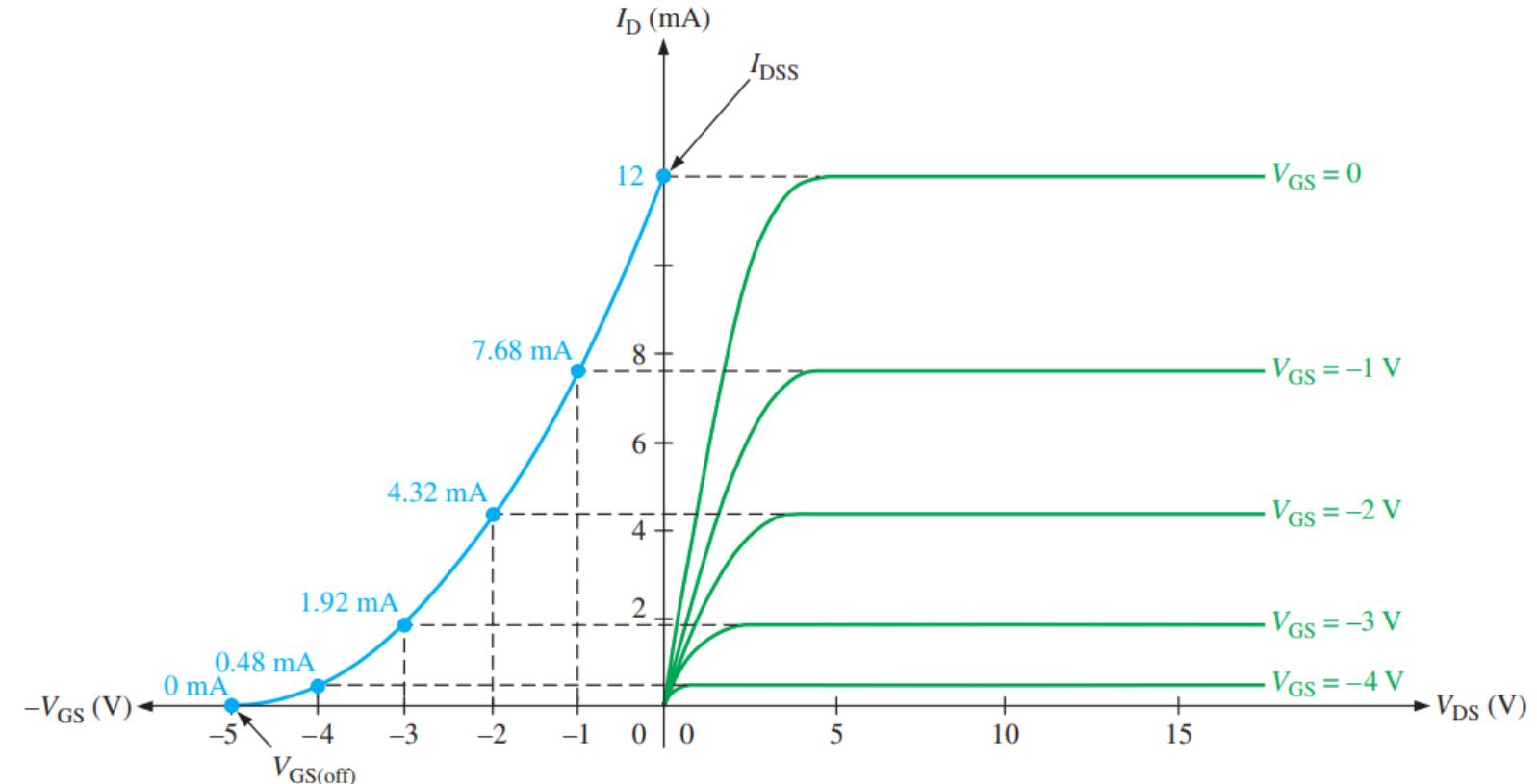
$$I_D = I_{DSS} \quad \text{when } V_{GS} = 0$$



# JFET'S CHARACTERISTICS AND PARAMETERS

- JFET Universal Transfer Characteristic**

- The transfer characteristic curve can also be developed from the drain characteristic curves by plotting values of  $I_D$  for the values of  $V_{GS}$  taken from the family of drain curves at pinch-off, as illustrated in Figure for a specific set of curves.
- Each point on the transfer characteristic curve corresponds to specific values of  $V_{GS}$  and  $I_D$  on the drain curves.
- For example, when Also, for this specific JFET,  $V_{GS(off)} = -5$  V and  $I_{DSS} = 12$  mA.



Example of the development of an n-channel JFET transfer characteristic curve (blue) from the JFET drain characteristic curves (green).

Acknowledgment:-Thomas L. Floyd Electronic Devices, Electron Flow Version, Ninth Edition

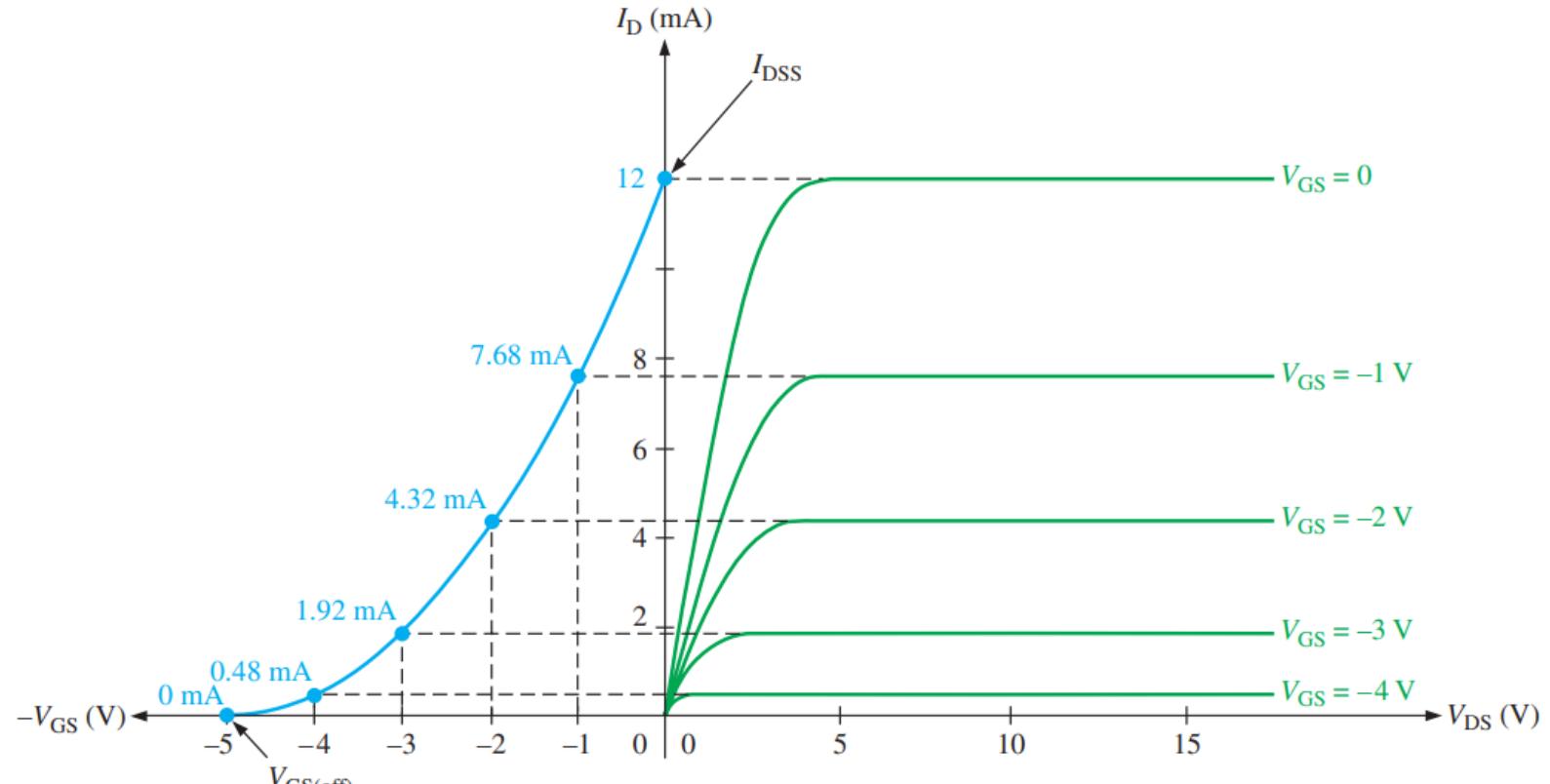
# JFET'S CHARACTERISTICS AND PARAMETERS

- JFET Universal Transfer Characteristic**

- A JFET transfer characteristic curve is expressed approximately as

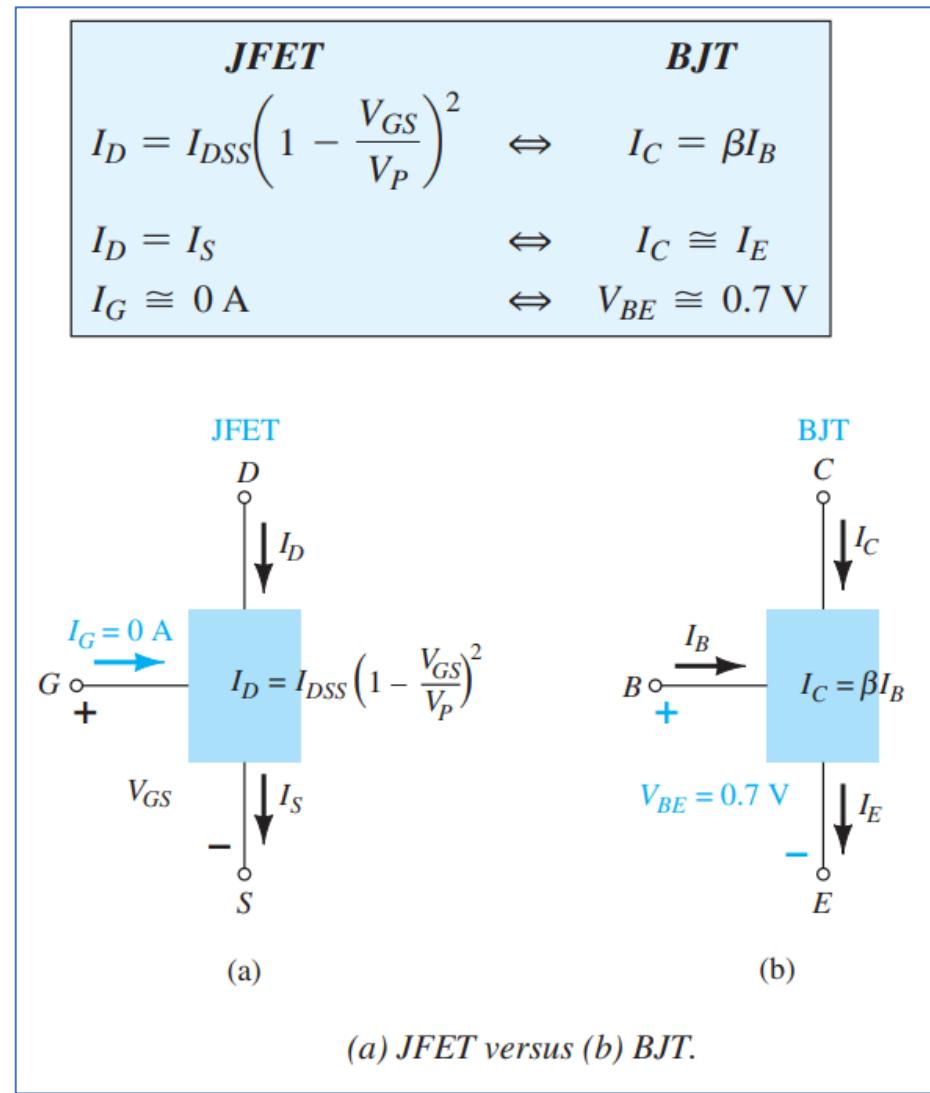
$$I_D \cong I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

- With Equation,  $I_D$  can be determined for any  $V_{GS}$  if  $V_{GS(off)}$  and  $I_{DSS}$  are known.
- Notice the squared term in the equation. Because of its form, a parabolic relationship is known as a square law, and therefore, JFETs and MOSFETs are often referred to as square-law devices



Example of the development of an n-channel JFET transfer characteristic curve (blue) from the JFET drain characteristic curves (green).

# Important relationship JFET versus BJT

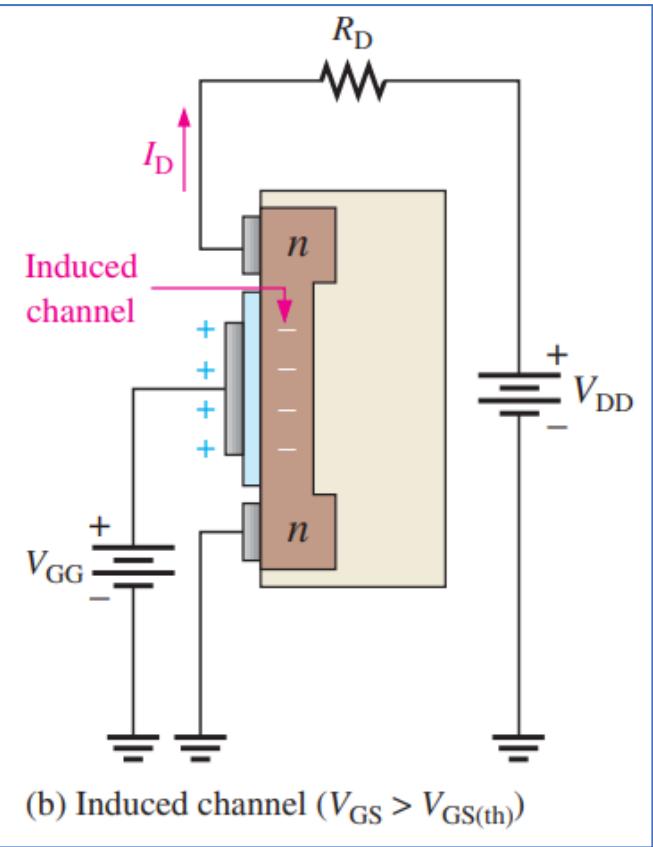
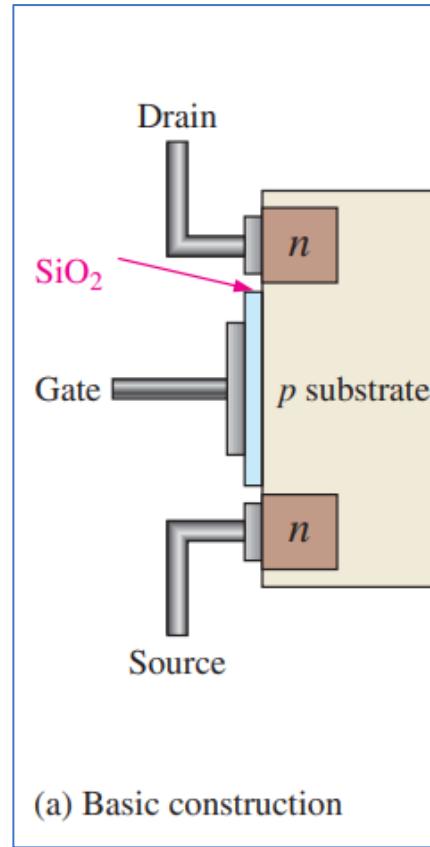
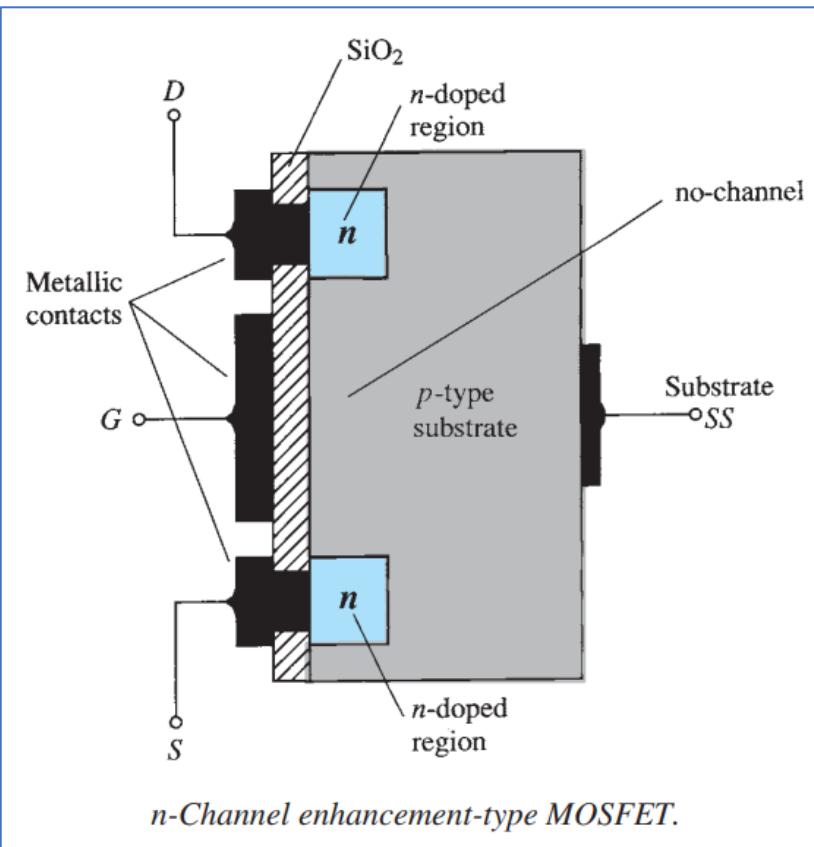


# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- The MOSFET (metal oxide semiconductor field-effect transistor) is another category of field-effect transistor.
- The MOSFET, different from the JFET, has no pn junction structure; instead, the gate of the MOSFET is insulated from the channel by a **silicon dioxide (SiO<sub>2</sub>)** layer.
- The two basic types of MOSFETs are **enhancement (E)** and **depletion (D)**.
- Of the two types, the **enhancement MOSFET** is more widely used.
- Because polycrystalline silicon is now used for the gate material instead of metal, these devices are sometimes called IGFETs (insulated-gate FETs)

# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- Basic Construction-Enhancement MOSFET (E-MOSFET)



Representation of the basic E-MOSFET construction and operation (n-channel)

Acknowledgment:-Electronic Devices and Circuit Theory, Boylestad and Nashelsky, 11th Edition

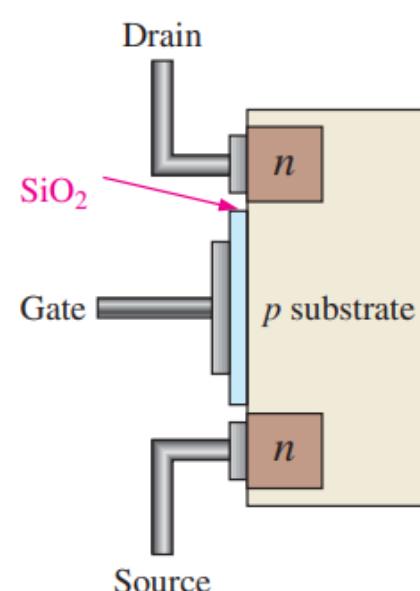
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Acknowledgment:-Thomas L. Floyd Electronic Devices, Electron Flow Version, Ninth Edition

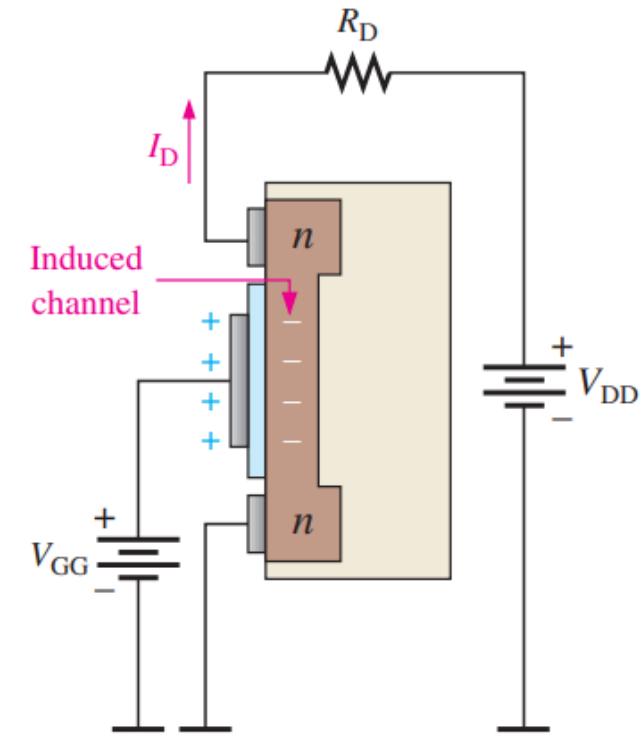
# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- Enhancement MOSFET (E-MOSFET)

- The E-MOSFET operates only in the enhancement mode and has no depletion mode.
- It differs in construction from the D-MOSFET, in that it has no structural channel.
- Notice in Figure (a) that the substrate extends completely to the  $\text{SiO}_2$  layer.
- For an n-channel device, a positive gate voltage above a threshold value induces a channel by creating a thin layer of negative charges in the substrate region adjacent to the  $\text{SiO}_2$  layer, as shown in Figure (b).
- The conductivity of the channel is enhanced by increasing the gate-to-source voltage and thus pulling more electrons into the channel area.
- For any gate voltage below the threshold value, there is no channel.



(a) Basic construction



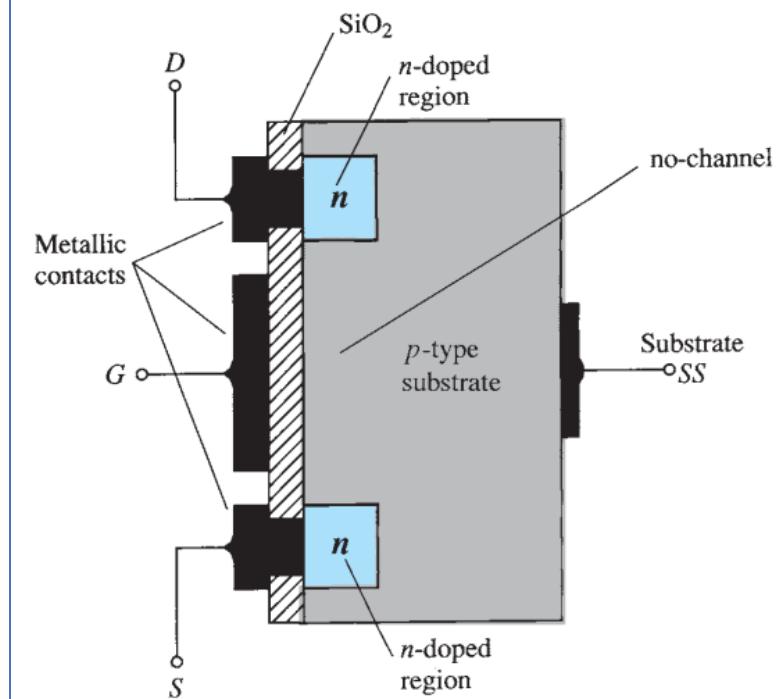
(b) Induced channel ( $V_{\text{GS}} > V_{\text{GS(th)}}$ )

Representation of the basic E-MOSFET construction and operation (n-channel)

# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- Basic Operation and Characteristics: Enhancement MOSFET (E-MOSFET)**

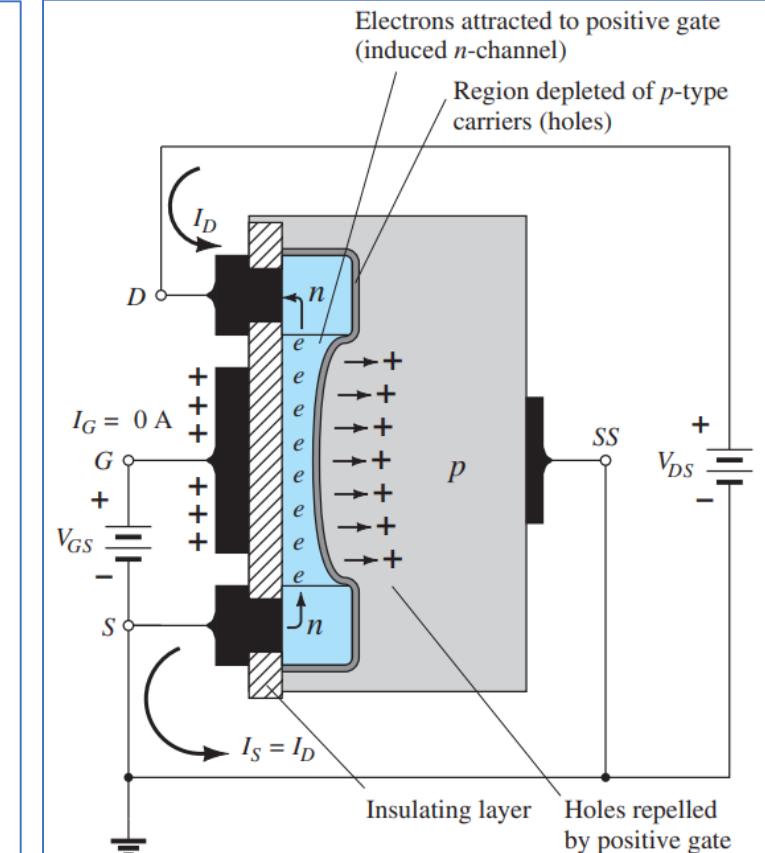
- If  $V_{GS}$  is set at 0 V and a voltage applied between the drain and the source of the device of Fig. , the absence of an n -channel (with its generous number of free carriers) will result in a current of effectively 0 A
- With  $V_{DS}$  some positive voltage,  $V_{GS}$  at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased p – n junctions between the n -doped regions and the p -substrate to oppose any significant flow between drain and source.



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- In Fig., both  $V_{DS}$  and  $V_{GS}$  have been set at some positive voltage greater than 0 V, establishing the drain and the gate at a positive potential with respect to the source.
- The positive potential at the gate will pressure the holes (since like charges repel) in the p -substrate along the edge of the  $\text{SiO}_2$  layer to leave the area and enter deeper regions of the p -substrate, as shown in the figure.
- The result is a depletion region near the  $\text{SiO}_2$  insulating layer void of holes.
- However, the electrons in the p -substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the  $\text{SiO}_2$  layer.
- The  $\text{SiO}_2$  layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal.
- As  $V_{GS}$  increases in magnitude, the concentration of electrons near the  $\text{SiO}_2$  surface increases until eventually the induced n -type region can support a measurable flow between drain and source.

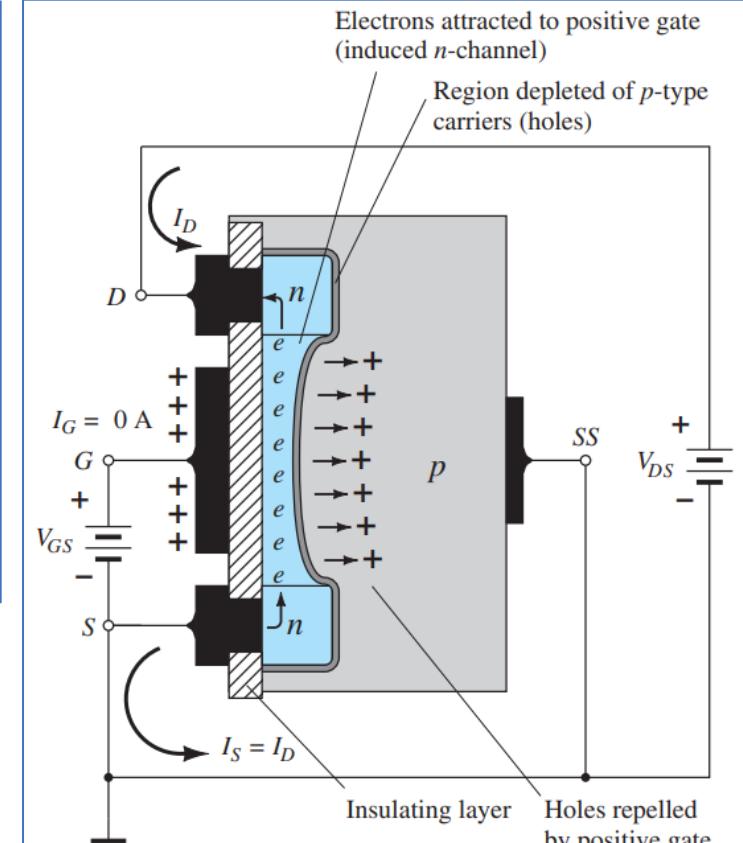


Channel formation in the n-channel enhancement-type MOSFET.

# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

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- The level of  $V_{GS}$  that results in the significant increase in drain current is called the threshold voltage and is given the symbol  $V_T$ .
- On specification sheets it is referred to as  $V_{GS(Th)}$ , although  $V_T$  is less unwieldy and will be used in the analysis to follow.
- Since the channel is nonexistent with  $V_{GS} = 0 \text{ V}$  and “enhanced” by the application of a positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET.*
- Both depletion- and enhancement-type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.



Channel formation in the n-channel enhancement-type MOSFET.

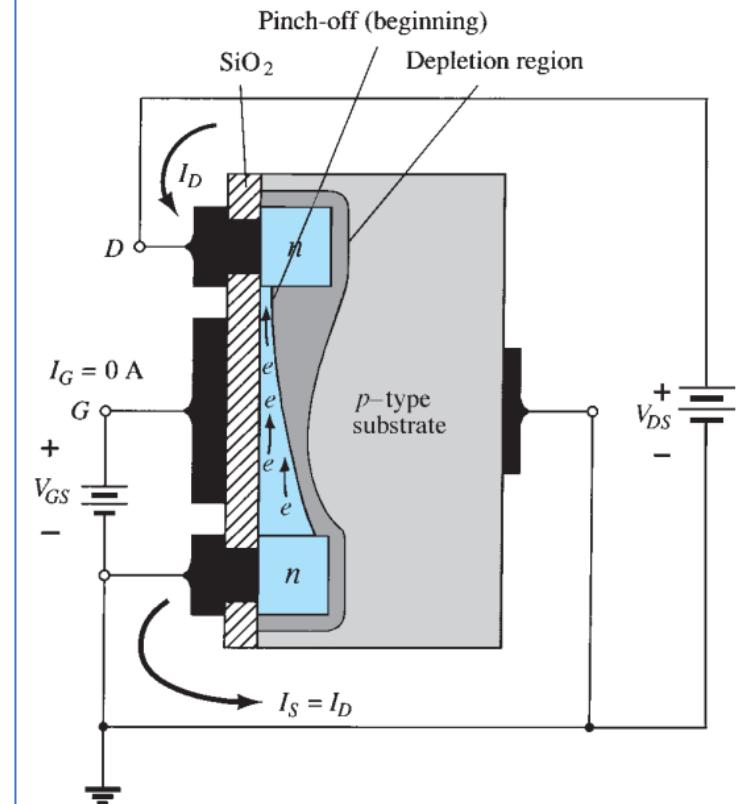
# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- Basic Operation and Characteristics: Enhancement MOSFET (E-MOSFET)**

- As  $V_{GS}$  is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current.
- However, if we hold  $V_{GS}$  constant and increase the level of  $V_{DS}$ , the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET.
- The leveling off of  $I_D$  is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig..
- Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. , we find that

$$V_{DG} = V_{DS} - V_{GS}$$

- If  $V_{GS}$  is held fixed at some value such as 8 V and  $V_{DS}$  is increased from 2 V to 5 V, the voltage  $V_{DG}$  [by Eq.] will increase from -6 V to -3 V and the gate will become less and less positive with respect to the drain.
- This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width.



Change in channel and depletion region with increasing level of  $V_{DS}$  for a fixed value of  $V_{GS}$ .

# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

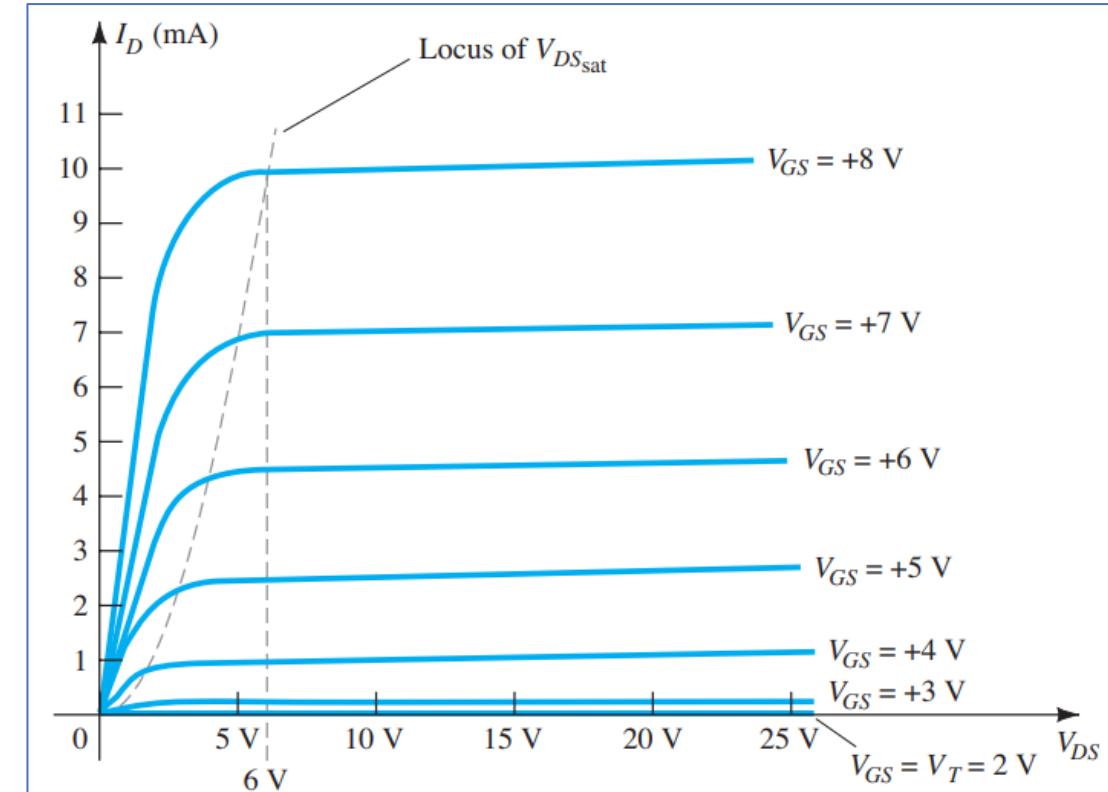
- Basic Operation and Characteristics: Enhancement MOSFET (E-MOSFET)**

- The drain characteristics of Fig. reveal that for the device with  $V_{GS} = 8 \text{ V}$ , saturation occurs at a level of  $V_{DS} = 6 \text{ V}$ .
- In fact, the saturation level for  $V_{DS}$  is related to the level of applied  $V_{GS}$  by.

$$V_{DS_{sat}} = V_{GS} - V_T$$

- Obviously, therefore, for a fixed value of  $V_T$ , the higher the level of  $V_{GS}$ , the greater is the saturation level for  $V_{DS}$ , as shown in Fig. by the locus of saturation levels.

For values of  $V_{GS}$  less than the threshold level, the drain current of an enhancement type MOSFET is 0 mA.



Drain characteristics of an n-channel enhancement-type MOSFET with  $V_T = 2 \text{ V}$  and  $k = 0.278 \times 10^{-3} \text{ A/V}^2$ .

# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- Basic Operation and Characteristics: Enhancement MOSFET (E-MOSFET)**

- Figure clearly reveals that as the level of  $V_{GS}$  increases from  $V_T$  to 8 V, the resulting saturation level for  $I_D$  also increases from a level of 0 mA to 10 mA.
- In addition, it is quite noticeable that the spacing between the levels of  $V_{GS}$  increases as the magnitude of  $V_{GS}$  increases, resulting in ever-increasing increments in drain current.

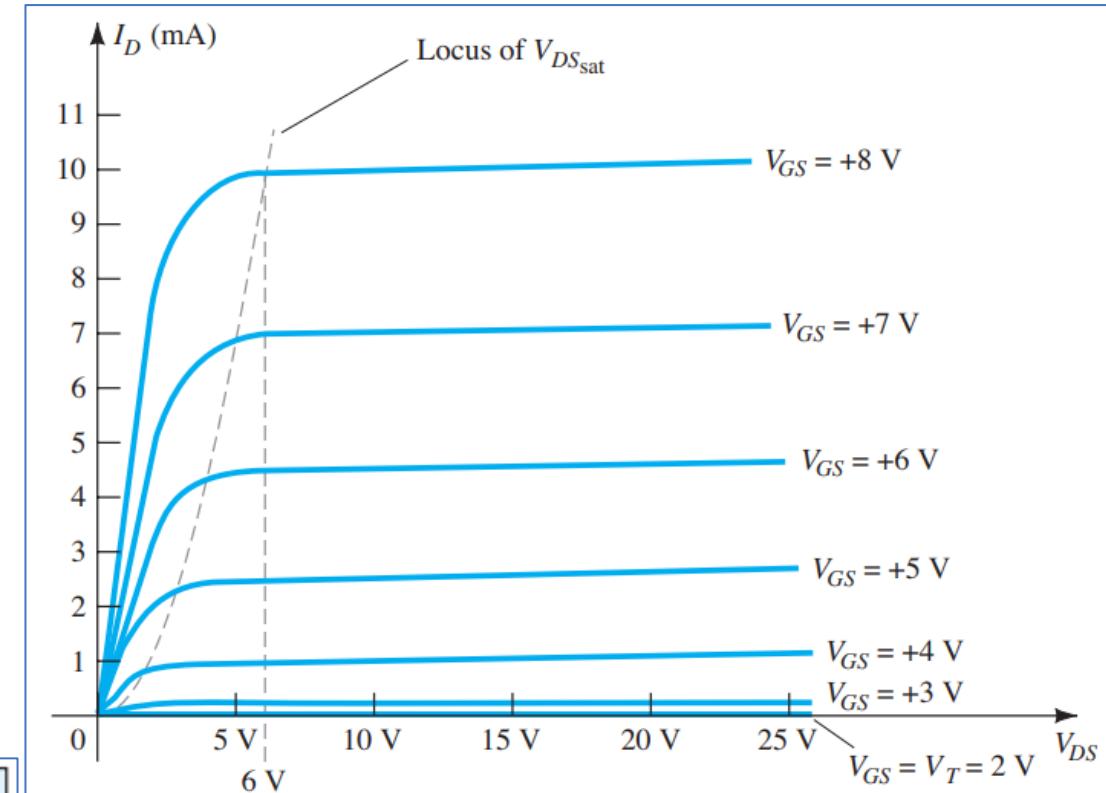
For levels of  $V_{GS} > V_T$ , the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

Again, it is the squared term that results in the nonlinear (curved) relationship between  $I_D$  and  $V_{GS}$ .

The  $k$  term is a constant that is a function of the construction of the device.

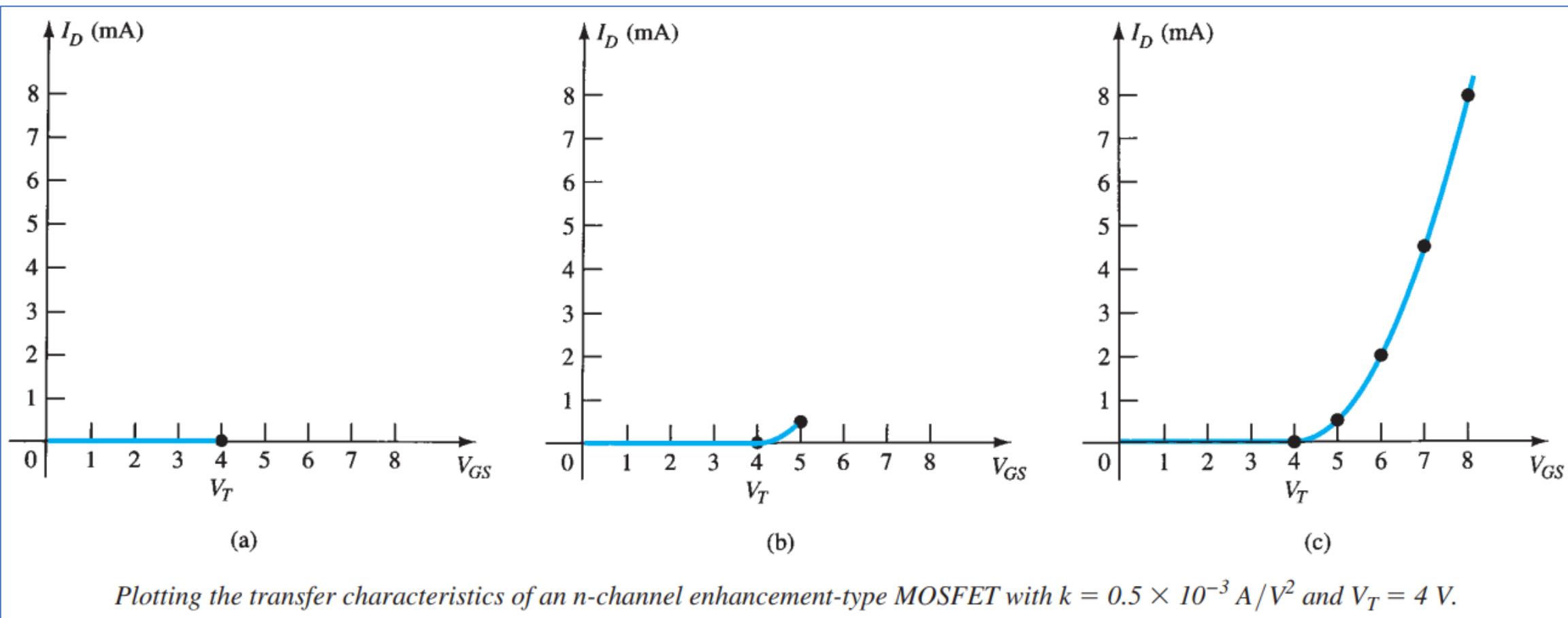
$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2}$$



Drain characteristics of an n-channel enhancement-type MOSFET with  $V_T = 2\text{ V}$  and  $k = 0.278 \times 10^{-3}\text{ A/V}^2$ .

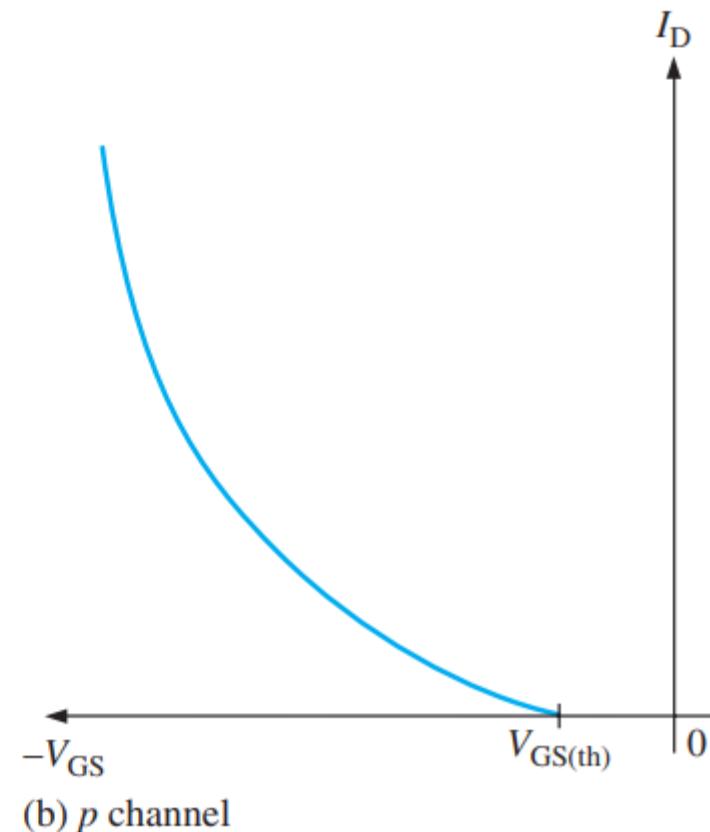
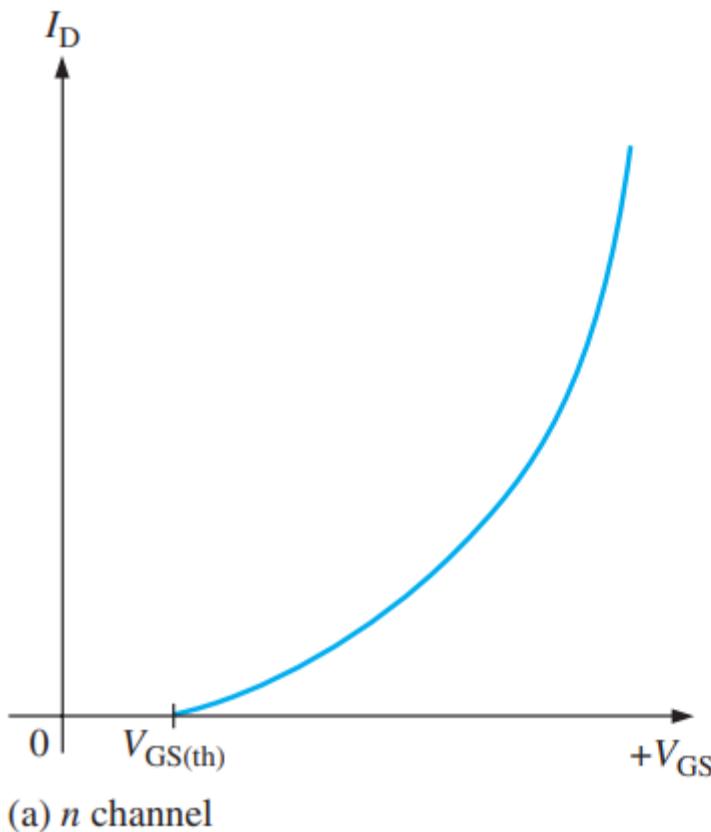
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# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- Basic Operation and Characteristics: Enhancement MOSFET (E-MOSFET) Transfer Characteristics



The equation for the E-MOSFET transfer characteristic curve is

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

The constant  $K$  depends on the particular MOSFET and can be determined from the datasheet by taking the specified value of  $I_D$ , called  $I_{D(on)}$ , at the given value of  $V_{GS}$  and substituting the values into Equation.

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**EXAMPLE** The datasheet (see [www.fairchild.com](http://www.fairchild.com)) for a 2N7002 E-MOSFET gives  $I_{D(on)} = 500 \text{ mA}$  (minimum) at  $V_{GS} = 10 \text{ V}$  and  $V_{GS(th)} = 1 \text{ V}$ . Determine the drain current for  $V_{GS} = 5 \text{ V}$ .

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$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17 \text{ mA/V}^2)(5 \text{ V} - 1 \text{ V})^2 = 98.7 \text{ mA}$$

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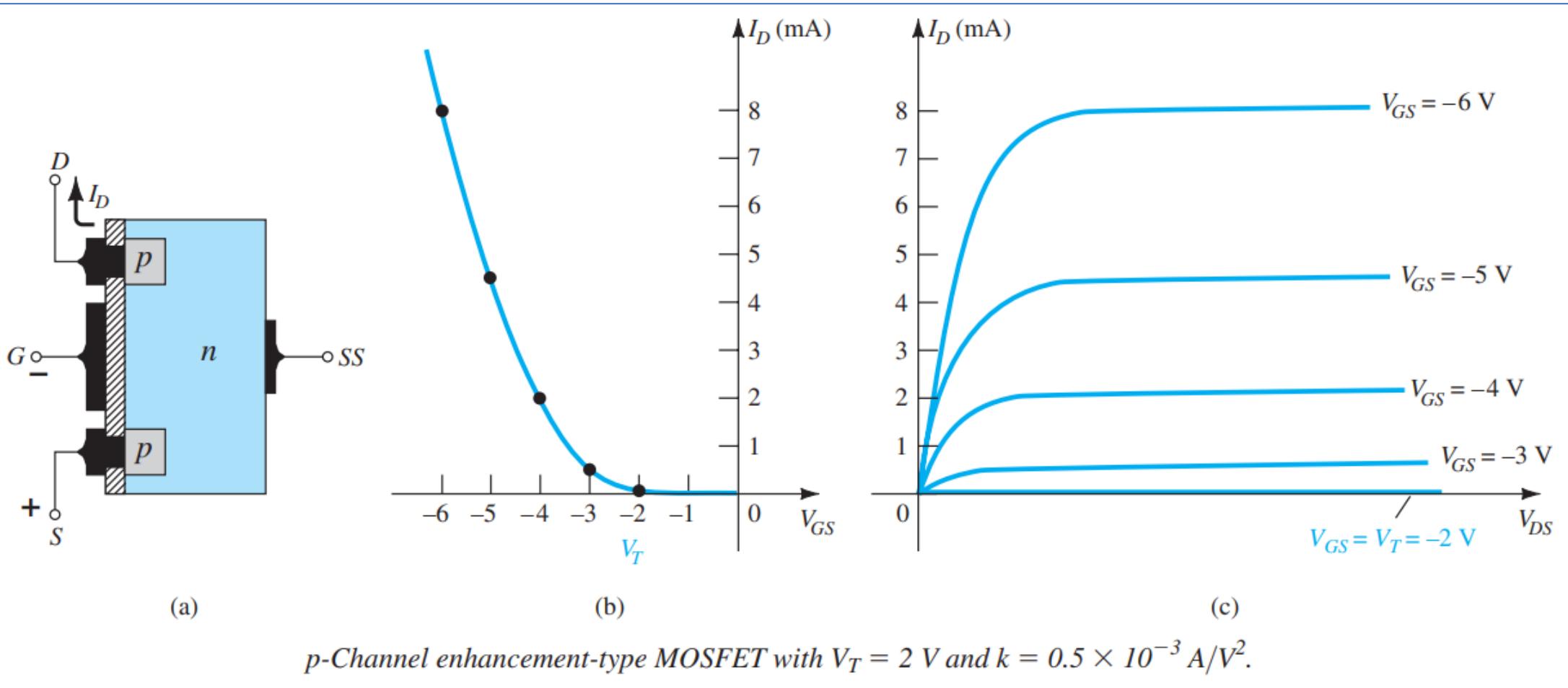
$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17 \text{ mA/V}^2)(5 \text{ V} - 1 \text{ V})^2 = 98.7 \text{ mA}$$

**Related Problem** The datasheet for an E-MOSFET gives  $I_{D(on)} = 100 \text{ mA}$  at  $V_{GS} = 8 \text{ V}$  and  $V_{GS(th)} = 4 \text{ V}$ . Find  $I_D$  when  $V_{GS} = 6 \text{ V}$ .

# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- p -Channel Enhancement-Type MOSFETs

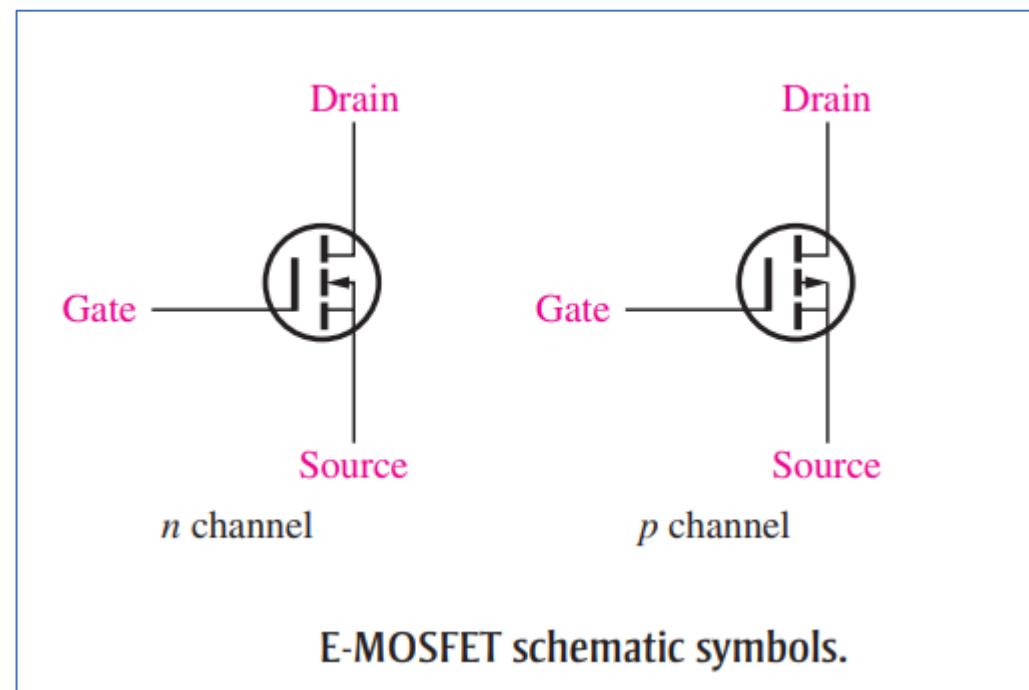
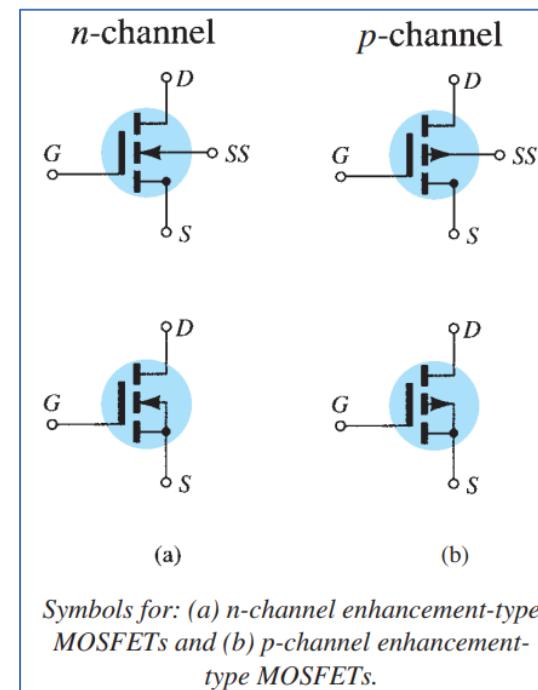
The construction of a p -channel enhancement-type MOSFET is exactly the reverse of that n -channel MOSFET



# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- Enhancement MOSFET (E-MOSFET)

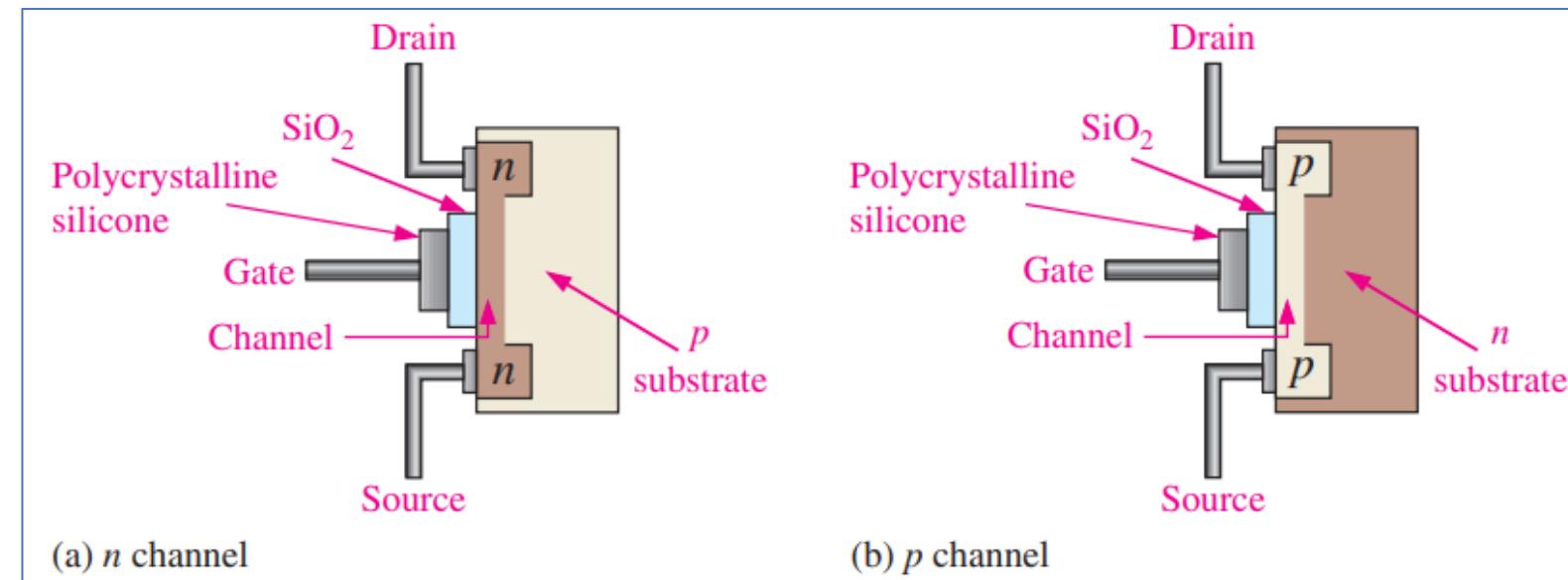
- The schematic symbols for the n-channel and p-channel E-MOSFETs are shown in Figure.
- The broken lines symbolize the absence of a physical channel. An inward-pointing substrate arrow is for n channel, and an outward-pointing arrow is for p channel.
- Some E-MOSFET devices have a separate substrate connection.



# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- **Depletion MOSFET (D-MOSFET)**

- Another type of MOSFET is the depletion MOSFET (D-MOSFET), and Figure illustrates its basic structure.
- The drain and source are diffused into the substrate material and then connected by a narrow channel adjacent to the insulated gate.
- Both n-channel and p-channel devices are shown in the figure.
- We will use the n-channel device to describe the basic operation.
- The p-channel operation is the same, except the voltage polarities are opposite those of the n-channel.



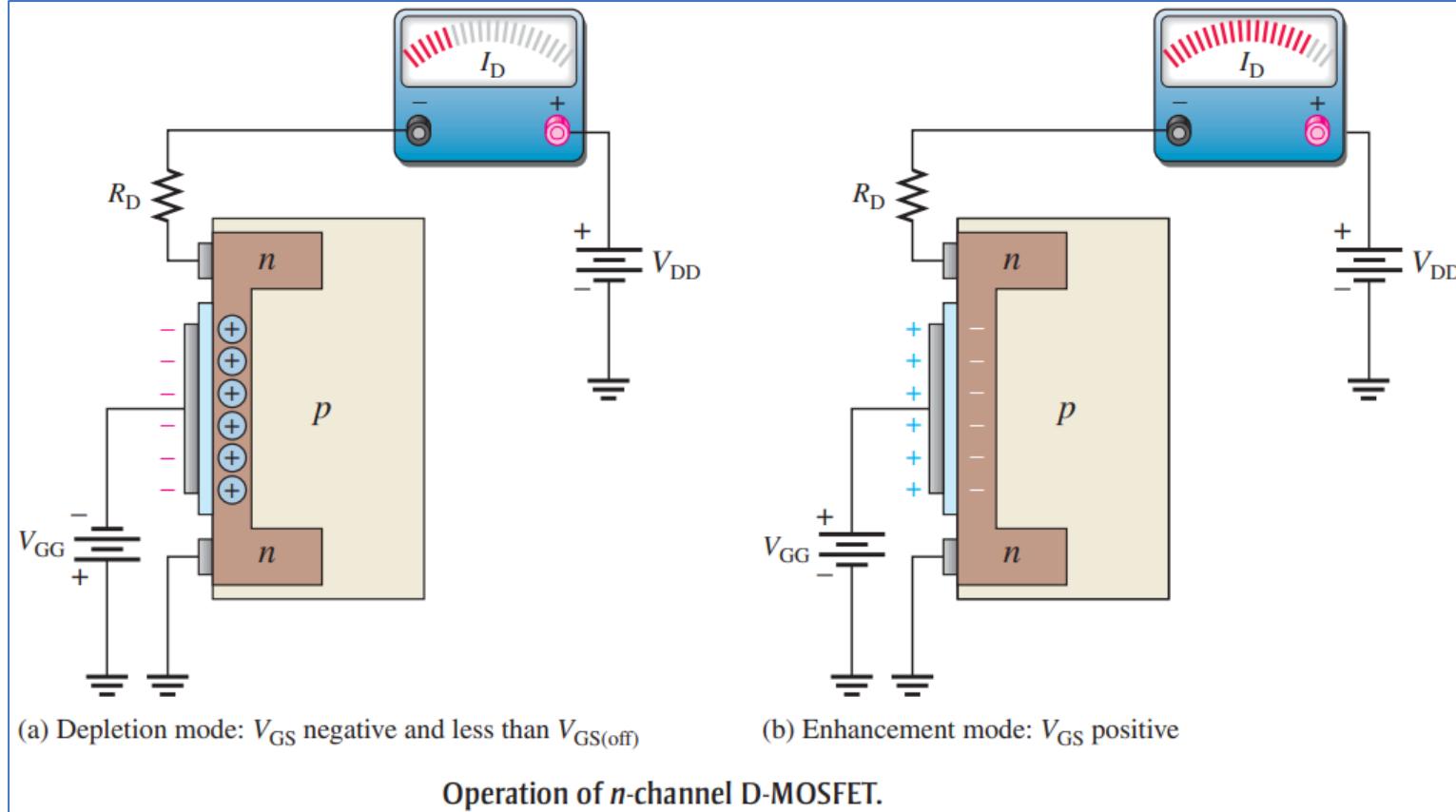
Representation of the basic structure of D-MOSFETs.

Acknowledgment:-Thomas L. Floyd Electronic Devices, Electron Flow Version, Ninth Edition

# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- **Depletion MOSFET (D-MOSFET)**

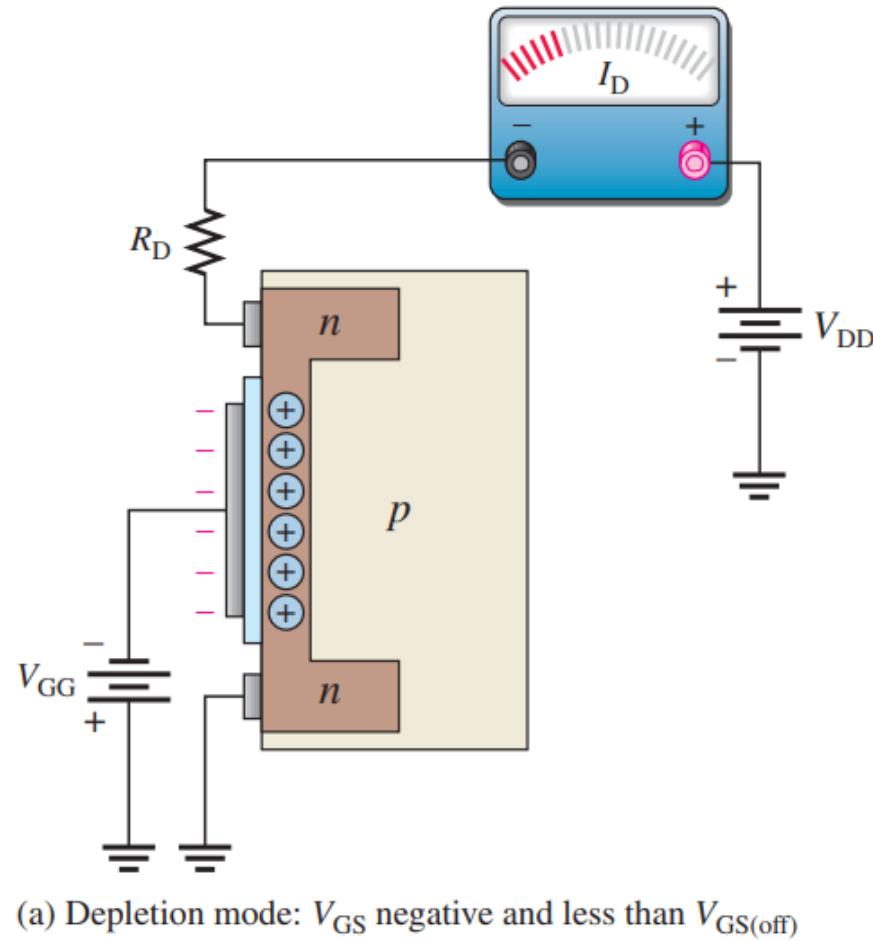
- The D-MOSFET can be operated in either of two modes—the **depletion mode or the enhancement mode**—and is sometimes called a depletion/enhancement MOSFET.
- Since the gate is insulated from the channel, **either a positive or a negative gate voltage** can be applied.
- *The n-channel MOSFET operates in the depletion mode when a negative gate-to-source voltage is applied and in the enhancement mode when a positive gate-to-source voltage is applied.*
- These devices are generally operated in the depletion mode.



# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- Depletion MOSFET (D-MOSFET)

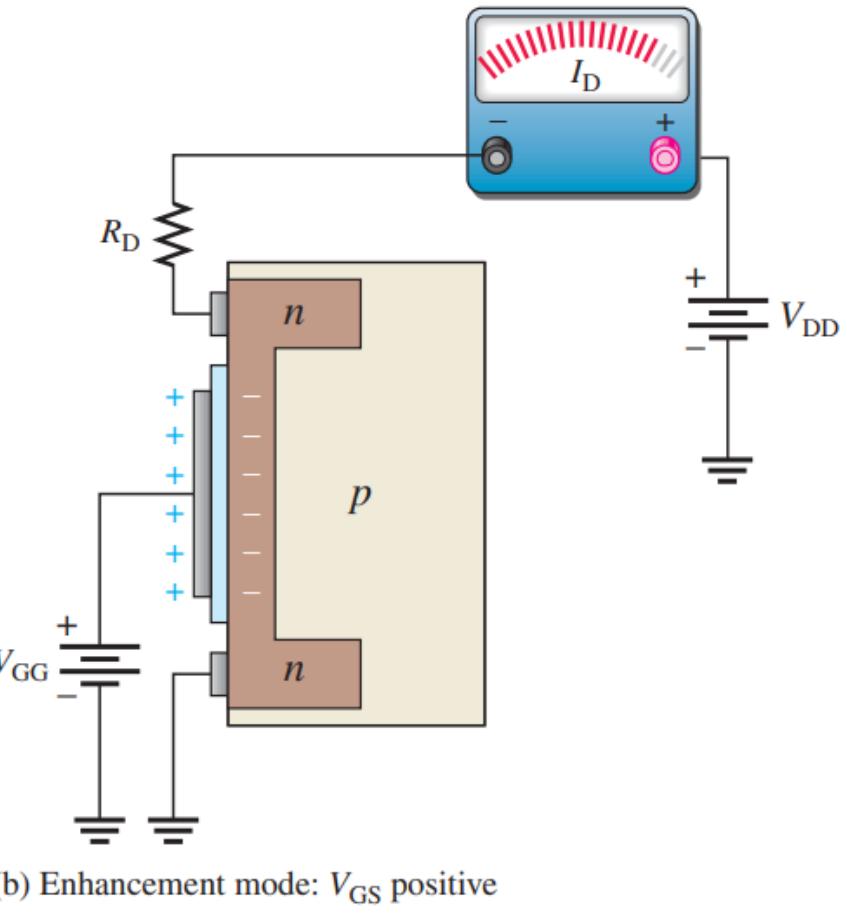
- **Depletion Mode**
- Visualize the gate as one plate of a parallel-plate capacitor and the channel as the other plate.
- The silicon dioxide insulating layer is the dielectric.
- With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place.
- Thereby, the n channel is depleted of some of its electrons, thus decreasing the channel conductivity.
- The greater the negative voltage on the gate, the greater the depletion of n-channel electrons.
- At a sufficiently negative gate-to-source voltage,  $V_{GS(off)}$ , the channel is totally depleted and the drain current is zero. This depletion mode is illustrated in Figure(a).
- Like the n-channel JFET, the n-channel D-MOSFET conducts drain current for gate-to-source voltages between  $V_{GS(off)}$  and zero. In addition, the D-MOSFET conducts for values of  $V_{GS}$  above zero.



# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- Depletion MOSFET (D-MOSFET)

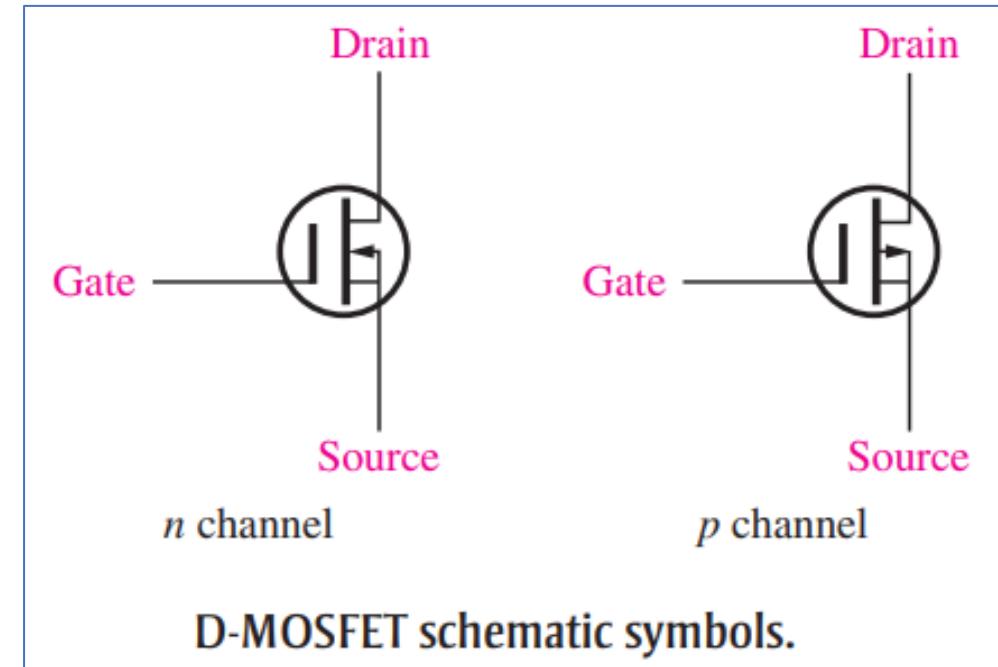
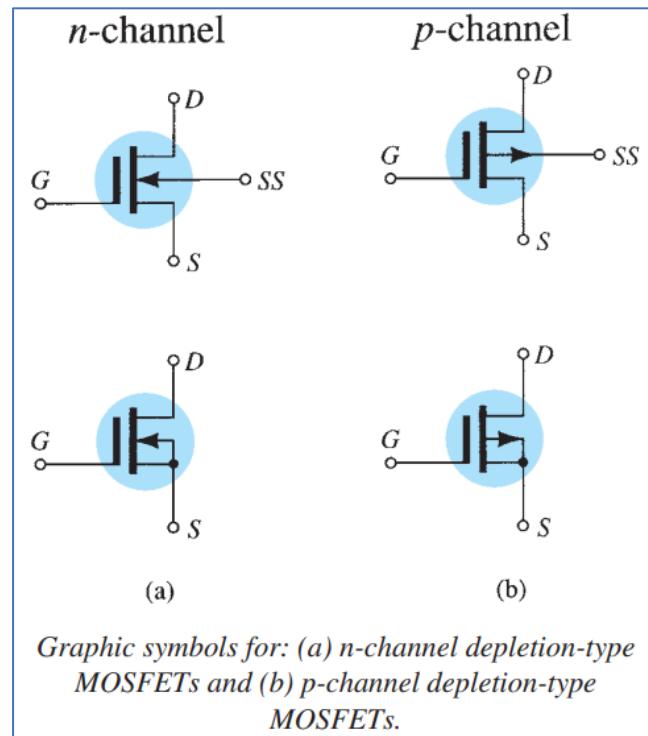
- **Enhancement Mode**
- With a positive gate voltage, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel conductivity, as illustrated in Figure (b).



# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

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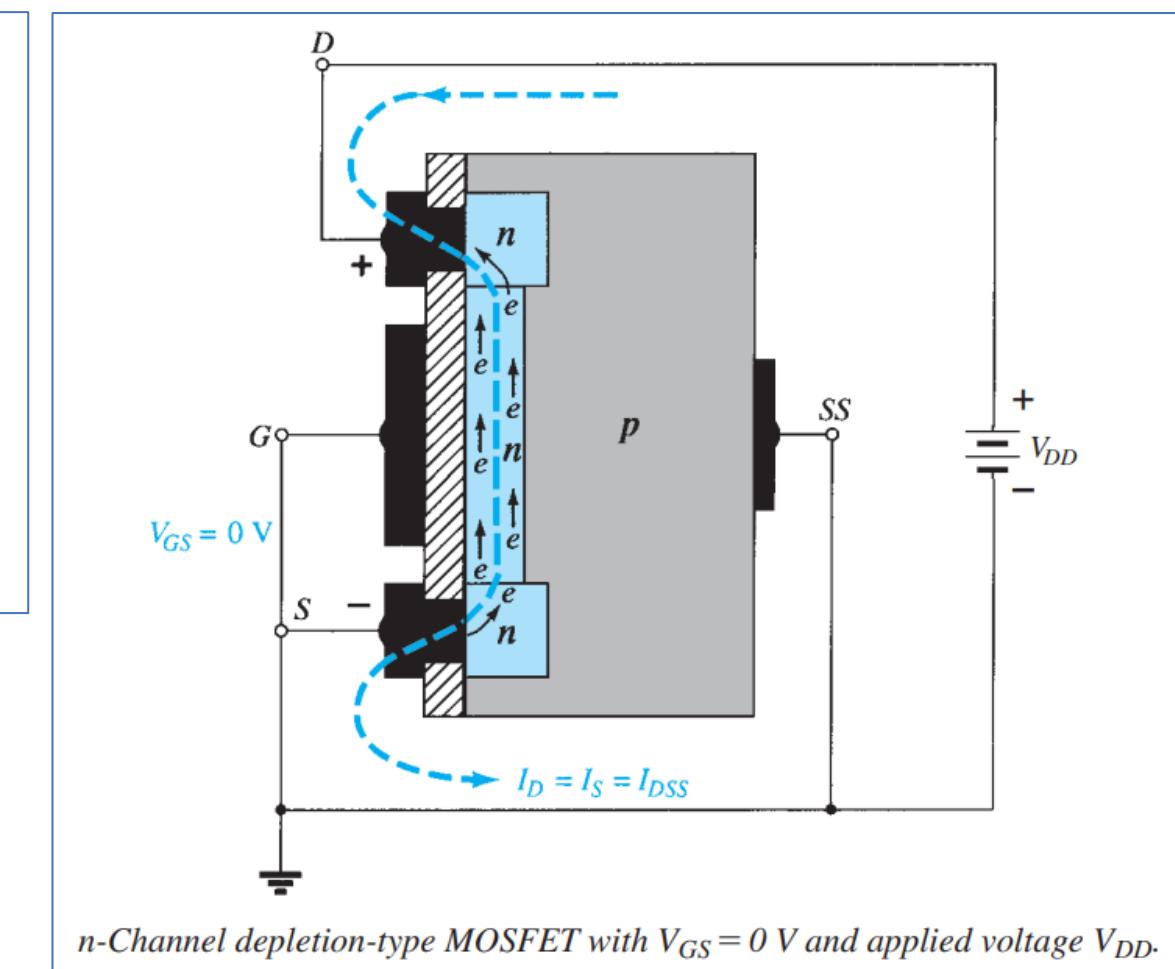
- D-MOSFET Symbols The schematic symbols for both the n-channel and the p-channel depletion MOSFETs are shown in Figure . The substrate, indicated by the arrow, is normally (but not always) connected internally to the source.
- Sometimes, there is a separate substrate pin.



# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

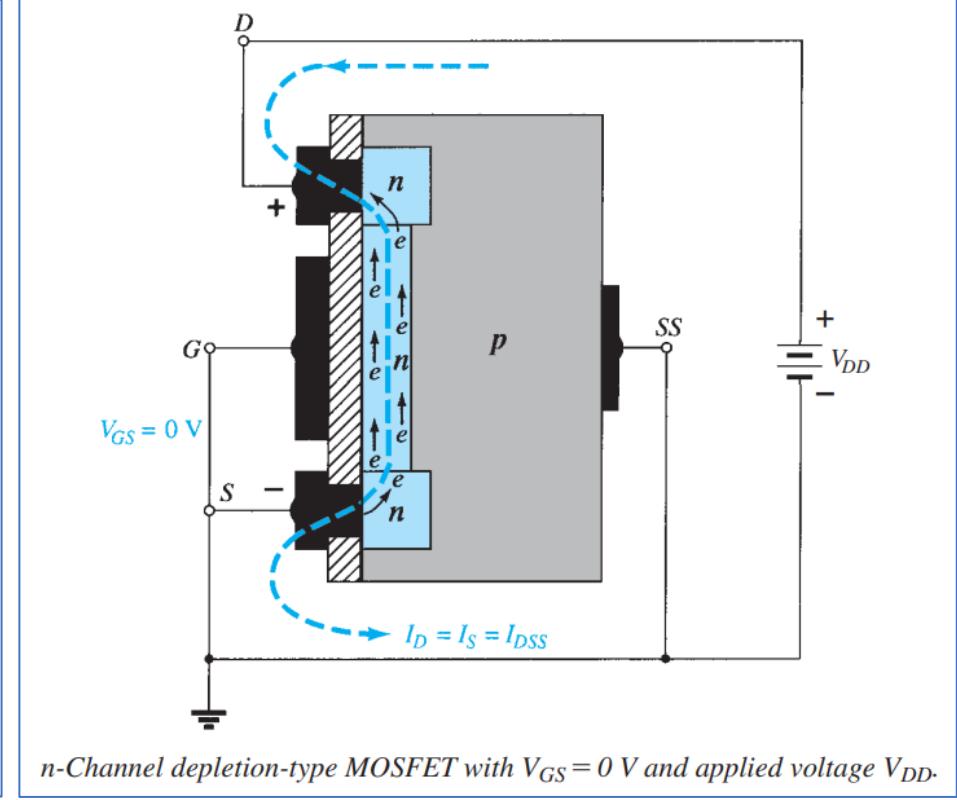
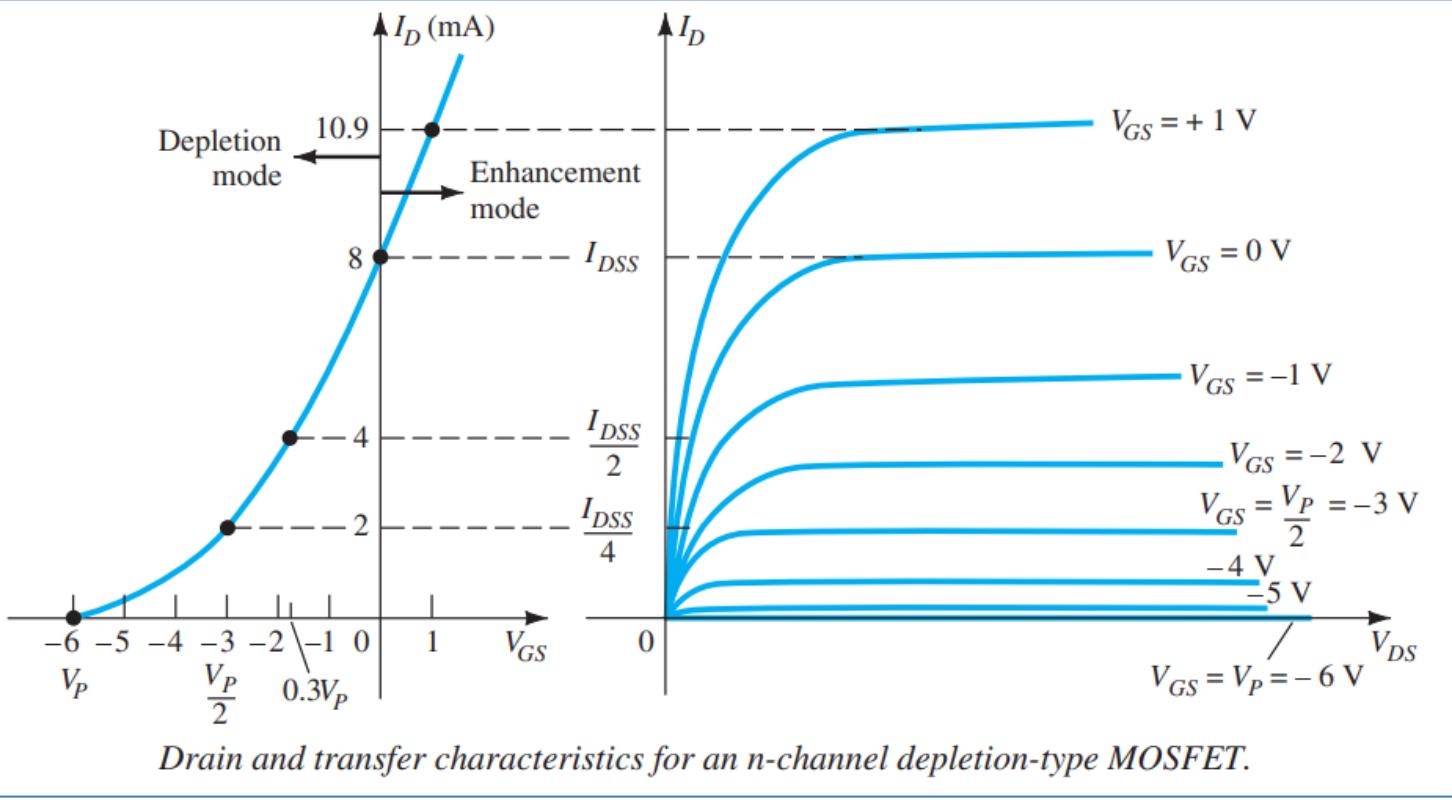
- Depletion MOSFET (D-MOSFET)

- **Basic Operation and Characteristics**
- In Fig. the gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage  $V_{DD}$  is applied across the drain-to-source terminals.
- The result is an attraction of the free electrons of the n-channel for the positive voltage at the drain.
- The result is a current similar to that flowing in the channel of the JFET.
- In fact, the resulting current with  $V_{GS} = 0$  V continues to be labeled  $I_{DSS}$ .



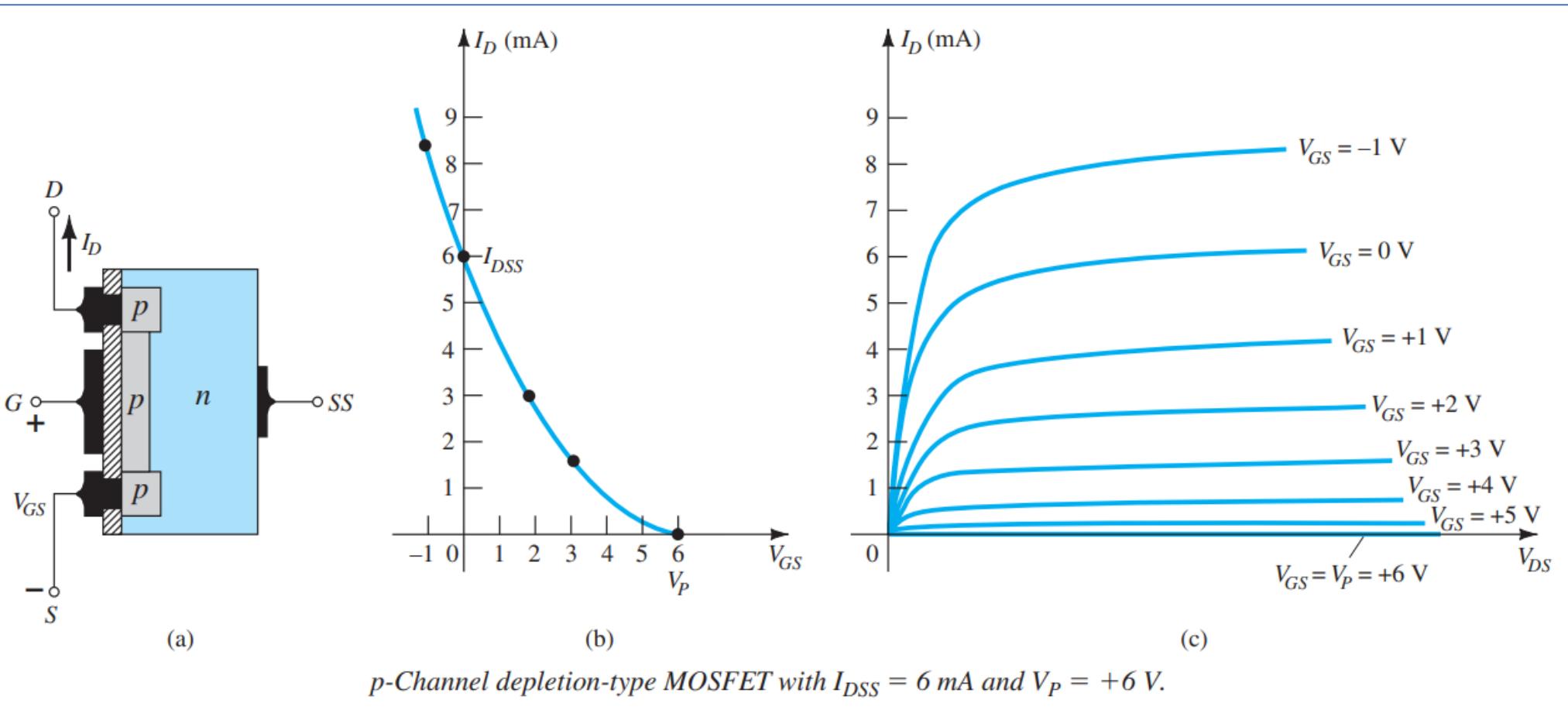
# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- Depletion MOSFET (D-MOSFET)



# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- Depletion MOSFET (D-MOSFET) *p-channel*



# The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor)

- D-MOSFET Vs E-MOSFET

## Enhancement mode

- Also known as Normally Off transistors.
  - A voltage must be applied to the gate of the transistor, at least equal to the threshold voltage, to create a conduction path between the source and the drain of the transistor before current can flow between the source and drain.

## Depletion mode

- Also known as Normally On transistors.
  - A voltage must be applied to the gate of the transistor, at least equal to the threshold voltage, to destroy a conduction path between the source and the drain of the transistor to prevent current from flowing between the source and drain.

D-MOSFET	E-MOSFET
Channel depletes with the gate voltage	Channel enhances with the gate voltage
Applying forward voltage to the gate increases the channel width.	Applying forward voltage generates and increases the width of the channel.
It can work in both depletion and enhancement mode.	It can work only in enhancement mode.
It is normally ON transistor	It is normally OFF transistor
It conducts current between its source and drain when there isn't any gate voltage	It doesnot conduct current between its source and drain when there isn't any gate voltage

## E- MOSFET biasing circuit

- Three ways to bias a MOSFET are:
- Zero-bias,
- Voltage-divider bias, and
- Drain-feedback bias.

Biasing is important in FET amplifiers

# E- MOSFET biasing circuit

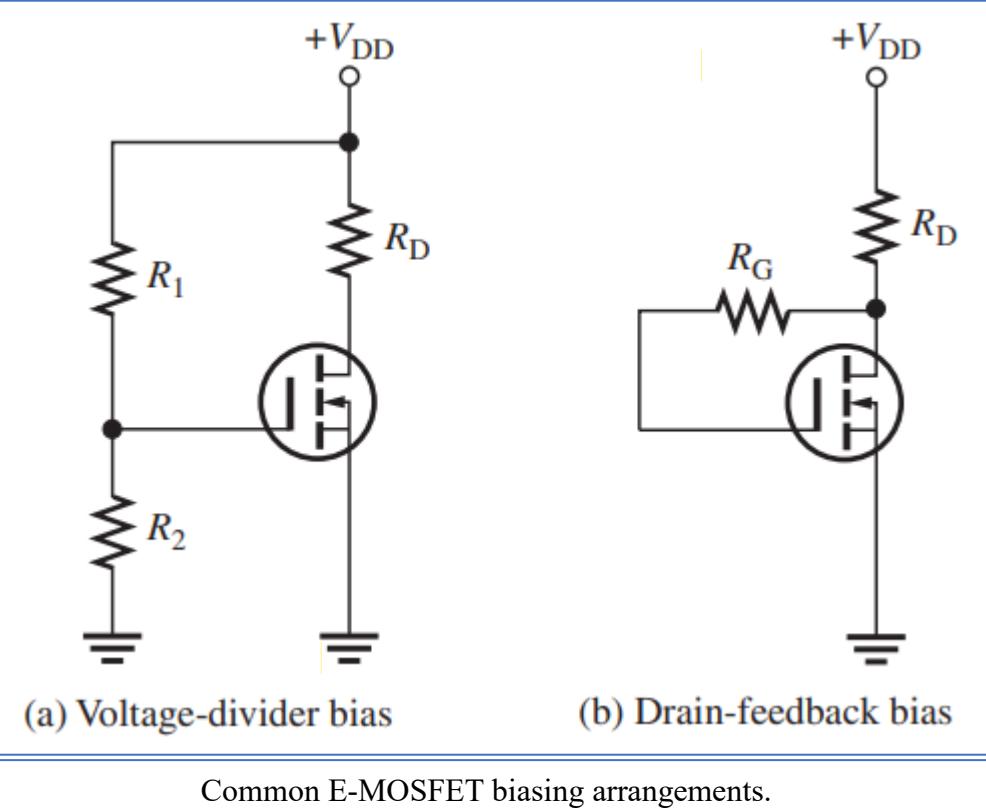
- E-MOSFETs must have a  $V_{GS}$  greater than the threshold value,  $V_{GS(th)}$ , **zero bias cannot be used**.
- Figure shows two ways to bias an E-MOSFET.
- An n-channel device is used for purposes of illustration.
- In either the voltage-divider or drain-feedback bias arrangement, the purpose is to make the gate voltage more positive than the source by an amount exceeding  $V_{GS(th)}$ .
- Equations for the analysis of the voltage-divider bias in Figure (a) are as follows:

$$V_{GS} = \left( \frac{R_2}{R_1 + R_2} \right) V_{DD}$$

$$V_{DS} = V_{DD} - I_D R_D$$

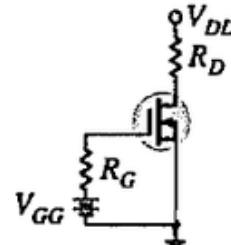
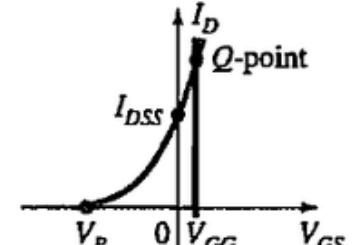
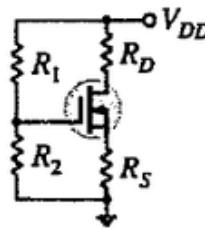
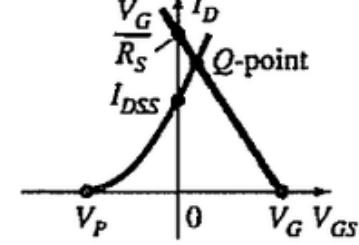
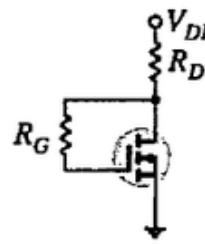
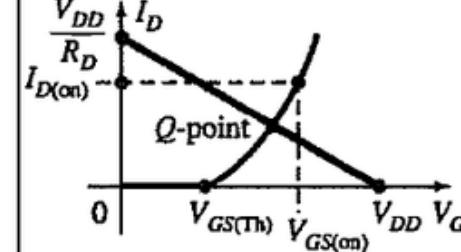
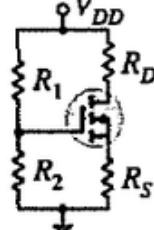
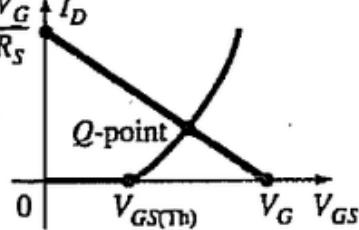
where  $I_D = K(V_{GS} - V_{GS(th)})^2$

In the drain-feedback bias circuit in Figure (b), there is negligible gate current and, therefore, no voltage drop across  $R_G$ . This makes  $V_{GS} = V_{DS}$ .



Common E-MOSFET biasing arrangements.

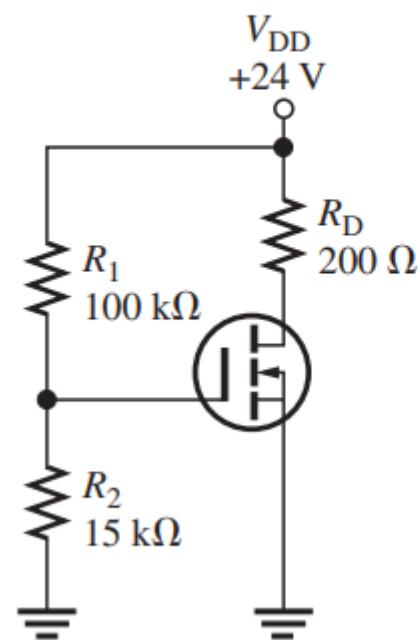
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Depletion-type MOSFET Fixed-bias		$V_{GSQ} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

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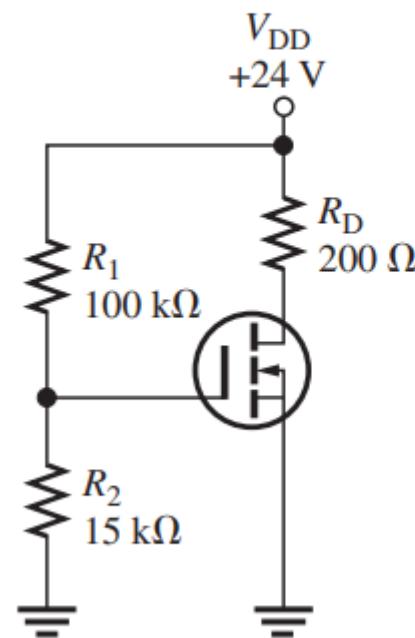
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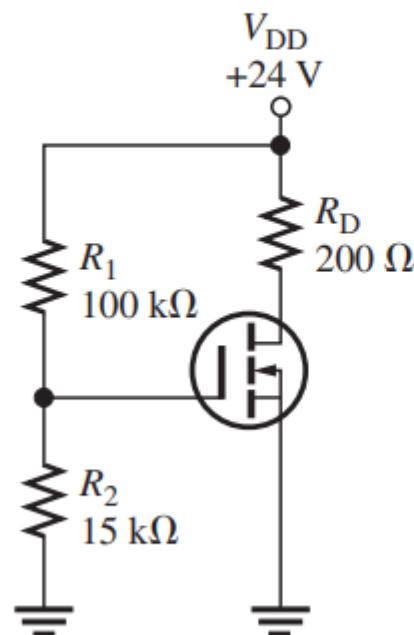
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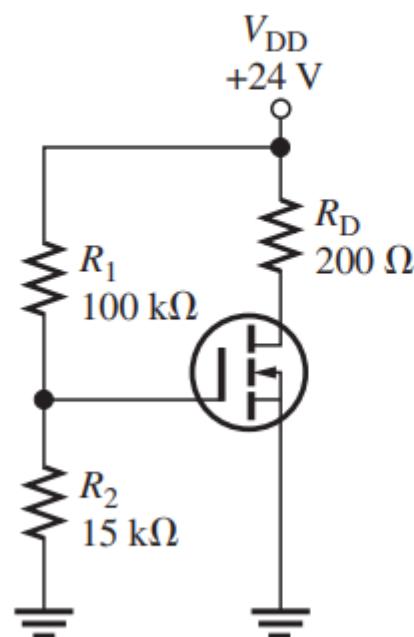
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Acknowledgment:-Thomas L. Floyd Electronic Devices, Electron Flow Version, Ninth Edition

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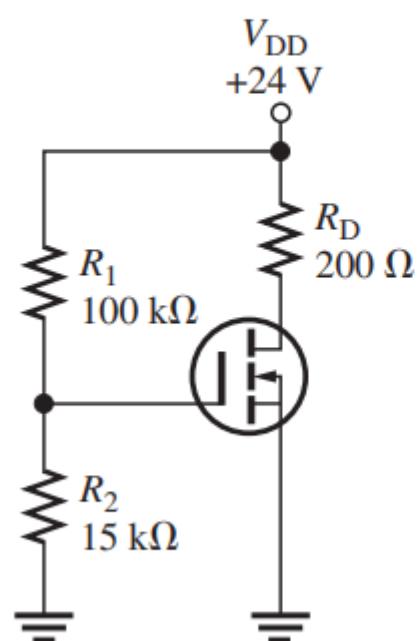
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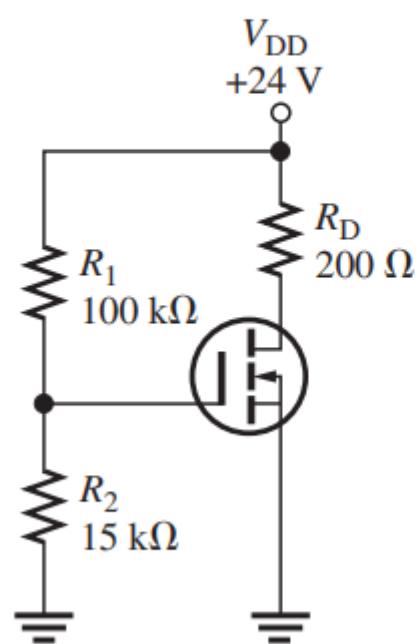
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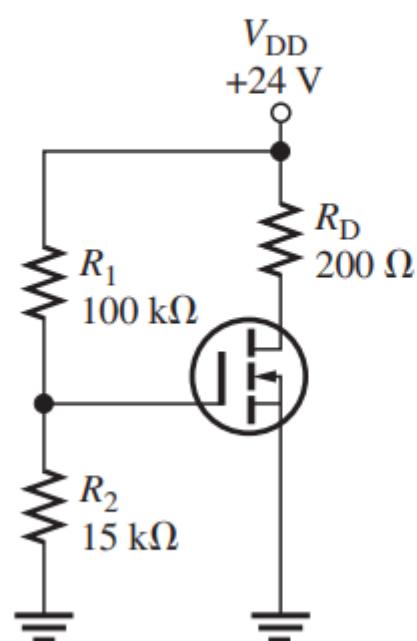
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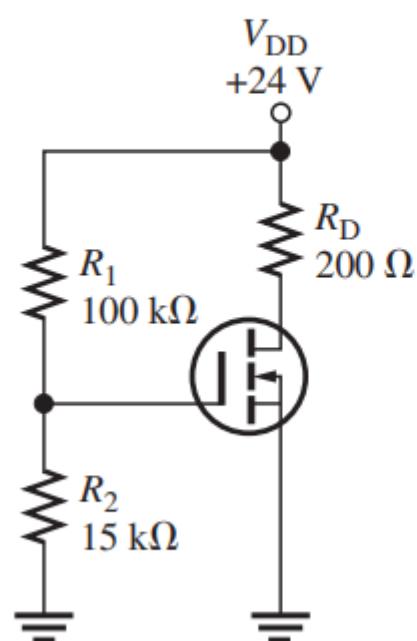
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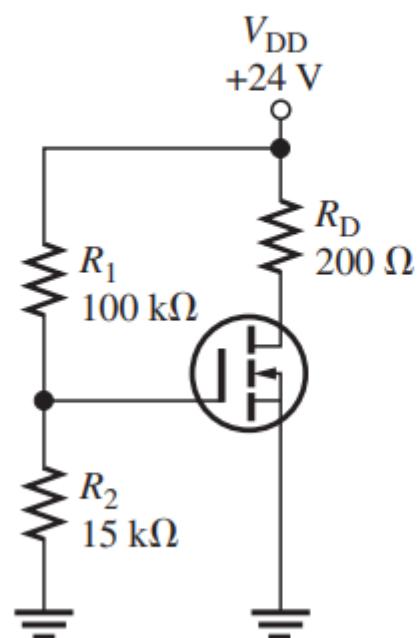
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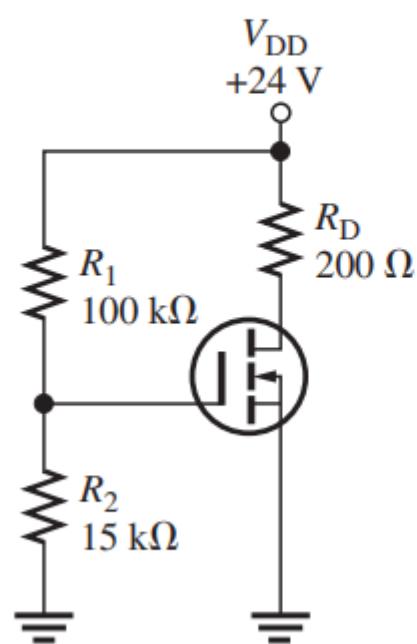
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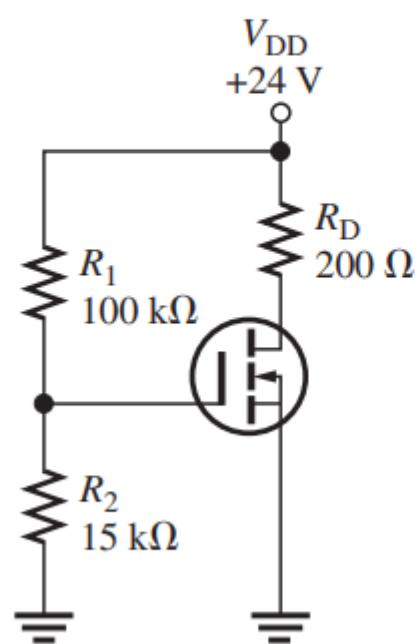
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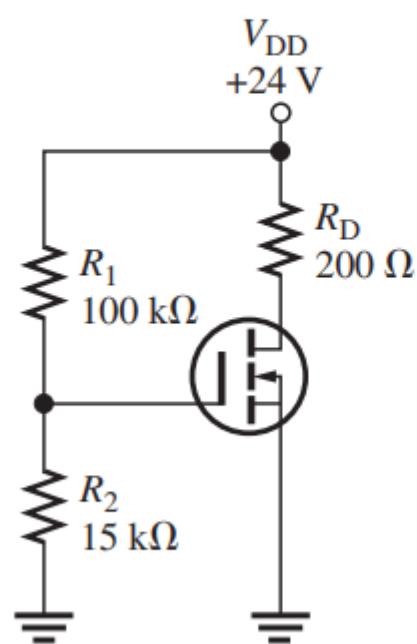
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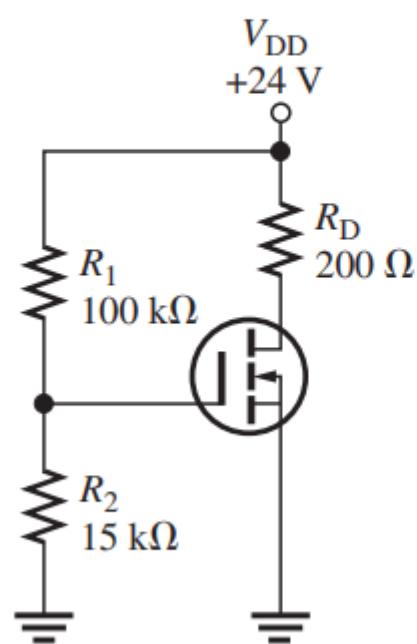
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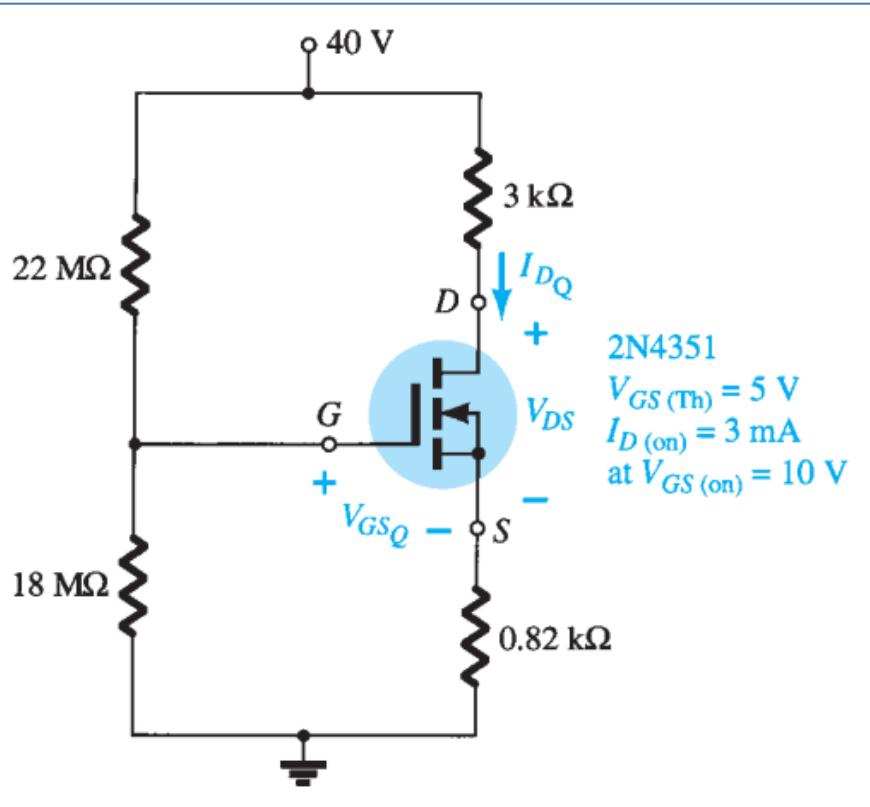
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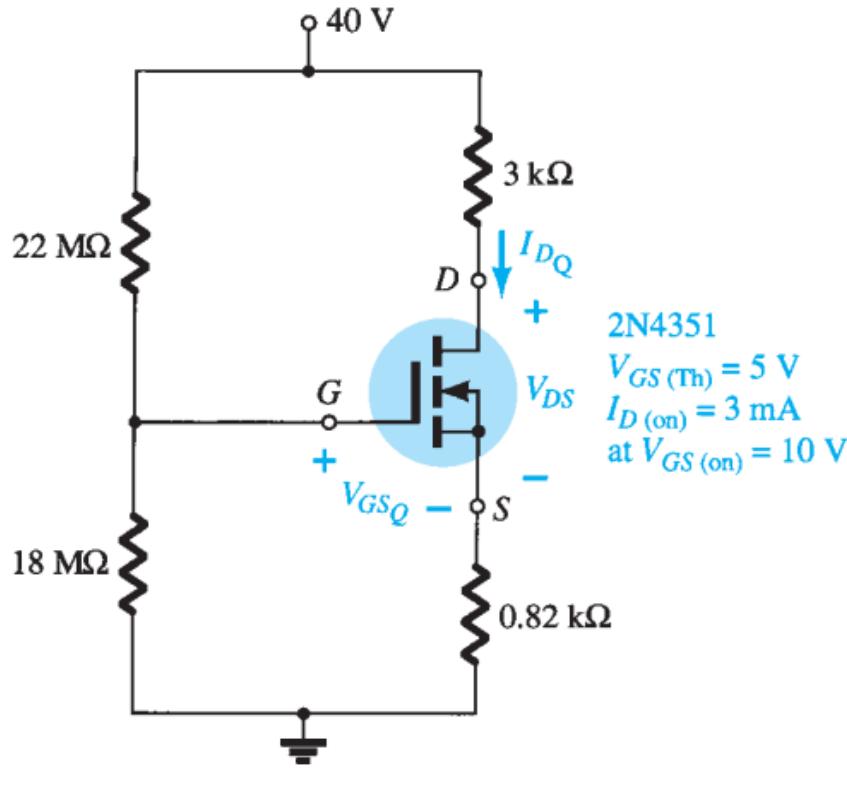
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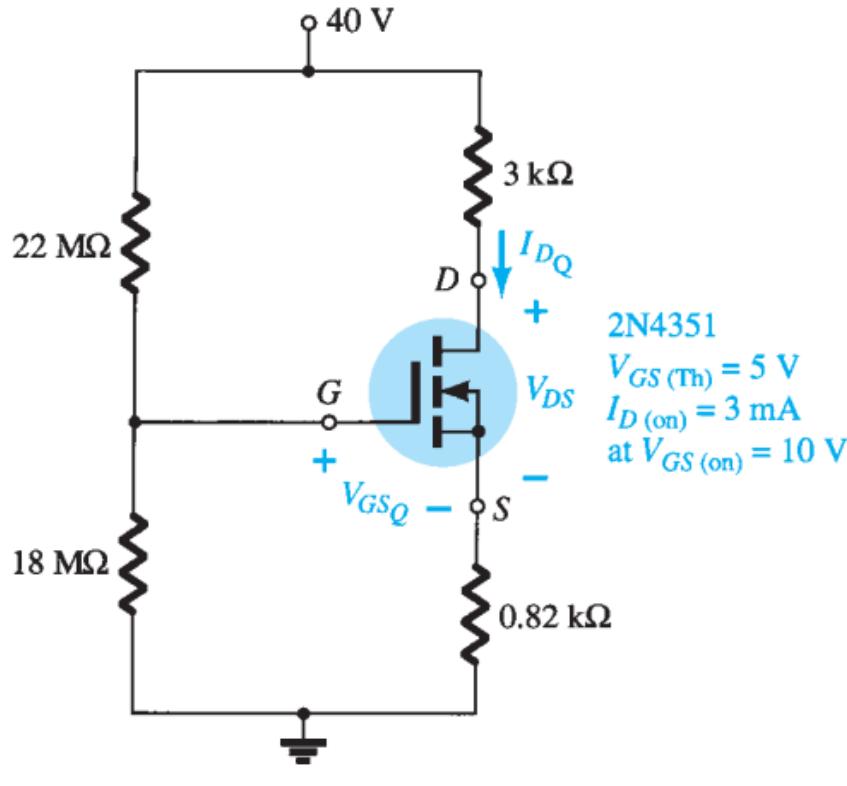
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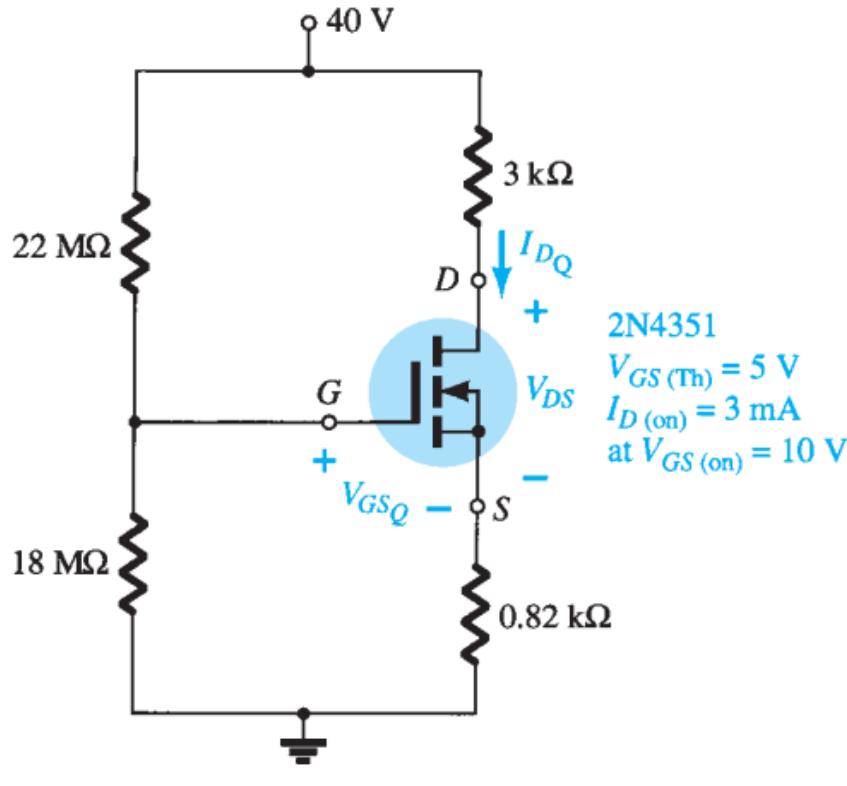
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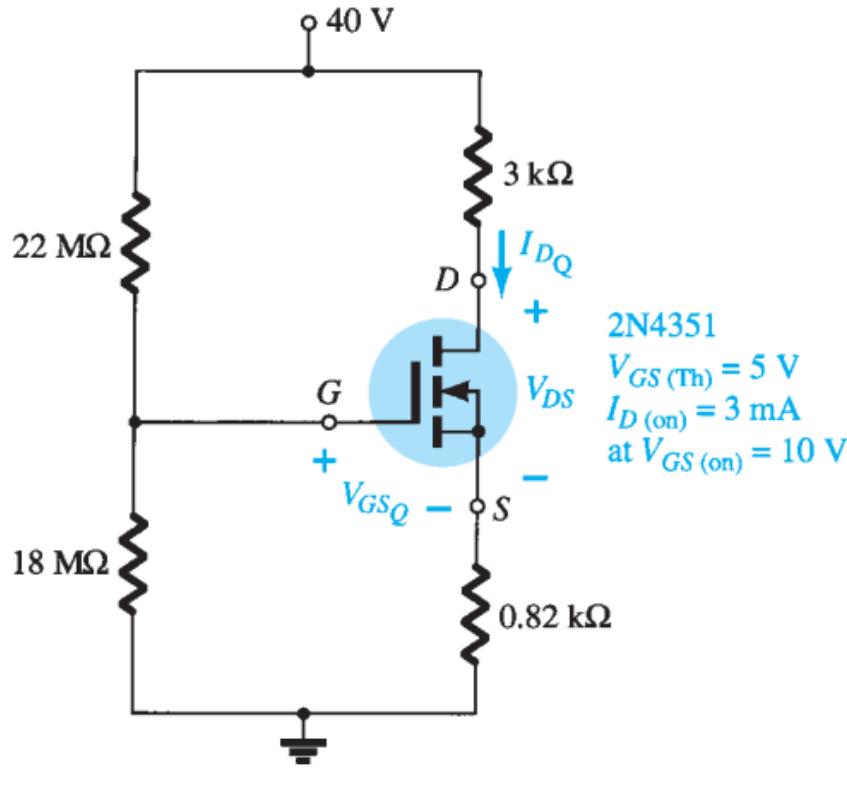
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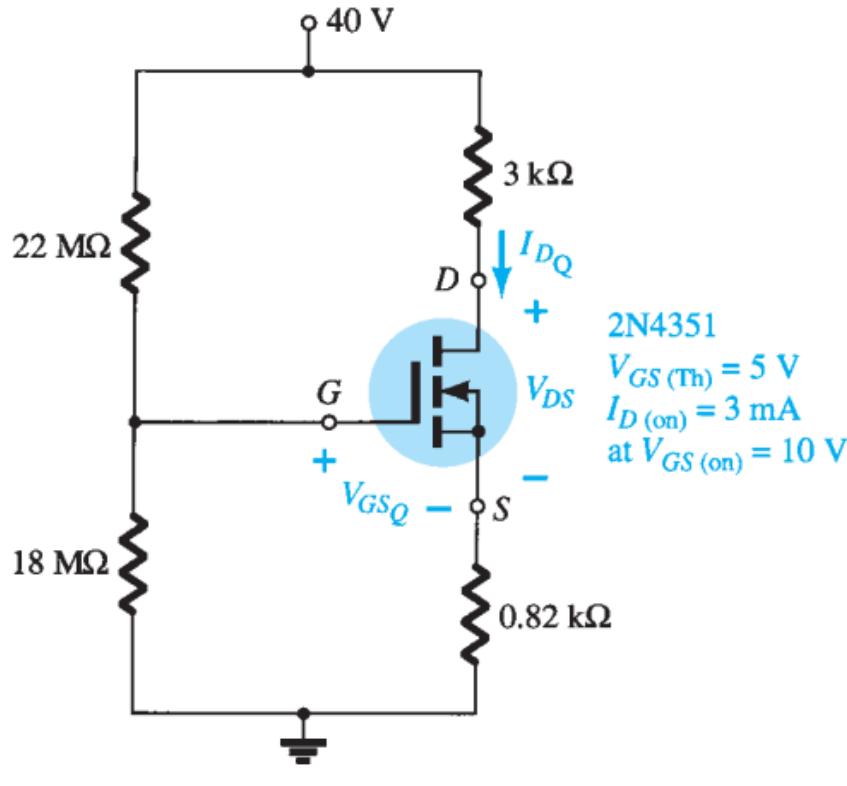
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$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18 \text{ M}\Omega)(40 \text{ V})}{22 \text{ M}\Omega + 18 \text{ M}\Omega} = 18 \text{ V}$$

$$V_{GS} = V_G - I_D R_S$$

# E- MOSFET biasing circuit

**EXAMPLE** Determine  $I_{DQ}$ ,  $V_{GSQ}$ , and  $V_{DS}$  for the network of Fig.



**Solution:**

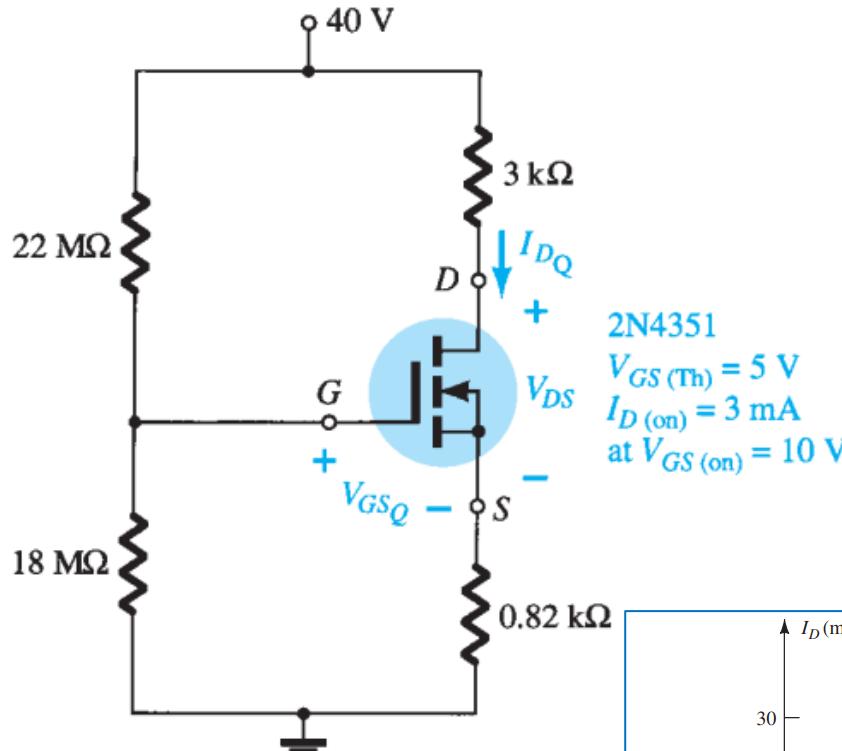
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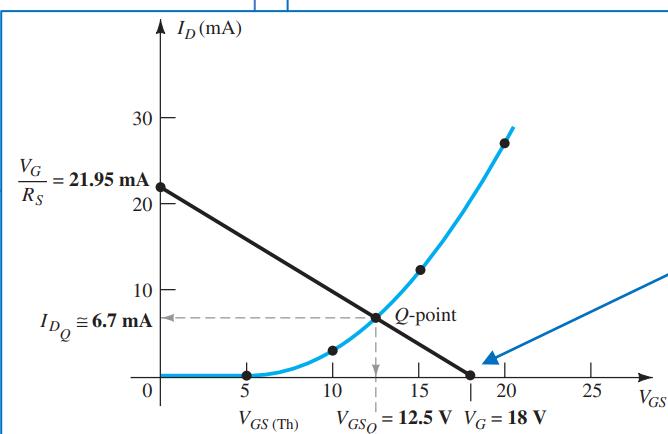
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When  $I_D = 0 \text{ mA}$ ,

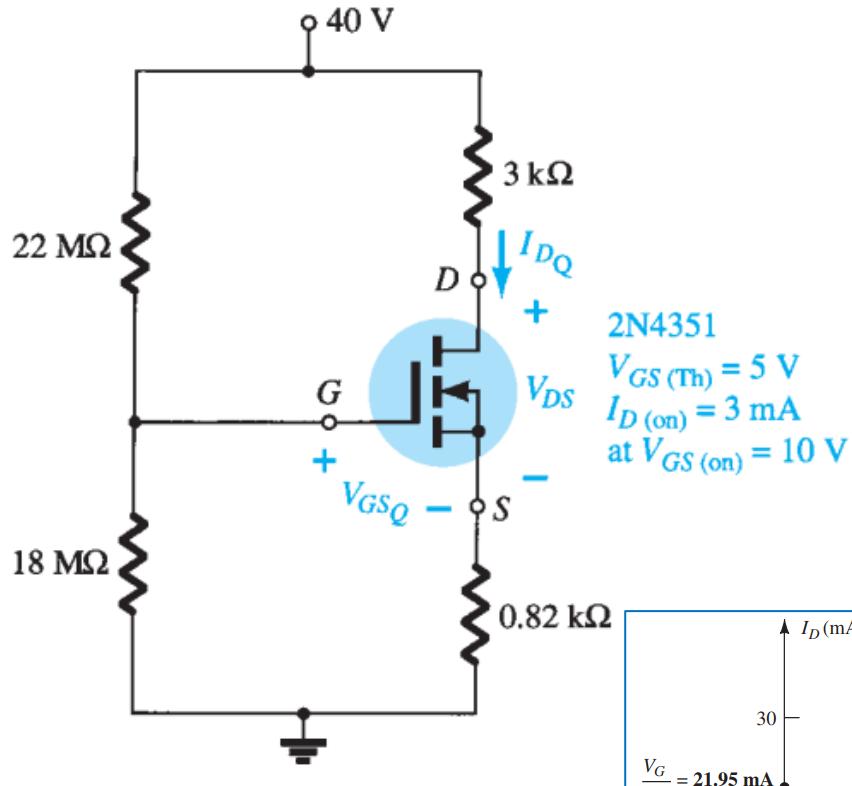
$$V_{GS} = 18 \text{ V} - (0 \text{ mA})(0.82 \text{ k}\Omega) = 18 \text{ V}$$



Acknowledgment:-Electronic Devices and Circuit Theory, Boylestad and Nashelsky, 11th Edition

# E- MOSFET biasing circuit

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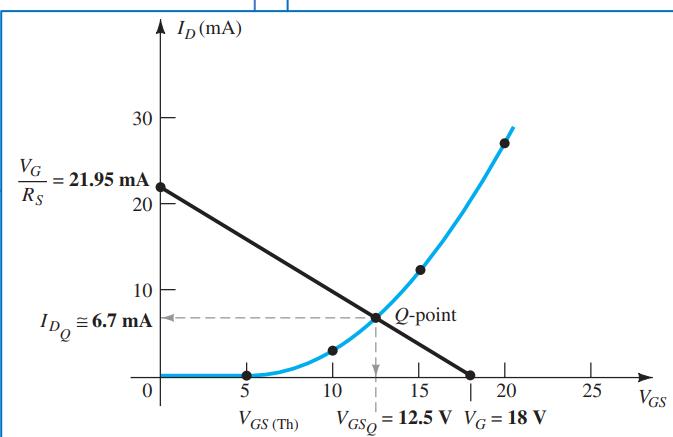
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as appearing on Fig.

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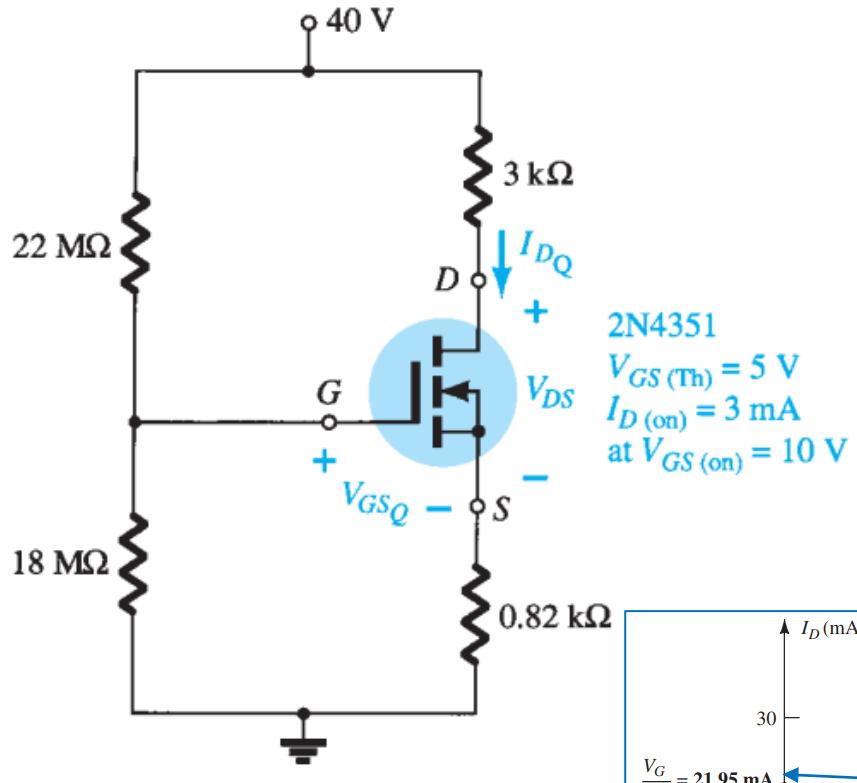
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# E- MOSFET biasing circuit

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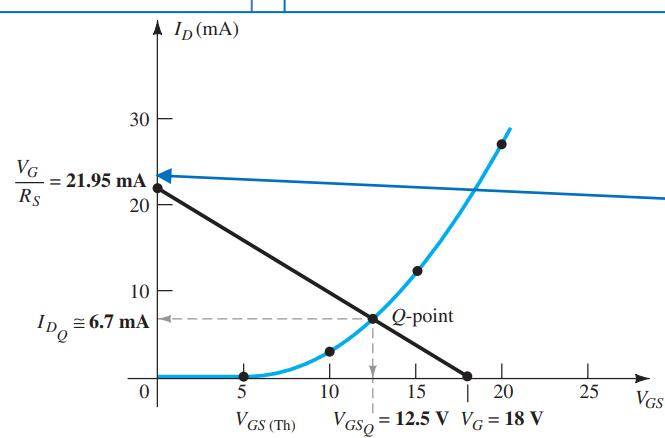
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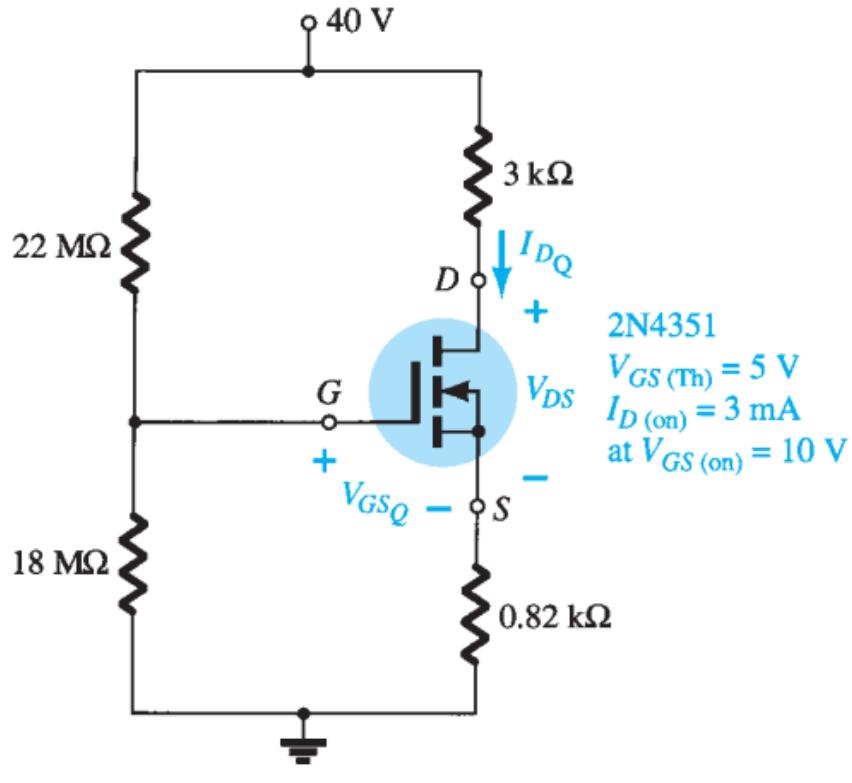
$$I_D = \frac{18 \text{ V}}{0.82 \text{ k}\Omega} = 21.95 \text{ mA}$$



Acknowledgment:-Electronic Devices and Circuit Theory, Boylestad and Nashelsky, 11th Edition

# E- MOSFET biasing circuit

**EXAMPLE** Determine  $I_{DQ}$ ,  $V_{GSQ}$ , and  $V_{DS}$  for the network of Fig.



**Solution:**

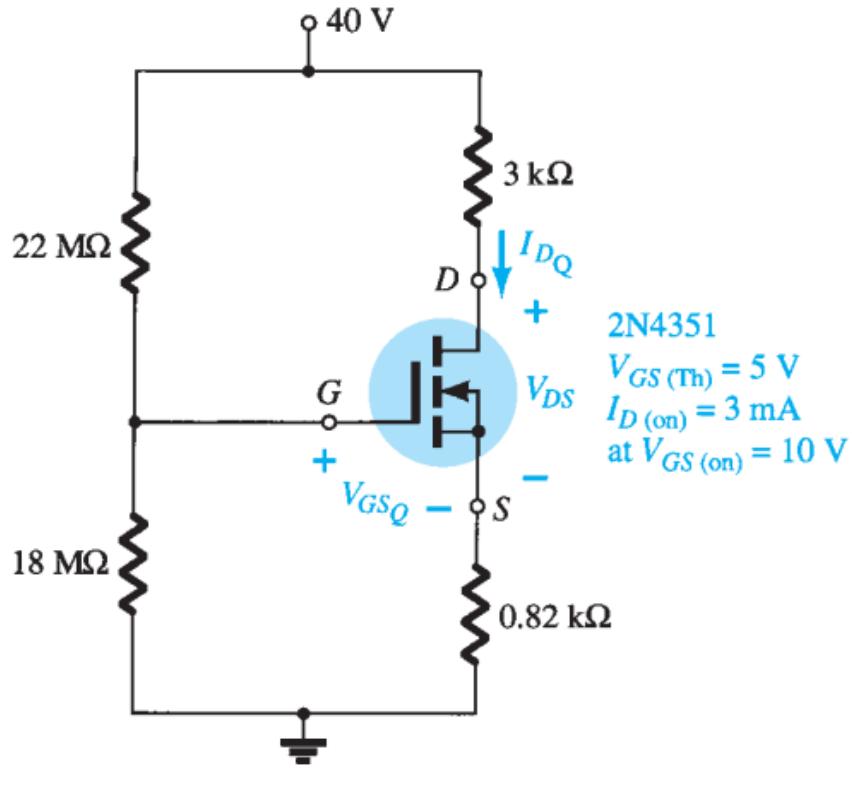
**Device**

$$V_{GS(\text{Th})} = 5 \text{ V}, \quad I_{D(\text{on})} = 3 \text{ mA} \text{ with } V_{GS(\text{on})} = 10 \text{ V}$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

# E- MOSFET biasing circuit

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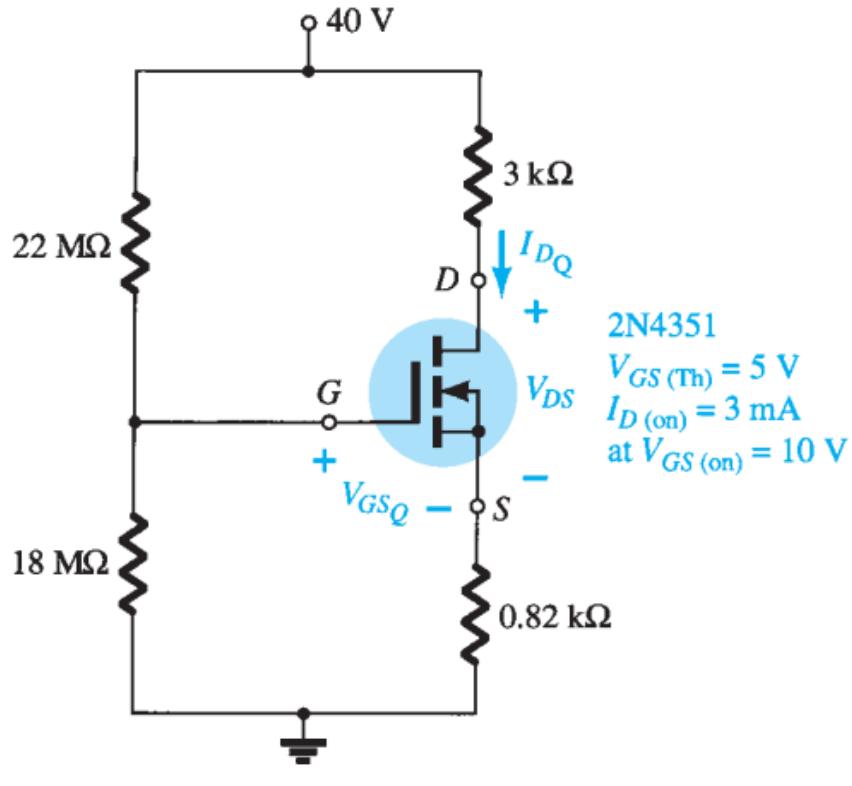
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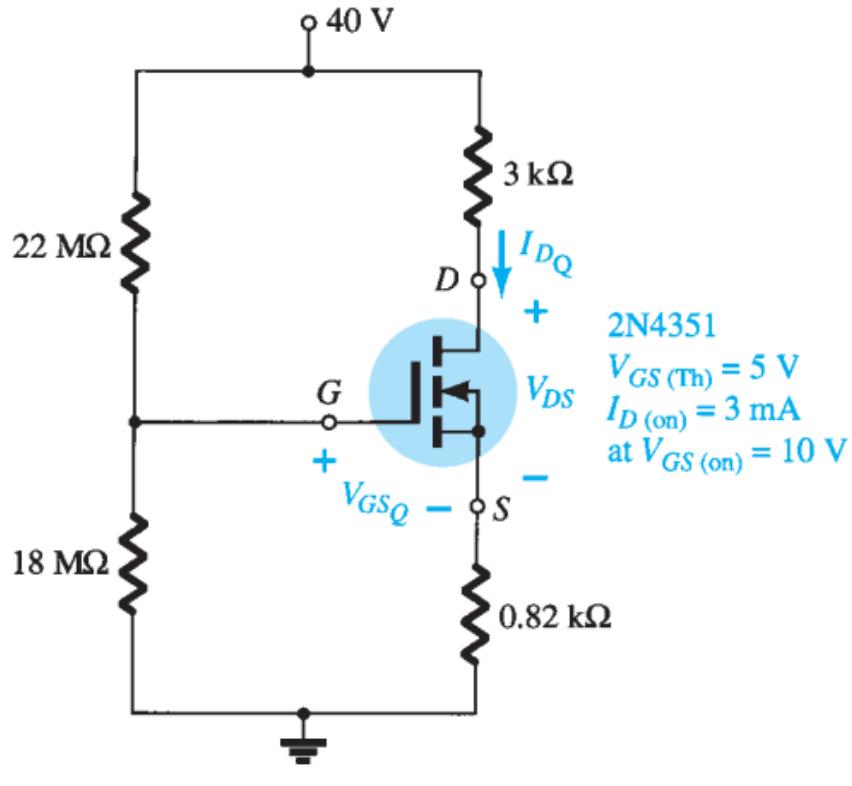
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$$\text{and} \quad I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

# E- MOSFET biasing circuit

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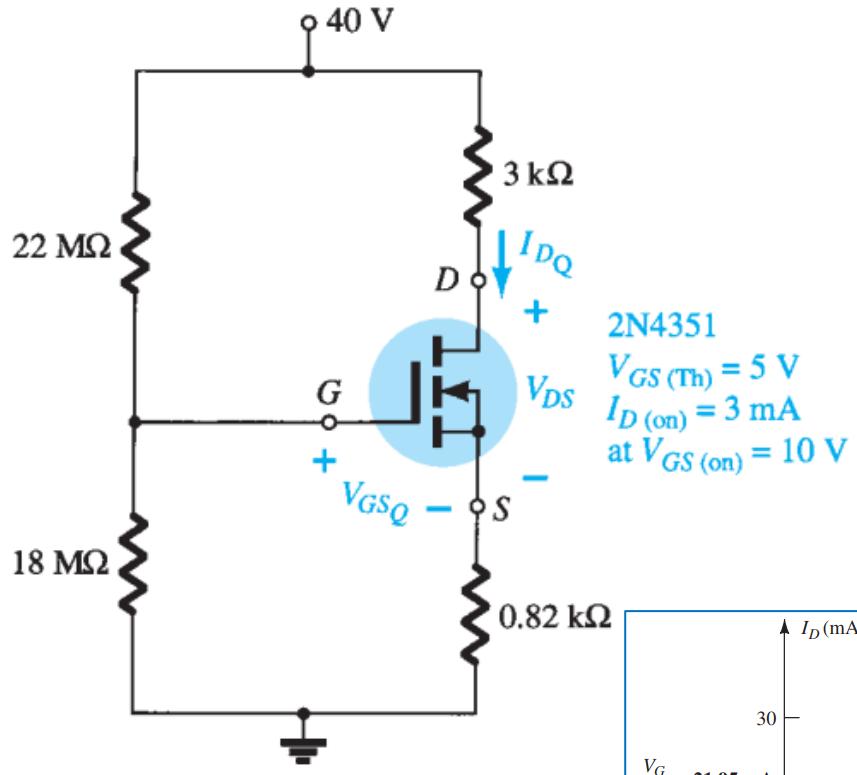
and

$$\begin{aligned} I_D &= k(V_{GS} - V_{GS(Th)})^2 \\ &= 0.12 \times 10^{-3}(V_{GS} - 5)^2 \end{aligned}$$

Acknowledgment:-Electronic Devices and Circuit Theory, Boylestad and Nashelsky, 11th Edition

# E- MOSFET biasing circuit

**EXAMPLE** Determine  $I_{DQ}$ ,  $V_{GSQ}$ , and  $V_{DS}$  for the network of Fig.



**Solution:**

**Device**

which is plotted on the same graph. From Fig.

$$I_{DQ} \approx 6.7 \text{ mA}$$

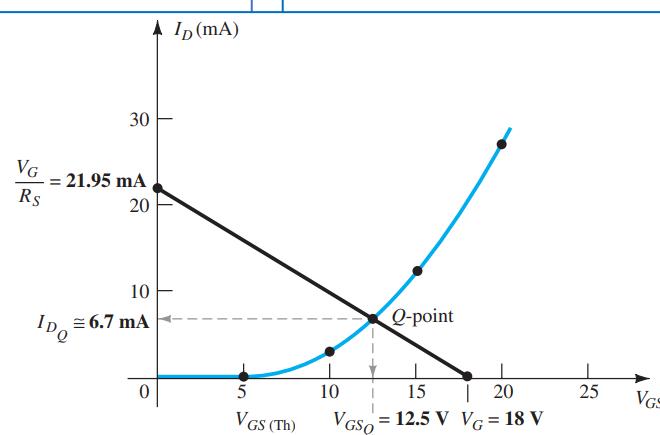
$$V_{GSQ} = 12.5 \text{ V}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40 \text{ V} - (6.7 \text{ mA})(0.82 \text{ k}\Omega + 3.0 \text{ k}\Omega)$$

$$= 40 \text{ V} - 25.6 \text{ V}$$

$$= 14.4 \text{ V}$$



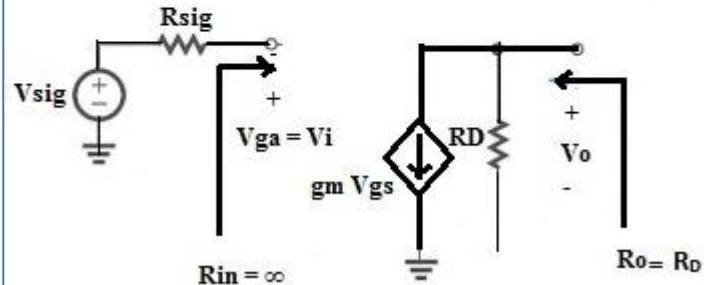
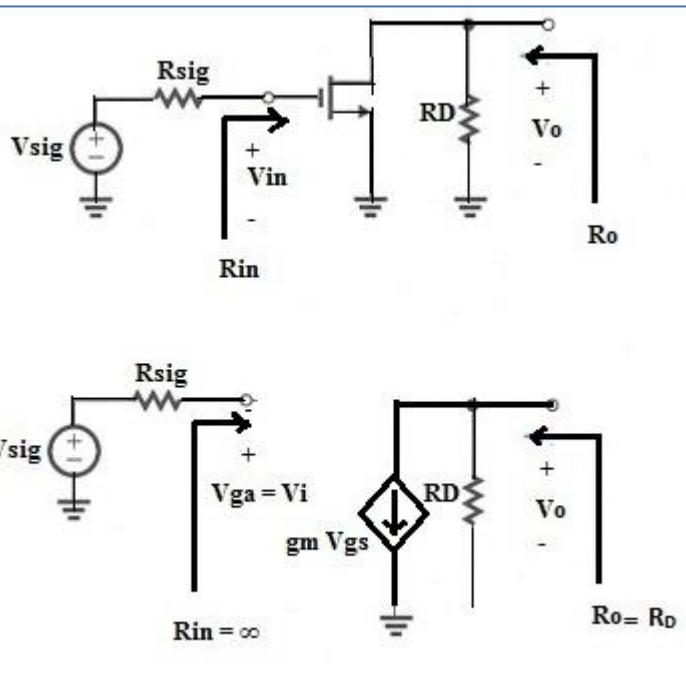
Acknowledgment:-Electronic Devices and Circuit Theory, Boylestad and Nashelsky, 11th Edition

# MOSFET amplifier configurations

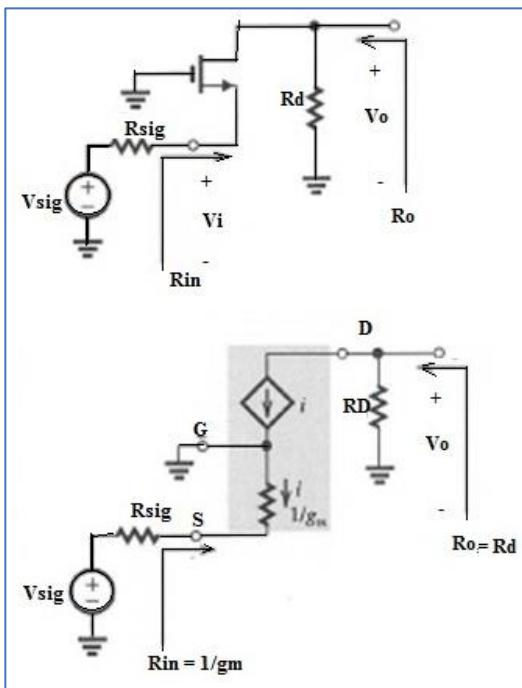
## Types of MOSFET Amplifiers

MOSFET amplifiers are available in three types like:

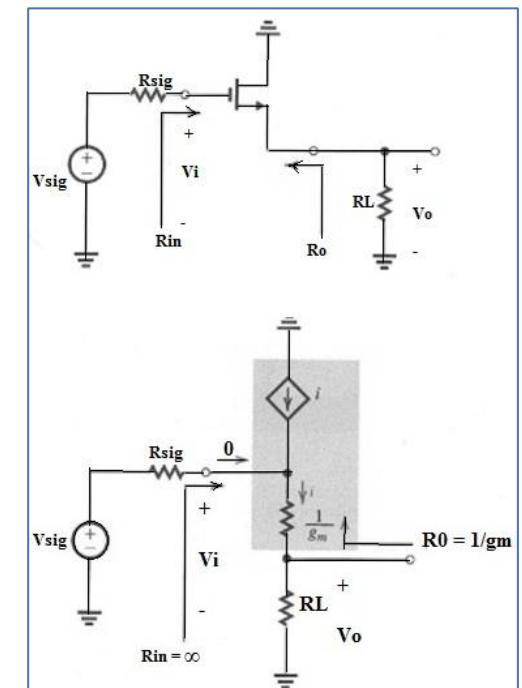
- Common Source (CS),
- Common Gate (CG), and
- Common Drain (CD),



Common Source (CS) Amplifier

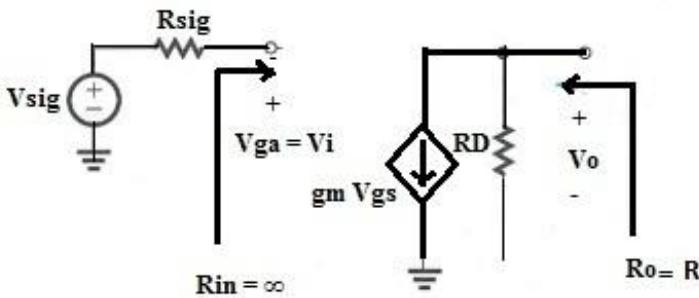
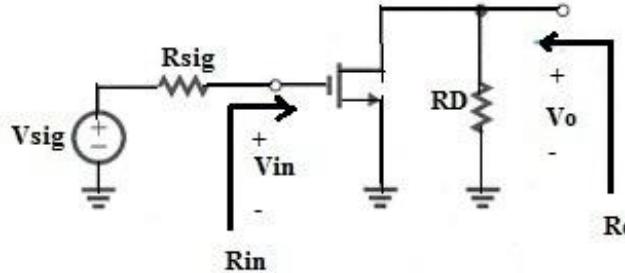


Common Gate (CG) Amplifier



Common Drain (CD) Amplifier

# Common Source MOSFET Amplifier



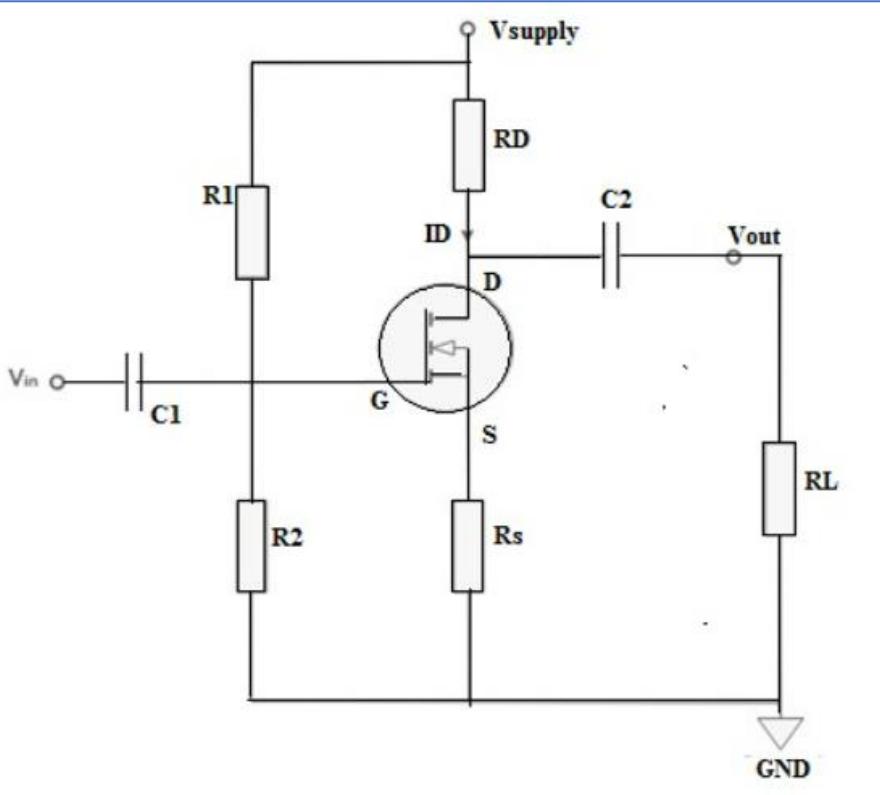
- Common source amplifier can be defined as when the i/p signal is given at both the terminals of the gate (G) & source (S), the o/p voltage can be amplified & attained across the resistor at the load within the drain (D) terminal.
- In this configuration, the source terminal acts as a common terminal in between the i/p and o/p.
- The common-source MOSFET amplifier is related to the CE (common-emitter) amplifier of BJT.
- This is very popular due to high gain and larger signal amplification can be achieved.
- The small-signal and hybrid  $\pi$  model of a common source MOSFET amplifier is shown figure.

- The CS MOSFET amplifiers have infinite i/p impedance, high o/p resistance & high voltage gain.
- The output resistance can be reduced by decreasing the RD but also the voltage gain can also be decreased.
- A CS MOSFET amplifier suffers from a poor high-frequency performance like most of the transistor amplifiers do.

# A common-source n-channel E-MOSFET amplifier

## MOSFET Amplifier Working

A complete MOSFET amplifier circuit can be designed by including a source, drain, load resistor & coupling capacities to the above circuit. The biasing circuit of the MOSFET amplifier is shown below.



- The biasing circuit includes a voltage divider, and the main function of this is to bias a transistor in one way.
  - So, this is the most frequently used biasing method in transistors.
  - It uses two resistors to confirm that voltage is separated and & distributed into the MOSFET at the right levels.
  - It is realized through two  $R_1$  &  $R_2$  parallel resistors.
  - The  $C_1$  &  $C_2$  coupling capacitors in the circuit protect the biasing DC voltage from the AC signal to be amplified.
  - At last, the output is given to a load, formed by the  $RL$  resistor.
- The bias or gate voltage can be given by

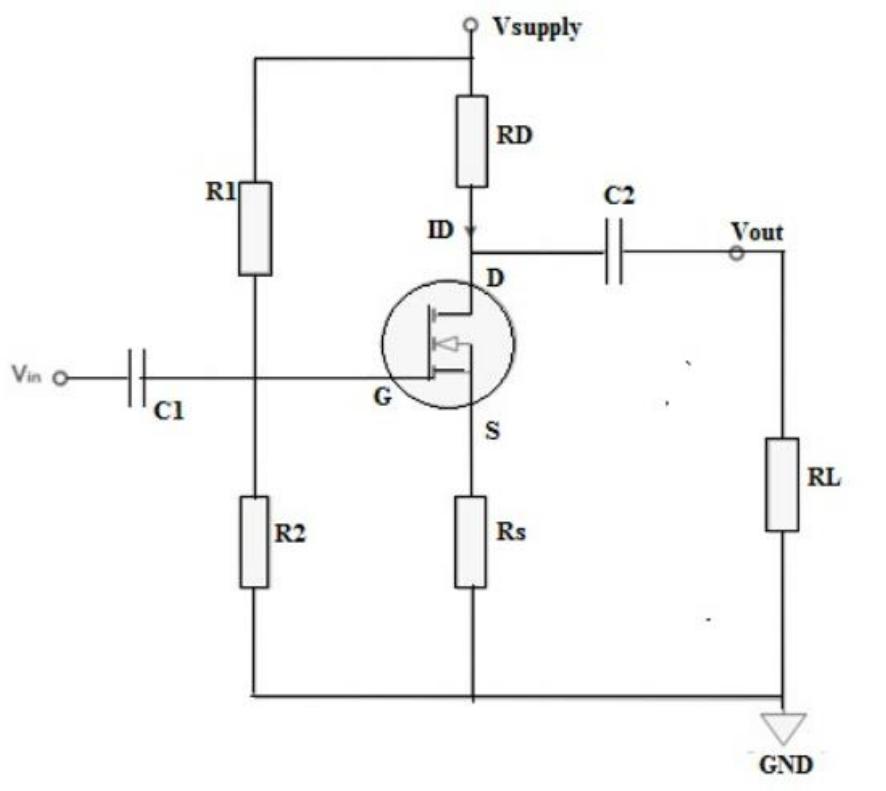
$$V_G = V_{\text{supply}} \times \left( \frac{R_2}{R_1 + R_2} \right)$$

Here, the  $R_1$  &  $R_2$  values are usually large to enhance the amplifier's input impedance & also to reduce the ohmic power losses.

# A common-source n-channel E-MOSFET amplifier

## MOSFET Amplifier Working : Input & Output Voltages (Vin & Vout)

- To make it simpler, we need to consider that there is no load is connected with the drain branch in parallel.
- The input voltage ( $V_{in}$ ) can be given through the gate (G) to source (S) voltage like  $V_{GS}$ .
- The voltage drop across the  $R_S$  resistor can be given by  $R_S \times I_D$ .



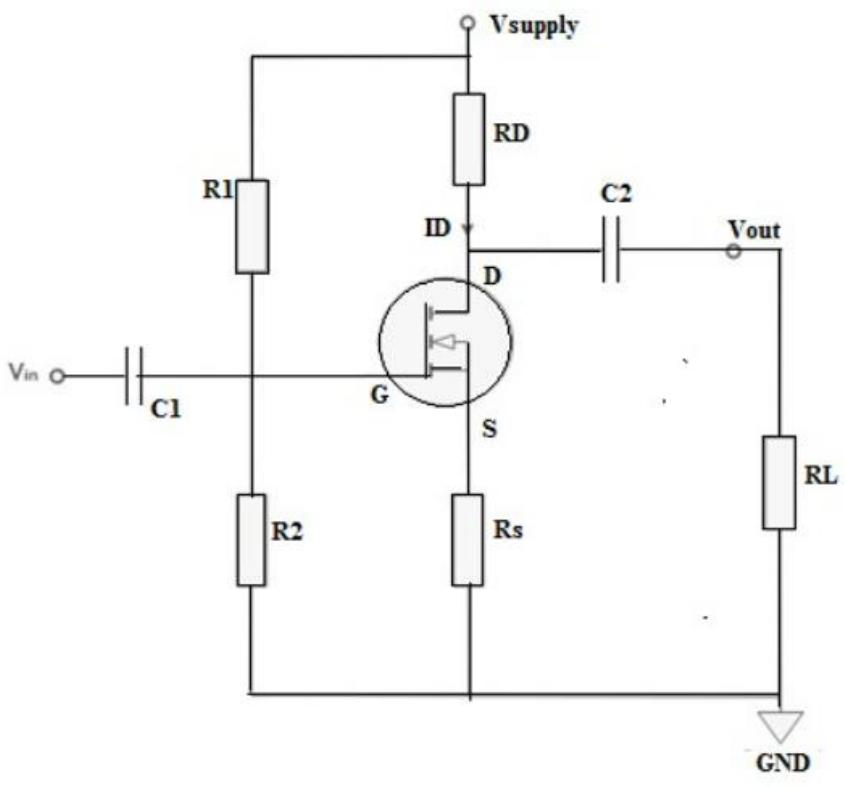
According to the transconductance ( $gm$ ) definition, the ratio of  $I_D$  (drain current) to  $V_{GS}$  (gate-source voltage) once a constant drain-source voltage is applied.

$$gm = I_D / V_{GS}$$

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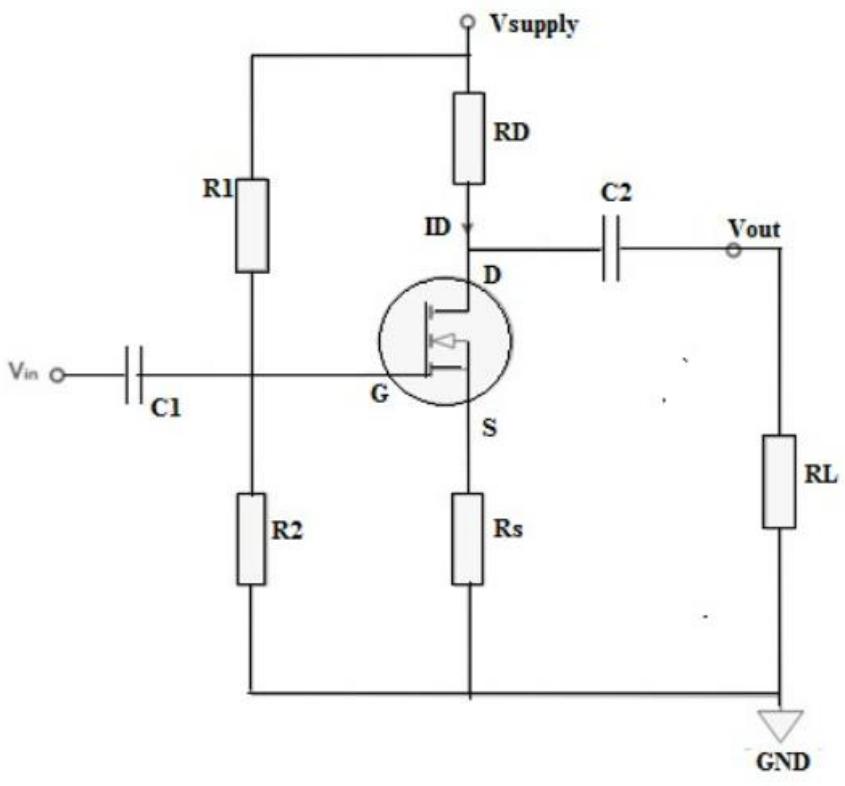
So,  $I_D = gm \times V_{GS}$  & the input voltage ( $V_{in}$ ) can be factored by  $V_{GS}$  like the following.

$$V_{in} = V_{GS} \times (1 + gmR_s)$$

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## MOSFET Amplifier Working : Input & Output Voltages (Vin & Vout)

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- The input voltage ( $V_{in}$ ) can be given through the gate (G) to source (S) voltage like  $V_{GS}$ .
- The voltage drop across the RS resistor can be given by  $R_s \times I_D$ .



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So,  $I_D = gm \times V_{GS}$  & the input voltage ( $V_{in}$ ) can be factored by  $V_{GS}$  like the following.

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The o/p voltage ( $V_{out}$ ) is simply given through the voltage drop across the drain resistor ( $RD$ )

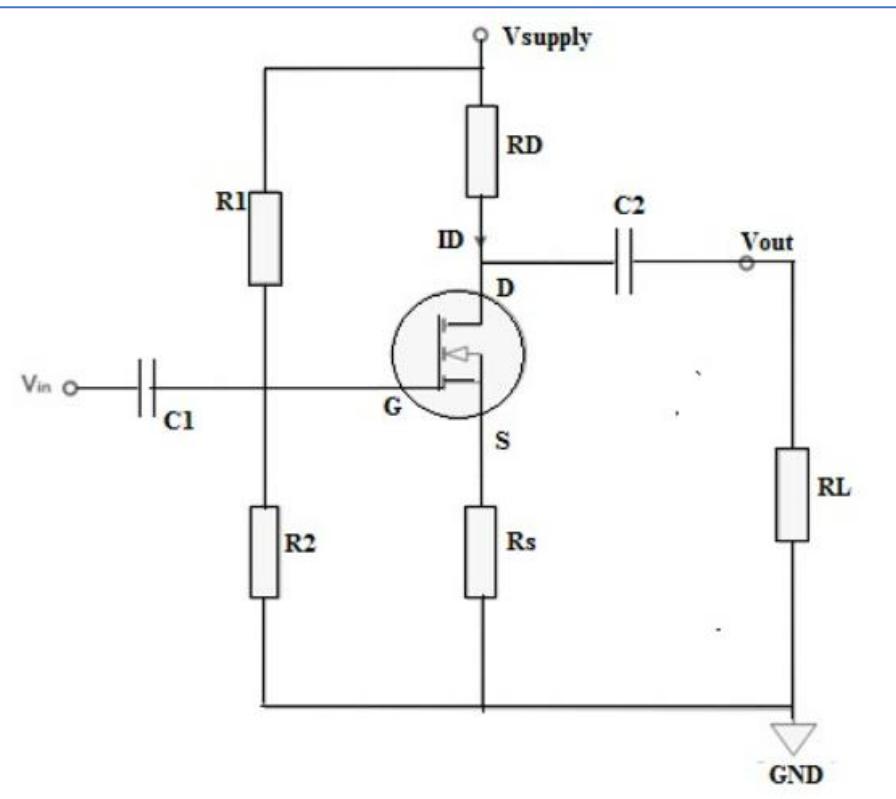
$$V_{out} = - R_D \times I_D = - gm V_{GS} R_D$$

# A common-source n-channel E-MOSFET amplifier

## MOSFET Amplifier Working : Voltage Gain

The voltage gain ( $A_V$ ) is the ratio of input voltage and output voltage. After that simplification, the equation will become

$$A_V = - R_D / R_s = 1/g_m$$

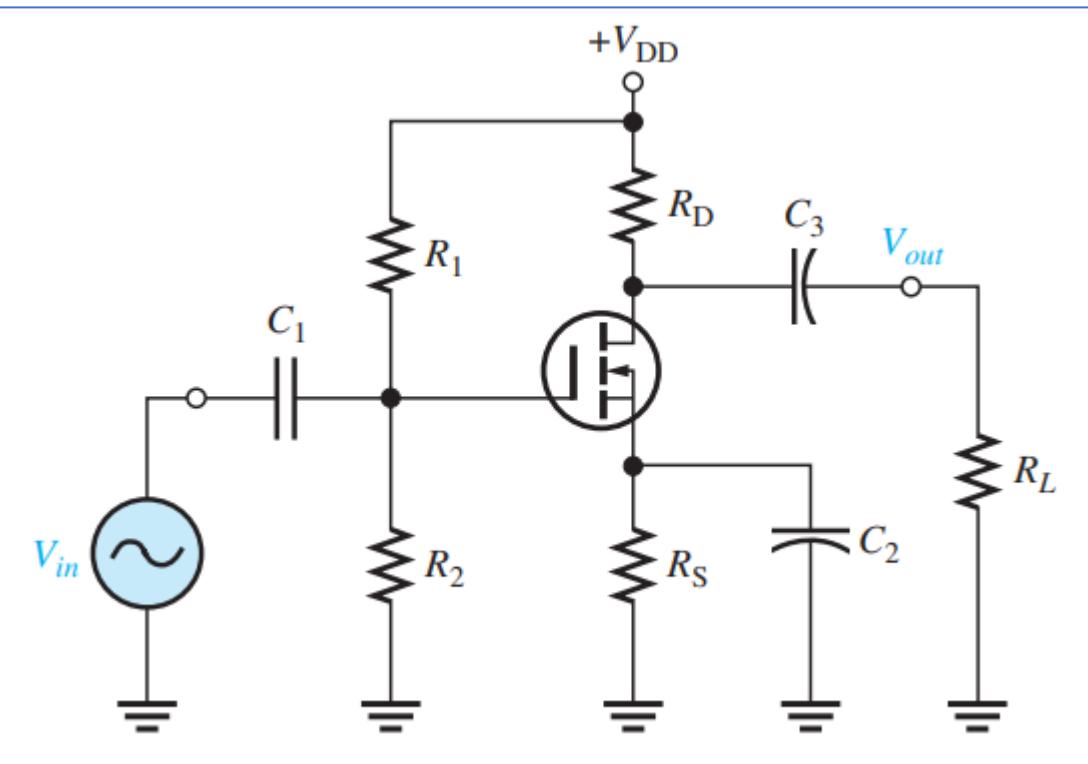


In the above equation, sign “-” comes from the fact that the MOSFET amplifier inverts the o/p signal in equivalence with the BJT CE Amplifier. So, the phase shift is  $180^\circ$  or  $\pi$  rad.

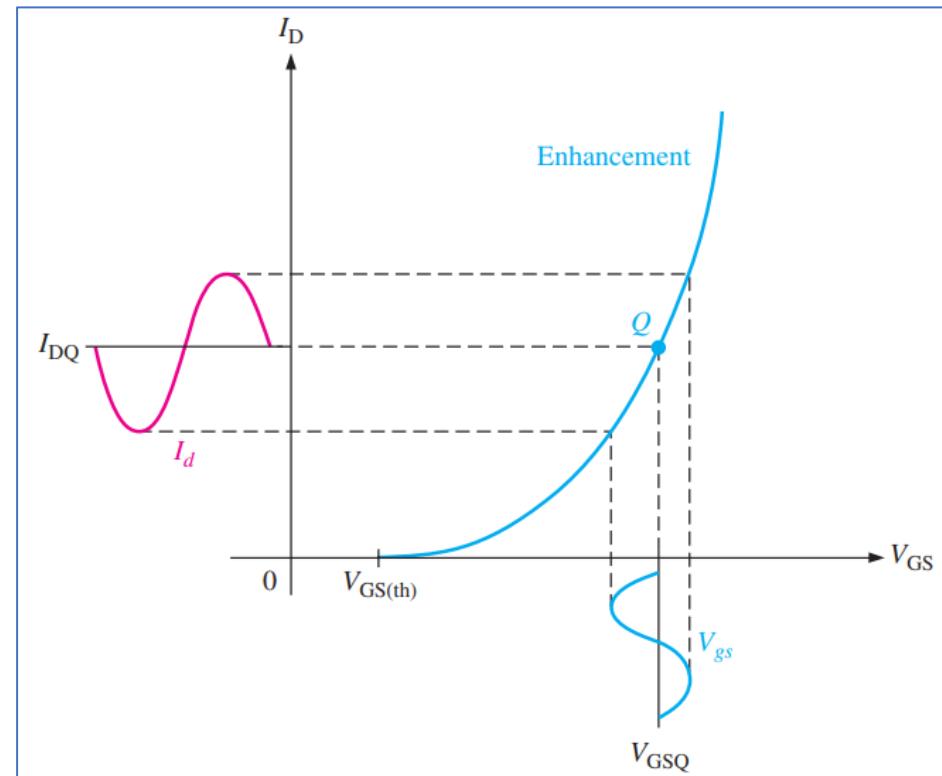
# A common-source n-channel E-MOSFET amplifier

- A common-source n-channel E-MOSFET with voltage-divider bias with an ac source capacitively coupled to the gate is shown in Figure.
- The gate is biased with a positive voltage such that  $V_{GS} > V_{GS(th)}$

- As with the JFET and D-MOSFET, the signal voltage produces a swing in  $V_{gs}$  above and below its Q-point value,  $V_{GSQ}$ .
- This, in turn, causes a swing in  $I_d$  above and below its Q-point value,  $I_{DQ}$ , as illustrated in Figure .
- Operation is entirely in the enhancement mode



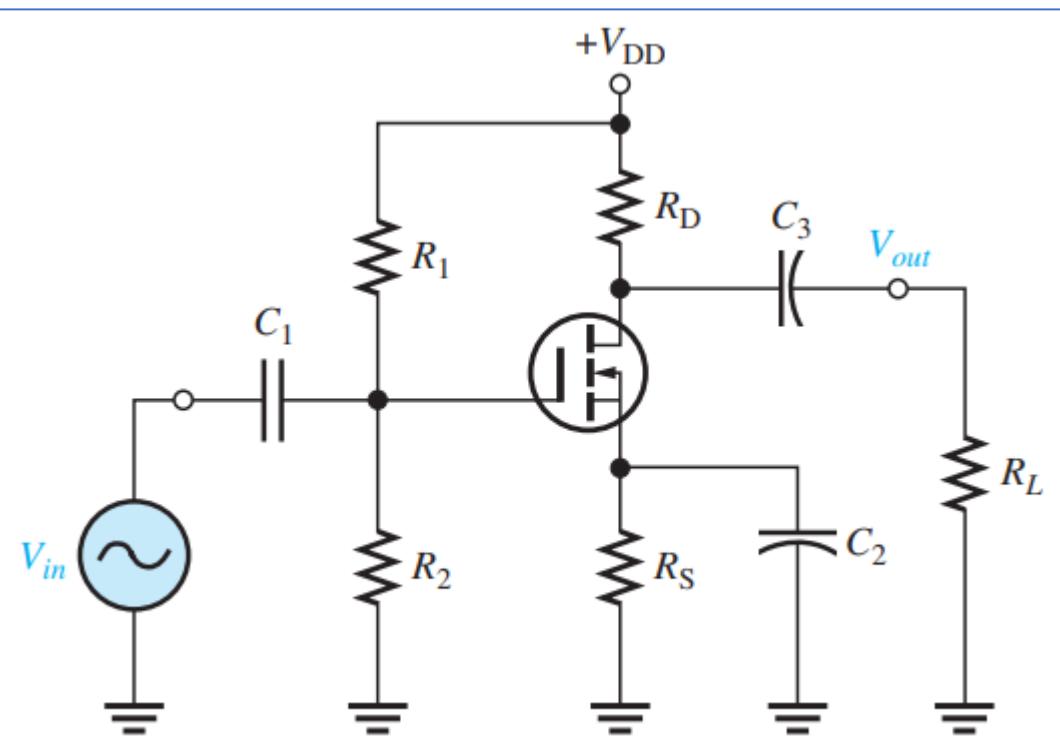
Common-source E-MOSFET amplifier with voltage-divider bias



E-MOSFET (n-channel) operation shown on transfer characteristic curve.

# A common-source n-channel E-MOSFET amplifier

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Common-source E-MOSFET amplifier with voltage-divider bias

- The circuit in Figure uses voltage-divider bias to achieve a  $V_{GS}$  above threshold.
- The general dc analysis proceeds as follows using the E-MOSFET characteristic equation to solve for  $I_D$ .

$$V_{GS} = \left( \frac{R_2}{R_1 + R_2} \right) V_{DD}$$

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

$$V_{DS} = V_{DD} - I_D R_D$$

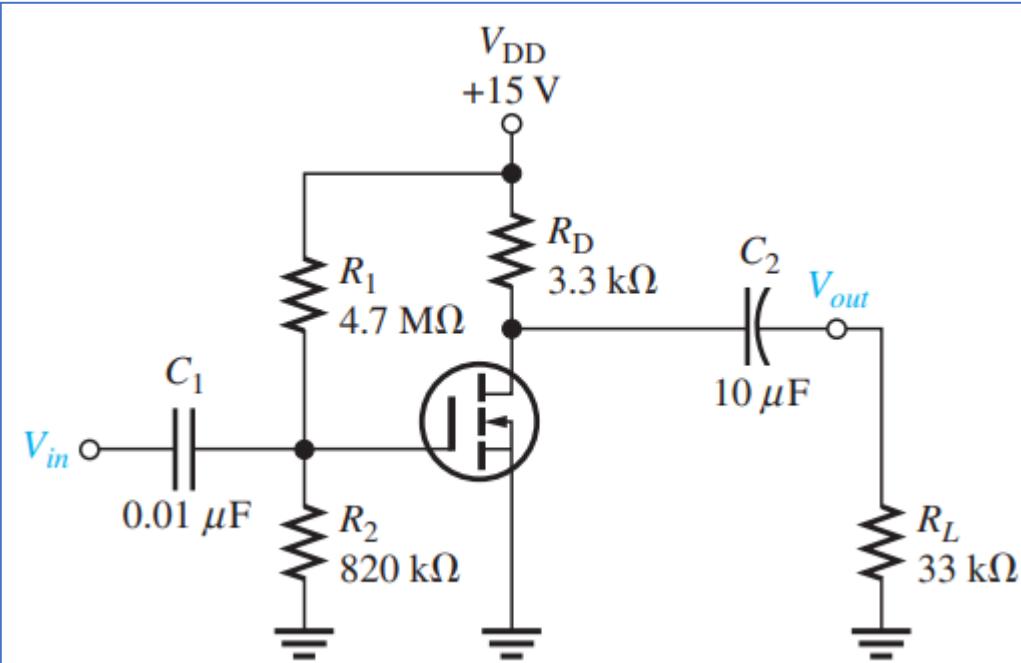
The voltage gain expression is the same as for the JFET and D-MOSFET circuits. The ac input resistance is

$$R_{in} = R_1 \parallel R_2 \parallel R_{IN(gate)}$$

where  $R_{IN(gate)} = V_{GS}/I_{GSS}$ .

# A common-source n-channel E-MOSFET amplifier

**EXAMPLE** A common-source amplifier using an E-MOSFET is shown in Figure . Find  $V_{GS}$ ,  $I_D$ ,  $V_{DS}$ , and the ac output voltage. Assume that for this particular device,  $I_{D(on)} = 200 \text{ mA}$  at  $V_{GS} = 4 \text{ V}$ ,  $V_{GS(th)} = 2 \text{ V}$ , and  $g_m = 23 \text{ mS}$ .  $V_{in} = 25 \text{ mV}$ .



$$V_{GS} = \left( \frac{R_2}{R_1 + R_2} \right) V_{DD}$$

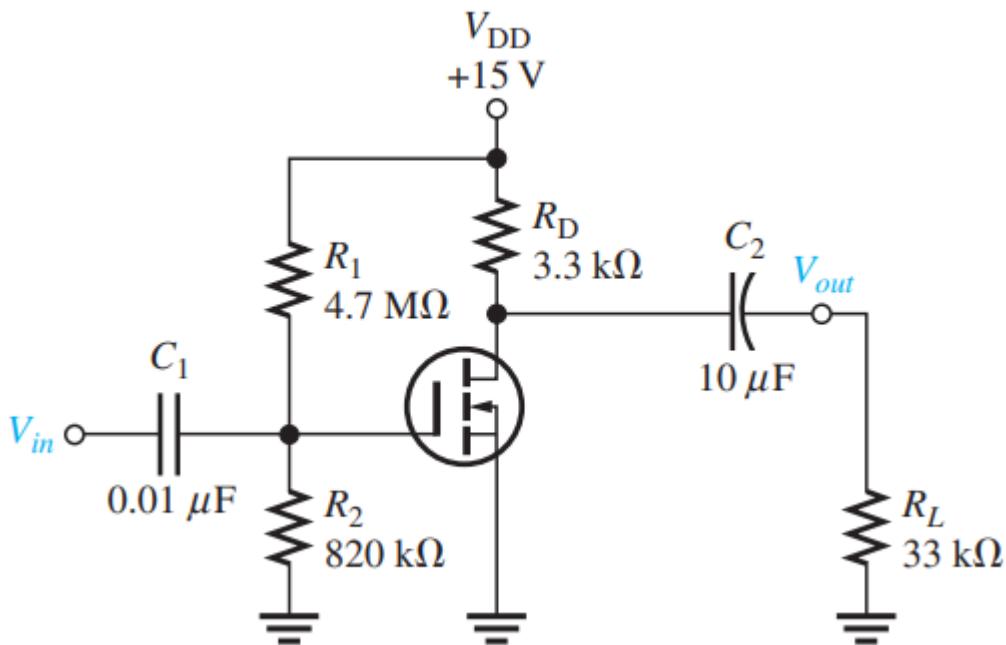
$$I_D = K(V_{GS} - V_{GS(th)})^2$$

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*Acknowledgment:-Thomas L. Floyd Electronic Devices, Electron Flow Version, Ninth Edition*

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**Solution**  $V_{GS} = \left( \frac{R_2}{R_1 + R_2} \right) V_{DD}$

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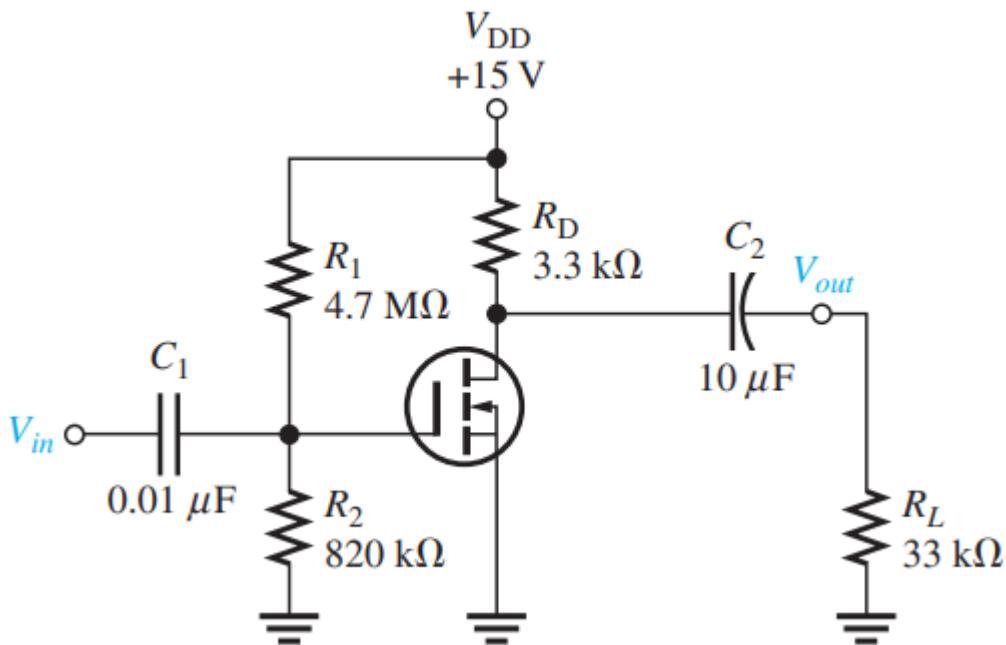
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$$I_D = K(V_{GS} - V_{GS(th)})^2$$

$$V_{DS} = V_{DD} - I_D R_D$$

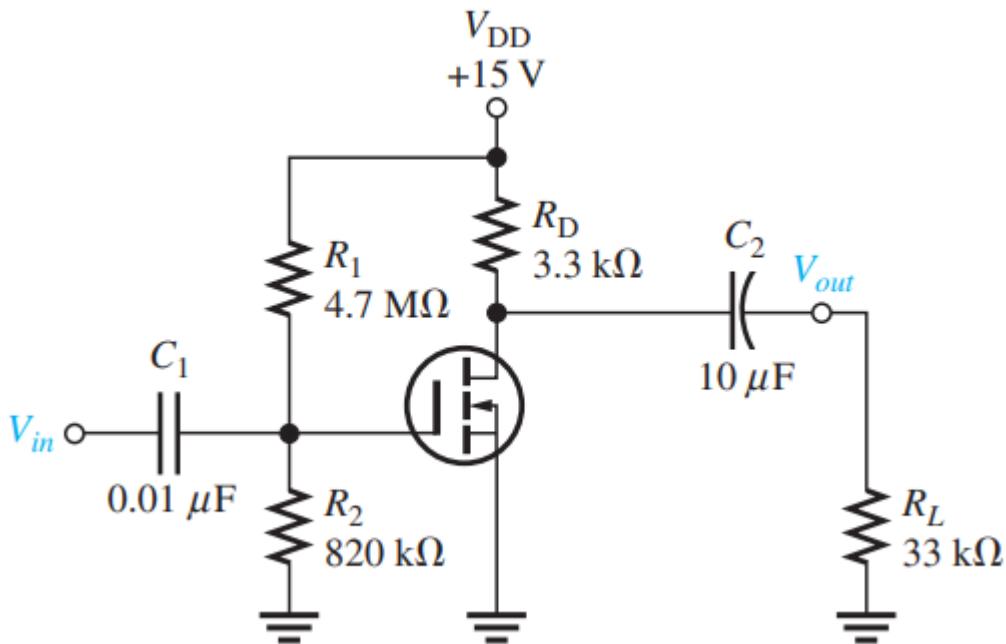
**Solution**  $V_{GS} = \left( \frac{R_2}{R_1 + R_2} \right) V_{DD} = \left( \frac{820 \text{ k}\Omega}{5.52 \text{ M}\Omega} \right) 15 \text{ V} = 2.23 \text{ V}$

For  $V_{GS} = 4 \text{ V}$ ,

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2}$$

# A common-source n-channel E-MOSFET amplifier

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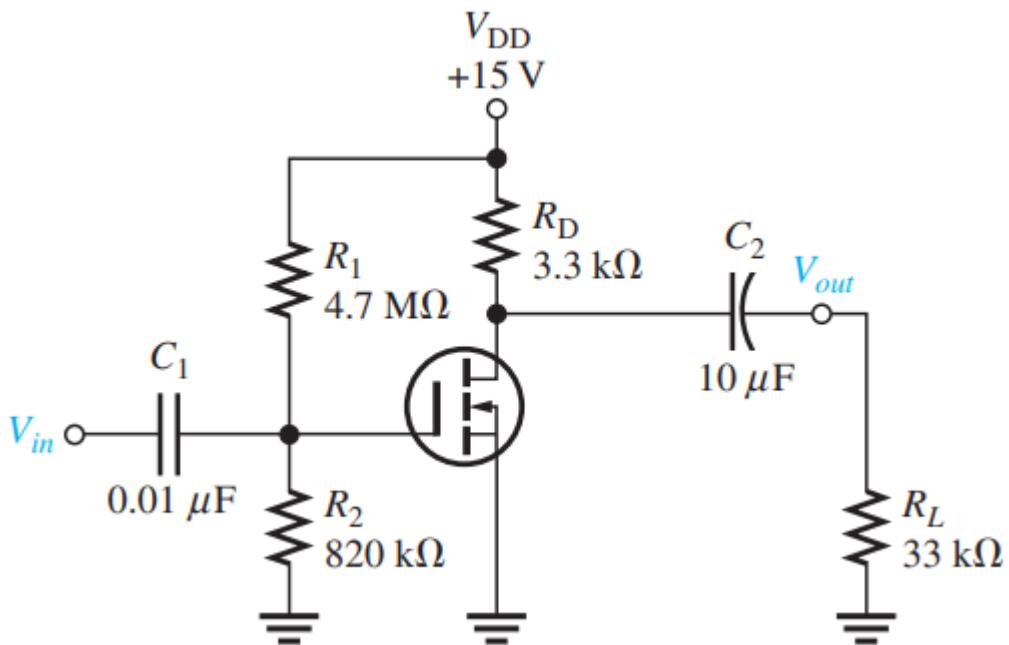
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$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{200 \text{ mA}}{(4 \text{ V} - 2 \text{ V})^2} = 50 \text{ mA/V}^2$$

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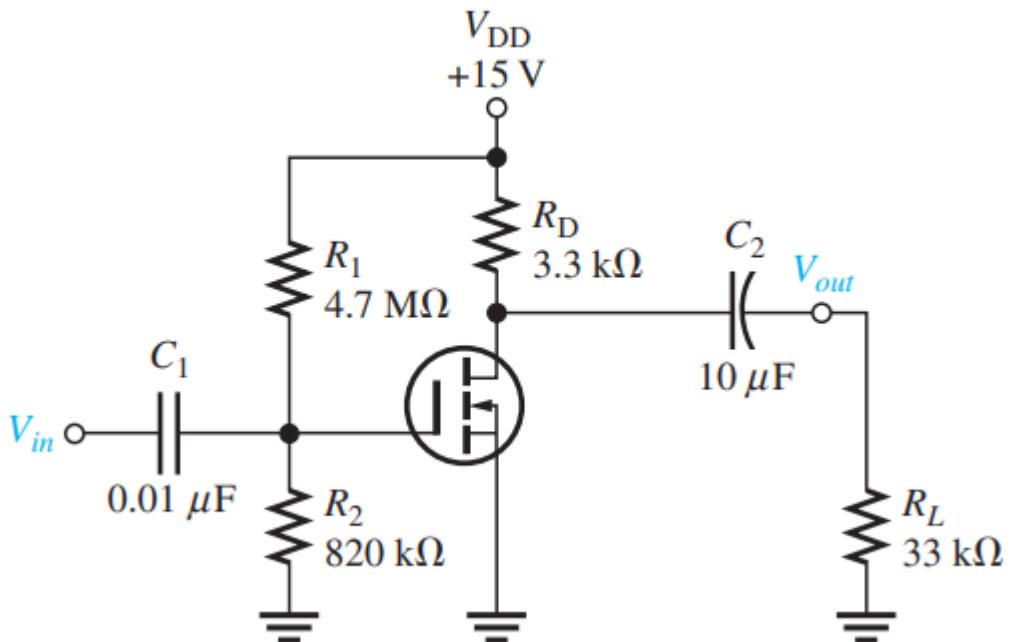
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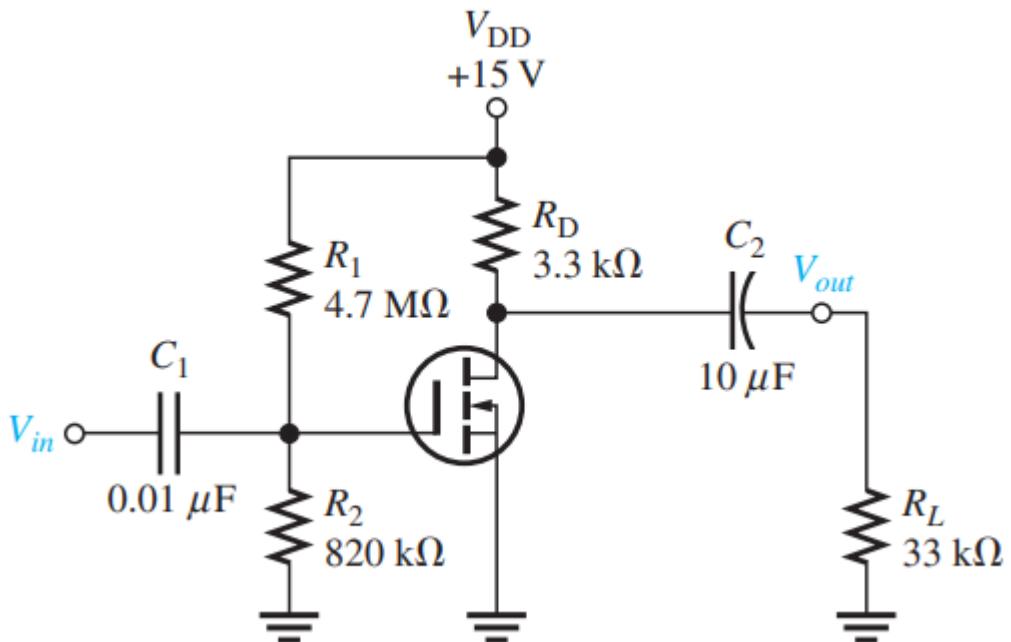
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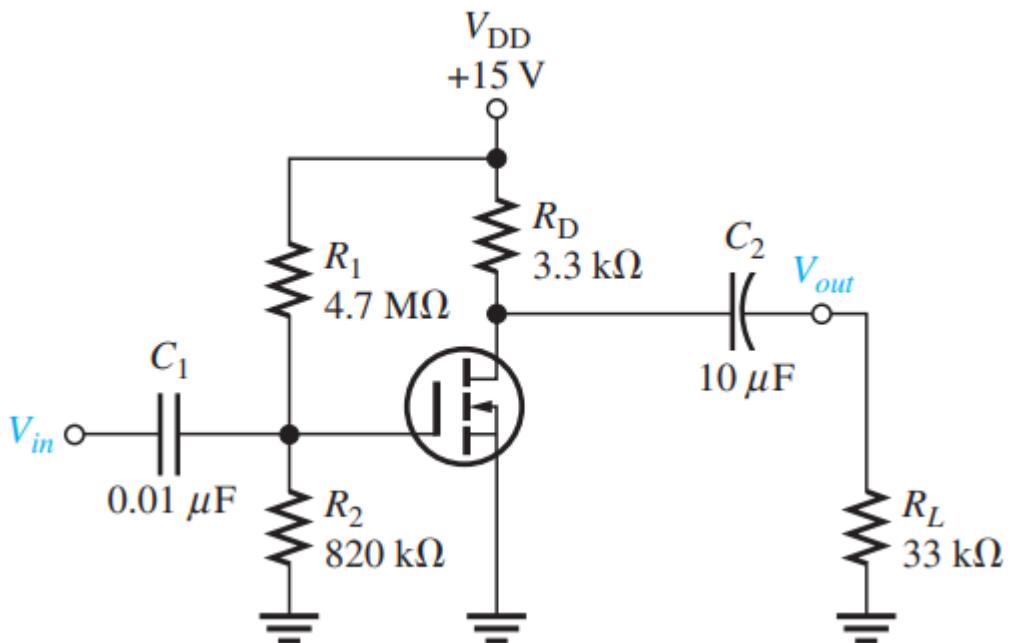
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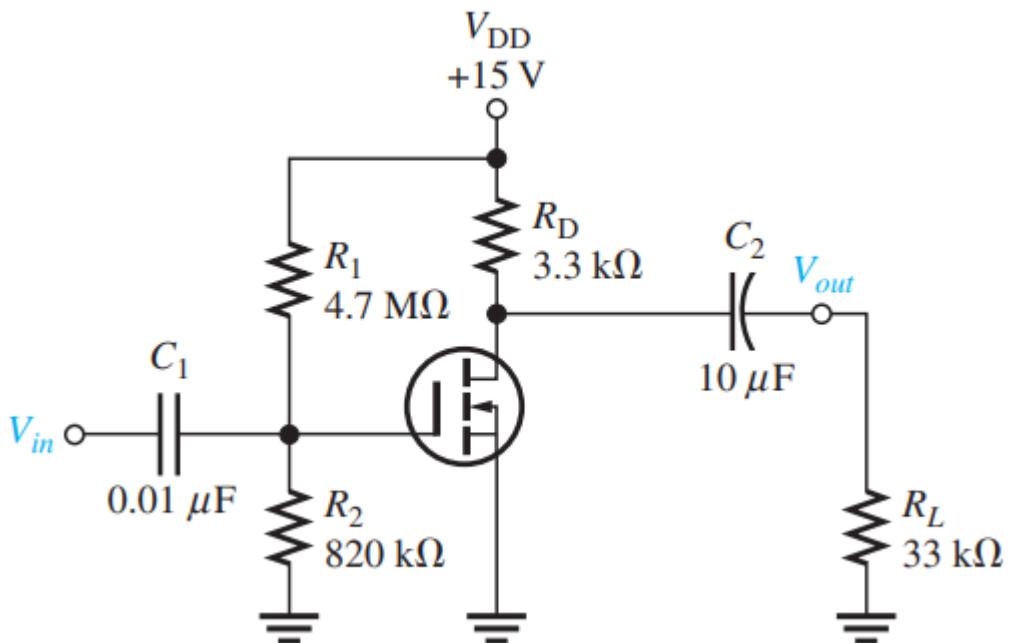
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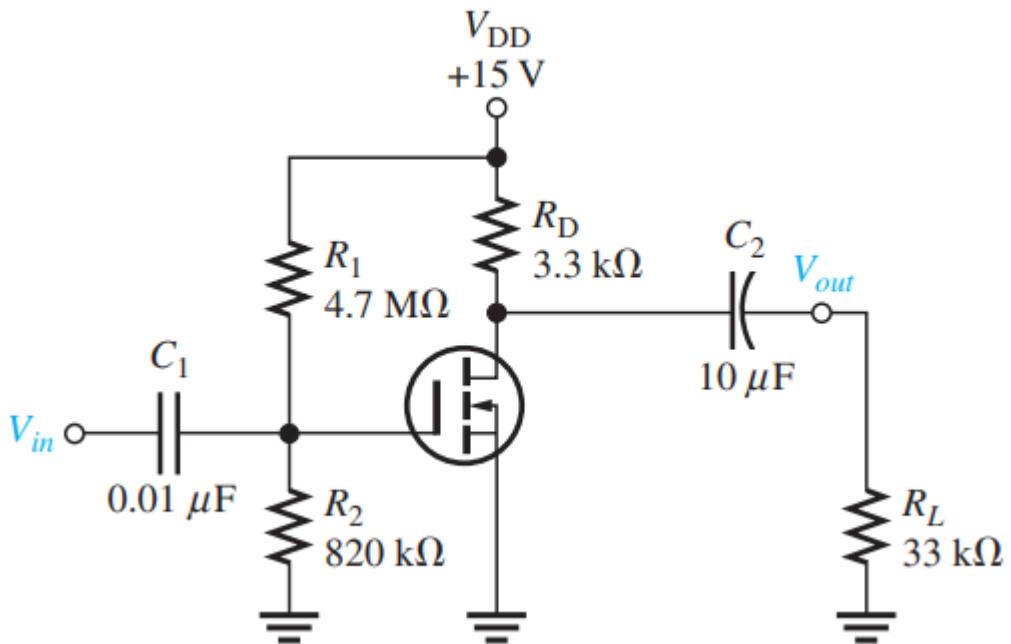
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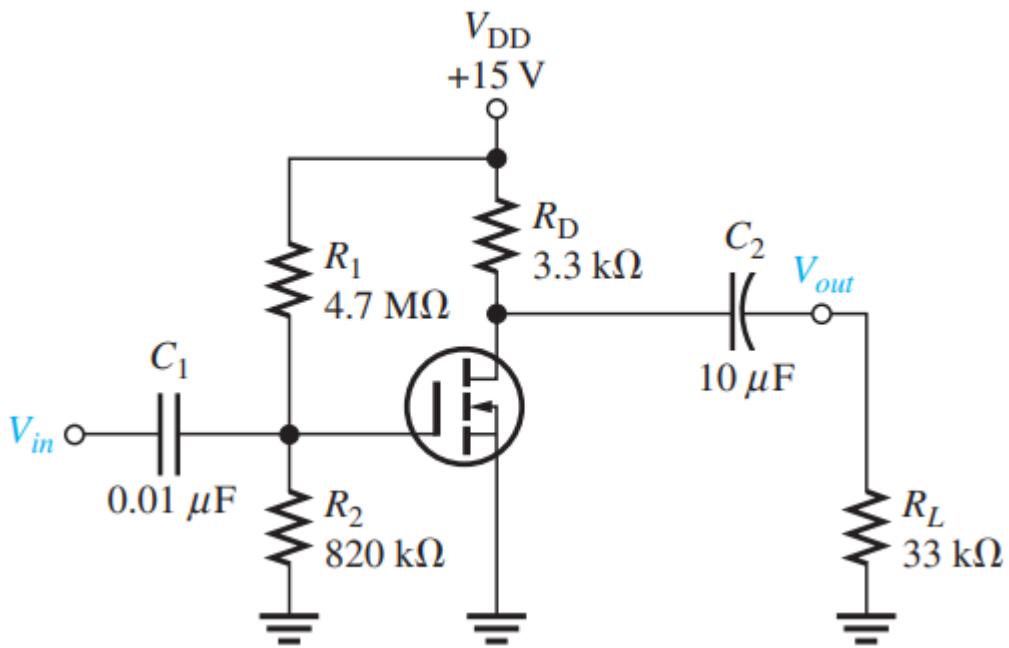
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$$R_d = R_D \parallel R_L = 3.3 \text{ k}\Omega \parallel 33 \text{ k}\Omega = 3 \text{ k}\Omega$$

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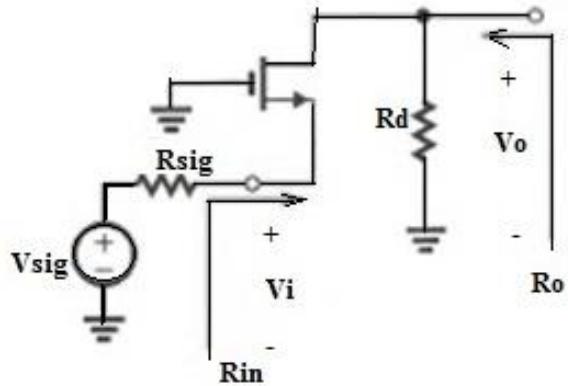
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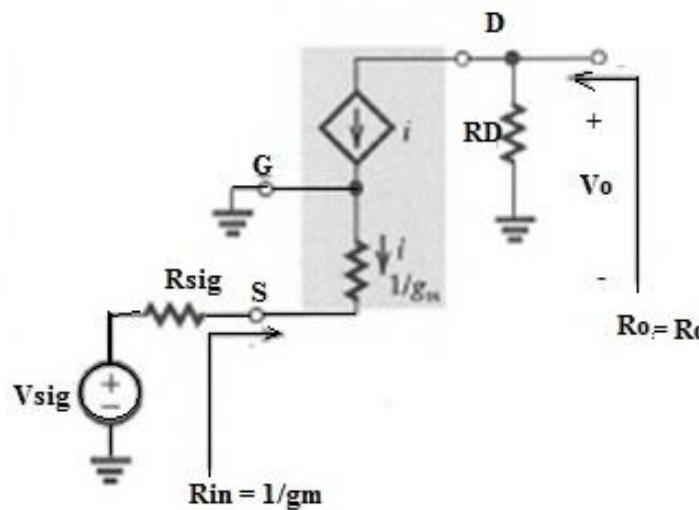
The ac output voltage is

$$V_{out} = A_v V_{in} = g_m R_d V_{in} = (23 \text{ mS})(3 \text{ k}\Omega)(25 \text{ mV}) = 1.73 \text{ V}$$

# A common-gate (CG) MOSFET amplifier

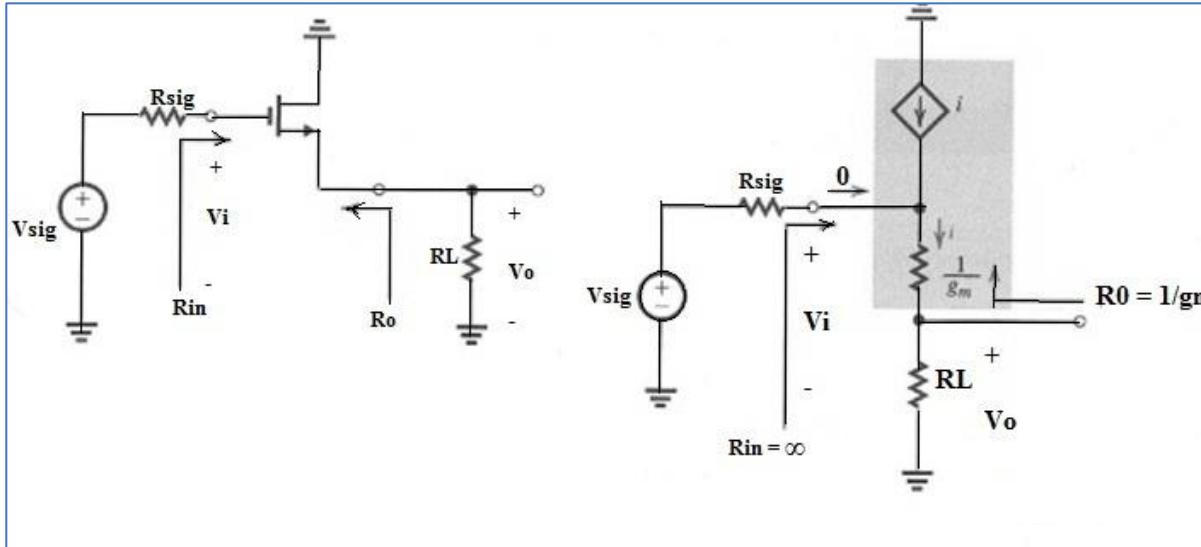


- A common-gate (CG) amplifier is normally used as a voltage amplifier or current buffer.
- In the CG configuration, the source terminal (S) of the transistor works like the input whereas the drain terminal works like the output & the gate terminal is connected to the ground (G).
- The common gate amplifier configuration is mainly used to provide high isolation in between i/p & o/p to prevent oscillation or less input impedance.



- The common gate MOSFET amplifier has less i/p resistance ' $1/gm$ '.
- So, this is undesirable because it will draw a huge current once it is driven through an input voltage.
- The CG amplifier's voltage gain can be made related in magnitude to that of the common source amplifier once  $RD||RL$  can be made large as compared to  $Rsig + 1/gm$ .
- The o/p resistance can be made high as  $Ro = RD$ .
- The frequency performance of this amplifier is high.

# Common Drain Amplifier or Source MOSFET Follower



- A common-drain (CD) amplifier is one where the input signal is given to the gate terminal & the output is obtained from the source terminal, making the drain (D) terminal common to both.
- The CD amplifier is frequently used as a voltage buffer to drive small o/p loads. This configuration provides extremely high i/p impedance & low o/p impedance.

- This common drain amplifier circuit is similar to the emitter follower circuit of the BJT.
- So, it is used as a voltage buffer. This amplifier is a unit-gain amplifier including very huge input impedance although a smaller o/p impedance.
- So it is excellent for high-impedance circuit matching to a less -impedance circuit otherwise to a circuit that works with a larger supply current.

# Three basic amplifier configurations: Summary and comparison

**Objective:** • Compare the general characteristics of the three basic amplifier configurations.

## Characteristics of the three MOSFET amplifier configurations

Configuration	Voltage gain	Current gain	Input resistance	Output resistance
Common source	$A_v > 1$	—	$R_{TH}$	Moderate to high
Source follower	$A_v \approx 1$	—	$R_{TH}$	Low
Common gate	$A_v > 1$	$A_i \approx 1$	Low	Moderate to high

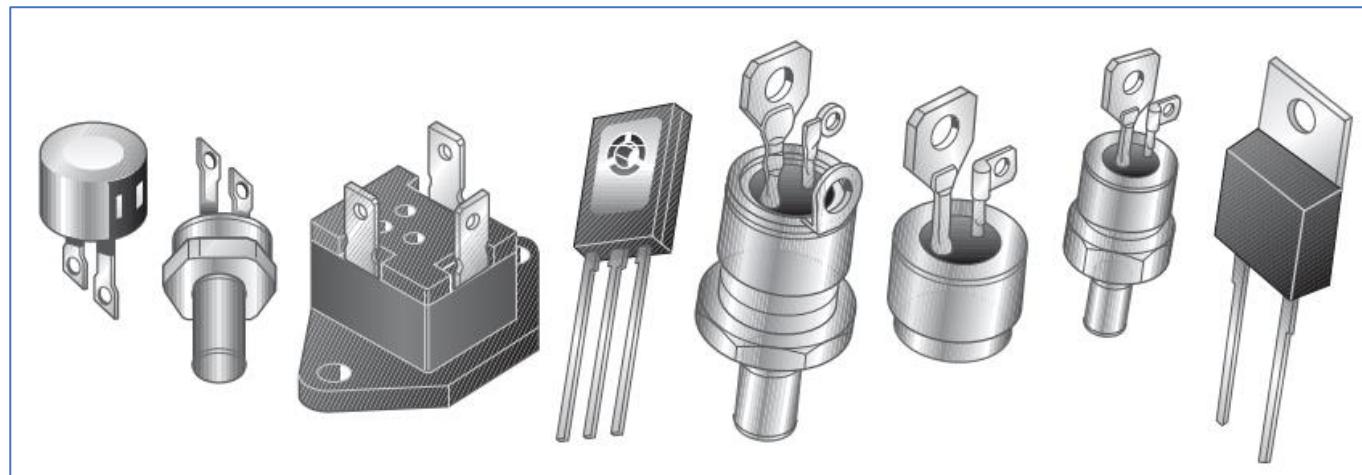
**NOTE : RTH is same as  $R_1 \parallel R_2$**

Circuit configuration	Phase shift
CS	$180^\circ$
CD	0
CG	0

- Common-Source (*CS*) configuration
  - best suited for the *bulk of gain*
- Common-Source (*CS*) configuration with  $R_s$  in the source
  - improved performance but *reduced gain*
- Common-Gate (*CG*) configuration
  - low input resistance
  - excellent high-frequency performance
  - unity-gain current amplifier
  - *cascode amplifier*
- Common-Drain (*CD*) or *Source follower*
  - *voltage buffer* for connecting a high-resistance source to
  - a low –resistance load
  - output stage in a multi-stage amplifier

# Power Devices

- A **power semiconductor device** is a semiconductor device used as a switch or rectifier in power electronics (for example in a switch-mode power supply).
- Such a device is also called a **power device** or, when used in an integrated circuit, a **power IC**.
- A power semiconductor device is usually used in "commutation mode" (i.e., it is either on or off), and therefore has a design optimized for such usage; it should usually not be used in linear operation.
- Linear power circuits are widespread as voltage regulators, audio amplifiers, and radio frequency amplifiers.
- Power semiconductors are found in systems delivering as little as a few tens of milliwatts for a headphone amplifier, up to around a gigawatt in a high voltage direct current transmission line.

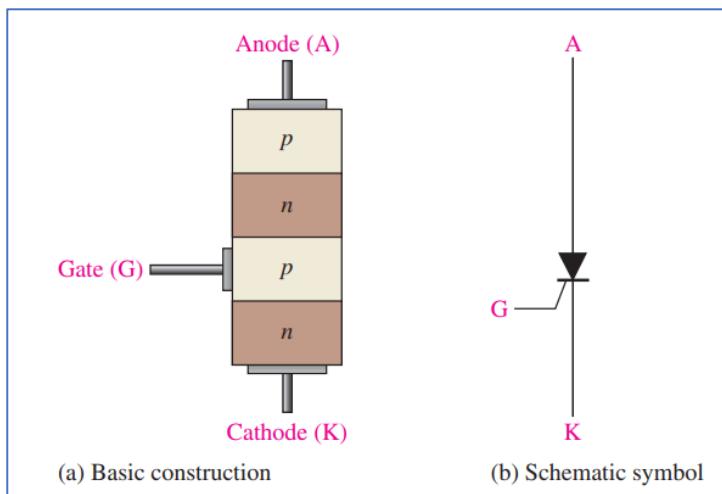


Typical SCR packages

[https://en.wikipedia.org/wiki/Power\\_semiconductor\\_device](https://en.wikipedia.org/wiki/Power_semiconductor_device)

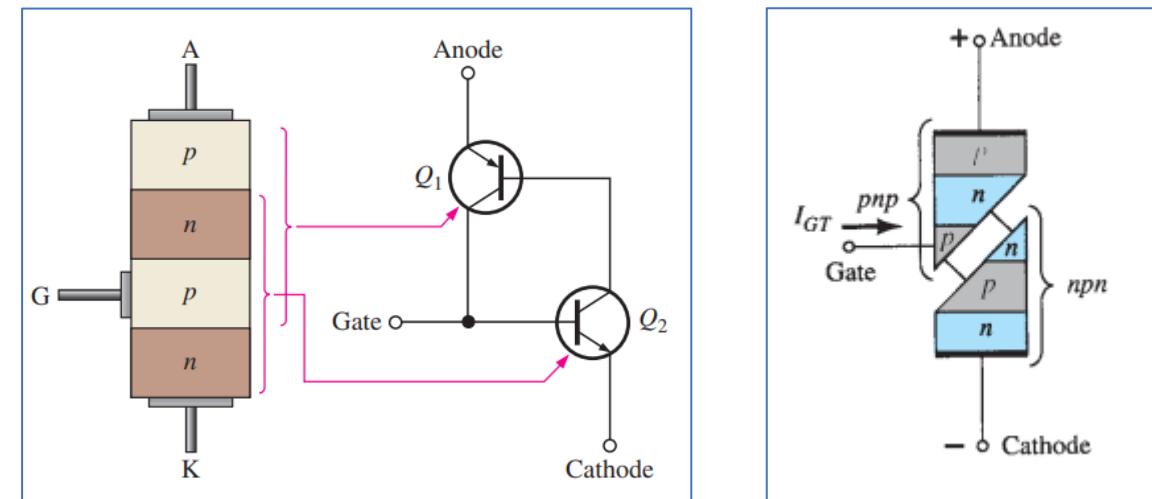
# An SCR (silicon-controlled rectifier)

- An SCR (silicon-controlled rectifier) is a 4-layer pnpn device similar to the 4-layer diode except with three terminals: anode, cathode, and gate.
- The basic structure of an SCR is shown in Figure (a), and the schematic symbol is shown in Figure (b).
- Other types of thyristors are found in the same or similar packages



## SCR Equivalent Circuit

- Like the 4-layer diode operation, the SCR operation can best be understood by thinking of its internal pnpn structure as a two-transistor arrangement, as shown in Figure.
- This structure is like that of the 4-layer diode except for the gate connection.
- The upper pnp layers act as a transistor,  $Q_1$ , and the lower npn layers act as a transistor,  $Q_2$ . Again, notice that the two middle layers are “shared.”

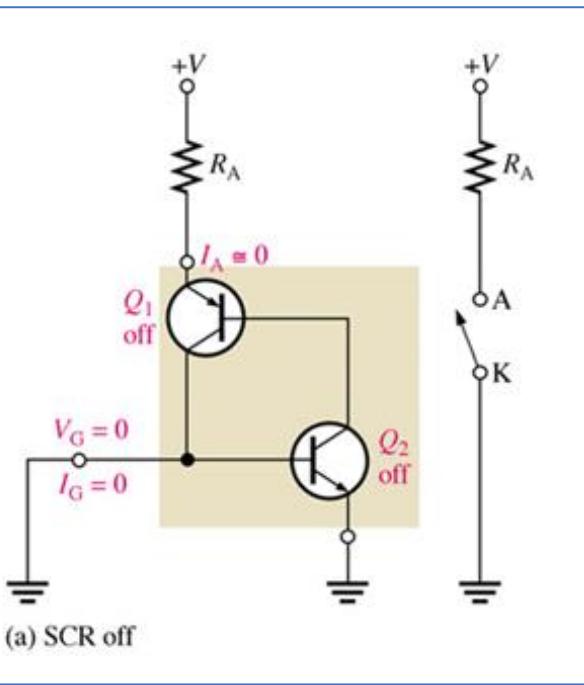


SCR equivalent circuit.

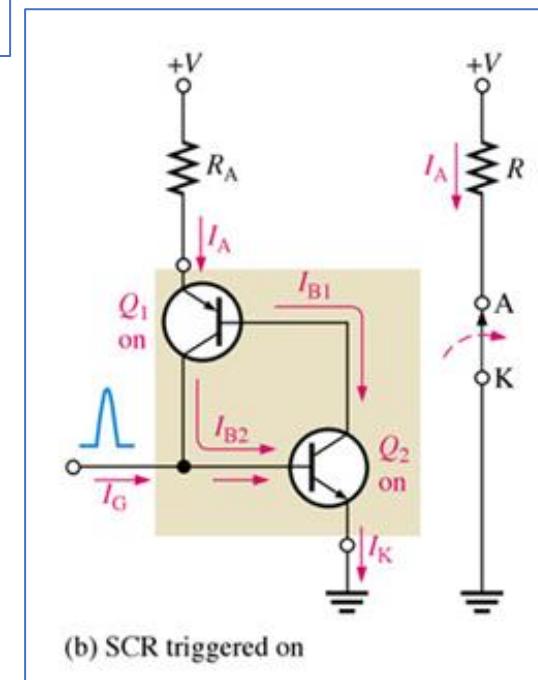
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# An SCR (silicon-controlled rectifier)

- **Turning the SCR On**
- When the gate current,  $I_G$ , is zero, as shown in Figure (a), the device acts as a 4-layer diode in the off state.
- In this state, the very high resistance between the anode and cathode can be approximated by an open switch, as indicated

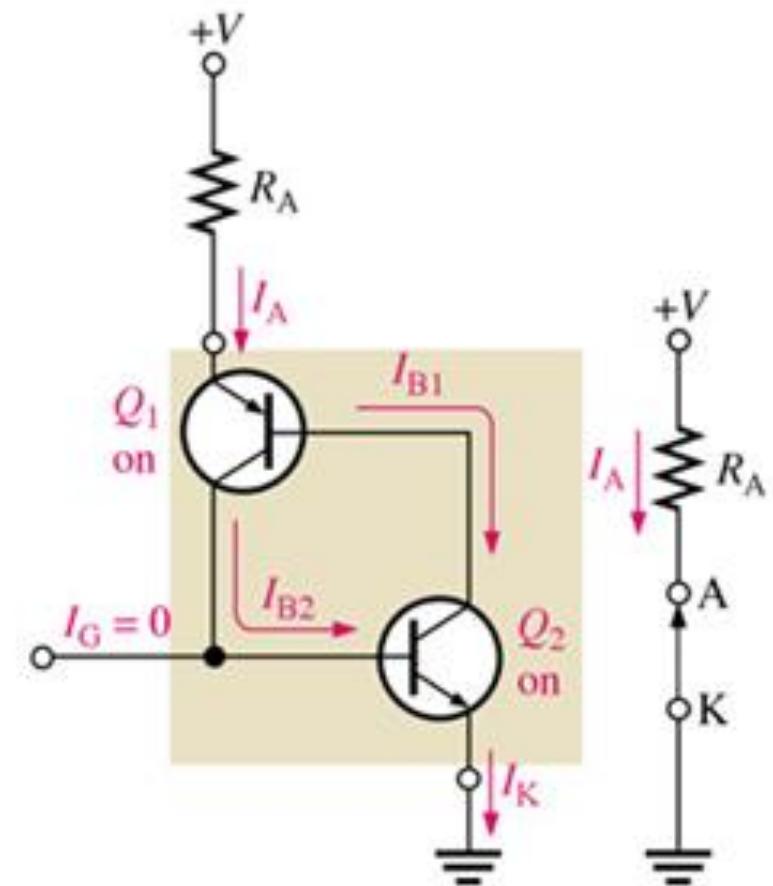


- When a positive pulse of current (trigger) is applied to the gate, both transistors turn on (the anode must be more positive than the cathode).
- This action is shown in Figure (b).  $I_{B2}$  turns on  $Q_2$ , providing a path for  $I_{B1}$  out of the  $Q_2$  collector, thus turning on  $Q_1$ .



# An SCR (silicon-controlled rectifier)

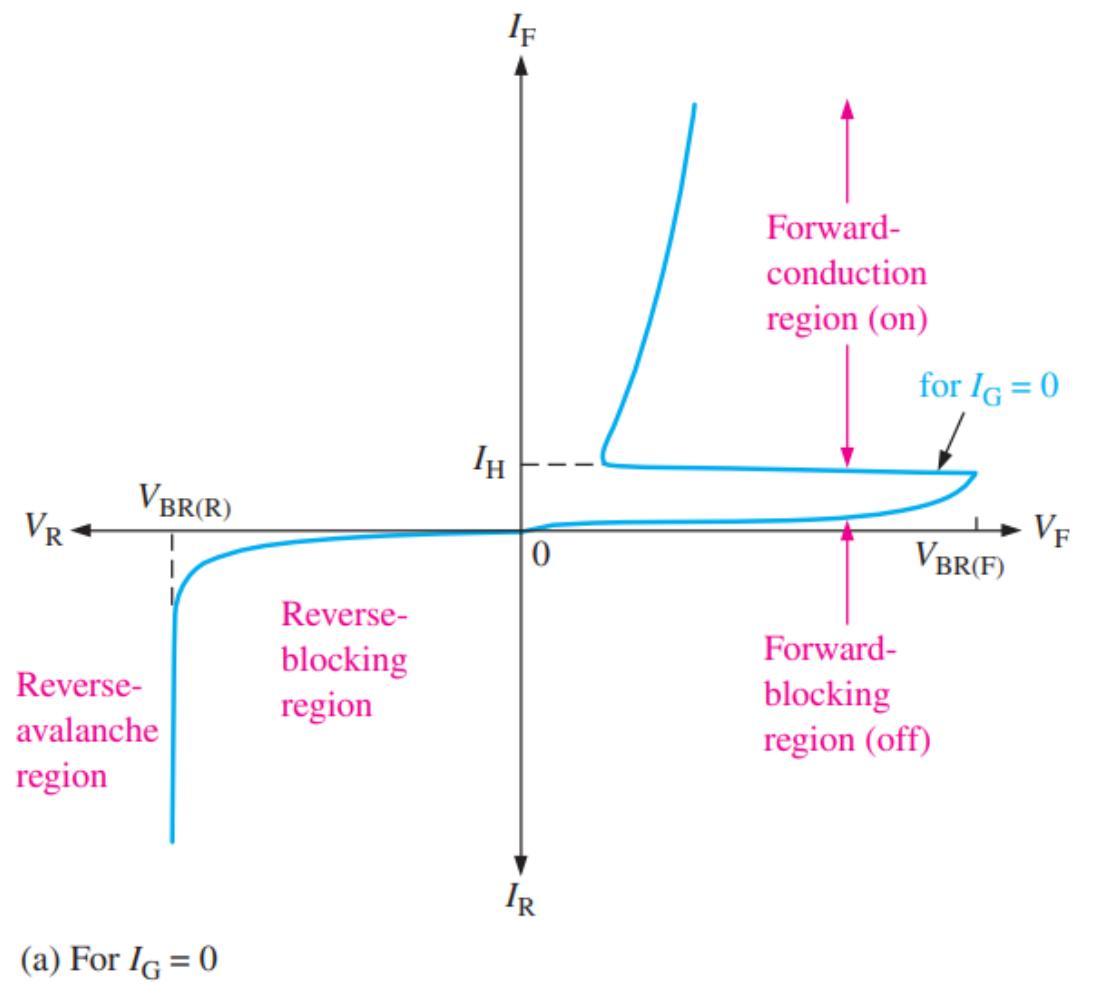
- **Turning the SCR On**
- The collector current of  $Q_1$  provides additional base current for  $Q_2$  so that stays in conduction after the trigger pulse is removed from the gate.
- By this regenerative action,  $Q_2$  sustains the saturated conduction of by providing a path for in turn, sustains the saturated conduction of  $Q_1$  by providing  $I_{B2}$
- Thus, the device stays on (latches) once it is triggered on, as shown in Figure (c). In this state, the very low resistance between the anode and cathode can be approximated by a closed switch, as indicated.



(c) SCR stays on after trigger pulse

# An SCR (silicon-controlled rectifier)

- **Turning the SCR On**
- An SCR can also be turned on without gate triggering by increasing the anode-to-cathode voltage to a value exceeding the forward-breakover voltage  $V_{BR(F)}$  as shown on the characteristic curve in Figure (a).

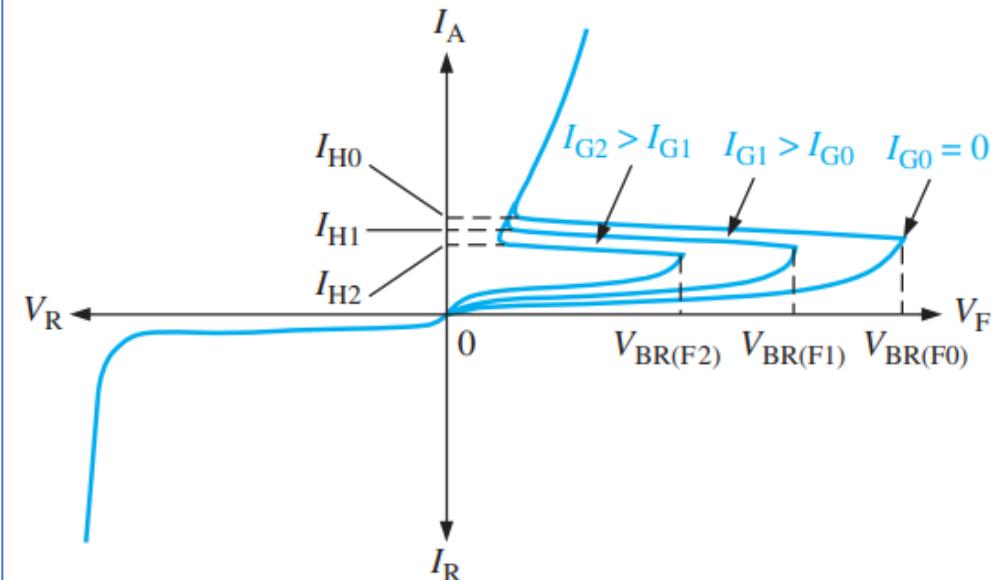


SCR characteristic curve

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# An SCR (silicon-controlled rectifier)

- **Turning the SCR On**
- The forward-breakover voltage decreases as  $I_G$  is increased above 0 V, as shown by the set of curves in Figure (b).
- Eventually, a value of  $I_G$  is reached at which the SCR turns on at a very low anode-to-cathode voltage. So, as you can see, the gate current controls the value of forward breakover voltage,  $V_{BR(F)}$  required for turn-on.
- Although anode-to-cathode voltages in excess of  $V_{BR(F)}$  will not damage the device if current is limited, this situation should be avoided because the normal control of the SCR is lost.
- It should normally be triggered on only with a pulse at the gate.



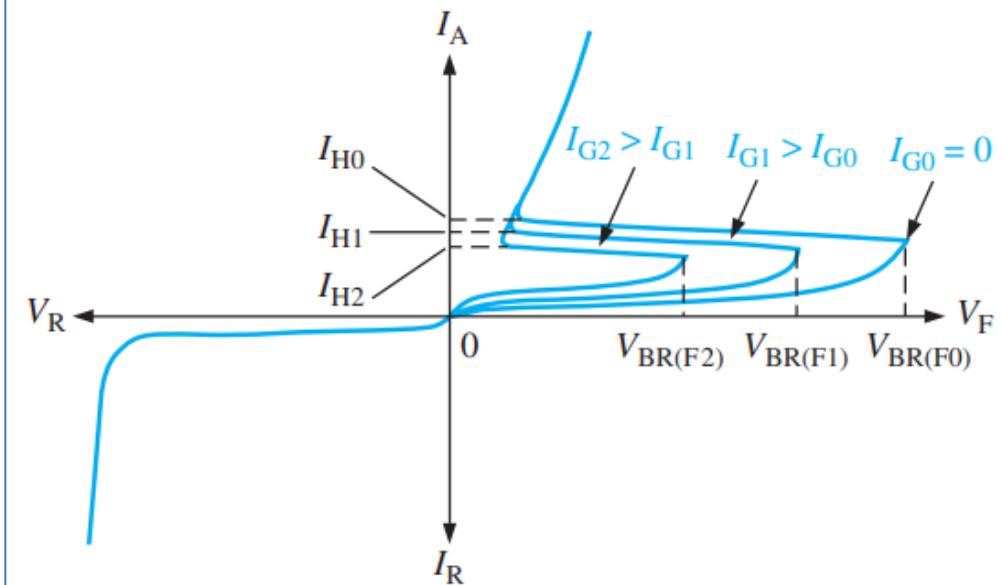
(b) For various  $I_G$  values

SCR characteristic curve

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# An SCR (silicon-controlled rectifier)

- **Turning the SCR Off**
- When the gate returns to 0 V after the trigger pulse is removed, the SCR cannot turn off; it stays in the forward-conduction region.
- The anode current must drop below the value of the holding current, in order for turn-off to occur.
- The holding current is indicated in Figure.



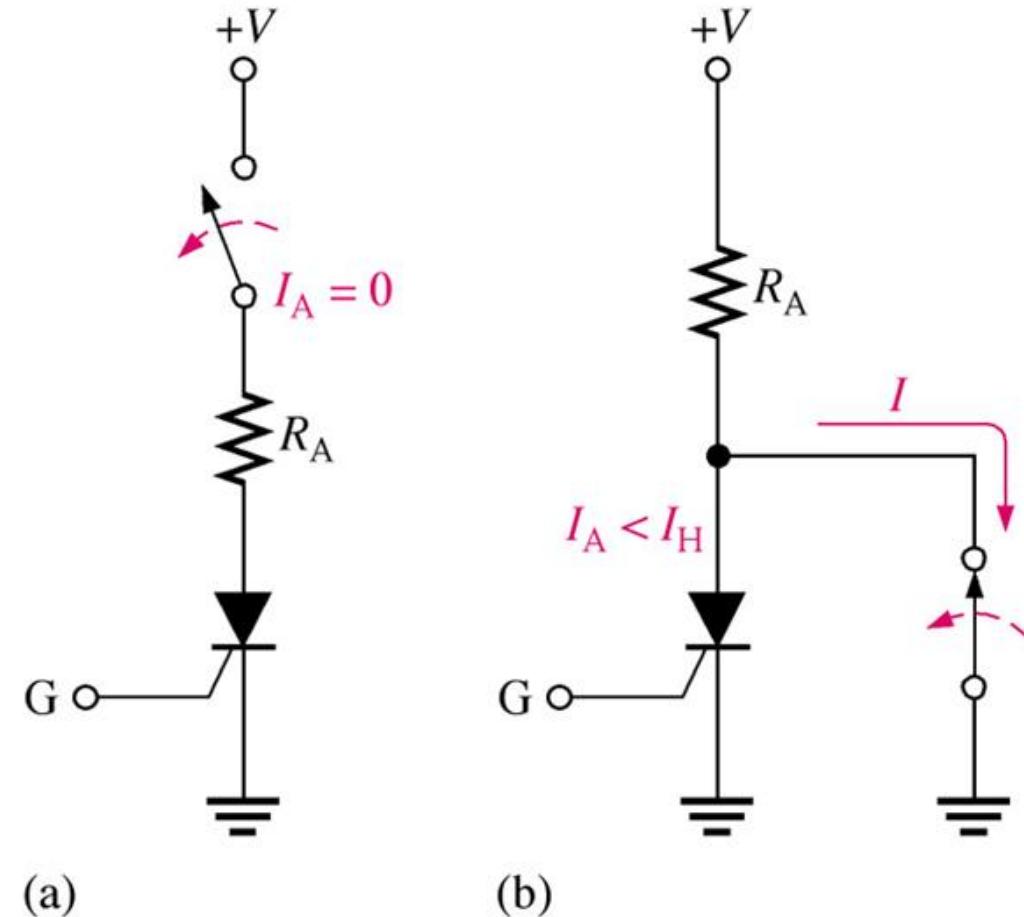
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# An SCR (silicon-controlled rectifier)

- **Turning the SCR Off**
- There are two basic methods for turning off an SCR: **anode current interruption and forced commutation.**
- The anode current can be interrupted by either a momentary series or parallel switching arrangement, as shown in Figure.
- The series switch in part (a) simply reduces the anode current to zero and causes the SCR to turn off.
- The parallel switch in part (b) routes part of the total current away from the SCR, thereby reducing the anode current to a value less than  $I_H$

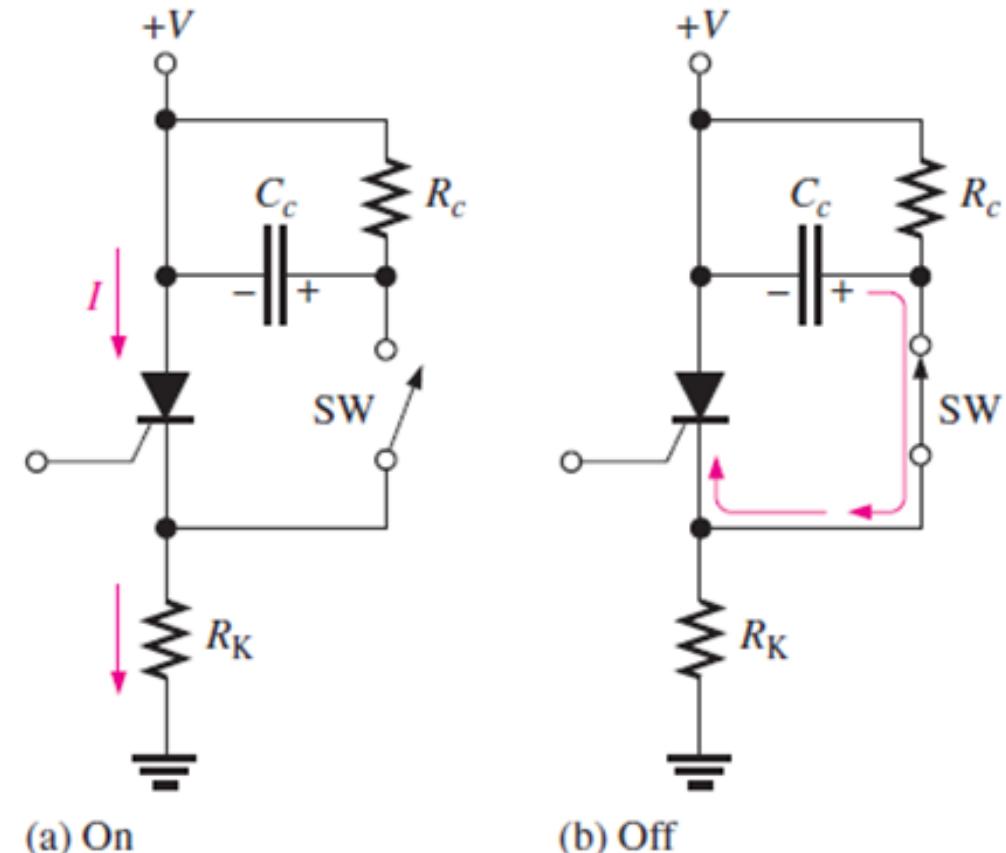


SCR turn-off by anode current interruption.

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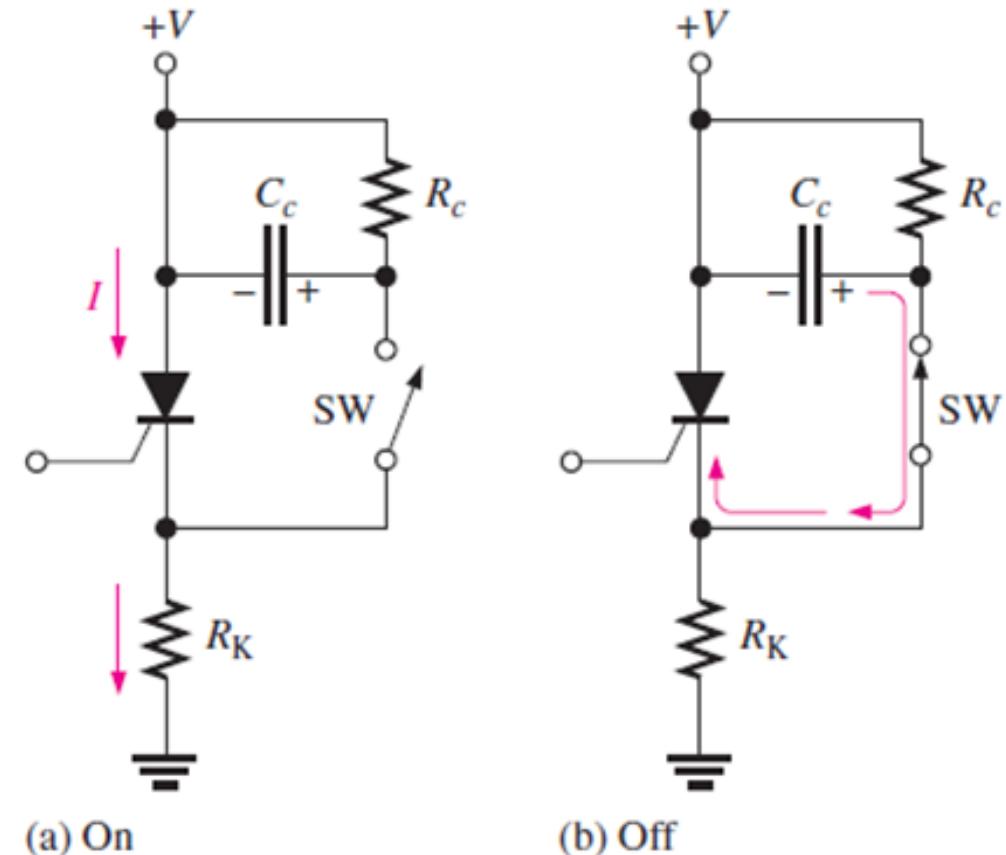
- **Turning the SCR Off**
- **The forced commutation** method basically requires momentarily forcing current through the SCR in the direction opposite to the forward conduction so that the net forward current is reduced below the holding value.
- The basic circuit, as shown in Figure, consists of a switch (normally a transistor switch) and a capacitor.
- While the SCR is conducting, the switch is open and is charged to the supply voltage through , as shown in part (a).
- To turn off the SCR, the switch is closed, placing the capacitor across the SCR and forcing current through it opposite to the forward current, as shown in part (b). Typically, turn-off times for SCRs range from a few microseconds up to about 30 ms.



SCR turn-off by forced commutation

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- The basic circuit, as shown in Figure, consists of a switch (normally a transistor switch) and a capacitor.
- While the SCR is conducting, the switch is open and is charged to the supply voltage through , as shown in part (a).
- To turn off the SCR, the switch is closed, placing the capacitor across the SCR and forcing current through it opposite to the forward current, as shown in part (b). Typically, turn-off times for SCRs range from a few microseconds up to about 30 ms.



SCR turn-off by forced commutation

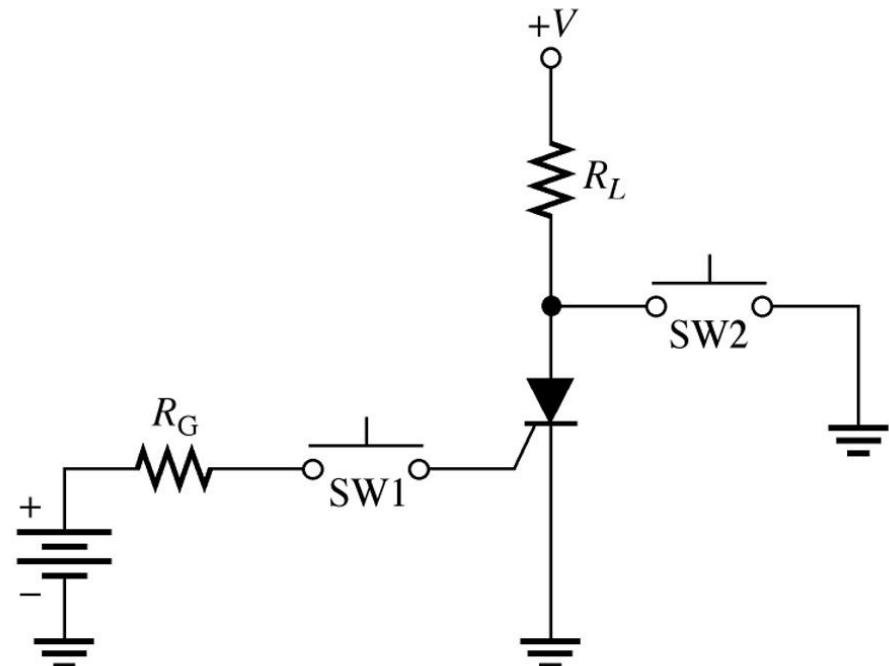
# Applications of Silicon-Controlled Rectifier (SCR),

- An Overvoltage Protection
- Saw tooth waveform generator
- Automatic Backup Lighting Circuits
- Half wave power control
- On-Off control
- Power regulators
- Motor control applications

# Applications of Silicon-Controlled Rectifier (SCR),

- **On-Off Control of Current**

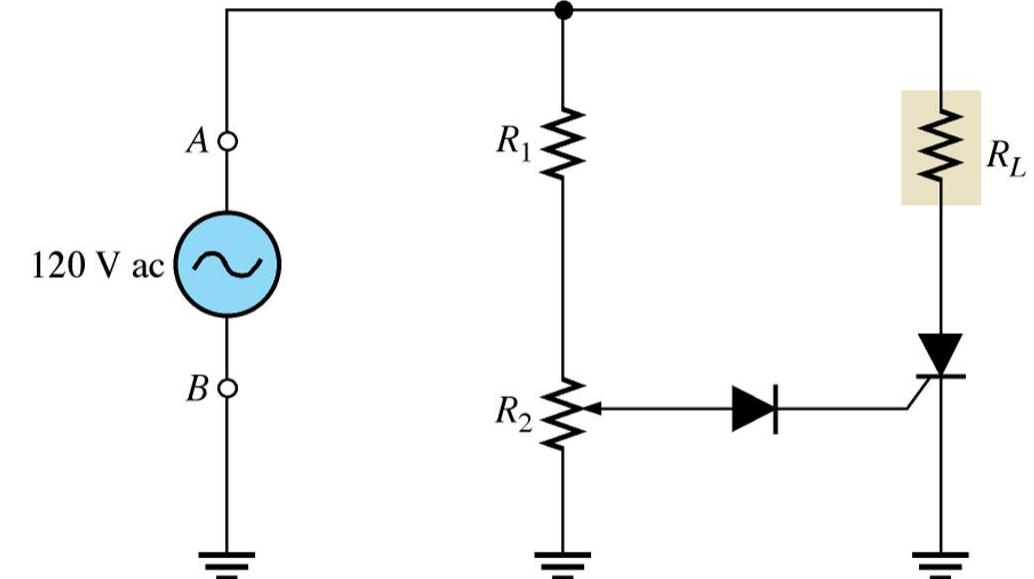
- Figure shows an SCR circuit that permits current to be switched to a load by the momentary closure of switch SW1 and removed from the load by the momentary closure of switch SW2
- Assuming the SCR is initially off, momentary closure of SW1 provides a pulse of current out of the gate, thus triggering the SCR on so that it conducts current through  $R_L$ .
- The SCR remains in conduction even after the momentary contact of SW1 is removed if the anode current is equal to or greater than the holding current,  $I_H$ .
- When SW2 is momentarily closed, current is shunted around the SCR, thus reducing its anode current below the holding value,  $I_H$ .
- This turns the SCR off and reduces the load current to zero



# Applications of Silicon-Controlled Rectifier (SCR),

- **Half-Wave Power Control**

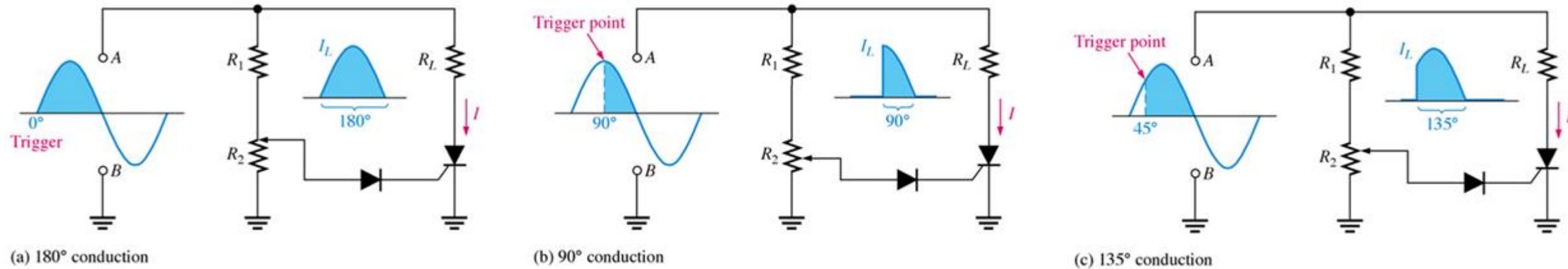
- A common application of SCRs is in the control of ac power for lamp dimmers, electric heaters, and electric motors.
- A half-wave, variable-resistance, phase-control circuit is shown in Figure ; 120 V ac are applied across terminals A and B;  $R_L$  represents the resistance of the load (for example, a heating element or lamp filament).
- Resistor  $R_1$  limits the current, and potentiometer  $R_2$  sets the trigger level for the SCR.



Half-wave, variable-resistance, phase control circuit

# Applications of Silicon-Controlled Rectifier (SCR),

- Half-Wave Power Control



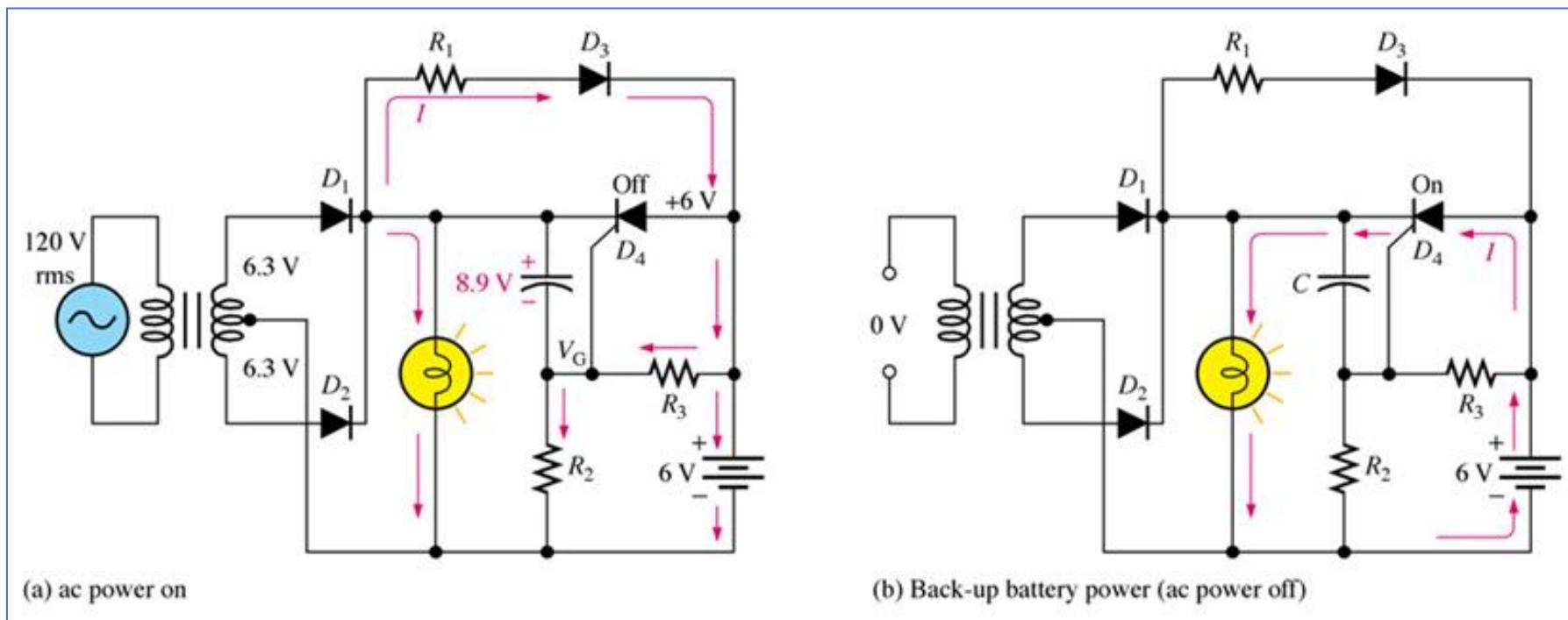
Operation of the phase-control circuit.

Acknowledgment:-Thomas L. Floyd Electronic Devices, Electron Flow Version, Ninth Edition

# Applications of Silicon-Controlled Rectifier (SCR),

- **Backup Lighting for Power Interruptions**

- As another example of SCR applications, let's examine a circuit that will maintain lighting by using a backup battery when there is an ac power failure.
- Figure 11–21 shows a center-tapped full-wave rectifier used for providing ac power to a low-voltage lamp.
- As long as
- the ac power is available, the battery charges through diode D3 and R1 .

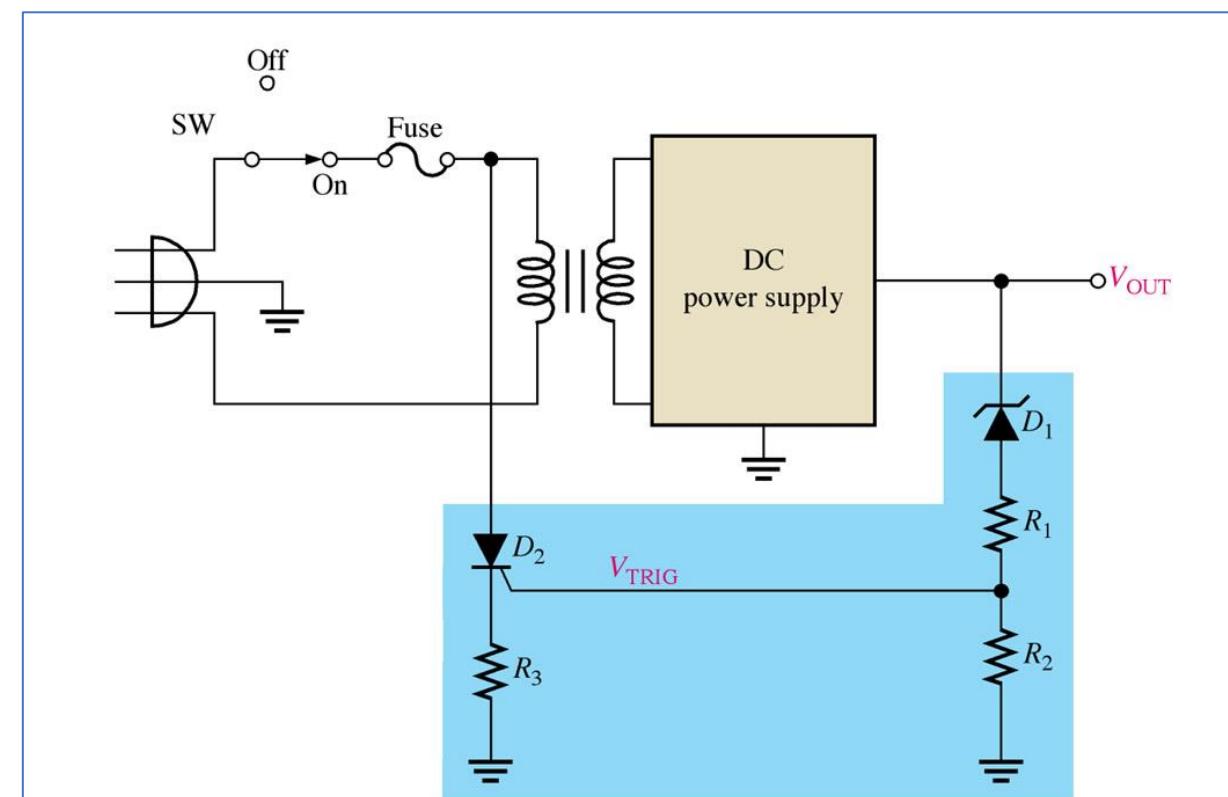


Automatic back-up lighting circuit.

# Applications of Silicon-Controlled Rectifier (SCR),

- An Over-Voltage Protection Circuit

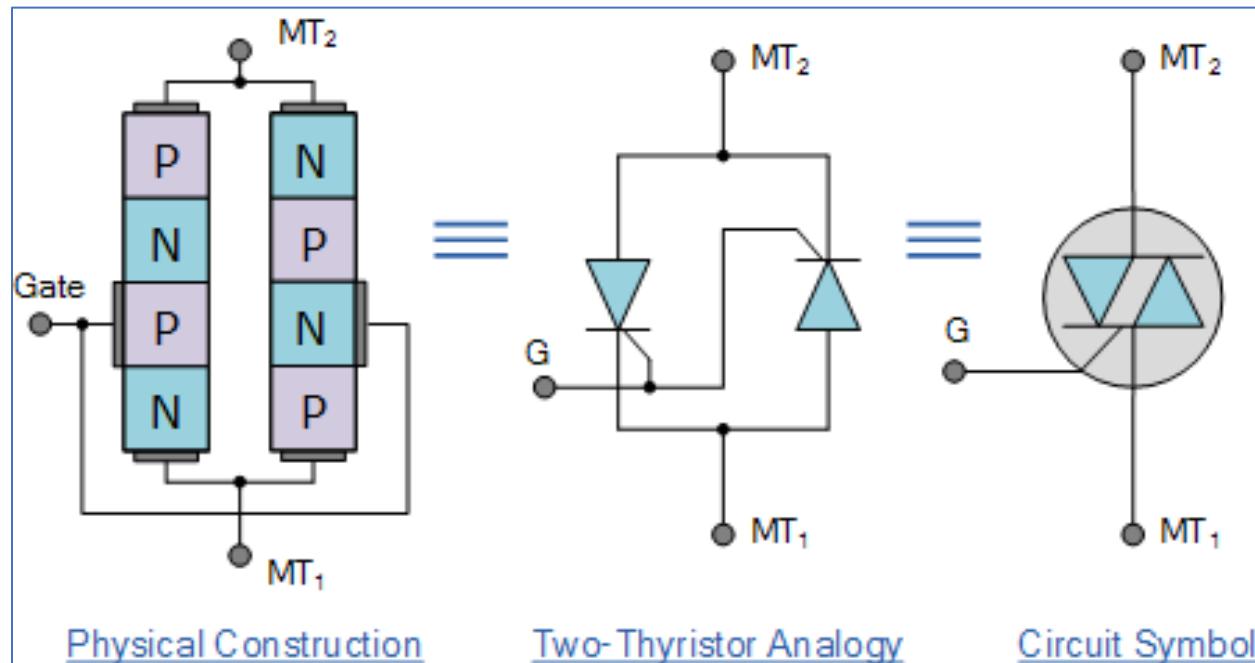
- Figure shows a simple over-voltage protection circuit, sometimes called a “crowbar” circuit, in a dc power supply.
- The dc output voltage from the regulator is monitored by the zener diode ( $D_1$ ) and the resistive voltage divider ( $R_1$  and  $R_2$ ).
- The upper limit of the output voltage is set by the zener voltage.
- If this voltage is exceeded, the zener conducts and the voltage divider produces an SCR trigger voltage.
- The trigger voltage turns on the SCR, which is connected across the line voltage.
- The SCR current causes the fuse to blow, thus disconnecting the line voltage from the power supply



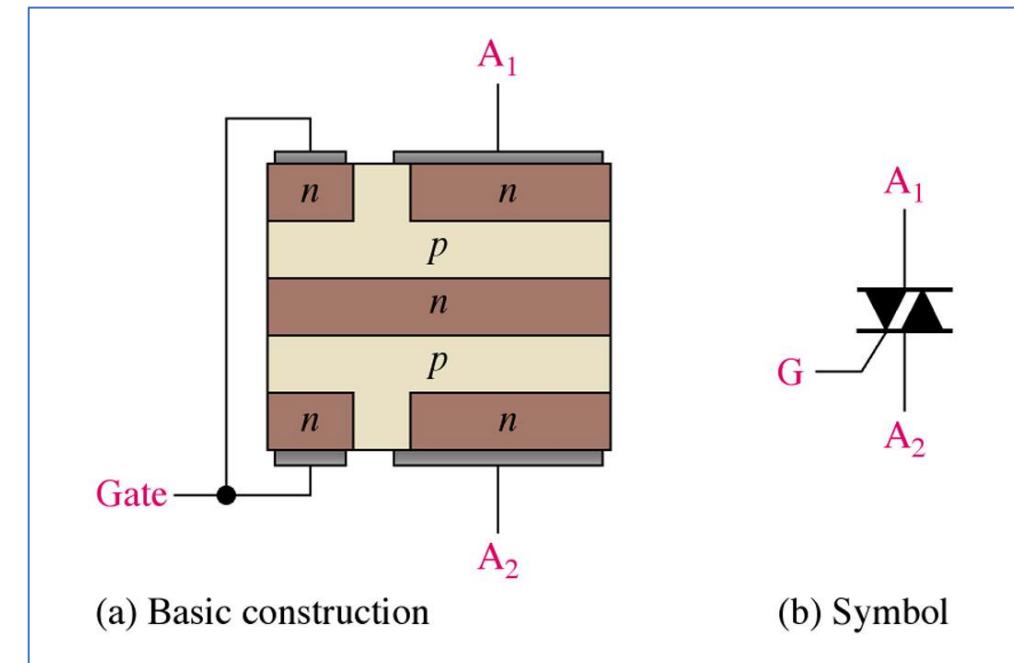
A basic SCR over-voltage protection circuit (shown in blue).

# The TRIAC

- A Triac is defined as a three terminal AC switch which is different from the other silicon controlled rectifiers in the sense that it can conduct in both the directions that is whether the applied gate signal is positive or negative, it will conduct. Thus, this device can be used for AC systems as a switch.

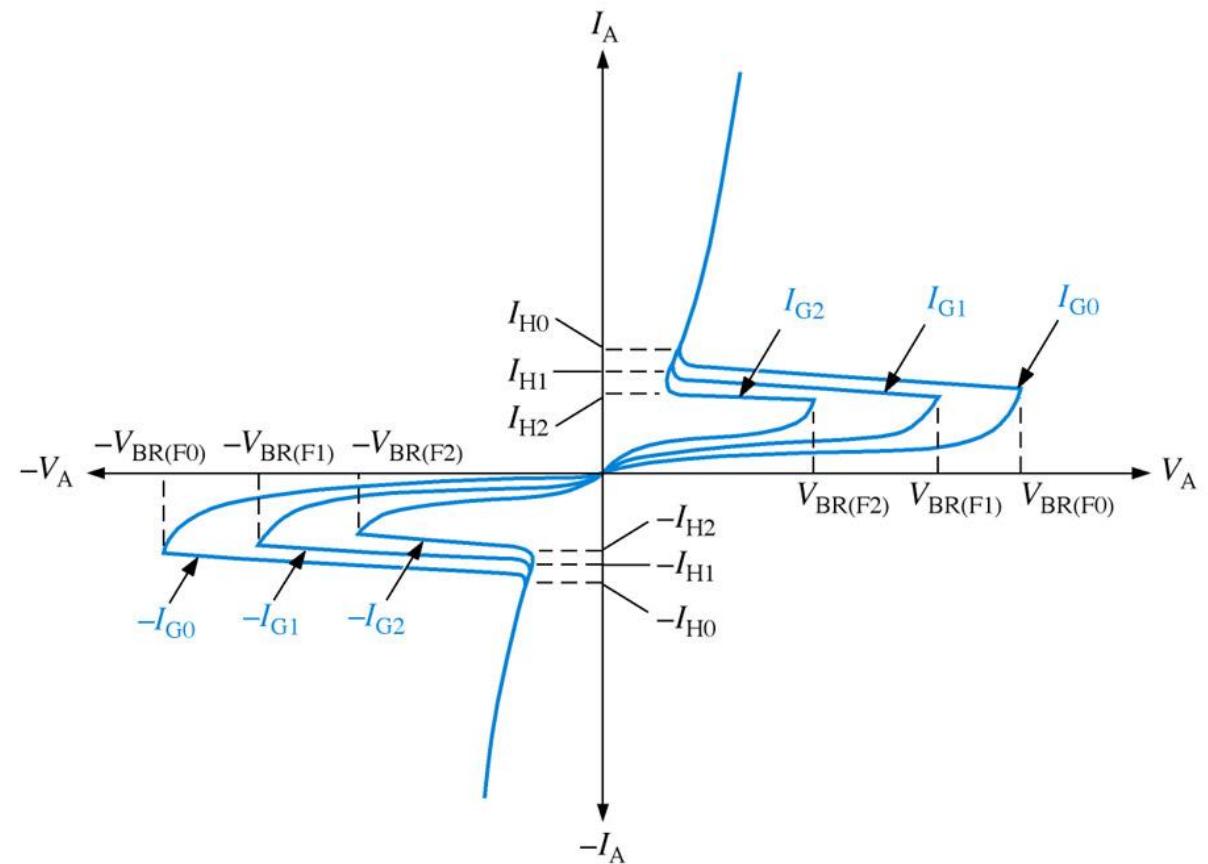


**The TRIAC: Basic Construction and symbol**



# The TRIAC : characteristic curves

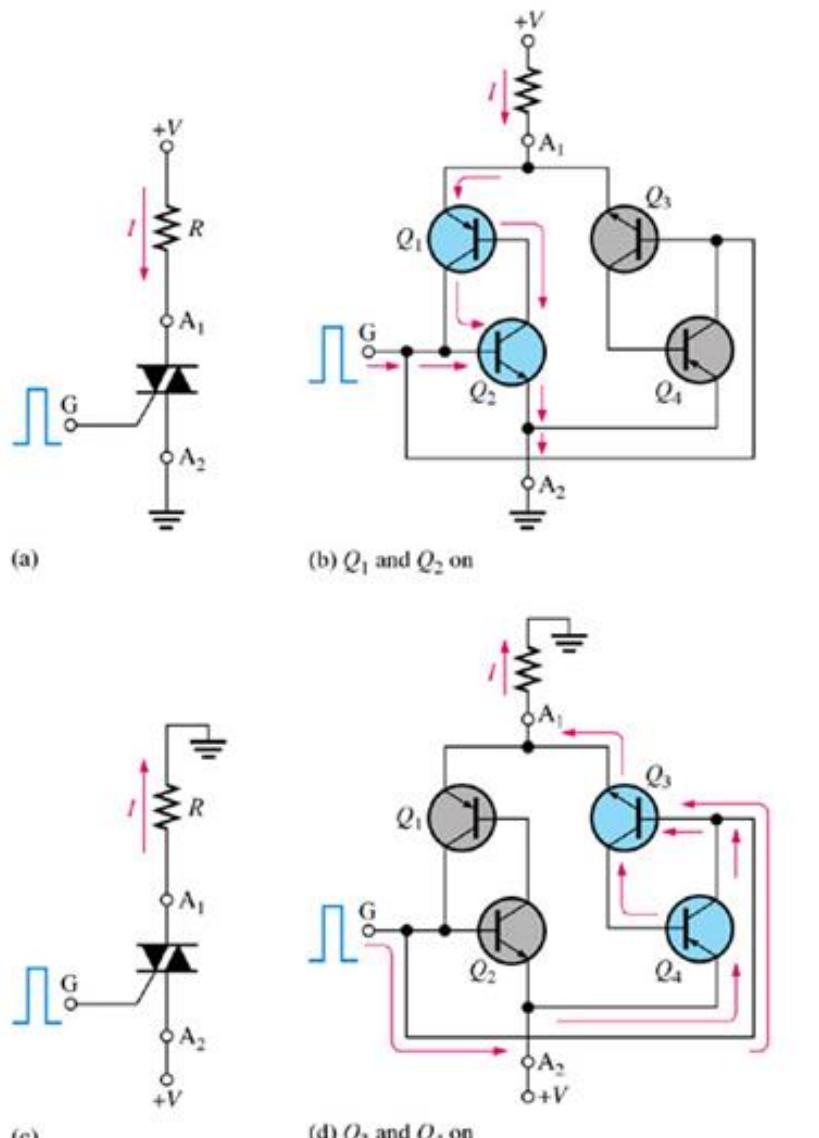
- The characteristic curve is shown in Figure .
- Notice that the breakdown potential decreases as the gate current increases, just as with the SCR.
- As with other thyristors, the triac ceases to conduct when the anode current drops below the specified value of the holding current,  $I_H$  .
- The only way to turn off the triac is to reduce the current to a sufficiently low level.



Triac characteristic curves

# The TRIAC : Bilateral operation

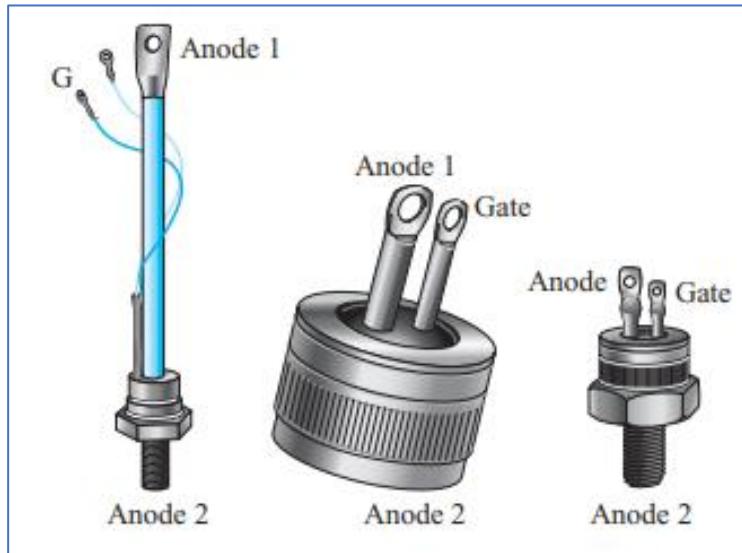
- Figure shows the triac being triggered into both directions of conduction.
- In part(a), terminal A1 is biased positive with respect to A2 so the triac conducts as shown when triggered by a positive pulse at the gate terminal.
- The transistor equivalent circuit in part (b) shows that Q1 and Q2 conduct when a positive trigger pulse is applied.
- In part (c), terminal A2 is biased positive with respect to A1 so the triac conducts as shown.
- In this case, Q3 and Q4 conduct as indicated in part (d) upon application of a positive trigger pulse.



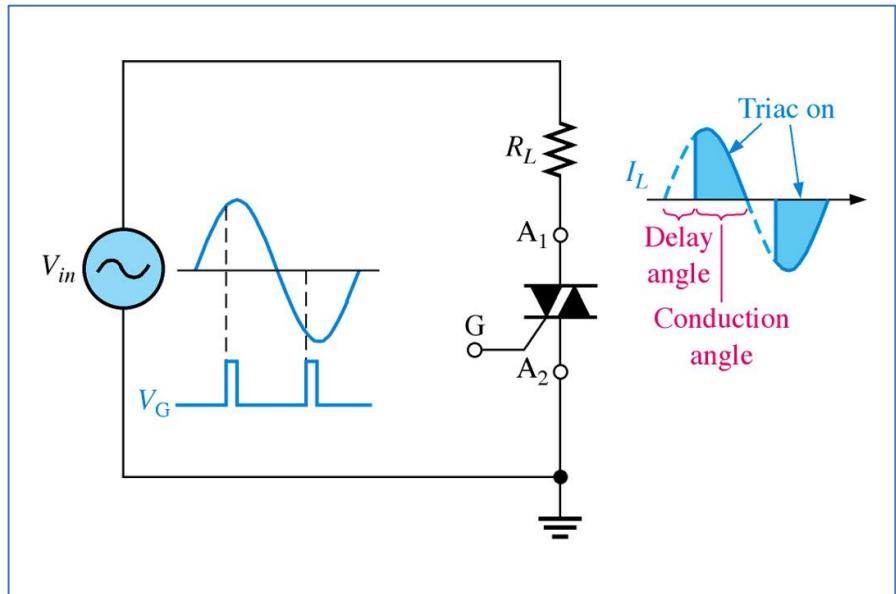
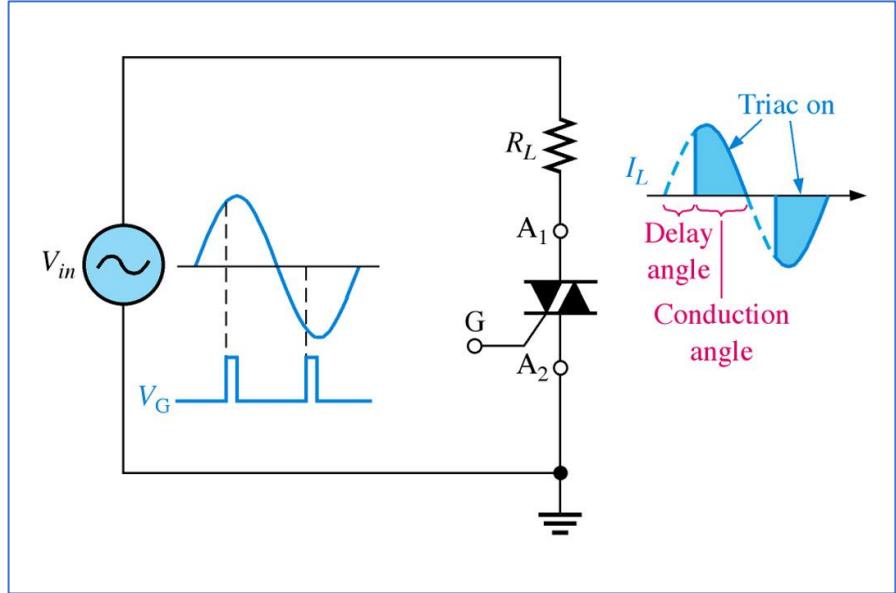
Bilateral operation of a triac

# The TRIAC : Applications

- Phase Control Circuit
- Control circuits like electric fan speed control and smaller motor controls.
- High Power lamp switching and light dimmers.
- AC power control domestic appliances.



photographs of the device



Basic triac phase control

Acknowledgment:-Thomas L. Floyd Electronic Devices, Electron Flow Version, Ninth Edition

THANK YOU