# **Computer Organization**

### 1. The input fields of each pipeline register:

IF/ID:

input: PC add1, instr

ID/EX:

input : RegWrite, MemtoReg, Branch, MemRead, MemWrite, RegDst, ALUOp,
ALUSrc, PC\_add1, ReadData1, ReadData2, signextend, instr[20:16],
instr[15:11]

EX/MEM:

input: RegWrite, MemtoReg, Branch, MemRead, MemWrite, ALU\_result, zero,
ReadData2, branch\_address, write\_address

MEM/WB:

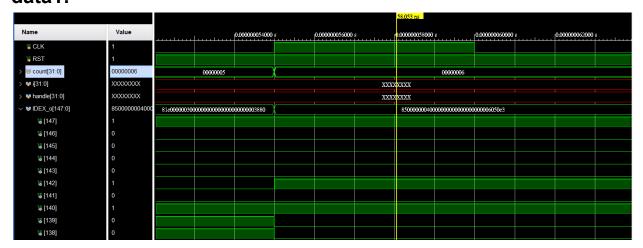
input: RegWrite, MemtoReg, Readdata, ALU\_result, write\_address

2. Compared with lab4, the extra modules:

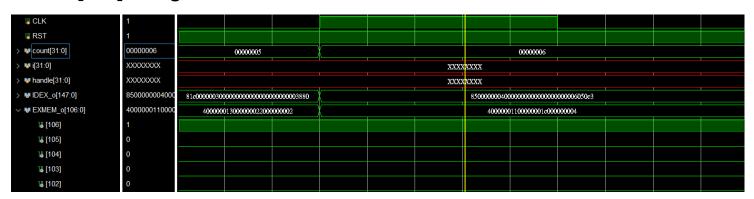
Pipeline\_Reg.v : To hold information produced in the previous cycle.

3. Explain your control signals in sixth cycle (both test patterns CO\_P5\_test\_data1 and CO\_P5\_test\_data2 are needed):

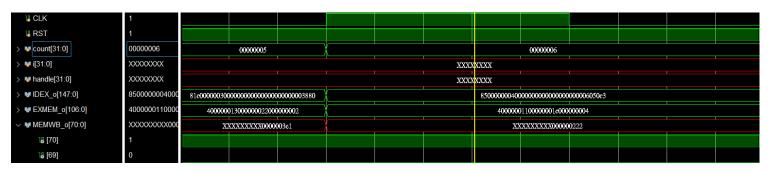
#### data1:



在ID/EX這個pipeline中, [138]是ALUSrc, [141:139]是ALUOp, [142]是RegDst。



在EX/MEM這個pipeline中, [102]是MemWrite, [103]是MemRead, [104]是Branch。



在MEM/WB這個pipeline中, [69]是MemtoReg[0](在本次作業中MemtoReg[1]這個bit並沒有用到, 因此實作部分中不採用), [70]是RegWrite。

## data2:(資料如data1所示)

| ∨ № IDEX_o[147:0] | 81c0000004000 | 81c0000003000 | 0000000000 | <u> </u> |  |  | 81c00 | 00004000000000 |  |  |  |  |
|-------------------|---------------|---------------|------------|----------|--|--|-------|----------------|--|--|--|--|
| 18 [147]          | 1             |               |            |          |  |  |       |                |  |  |  |  |
| 18 [146]          | 0             |               |            |          |  |  |       |                |  |  |  |  |
| 18 [145]          | 0             |               |            |          |  |  |       |                |  |  |  |  |
| 18 [144]          | 0             |               |            |          |  |  |       |                |  |  |  |  |
| ¼ [143]           | 0             |               |            |          |  |  |       |                |  |  |  |  |
| Ta [142]          | 0             |               |            |          |  |  |       |                |  |  |  |  |
| 18 [141]          | 0             |               |            |          |  |  |       |                |  |  |  |  |
| ⅓ [140]           | 1             |               |            |          |  |  |       |                |  |  |  |  |
| 18 [139]          | 1             |               |            |          |  |  |       |                |  |  |  |  |
| 18 [138]          | 1             |               |            |          |  |  |       |                |  |  |  |  |

|                    |               |               |                |   |                |   |         | 58.460 ns |                |   |      |                |   |               |
|--------------------|---------------|---------------|----------------|---|----------------|---|---------|-----------|----------------|---|------|----------------|---|---------------|
| Name               | Value         |               | 0.000000054000 | 8 | 0.000000056000 | 8 | 0.00000 | 0058000   | 8              | 0.000000060000                          | 8    | 0.000000062000 | s | 0.00000006400 |
| <b>¼</b> CLK       | 1             |               |                |   |                |   |         |           |                |   |      |                |   |               |
| <b>¼</b> RST       | 1             |               |                |   |                |   |         |           |                |   |      |                |   |               |
| > W count[31:0]    | 00000006      | 000           | 00005          |   |                |   |         |           | 0000           | 0006                                    |      |                |   |               |
| > w i[31:0]        | XXXXXXXX      |               |                |   |                |   |         | XXX       | XXXXX          |   |      |                |   |               |
| > W handle[31:0]   | XXXXXXXX      |               |                |   |                |   |         | XXX       | XXXXX          |   |      |                | 1 |               |
| > WIDEX_o[147:0]   | 81c0000004000 | 81c0000003000 | 0000000000     |   |                |   |         | 81c00     | 0000400000000  | 000000000000000000000000000000000000000 | 28a0 |                |   |               |
| ∨ W EXMEM_o[106:0] | 4000000c0000  | 40000000a0000 | 00001000000    |   |                |   |         |           | 40000000c00000 | 0012000000004                           |      |                |   |               |
| 18 [106]           | 1             |               |                |   |                |   |         |           |                |   |      |                |   |               |
| 18 [105]           | 0             |               |                |   |                |   |         |           |                |   |      |                |   |               |
| 18 [104]           | 0             |               |                |   |                |   |         |           |                |   |      |                |   |               |
| 18 [103]           | 0             |               |                |   |                |   |         |           |                |   |      |                |   |               |
| ₩ [102]            | 0             |               |                |   |                |   |         |           |                |   |      |                |   |               |

|                         |               |                  |                |   |                |   |                   | 58.460 ns |                |   |      |                |   |                |
|-------------------------|---------------|------------------|----------------|---|----------------|---|-------------------|-----------|----------------|---|------|----------------|---|----------------|
| Name                    | Value         |                  | 0.000000054000 | 8 | 0.000000056000 | 8 | 0.00000           | 0058000   | 8              | 0.000000060000                          | ·    | 0.000000062000 | 8 | 0.000000064000 |
| <b>¼</b> CLK            | 1             |                  |                |   |                |   |                   |           |                |   |      |                |   |                |
| <b>¼</b> RST            | 1             |                  |                |   |                |   |                   |           |                |   |      |                |   |                |
| > w count[31:0]         | 00000006      | 0000             | 0005           |   |                |   |                   |           | 0000           | 0006                                    |      |                |   |                |
| > 🕨 i[31:0]             | XXXXXXXX      |                  |                |   |                |   |                   | XXX       | XXXXX          |   |      |                |   |                |
| > <b>W</b> handle[31:0] | XXXXXXXXX     |                  |                |   |                |   |                   | XXX       | XXXXX          |   |      |                |   |                |
| > ₩ IDEX_o[147:0]       | 81c0000004000 | 81c0000003000    | 0000000000     |   |                |   |                   | 81c00     | 0000400000000  | 000000000000000000000000000000000000000 | 28a0 |                |   |                |
| > ₩ EXMEM_o[106:0]      | 4000000c0000  | 40000000a0000    | 0001000000     |   |                |   |                   |           | 40000000c00000 | 0012000000004                           |      |                |   |                |
| ∨ ₩ MEMWB_o[70:0]       | XXXXXXXXXX000 | XXXXXXXX000000e2 |                |   |                |   | XXXXXXXX000000103 |           |                |   |      |                |   |                |
| 18 [70]                 | 1             |                  |                |   |                |   |                   |           |                |   |      |                |   |                |
| 18 [69]                 | 0             |                  |                |   |                |   |                   |           |                |   |      |                |   |                |

#### Picture:

| CO_P5_test_data1   | CO_P5_test_data2  |
|--|---|
| ALUSrc = 0 ALUOp = 010 RegDst = 1 MemWrite = 0 MemRead = 0 Branch = 0 MemtoReg[0] = 0 RegWrite = 1 | ALUSrc = 1<br>ALUOp = 011<br>RegDst = 0<br>MemWrite = 0<br>MemRead = 0<br>Branch = 0<br>MemtoReg[0] = 0<br>RegWrite = 1 |

### 4. Problems you met and solutions:

I should have been more careful because I encountered problems such as forgetting variable names and mistakenly pulling the wrong wire on the pipeline.

## 5. Summary:

After completing the homework, I have become more familiar with the Pipeline CPU and the path that instructions follow.