Computer Organization

1. The input fields of each pipeline register:

IF/ID:

input : PC_add1, instr

ID/EX:

input : RegWrite, MemtoReg, Branch, MemRead, MemWrite, RegDst, ALUOp, ALUSrc, PC_add1, ReadData1, ReadData2, signextend, instr[20:16], instr[15:11]

EX/MEM:

input: RegWrite, MemtoReg, Branch, MemRead, MemWrite, ALU_result, zero, ReadData2, branch_address, write_address

MEM/WB:

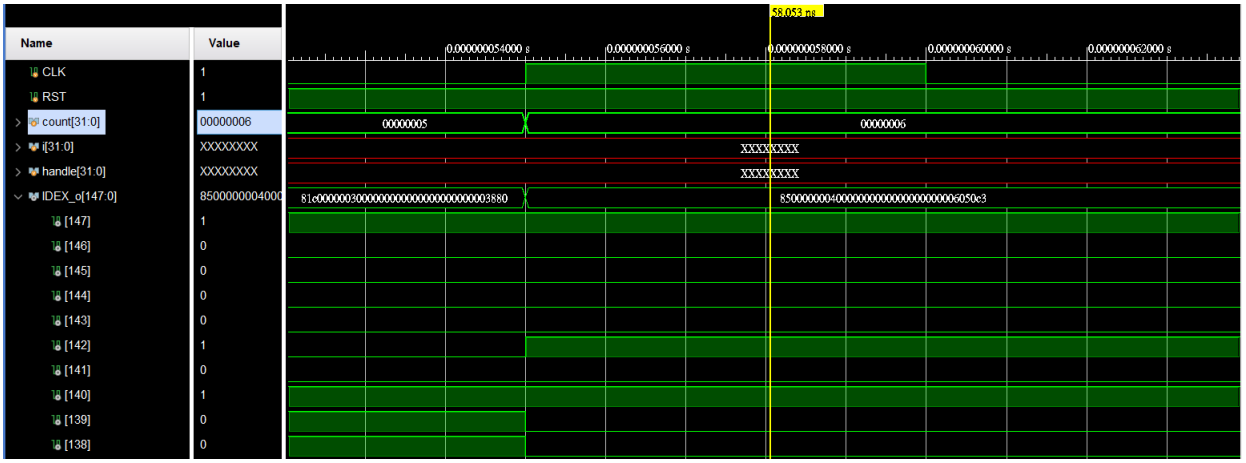
input: RegWrite, MemtoReg, Readdata, ALU_result, write_address

2. Compared with lab4, the extra modules:

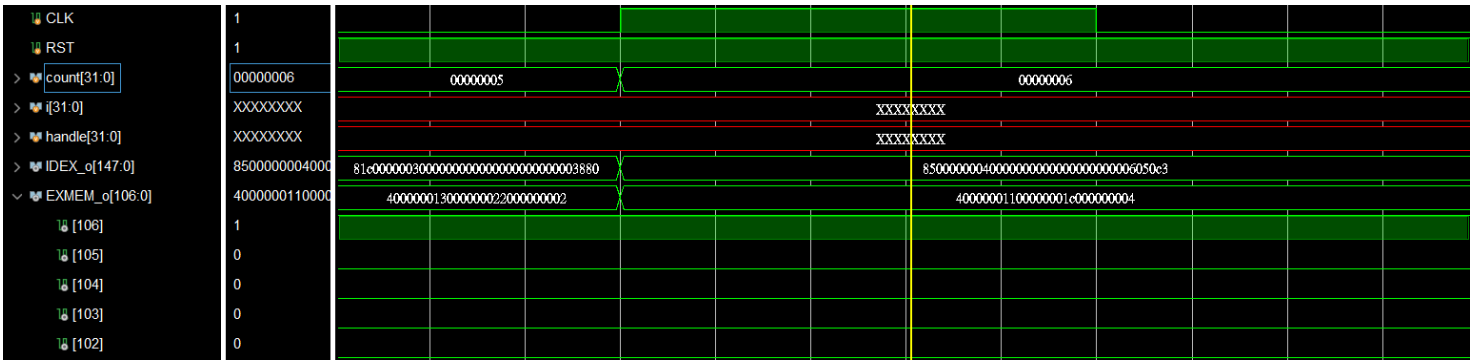
Pipeline_Reg.v : To hold information produced in the previous cycle.

3. Explain your control signals in sixth cycle (both test patterns CO_P5_test_data1 and CO_P5_test_data2 are needed):

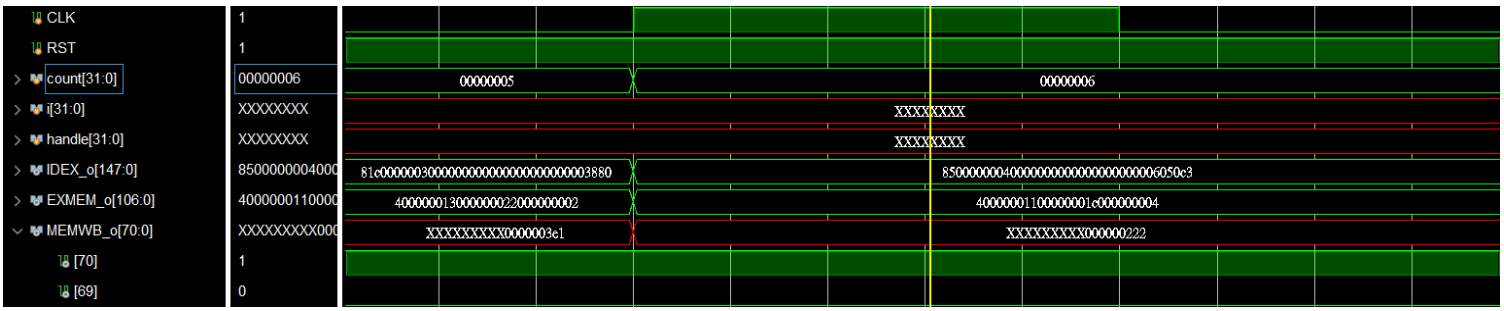
data1:



在ID/EX這個pipeline中，[138]是ALUSrc，[141:139]是ALUOp，[142]是RegDst。

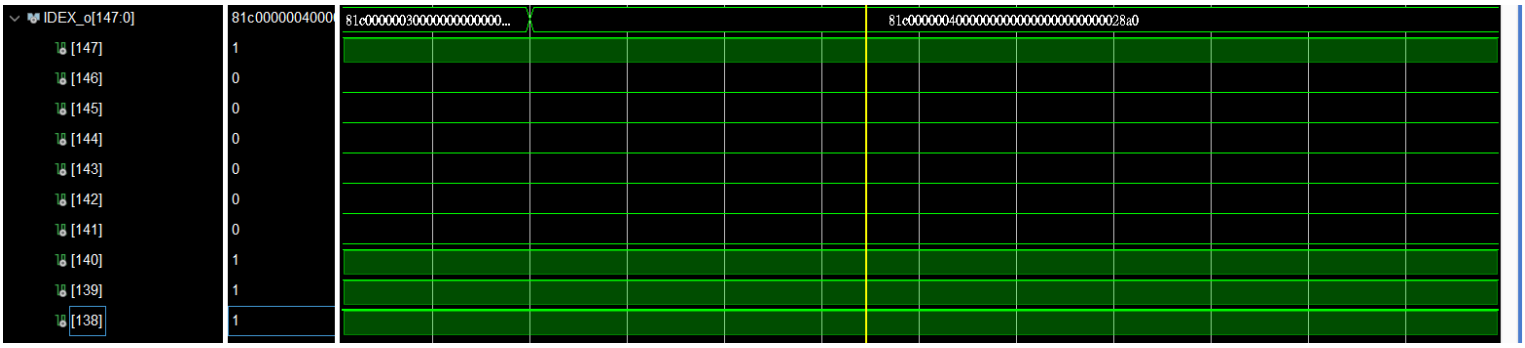


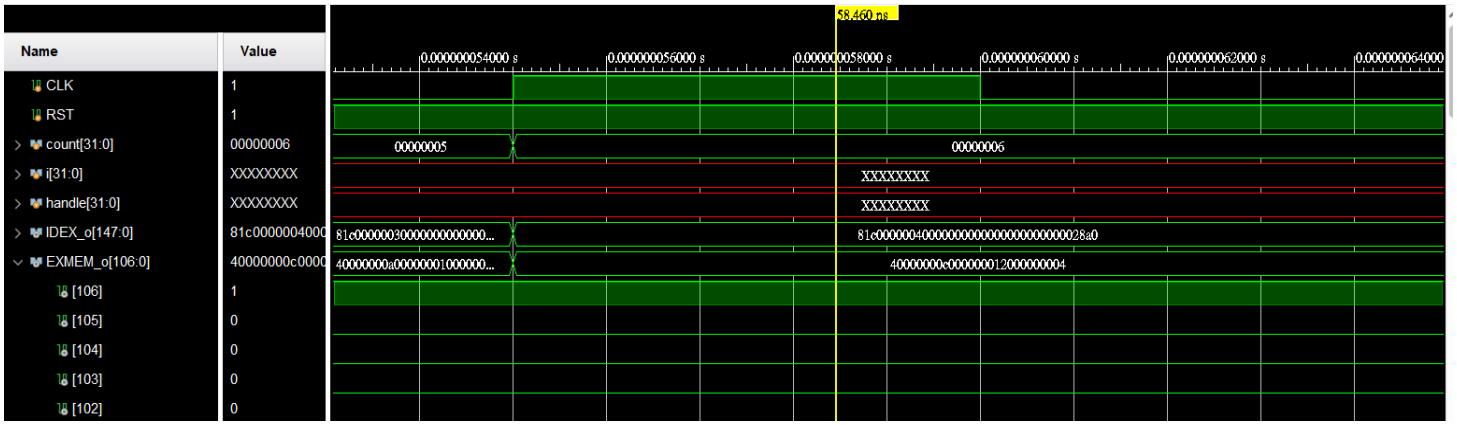
在EX/MEM這個pipeline中，[102]是MemWrite，[103]是MemRead，[104]是Branch。

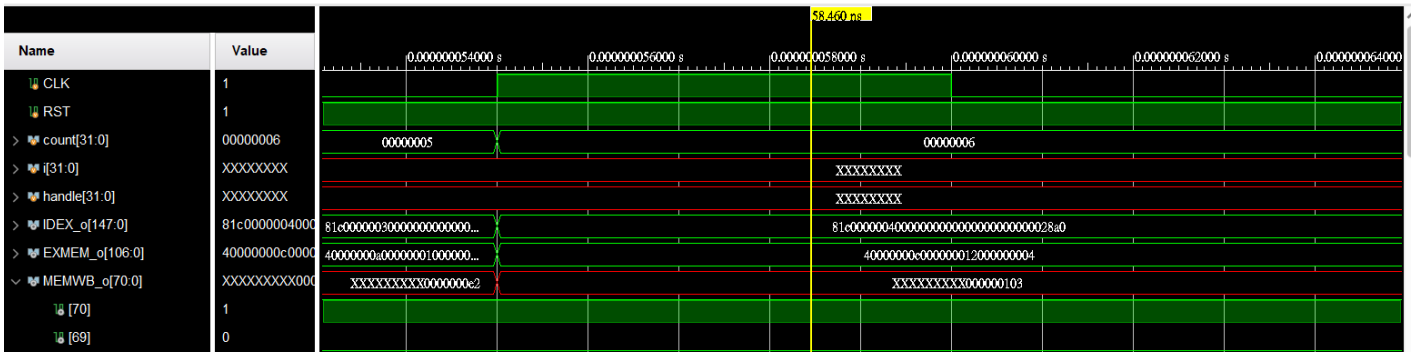


在MEM/WB這個pipeline中，[69]是MemtoReg[0](在本次作業中MemtoReg[1]這個bit並沒有用到，因此實作部分中不採用)，[70]是RegWrite。

data2:(資料如data1所示)







Picture:

CO_P5_test_data1	**CO_P5_test_data2**
ALUSrc = 0 *ALUOp = 010* *RegDst = 1* *MemWrite = 0* *MemRead = 0* *Branch = 0* *MemtoReg[0] = 0* *RegWrite = 1*	*ALUSrc = 1* *ALUOp = 011* *RegDst = 0* *MemWrite = 0* *MemRead = 0* *Branch = 0* *MemtoReg[0] = 0* *RegWrite = 1*

4. Problems you met and solutions:

I should have been more careful because I encountered problems such as forgetting variable names and mistakenly pulling the wrong wire on the pipeline.

5. Summary:

After completing the homework, I have become more familiar with the Pipeline CPU and the path that instructions follow.