
VE311 Electronic Circuit Homework 5

Due: Jul 2th 11:59a.m.

Note:

- 1) Please use A4 size paper or page.*
- 2) Please clearly state out your final result for each question.*
- 3) Please attach the screenshot of Pspice simulation result if necessary.*

Peilin, a talented young engineer, has recently joined Blue Tiger Electronics. Peilin's demanding supervisor, Xuyang, is determined to outshine their rival company, Red Tiger Technologies, and secure a prestigious government contract that will ensure Blue Tiger's dominance in the industry. To achieve this, Xuyang assigns Peilin a series of challenging tasks to demonstrate Blue Tiger's superior MOSFET technology.

Question 1. MOSFET DC Biasing

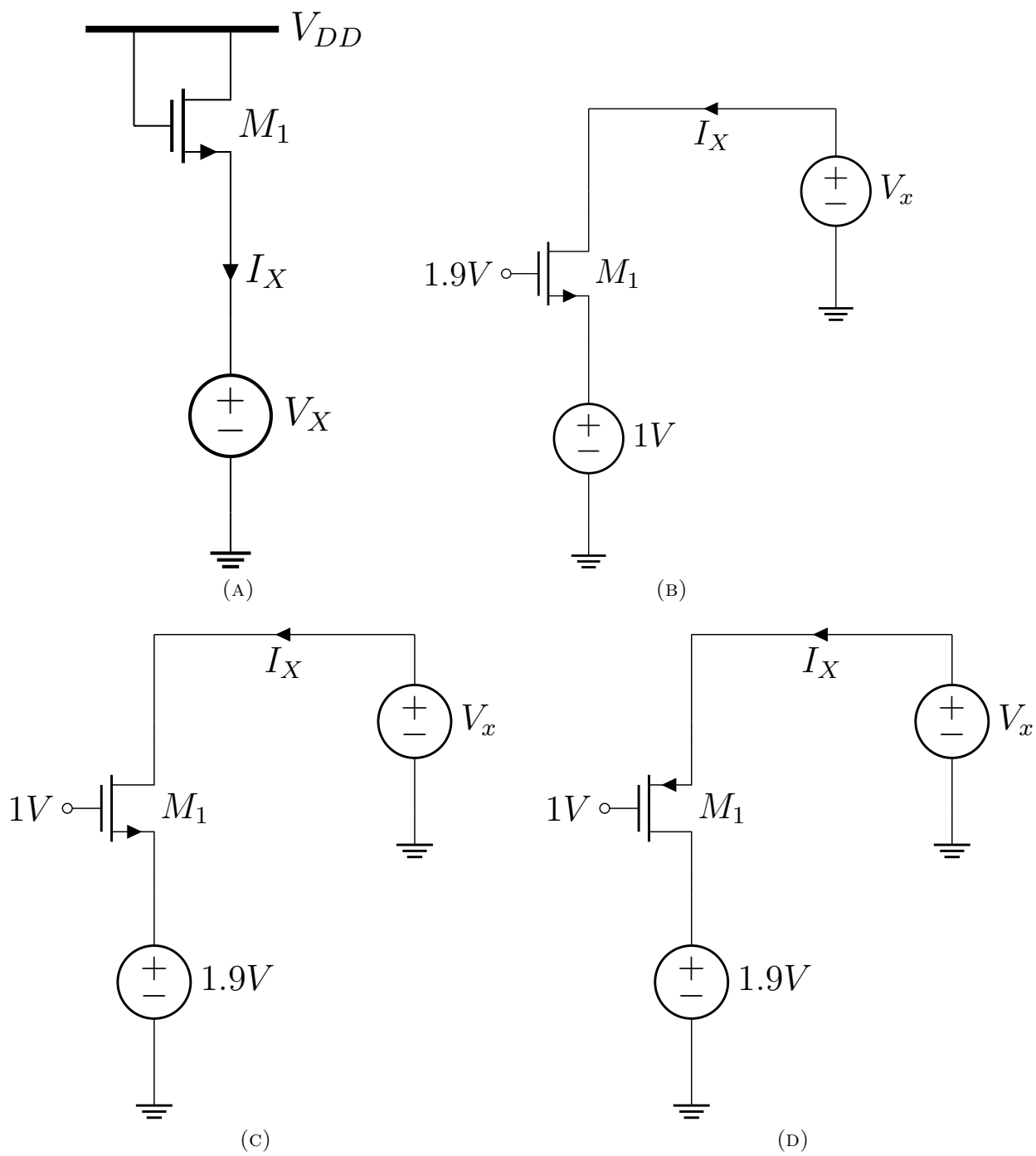
Peilin meticulously works through the drain current equations shown below, knowing that his performance on this task is critical for the company's success. Don't consider channel-length modulation and body effect. Assuming $\mu_n = 350 \times 10^{-4} \text{m}^2/\text{V}/\text{s}$, $\mu_p = 350 \times 10^{-4} \text{m}^2/\text{V}/\text{s}$, $V_{TH} = 0.7\text{V}$ (NMOS), $V_{TH} = -0.8\text{V}$ (PMOS), $W_{drawn}/L_{drawn} = 20\mu\text{m}/2\mu\text{m}$, $t_{ox} = 9 \times 10^{-9}\text{m}$, $L_D = 0.08\mu\text{m}$, sketch I_X of M_1 as a function of V_X increasing from 0V to $V_{DD} = 5\text{V}$.

$$(1) \quad I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \text{ (NMOS in triode region)}$$

$$(2) \quad I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_{TH})^2 \text{ (NMOS in saturation region)}$$

$$(3) \quad I_D = \mu_p C_{ox} \frac{W}{L_{eff}} \left[(V_{SG} - |V_{TH}|) V_{SD} - \frac{1}{2} V_{SD}^2 \right] \text{ (PMOS in triode region)}$$

$$(4) \quad I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L_{eff}} (V_{SG} - |V_{TH}|)^2 \text{ (PMOS in saturation region)}$$



Question 2. Combination of MOSFET

Next, Xuyang assigns Peilin the task of analyzing a complex circuit involving a combination of MOSFETs. For the circuit below, he needs to determine the labeled node voltages. The NMOS transistor has $V_{TH} = 0.9V$, $k_n = \mu_n C_{ox}(W/L) = 1.5mA/V^2$.

