UM-SJTU Joint Institute

ELECTRONIC CIRCUIT LABORATORY

(ECE3110J)

Laboratory Report

Lab 4

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1 Exercise 2.1.1

The obtained values are shown below, simulated by Proteus.

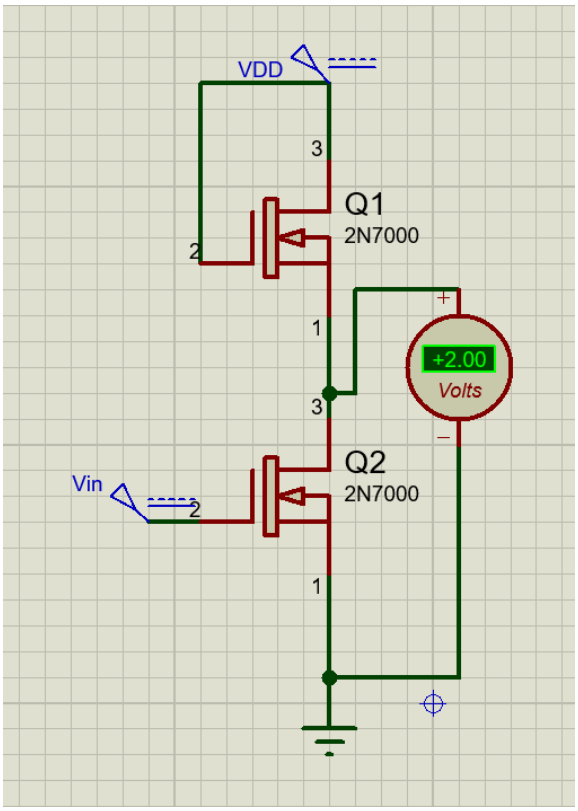

Figure 1: Circuit of 2.1.1

The resulting graph of V_{OUT} vs. V_{IN} is shown in Figure 2. From the curve, when $V_{IN} = 3V$, $V_{OUT} = 2V$ and when $V_{IN} = 3.01V$, $V_{OUT} = 1.99V$. Thus, the slope is:

$$\left|\frac{1.99 - 2}{3.01 - 3}\right| = 1$$

As we set $V_{IN} = 3V$, $A_V = -1.5$. Two NMOS are both on and in the saturation region. The dc sweep from 0v to 3v is shown below.

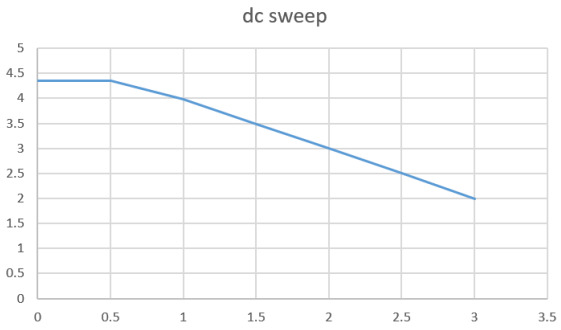

Figure 2: DC sweep of 2.1.1

2 Exercise 2.1.2

In this part of simulation, when $V_{IN} = 1.50V$, $V_{OUT} = 3.24V$ and when $V_{IN} = 1.52V$, $V_{OUT} = 3.21V$. Thus, the gain equals to:

$$\left|\frac{3.24 - 3.21}{1.50 - 1.52}\right| = 1.5$$

NMOS are in the saturation region. Comparing the value of A_V with that in 2.1.1, we can conclude it does not double.

This is because therotically:

$$-g_{m1}\left(\frac{1}{g_{m2} \parallel r_{01} \parallel r_{02} \parallel \frac{1}{g_{mb2}}}\right) \neq -(g_{m1} + g_{m3})\left(\frac{1}{g_{m2} \parallel r_{01} \parallel r_{02} \parallel r_{03} \parallel \frac{1}{g_{mb2}}}\right)$$

Hence, the relation between two A_Vs is not double or half.

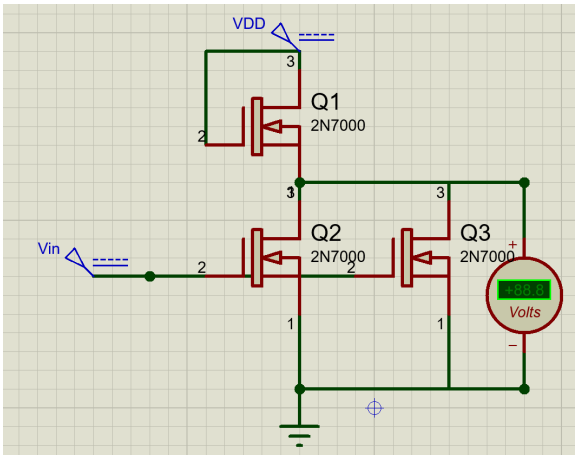

Figure 3: Circuit of 2.1.2

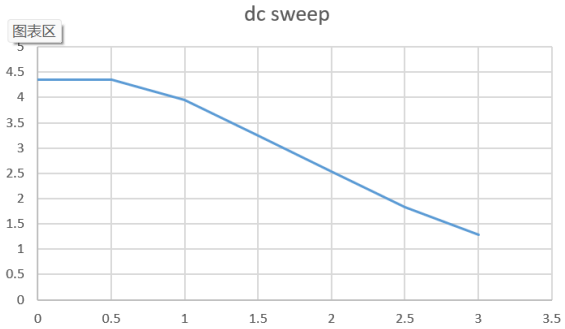

Figure 4: DC sweep of 2.1.2

3 Exercise 2.1.3

According to the experiment's results, $|A_V| = 0.91$ very close to 1.

The experimental result is shown below:

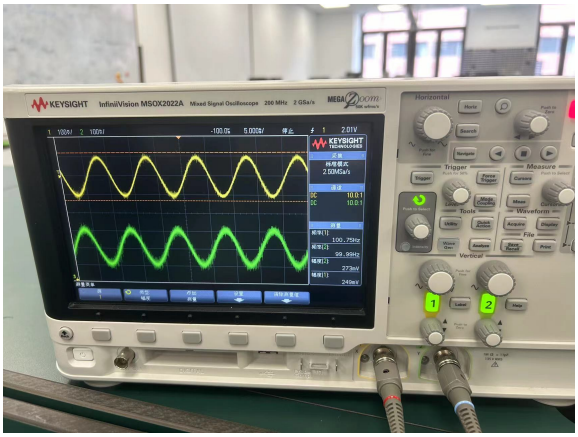

Figure 5: Lab result of 2.1.3

4 Exercise 2.2.1

In this part, according to the simulation below:

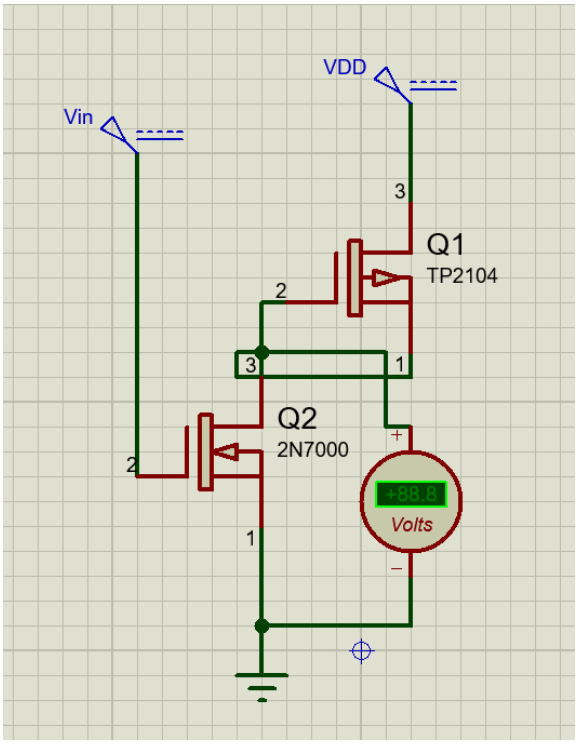

Figure 6: Circuit of 2.2.1

The resulting graph of V_{OUT} vs. V_{IN} is shown in Figure 9. From the curve, when $V_{IN} = 1.60V$, $V_{OUT} = 4.24V$ and when $V_{IN} = 1.70V$, $V_{OUT} = 4.21V$. Thus, the gain is:

$$\frac{4.24 - 4.21}{1.60 - 1.70} = 0.3$$

The dc sweep from 0v to 3v is shown below.

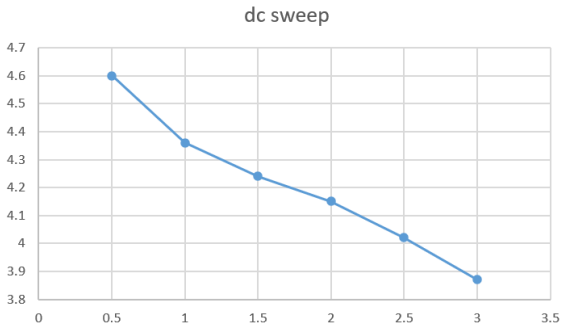

Figure 7: DC sweep of 2.2.1

5 Exercise 2.2.2

When $V_{IN} = 0.80V$, $V_{OUT} = 4.51V$ and when $V_{IN} = 0.85V$, $V_{OUT} = 4.48V$. Thus, the gain equals to -0.6. Reason: Switching from a single PMOS diode connected load with a single NMOS driver to two parallel PMOS diode connected loads in a common source amplifier results in reduced voltage gain.

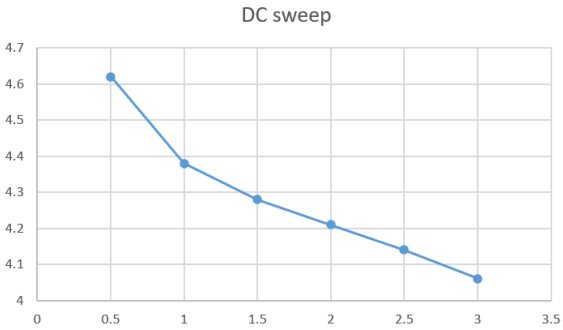

Figure 8: Simulation of 2.2.2

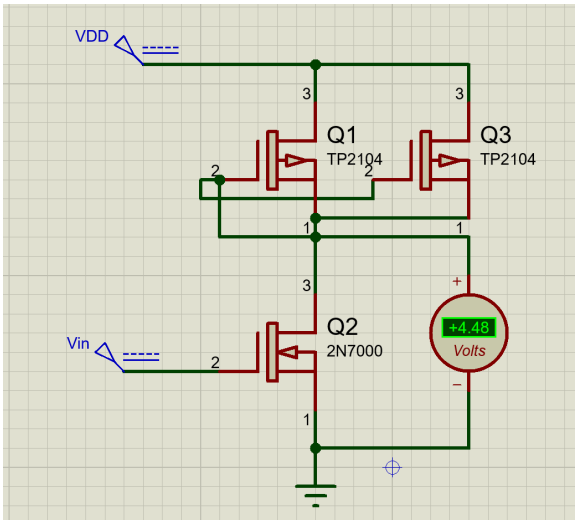

Figure 9: Circuit of 2.2.2

6 Exercise 4.2.3

According to the experiment's results, $|A_V| = 0.39$ very close to 0.3.

The experimental result is shown below:

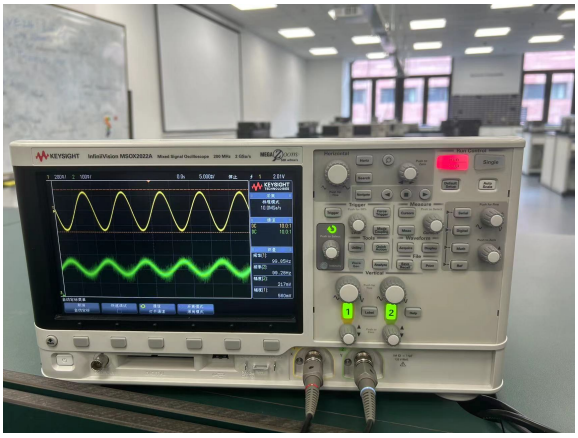

Figure 10: Lab result of 2.2.3

7 Error Analysis and Discussion

Discrepancies between simulated and experimental results revealed challenges in electronic circuit design. Differences in component characteristics, measurement inaccuracies, and environmental factors such as temperature variations and electromagnetic interference significantly influenced circuit performance.

8 Conclusion

Despite challenges, the experiments provided valuable insights into amplifier behavior using MOSFET configurations. They highlighted the importance of integrating theoretical knowledge with hands-on experience to optimize circuit design and measurement methodologies.