Course: **Electronic Circuits, VE 311, Summer 2023** **Final**

上　海　交　通　大　学　试　卷

2022 – 2023 Academic Year (Summer Term)

Name (Hanzi) ______________________ Name (Pinyin) ______________________

Student No. ______________________ Class No. ______________________

You have **100 minutes** to complete this Final. Please write your answers in this booklet. Remember to write neatly and clearly, so your answers can be fully understood. Make sure that you explain your reasoning in as detailed a manner as possible.

- You **may not** use your electronic devices other than your calculator.
- **One double-sided** cheating-sheet can be used.
- Time is tight. If you don't know how to answer, come back to the question later.

Pledge of Honor

The University of Michigan –Shanghai Jiao Tong University Joint Institute trusts its students to participate in examinations in an honorable and respectful manner, following a spirit of fairness and equality. Cheating, seeking unfair advantage, and disturbing the safe and harmonious environment of examinations are contrary to the ethical principles of students of the Joint Institute. The letter and spirit of the Honor Code shall guide the behavior of students, faculty and all members of the Joint Institute. Therefore, I hereby declare that

(i) I will neither give nor receive unauthorized aid during the present examination, nor will I conceal any violations of the Honor Code by others or myself.

(ii) I confirm that I have read and understood the rules and procedures for the examination set out by SJTU. I will follow them to the best of my ability.

(iii) I understand that violating the rules and procedures for examinations or the Honor Code will lead to administrative and/or academic sanctions.

Date: ______________

Signature: ______________

Note: The value of each question is approximately proportional to the number of minutes indicated in the bracket.

Exercise	Points	Grader's Signature
1		
2		
3		
Total		

1 Job Interview (15 minutes)

Welcome to Blue Tiger Analog! We are thrilled to offer employment opportunities to individuals who have demonstrated a solid understanding of our VE 311 course. As you prepare to embark on your journey as an analog circuit designer, we have prepared a set of engaging questions to help you practice and assess your grasp of the fundamentals. Get ready to put your knowledge to the test and showcase your skills.

1. (Easy) A 13 dBm 10 GHz signal is fed into a device with an input impedance of 50 Ω, what is V_{rms}.

2. (Easy) For the circuit in Fig. 1, ignore channel length modulation and body effect. V_{TH} = 0.8 V, $\mu_n C_{ox}\frac{W}{L} = 5mA/V$.

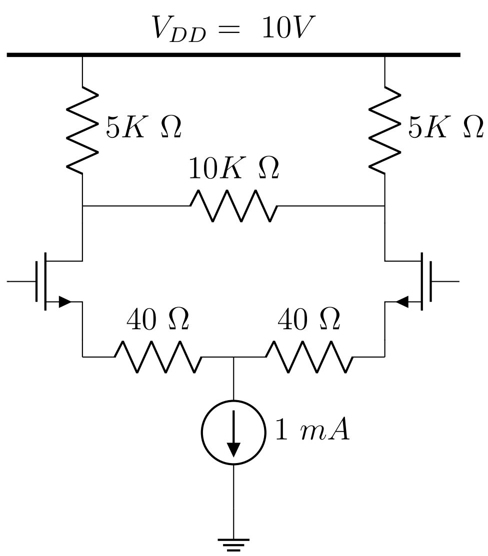

Figure 1: A differential pair

(1) Find the location of the inputs and the outputs for it to work as a voltage amplifier.

(2) Draw the half-circuit equivalent of a common mode input.

(3) Draw the half-circuit equivalent of a differential mode input.

(4) Find the differential gain of the amplifier.

3. (Medium) For the circuit in Fig. 2, the gain equals to G = -5, find the output impedance of the circuit.

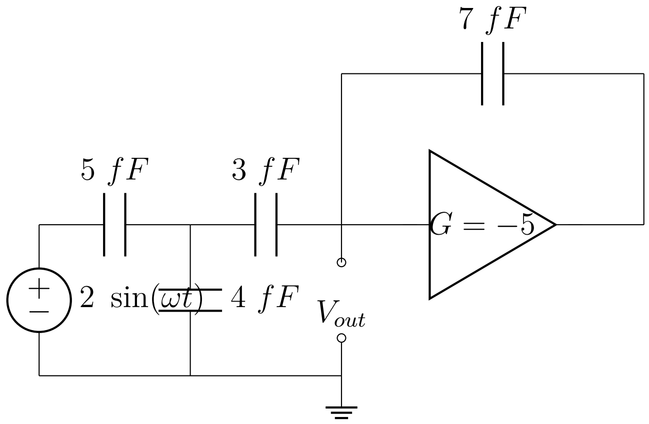

Figure 2: Miller

Question 1 Answer Sheet Page 1

Question 1 Answer Sheet Page 2

2 Current Mirror (70 minutes)

Blue Tiger Analog has expanded into bias circuit design, and you have been entrusted with leading the program. While the BJTs and mosfets are excellent, the power supply is subpar. To create an exceptional current mirror, you decide to start with the ideal current mirror learned in VE 311.

1. (Easy) For a current mirror circuit, $I_{REF} = 100\mu A$. We are going to ignore Early effect, i.e. V_A is infinite, and choose a $V_T = 26mV$ and $I_{s1} = I_{s2} = 15fA$.

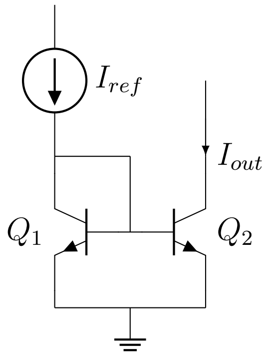

Figure 3: Simplest current mirror

(a) For the first part, you have told your boss with confidence to ignore I_B, because that is very small as compare to the collector current. what is the voltage V_{BE}?

(b) There is an output current flowing into Q_2 collector, what is the current assuming Q_2 is saturation?

2. (Easy) Although the current available appears too large for your amplifiers, it's the only type of BJT currently accessible to you. In order to mitigate this issue, you opt to employ resistance to decrease the current magnitude. In a stroke of rediscovery, you stumble upon a novel current mirror, famously known as the "Widlar mirror," named after the legendary semiconductor genius and notorious alcoholic, Robert Widlar. Widlar, while at Fairchild Semiconductor, invented the remarkable μ A 702 op-amp. The schematic of the design in shown in Fig. 4.

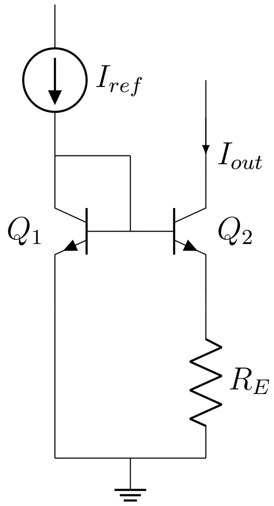

Figure 4: A widlar current mirror

Calculate V_{BE2} and R_E so that the output current is reduced to $\frac{1}{4}$ of its original amount.

Question 2 Answer Sheet Page 1

3. (Medium) You are now provided with another sets of BJTs, and part of the datasheet information is missing. You have measured that the $\beta_1 = \beta_2 = 150$, $V_T = 26\ mV$, $I_{s1} = I_{s2}$ but not equal to the previous 15 fA value. $V_{BE1} = 0.7\ V$, the R_E resistor is also chosen differently. and When $I_{ref} = 0.7mA$ and $V_{C2} = 1V$, $I_o = 25\mu A$.

(a) What is the definition of V_A (The name, the physical meaning (What happens at this particular voltage), the physics behind it, and the mathematical formulation.) and how do you measure it?

(b) Let's say $V_A = 100V$. What will the I_{out} be when $V_{C2} = 4V$?, if I_{out} cannot be determined, state why.

One advantage of Widlar source is it is less sensitive to the variation of the supply voltage. To make our life easier, consider the MOSFET version of Wildar below.

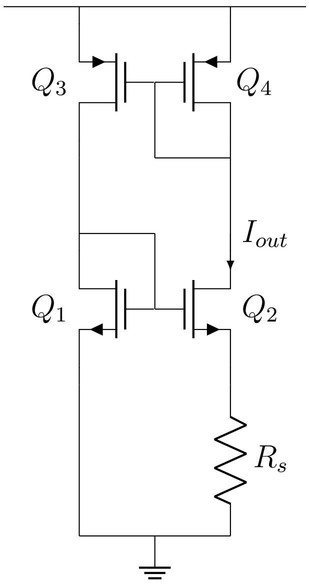

Figure 5: A blue-tiger mirror. Power supply rejection ratio is a term widely used to describe the capability of an electronic circuit to suppress any power supply variations to its output signal.

4. (Medium) In this problem, $V_{DD} = 5\ V$, $U_nC_{ox} = 341\ \mu A/V^2$, $U_pC_{ox} = 120\ \mu A/V^2$, $V_{th} = 0.7\ V$. Ignore channel length modulation. Ignore body effect. The PMOS transistors have equal sizes of $\frac{W}{L} = 30$. The length of the nmos transistors are the same, while the $\frac{W}{L}$ of transistor $Q_1 = 10$. The resistance $R_s = 100\ \Omega$. I_{out} is the current flowing through the resistor (or the right branch).

(a) Assume all mosfet are in saturation, Express I_{out} in terms of circuit parameters. Hint: This is suppose to be not sensitive (or unrelated) to V_{DD}.

(b) What is the size of Q_2 so that it produces a current of 5 mA.

(c) Check whether all transistors are indeed in saturation.

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5. (Hard) The design you implemented proves to be an unprecedented triumph, leaving your business competitor, Red-Lion Analog, green with envy. However, they are unable to directly replicate your design. In an overconfident and rather lackluster display of their VE 311 skills, the boss of Red-Lion Analog conceives the design depicted in Figure 6. Sensing the impending disaster, you delve into their idea and feel compelled to offer a warning before they squander a significant fortune.

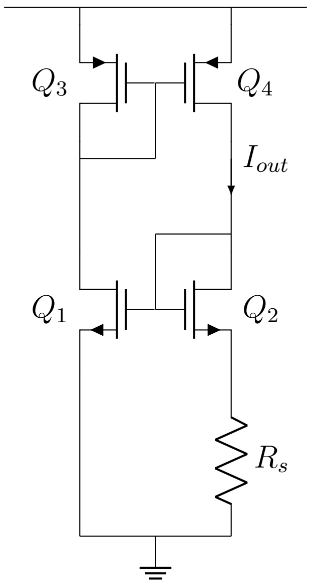

Figure 6: A Red-lion Mirror

(a) In the blue-tiger design (widlar), how will the Q_2 drain voltage change when you start with increasing the voltage at the gate of Q_3, why? Is the a positive feedback or negative feedback?

(b) In the red lion design, how will the Q_2 drain voltage change when you start with increasing the voltage at the gate of Q_4, why? Is it a positive feedback or negative feedback design?

(c) Find the expression of the loop gain of the blue-tiger and the red-lion using transistor small signal parameters such as g_m, r_s, etc. for example, in blue-tiger design, the loop gain can be calculated by breaking the Q3 gate connection, and then find out how much does the drain voltage at Q_4 changes as Q3 gate changes by ΔV, which design gives you a loop gain that can be used for a stable circuit?

Question 2 Answer Sheet Page 3

3 Frequency Estimation (15 minutes)

Overwhelmed with shame for their copycat behavior, the Red-Lion team finds themselves profoundly impressed by your magnanimity and your expertise in circuit design, particularly in VE 311. Recognizing the opportunity for growth and redemption, they humbly offer their services as your collaborator, ready to join forces in conquering new challenges in the realm of circuit design.

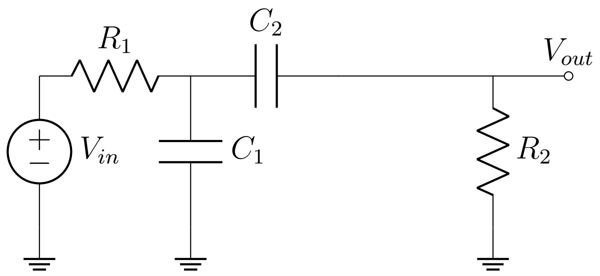

Figure 7: A π network filter

1. (Easy) In Fig. 7, $L_1 = 10$ nH, $C_1 = 120$ fF, $C_2 = 150$ fF. $R_1 = 40\ \Omega$ and $R_2 = 80\ \Omega$.

   (a) Find the 2nd-order transfer function using the time constant method and the lowest cut-off frequency.

   (b) Sketch the pole-zero constellation in the s-plane.

   (c) Sketch the magnitude and phase Bode plots

Question 3 Answer Sheet