



Lecture 1: Introduction

ECE3110J, Electronic Circuits

Xuyang Lu
2024 Summer



上海交通大学
SHANGHAI JIAO TONG UNIVERSITY

Logistics

Instructor: Xuyang Lu

- Princeton University, ECE, Ph.D
- Rice University, ECE, B.S

Teaching Assistant:

- Tianrui Dang
- Yuheng Wang
- Jiale Chu
- Anlin Ma
- Kezhi Li

Lab Manager: Yu Sun



Lecture Hours



- Mondays: 18:20-20:00 @ DXY415
- Wednesdays: 18:20-20:00 @ DXY415
- Friday: 14:00-15:40 (Weeks 2, 4, 6) @ DXY415

Recitation and TA Office Hours:



- 15:40-16:40 on Fridays @ DXY415

Instructor Office Hr:

- By appointment via Feishu.

Grading Policy

Attendance:

In-class participation recommended.

Grading:

- ① Problem sets and Lab reports (18%, 9 scheduled, subject to change)
 - Will be posted on Canvas on Wednesdays and due the next Tuesday at 11:59 am (Noon, not evening).
- ② Lab reports (15%) (5 scheduled in **Week 3, 5, 7, 9, 11**)
- ③ Midterm Exam (33%)
- ④ Final Exam (33%)
- ⑤ Teaching Evaluation (1%)

Late and Regrade Policies



Late Policies:

- Late submissions are accepted for the next 24 hours with 25% late penalty.
- Sets turned in more than 24 hours late are counted zero but will be graded.

Regrade Policy:

- Students have one week to submit a request for re-grade.
- Late regrade will not be accepted.

Final Letter Grade Policy



Letter grades are assigned based on final course numerical grades.

- > 90.0% will always be some sort of A (A-, A, or A+)
- > 80.0% will always be some sort of B (B-, B, or B+) or better
- > 70.0% will always be some sort of C (C-, C, or C+)

If you all did not do well, the course will be curved up at a median of B.

Collaboration and the Honor Code



- Direct copying of answers from other students or online solutions is professionally unethical. This is considered plagiarism and is not allowed.
- Do not copy others lab report.

Slide Improvement and Vectorization Program



- ① In addition to our TAs, special Thanks to students from last year (In alphabetical order) participated in “beamerizing” and “vectorizing” Power-point slides for better teaching quality.
 - 李健恺, 王嘉俊, 王禹珩, 谢天晗, 熊振翔
- ② We teach/hire student contributors for slide vectorization and quality improvement.
- ③ We hire student to create handouts and interactive textbooks for this course.
- ④ Talk to me if you want to learn how to make slides with beamer.

Tentative Course Schedule

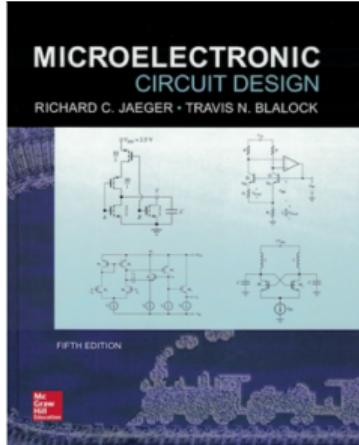
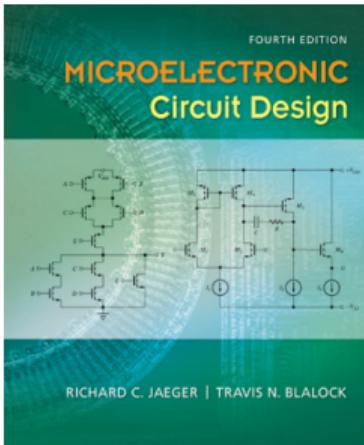


	Apr	May			Jun				Jul					Aug				Sep		
Monday	29	6	13	20	27	3	10	17	24	1	8	15	22	29	5	12	19	26	2	9
Tuesday	30	7	14	21	28*	4*	11*	18*	25	2*	9*	16*	23*	30*	6	13	20	27	3	10
Wednesday	1	8	15	22	29	5	12	19	26	3	10	17	24	31	7	14	21	28	4	11
Thursday	2	9	16	23	30	6	13	20	27	4	11	18	25	1	8	15	22	29	5	12
Friday	3	10	17	24	31	7	14	21	28	5	12	19	26	2	9	16	23	30	6	13
Saturday	4	11	18	25	1	8	15	22	29	6	13	20	27	3	10	17	24	31	7	14
Sunday	5	12	19	26	2	9	16	23	30	7	14	21	28	4	11	18	25	1	8	15
JI Week			1	2	3	4	5	6	7	8	9	10	11	12	13					
JI Semester	Spr. Break		Summer Term											Summer Break						

- Yellow: Lectures
- Blue: Midterm and final exams

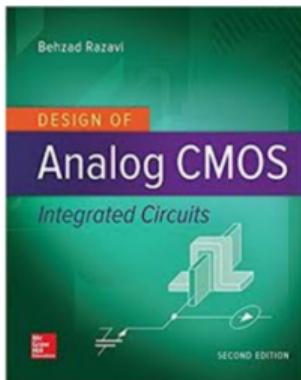
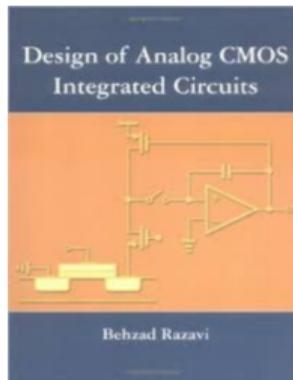
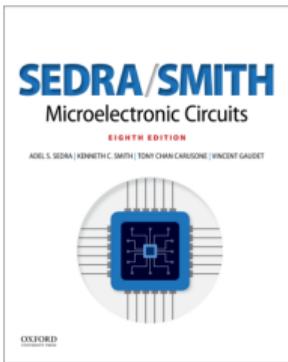
- Red: Lab report due dates
- *: Assignment due dates

Textbooks and Recommended Readings



- Richard C. Jaeger, Travis N. Blalock. *Microelectronic Circuit Design*

Textbooks and Recommended Readings



- Adel S. Sedra et.al.
Microelectronic Circuits
- Behzad Razavi *Design of Analog CMOS Integrated Circuits*

Topics



- Review: KCL, KVL, Thevenin, $H(s)$, Laplace, Bode plots
- Diode and Diode Circuits
- BJT
- BJT Circuits
- MOSFET
- MOSFET Single Stage Amplifiers
- DC, AC, and frequency response
- MOSFET Differential Amplifiers
- Op-amp circuits and filter design

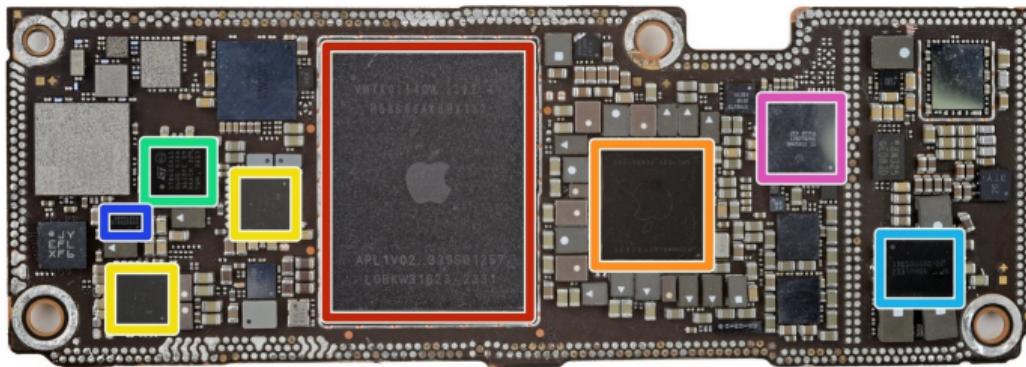
iPhone 15 Teardown



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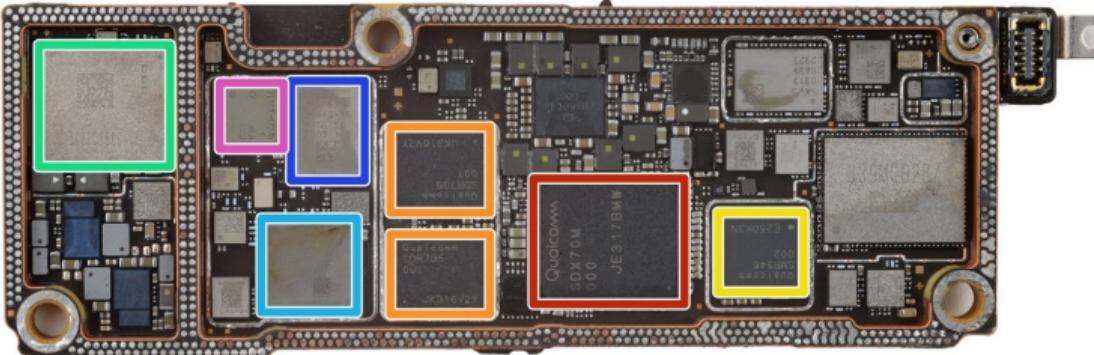
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iPhone 15 Teardown (Main PCB Side)



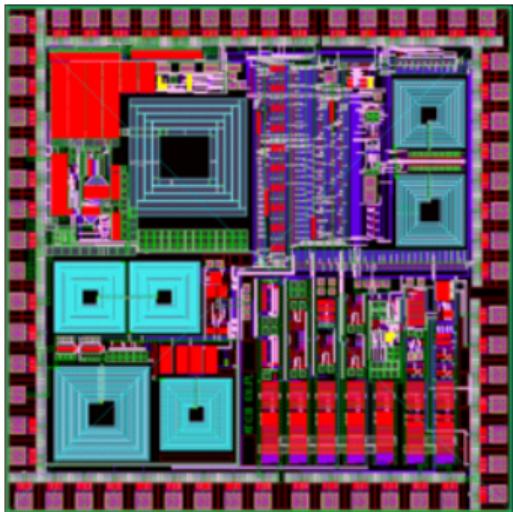
- A17 Pro + SK hynix
- Apple APL109A PM
- STM STCPM1A3 PM
- STM STB605A11 PM
- 338S00946 PM
- 338S00616 PM
- TI SN2012017 battery charger

iPhone 15 Teardown (RF Side 1 - Connectivity)



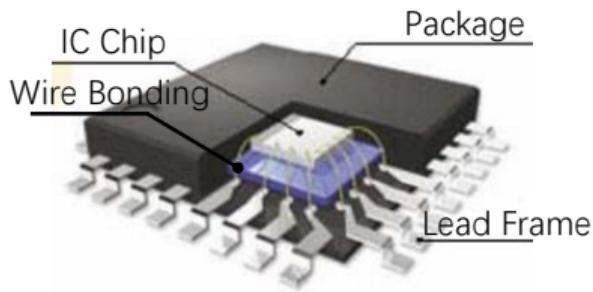
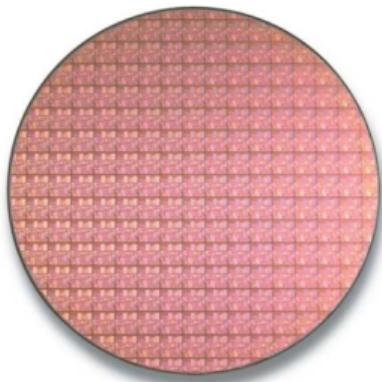
- Qualcomm SDX70M modem
- SDR735 TRx
- SMR546 TRx
- Apple WiFi & Bluetooth
- Broadcom AFEM-8234 FE
- Skyworks SKY58440-11 FE
- Qorvo QM76305 FE

Related Courses Offered at JI



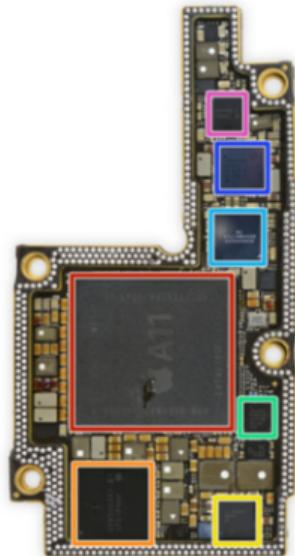
- VE215: Introduction to Circuits
 - **VE311: Electronic Circuits**
 - VE312: Digital Integrated Circuits
 - **VE411/611: Microwave Circuits I**
 - VE413: Monolithic Amplifier Circuits
 - **VE427: VLSI Design I**

Related Courses Offered at JI: Semiconductor Devices



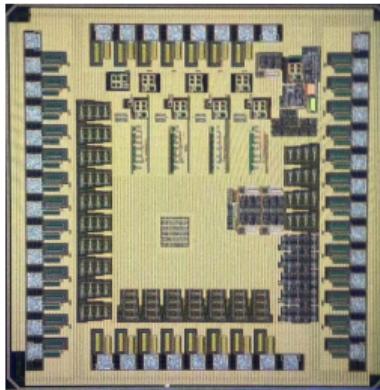
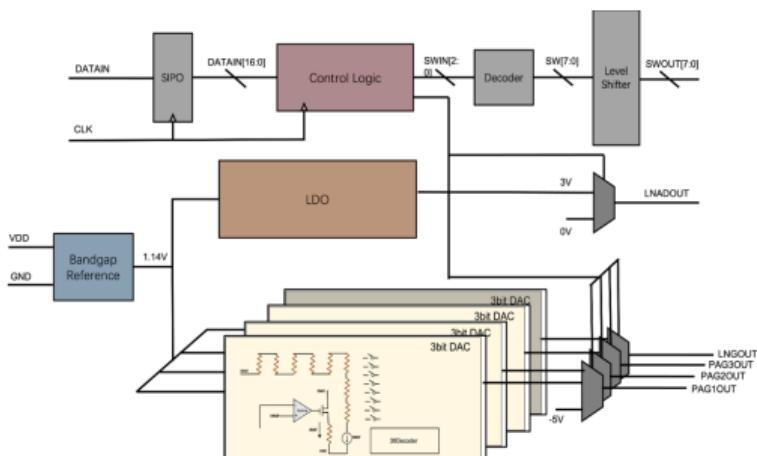
- VE320: Introduction to Semiconductor Devices
- VE421: Properties of Transistors

IC Designs are Not Far Away from Us



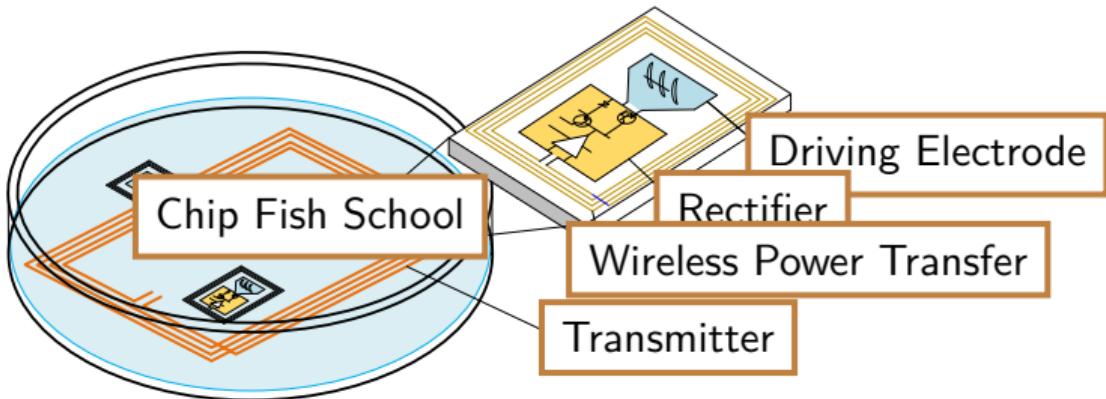
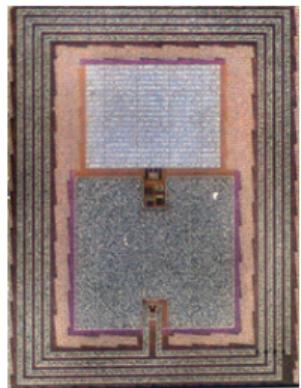
- Apple APL1W72 A11 Bionic SoC layered over SK Hynix 3 GB LPDDR 4x RAM
- Apple 338S00341-B1 power management IC
- TI78AVZ81 battery charger
- NXP 1612A1-Likely an iteration of the 1610 tristar IC
- Apple 338S00248 audio codec
- Facial Recognition Driver STB600BO
- Apple 338S00306 power management IC

Students Tapeout: Power Electronics



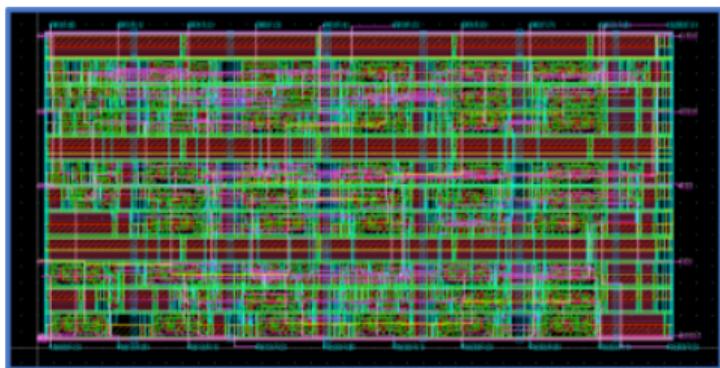
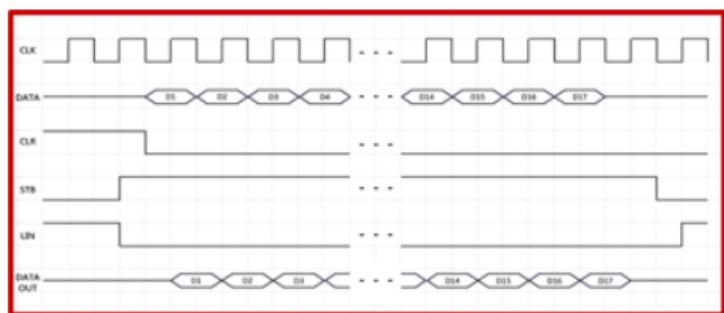
- Runqin Cai, a JI undergraduate student, now a Ph.D student in my group.
- He designed single-handedly a power management IC in his junior-year.

Students Tapeout: Power Electronics



- In his first Ph.D. year, he looked into parity-time symmetry method and designed a wirelessly powered chip that can swim in water.

IC design Example



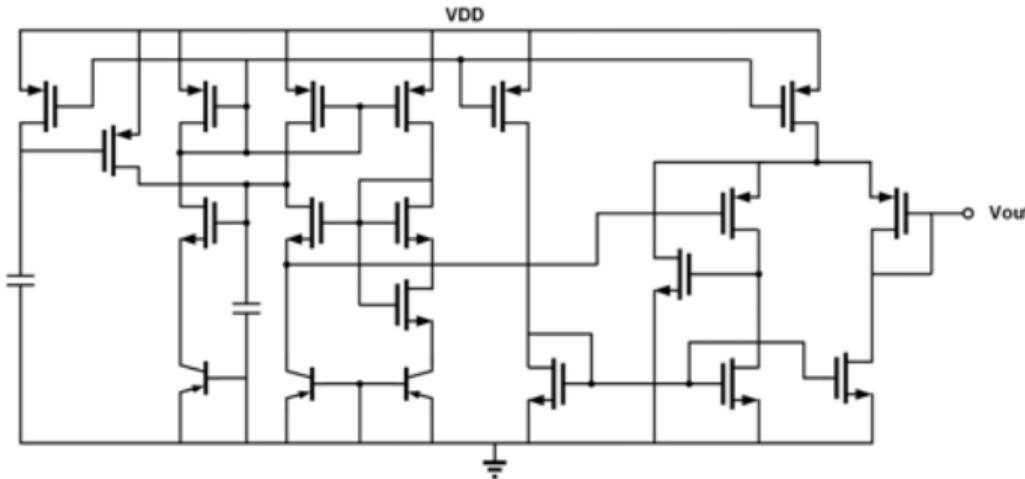
- Digital Circuit design (Verilog to circuit, discussed in 427)

IC Design Example

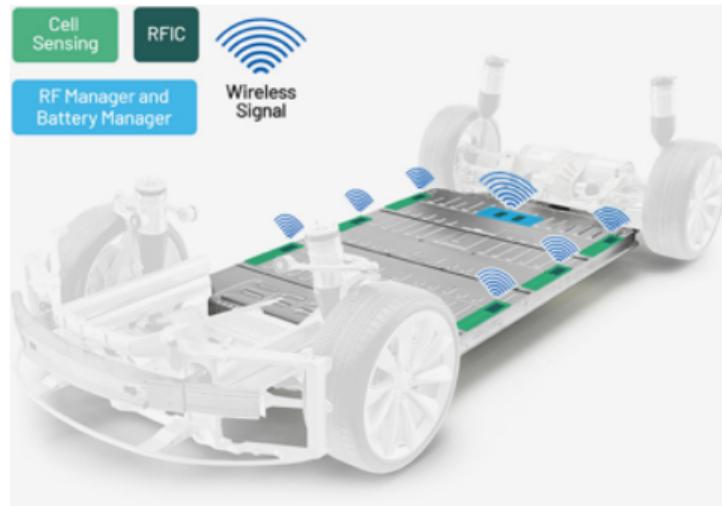
Analog design using cadence,
covered in 413 and 411.

Contains

- Bandgap reference
- LDO circuits
- 3-bit DAC

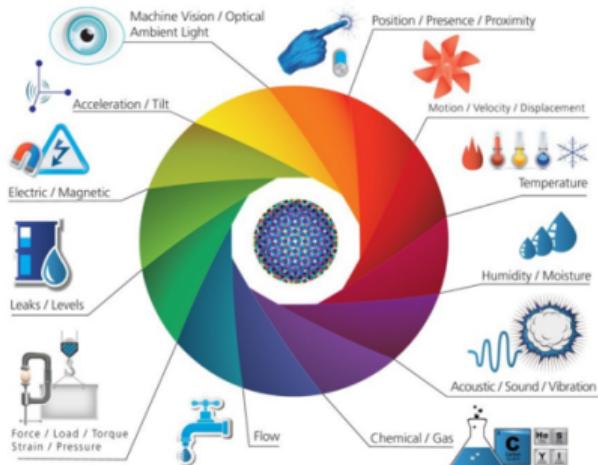


Power Electronics and Future Applications



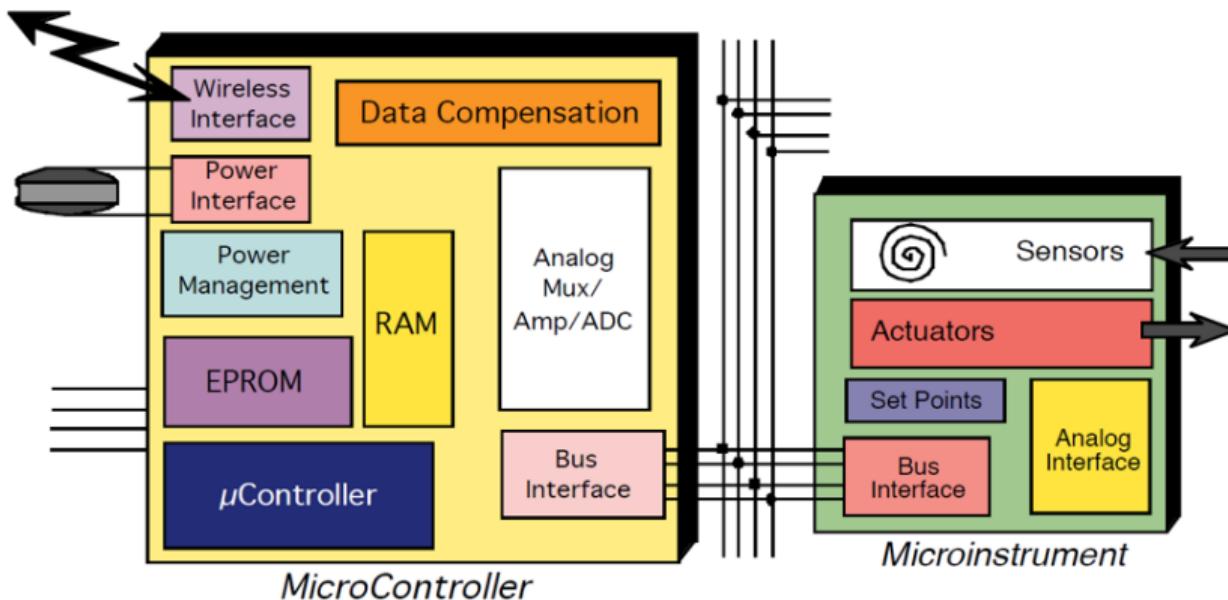
- Save up to 90% of the wiring and up to 15% of the volume in the battery pack.
- Circuit design is a trillion-dollar business and is still evolving.

What Else We Can Do with Circuits?



- Understanding the trend will lead you to success.
- 5G smart sensors and IoT

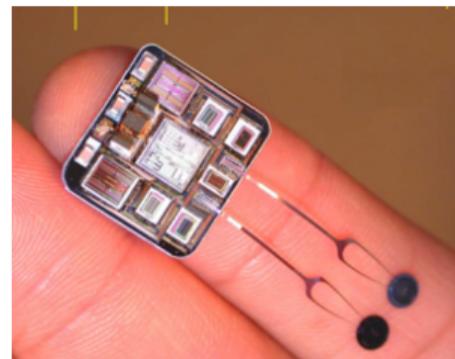
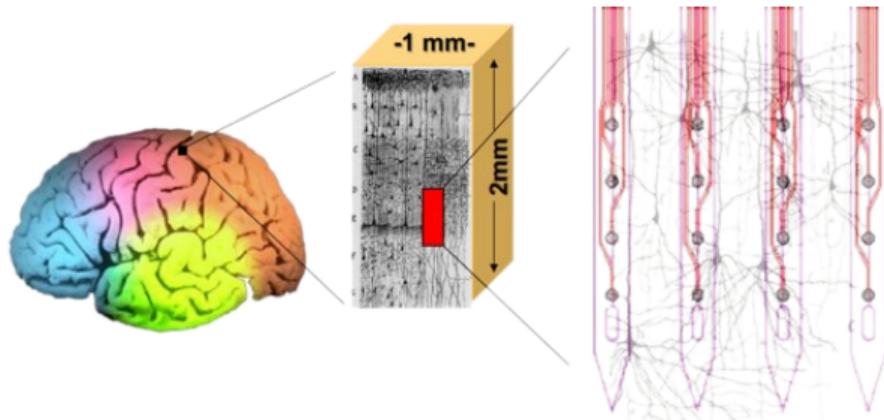
What Else We Can Do with Circuits?



Brain-Machine Interface

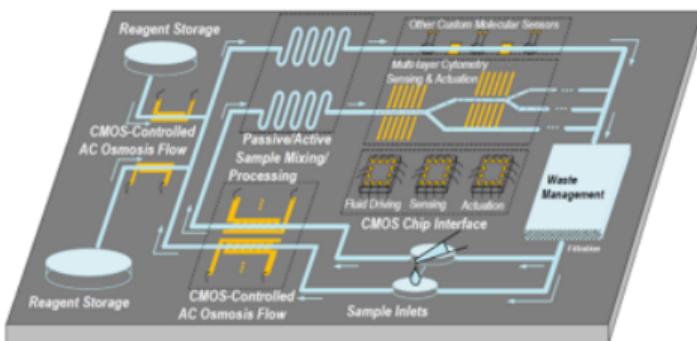


- Another hot topic is health driven applications

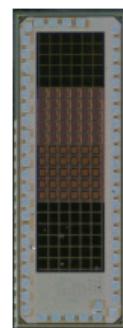


Polymerase Chain Reaction (PCR) Test

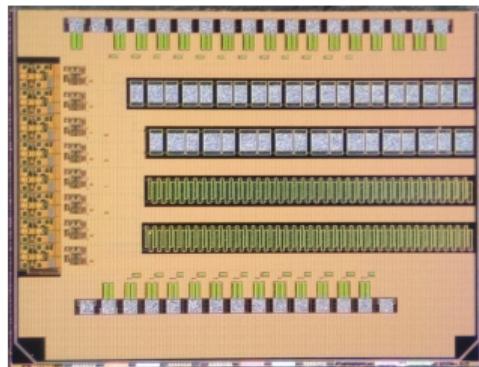
- Yuchen Ai, a former JI undergraduate student, currently a Ph.D student in my lab, is developing a portable PCR device.



System Setup



Optics Chip



Osmosis Chip Photo

Future Cellphones (Wireless Comm)

- Why is 5G faster and cost less energy?

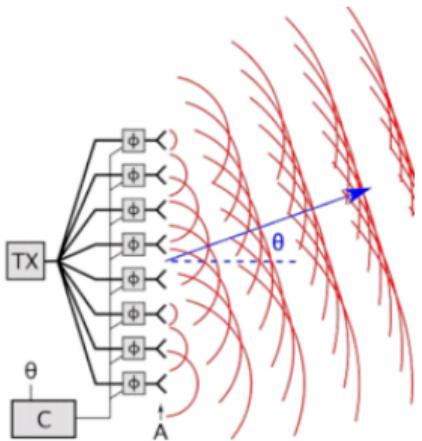


Current (4G) Antenna for 4th-generation base systems



New (5G) base systems Massive APAA for 5th-generation base systems

Future Cellphones (Wireless Comm)



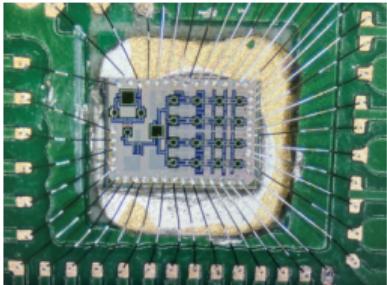
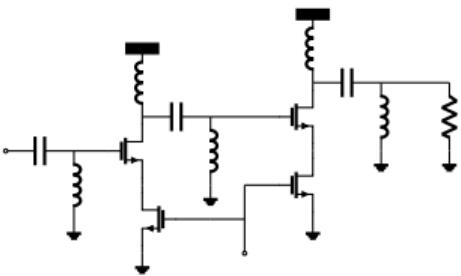
- Concept of phased arrays

Future Radar



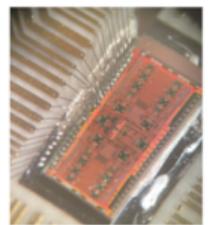
- JAGM tri-mode seeker from Lockheed Martin combines mmW, IR, and laser.
- Fundamental RF building blocks my students tapedout this year.

Future Cellphones (Wireless Comm)

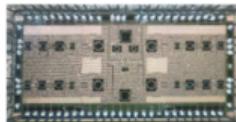


- Zhehao. Yu, Xuyang. Lu, Changzhan. Gu, Suresh. Venkatesh and Junfa. Mao, "mmWave Spatial–Temporal Single Harmonic Switching Transmitter Arrays for High Back-Off Beamforming Efficiency," in IEEE Transactions on Antennas and Propagation, vol. 70, no. 9, pp. 8122-8136, Sept. 2022.
- Zhehao Yu published a first-author paper in his 4th year here at JI and taped out a chip.

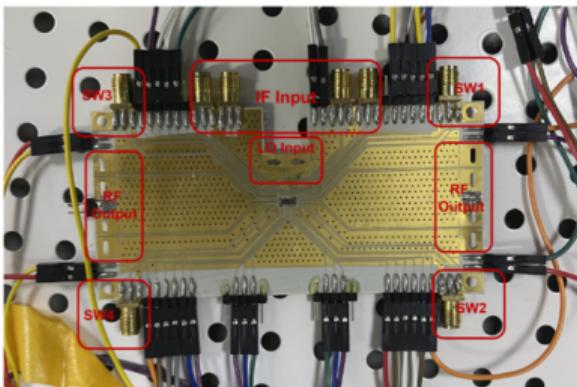
Future Cellphones (Wireless Comm)



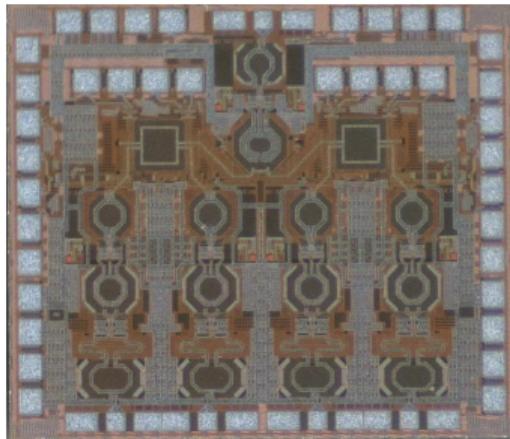
Bonding structure



Packaged chip

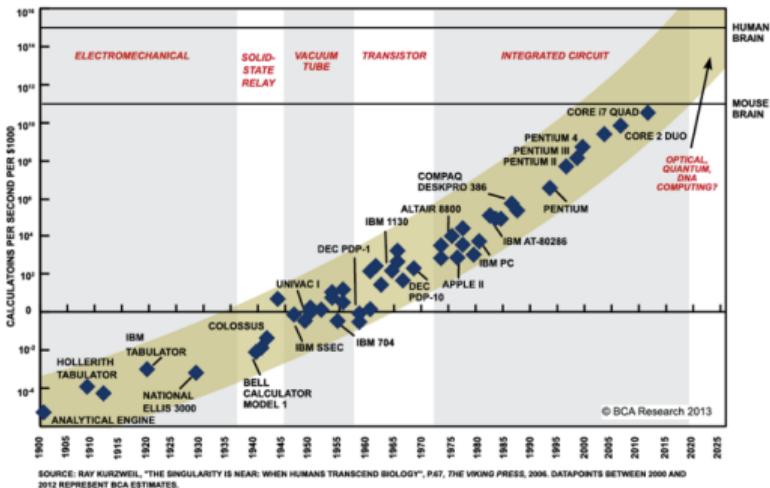


Measuring setup



- In integrated circuit (IC) design, a critical aspect lies in the embrace of failure and the commitment to rapid iteration for improvement.

Long Live Moore's Law



- People start to predict the death of Moore's law since 2015.

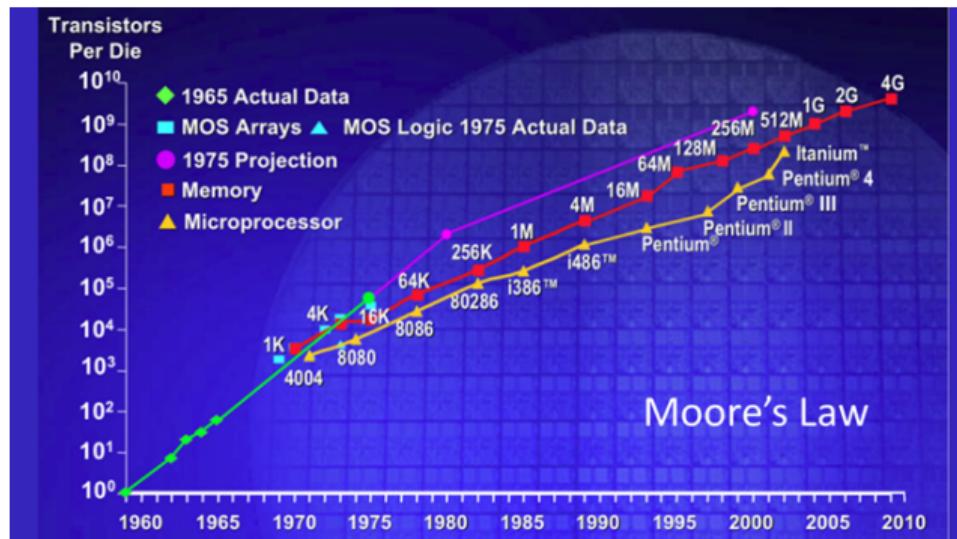
Why is Moore's Law Important?



Gordon Moore,
Co-founder of Fairchild and Intel

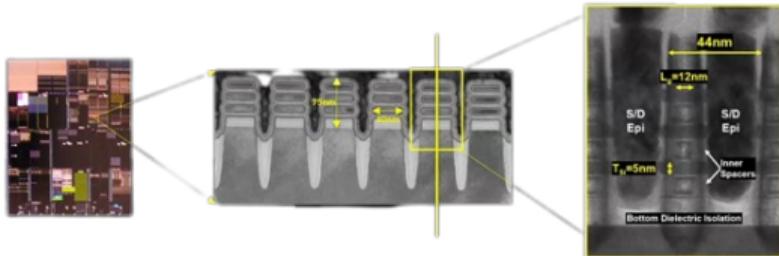
- Every digital circuit class talks about Moore's law in the first class, why?
- What makes semiconductor a \$300 Billion market?
- Moore's law is what makes electrical engineer a good job.

Why is Moore's Law Important?



- Memory scales with processors as well.

IBM's 2 nm Process



IBM announced the world's first chip with 2 nm technology that combines:

- A 2nd generation Inner Spacer dry process for precise gate control
- EUV patterning to produceable Nanosheet widths from 15 nm to 70 nm
- Expected to offer 45% performance improvement or 75% power reduction compared to 7nm

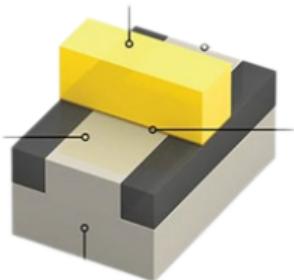
The Power of Scaling



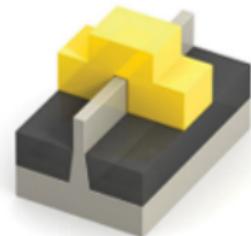
Tech node	IBM	TSMC	Intel	Samsung
22 nm			16.50	
14 nm		28.88	44.67	33.32
10 nm		52.51	100.8	51.82
07 nm		91.20	237.2	95.08
05 nm		171.3		
03 nm		292.2		
02 nm	333.3			

- Millions of transistors that can be placed in 1 mm²
- Higher density of transistors

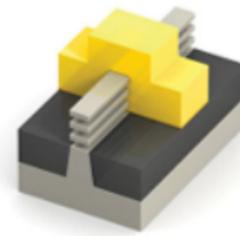
State of Art 2 nm Process



Planar FET



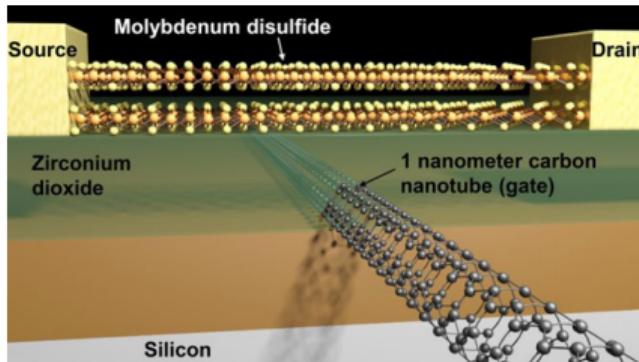
FinFET



nanosheet

- Up until about 2011, planar transistors were the best devices available.
- Multi-layer gate is created through nanosheet transistors to improve leakage

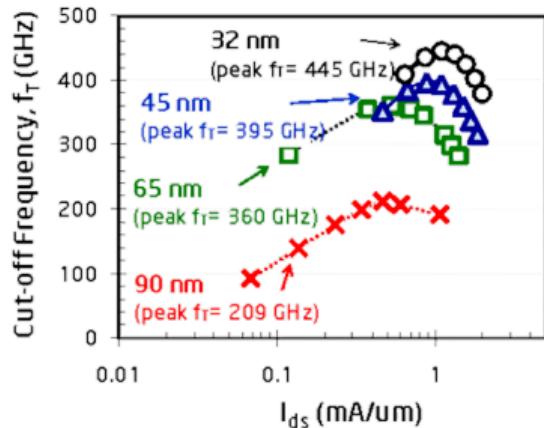
What We Expect



Prof. Ali Javey at Lawrence Berkeley National Laboratory

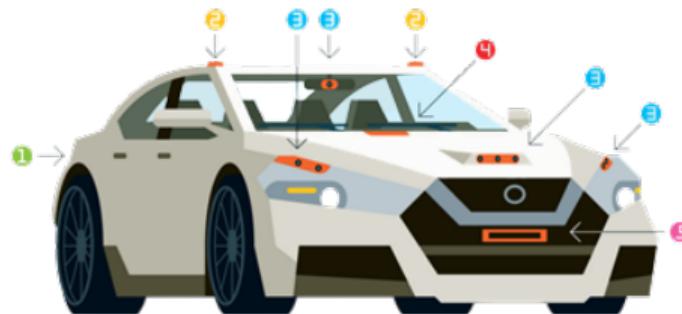
- We are currently at 7 nm. Carbon nanotube research points to at least 0.04 nm.
- The number of transistor doubles about every two years, **how many years?**

Other Benefits of Scaling



Dennard Scaling and F_T

- Now we can interact with higher and higher frequencies.
- What my lab explores.



mmWave Radar and Sensing