Lecture 2

VE 311 Analog Circuits

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Recap of Last Lecture

- Logistics
- Analog Circuits
- Moore's Law

To Be Covered In This Lecture

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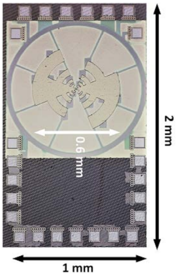
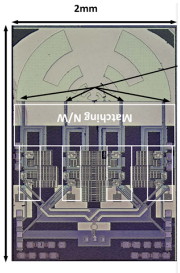
- Scaling
- Review of 215 (Thevenin)
- Semiconductor Basics

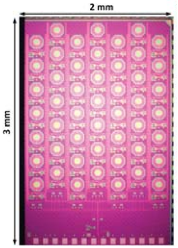
RF, mm-Wave, and THz chips



Imaging



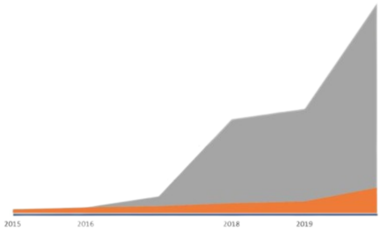
Communication



Biomedical

- Now we can interact with higher and higher frequencies.
- What my lab explores.

Apple A-series As an Example

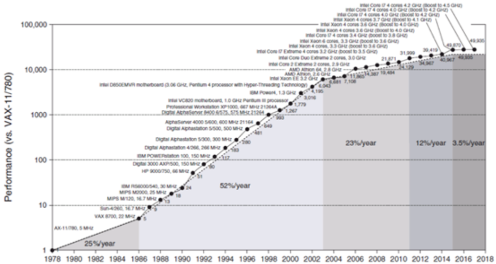


Alternative Processing Power (A9-A14)

- 16 core NPU (11 TOPS)
- ML accelerators
- GPU and Rendering
- Facial recognition
- Speech recognition
- Augmented reality

- Emergence of dedicated AI accelerator ASICs are 10× more efficient than CPU.
- Historically CPU doubles every 24 mos., it's now down to 30%
- We're now seeing 100%+ processing power improvements for SoC

CPU Performance Trends



Performance of CPU over the years (Source: HENNESSY,2017)

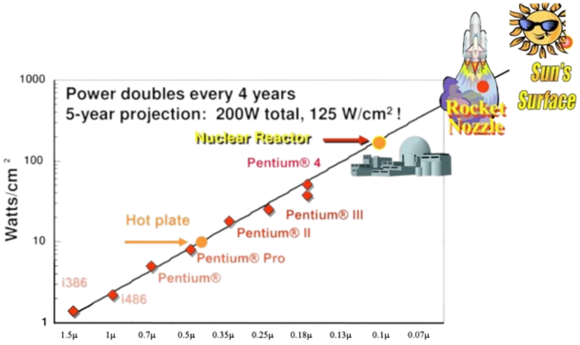
- Dennard scaling in CPU has come to an end.
- Now transistors can interact with 100 GHz, why the clock is still 4 GHz?

Dennard Scaling

Transistor properties	dennardian	post dennard
Quantity	s^2	s^2
Frequency	s	s
Capacitance	$1/s$	$1/s$
V_{dd}^2	$1/s^2$	1
power $= V_{dd}^2 \cdot F \cdot C \cdot Q$	1	s^2

- As the size of the transistors shrunk, and the voltage was reduced, circuits could operate at higher frequencies at the same power.
- Dennard scaling ignored the leakage current, saturation velocity, and threshold voltage, which establish a baseline of power per transistor.

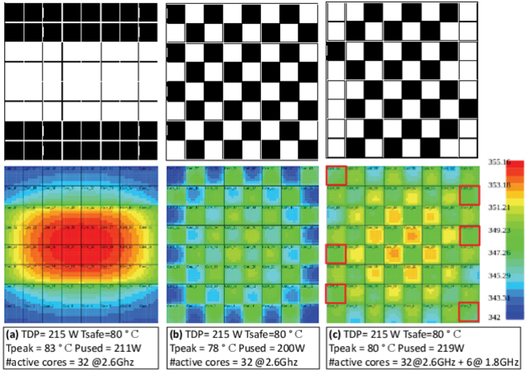
CPU Performance Trends



Source: Fred Pollack

- Power density increases exponentially.

Dark Silicon



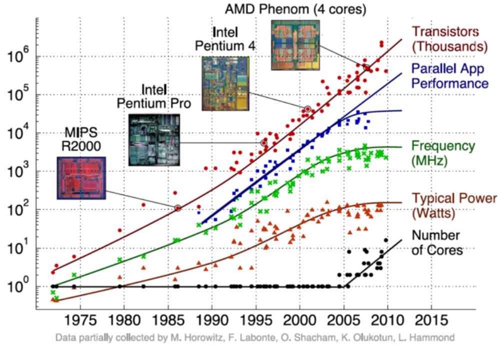
Heat map of multi-core processors

Solutions:

- Thermal management
- Power management
- Multi-thread mapping
- Degree of-parallelism
- Frequency/Supply (Dim)

In a 10 nm process, dark silicon can be 50% 80%

Power and Performance



Performance of CPU over the years

- These created a “Power Wall” that has limited practical processor frequency to around 4 GHz since 2006.
- Improvement from multi-core and accelerators, but not frequency.

Ever-increasing Need

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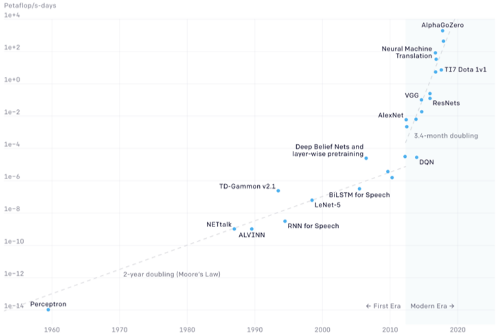
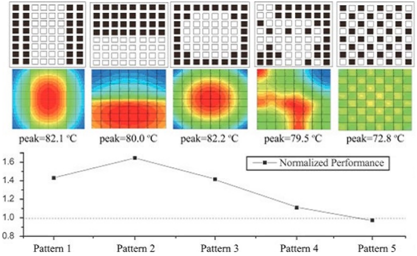


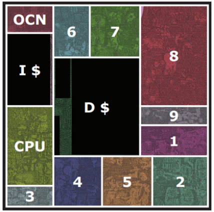
Requirement of computational power over algorithms

- The development of AI algorithms requires increasing computational power.

Area versus Power



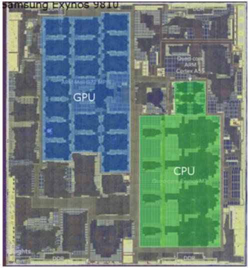
Heatmaps



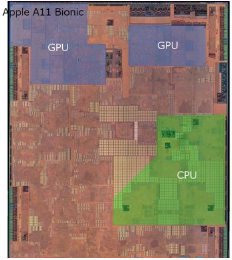
ASIC Cores

- Because of dark silicon, power instead of area is the biggest challenge.
- In RISC, many power are wasted for reconfigurability, such as instruction fetching.

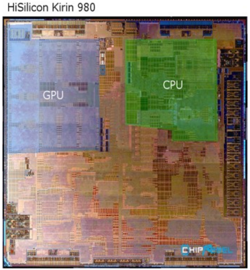
RF, mm-Wave, and THz chips



Samsung 9810



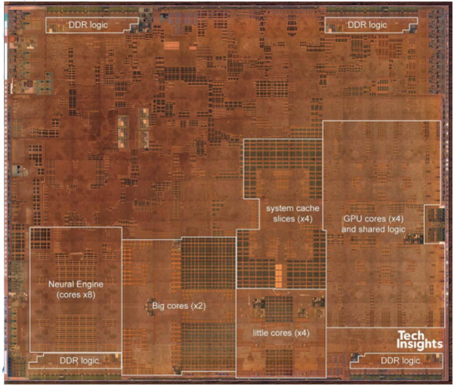
Apple A11 Bionic



Kirin 980

- Integration of CPU, GPU, and XPU on the same die is possible.

State of the Art SOCs



- 2x Large CPUs
- 4x Small CPUs
- GPUs
- Neural processing unit (NPU)
- Lots of memory
- DDR memory interfaces

Course Outcome

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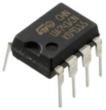
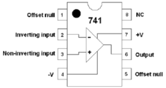
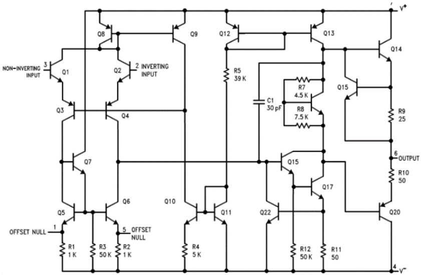
Understanding





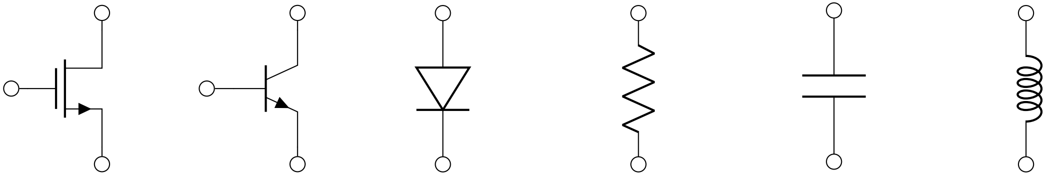


Innovation

- You are only bounded by your imagination.
- Welcome to our lab’ s weekly group meeting.
- Propose project ideas and seek guidance.
- Take upper-level courses.

Active vs Passive Components

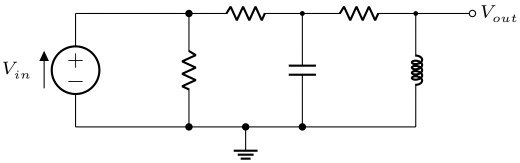
Active Components | Passive Components

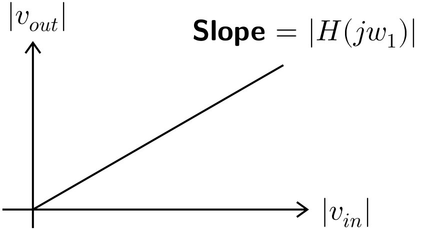


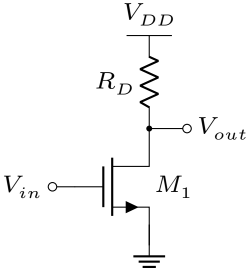
MOSFET BJT Diode | Resistor Capacitor Inductor

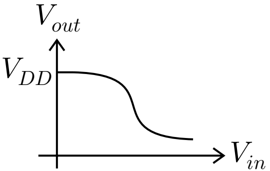
VE311 | **VE215**

Linear vs Nonlinear Circuit









Analog vs Digital

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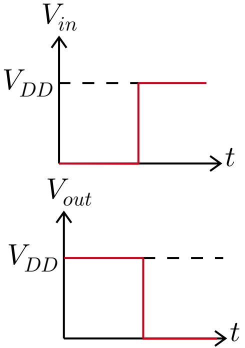
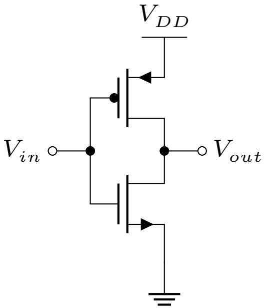
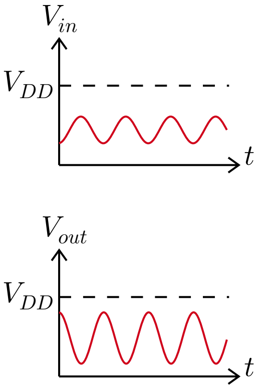
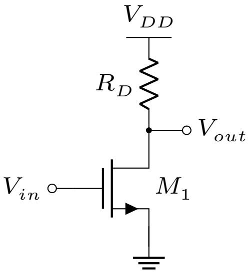
VE312: Digital



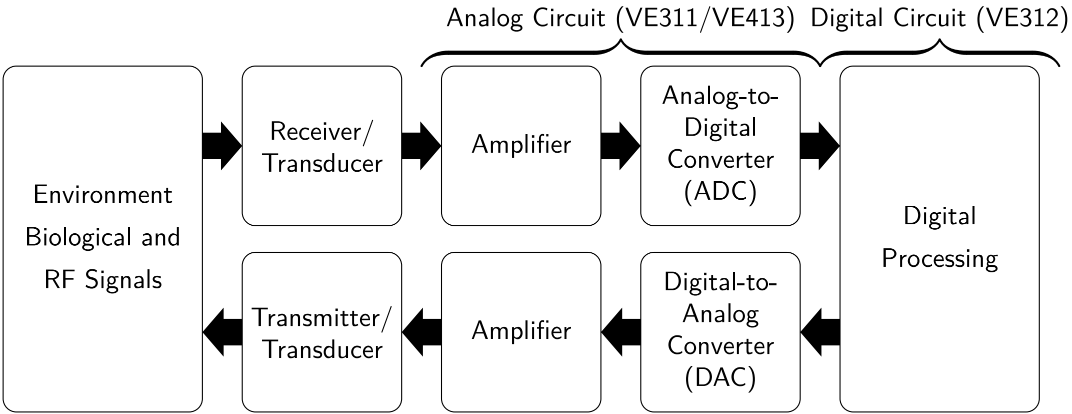


VE311: Analog





Analog Circuit in IC



IC Design Process

Hand calculations on paper based on proper approximations.

↓

Pre-simulation: Schematic design and simulation on Spice.

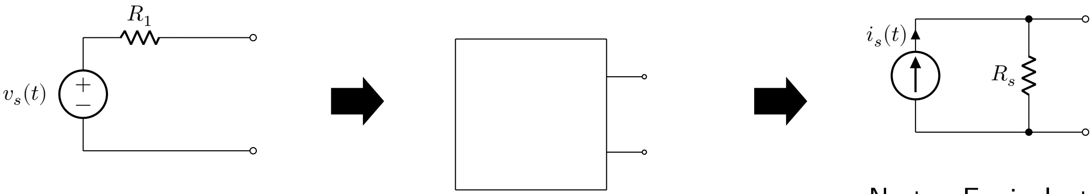
→

Post-simulation: Layout drawing, simulation and design rule check on Cadence.

↑

Tapeout: Layout design sent to IC manufacturers.

Thevenin and Norton Equivalents

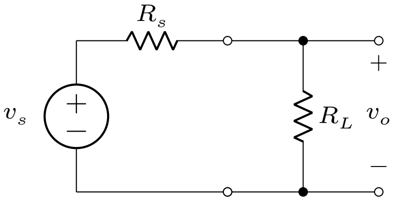


Thevenin Equivalent

Norton Equivalent

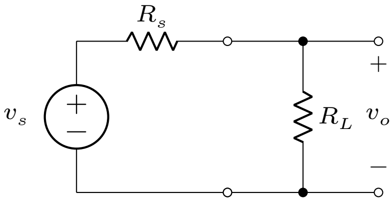
- Read Sedra and Smith, Section 1.1

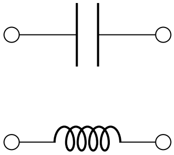
Thevenin and Norton Equivalents



- What is the voltage at the output?
- We should know Thevenin and Norton Equivalents of a network.

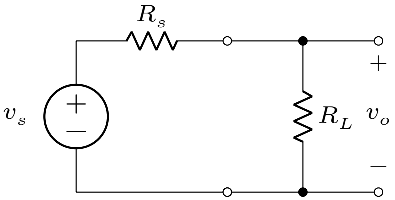
Thevenin and Norton Equivalents





- If the resistance is replaced with an impedance, the same principle shall hold.

Thevenin and Norton Equivalents



- Do we want larger or smaller R_s to get the largest output voltage?

Thevenin and Norton Equivalents

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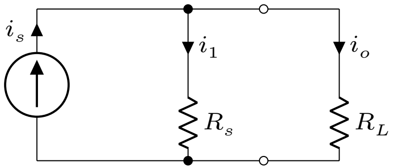

Norton Equivalents

$$i_o = i_s \frac{R_s}{R_L + R_s}$$

- From a current perspective, do we want large or small R_s?

Thevenin and Norton Equivalents

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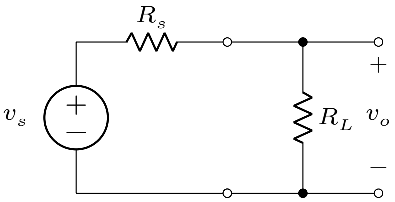


- What is the condition for maximum power transfer to the load?
- Why is it important?

Power Calculation

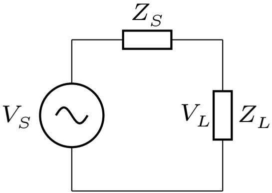
Why is power $\frac{1}{2}\,\mathrm{Re}\left\{\mathrm{VI}^*\right\}$

$$s(t) = v(t) \cdot i(t) = V_M \cdot \cos\left(\omega t + \phi_V\right) \cdot I_M \cdot \cos\left(\omega t + \phi_I\right) \tag{1}$$

$$= \frac{V_M I_M}{2} \cdot \left[\cos\left(\phi_V - \phi_I\right) + \cos\left(2\omega t + \phi_V + \phi_I\right)\right] \tag{2}$$

So the average power is nothing more than the non-time varying component.
Therefore, we create the complex power notion $S = P + jQ$

Maximum Power Transfer



What is the power delivered to the load?

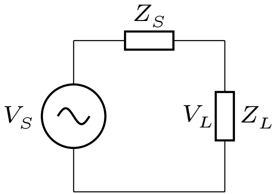
- source impedance

$$Z_s = R_s + jX_s \tag{3}$$

- load impedance

$$Z_L = R_L + jX_L \tag{4}$$

Maximum Power Transfer



$$P = \frac{1}{2} V_L^2 \,\mathrm{Re}\left(\frac{1}{Z_L}\right) = \frac{1}{2} V_S^2 \left|\frac{Z_L}{Z_S + Z_L}\right|^2 \mathrm{Re}\left(\frac{1}{Z_L}\right) \tag{5}$$

$$P = \frac{1}{2} V_S^2 \frac{R_L}{(R_S + R_L)^2 + (X_S + X_L)^2} \tag{6}$$

- power delivered to load as function of circuit parameters

Maximum Power Transfer

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$$P = \frac{1}{2} V_S^2 \frac{R_L}{(R_S + R_L)^2 + (X_S + X_L)^2} \tag{7}$$

- To find the maximum, we can take partial derivative and set them to be zeros
- We can do $\frac{\partial P}{\partial R_L} = 0$ and $\frac{\partial P}{\partial X_L} = 0$

$$\begin{cases} R_S^2 - R_L^2 + (X_L + X_S)^2 = 0 \\ X_L (X_L + X_S) = 0 \end{cases} \tag{8}$$

$$\begin{cases} R_S = R_L \\ X_L = -X_S \end{cases} \tag{9}$$

Maximum Power Transfer

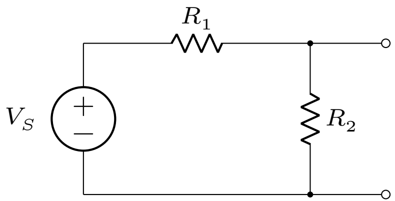
$$P = \frac{1}{2}V_S^2 \frac{R_L}{(R_S + R_L)^2 + (X_S + X_L)^2} \tag{10}$$

- Now we plug it back into the equation

$$P = \frac{V_S^2}{8R_S} \tag{11}$$

- It represents the highest power that can be extracted from the source.

Finding Thevenin Equivalent Voltage



To find V_{TH}

- Open circuit output terminals
- Find V_{OC}

$$V_{TH} = V_{OC} \tag{12}$$

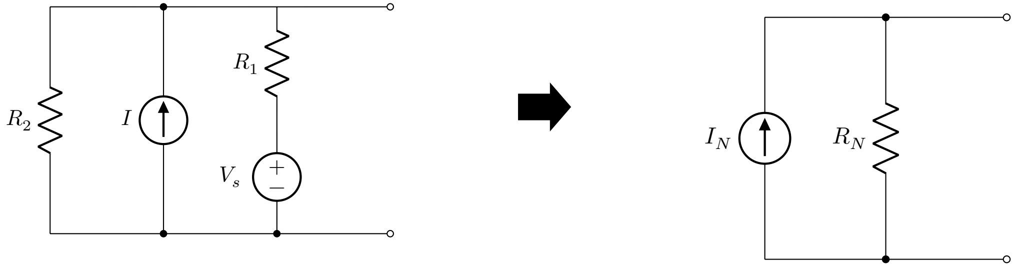
Finding Thevenin Equivalent Resistance

To find R_{TH}

- Zero out independent sources
- Current sources are replaced with an open circuit and voltage sources are replaced with a short circuit.
- Determine the equivalent resistance seen through the port by applying a test source (V_T or I_T)

$$R_{TH} = V_T / I_T \tag{13}$$

Practice: Finding Norton Equivalent



- Make sure you know this by heart, practice Thevenin model as well.

Thevenin Voltage of Dependent Sources

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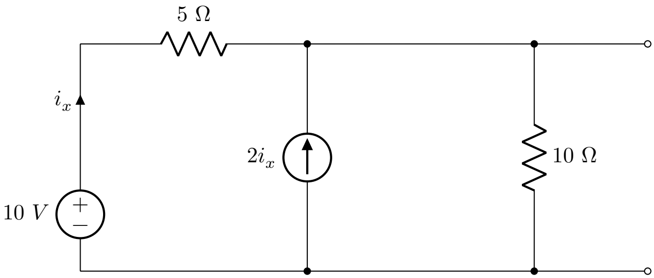

Thevenin Resistance of Dependent Sources

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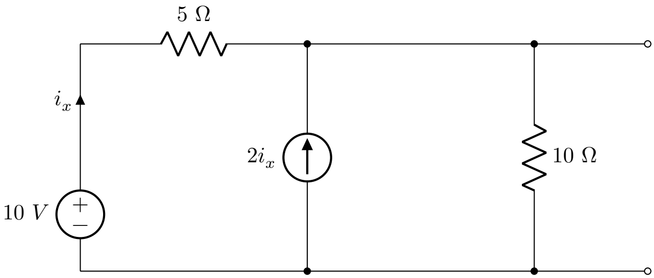
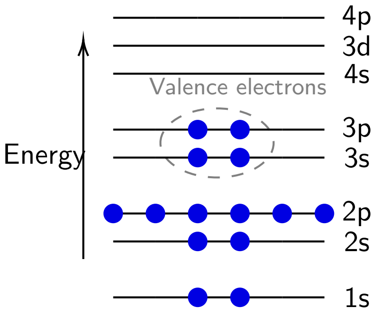


Semiconductor Physics



- Pauli exclusion principle requires that each electron must have a distinct energy state defined by a unique set of quantum numbers.

Semiconductor Physics

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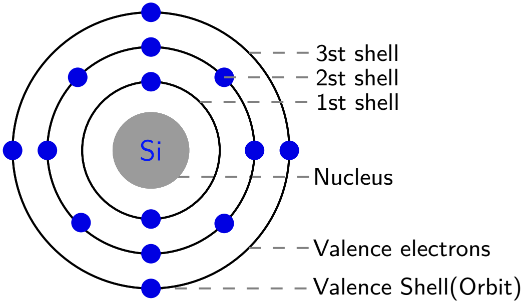

- Silicon has its inner shell (1s, 2s and 2p orbitals) totally filled with electrons.
- It's outer shell has 2 valence electrons in 3s orbital and 2 valence electrons in 3p orbital.

Semiconductor Physics

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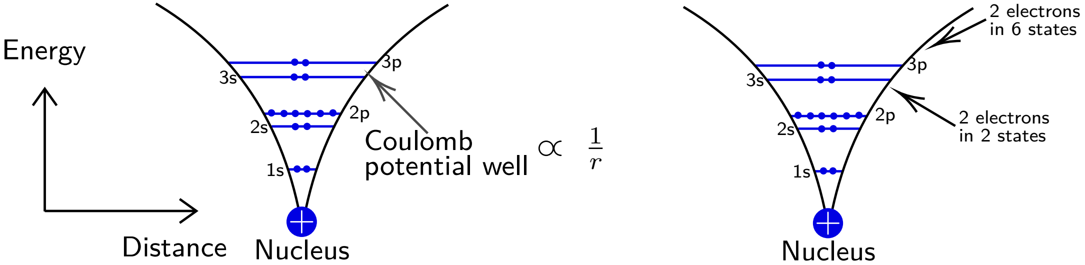
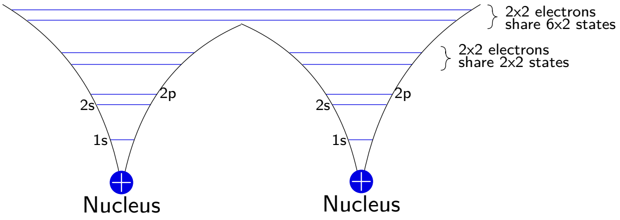
- When two silicon atoms are far away from each other, there is no interaction.



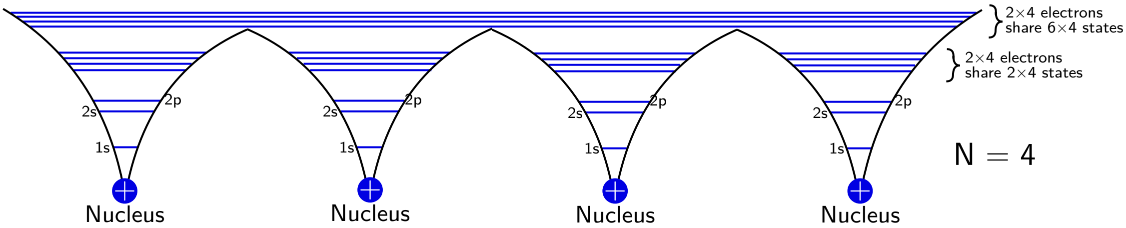
Semiconductor Physics



When two silicon atoms are close enough to each other:

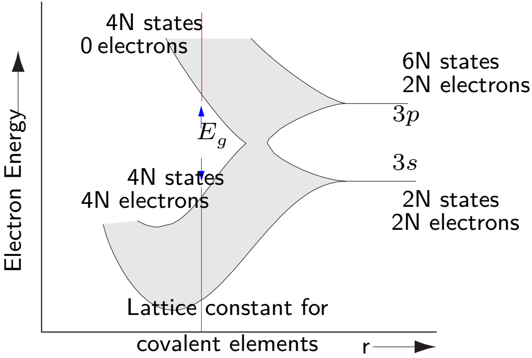
- Wavefunctions overlap and potential wells are influenced by neighboring nucleus
- The valence electrons become delocalized (e.g. through tunneling).
- Each state splits into N substates, where N is number of atoms.

Semiconductor Physics



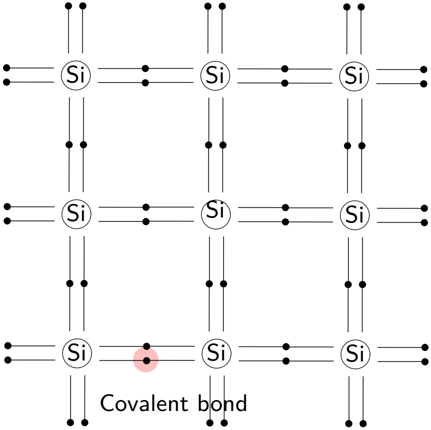
- Discrete states grow into bands when N is large.

Semiconductor Physics

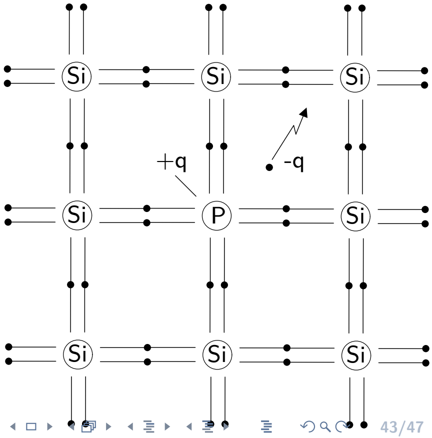


- the band gap energy (1.12 eV) is relatively small
- electrons with sufficient thermal energy can jump from valence band to conduction band

Intrinsic Si



Electrons with sufficient thermal energy can jump from valence band to conduction band.



Intrinsic Si

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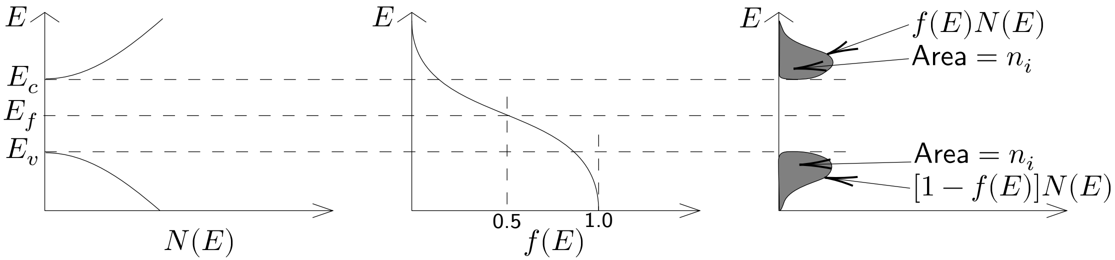
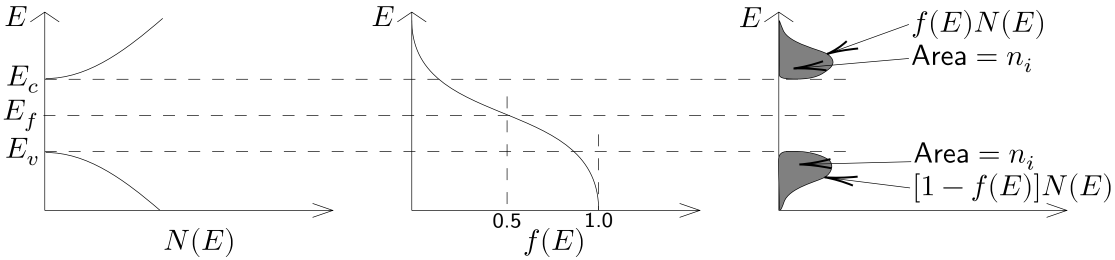


Density of States$/(\mathrm{cm}^3 * \mathrm{J})$

Fermi-Dirac Distribution

$$f(E) = \frac{1}{\exp(\frac{E - E_f}{k\mathrm{T}}) + 1} \tag{14}$$

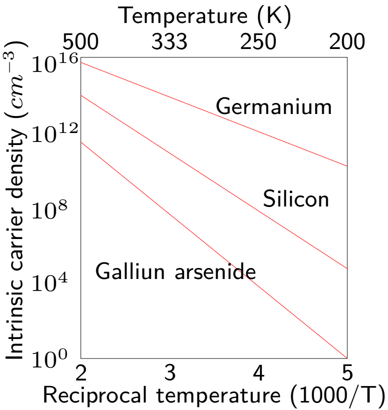
Intrinsic Si



$$n = \int_{E_c}^{\infty} f(E)N(E)dE = n_i \qquad (15)$$

$$p = \int_{-\infty}^{E_v} [1-f(E)]N(E)dE = n_i \qquad (16)$$

Intrinsic Si



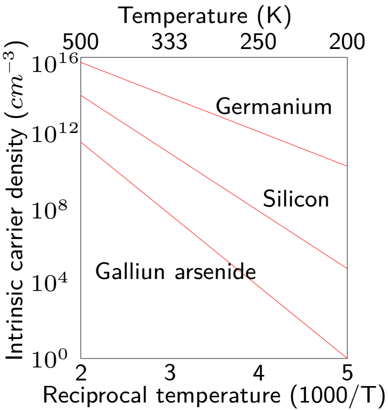
$$np = n_i^2 = \mathrm{B}\mathrm{T}^3 \exp\left(-\frac{E_G}{k\mathrm{T}}\right) \tag{17}$$

k (Boltzmann's Constant)

$$= 1.38 \times 10^{-23}\ \mathrm{J/K} = 8.62 \times 10^{-5}\ e\mathrm{V/K} \tag{18}$$

	B ($K^{-3}\cdot cm^{-6}$)	E_G (eV)
Si	1.08 $\times 10^{31}$	1.12
Ge	2.31 $\times 10^{30}$	0.66
GaAs	1.27 $\times 10^{29}$	1.42

Intrinsic Si



At 300K

$$n_i^2 = (1.08 \cdot 10^{31}) \cdot 300^3 \cdot e^{\frac{-1.12}{(8.62 \cdot 10^{-5}) \cdot 300}}$$

$$= 4.52 \times 10^{19} (1/\mathrm{cm}^6) \tag{19}$$

$$n_i = 6.73 \times 10^{9} (1/\mathrm{cm}^3) \approx 10^{10} (1/\mathrm{cm}^3) \tag{20}$$