Lecture 11: Mosfet Large Signal

VE311 Electronic Circuits

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Recap of Last Lecture

- MOSFET

Topics to Be Covered

- MOSFET Circuits

Spice Models

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NMOS Model			
LEVEL=1	VTO=0.7	GAMMA=0.45	PHI=0.9
NSUB=9e+14	LD=0.08e-6	UO=350	LAMBDA=0.1
TOX=9e-9	PB=0.9	CJ=0.56e-3	CJSW=0.35e-11
MJ=0.45	MJSW=0.2	CGDO=0.4e-9	JS=1.0e-8
PMOS Model			
LEVEL=1	VTO=-0.8	GAMMA=0.4	PHI=0.8
NSUB=5e+14	LD=0.09e-6	UO=100	LAMBDA=0.2
TOX=9e-9	PB=0.9	CJ=0.94e-3	CJSW=0.32e-11
MJ=0.5	MJSW=0.3	CGDO=0.3e-9	JS=0.5e-8

Spice Models

- Simulators such as SPICE and Cadence need accurate models for each device.
- Above is the simplest MOS SPICE model, known as "Level 1," and provide typical values for each parameter corresponding to 0.5-μm technology.

Spice Models

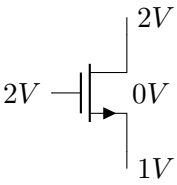
VTO : threshold voltage with zero V_{SB} (unit : V)
GAMMA : body effect coefficient (unit : $V^{1/2}$)
PHI : $2\Phi_F$ (unit : V)
TOX : gate oxide thickness (unit : m)
NSUB : substrate doping (unit : cm^{-3})
LD : source/drain side diffusion (unit : m)
UO : channel mobility (unit : $cm^2/V/s$)
LAMBDA : channel-length modulation coefficient (unit : V^{-1})

Spice Models

CJ : source/drain bottom-plate junction capacitance per unit area (unit : F/m^2)
CJSW : source/drain sidewall junction capacitance per unit length (unit : F/m)
PB : source / drain junction built-in potential (unit : V)
MJ : exponent in CJ equation (unitless)
MJSW : exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit : F/m)
CGSO : gate-source overlap capacitance per unit width (unit : F/m)
JS : source/drain leakage current per unit area (unit : A/m^2)

Body Effect Example

$$\lambda \neq 0 \quad \gamma \neq 0 \tag{1}$$



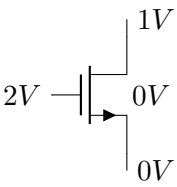
$$(\frac{W_{drawn}}{L_{drawn}}) = \frac{10\mu m}{2\mu m} \tag{2}$$

$$V_{th} = 0.7 + 0.45(\sqrt{0.9+1} - \sqrt{0.9}) \tag{3}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{4}$$

Body Effect Example

$$\lambda \neq 0 \quad \gamma \neq 0 \tag{5}$$



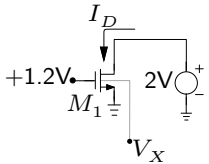
$$(\frac{W_{drawn}}{L_{drawn}}) = \frac{10\mu m}{2\mu m} \tag{6}$$

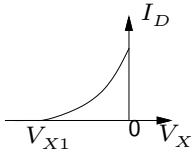
$$V_{th} = 0.7 + 0.45(\sqrt{0.9+1} - \sqrt{0.9}) \tag{7}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L_{eff}}\right)\left[(V_{GS} - V_{TH})\,V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{8}$$

Body Effect Example

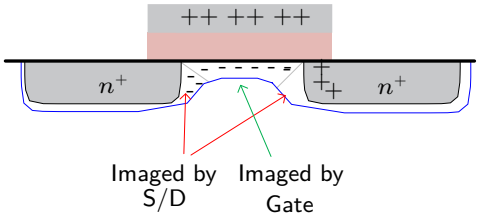
Sketch I_D as a function of V_X increasing from $-\infty$ to 0. Assume $V_{TH} = 0.6V$, $\gamma = 0.4V^{1/2}$ and $2\Phi_F = 0.7V$.

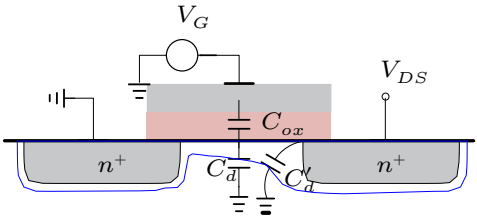




Solution: $1.2 = 0.6 + 0.4\left(\sqrt{0.7 - V_X} - \sqrt{0.7}\right), V_X = -4.76\ V$

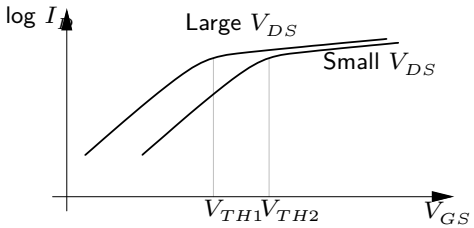
Drain-induced Barrier Lowering

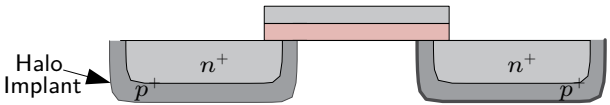




In short-channel devices, the drain is close enough to gate the channel, and so a high drain voltage can open the bottleneck and turn on the transistor prematurely.

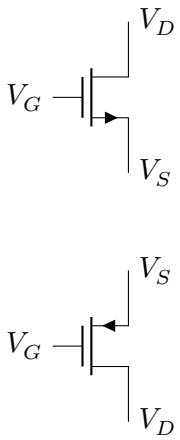
Drain-induced Barrier Lowering

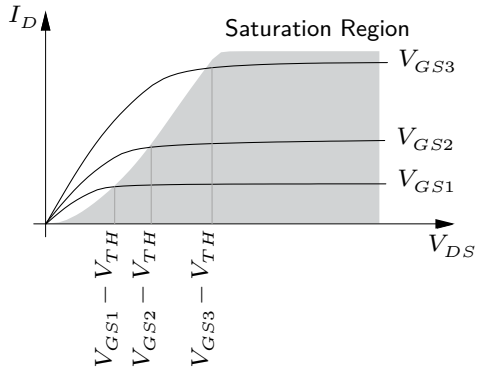




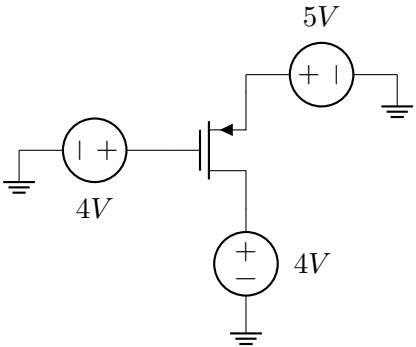
In short-channel devices, the drain is close enough to gate the channel, and so a high drain voltage can open the bottleneck and turn on the transistor prematurely.

NMOS vs PMOS


V_D
V_G
V_S
V_S
V_G
V_D

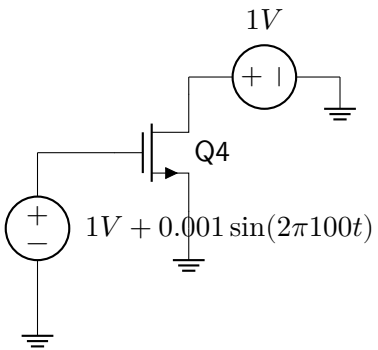

I_D
Saturation Region
V_{GS3}
V_{GS2}
V_{GS1}
V_{DS}
$V_{GS1} - V_{TH}$
$V_{GS2} - V_{TH}$
$V_{GS3} - V_{TH}$

PMOS Example



Small-Signal Example

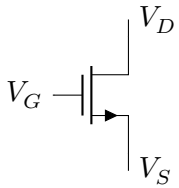
$$(\frac{W_{drawn}}{L_{drawn}}) = \frac{10\mu m}{2\mu m} \qquad (9)$$



- No bulk connect means ground for NMOS

Transconductance

- For the NMOS operating in the saturation region ($V_{DS} \geq V_{GS}–V_{TH}$):



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}\left(V_{GS} - V_{TH}\right)^2 \quad (10)$$

- ΔV_{GS} results in $\Delta I_D = g_m \times \Delta V_{GS}$.

Transconductance

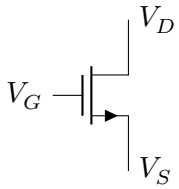
$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH}) = \sqrt{2\mu_n C_{ox} \frac{W}{L'} I_D} = \frac{2I_D}{V_{GS} - V_{TH}} \tag{11}$$

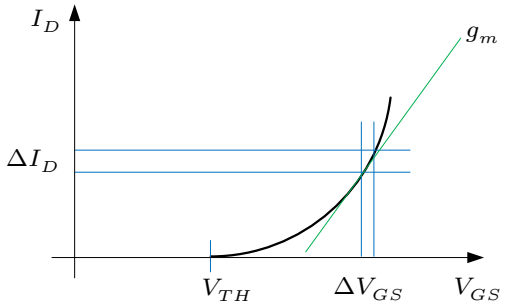
With channel-length modulation

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) (1 + \lambda V_{DS}) \tag{12}$$

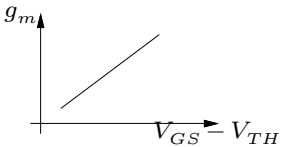
$$= \sqrt{2\mu_n C_{ox} (W/L) I_D (1 + \lambda V_{DS})} \tag{13}$$

Transconductance

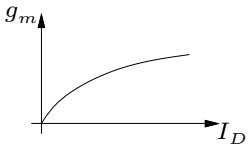




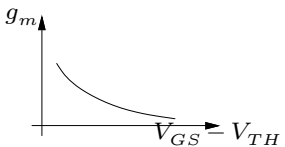
Transconductance



W/L Constant



W/L Constant



I_D Constant

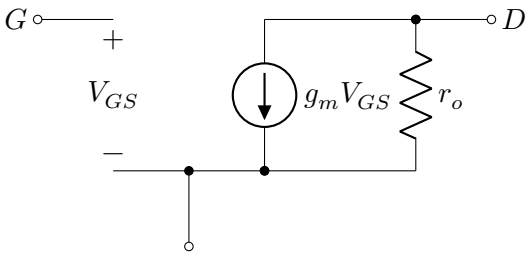
- For a given NMOS, gm changes according to the DC biasing condition.
- If a small signal is applied to a NMOS with defined biasing values, we assume the signal amplitude is small enough that the variation in gm is negligible.

Small-Signal Model for NMOS

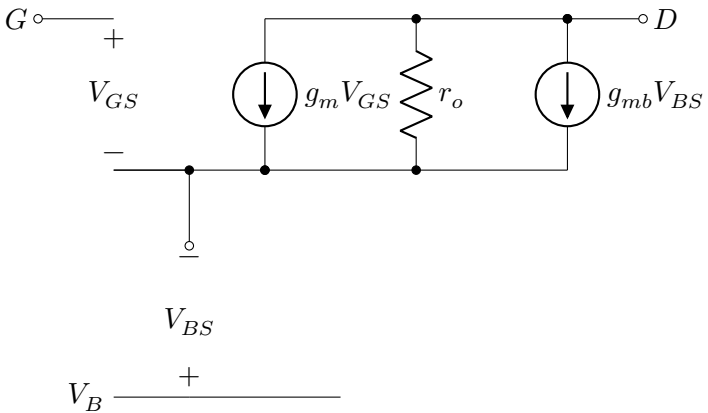
$$r_o = \frac{\partial V_{DS}}{\partial I_D} \tag{14}$$

$$= \frac{1}{\partial I_D / \partial V_{DS}} \tag{15}$$

$$= \frac{1}{\frac{1}{2}\mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_{TH}\right)^2 \cdot \lambda} \tag{16}$$



Small-Signal Model for NMOS



Small-Signal Model for NMOS

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} \tag{17}$$

$$= \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_{TH}\right) \left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right) \tag{18}$$

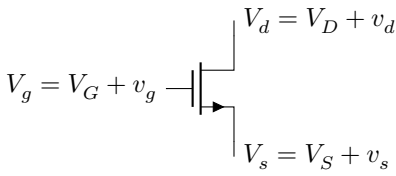
$$\frac{\partial V_{TH}}{\partial V_{BS}} = -\frac{\partial V_{TH}}{\partial V_{SB}} \tag{19}$$

$$= -\frac{\gamma}{2} \left(2\Phi_F + V_{SB}\right)^{-1/2} \tag{20}$$

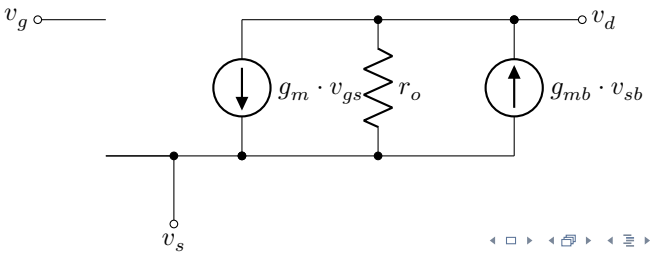
$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} \tag{21}$$

$$= \eta g_m \tag{22}$$

Small-Signal Model for NMOS

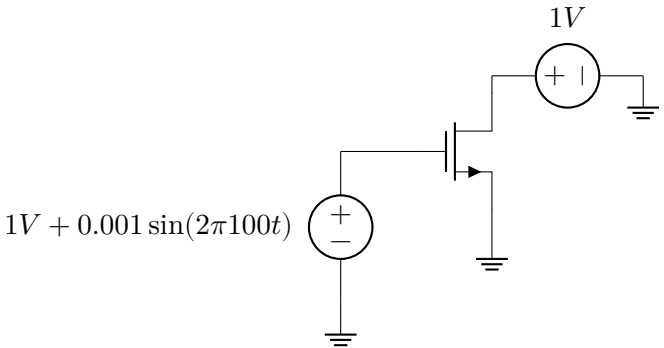


$$\downarrow i_d = g_m \cdot v_{gs} \quad \uparrow i_d = g_{mb} \cdot v_{sb} \quad (23)$$



Small-Signal Example

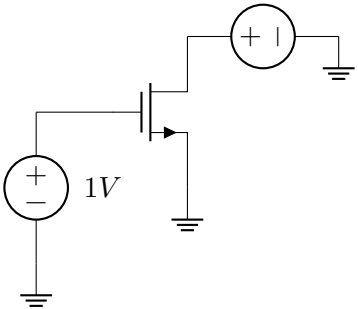
$$(\frac{W_{drawn}}{L_{drawn}}) = \frac{10\ \mu m}{2\ \mu m} \qquad (24)$$



Small-Signal Example

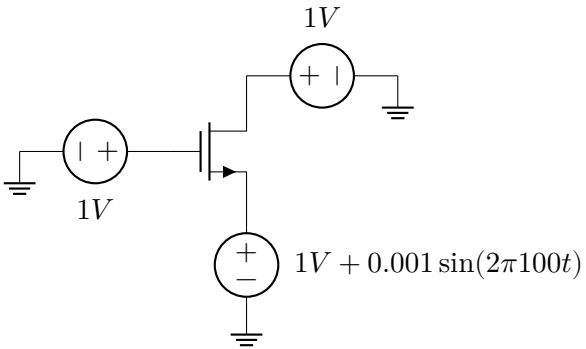
$$(\frac{W_{drawn}}{L_{drawn}}) = \frac{10\ \mu m}{2\ \mu m} \qquad (25)$$

$$1V + 0.001\sin(2\pi 100t)$$

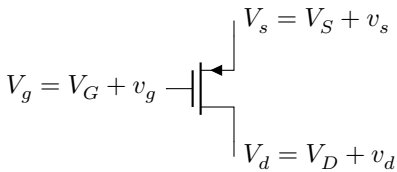


Small-Signal Example

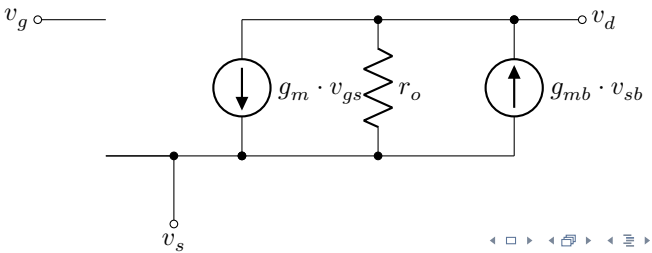
$$(\frac{W_{drawn}}{L_{drawn}}) = \frac{10\ \mu m}{2\ \mu m} \qquad (26)$$



Small-Signal Model for PMOS

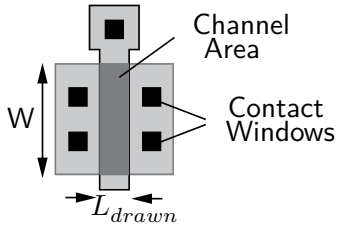


$$\uparrow i_d = g_m \cdot v_{gs} \quad \downarrow i_d = g_{mb} \cdot v_{sb} \quad (27)$$

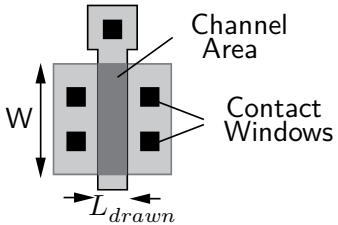


Layout

NMOS



PMOS



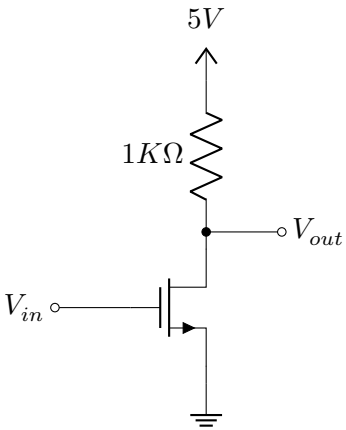
Layout

- W/L is chosen to determine g_m.
- Minimum L is dictated by the process.
- Design rules:
  - Poly-Si extends beyond the channel area by some amount.
  - Enough n^+, p^+ or poly-Si area surrounding each via.
  - Enough distance between two vias.
  - Many others.

NMOS vs PMOS in Performance

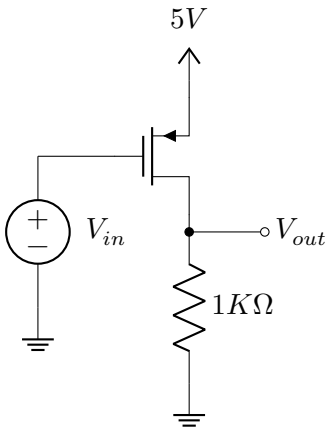
- PMOS devices are quite inferior to NMOS in most CMOS technology.
- Lower mobility of holes ($\mu_p C_{ox} \approx 0.5\mu_n C_{ox}$) yield lower current drive and conductance.
- NMOS exhibit higher output resistance, providing more ideal current sources and higher voltage gain.
- It is preferable to use NMOS rather than PMOS wherever possible.

Common-Source



$$V_{in} = 0.8 + 0.001\sin(2\pi 100t) \quad (28)$$

Common-Source



$$V_{in} = 4.1 + 0.001\sin(2\pi 100t) \quad (29)$$