

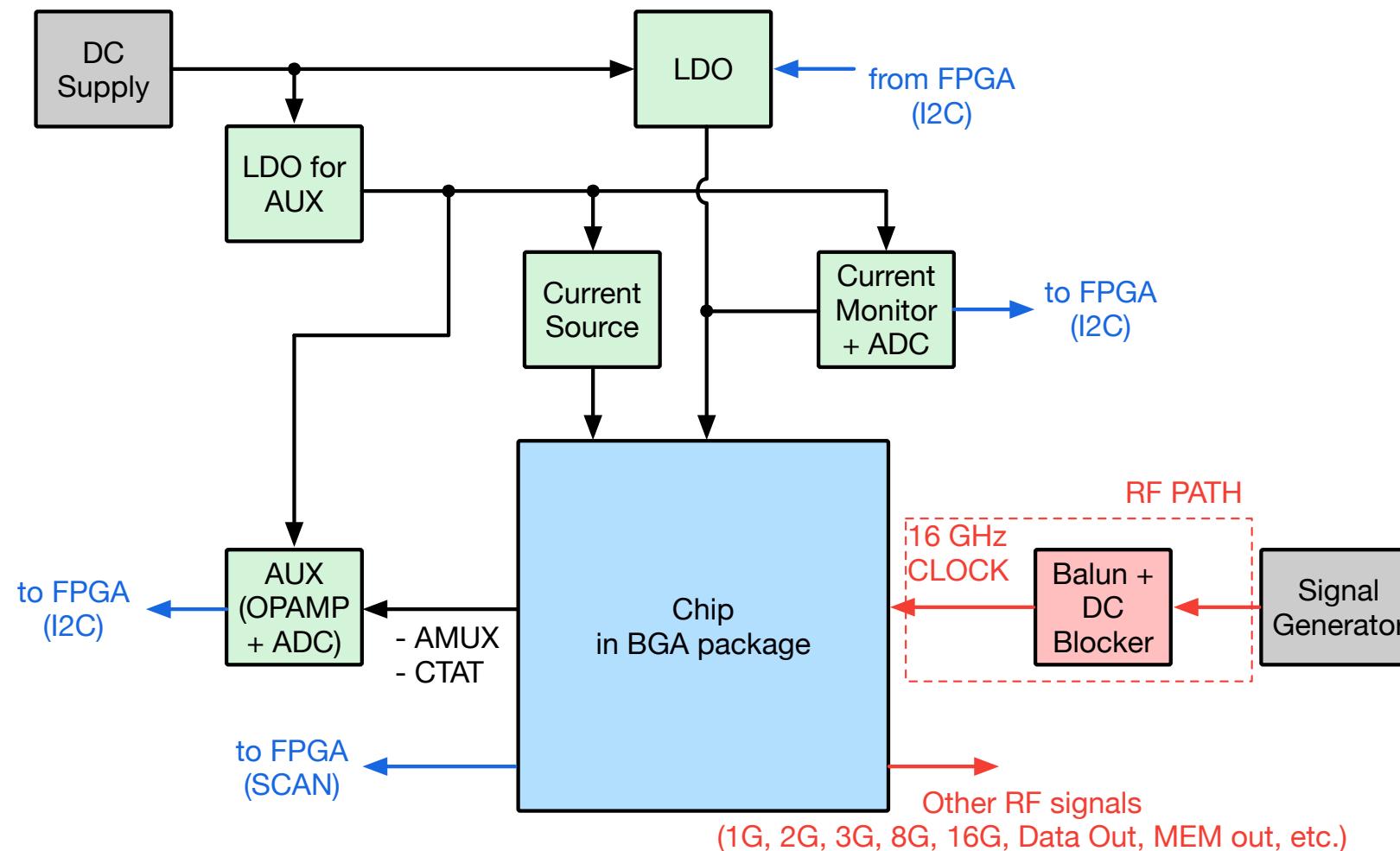
Test Plan for ADC-Based High- Speed SerDes Rx

Kunmo Kim

Outline

- Simplified Block Diagram
- Schematic Overview
 - Stack-Up & Laminate/Prepreg Material review
 - RF Path (On-board Balun + DC Blocker for 16 GHz Clock)
 - LDO (Main & AUX)
 - Current Source
- Appendix
 - SCAN signal (schematic + delay matching)
 - I2C MUX + Address Assignment
 - AUX Circuit (OPAMP + ADC for DC measurement)

Simplified Block Diagram

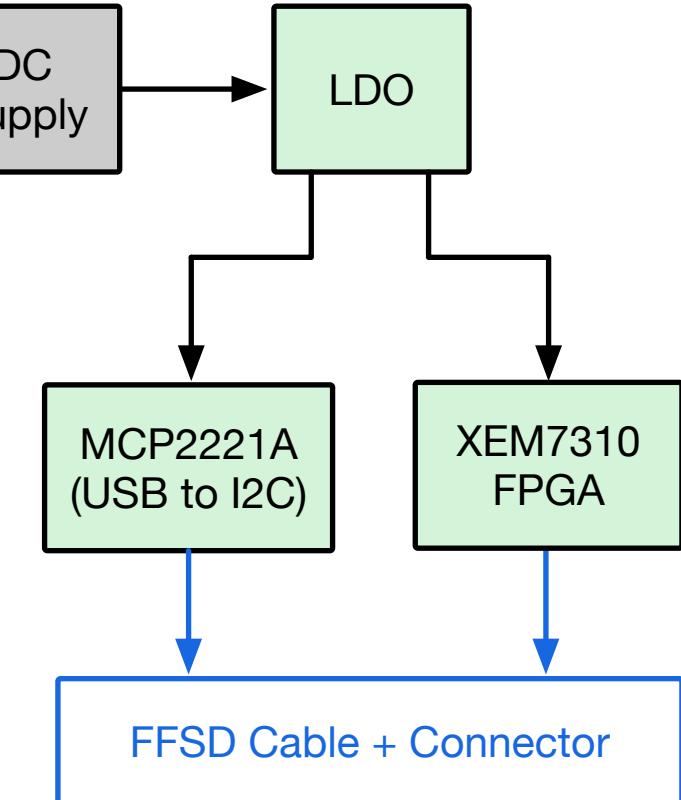


Mainboard

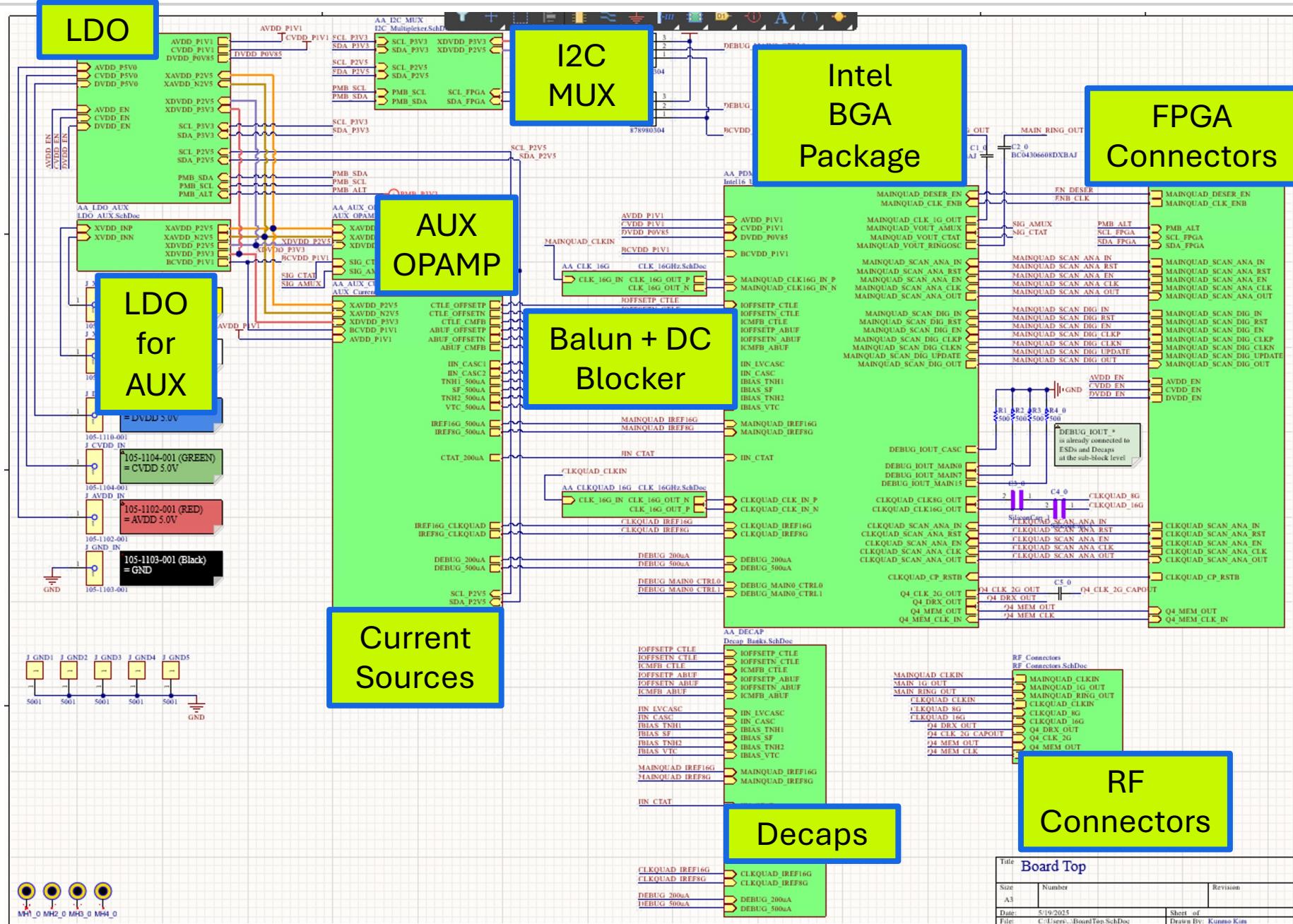
1G: retimer clock (divided by 4)
2G: DSP domain clock
2G: Ring OSC output
8G: CLKQUAD 8G out
16G: CLKQUAD 16G out

Data: 2Gbps deserialized data
MEM out: memory output (100 Mbps)

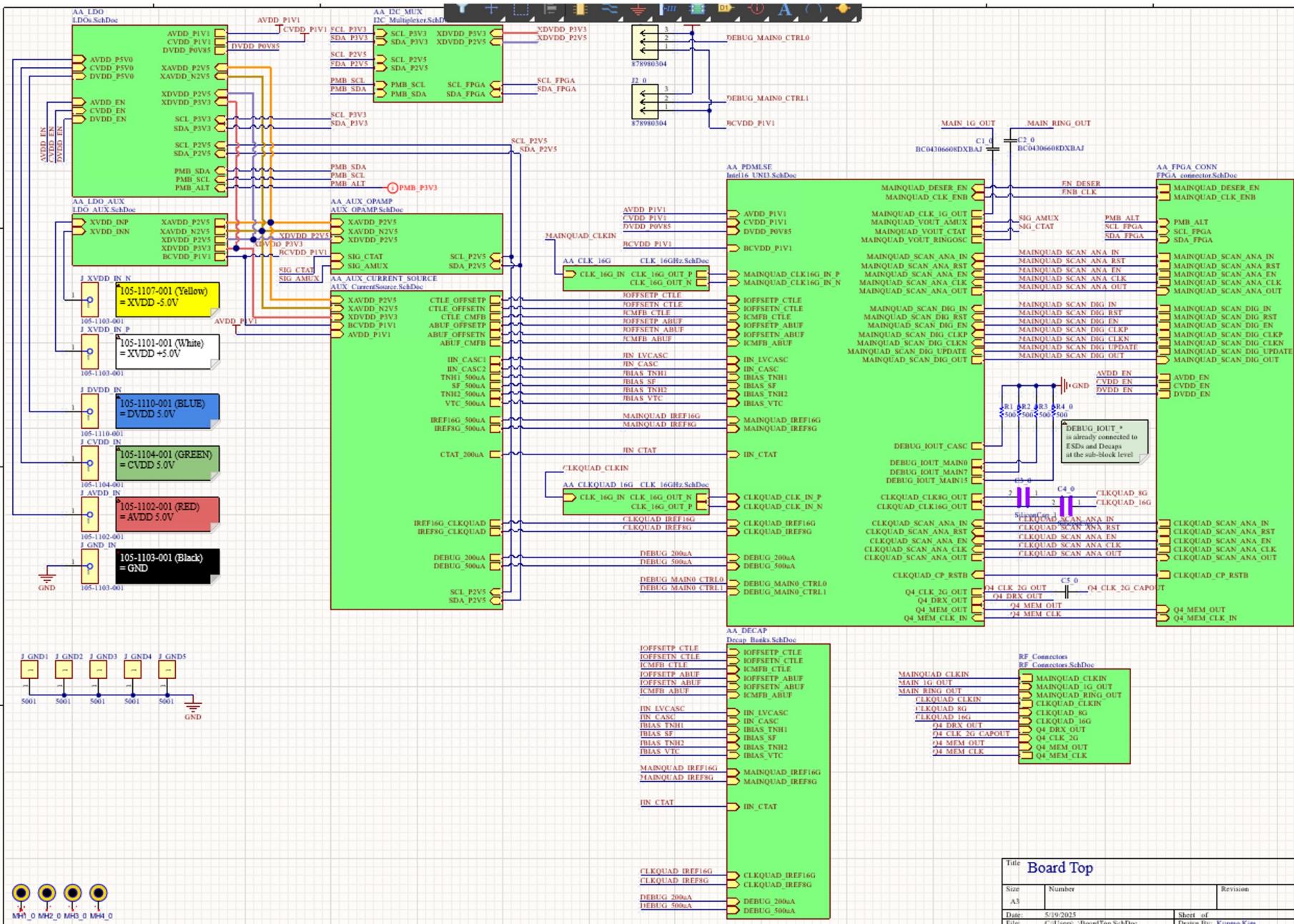
FPGA Breakout Board



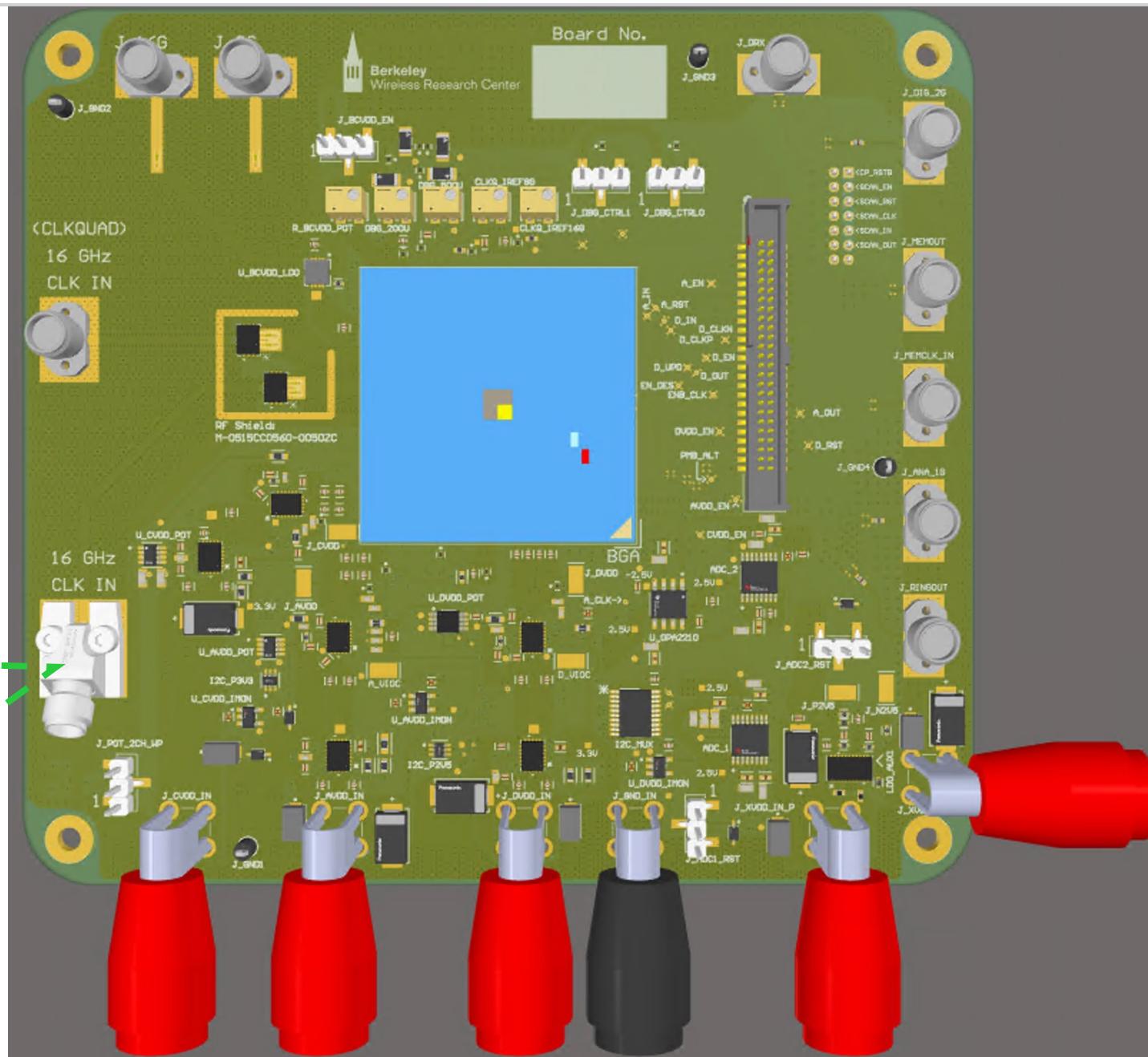
Main Board (Schematic)



Main Board (Schematic)

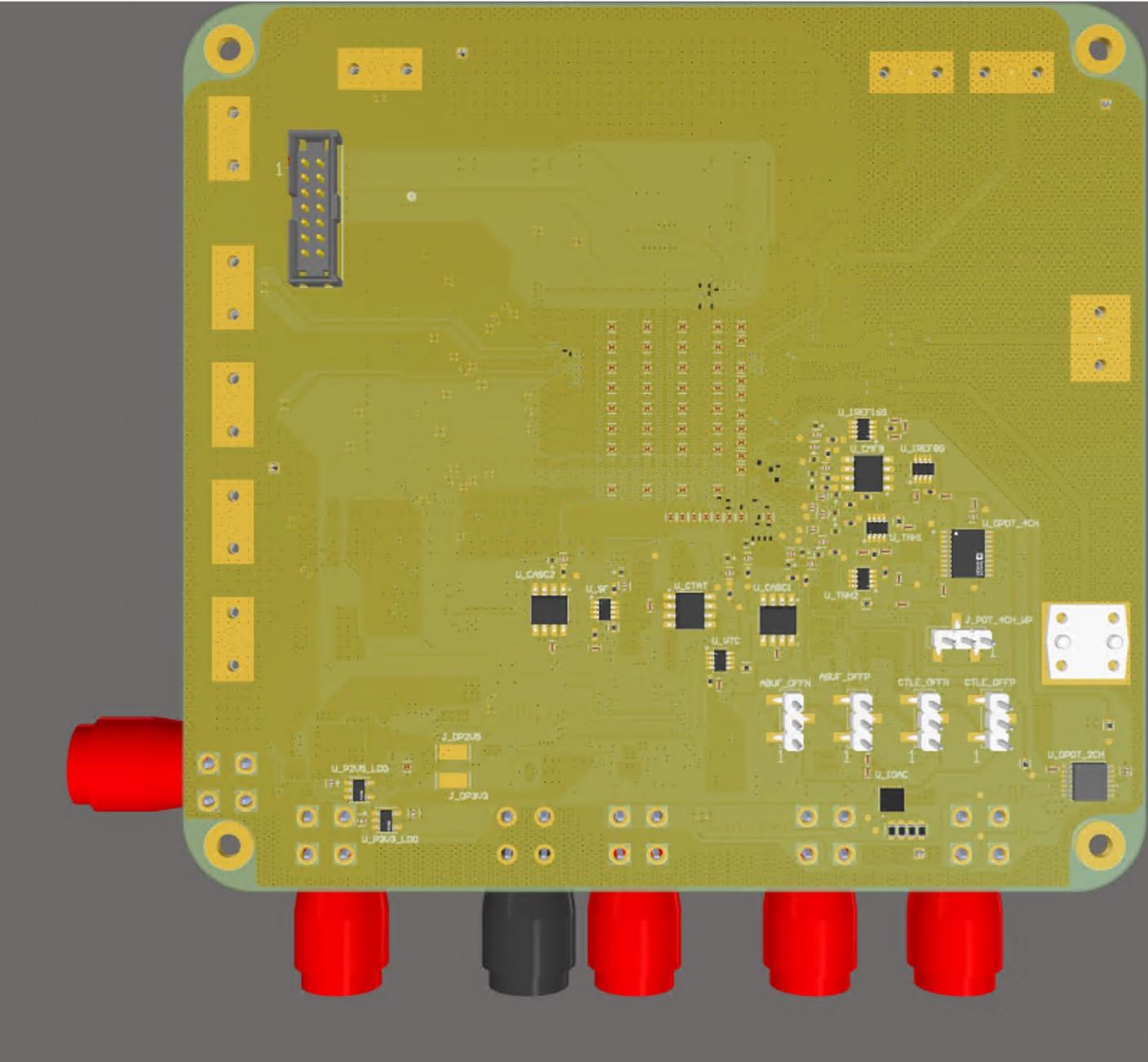


Main Board (Layout, 3D)



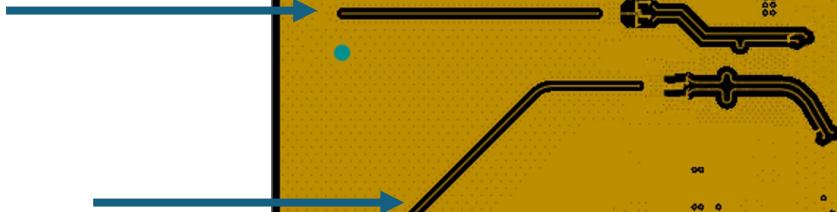
Main Board (Backside)

Mostly current sources, digipots, and IDAC



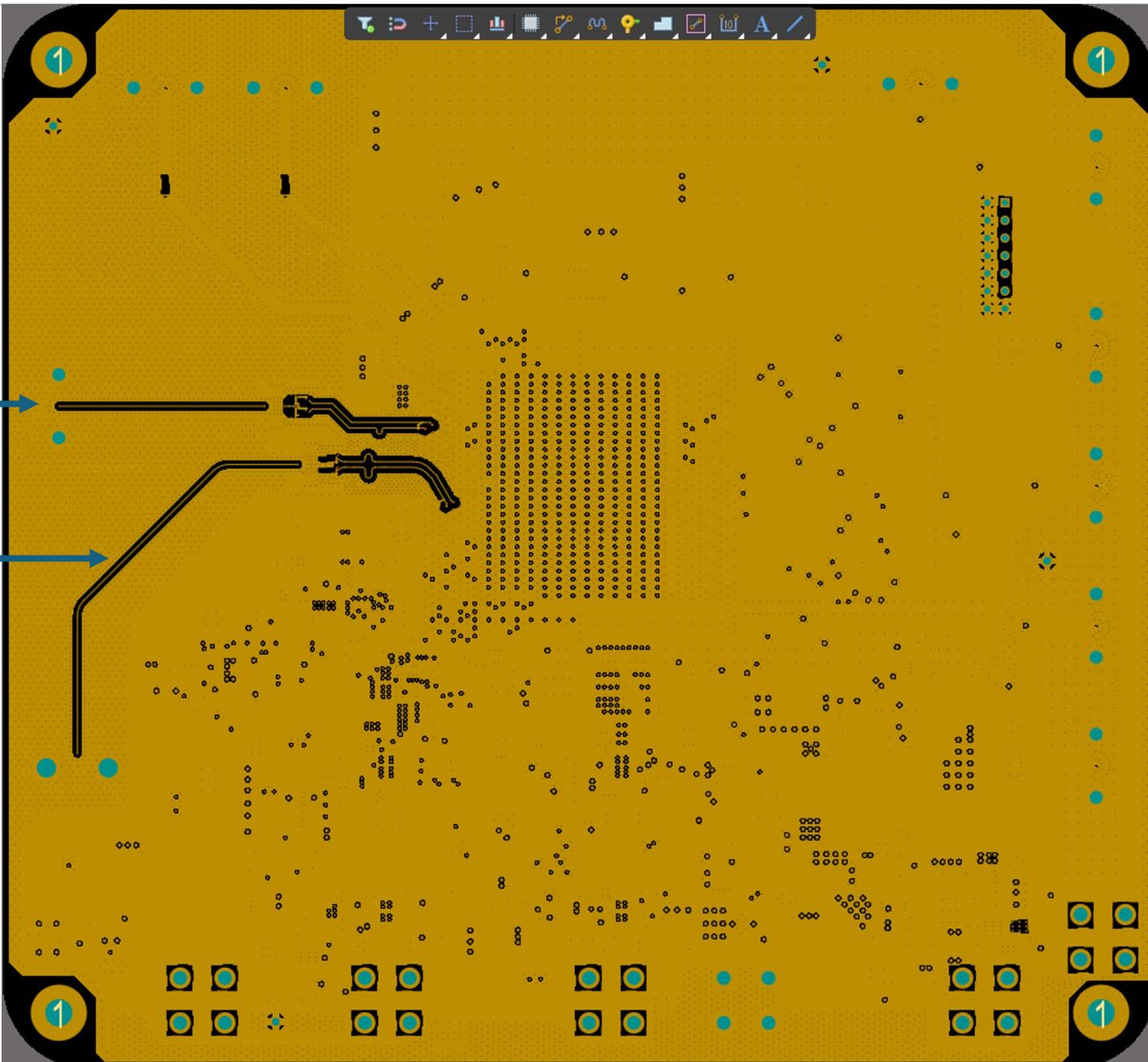
Main Board (Layout, 2D) – L2

16 GHz CLK for CLKQUAD testing



Main RF signal (16 GHz CLK).

Stripline is used to maximize isolation



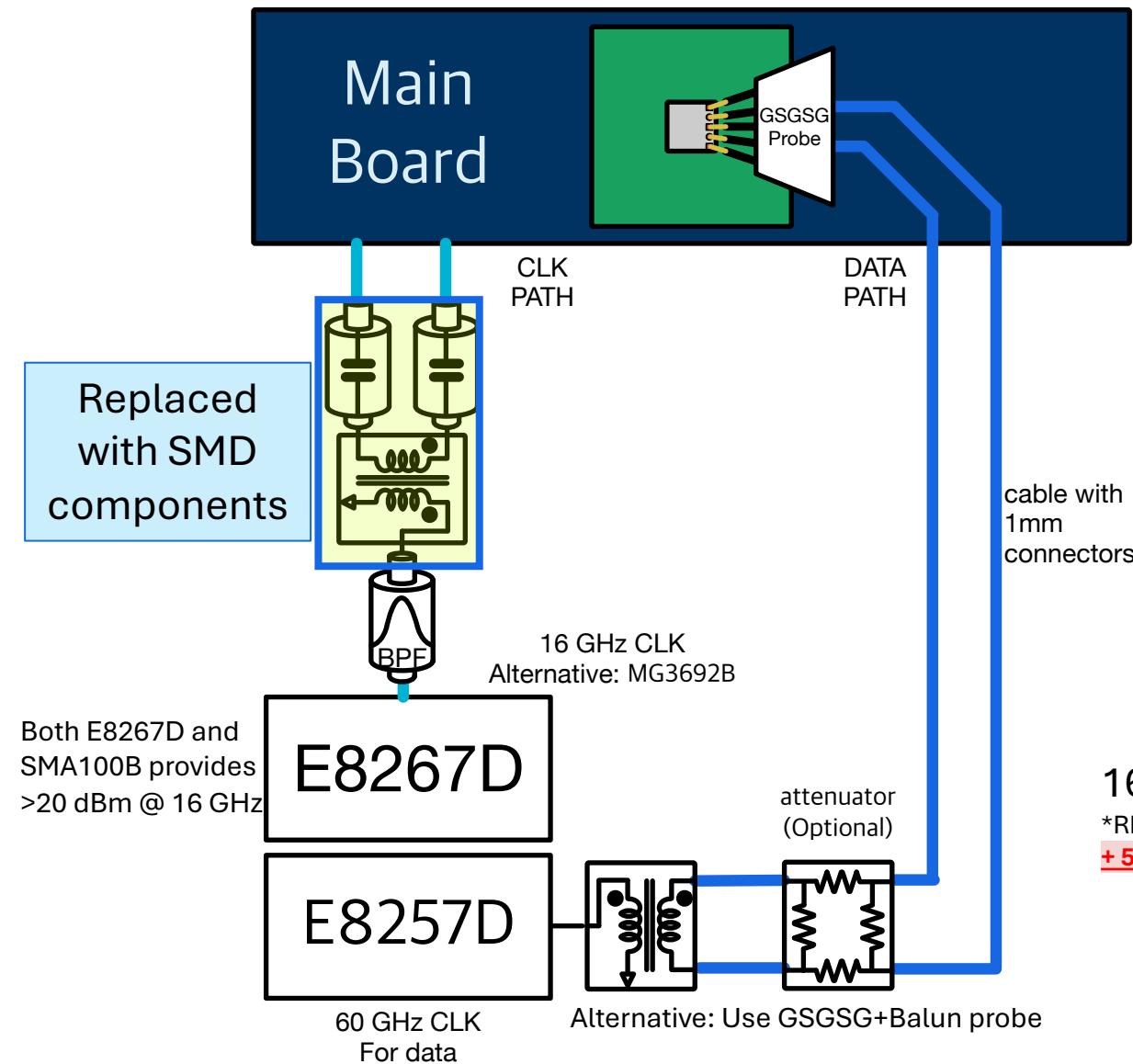
Stack-Up & Prepreg/Laminate Materials

Stack-Up

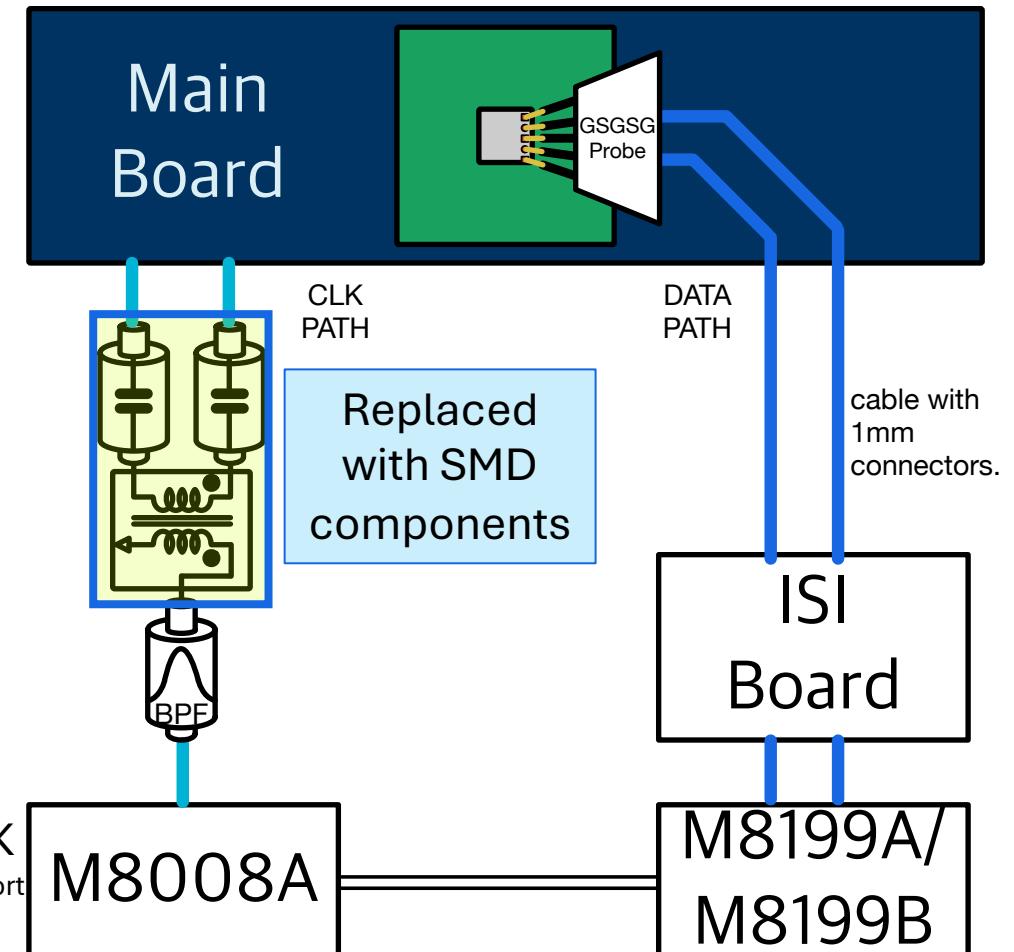
RF Path

Test Plan

1. Testing with CLK pattern



2. Testing with AWG



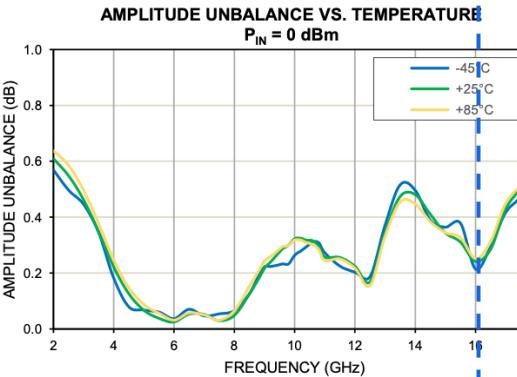
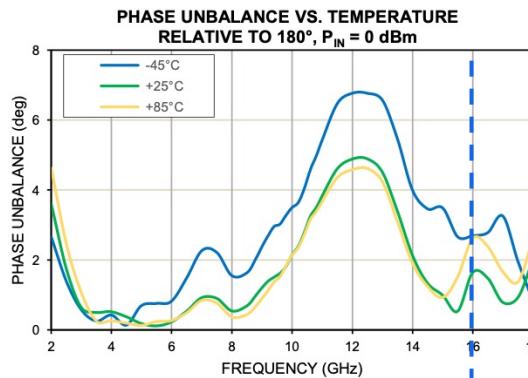
Balun Selection

* 1:2 Impedance Ratio Balun only

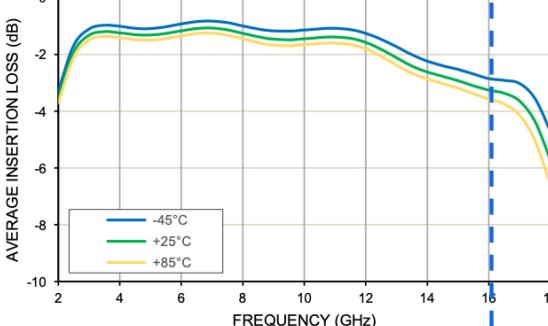
Balun Selection (MiniCircuit On-Board Balun)

- Phase Imbalance
 - MTX2-183+: $\sim 2^\circ$
 - ABSD-10168: $\sim 0.2^\circ$
- Amplitude Imbalance
 - MTX2-183+: ~ 0.2 dB
 - ABSD-10168 : ~ 0.1 dB
- Insertion Loss
 - MTX2-183+: -6.5 dB
 - ABSD-10168 : +6 dB

MTX2-183+

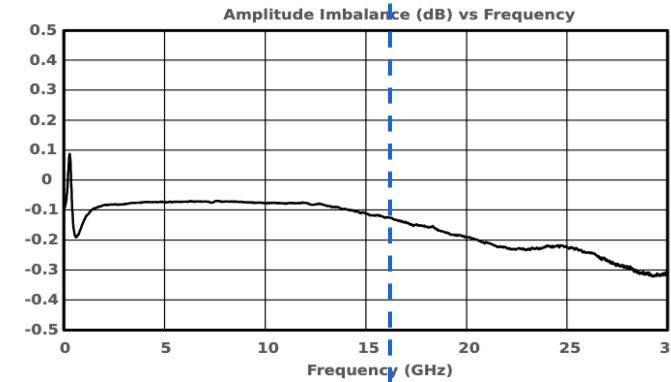
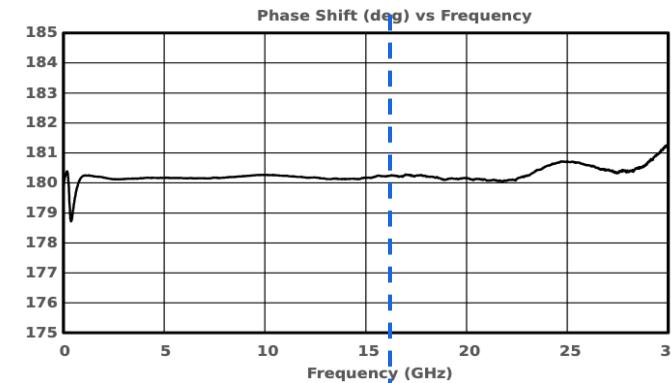


AVERAGE INSERTION LOSS VS. TEMPERATURE
ABOVE 3 dB THEORETICAL, $P_{IN} = 0$ dBm

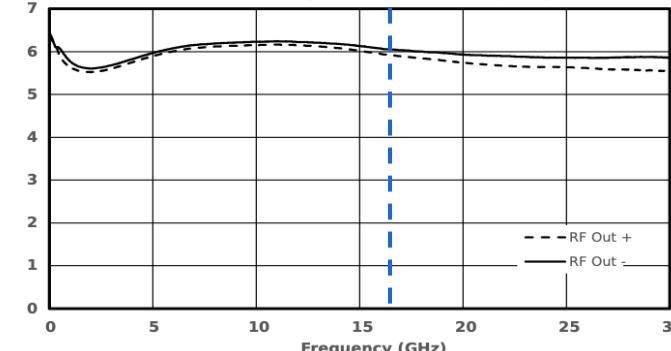


(Marki's On-Board Balun)

ABSD-10169PSM



Small Signal Gain (dB) vs Frequency



DC Blocker Selection

939114492510-T3S

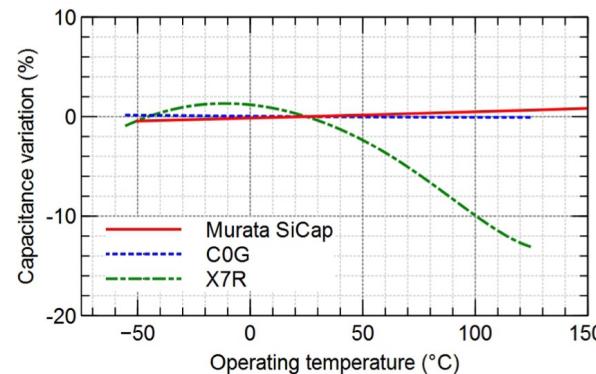
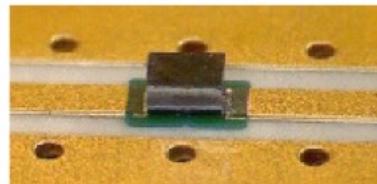


Fig. 1: Capacitance variation vs temperature
(for BBSC and MLCC technologies)

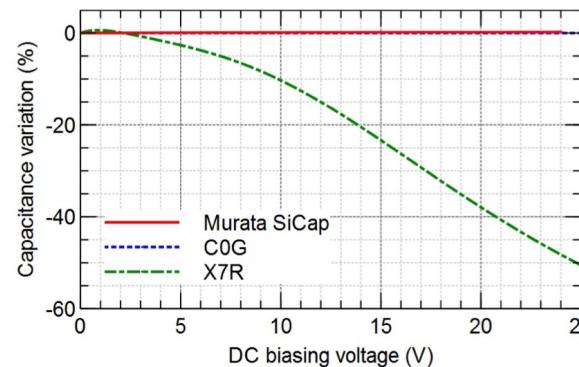


Fig.2: Capacitance variation vs DC biasing voltage
@ BV30 (for BBSC and MLCC technologies)

- 0201-size silicon cap DC Blocker from Murata
- Mainly used for 16 GHz CLK path

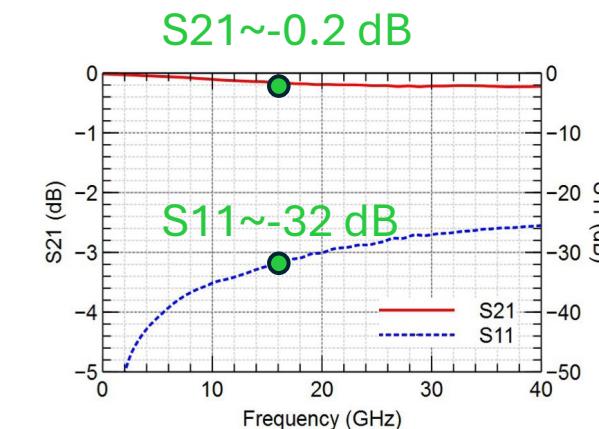
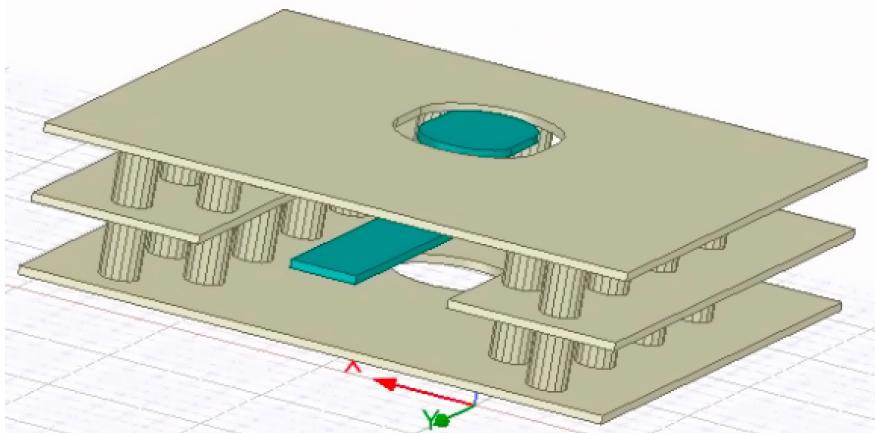


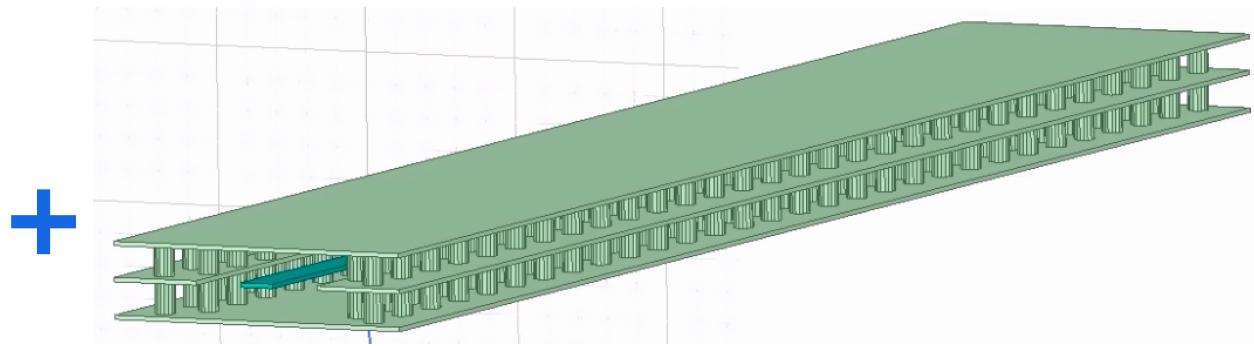
Fig.3: 10 nF/0201 BBSC @ BV30 measurement
results (S-parameters in transmission mode)

FREE S-Parameters-Based Linear Simulation Models for
ADS: <http://www.modelithics.com>

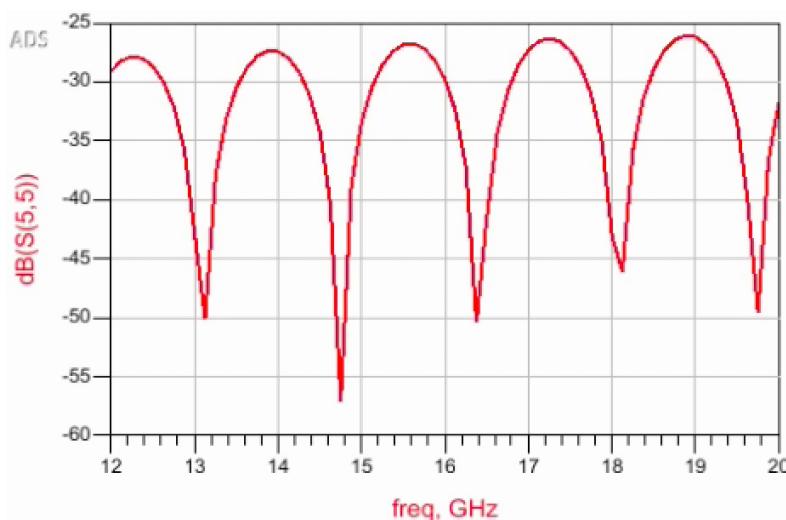
Simulation Results (K-Connector to Balun)



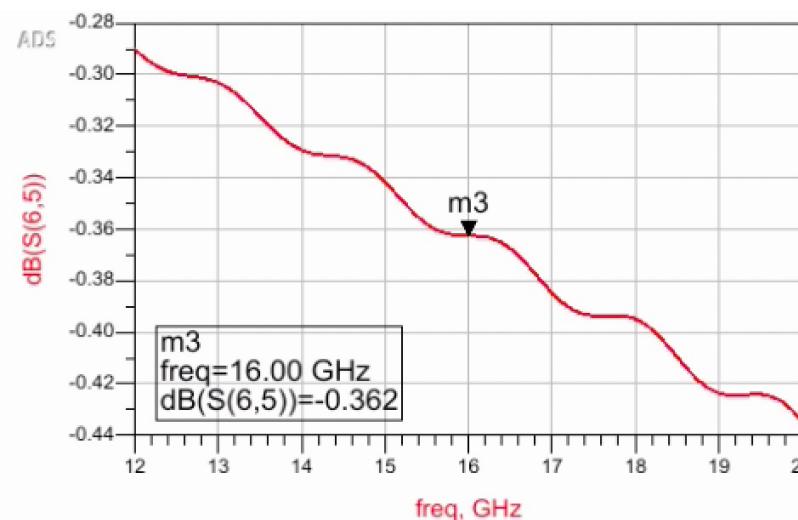
K Conn -> SL transition (x2)



600 mils SL x3 -> 1800 mils (4.57 cm)

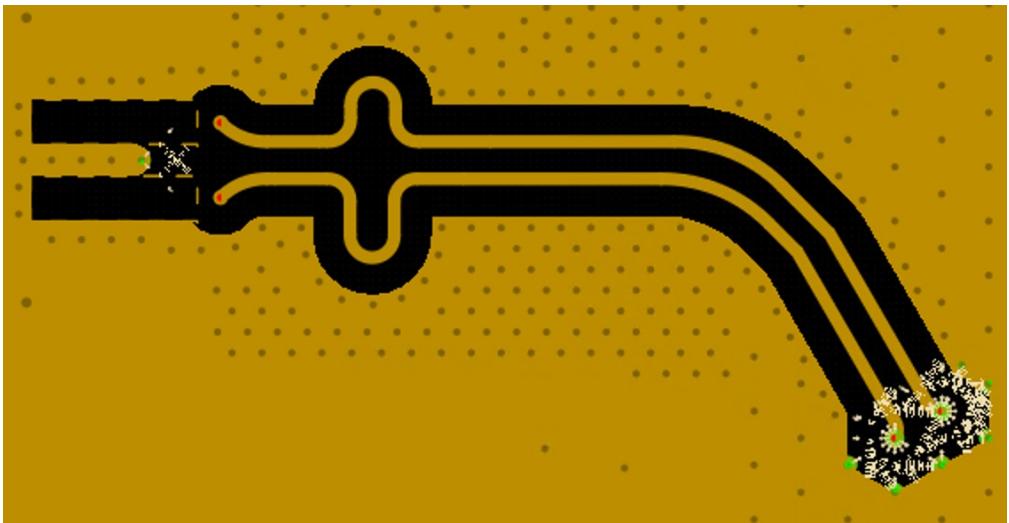


- Surface roughness included.
 - Radius = 0.5 μ m, Area Ratio = 4.4

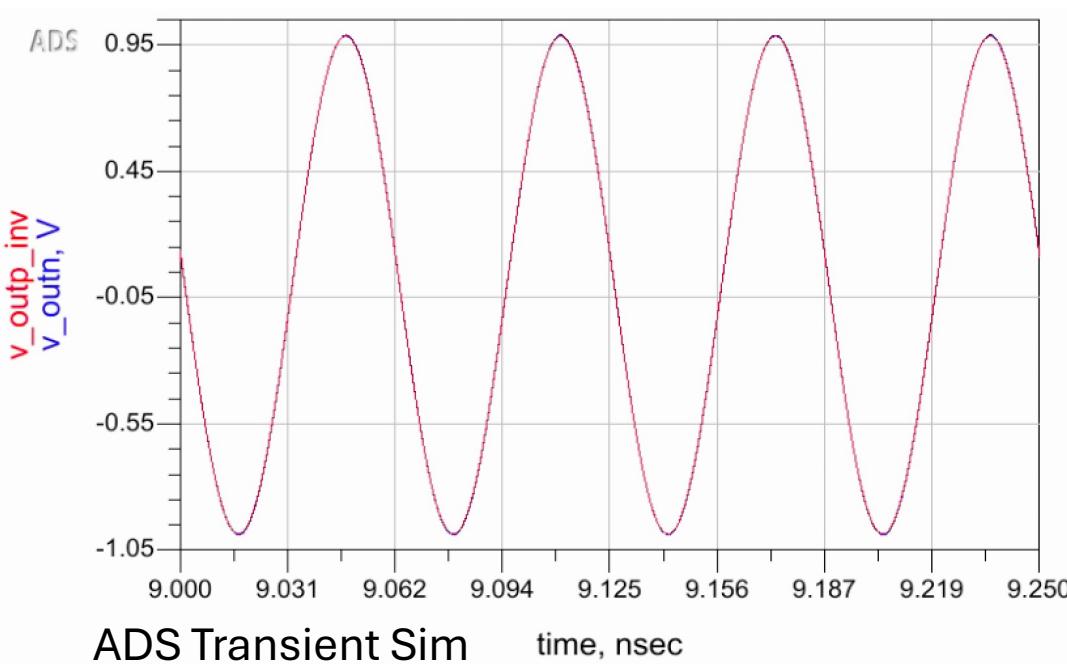
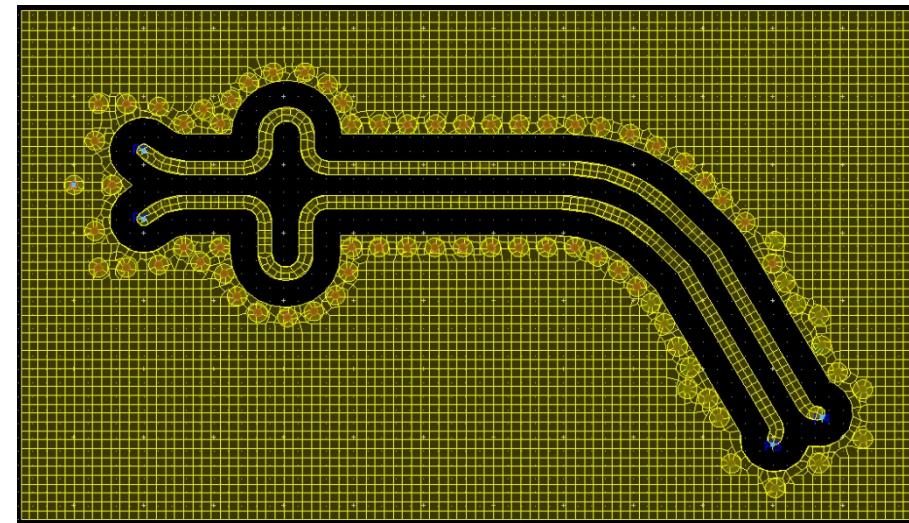


Simulation Results (Balun to UNI3 Package)

Altium Layout



ADS Momentum Microwave EM Sim

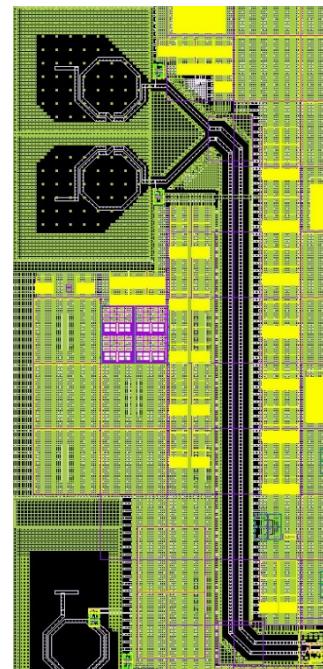
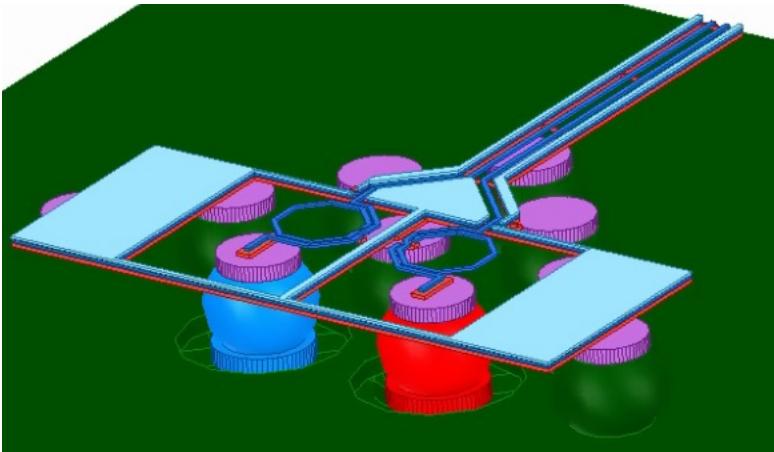
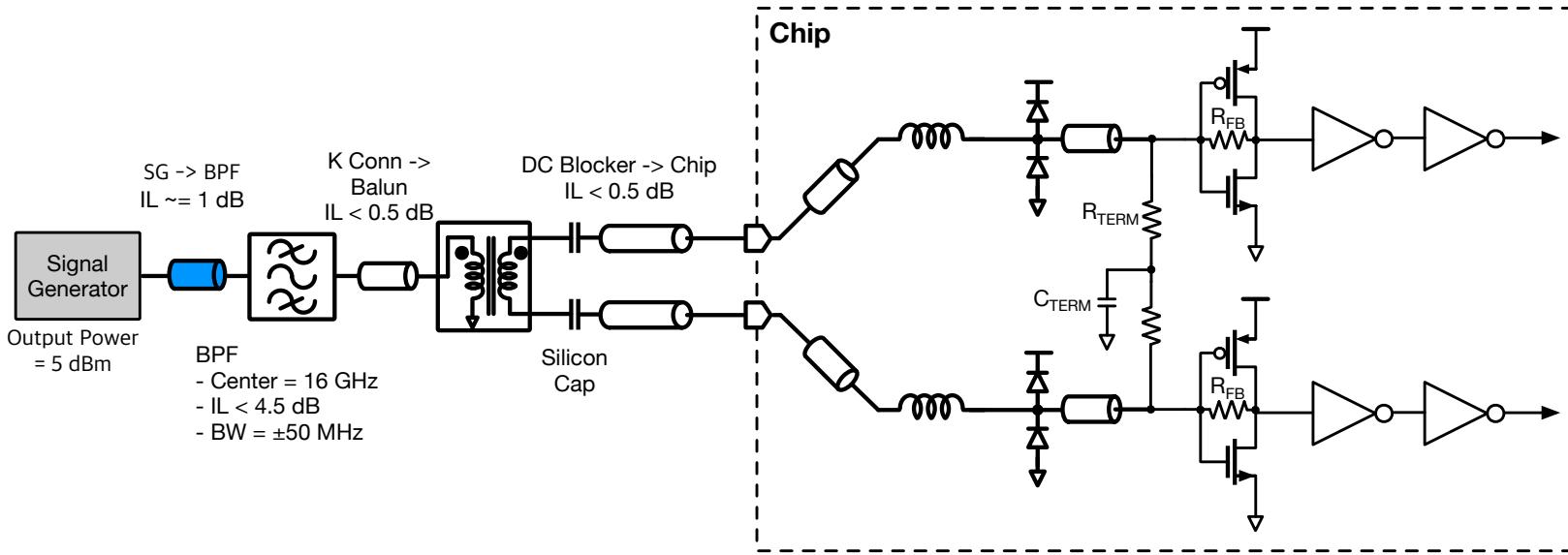


Altium Differential Pair Editor

2 Nets (0 Highlighted)				
Name	Node Cou...	Signal Length (mil)	Routed Length (mil)	Delay (ps)
CLK_16G_IN_N (-)	2	677.67	675.208	100.261
CLK_16G_IN_P (+)	2	677.642	675.179	100.256

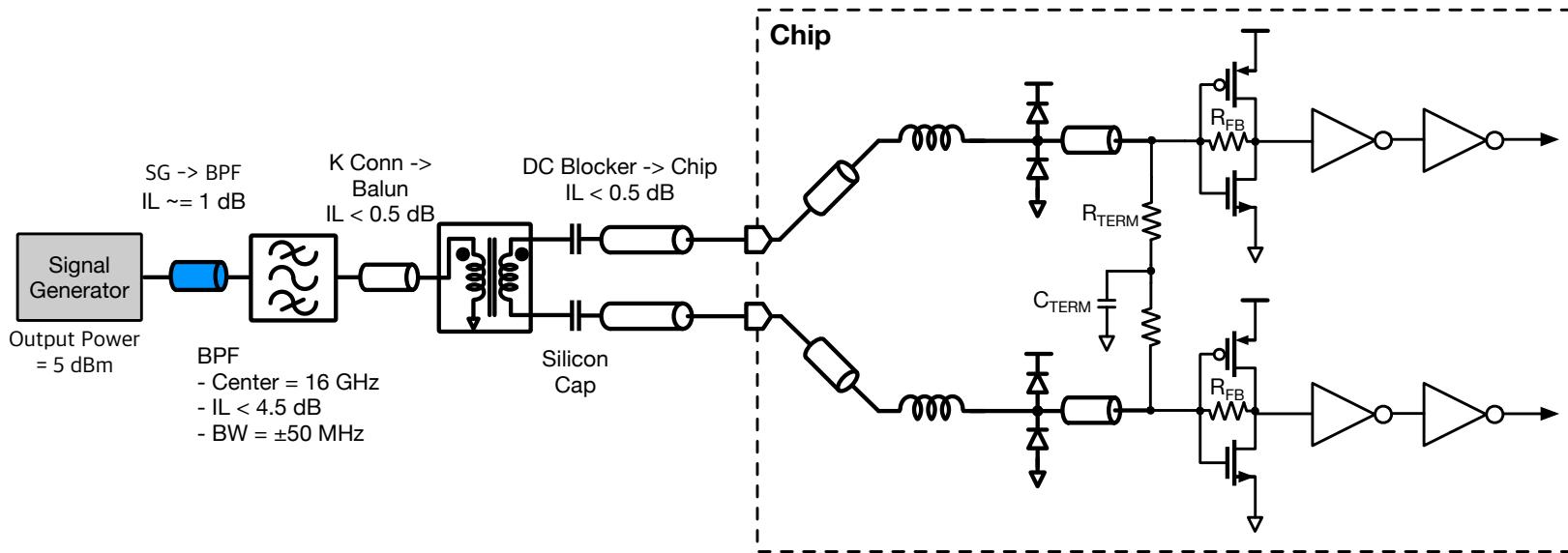
- Verified using both Altium's Differential Pair length check tool & ADS
- almost 180° phase shift between 'P' and 'N' side.

Simulation Results (Transient)



- HFSS model includes both the package-to-chip interface and on-chip transmission line (not shown)

Simulation Results (Transient)

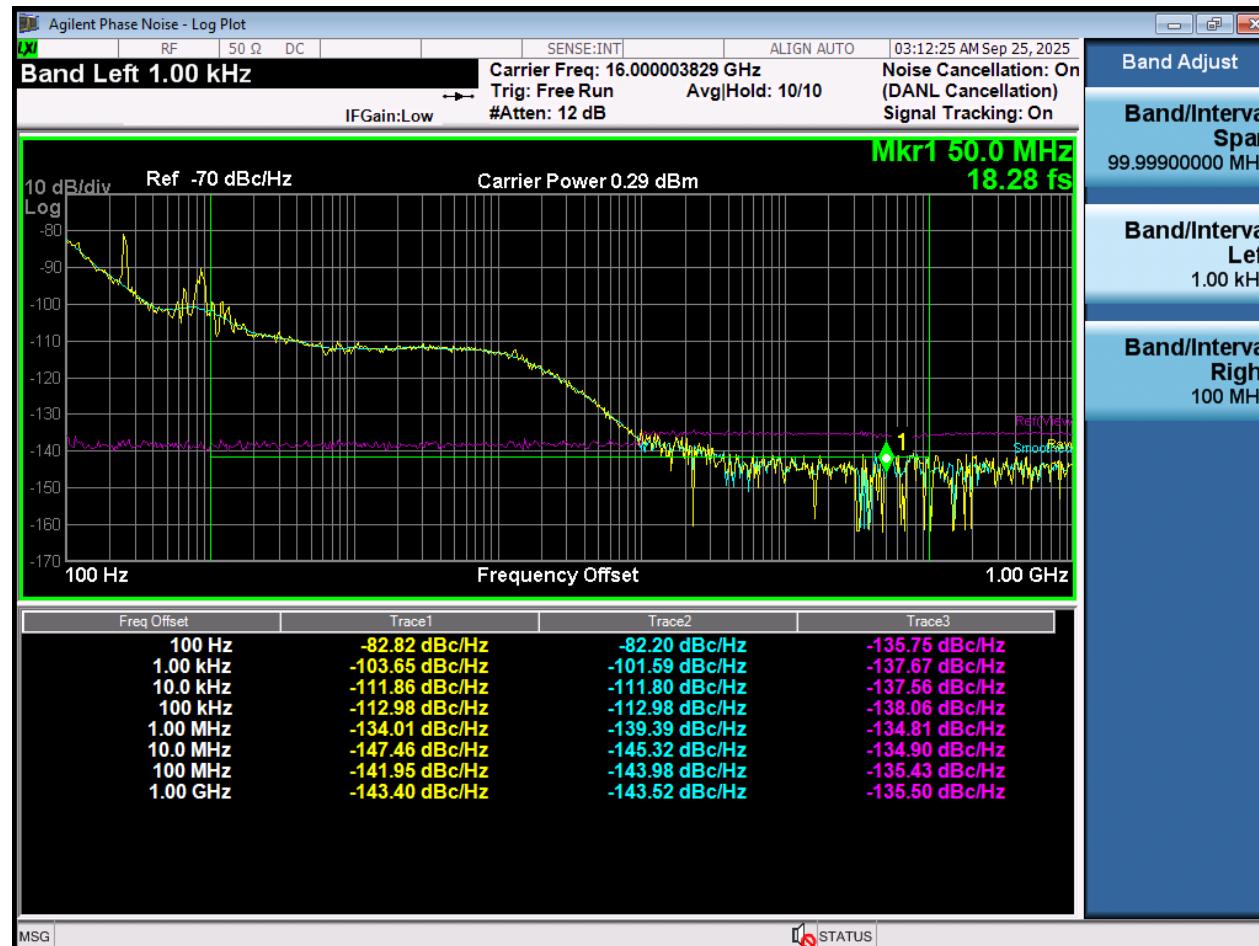


	Passive Balun MTX2-183+	Active Balun ABSD-10169PSM
Average Duty Cycle	49.41 %	50 %
Timing Skew between P&N	2 ps	0.508 ps
Voltage Swing @ TIA Input	163/171 mV (P&N)	998.7/985.2 mV

Simulation Results (PSS + PNOISE)

	Ideal Source + -3dBm Power + TIA	Ideal Source +3dBm Power + TIA	Phase noise profile + -3dBm power + TIA	Phase noise profile + +3dBm power + TIA
J_{ee} jitter (rms)	13.3 fs	8.1 fs	85.7 fs	91.5 fs

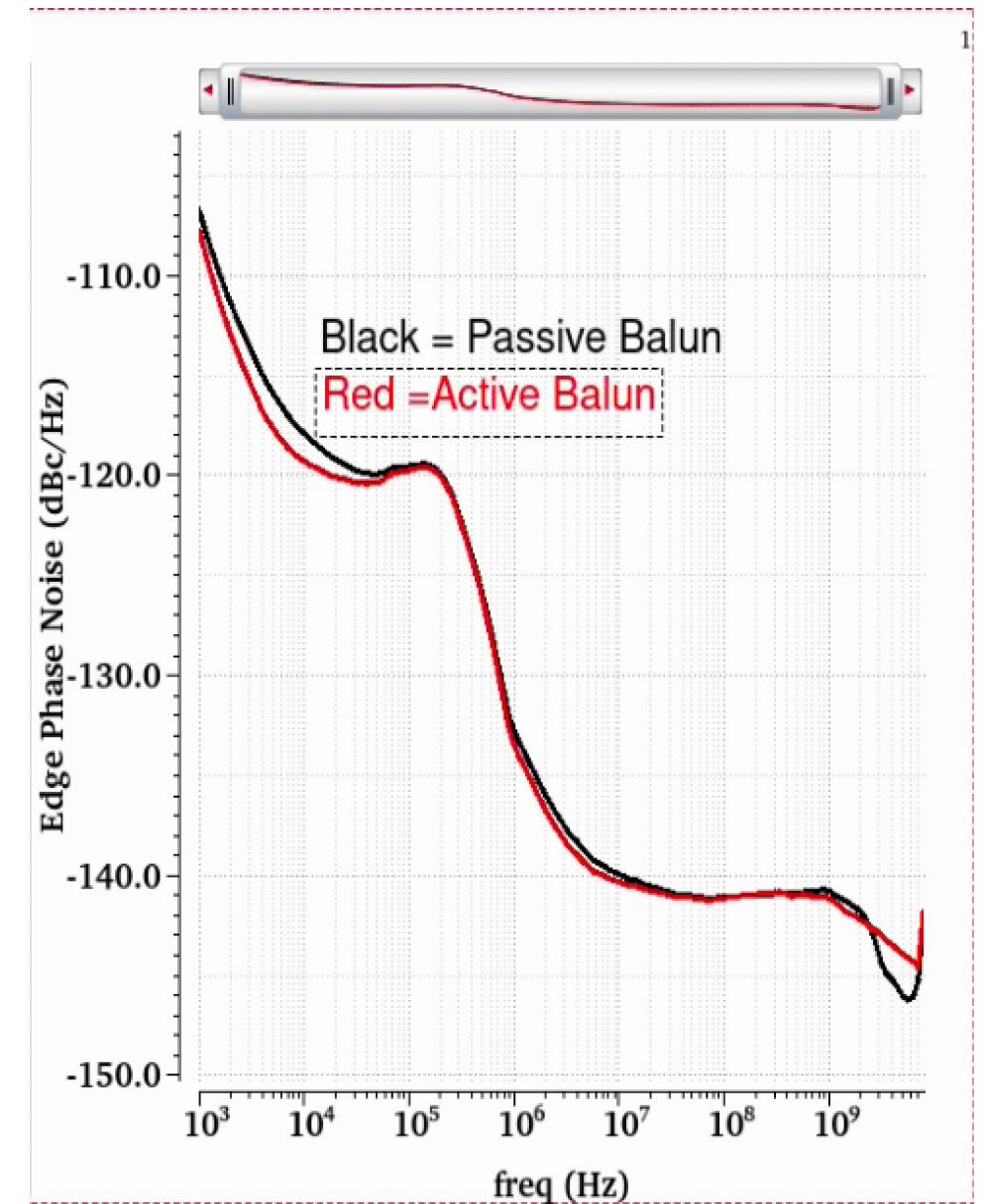
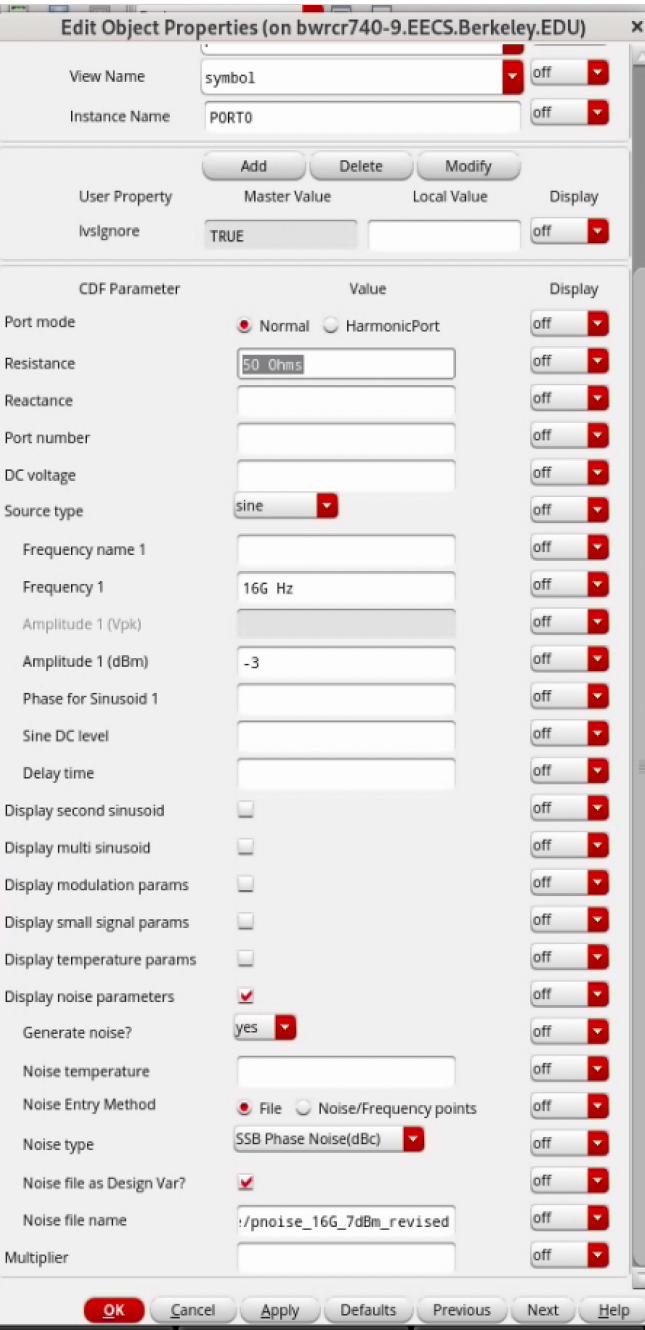
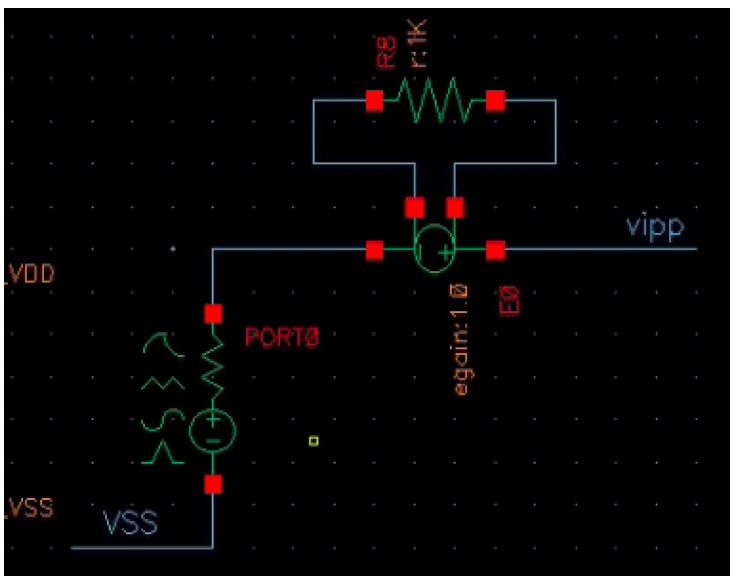
Source: E8267D
Analyzer: N9030A (SA)



Active Balun won't help much

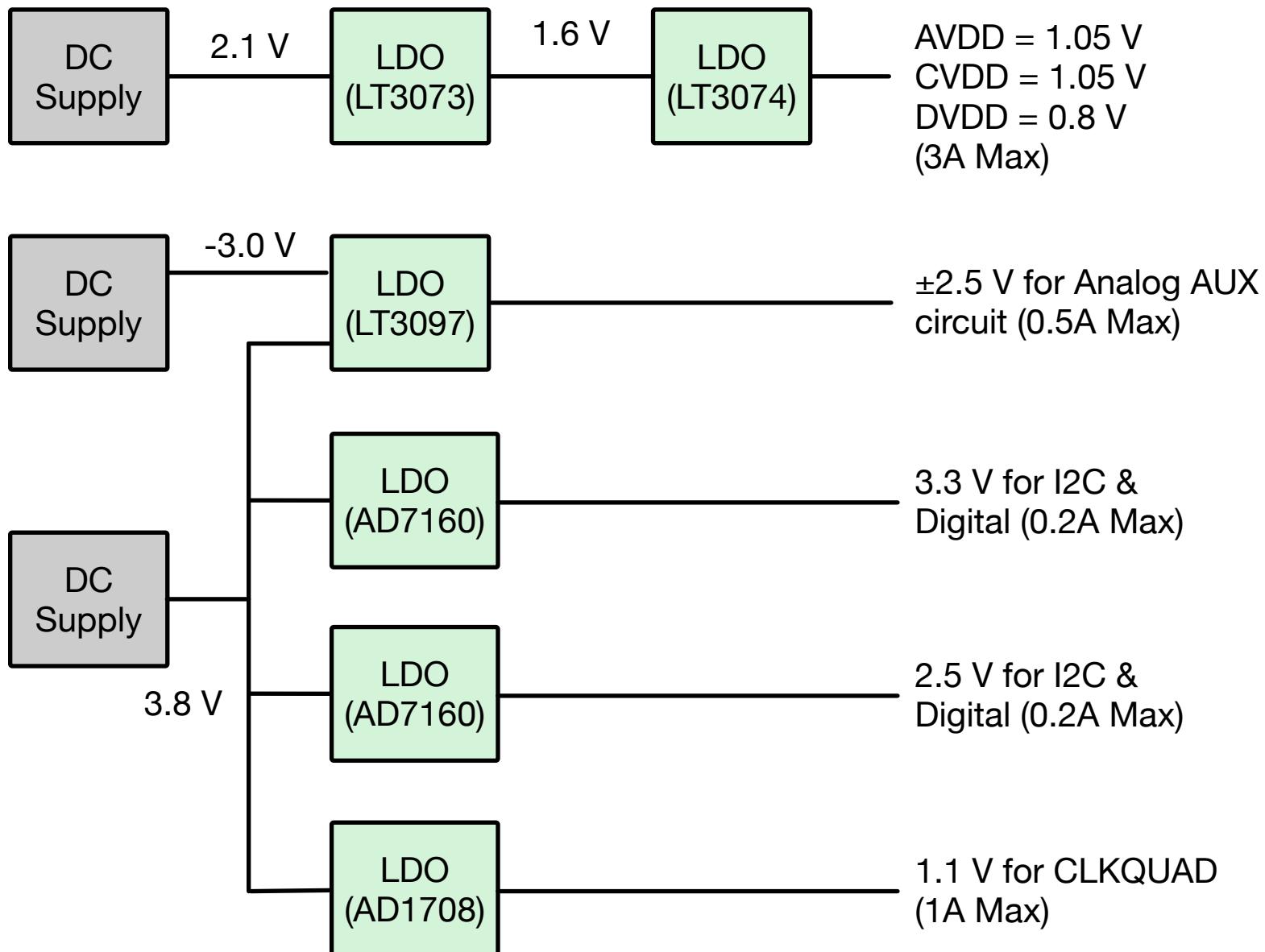
phase noise profile used for 'pnoise' simulation.

Simulation Setup (PSS + PNOISE)

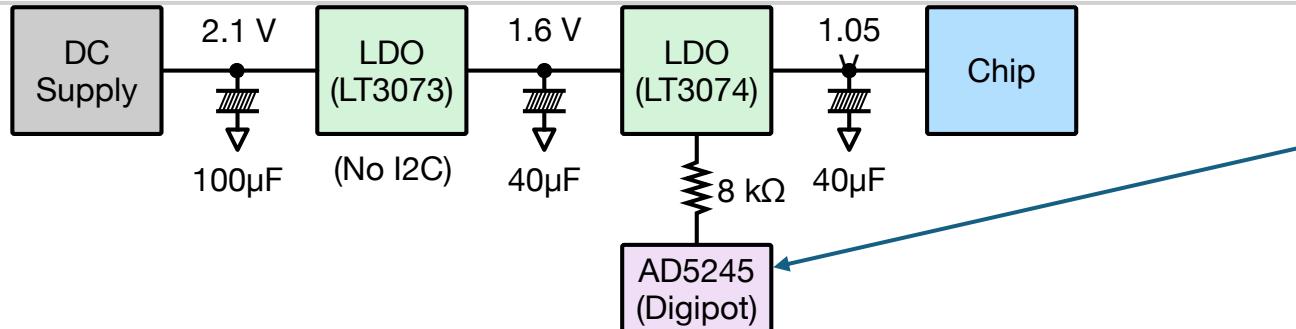


Power Management

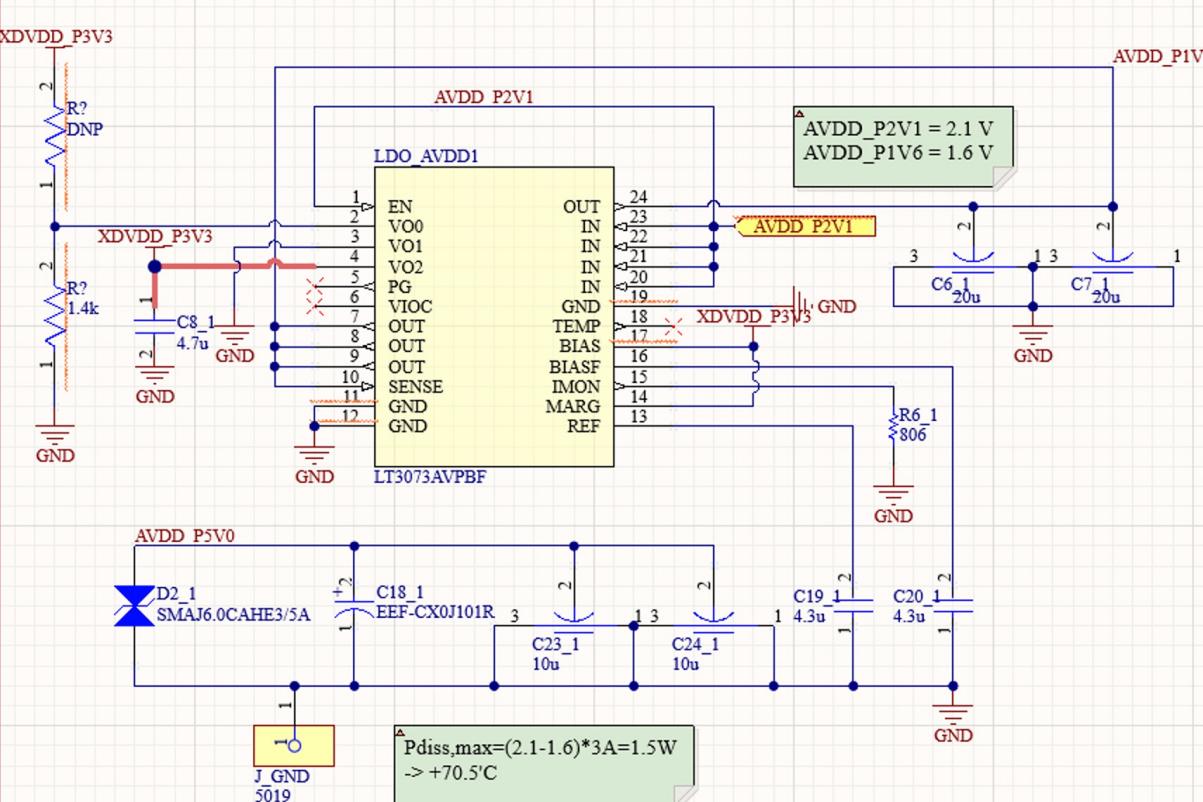
Main Board Power Distribution



Cascaded LDO

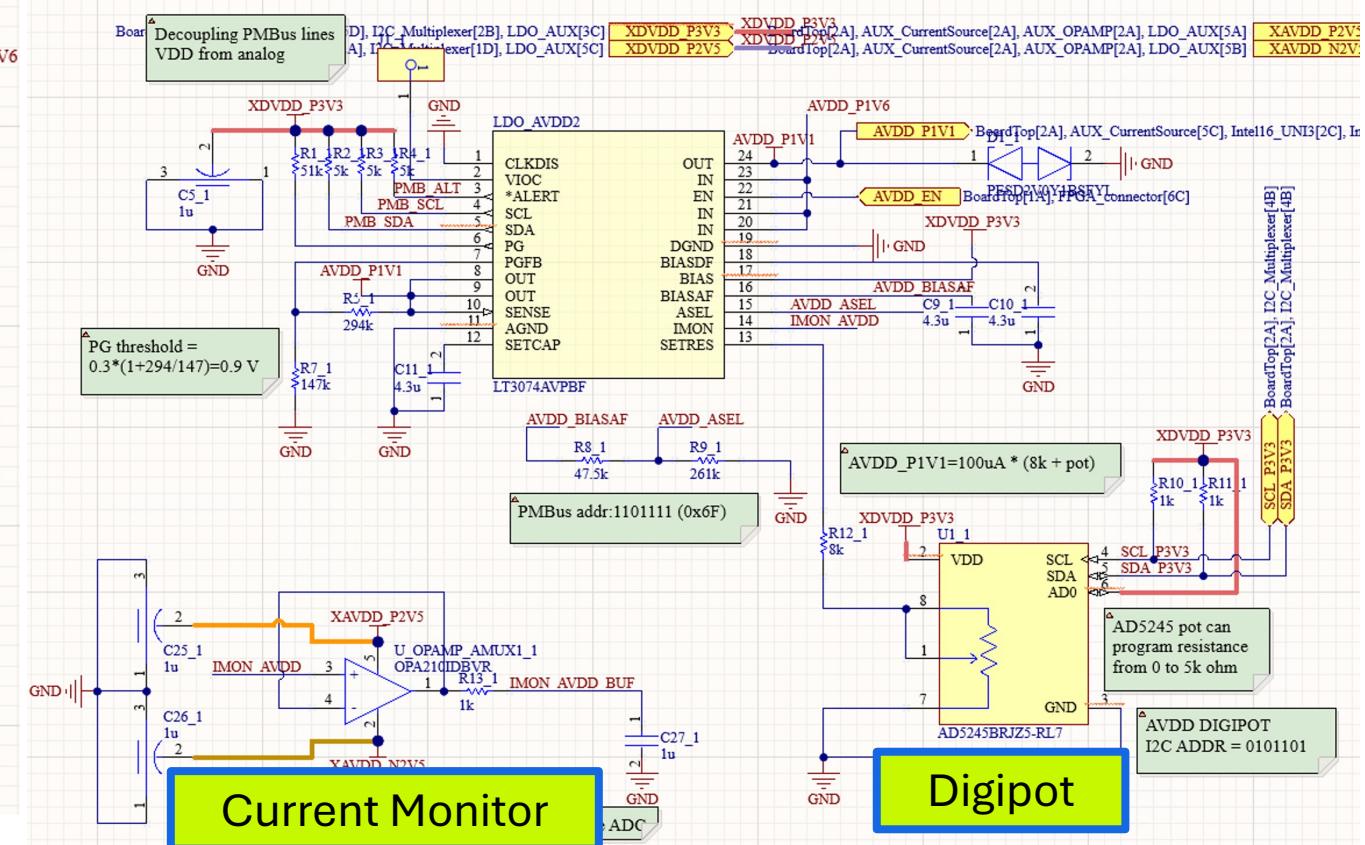


1st LDO (2.1 V \rightarrow 1.6 V), 3A Max

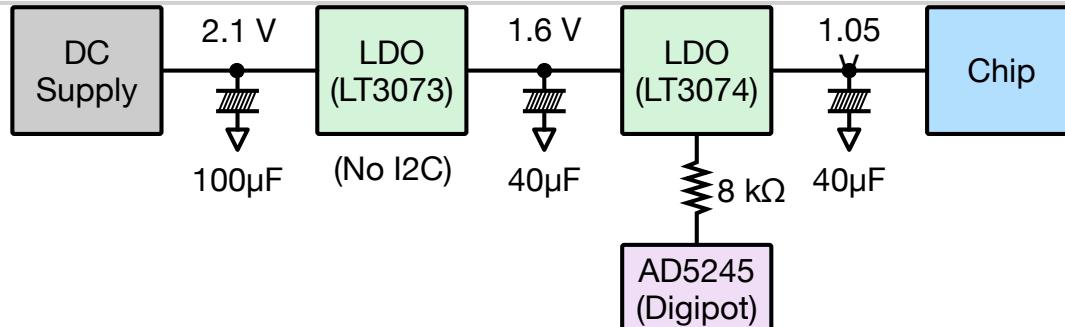


- AD5245 for AVDD & CVDD
- MCP4551 (Maxim's Digipot) for DVDD due to limited I2C address AD5245 has

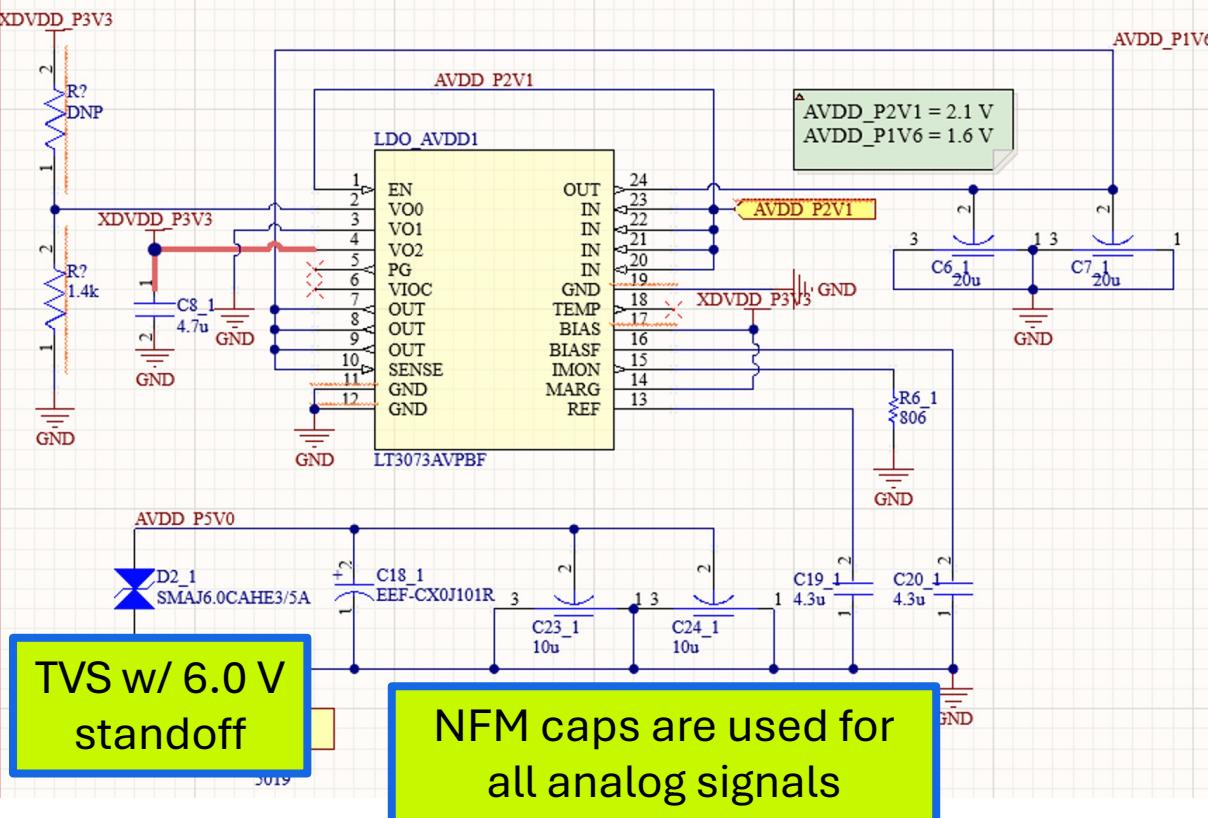
2nd LDO (1.6 V \rightarrow 1.1 V), 3A Max



Cascaded LDO

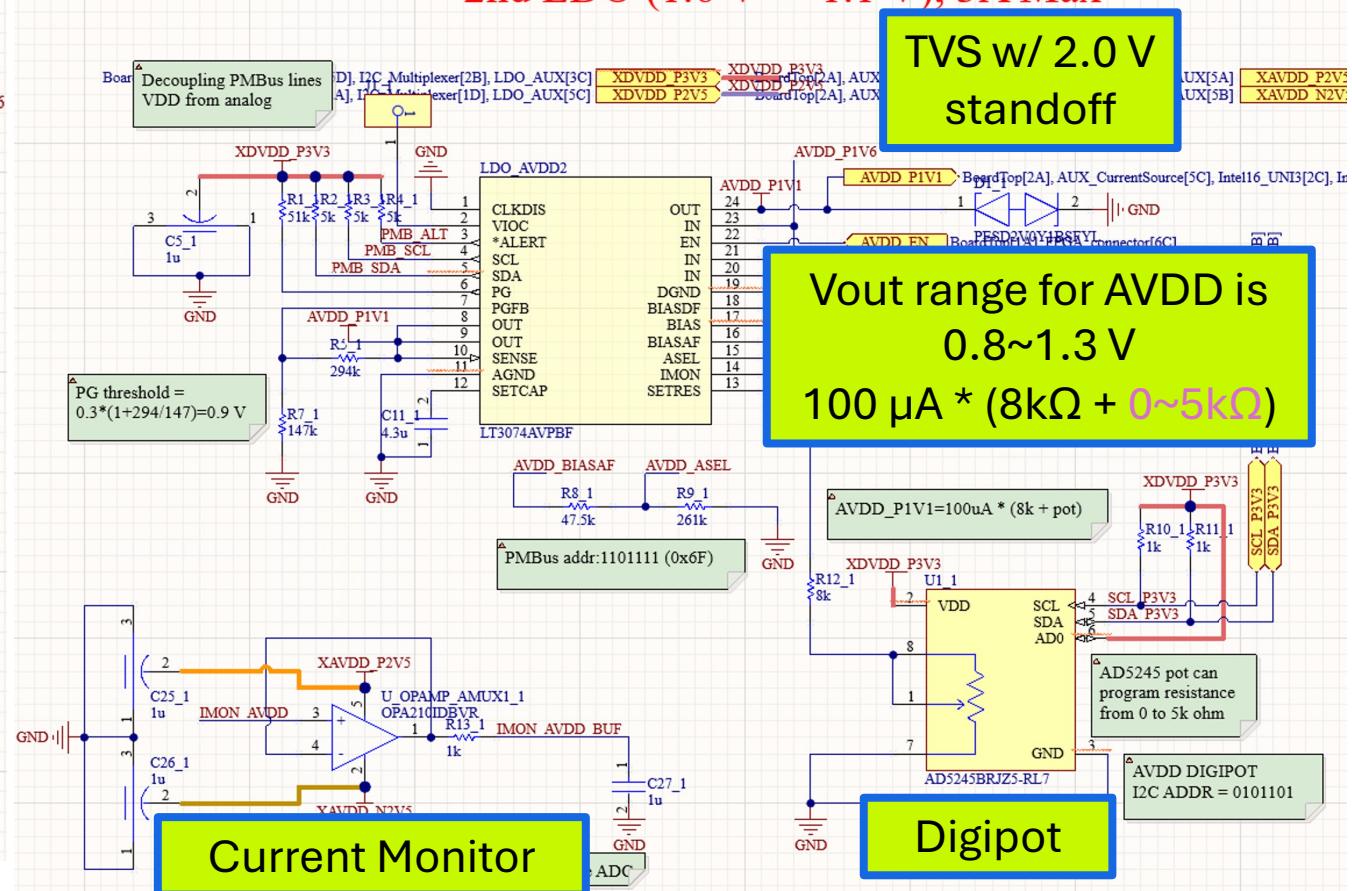


1st LDO (2.1 V \rightarrow 1.6 V), 3A Max

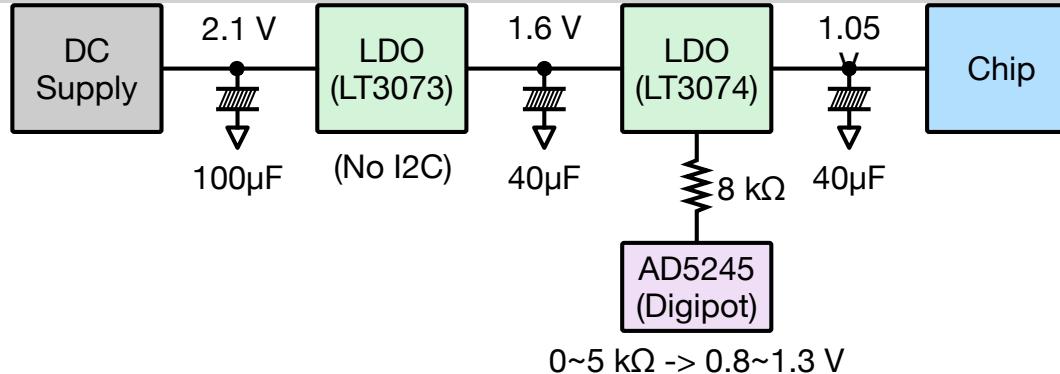


- Extra decaps are placed underneath of BGA
 - 6µF for AVDD (6x 1µF)
 - 4µF for CVDD (4x 1µF)
 - 20µF for DVDD (20x 1µF)
 - all NFM caps

2nd LDO (1.6 V \rightarrow 1.1 V), 3A Max



Cascaded LDO (Thermal Consideration)



Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Table 3. Thermal Resistance

PACKAGE TYPE ¹	θ_{JA}	θ_{JCTOP}	θ_{JCBOT}	UNIT
22-LEAD 3mm x 4mm LQFN	33	47	3.5	°C/W

¹ θ values are determined per JESD51. θ_{JA} value is obtained with demo board.

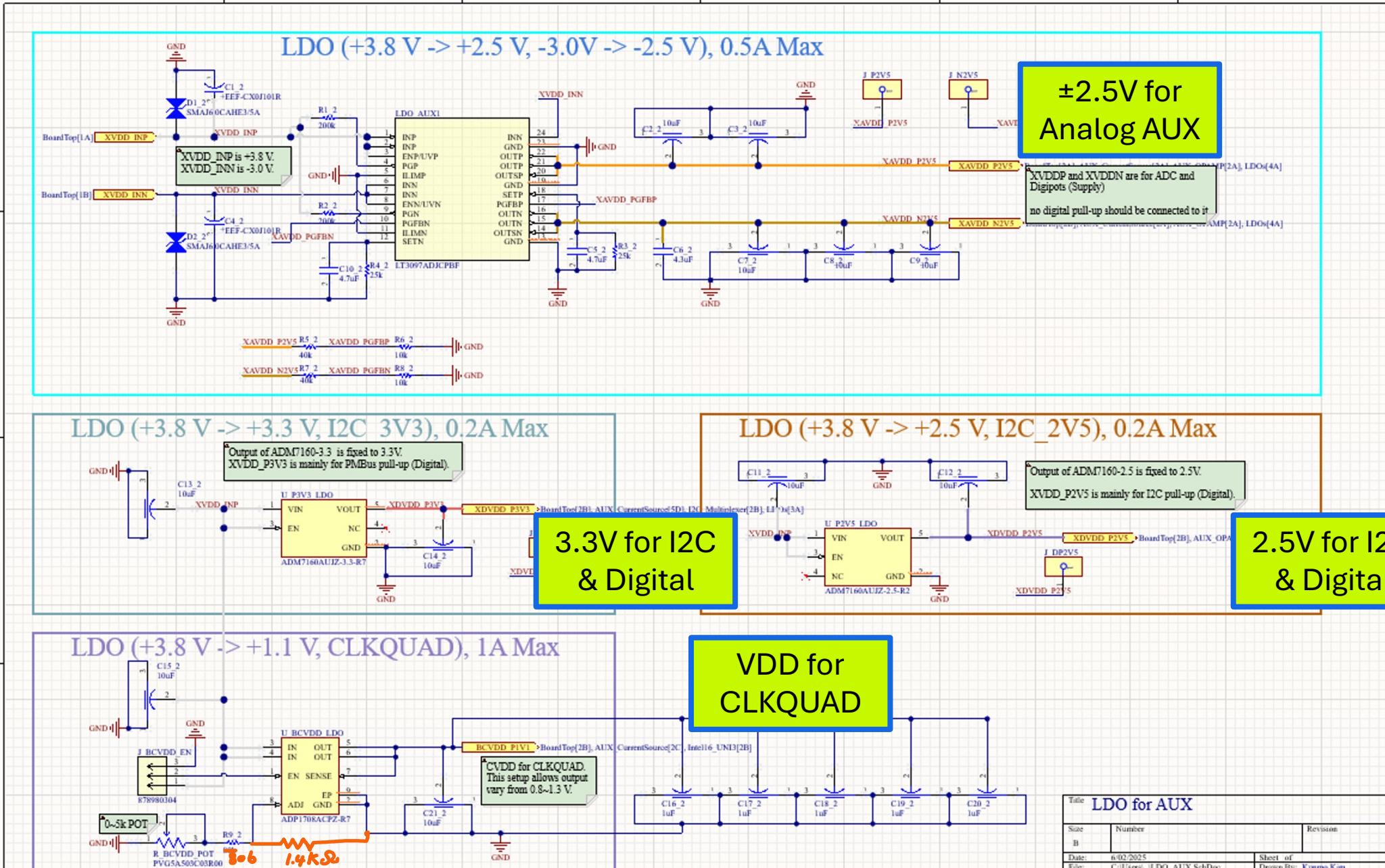
Max power rating

$$P_{DISS} = I_{OUT(MAX)} \times (V_{IN} - V_{OUT}) + I_{GND} \times V_{BIAS}, \quad I_{GND} = 5mA$$

2nd stage LDO

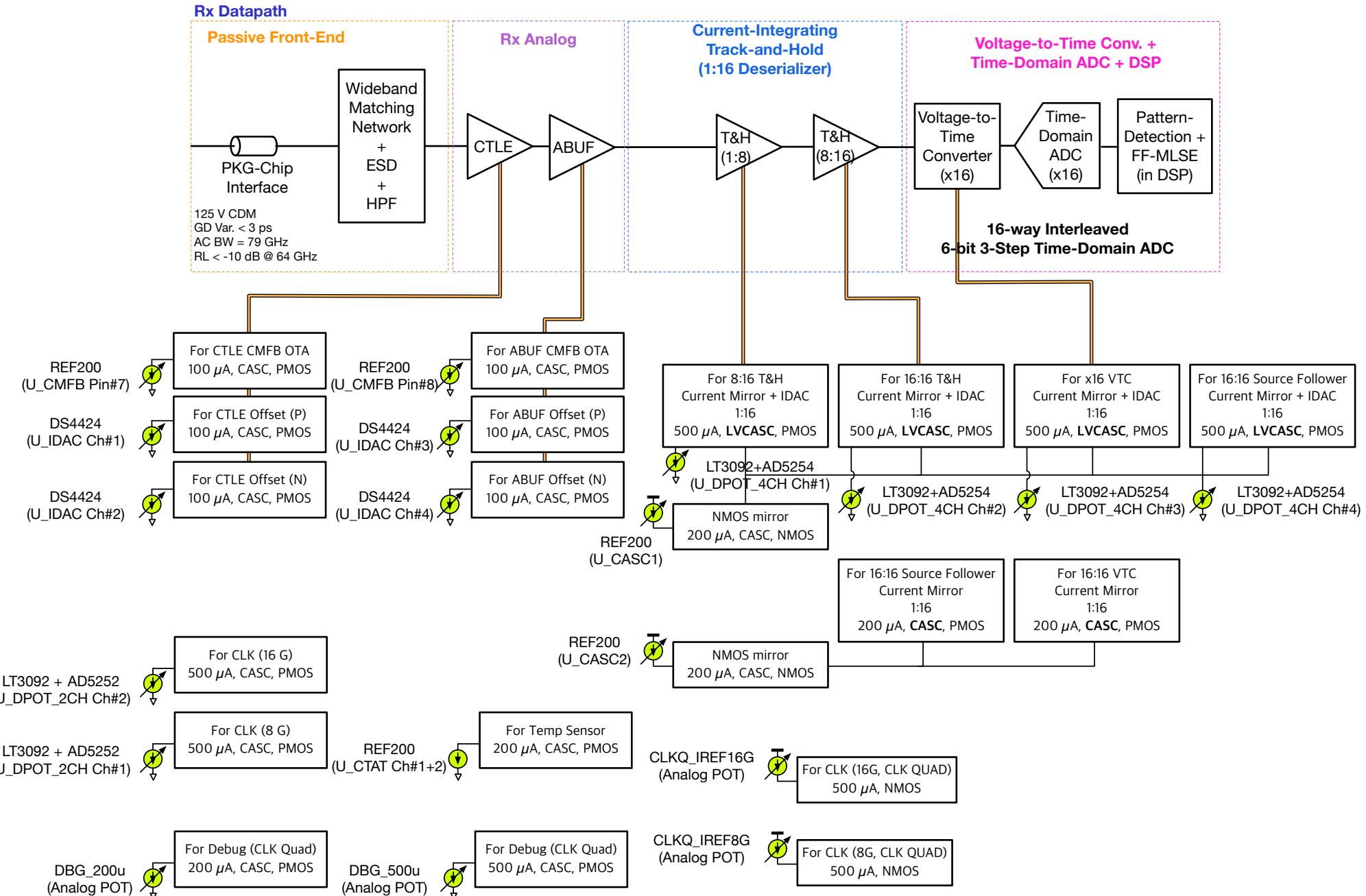
- $P_{DISS,MAX(2nd)} = 3A * (1.6 - 1.1) + 0.005 * 5 = 1.525 W \rightarrow +72 ^\circ C$
- Expected power consumption
 - w/ 1.5A load = 0.775 W $\rightarrow +37 ^\circ C$
 - w/ 1.0A load = 0.525 W $\rightarrow +24.7 ^\circ C$

LDO for AUX

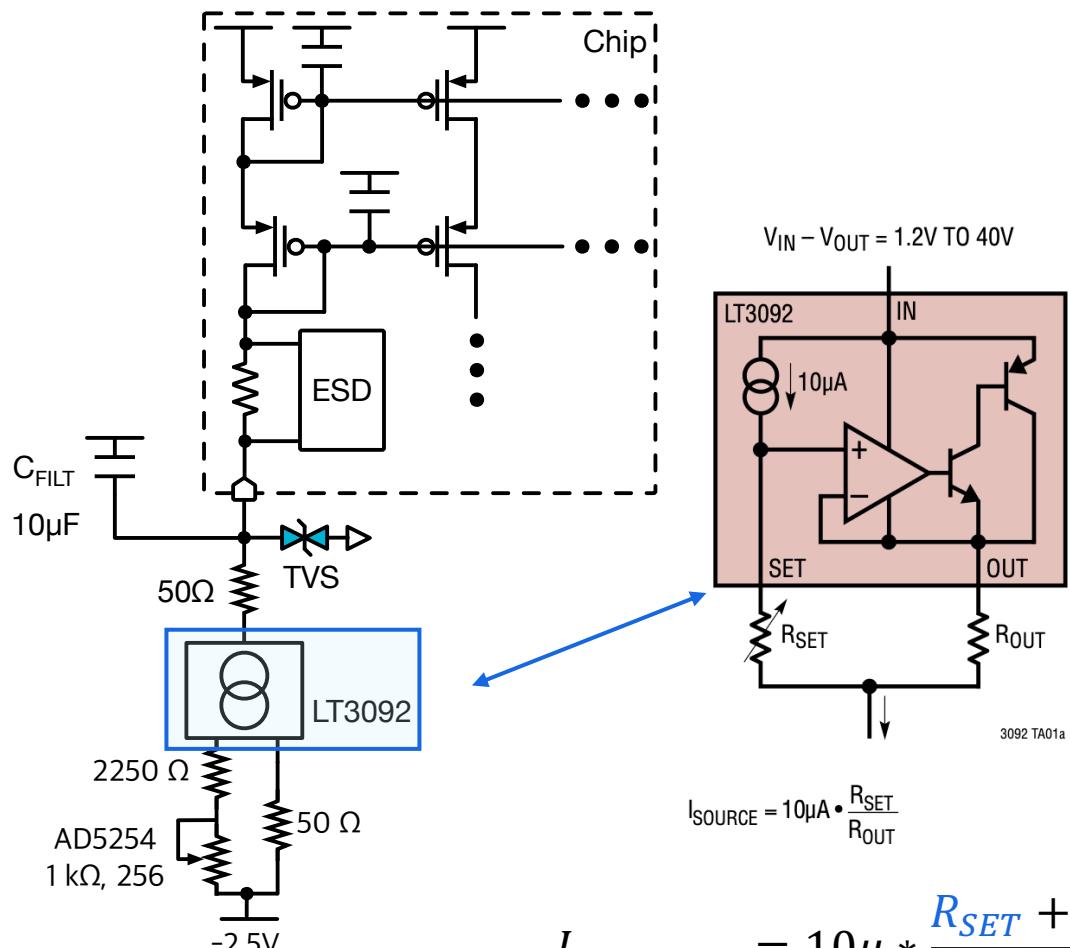


Current Source

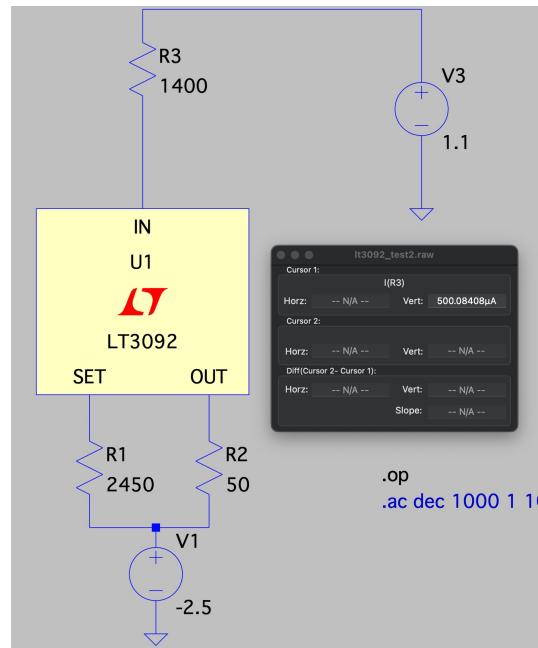
Current Source Map



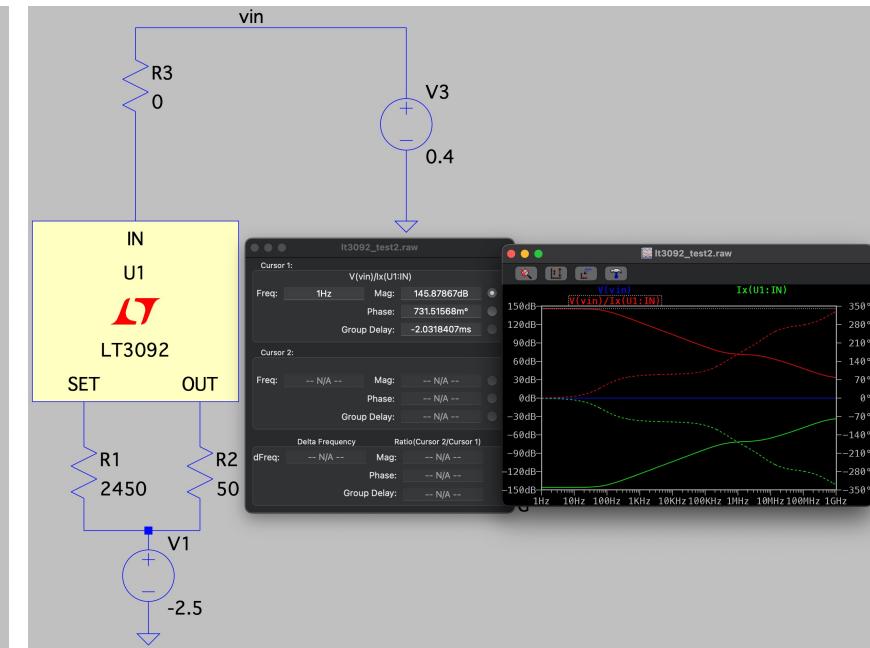
Current Source (LT3092)



DC Sim



Output Impedance Sim
 $R_{OUT} = 145 \text{ dB (} 18 \text{ M}\Omega \text{) @ DC}$



$$I_{IN,LT3092} = 10\mu\text{A} * \frac{R_{SET} + R_{OUT}}{R_{OUT}}$$

Why LT3092? Why not LM334?

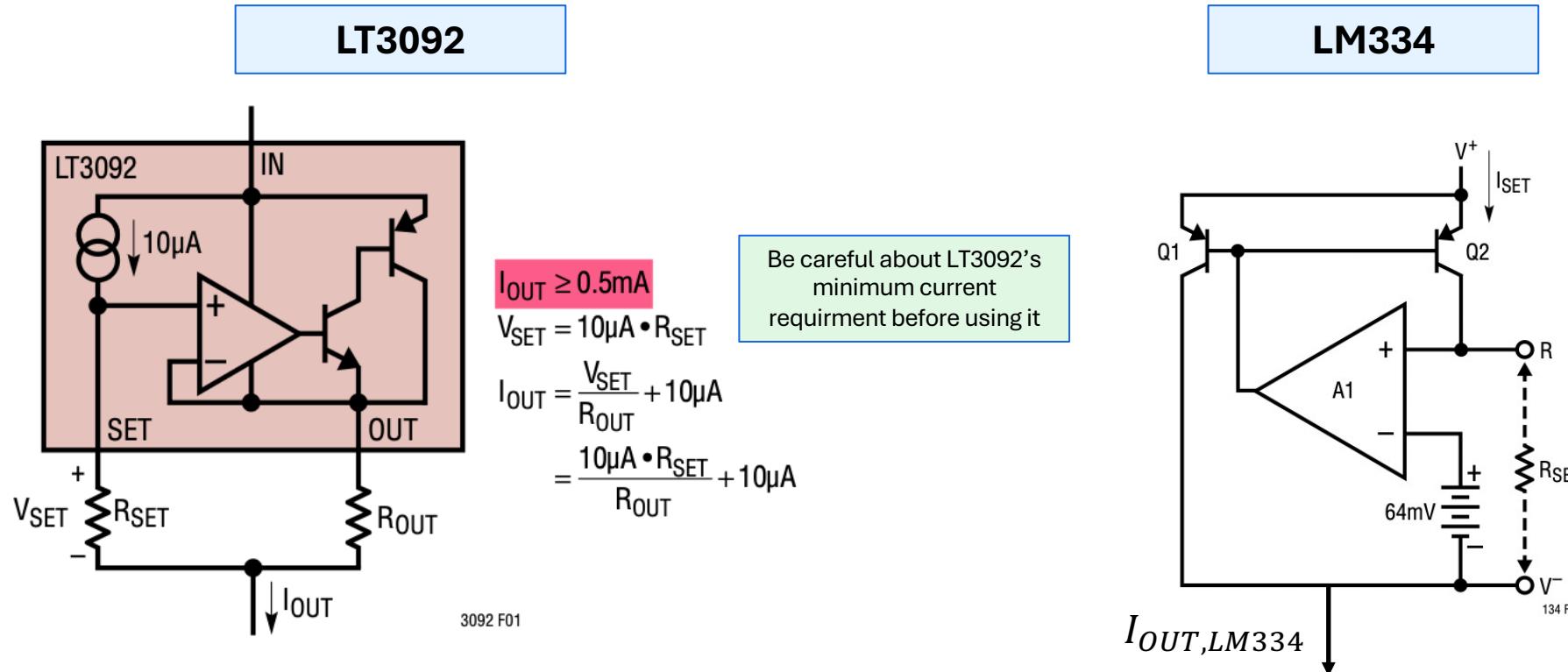


Figure 1. Using the LT3092 as a Current Source

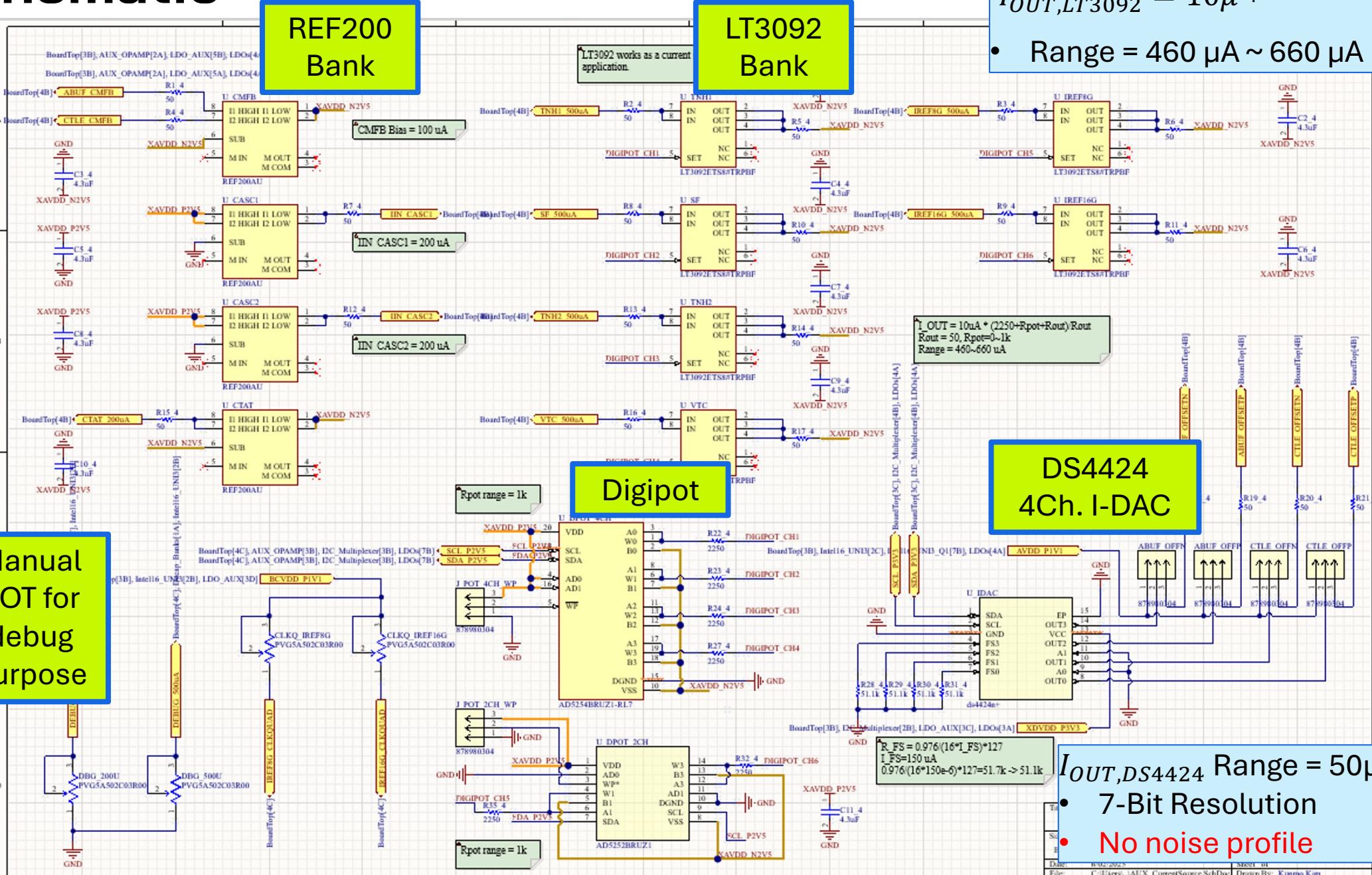
$$I_{IN,LT3092} = 10\mu \cdot \frac{R_{SET} + R_{OUT}}{R_{OUT}}$$

$$I_{OUT,LM334} = 1.059 \cdot \frac{67.7 \text{ mV}}{R_{SET}}$$

- Both have NSD $\sim 2.5 \text{ pA}/\sqrt{\text{Hz}}$.

- Need small resistance for R_{SET}
- non-linear I_{OUT} profile ($1/x$)

Schematic



$$I_{OUT,LT3092} = 10\mu * \frac{2250 + (0\sim 1k) + R_{OUT}}{R_{OUT}}$$

2nd PCB – FPGA Breakout Board

Stack-Up

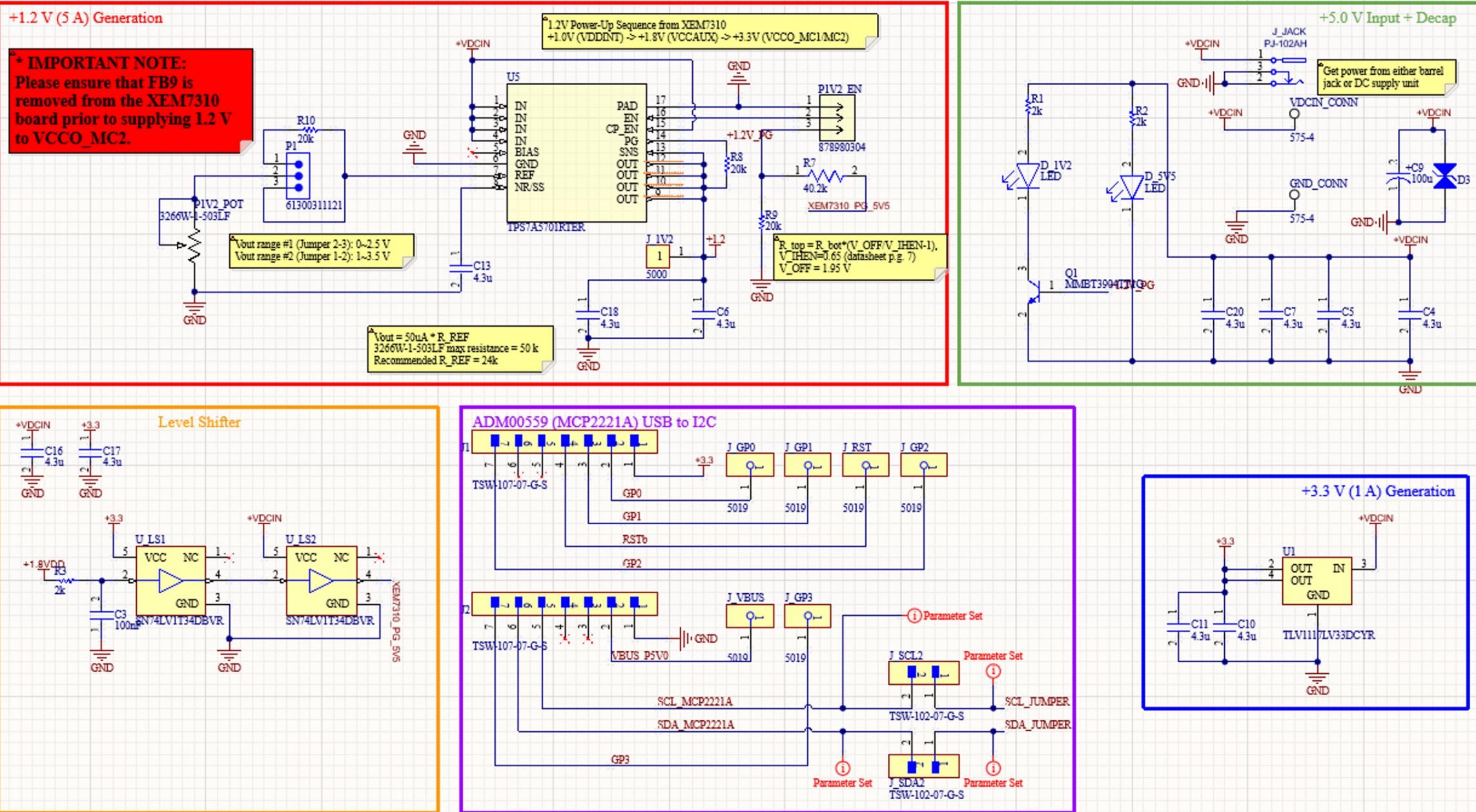
#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.4mil	3.5	
1	Top Layer		Signal	1oz	1.378mil		
	Dielectric 2	7628	Prepreg		8mil	4.4	0.02
2	Layer 1 (GND)	CF-004	Plane	1oz	1.378mil		
	Dielectric 1	FR-4	Core		40.6mil	4.6	
3	Layer 2 (PWR)	CF-004	Plane	1oz	1.378mil		
	Dielectric 3	7628	Prepreg		8mil	4.4	0.02
4	Bottom Layer		Signal	1oz	1.378mil		
	Bottom Solder	Solder Resist	Solder Mask		0.4mil	3.5	
	Bottom Overlay		Overlay				

2) JLC041611-7628 Stackup

Compatible copper & dielectric thickness

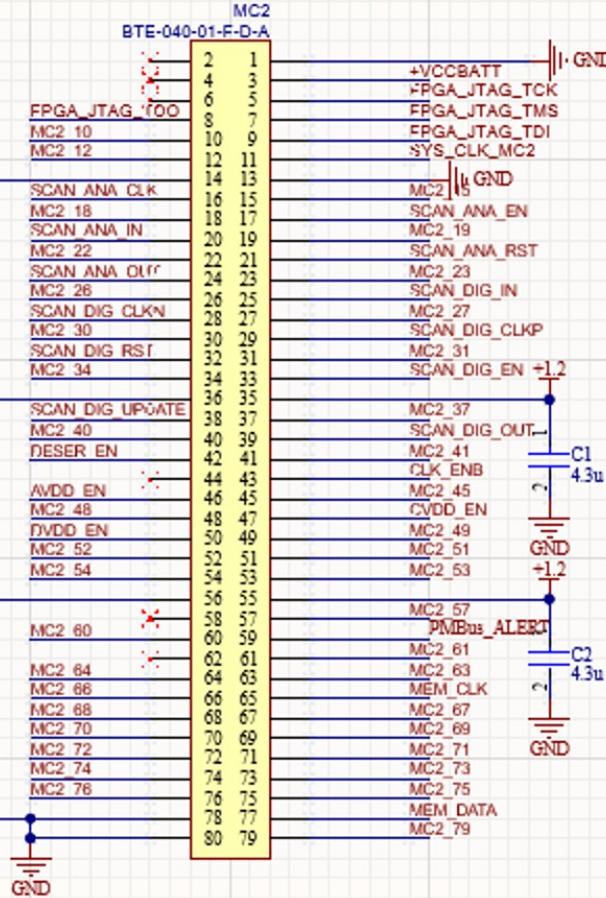
Layer	Material Type	Thickness	
Top Layer	Copper	0.035mm	
Prepreg	7628*1	0.203mm	
Inner Layer L2	Copper	0.03mm	
Core>	Core	1.03mm	1.1mm 1/1OZ with copper
Inner Layer L3	Copper	0.03mm	
Prepreg	7628*1	0.203mm	
Bottom Layer	Copper	0.035mm	

FPGA Breakout Board (Schematic #1)

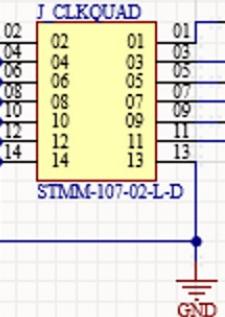


FPGA Breakout Board (Schematic #2)

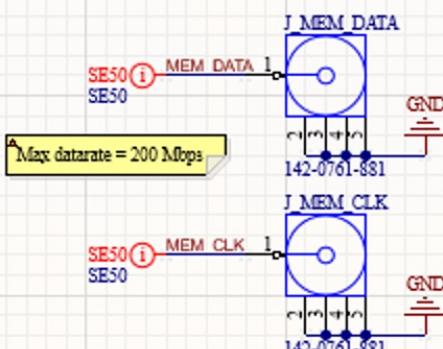
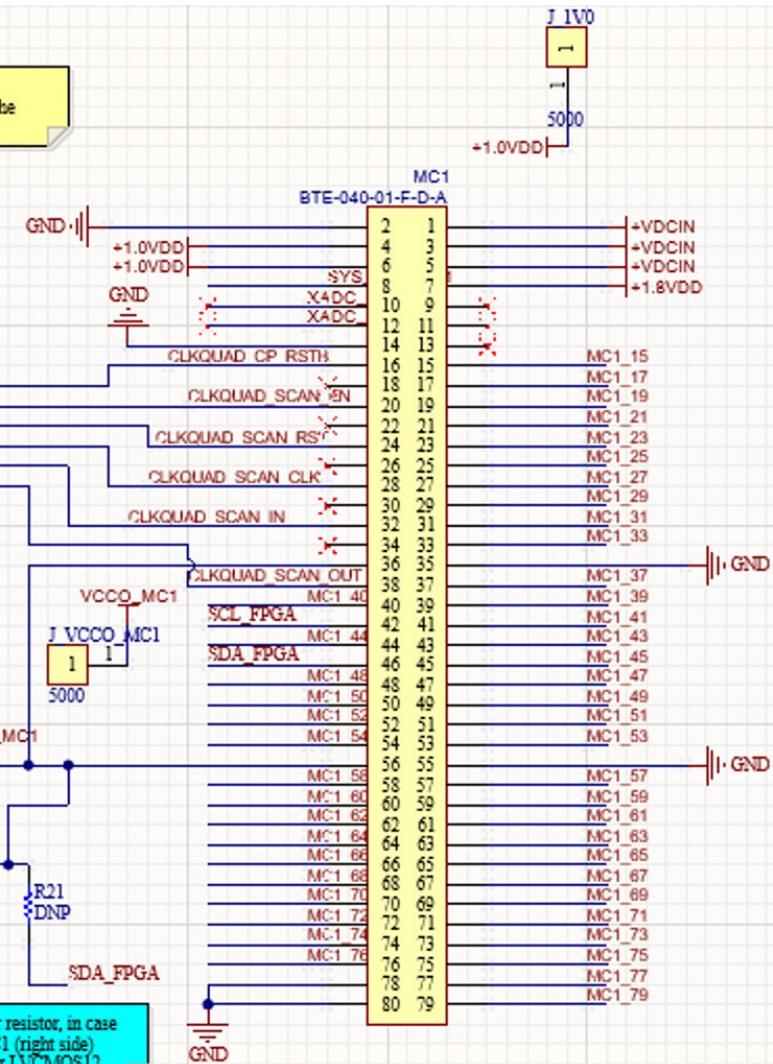
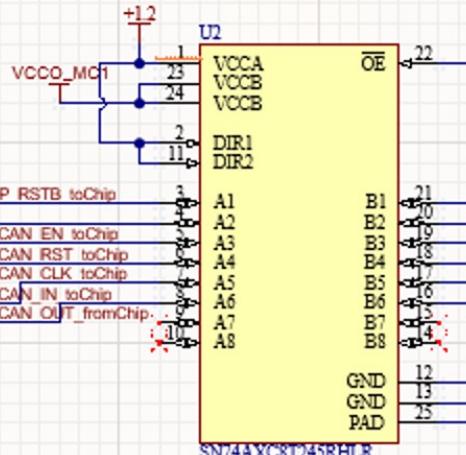
Mezzanine Connectors



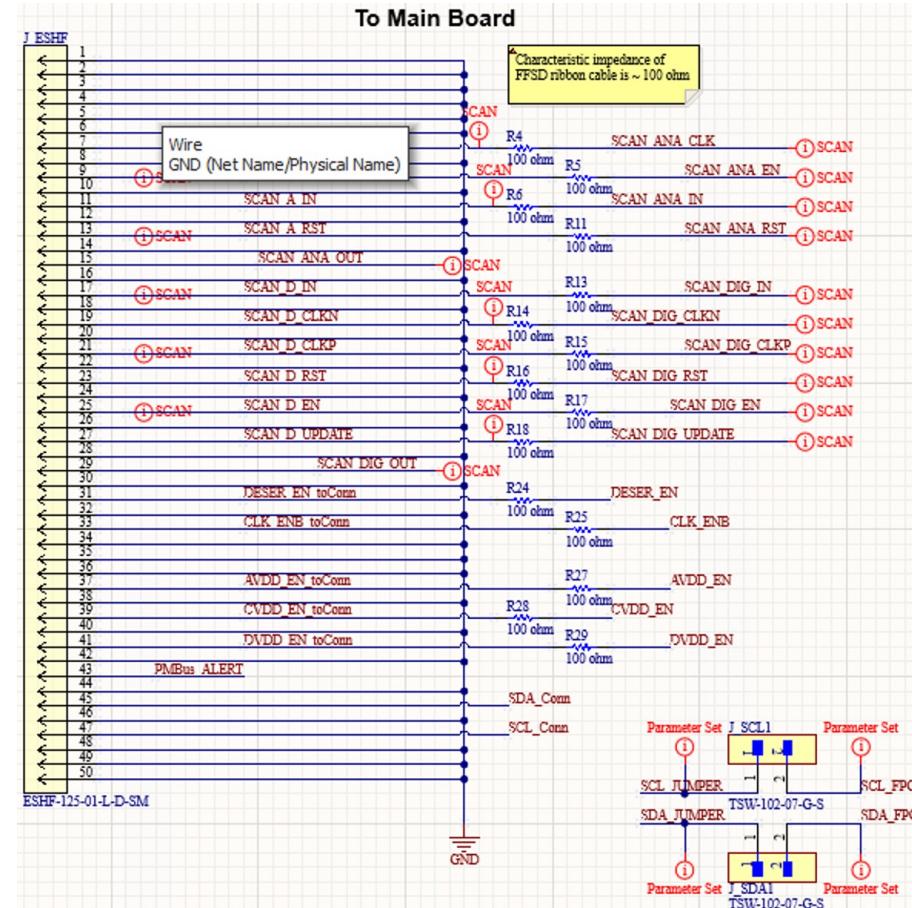
Characteristic impedance of
FFSD ribbon cable is ~ 100 ohm



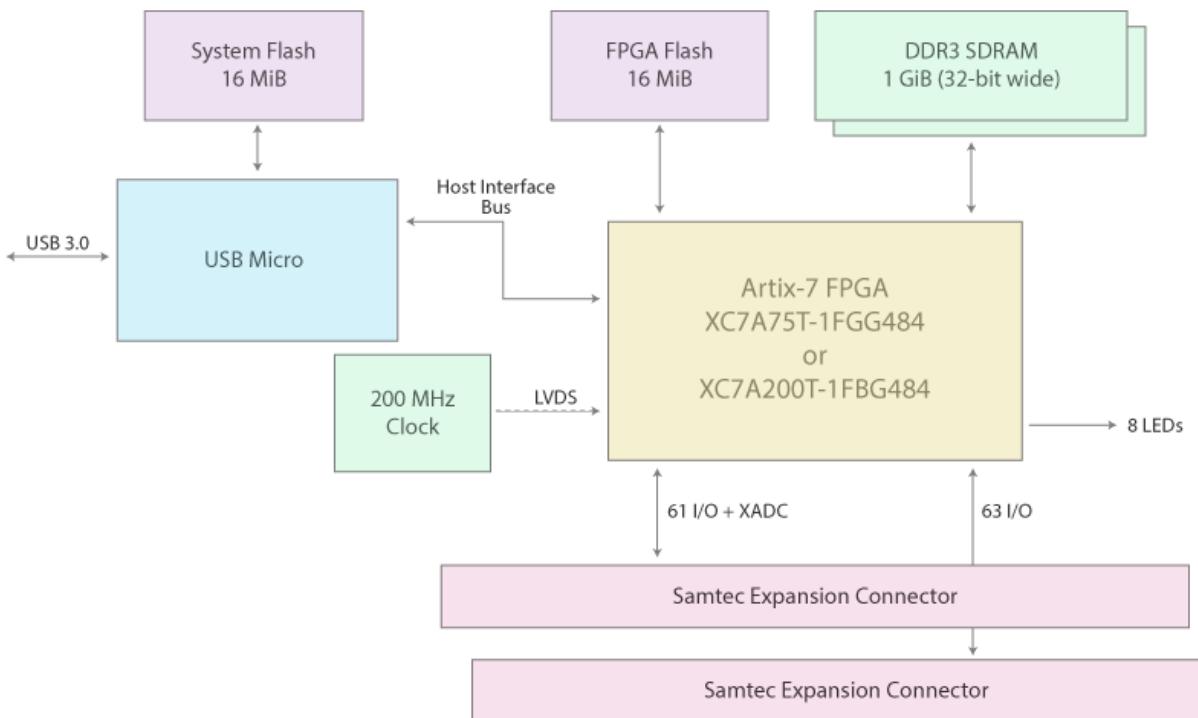
Level shifter for the CLKQUAD SCAN.
Note: VCCO of MC1 is fixed to 3.3 V. DO NOT REMOVE FB8 on the
XEM7310 board.



FPGA Breakout Board (Schematic #3)

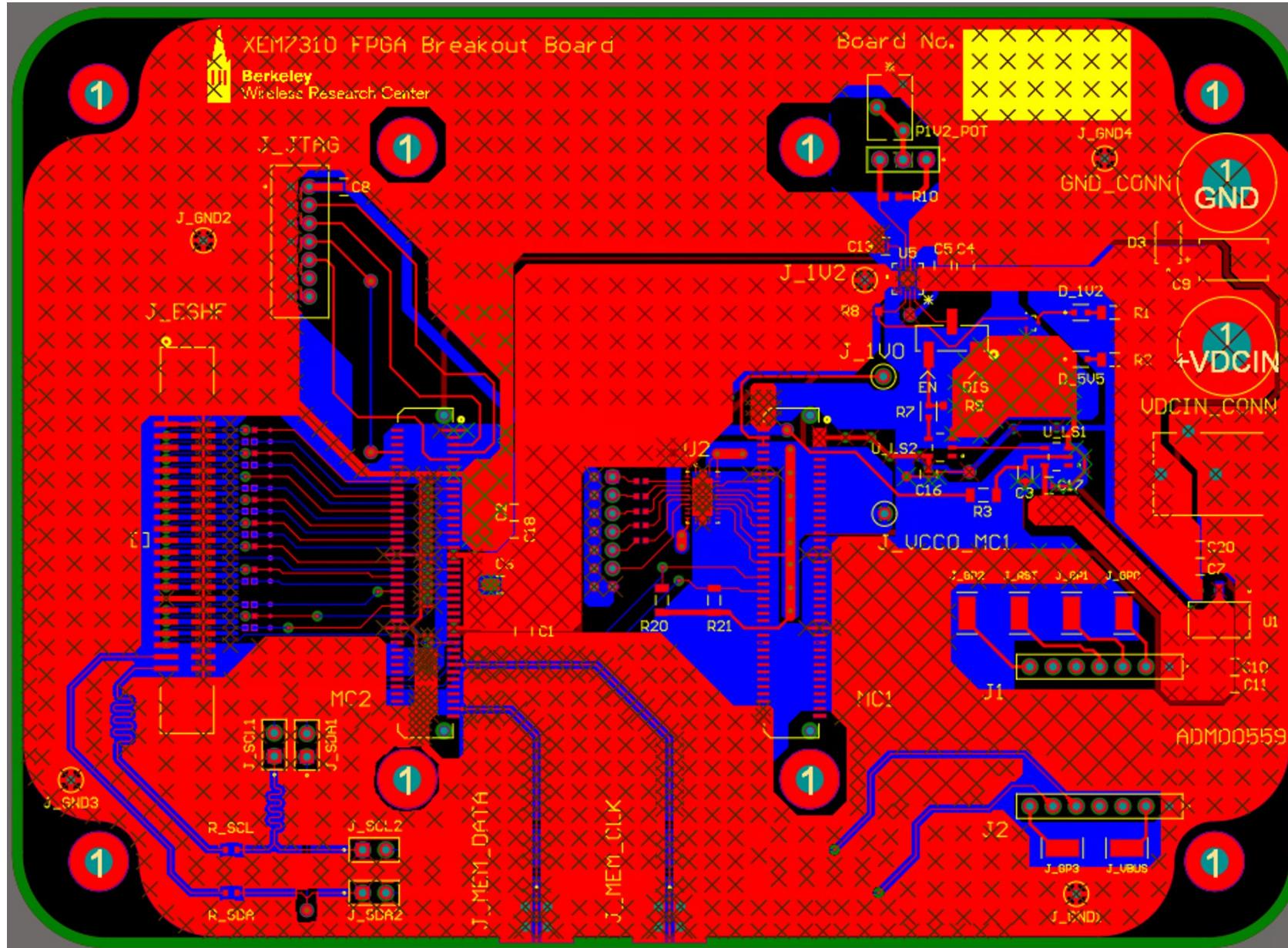


FPGA Selection



- Artix-7 FPGA provides HR IO Bank
 - **It means I can use LVC MOS12**
 - No level shifters are needed !!!
- 13 MB BlockRAM
- 269,200 DFFs
- 1 GB DDR3 RAM
- LOTS of IO pins !!!

FPGA Breakout Board (Layout, 2D)

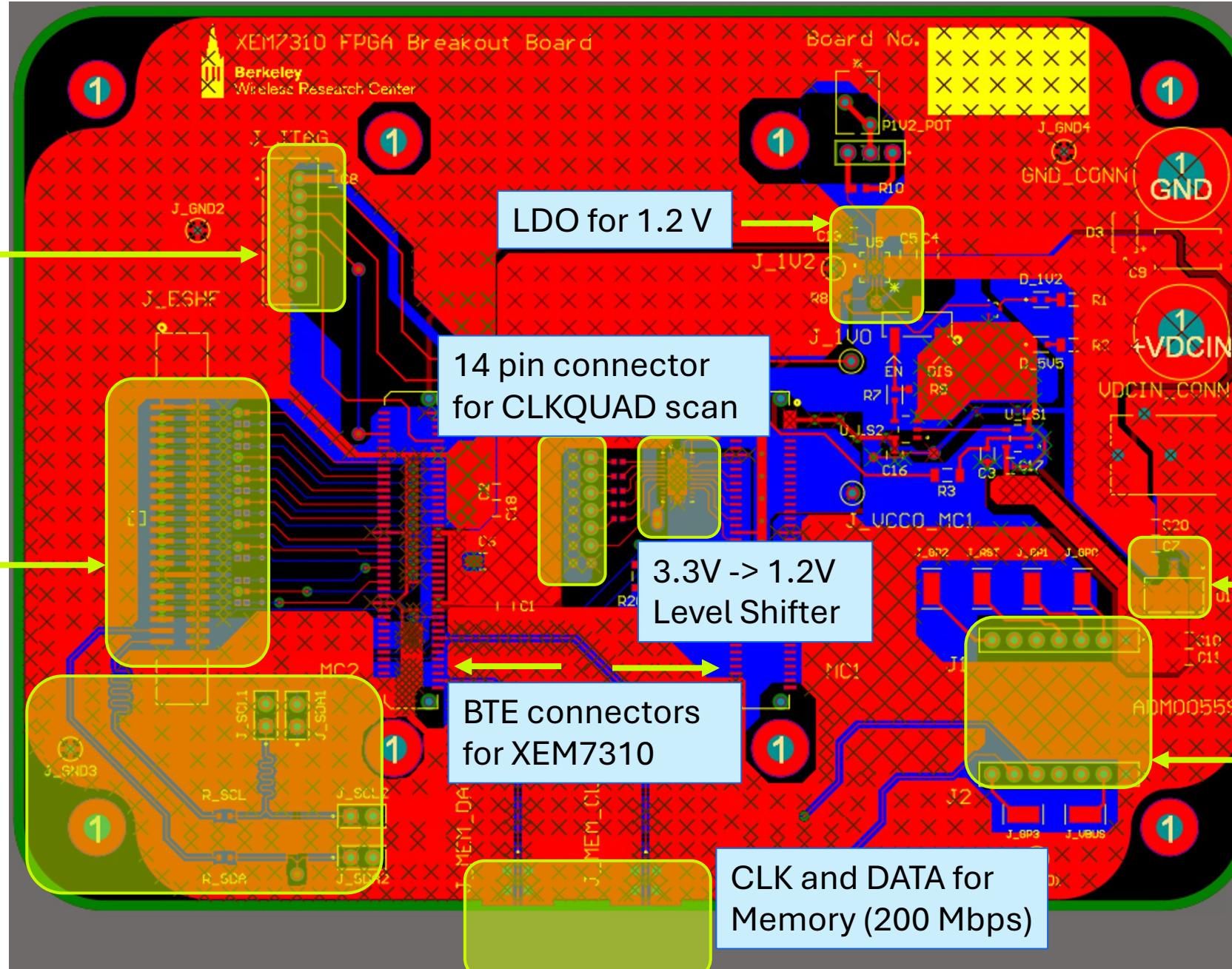


FPGA Breakout Board (Layout, 2D)

14 pin connector for JTAG

50-pin ESHF connector (all scan signals are back-terminated with $100\ \Omega$)

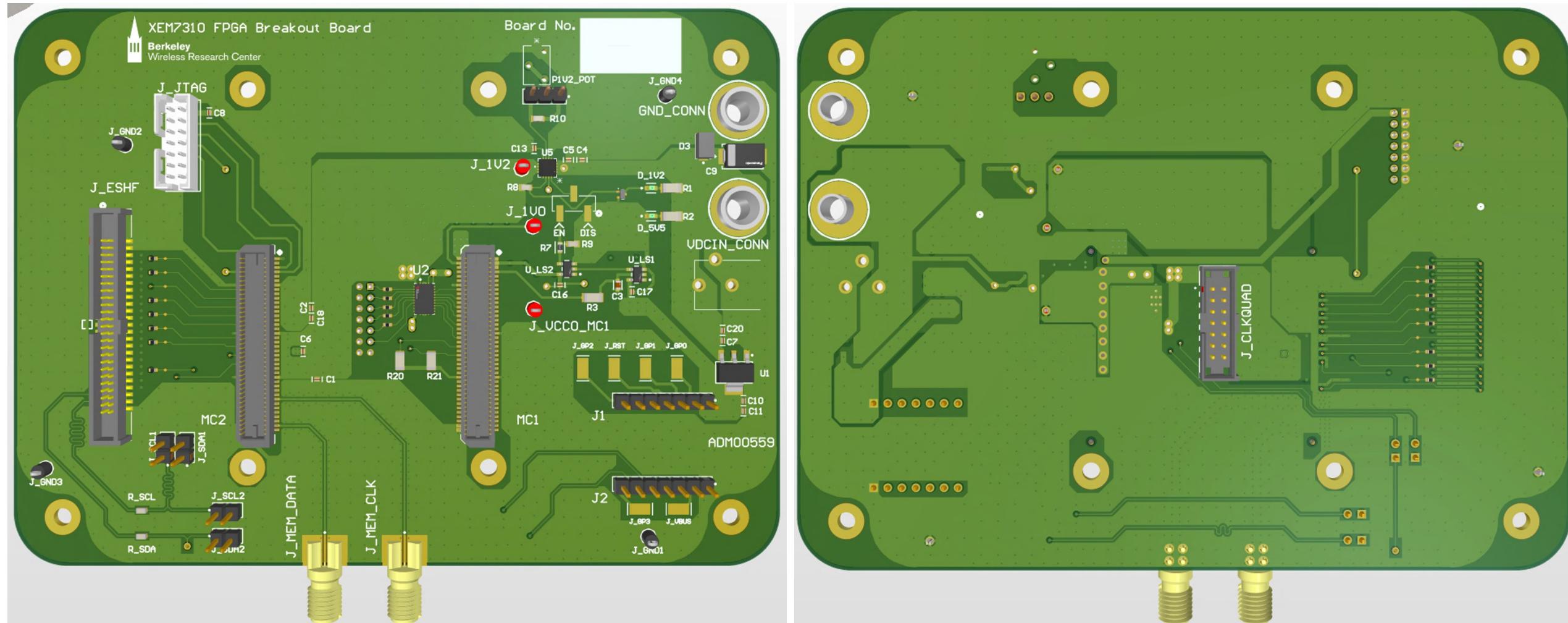
Jumpers for I₂C



LDO for 3.3 V

ADM00559 USB to I₂C Controller

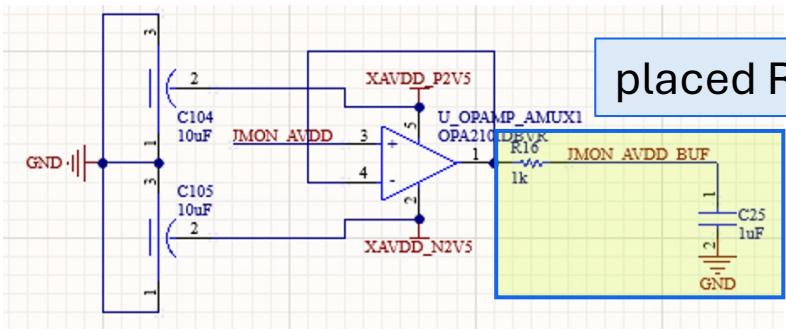
FPGA Breakout Board (Layout, 3D)



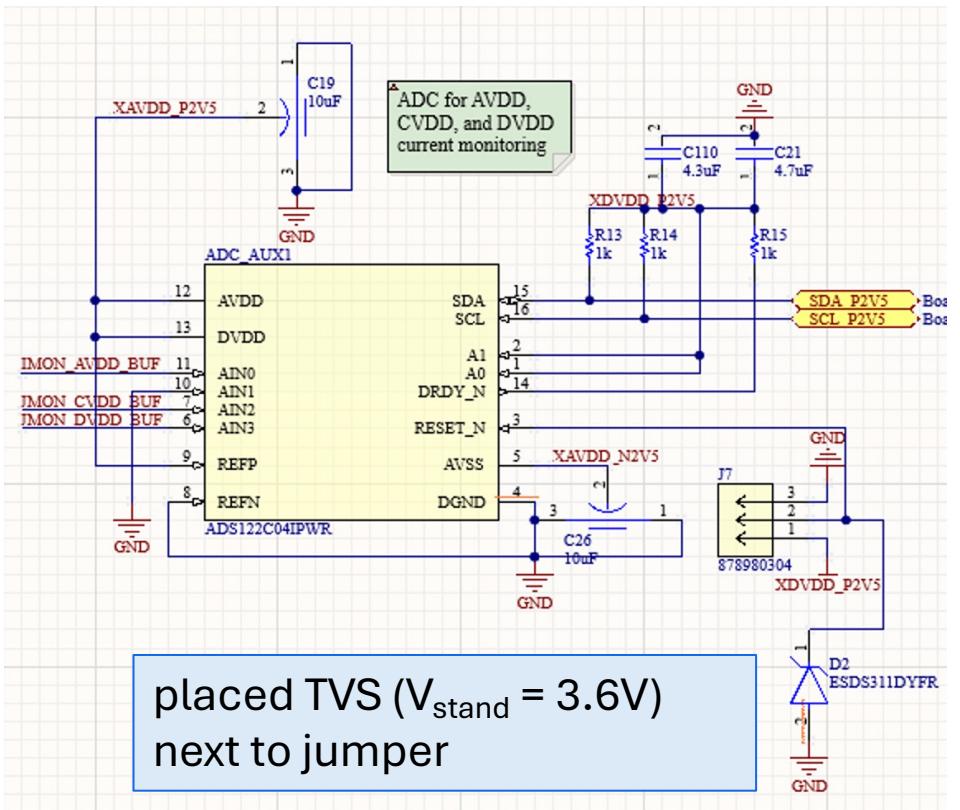
Appendix

AUX Circuit for DC Signal Measurement

ADC #1 for Current Monitor



placed RC LPF right next to the ADC input



placed TVS ($V_{\text{stand}} = 3.6V$)
next to jumper

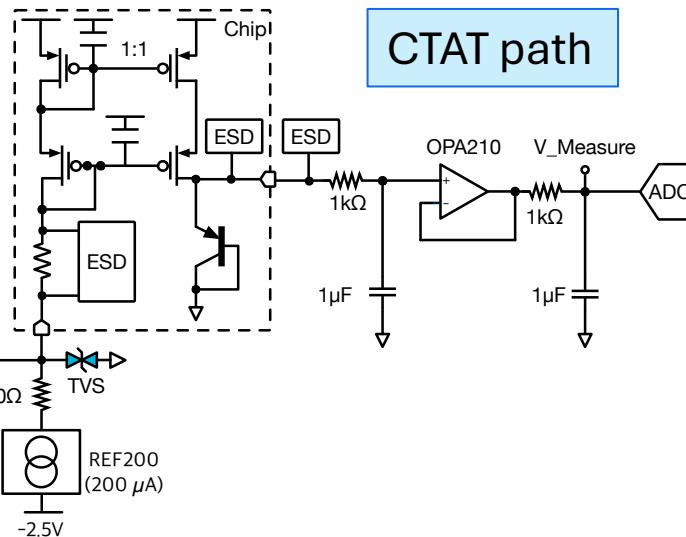
OPA210 (Texas Instruments)

- low noise ($2.2 \text{ nV}/\sqrt{\text{Hz}}$)
- low offset ($5 \mu\text{V}$)
- $A_{\text{OL}} = 120 \text{ dB}$
- High CMRR (132 dB)
- GBW = 18 MHz (doesn't matter much tho)
- Quiescent current = 2.5 mA

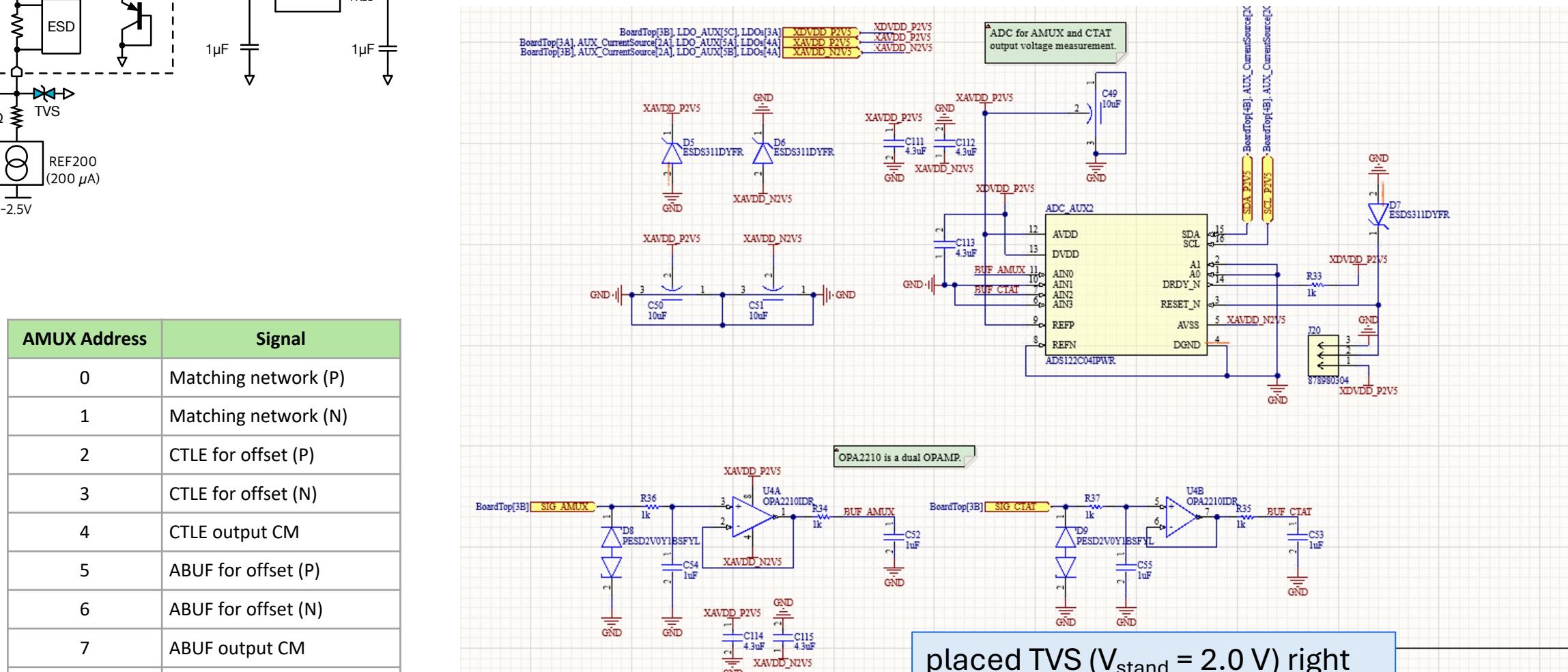
ADS122C04 (Texas Instruments)

- 24-bit Sigma-Delta ADC with I2C Interface
- 2.048 V internal reference
- Programmable gain: 1~128
- Max sampling rate = 2kSPS
 - sampling frequency generated internally

ADC #2 for AMUX & CTAT Output Monitor



CTAT path

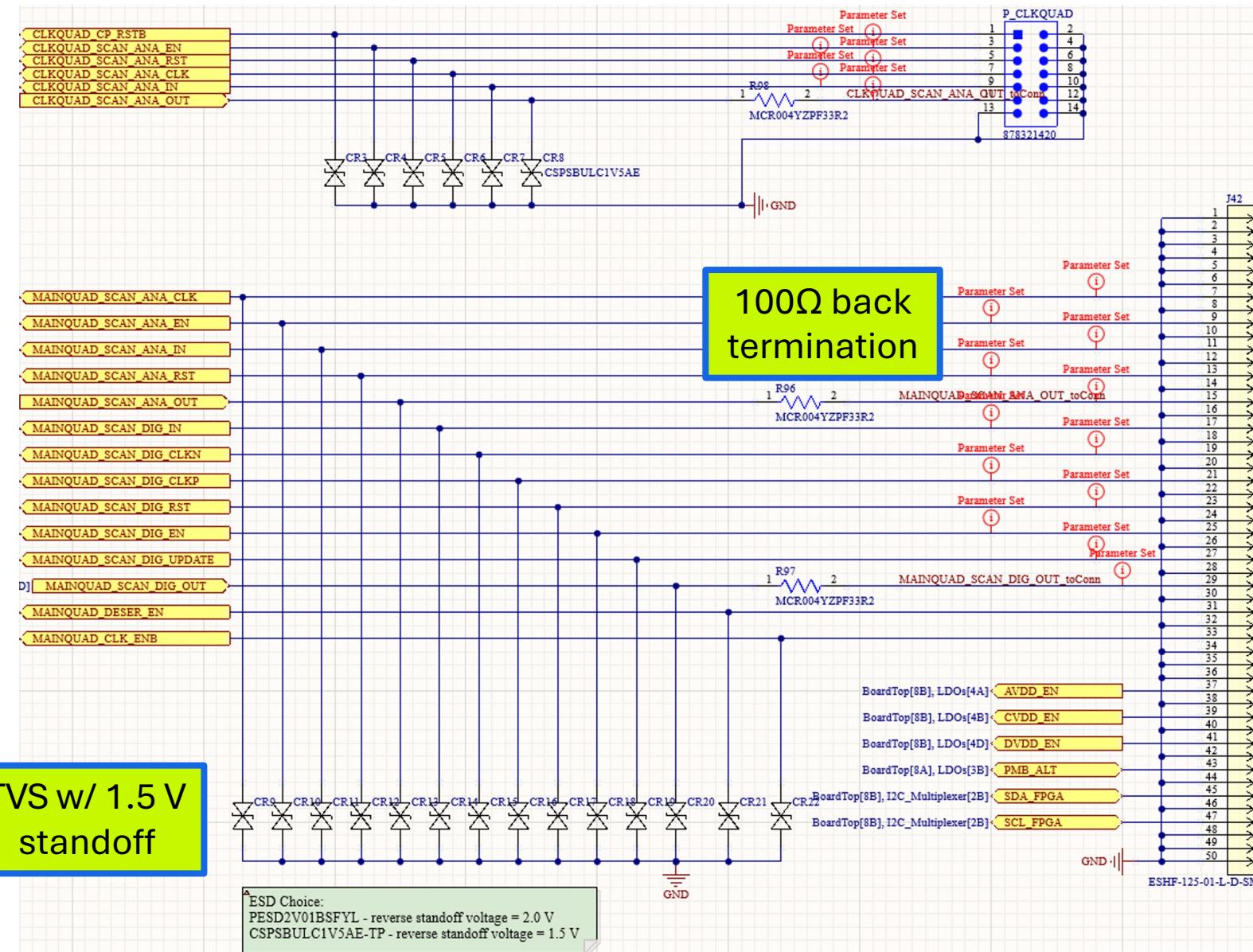


placed TVS ($V_{stand} = 2.0$ V) right underneath of BGA package

AMUX Address	Signal
0	Matching network (P)
1	Matching network (N)
2	CTLE for offset (P)
3	CTLE for offset (N)
4	CTLE output CM
5	ABUF for offset (P)
6	ABUF for offset (N)
7	ABUF output CM
8	VDD check

SCAN Signal Bus

SCAN Signal Bus



50 pin (2x 25) FFSD cable. 30 cm
G - S - G - S - G ... to minimize crosstalk



Z₀ of IDE ribbon cable ≈ 100 Ω

SCAN Signal Delay Matching

- SCAN for analog

5 Nets (0 Highlighted)					
*	Name	Node C...	Signal L...	Route...	Delay (ps)
	MAINQUAD_SCAN_ANA_CLK	3	n/a	4457.75	618.892
	MAINQUAD_SCAN_ANA_EN	3	n/a	4333.75	618.601
	MAINQUAD_SCAN_ANA_IN	3	n/a	3964.08	618.809
	MAINQUAD_SCAN_ANA_OUT_toC	2	4330.178	4331.66	619.233
	MAINQUAD_SCAN_ANA_RST	3	n/a	4151.95	619.113

Max Delay difference = 0.632 ps
Assuming SCAN is running at 100 Mbps
➤ $T_{b,SCAN}/2 = 5 \text{ ns}$
0.632 ps time difference is 0.012% (0.045°) of $T_{b,SCAN}/2$
➤ Negligible

- SCAN for digital

7 Nets (0 Highlighted)					
*	Name	Node C...	Signal L...	Route...	Delay (ps)
	MAINQUAD_SCAN_DIG_CLKN	3	n/a	3084.24	459.087
	MAINQUAD_SCAN_DIG_CLKP	3	n/a	3030.64	461.914
	MAINQUAD_SCAN_DIG_EN	3	n/a	3536.28	460.586
	MAINQUAD_SCAN_DIG_IN	3	n/a	2954.46	462.086
	MAINQUAD_SCAN_DIG_OUT_toC	2	3459.947	3457.26	459.108
	MAINQUAD_SCAN_DIG_RST	3	n/a	3490.49	471.409
	MAINQUAD_SCAN_DIG_UPDATE	3	n/a	3337.06	468.210

Max Delay difference = 12 ps
Assuming SCAN is running at 100 Mbps
12 ps time difference is 0.24% (0.86°) of $T_{b,SCAN}/2$
➤ Negligible

I2C Signal Delay Matching

2 Nets (0 Highlighted)						
*	Name	Node C...	Signal L...	Rout...	Delay (ps)	
[]	SCL_FPGA	2	2803.381	2781.41	340.291	
[]	SDA_FPGA	2	2710.103	2700.22	340.697	

6 xSignals (0 Highlighted)							
*	Name	No...	Sign...	Total...	Routed ...	Unr...	Delay...
[]	PMB_SCL_PP4	2	1422.81	0	1422.812	0	192.575 N/A
[]	PMB_SCL_PP5	2	3758.31	0	3758.311	0	562.139 N/A
[]	PMB_SCL_PP6	2	2519.01	0	2519.017	0	353.538 N/A
[]	PMB_SDA_PP4	2	1355.30	0	1355.306	0	184.367 N/A
[]	PMB_SDA_PP5	2	3643.21	0	3643.239	0	544.913 N/A
[]	PMB_SDA_PP6	2	2449.11	0	2449.114	0	344.109 N/A

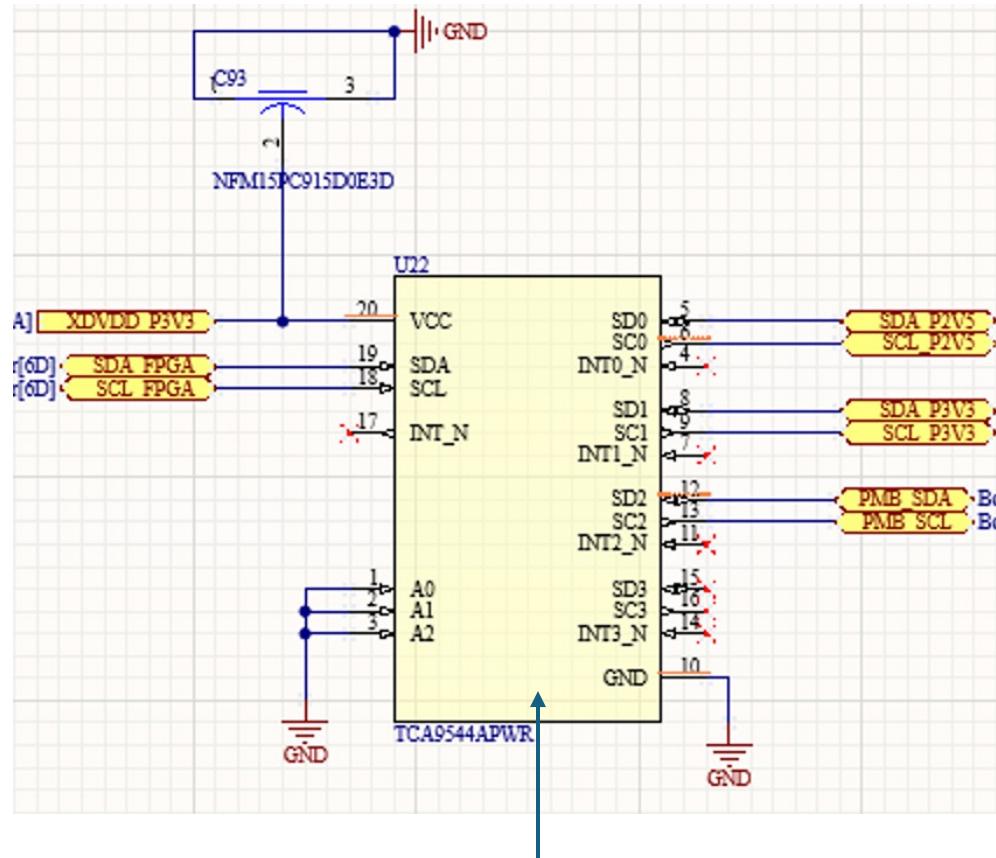
10 xSignals (0 Highlighted)							
*	Name	No...	Sign...	Total...	Routed ...	Unr...	Delay...
[]	SCL_P2V5_PP1	2	4211.26	0	4211.266	0	541.482 N/A
[]	SCL_P2V5_PP2	2	3158.09	0	3158.09	0	405.719 N/A
[]	SCL_P2V5_PP3	2	5954.76	0	5954.764	0	804.230 N/A
[]	SCL_P2V5_PP4	3	2029.44	0	2029.443	0	270.894 N/A
[]	SCL_P2V5_PP5	2	1055.07	0	1055.07	0	122.855 N/A
[]	SDA_P2V5_PP1	2	4055.20	0	4055.202	0	538.341 N/A
[]	SDA_P2V5_PP2	2	2979.78	0	2979.782	0	397.044 N/A
[]	SDA_P2V5_PP3	2	5806.00	0	5806.002	0	818.059 N/A
[]	SDA_P2V5_PP4	3	2028.80	0	2028.801	0	269.820 N/A
[]	SDA_P2V5_PP5	2	1054.67	0	1054.676	0	122.803 N/A

6 xSignals (0 Highlighted)							
*	Name	No...	Sign...	Total...	Routed ...	Unr...	Delay...
[]	SCL_P3V3_PP4	2	1665.06	0	1665.066	0	203.001 N/A
[]	SCL_P3V3_PP5	3	4376.51	0	4376.571	0	652.557 N/A
[]	SCL_P3V3_PP6	2	4006.56	0	4006.569	0	600.823 N/A
[]	SDA_P3V3_PP4	2	1616.64	0	1616.641	0	196.638 N/A
[]	SDA_P3V3_PP5	3	4352.55	0	4352.555	0	657.374 N/A
[]	SDA_P3V3_PP6	2	4154.64	0	4154.641	0	624.536 N/A

All good!

I2C MUX + Address Assignment

I2C MUX + Address

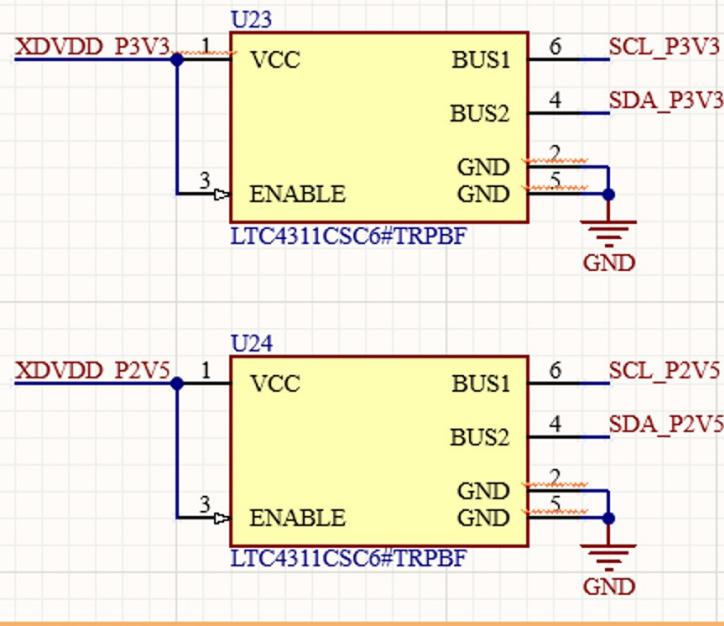


I2C Address of TCA9544 = 1110110 or 0x75

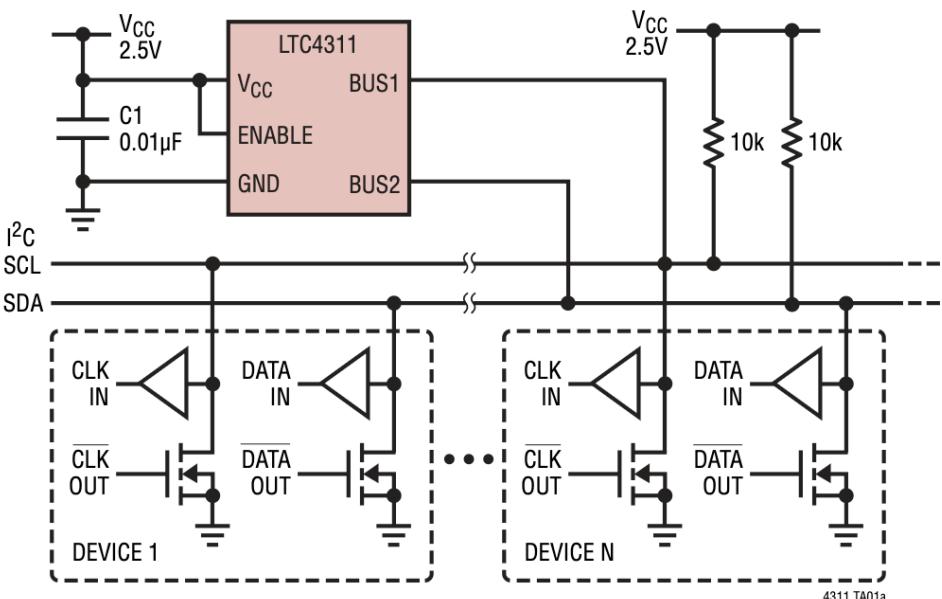
I2C Mux Channel	Component	I2C Address
Channel #1: • SDA_P2V5 • SCL_P2V5	Digipots (for LT3092)	0101100 or 0x2C (2Ch DPOT) 0101111 or 0x2F (4Ch DPOT)
	ADC #1 (LDO current monitor)	1000101 or 0x45
	ADC #2 (AMUX and CTAT)	1000000 or 0x40
Channel #2: • SDA_P3V3 • SCL_P3V3	IDAC (DS4424)	0010000 or 0x10 (Current DAC for Offset Cal)
	Digipots (LDO)	0101101 or 0x2D (AVDD, AD5245) 0101100 or 0x2C (CVDD, AD5245) 0101110 or 0x2E (DVDD, MCP4551)
	LDO for AVDD	1101111 or 0x6F
Channel #3: • PMB_SDA • PMB_SCL	LDO for CVDD	1101010 or 0x6A
	LDO for DVDD	1100000 or 0x60

I²C Improver

I²C Improver



TYPICAL APPLICATION



Comparison of I²C Waveforms for the LTC4311 vs Resistor Pull-Up

