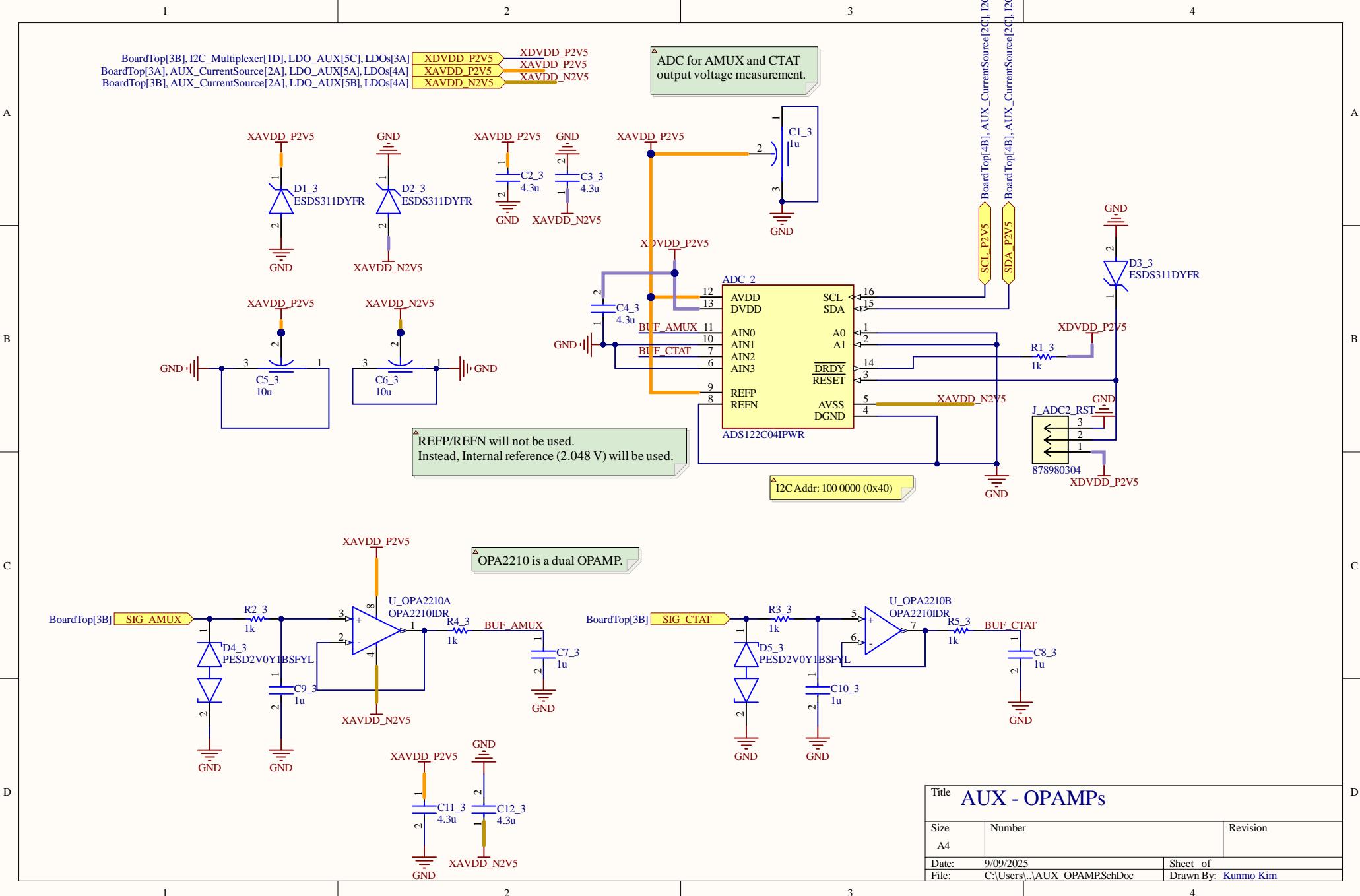
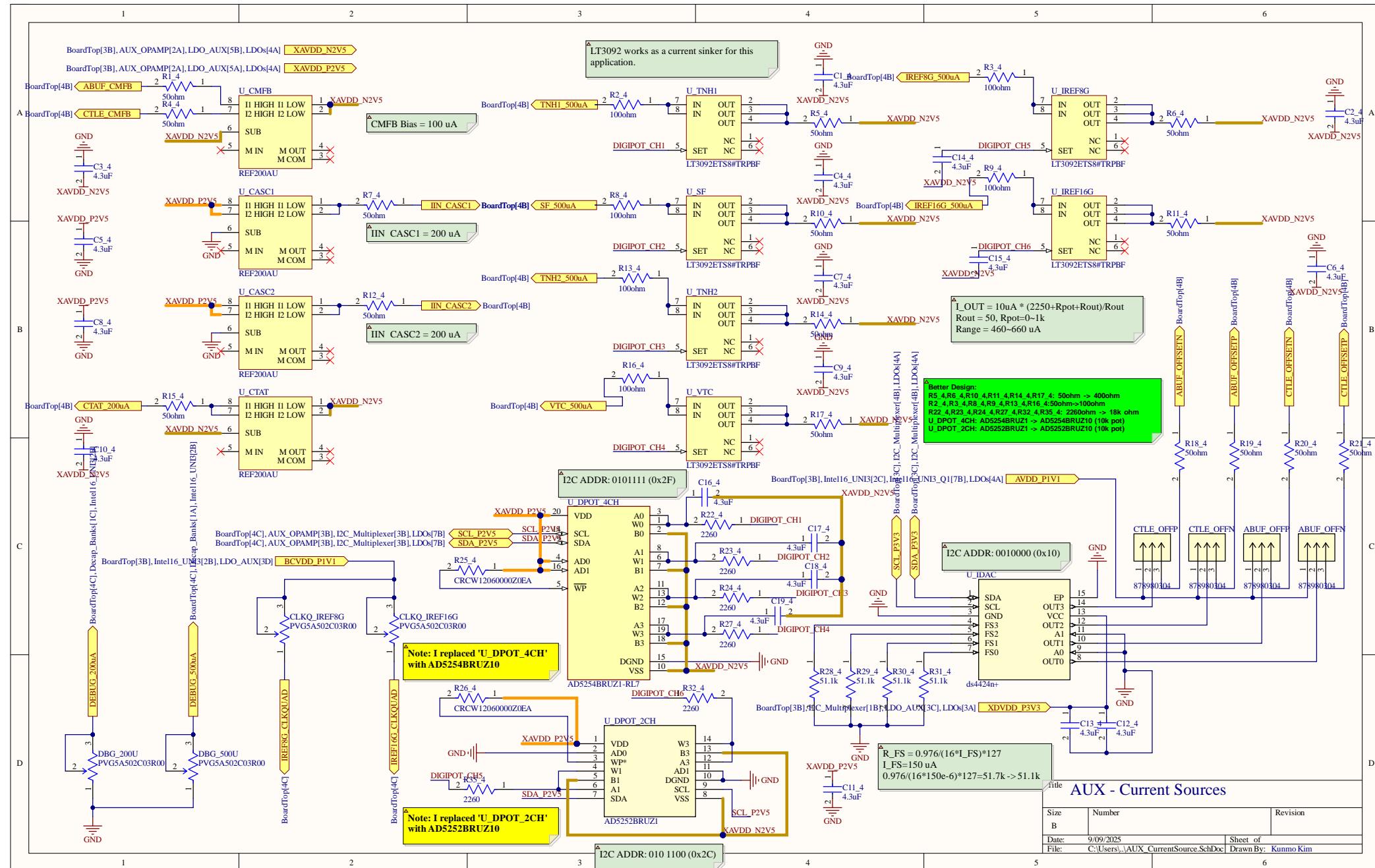


Title LDO for AUX

Size	Number	Revision
B		

Date: 9/09/2025 Sheet of
File: C:\Users\...\LDO_AUX.SchDoc Drawn By: Kunmo Kim





A

A

B

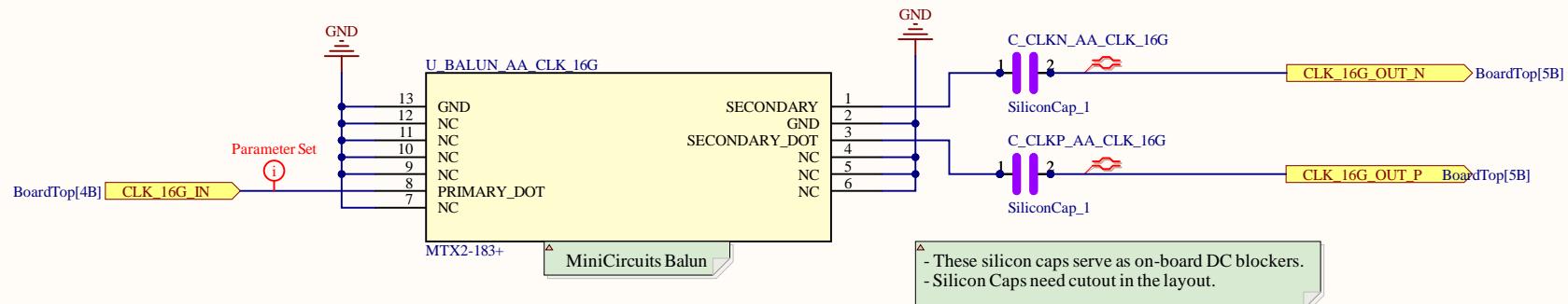
B

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10

5



Title 16 GHz Clock Input		
Size	Number	Revision
A4		
Date:	9/09/2025	Sheet of
File:	C:\Users\ser\1 CLK_16GHz.SchDoc	Drawn By: Kunmo Kim

A

A

B

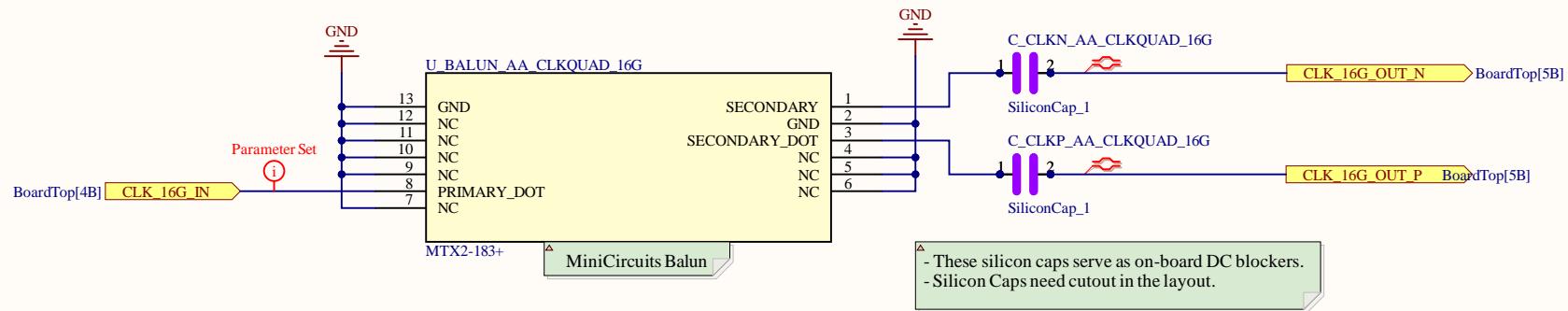
B

C

C

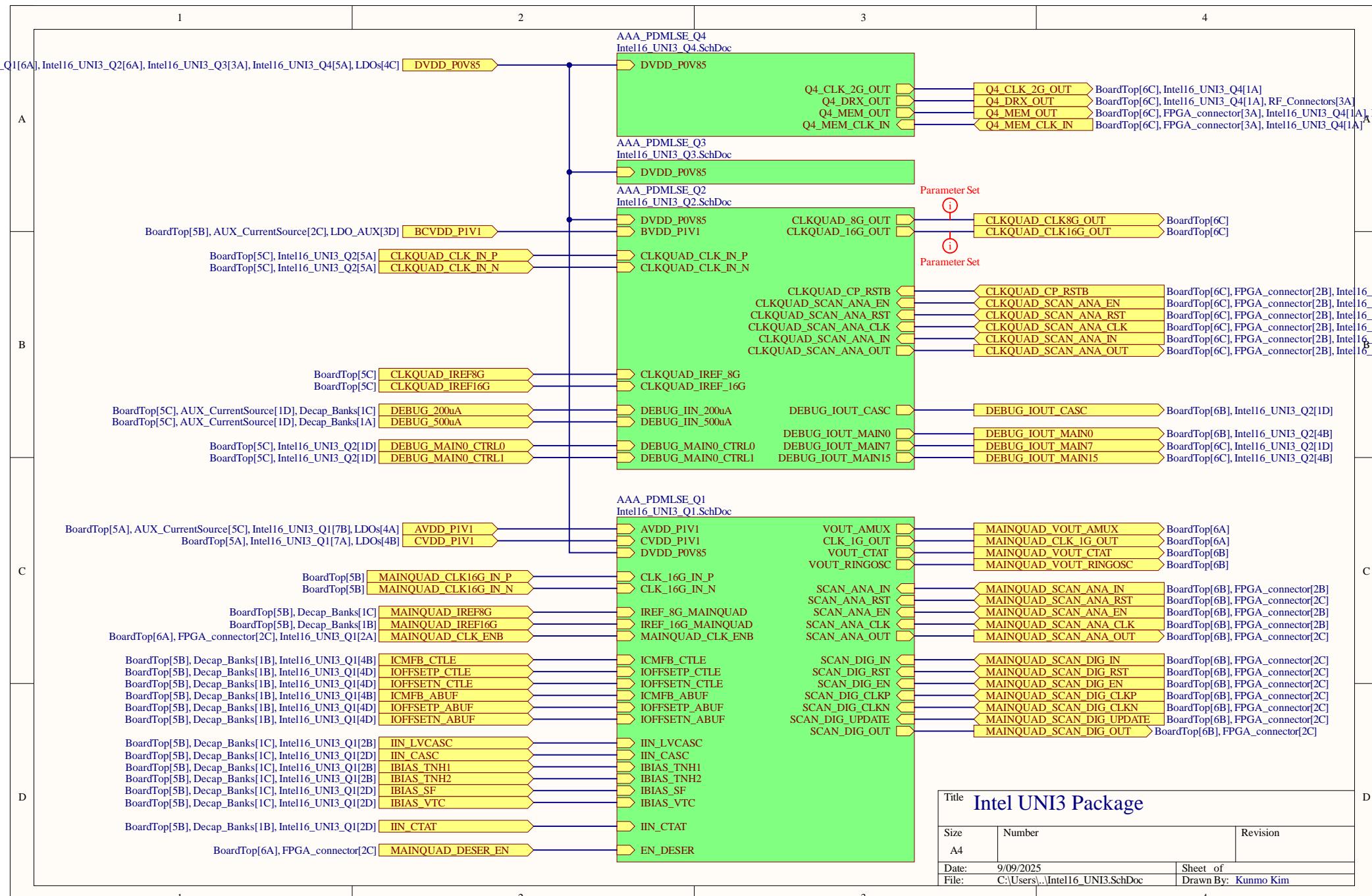
D

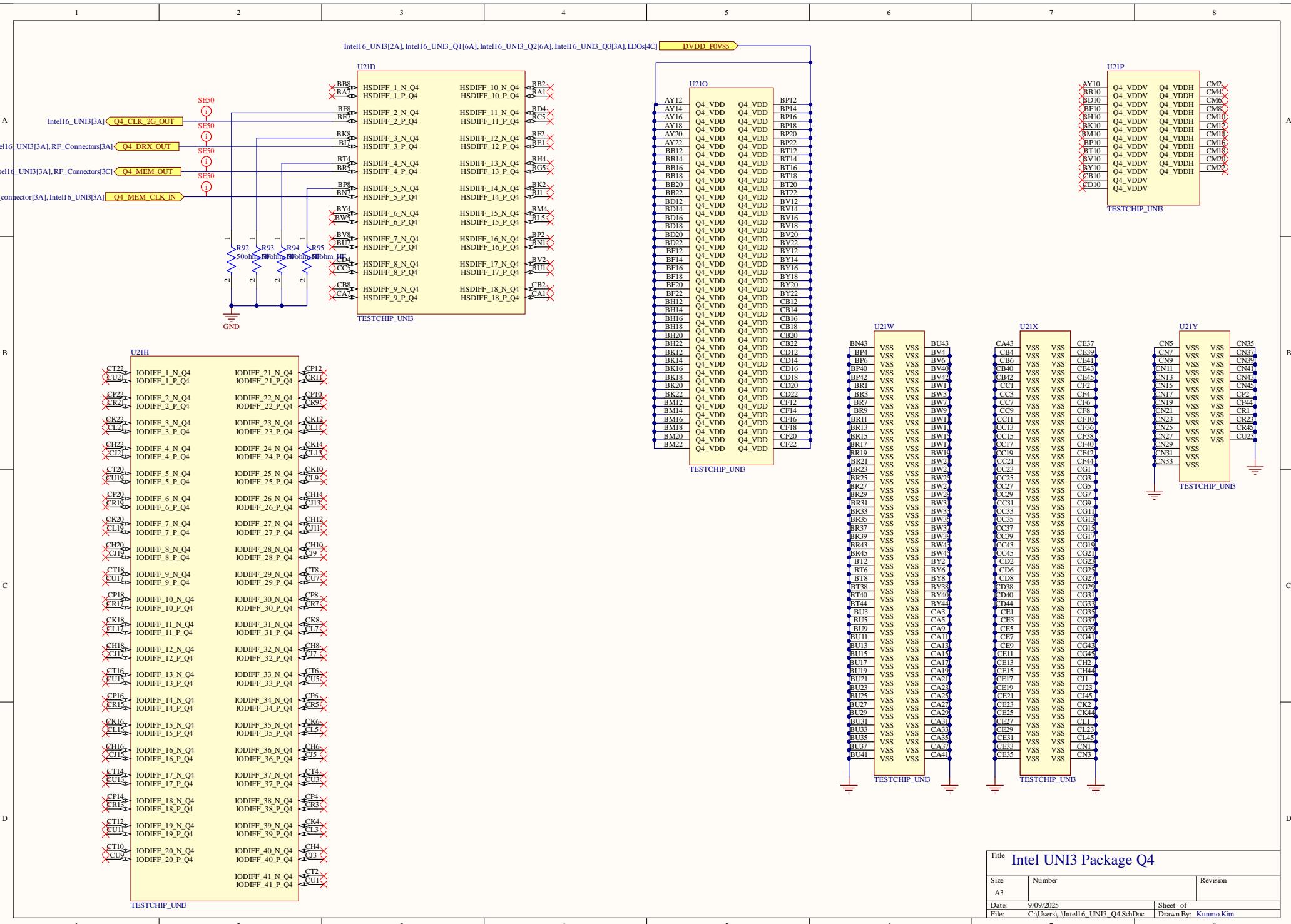
D

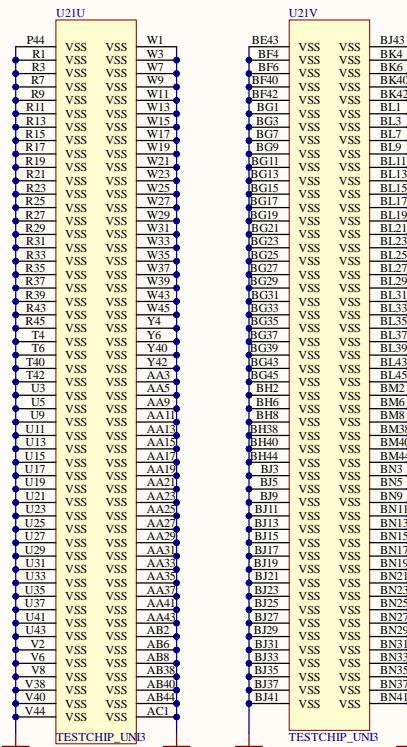
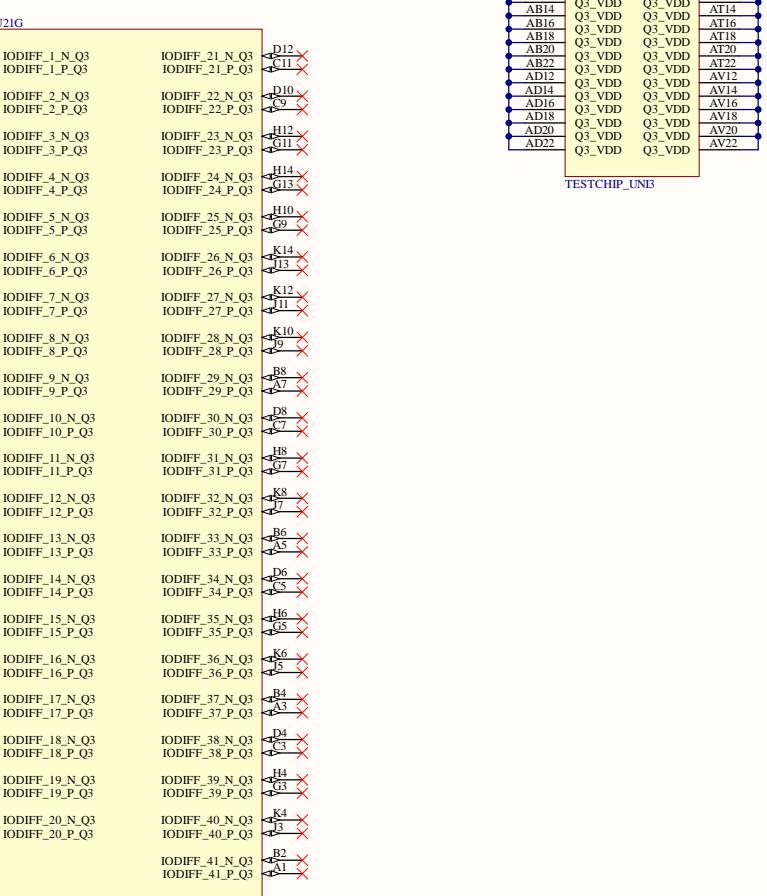
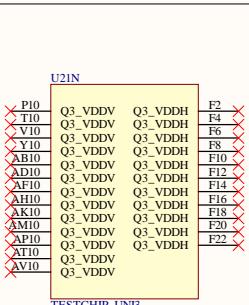
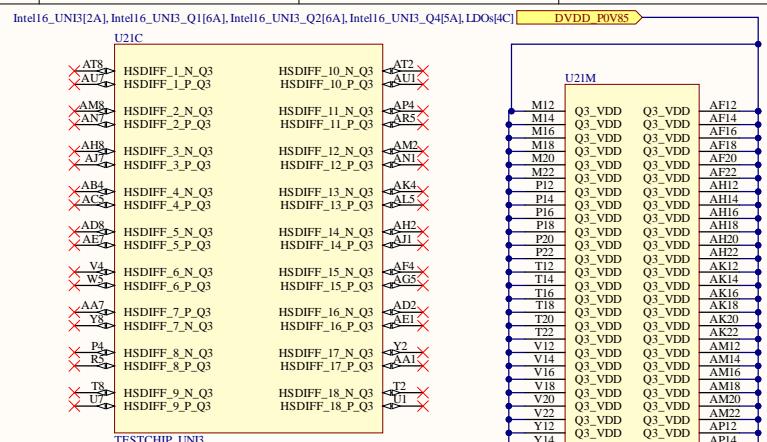


Title 16 GHz Clock Input

Size	Number	Revision
A4		
Date: 9/09/2025	Sheet of	
File: C:\Users..\CLK_16GHz.SchDoc		Drawn By: Kunmo Kim

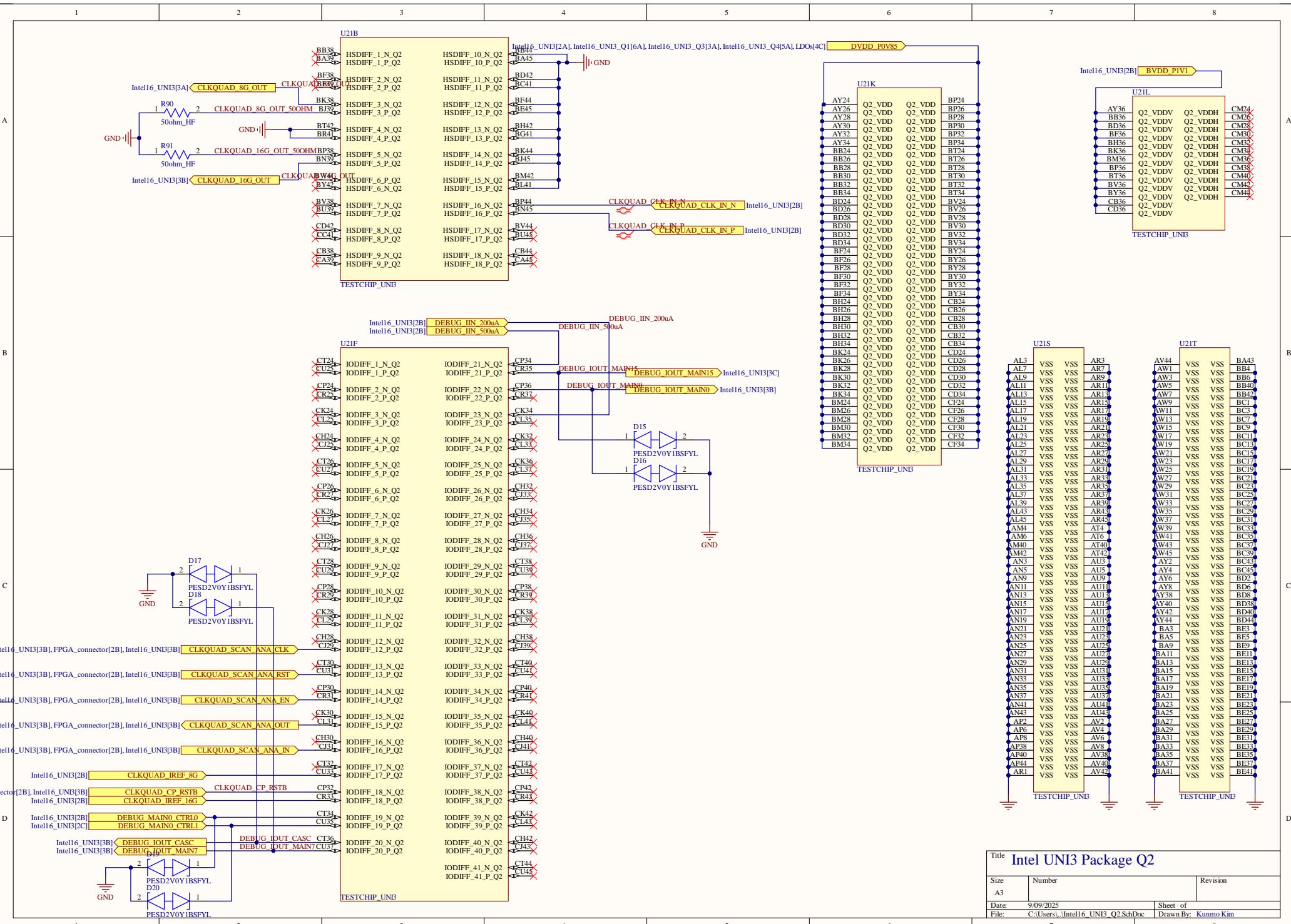






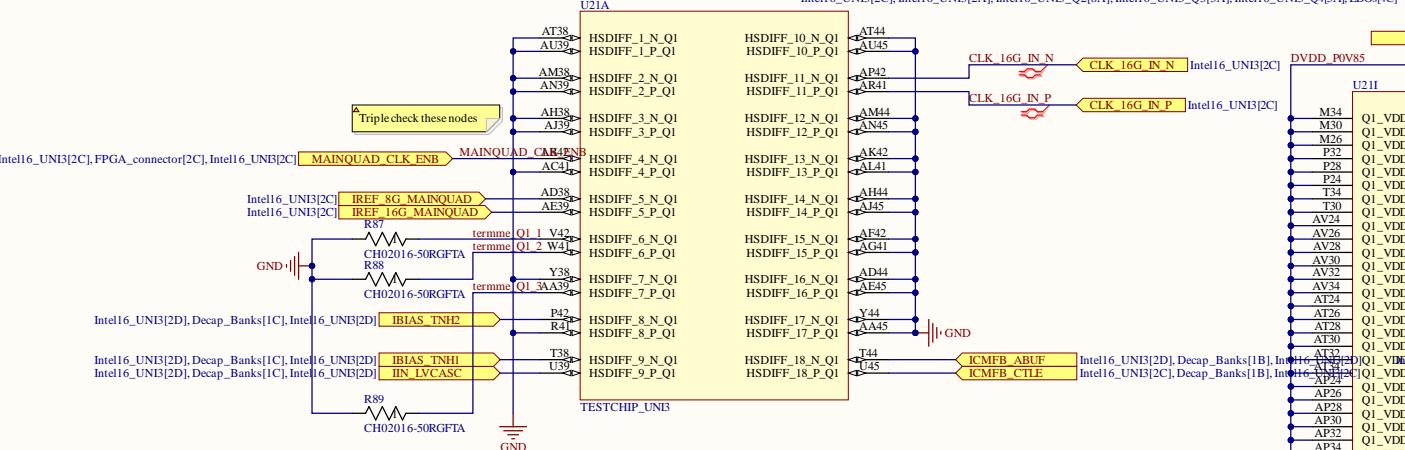
Title Intel UNI3 Package O3

Size	Number	Revision
A3		
Date: 9/09/2025	Sheet of	
File: C:\Users...\Intel116\UNI3\O3.SchDoc	Drawn By: Kunmo Kim	

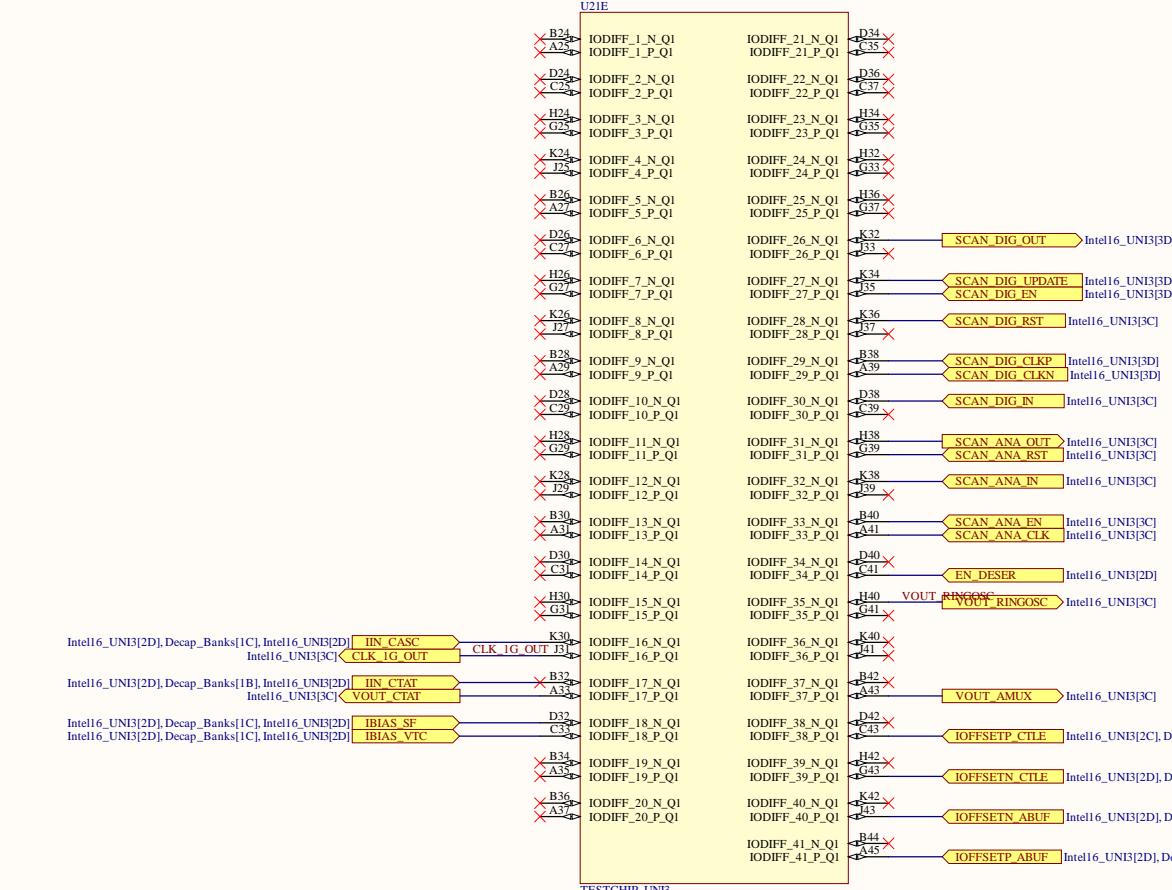


Intel16_UNI3[2C], Intel16_UNI3[2A], Intel16_UNI3_Q2[6A], Intel16_UNI3_Q3[3A], Intel16_UNI3_Q4[5A], LDOs[4C]

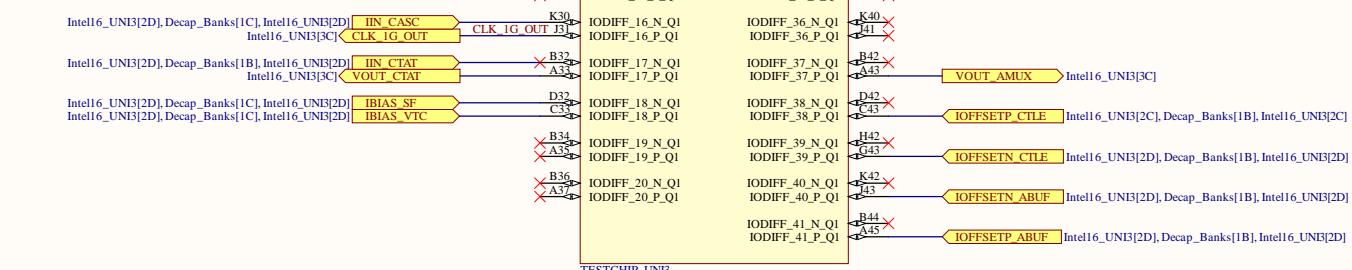
A



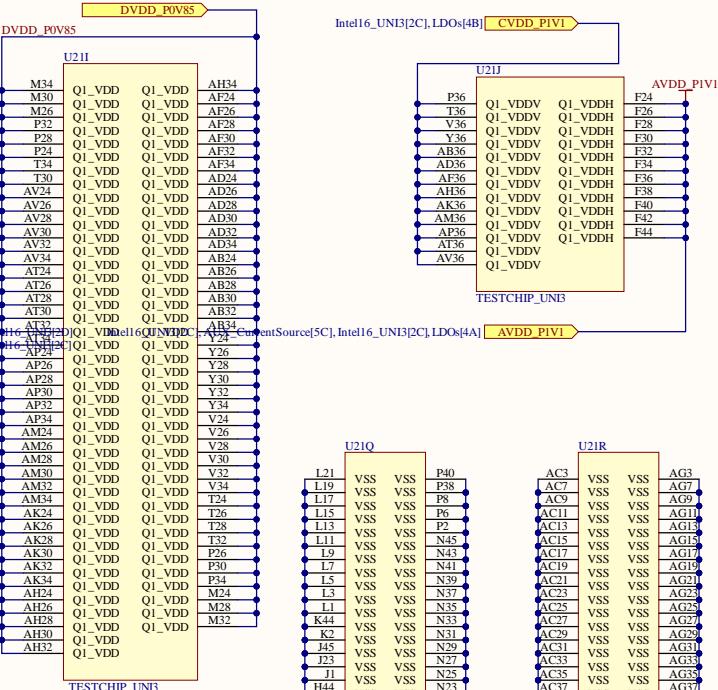
B



C

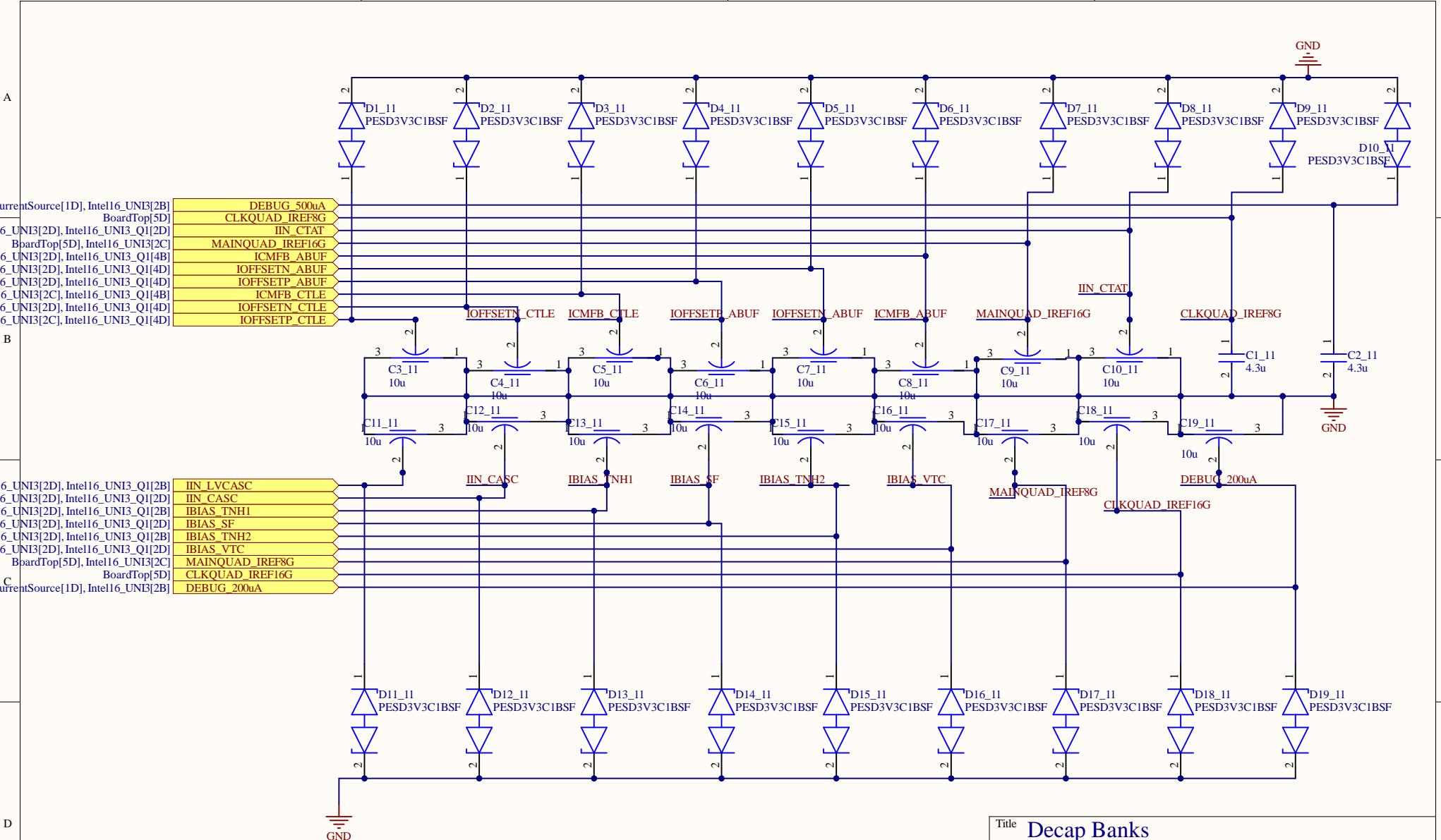


D



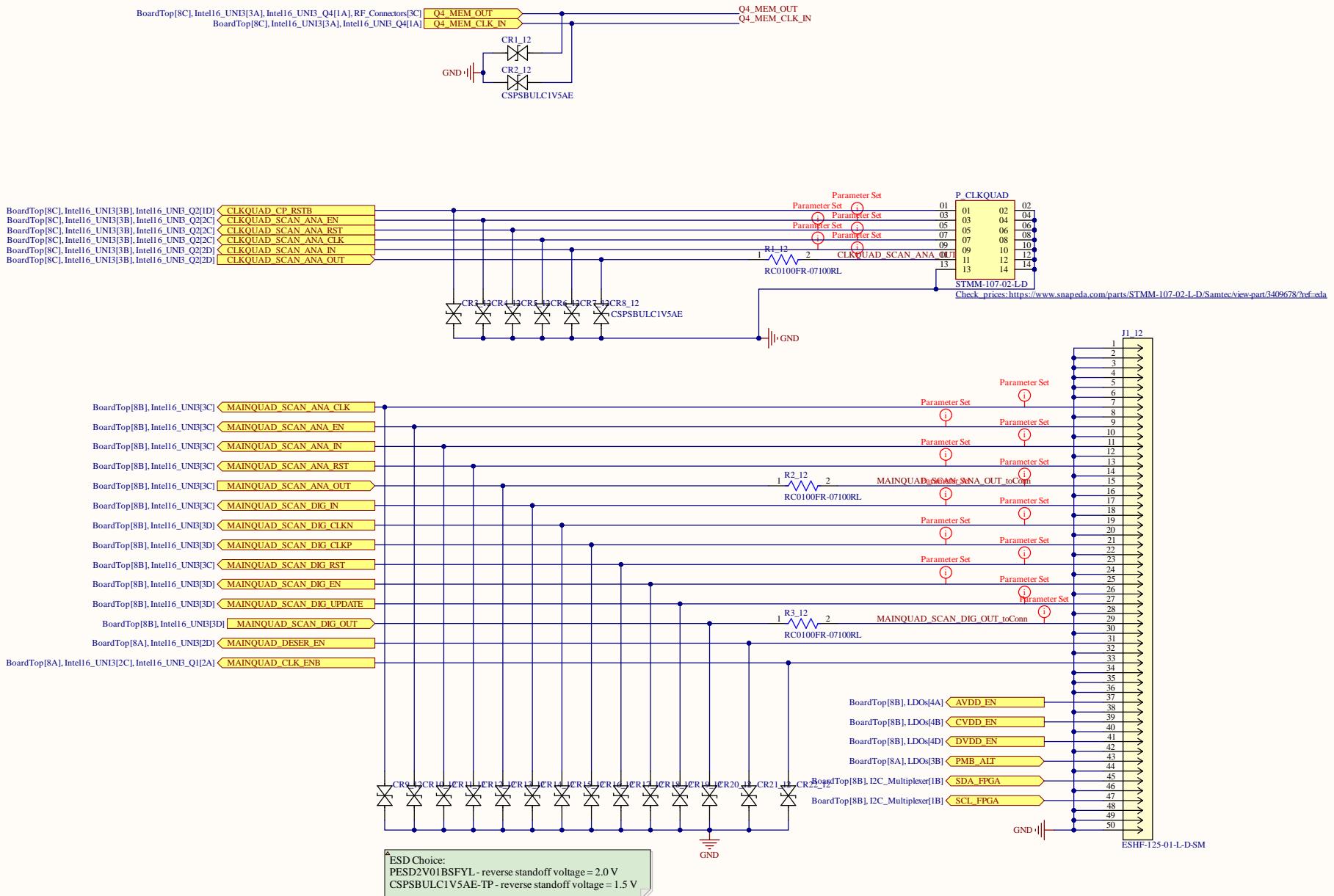
Title Intel UNI3 Package Q3

Size	Number	Revision
A3		
Date: 9/09/2025	Sheet of	
File: C:\Users\...\Intel16_UNI3.Q1.SchDoc	Drawn By: Kunmo Kim	



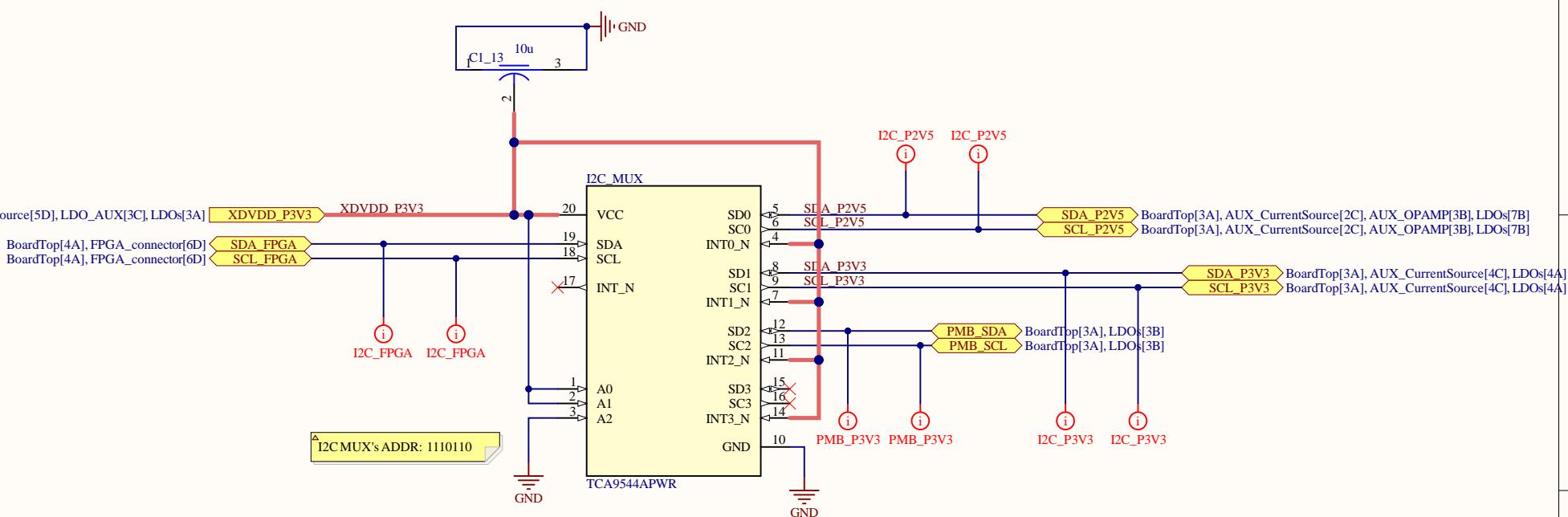
Title Decap Banks

Size	Number	Revision
A4		
Date: 9/09/2025	Sheet of	
File: C:\Users..\Decap_Banks.SchDoc		Drawn By: Kunmo Kim

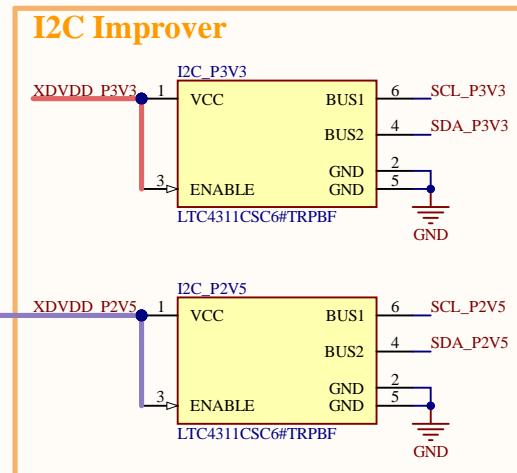
Title **FPGA Connector + ESD Protection**

Size	Number	Revision
A3		
Date: 9/09/2025	Sheet of	
File: C:\Users\...\FPGA_connector.SchDoc		Drawn By: Kunmo Kim

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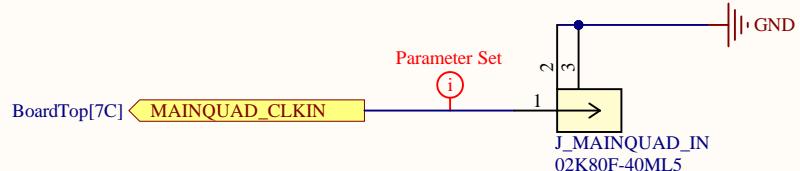


D

Title I2C Multiplexer		
Size A4	Number	Revision
Date: 9/09/2025	Sheet of	
File: C:\Users...\I2C_Multiplexer.SchDoc	Drawn By: Kunmo Kim	

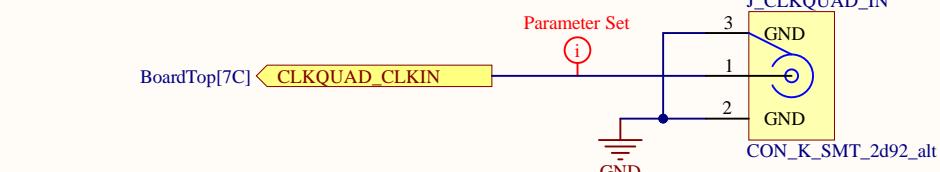
A

A



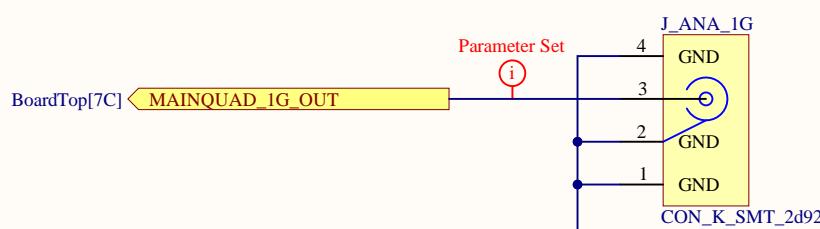
B

B



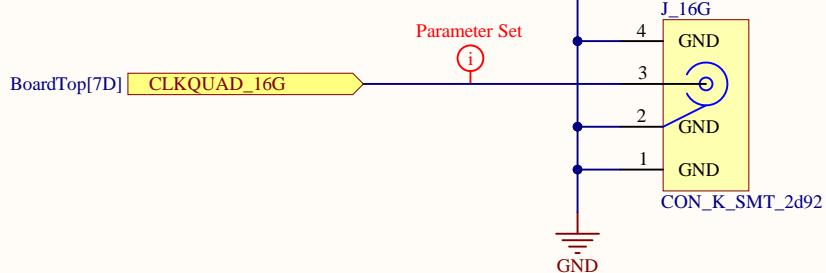
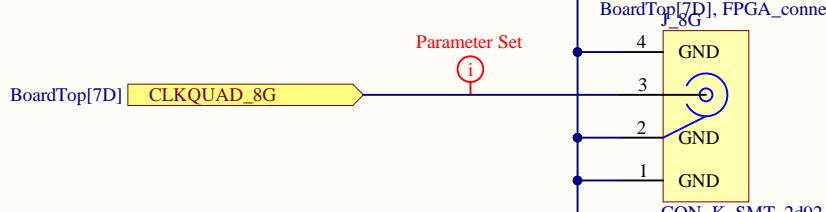
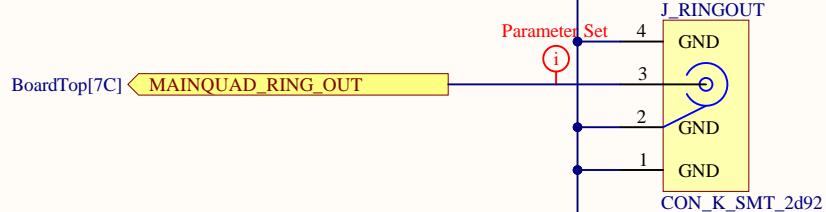
C

C



D

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Title RF Connectors

Size	Number	Revision
A		
Date: 9/09/2025	Sheet of	
File: C:\Users\..\RF_Connectors.SchDoc		Drawn By: Kunmo Kim

