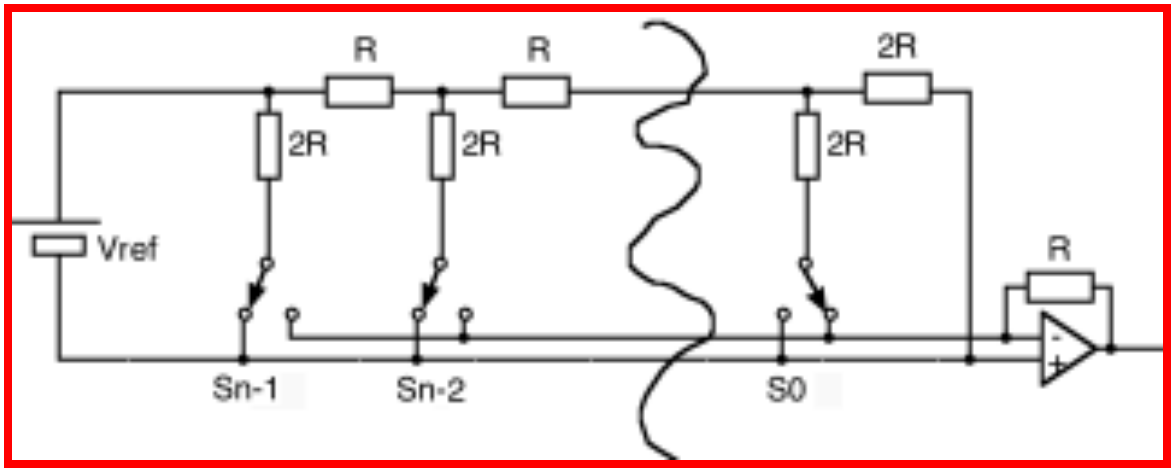
ECE3073 Computer Systems

Practice Questions

Analogue Interfacing

(i) Draw a circuit diagram of an INVERTED R-2R LADDER digital to analogue converter.



(ii) By referring to the diagram you drew for part (i) explain the operation of the INVERTED R-2R LADDER digital to analogue converter.

As current flows from the voltage reference Vref this current is successively divided in two. Half of the current flows down the vertical 2R resistor and the other half flows through the horizontal resistor R. The final horizontal resistor has a value of 2R to match the resistance seen by previous ladder rungs.

The total current flowing from Vref is Vref/R.

The result is that the current flowing towards the Sn-1 switch is (Vref/R)*0.5, Sn-2 is (Vref/R)*0.25, etc. (binary weighted currents).

Depending on the position of each switch the current passes to ground or it is passed to the summing junction of the amplifier. Thus the current into the amplifier is the sum of the selected binary weighted currents.

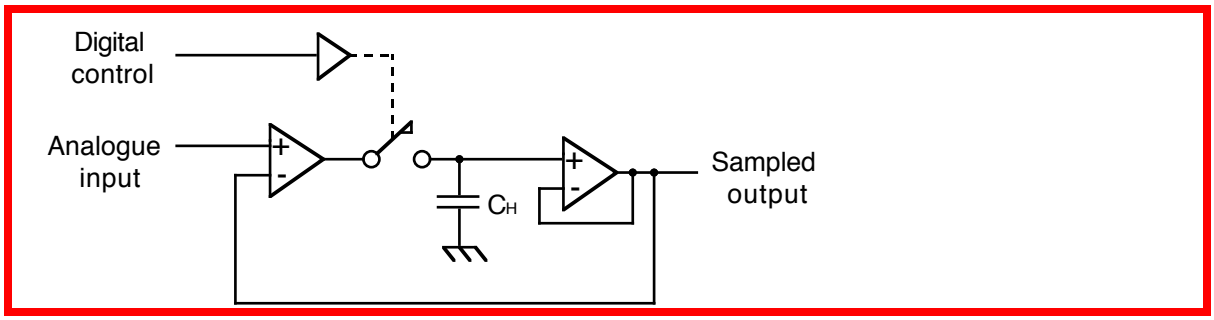
(iii) List the advantages of the INVERTED R-2R LADDER digital to analogue converter.

1) The inverted R-2R ladder DAC only uses two resistor values
2) The DAC draws a constant current from the reference source Vref.

(iv) Explain why the OUTPUT signal of a DIGITAL TO ANALOGUE CONVERTER is sometimes passed through a sample and hold circuit.

A digital system can output more than one analogue signal using a single DAC if each analogue output has its own sample and hold circuit. The DAC then cycles through each sample and hold outputting the voltage required for that circuit. The sample and hold samples its voltage from DAC and then holds it while the DAC moves on to the next one. Because the voltage stored on the sample and hold circuits drifts over time each one must be regularly 'refreshed' by sampling its specific voltage again.

(v) Draw a diagram showing the major components of a PRACTICAL sample and hold circuit.



(vi) Explain the function of each of the components in your diagram of a sample and hold

The left-hand amplifier provides a high input impedance for the sample and hold circuit so that it does not 'load' the source and a low output impedance to quickly charge the hold capacitor C_H.

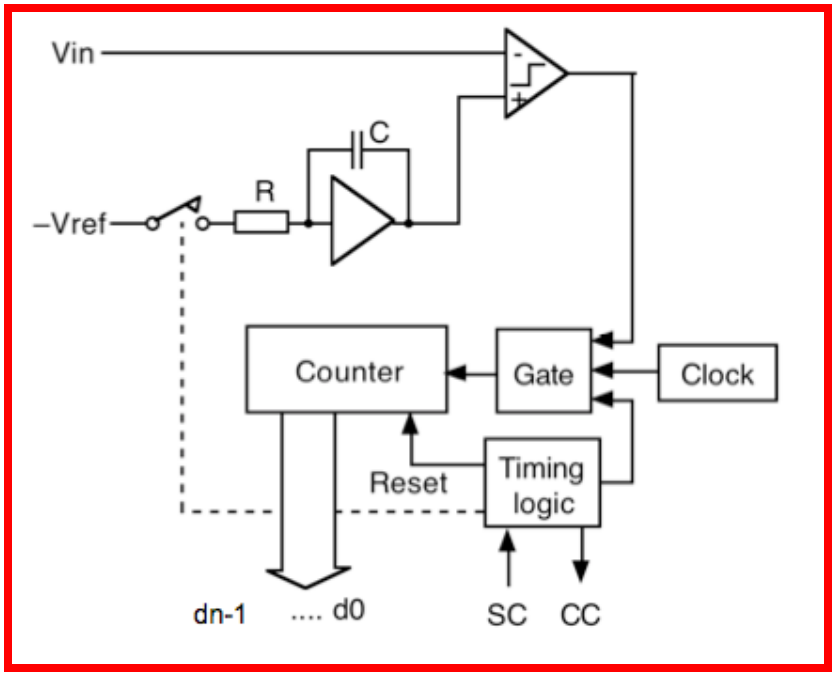
The digital controlled switch connects the analogue input signal to the capacitor during the sample period and disconnects during the hold period.

Hold capacitor C_H maintains the sampled value of the analogue input when the switch is open.

The right hand unity gain amplifier has a high input impedance so that it does not discharge C_H during the hold period and a low output impedance to drive an external load.

Feedback from the output to the left-hand amplifier maintains an all-over unity gain for the circuit.

(vi) Draw a diagram showing the major components of a single-slope analogue to digital converter.



(vii) Describe how the single-slope analogue to digital converter functions. Your description should incorporate the equations governing its operation.

When the start conversion signal (SC) is asserted the counter is zeroed and the integrator capacitor is discharged. Then the switch connecting –Vref to the integrator is closed and clock pulses are gated through to the counter.

The output of the integrator linearly increases with time until its value exceeds the unknown analogue input Vin. When this happens the output of the comparator changes state.

The change in the comparator output stops the clock pulses going to the counter. The counter value is then proportional to the unknown voltage Vin

$$Vin = -\frac{1}{RC}\int_0^T -Vref\ dt$$

$$Vin = \frac{VrefT}{RC}$$

provided that Vref, R and C are all constant. By correct choice of Vref, R and C the counter count can be directly scaled to indicate voltage in volts.

(viii) Explain the advantages and disadvantages of the single-slope analogue to digital converter.

Advantages: Being an integrating converter high frequency noise is reduced by the integrator which acts like a low-pass filter.

Disadvantages: Accuracy depends on the values of Vref, R, C and the precise measurement of time. With the availability of crystal controlled oscillators time can be measured accurately. Precise and stable resistors and capacitors are expensive. There will always be drift with temperature and time. Bandgap voltage sources are accurate and stable.

Calculation Questions

i) For a 10-bit digital to analogue converter with a 5 volt reference voltage and gain factor of 1 calculate the converter step size.

Step Size = (k Vref) / (2^n)

Where k=1
Vref = 5V
N = 10

Step Size = $1*5/2^{10}$ = 5/1024 = 4.883mV

ii) For a 12-bit analogue to digital converter with a reference voltage of 10V what digital output (in binary) would you expect for an analogue input of 4.7Volts?

Step Size = (k Vref) / (2^n)

Where k=1
Vref = 5V
N = 12

Step Size = $1*10/2^{12}$= 10/4096 = 2.44mV
Therefore the number of steps required to equal 4.7V is

Digital output = 4.7/0.00244 = 1926.23

ADC will round the result

Rounded digital output = 1926

2)1926 = 963 r0
2)963 = 481 r1
2)481 = 240 r1
2)240 = 120 r0
2)120 = 60 r0
2)60 = 30 r0
2)30 = 15 r0

2)15 = 7 r1
2)7 = 3 r1
2)3 = 1 r1
2)1 = 0 r1

The binary output is = 111 1000 0110

iii) For an 8-bit digital to analogue converter with a reference voltage of 12V what output voltage would you expect for a digital input of 0x15?

Step Size = (k Vref) / (2^n)

Where k=1
Vref = 12V
N = 8

Step Size = 1*12/2^8 = 12/512 = 23.44mV

0x15 = 21 in decimal

Output voltage = number of steps * step size = 21 * 0.02344 = 0.4922V

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