ECE3073 Computer Systems

Practice Questions

Performance Enhancement

i) In the context of computer cache memory explain the following terms:

a) spatial coherence

If a processor accesses a particular memory location the chances are it will access an adjacent memory location soon.

b) temporal coherence

If a processor accesses a particular memory location the chances are it will access the same memory location again soon.

c) cache hit

A cache hit occurs when a computer requests the contents of a particular memory location and the cache contains that information and can provide it without accessing main memory.

ii) What is the average memory access time of a computer whose hit rate is 93% with a cache access time of 5 ns and a main memory access time of 80 ns?

$t_{av} = h * t_{cache} + (1 - h)\, t_{main}$

$= 0.93 * 5 * 10^{-9} + (1 - 0.93) * 80 * 10^{-9}$

10.25 ns

iii) If we want an average memory access time of 6.5 ns, our cache access time is 5 ns and our main memory access time is 80 ns, what cache hit rate must we achieve?

$h = (t_{av} - t_{main}) / t_{cache} - t_{main})$

$= (6.5 * 10^{-9} - 80 * 10^{-9}) / (5 * 10^{-9} - 80 * 10^{-9})$

$= 0.98$

iii) How does pipelining increase the throughput of a computer?

Pipelining divides the computer datapath into a number of sequential combinatorial logic blocks and places a bank of registers between each block.

Without the pipelining only one instruction can be processed by the datapath and the system must wait for the instruction to propagate the full length of the datapath before starting the next one. With pipelining a new instruction can be introduced into the datapath after the previous instruction has propagated through the first logic block and the result latched into the register between the first and second logic block. If the datapath is divided into n logic blocks then (in theory) n instructions can be processed in the time it takes a non-pipelined datapath to process a single instruction.

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