ECE3073 Computer Systems

Practice Questions

Bus Interfacing

i) What is the minimum number of address lines required to address the following items is a byte-wide memory map?

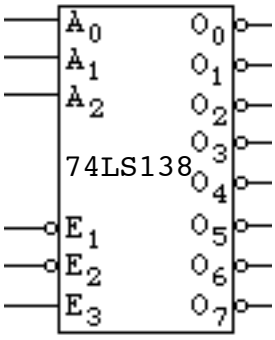
a) 1024 kbytes of RAM
b) 3 by 16bit input devices
c) 512 kbytes of ROM
d) 1024 LEDs organised in groups of 8

ii) A 74LS138 decoder is to provide the chip select signals for eight memory chips. Draw a diagram of the connections (using a minimum of additional logic functions) between a 16-bit address bus and the decoder chip to provide 8 chip selects with the following address ranges:

74LS138 output	Address range
0	C100 - C1FF
1	C500 - C5FF
2	C900 - C9FF
3	CD00 - CDFF
4	D100 - D1FF
5	D500 - D5FF
6	D900 - D9FF
7	DD00 - DDFF

Address			Enable			Outputs							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

Truthtable for 74LS138 decoder



Decoder chip logic symbol.

iii) When a microprocessor system outputs parallel digital data via a PIO (Parallel Input/Output) circuit this causes a sequence of signals to appear on the system data, address and control busses. Briefly describe these signals and explain how they result in a change in the digital output of the PIO.

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