ECE3073 Computer Systems
Mid-Semester Test 2012

50 minutes duration, closed book, no calculators
Total test marks are 20.
DO NOT USE RED PEN TO ENTER YOUR ANSWERS

Family Name ……Given Name ……

ID# .....

Question 1 (6 marks)

For the Nios processor what are the three kinds of exceptions (interrupts) that can trigger a context switch?

1)…… 1

2)…… 1

3)…… 1

There are four conditions that must be satisfied before a rising edge on a PIO input of a Nios processor will cause an interrupt. Fill in the three missing conditions:

1) Using SOPC Builder the PIO must be configured to set up rising edge triggered interrupts .

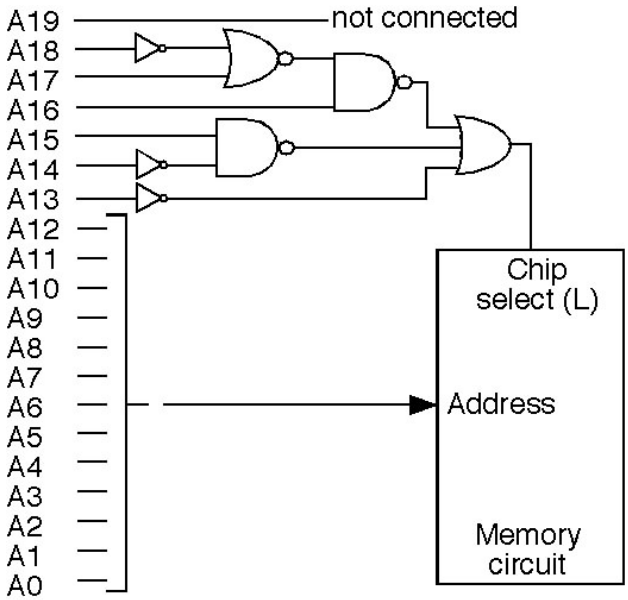
2) …… 1

3) …… 1

4) …… 1

Question 2 (6 marks)

In a microprocessor system with a 20-bit address bus (A0 to A19) the following circuit is used as address decoding logic for a block of memory to produce a memory select signal asserted low:



a) What is the size of the block of memory in kilobytes?

…… 2

b) What is the pattern of digital inputs to the logic that results in the memory block being selected?

A19 =
A18 =
A17 =
A16 =
A15 =
A14 =
A13 =

Deduct half a mark for each mistake 2

c) Give the address ranges over which the memory block will be addressed (in hexadecimal notation)

…….. 1

…….. 1

Question 3 (4 marks)

If 8-bit asynchronous serial data is transmitted with no parity and one stop bit what is the maximum error that can occur between the transmitting and receiving clocks before this error will cause a problem?

Note: because you do not have a calculator you can just give the equation for the result.

Mark for appropriate working 

Mark for the correct answer 

Question 4 (4 marks)

With reference to memory caches give a short description of each of the following terms:

1) compulsory miss:

……..

……..

……..

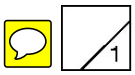
 

2) capacity miss:

……..

……..

……..

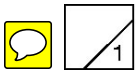


3) conflict miss:

……..

……..

……..



4) cache write through:

……..

……..

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******* END OF THE TEST ********