2013 Unit Guide

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ECE3073
Computer Systems

For the unit synopsis see the University Handbook:

http://www.monash.edu.au/pubs/handbooks/units/ECE3073.html

Mode of Delivery	**Clayton, Malaysia**
Workload requirements	Refer to handbook: http://www.monash.edu.au/pubs/2013handbooks/units/index-byfaculty-eng.html
Unit Relationships	Refer to handbook: http://www.monash.edu.au/pubs/2013handbooks/units/index-byfaculty-eng.html
Prerequisites	Refer to handbook: http://www.monash.edu.au/pubs/2013handbooks/units/index-byfaculty-eng.html
Co-requisites	Refer to handbook: http://www.monash.edu.au/pubs/2013handbooks/units/index-byfaculty-eng.html
Prohibitions	Refer to handbook: http://www.monash.edu.au/pubs/2013handbooks/units/index-byfaculty-eng.html
Chief Examiner(s)	Refer to handbook: http://www.monash.edu.au/pubs/2013handbooks/units/index-byfaculty-eng.html
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SEMESTER 1, 2013
Unit URL http://moodle.vle.monash.edu/my/

MONASH University www.monash.edu

ACADEMIC OVERVIEW
Learning Outcomes

See: http://www.monash.edu.au/pubs/handbooks/units/ECE3073.html

Graduate Attributes
Monash prepares its graduates to be:

1. responsible and effective global citizens who:
    a. engage in an internationalised world
    b. exhibit cross-cultural competence
    c. demonstrate ethical values
2. critical and creative scholars who:
    a. produce innovative solutions to problems
    b. apply research skills to a range of challenges
    c. communicate perceptively and effectively

Engineers Australia stage 1 competencies

The Engineers Australia Policy on Accreditation of Professional Engineering Programs – requires that all programs ensure that their engineering graduates develop to a substantial degree the stage 1 competencies. Listed below are the activities in this unit that will help you to achieve these competencies.

Note: that not all stage 1 competencies are relevant to each unit.

Stage 1 competencies	**Activities used in this unit to develop stage 1 competencies**
PE1.1 Knowledge of science and engineering fundamentals	A series of laboratory exercises specifically designed to explore the basic techniques of designing and interfacing microprocessor systems, and the tools required to program them.
PE1.2 In-depth technical competence in at least one engineering discipline	Practical experience in designing, constructing and programming a modern, FPGA based, softcore microprocessor system.
PE1.3 Techniques and resources	Use of leading technology in laboratories including different FPGA devices, memory and a range of peripherals.
PE1.4 General knowledge	Designing a microprocessor to accept input from sensors and use output devices to affect the real world.

PE2.1Ability to undertake problem identification, formulation, and solution	Fault finding and debugging techniques to cover all aspects of hardware and software fault finding
PE2.2 Understanding of social, cultural, global, and environmental responsibilities and the need to employ principles of sustainable development	Examining the issues of what microprocessors can do, their potential hazards and how all microprocessor hardware must be treated with respect. The risks and hazards involved in poor design and programming
PE2.3 Ability to utilise a systems approach to complex problems and to design and operational performance	Data Flow Modelling of software. Memory Map model of microprocessor hardware interfacing.
PE2.4 Proficiency in engineering design	A series of laboratories to explore each of the fundamental techniques required to program any complementary microprocessor system.
PE2.5 Ability to conduct an engineering project	Interrupt programming, Peripheral interfacing.
PE2.6 Understanding of the business environment	Cost effectiveness of design. The design Cycle model.
PE3.1 Ability to communicate effectively, with the engineering team and with the community at large	Labwork group discussions and presentation of results to lab demonstrators
PE3.2 Ability to manage information and documentation	Ability to manage complex software and hardware design projects in an environment typically found in an industrial environment .
PE3.3 Capacity for creativity and innovation	When preformed correctly the laboratory exercises provide the opportunity for students to be creative.
PE3.4 Understanding of professional and ethical responsibilities, and commitment to them	Safety and reliability of design. Design and test for reliability. Maintenance of a system in the field.
PE3.5 Ability to function effectively as an individual and in multidisciplinary and	Students are encouraged to ask questions, share their experiences and

multicultural teams, as a team leader or manager as well as an effective team member	knowledge with others.
PE3.6 Capacity for lifelong learning and professional development PE3.7 Professional attitudes	This unit exemplifies the need for practice and planning. Lab exercises require a degree of self-motivated learning which is an essential part of life-long learning

UNIT SCHEDULE

Week	Activities	Assessment
0		No formal assessment is undertaken in week 0
1	Lectures: • Unit introduction • Nios programmer's model * Nios assembler and machine code	Read the notes on safety and complete the safety quiz
2	Lectures: • Responding to outside events • Synchronous and asynchronous transfers • polling, interrupts and DMA	Lab 1 Altera Monitor and Nios machine code
3	Lectures: • Bus structures • Memory devices • Bus interfacing and address decoding • Parallel interfaces	Lab 2 Nios assembler and instruction timing
4	Lectures: • I2C • Asynchronous serial communications	Lab 3 Polling and polling latency in C
5	Lectures: • Improving processor performance • Cache and pipelining	Lab 4 Interrupts and interrupt latency
6	Lectures: • Analogue interfacing • ADC and DAC • Sample and hold, voltage references, etc.	Lab 5 Programming the serial interface
7	Lectures: Operating systems – process state, scheduling, structure, Timing requirements, hard and soft real time	Catchup lab Mid-semester test

	systems;	
8	Lectures: Task Creation and real time priorities and Process Statistics Scheduling policies – rate-monotonic, earliest-deadline-first.	Lab 6. Introduction to real time kernel
9	Lectures: Inter-process communication – blocking/non-blocking, semaphores, signals, shared memory, priority inversion	Lab 6. Introduction to real time kernel
10	Lectures: Program Design and Analysis: Models; Assembly and linking; Compilation techniques; Analysis and optimization of execution time, and program size;	Lab 7. Real time processes
11	Lectures: Program validation and testing;	Lab 7. Real time processes
12	Revision	Lab test
	SWOT VAC	No formal assessment is undertaken in SWOT VAC
	Examination period	LINK to Assessment Policy: www.policy.monash.edu/policybank/academic/education/assessment/assessment-in-coursework-policy.html

Assessment Summary

Assessment Task	Value	Due Date
1. Laboratory assessment	10%	End of associated lab period
2. Mid-semester test	10%	Administered in week 7
3. Lab test	10%	Administered in

		week 12
4. Written examination	70%	Exam period

Teaching and Learning Method

The unit consists of lectures and practical laboratories which are closely linked and demonstrate techniques for designing and programming microprocessor systems using industry based tools and software packages. The lectures are closely linked to the laboratories. Participation in lectures is strongly advised. Students are treated as adults and are expected to actively participate in the lectures, asking questions and participating in discussions. The laboratories will use an Altera FPGA based development board as the base however many of the tools and techniques discussed are applicable to many other families of microprocessor device. Students are actively encouraged to test their boundaries and limits in these labs and lectures.

Laboratory allocation

There are 3 hours of practice/ laboratory classes scheduled each week, commencing in week 2. Students must enroll in one practice class only using Allocate Plus. Students not allocated to a particular practice class will not be accepted into that session. Once a particular session is full, no more students will be accepted because of the limited amount of lab equipment and the need to provide an adequate number of demonstrators to cover lab numbers.

Communication, participation and feedback

Self-paced learning and feedback will be provided by a sequence of practice sheets which pose questions about the lecture material. Answers will be provided to allow students to gauge their understanding of the material. The mid-semester test and end of semester lab test will provide similar feedback. Exercises based on digital design and computer programming automatically provide a level of self-assessment. If the program/digital system function correctly then this indicates correctness at a functional level (however, there will be further criteria used to evaluate designs – cost, complexity, documentation, etc.)

Teaching Approach

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microprocessor device. Students are actively encouraged to test their boundaries and limits in these labs and lectures.

ASSESSMENT REQUIREMENTS

Assessment Tasks

It is a requirement of the Department of Electrical and Computer Systems Engineering that you complete a laboratory safety induction before working in the labs. Details of how to complete the safety induction will be provided on Moodle. If you have not completed the safety induction then you will not be allowed to do the laboratory exercises and no continual assessment marks will be entered under your name. As a result you will fail the unit.

Laboratory exercises will be marked in the lab sessions. The demonstrators will only enter marks for the current session or the immediate previous session. Lab marks are dependent on your completion of the preliminary work and how far you get in completing the lab exercise. Overall the lab marks correspond to 10% of your assessment in the unit. See the individual lab sheet for details of the marking scheme.

The mid-semester test will examine what you have learnt in the first 6 weeks of semester, both in lectures and labs. The test will contribute 10% to your final assessment.

An end of semester lab test will examine what you have learnt in the labs. The test will contribute 10% to your final assessment

Examination(s)

There will be a 3 hour written examination held during the semester 1 examination period. This will be worth 70% of the overall assessment for this unit. Students must achieve a mark of 45% or greater in this written exam and also in the continual assessment component to pass the unit. A further requirement to pass the unit is an overall mark of 50% or greater.

Learning resources

Recommended texts:

Wayne Wolf, Computers as Components: Principles of Embedded Computer System Design (2nd Edition), Morgan and Kaufmann

David A. Patterson and John, L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Morgan & Kaufmann

Feedback to you

All marks involving continual assessment will appear on Moodle when they are available. In addition you will see the mark that you get for each laboratory exercise and the lab test as it is entered by the demonstrator at the end of your lab/test. For the mid-semester test your test

paper will be returned to you after the marks have been entered on Moodle. The test papers will be returned during your lab period.

Examination material or equipment

The examination for ECE3073 is a closed book examination. You are NOT allowed to use calculators and there are no other specifically permitted items.

OTHER INFORMATION

Policies

Monash has educational policies, procedures and guidelines, which are designed to ensure that staff and students are aware of the University's academic standards, and to provide advice on how they might uphold them. You can find Monash's Education Policies at: www.policy.monash.edu.au/policy-bank/academic/education/index.html

Key educational policies include:

- Plagiarism;
- Assessment in Coursework Programs;
- Special Consideration;
- Grading Scale;
- Discipline: Student Policy;
- Academic Calendar and Semesters;
- Orientation and Transition; and
- Academic and Administrative Complaints and Grievances Policy.

Graduate Attributes Policy
http://www.policy.monash.edu/policy-bank/academic/education/management/monash-graduate-attributes-policy.html

Student Services
The University provides many different kinds of services to help you gain the most from your studies.Contact your tutor if you need advice and see the range of services available at www.monash.edu.au/students

Monash University Library
The Monash University Library provides a range of services, resources and programs that enable you to save time and be more effective in your learning and research. Go to www.lib.monash.edu.au or the library tab in my.monash portal for more information.

Disability Liaison Unit
Students who have a disability or medical condition are welcome to contact the Disability Liaison Unit to discuss academic support services. Disability Liaison Officers (DLOs) visit all Victorian campuses on a regular basis.

- Website: www.monash.edu/equity-diversity/disability/index.html
- Telephone: 03 9905 5704 to book an appointment with a DLO;
- Email: dlu@monash.edu
- Drop In: Equity and Diversity Centre, Level 1, Building 55, Clayton Campus.

Your Feedback to Us

Monash is committed to excellence in education and regularly seeks feedback from students, employers and staff. One of the key formal ways students have to provide feedback is through the Student Evaluation of Teaching and Units (SETU) survey. The University's student evaluation policy requires that every unit is evaluated each year. Students are strongly encouraged to complete the surveys. The feedback is anonymous and provides the Faculty with evidence of aspects that students are satisfied and areas for improvement.

For more information on Monash's educational strategy, see: www.monash.edu.au/about/monash-directions/directions.html and on student evaluations, see: www.policy.monash.edu/policy-bank/academic/education/quality/student-evaluation-policy.html

Previous Student Evaluations of this Unit

Student feedback has highlighted the following strength(s) in this unit:

Many students found the laboratory exercises particularly challenging and satisfying to solve.

Student feedback has also informed improvements to this unit, including:

Practice questions and answers were introduced to provide a better idea of the kinds of questions that would be asked in the written exam and the level of answers that are expected.

If you wish to view how previous students rated this unit, please go to https://emuapps.monash.edu.au/unitevaluations/index.jsp