ECE3073 Computer Systems

Practice Questions

Bus Interfacing

i) What is the minimum number of address lines required to address the following items is a byte-wide memory map?

a) 1024 kbytes of RAM
b) 3 by 16 bit input devices
c) 512 kbytes of ROM
d) 1024 LEDs organised in groups of 8

Answer

a) 1 kbyte = 1024 bytes = 2^{10} bytes

1024 kbytes = 1024 * 2^{10} bytes = 2^{20} bytes

therefore, this requires 20 address lines to address each individual byte.

b) each 16 bit input device will be addressed as 2 bytes

3 by 16 bit input devices represent 6 bytes in total

2^n <= 6 where n is the number of address lines to address 2^n bytes

therefore n = 3

c) 512 kbytes = 512 * 2^{10} bytes = 2^{19} bytes

therefore, this requires 19 address lines to address each individual byte

d) 1024 LEDs represents 128 groups of 8

128 = 2^7

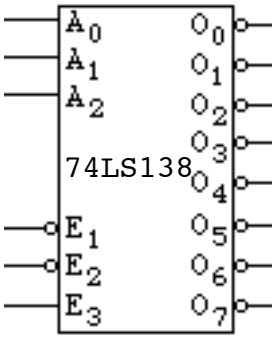
Therefore, 7 address lines are required to address all of the LEDs

ii) A 74LS138 decoder is to provide the chip select signals for eight memory chips. Draw a diagram of the connections (using a minimum of additional logic functions) between a 16-bit address bus and the decoder chip to provide 8 chip selects with the following address ranges:

74LS138 output	Address range
0	C100 - C1FF

1	C500 - C5FF
2	C900 - C9FF
3	CD00 - CDFF
4	D100 - D1FF
5	D500 - D5FF
6	D900 - D9FF
7	DD00 - DDFF

Address			Enable			Outputs							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H



Truthtable for 74LS138 decoder

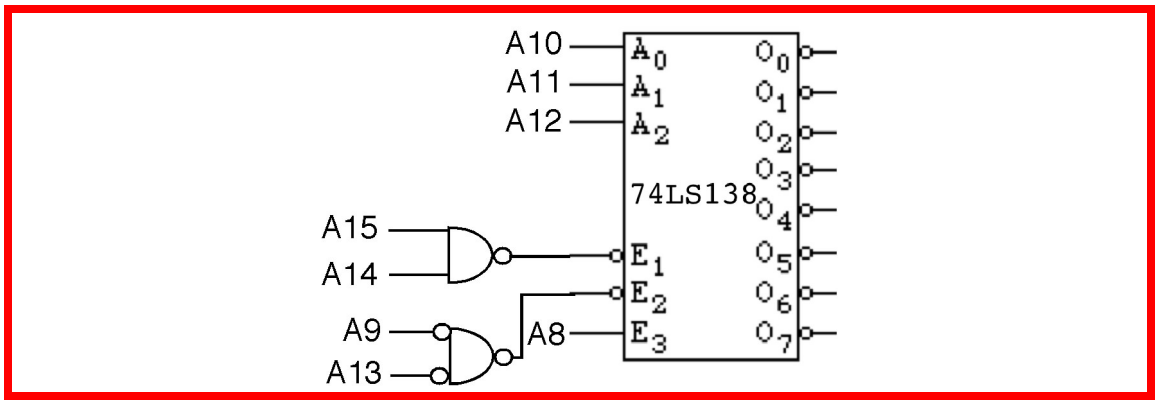
Decoder chip logic symbol.

Answer

Bits 0 to 7 of the address change within the address range and therefore these are the lines which go directly to the memory chip - we do not have to decode these lines.

Bit 15 is always '1'
Bit 14 is always '1'
Bit 13 is always '0'
Bits 12, 11, 10 change depending on which address range is selected
Bit 9 is always '0'
Bit 8 is always '1'

Therefore I will assign:



iii) When a microprocessor system outputs parallel digital data via a PIO (Parallel Input/Output) circuit this causes a sequence of signals to appear on the system data, address and control busses. Briefly describe these signals and explain how they result in a change in the digital output of the PIO.

The data register of the PIO will have a unique address in either the microprocessor memory space (for memory mapped peripherals) or I/O space (for I/O mapped peripherals). This address will be placed on the address bus.

At about the same time the digital data to be written to the PIO will be placed on the data bus.

A write operation will be performed to send data to the PIO so once the address and data busses have stabilised the write signal of the control bus will be asserted.

Decoding logic in the PIO will detect the matching address plus write signal and enable a register to latch the current contents of the data bus.

The contents of the register will then be amplified and made available to the outside world as the output of the PIO.

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