Jetson AGX Orin Series and Jetson AGX Xavier Series Interface Comparison and Migration

Application Note

Document History

DA-10655-001_v1.1

Version	Date	Description of Change
1.0	March 18, 2022	Initial release
1.1	March 29, 2022	• Added note to "Introduction" section • Updated functions in Table 5

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Introduction

This application note compares the features and interfaces supported on the NVIDIA® Jetson™ AGX Orin and NVIDIA® Jetson AGX Xavier™ Series modules. This application note also describes the migration path for designers familiar with Jetson AGX Xavier to design a carrier board for Jetson AGX Orin that will support the features available on Jetson AGX Orin.

> **Note**s:
> - References to Jetson AGX Orin applies to Jetson AGX Orin 32GB and Jetson AGX Orin 64GB except where explicitly noted.
> - References to Jetson AGX Xavier applies to Jetson AGX Xavier and Jetson AGX Xavier 64GB except where explicitly noted.

Jetson AGX Orin vs. Jetson AGX Xavier

Jetson AGX Orin and Jetson AGX Xavier are largely pin compatible. This section describes the differences between the modules.

The following figures show the Jetson AGX Orin and Jetson AGX Xavier block diagrams. The interfaces or blocks that are supported only by one of the modules are highlighted in red. The interface types that are supported on all three modules but where the number of lanes and instances, voltage level, or access is different, are highlighted in magenta.

Figure 1. Jetson AGX Xavier Block Diagram
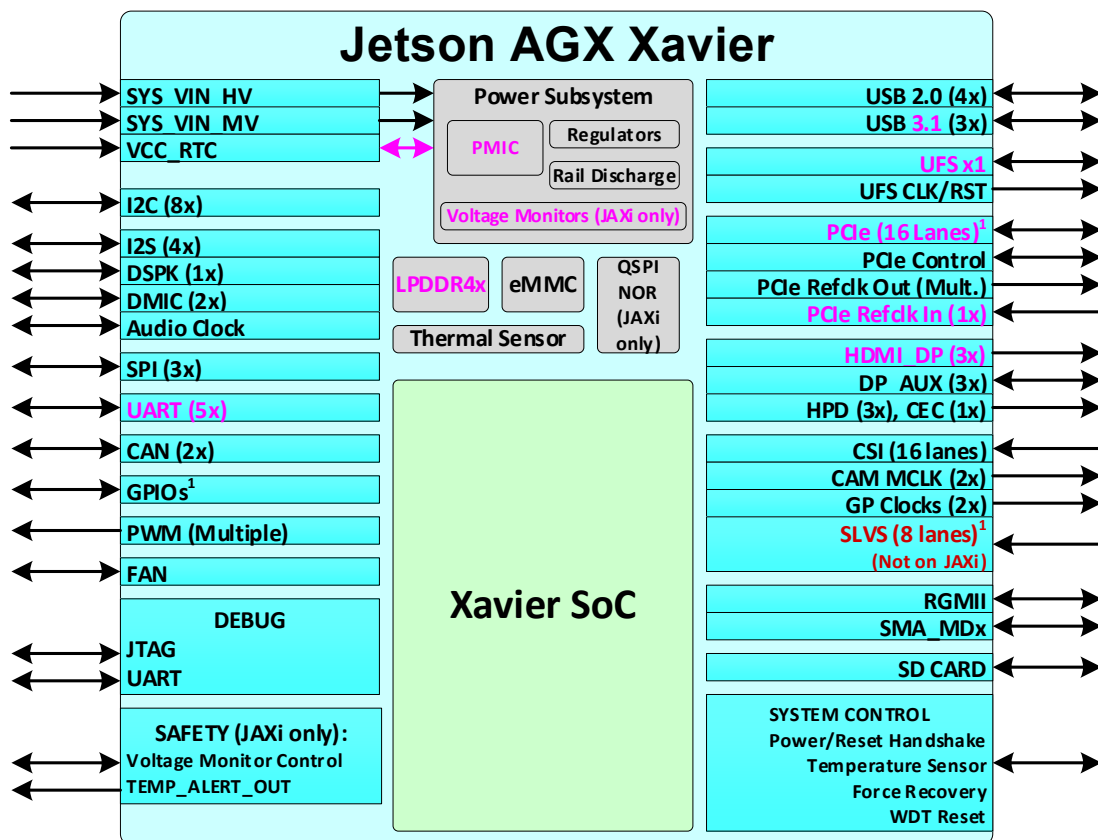
> **Note**: SLVS and PCIe share UPHY lanes.

Figure 2.   Jetson AGX Orin Block Diagram
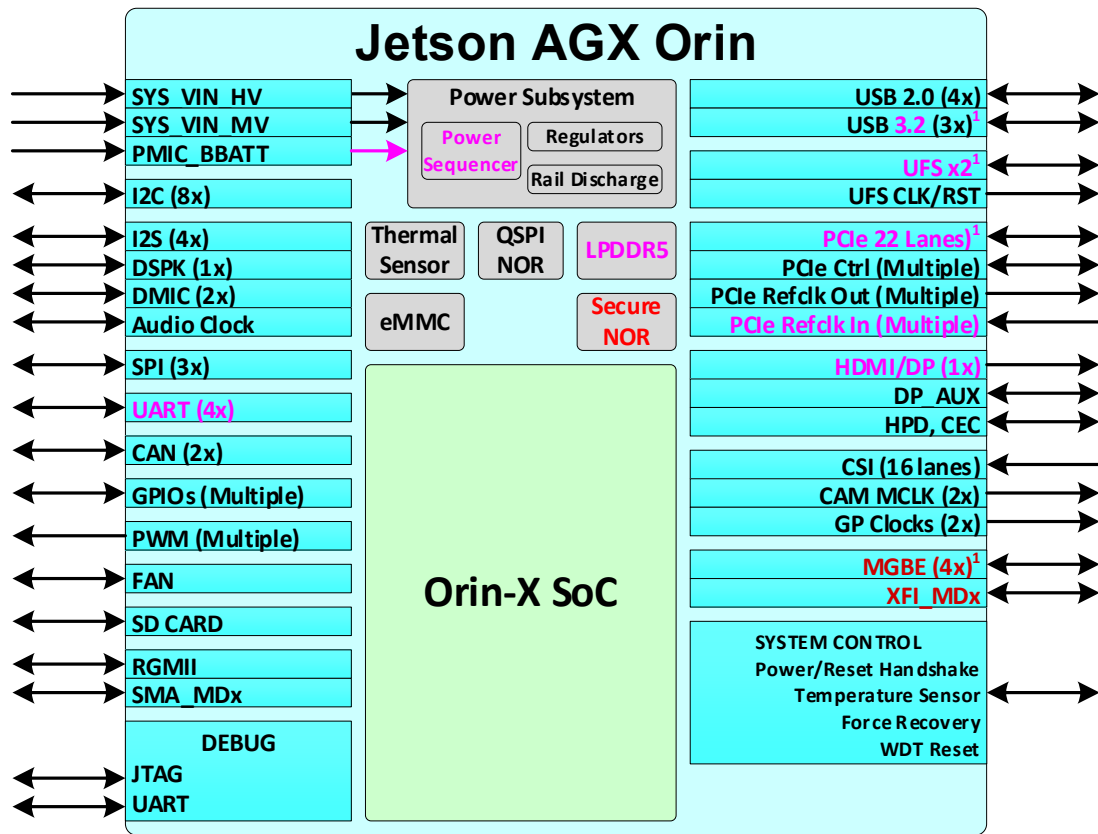
Note: One USB 3.2 port, UFS, and MGBE share UPHY lanes with PCIe.

Module Interface Comparisons

Table 1 lists the key system specifications, devices, and interfaces that are supported on either the Jetson AGX Orin series modules or the Jetson AGX Xavier series modules.

> 📝 **Note**: The commercial modules are the only modules covered in this application note.

Table 1.   Jetson AGX Orin and Jetson AGX Xavier Feature Comparison

Feature	Jetson AGX Xavier	Jetson AGX Xavier 64GB	Jetson AGX Orin 32GB	Jetson AGX Orin 64GB
System Specifications and Device on the Module				
AI Performance	32 INT8 Dense TOPs		200 INT8 Sparse TOPs	275 INT8 Sparse TOPs
GPU	NVIDIA Volta™ architecture with 512 NVIDIA CUDA cores and 64 Tensor cores. (22.6 Dense INT8 TOPs).		NVIDIA Ampere Architecture with 2048 NVIDIA® CUDA® cores and 64 Tensor Cores. (108 Sparse INT8 TOPs)	NVIDIA Ampere Architecture with 2048 NVIDIA® CUDA® cores and 64 Tensor Cores. (170 Sparse INT8 TOPs).
CPU	8-core NVIDIA Carmel Arm®v8.2 64-bit CPU, 8MB L2 + 4MB L3		8 core Cortex A78 ARM 64-bit CPU, 2 clusters (4x 256KB L2 + 2MB L3) + 4MB L4	12 core Cortex A78 ARM 64-bit CPU, 3 clusters (4x 256KB L2 + 2MB L3) + 4MB L4
DL Accelerator	2x NVDLA Engines (5.7 TOPs each)		2x NVDLA 2.0 Engines (48 TOPs each)	2x NVDLA 2.0 Engines (50 TOPs each)
Vision Accelerator	2x PVA v1		1x PVA v2	1 x PVA v2
Memory	16/32 GB, 137 GB/s	64 GB, 137 GB/s	32 GB, 204 GB/s	64 GB, 204 GB/s
Storage	32 GB eMMC		64 GB eMMC	
Networking RGMII MGBE	10/100/1000 Mbit Not Supported		10/100/1000 Mbit 4 x 10Gbe XFI	

Feature	Jetson AGX Xavier			Jetson AGX Xavier 64GB			Jetson AGX Orin 32GB			Jetson AGX Orin 64GB		
Video Decode	**H.265** 2x 8Kp30 6x 4K60 12x 4K30 26x 1080p60 52x 1080p30	**H.264** 4x4K60 8x4K30 16x1080p60 32x1080p30	**VP9** 4x4K60 8x4K30 18x1080p60 38x1080p30	**H.265** 1x8K30 2x4K60 4x4K30 9x1080p60 18x1080p30 **H.264** 1x4K60 2x4K30 5x1080p60 11x1080p30	**AV1** 1x8K30 2x4K60 4x4K30 8x1080p60 20x1080p30 **VP9** 15x1080p30		**H.265** 1x8K30 3x4K60 7x4K30 11x1080p60 22x1080p30 **H.264** 1x4K60 3x4K30 6x1080p60 13x1080p30	**AV1** 1x8K30 3x4K60 6x4K30 12x1080p60 24x1080p30 **VP9** 18x1080p30	
Video Encode	**H.265** 4x4K60 8x4K30 16x1080p60 32x1080p30	**H.264** 4x4K60 8x4K30 14x1080p60 30x1080p30	**VP9** 2x4K60 4x4K30 10x1080p60 20x1080p30	**H.265** 1x4K60 3x4K30 6x1080p60 12x1080p30 **H.264** 1x4K60 2x4K30 5x1080p60 11x1080p30	**AV1** 1x4K60 3x4K30 6x1080p60 12x1080p30		**H.265** 2x4K60 4x4K30 8x1080p60 16x1080p30 **H.264** 1x4K60 3x4K30 7x1080p60 14x1080p30	**AV1** 2x4K60 4x4K30 7x1080p60 15x1080p30	
Video Input CSI	16 lanes MIPI CSI-2 D-PHY 1.2 (40 Gbps) C-PHY 1.1 (62 Gbps)						16 lanes MIPI CSI-2 D-PHY 2.1 (40 Gbps) C-PHY 2.0 (164 Gbps)		
SLVS	8-lane						Not Supported		

Interfaces

USB 2.0	4x											
USB 3.x (Note 1)	3x (3.1) Gen2 (10 Gbps)						3x (3.2) Gen2 (10 Gbps)					
PCIe (Note 1)	2 x1 + 1 x2 + 1 x4 + 1 x8. PCIe Gen 4. All support Root Port. Only x8 has Root Port and Endpoint support. 1 x8 shared with SLVS						Up to 2 x8 + 1 x4 + 2 x1. PCIe Gen 4.All support Root Port. Only 2 x8 has Root Port and Endpoint support. 4 lanes of 1 x8 shared with MGBE.					
Display	Three multi-mode (2x 4K60) (e)DP 1.4/HDMI™ 2.0a						One multi-mode (8K60, 2x4K60), (e)DP 1.4 (HBR3, MST, DSCT), HDMI™ 2.1					
Camera	Up to 4x4 or 6x2 MIPI CSI interfaces 1 SLVS camera (Up to 8-lanes)						Up to 4x4 or 6x2 MIPI CSI interfaces SLVS Not Supported					
Audio I2S DMIC DSPK	4x 2x 1x						4x (compatible) + 2x additional 2x (compatible) + 2x additional 1x (compatible) + 1x additional					
SDIO/SD Card	1x SD Card/SDIO											
GbE	Supported											

Feature	Jetson AGX Xavier	Jetson AGX Xavier 64GB	Jetson AGX Orin 32GB	Jetson AGX Orin 64GB
MGBE (Multi-Gigabit Ethernet)	Not Supported		4x 10Gbe XFI (shared with 4 UPHY lanes)	
I2C	8x			
UART	5x		4x (compatible) + 2x additional (note 2)	
SPI	3x		3x (compatible) + 1x additional	
CAN	2x			
JTAG	Supported			
Fan	PWM and Tach Input			
Miscellaneous				
RTC Back-up	VCC_RTC (input/output). Supports rechargeable cells, non-rechargeable cells and super-caps.		PMIC_BBATT (input only) Supports non-rechargeable cells only	
WiFi	Requires external solution			
Mechanical	100 mm x 87 mm x 15.23 mm			
Power	10W|15W|30W		15W | 30W | 40W	15W | 30W | 50W Max Power Up to 60W
Input Voltage	HV rail: 9V to 20V MV rail: 5V		HV rail: 7V to 20V MV rail: 5V	

Note:

1. "compatible" means the same functionality exists on both Jetson AGX Orin and Jetson AGX Xavier on the same module pins.

2. Two of the additional UART functions share pins with other UARTs but are SBSA compliant.

Function and Interface Difference Details

Module Power

The following table lists the module power requirement for both the NVIDIA Jetson AGX Xavier series SOM and the Jetson AGX Orin Module.

Table 2.　　　Module Power Requirement

Features	Jetson AGX Xavier and Xavier 64GB	Jetson AGX Orin 64GB	Jetson AGX Orin 32GB
Thermal design power	10 W	15 W	15 W
	15 W	30 W	30 W
	30 W	50 W	40 W
		MAXN (Up to 60 W)	

Input Voltage Rails

Both Jetson AGX Xavier and Jetson AGX Orin have two main input supplies plus an RTC battery back-up supply.

Table 3.　　　Input Voltage Rails Power Supplies

| Power Rail	Jetson AGX Xavier and Xavier 64GB	Jetson AGX Orin 64GB	Jetson AGX Orin 32GB
SYS_VIN_HV	9V to 20V	7V to 20V	
SYS_VIN_MV	5V nominal	5V nominal	
Jetson AGX Xavier: VCC_RTC (Pin L53) Jetson AGX Orin: PMIC_BBATT (Pin D37)	2.5V to 3.3V nominal. Input for RTC back-up when system is off. Output to charge a super capacitor or rechargeable cell when system is on.	1.65V to 3.45V nominal. Supports input for RTC back-up when system is off. Supports only non-rechargeable cells.	

Mechanical Differences

Jetson AGX Orin and Jetson AGX Xavier have the same X/Y/Z dimensions as can be seen in Table 4.

Table 4.   Mechanical Differences

Feature	Jetson AGX Xavier and Xavier 64GB	Jetson AGX Orin 64GB	Jetson AGX Orin 32GB
Size	100 mm x 87 mm x 15.23 mm		
Built-in thermal solution	Thermal transfer plate (TTP)		
Thermal solution mounting	4x 2 mm diameter corner mounting holes		

Figure 3.   Jetson AGX Orin and Jetson AGX Xavier
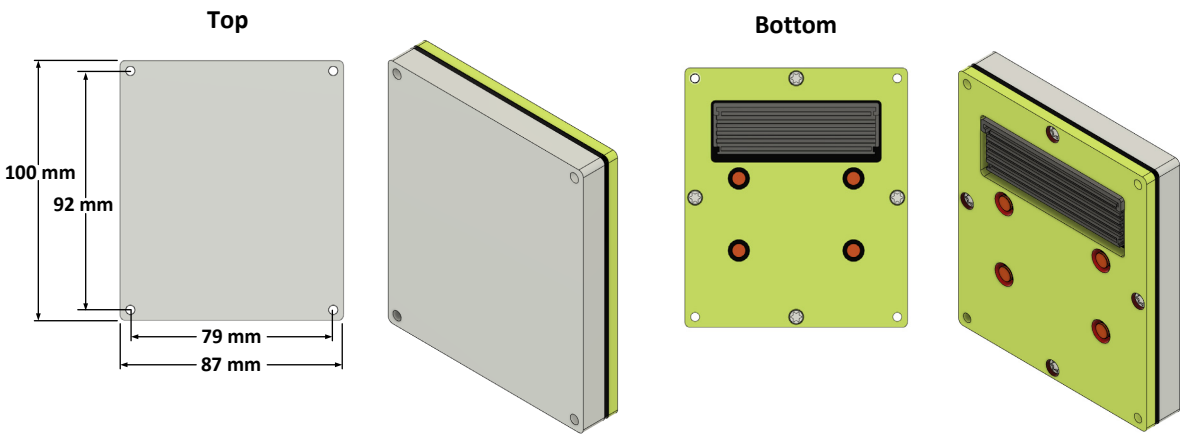
Interface Migration

This section shows the functional pin mapping options for the NVDIA Jetson AGX Xavier and the Jetson AGX Orin and how they align or differ.

USB 3.x, PCIe, UFS and MGBE Mapping Options

This section details the USB, PCIe, UFS, and MGBE mapping options for Jetson AGX Orin and Jetson AGX Xavier.

USB 3.x

Jetson AGX Xavier supports three USB 3.1 ports. Jetson AGX Orin supports up to three USB 3.2 ports. One of the ports is shared with a PCIe x1 interface. See the USB 3.x, PCIe, UFS, and MGBE mapping options table for where the USB 3.x ports map for each module.

PCIe

Jetson AGX Orin supports up to five PCIe interfaces (All Gen4 capable).

Jetson AGX Xavier supports five PCIe interfaces (All Gen4 capable). See Table 5 for details.

UFS

Jetson AGX Orin supports a two lane UFS interface [1:0] on UPHY[11:10). Jetson AGX Xavier supports a single lane UFS interface on UPHY10. This maps to the UFS Lane 1 on the NVIDIA® Xavier™ system-on-chip (SoC).

Multi-GigaBit Ethernet

Jetson AGX Orin supports up to four Multi-GigaBit Ethernet (MGBE) interfaces on UPHY[9:6]. Jetson AGX Xavier does not support this interface.

Table 5.   USB 3.x, PCIe, UFS, and MGBE Mapping Options

Jetson AGX Xavier Connector Pin Names	Jetson AGX Orin Pin Names	Orin UPHY Block and Lane		Jetson AGX Xavier Functions		Jetson AGX Orin Functions		
						Config #1	Config #2	Config #3
UPHY_RX0/TX0	UPHY_RX0/TX0	UPHY0, L0		PCIe x1 (C1), RP		USB 3.2 (P0)	PCIe x1 (C0), RP	
UPHY_RX1/TX1	UPHY_RX1/TX1	UPHY0, L1		USB 3.1 (P2)		USB 3.2 (P1)	USB 3.2 (P1)	USB 3.2 (P1)
NVHS1_RX0/TX0	UPHY_RX20/TX20	UPHY0, L2				USB 3.2 (P2)	USB 3.2 (P2)	USB 3.2 (P2)
NVHS1_RX1/TX1	UPHY_RX21/TX21	UPHY0, L3				PCIe x1 (C1), RP	PCIe x1 (C1), RP	
NVHS1_RX2/TX2	UPHY_RX22/TX22	UPHY0, L4				PCIe x4 (C4), RP	PCIe x4 (C4), RP	
NVHS1_RX3/TX3	UPHY_RX23/TX23	UPHY0, L5						
UPHY_RX10/TX10	UPHY_RX10/TX10	UPHY0, L6		UFS x1				UFS x2
UPHY_RX11/TX11	UPHY_RX11/TX11	UPHY0, L7		USB 3.1 (P3)				
NVHS0_SLVS_RX0/TX0	UPHY_RX12/TX12	UPHY1, L0		PCIe x8 (C5), RP/EP		PCIe x8 (C5), RP/EP	PCIe x8 (C5), RP/EP	PCIe x8 (C5), RP/EP
NVHS0_SLVS_RX1/TX1	UPHY_RX13/TX13	UPHY1, L1						
NVHS0_SLVS_RX2/TX2	UPHY_RX14/TX14	UPHY1, L2						
NVHS0_SLVS_RX3/TX3	UPHY_RX15/TX15	UPHY1, L3						
NVHS0_SLVS_RX4/TX4	UPHY_RX16/TX16	UPHY1, L4						
NVHS0_SLVS_RX5/TX5	UPHY_RX17/TX17	UPHY1, L5						
NVHS0_SLVS_RX6/TX6	UPHY_RX18/TX18	UPHY1, L6						
NVHS0_SLVS_RX7/TX7	UPHY_RX19/TX19	UPHY1, L7						
UPHY_RX2/TX2	UPHY_RX2/TX2	UPHY2, L0		PCIe x4 (C0), RP			PCIe x8 (C7), RP/EP	PCIe x1 (C7), RP/EP
UPHY_RX3/TX3	UPHY_RX3/TX3	UPHY2, L1						
UPHY_RX4/TX4	UPHY_RX4/TX4	UPHY2, L2						
UPHY_RX5/TX5	UPHY_RX5/TX5	UPHY2, L3						
UPHY_RX6/TX6	UPHY_RX6/TX6	UPHY2, L4		USB 3.1 (P0)		MGBE (C0)		MGBE (C0)
UPHY_RX7/TX7	UPHY_RX7/TX7	UPHY2, L5		PCIe x1 (C3), RP				MGBE (C1)
UPHY_RX8/TX8	UPHY_RX8/TX8	UPHY2, L6		PCIe x2 (C4), RP				MGBE (C2)
UPHY_RX9/TX9	UPHY_RX9/TX9	UPHY2, L7						MGBE (C3)

HDMI and DisplayPort Mapping Options

Jetson AGX Orin supports a single HDMI™, VESA® DisplayPort® (DP), and embedded DisplayPort (eDP) interface and supports multi-head support through MST. Jetson AGX Xavier supports three HDMI, eDP, and DP interfaces but does not support multi-head operation through MST. On Jetson AGX Orin, SFI, UPHY, and RSVD pins replace the missing interfaces on Jetson AGX Xavier.

Table 6.   HDMI and DisplayPort Mapping Options

Connector Signal Group	Jetson AGX Xavier Functions	Jetson AGX Orin Functions
HDMI_DP0_TX HDMI_DP0_RX	HDMI_DP0	RSVD
HDMI_DP1_TX HDMI_DP1_RX	HDMI_DP1	Misc. (PCIe Clock, etc.)
HDMI_DP2_TX HDMI_DP2_RX	HDMI_DP2	HDMI_DP2

Ethernet

Both Jetson AGX Orin and Jetson AGX Xavier support an RGMII Gigabit Ethernet interface at the module pins. Jetson AGX Orin also supports up to four MGBE interfaces. These share UPHY lanes with PCIe in one of the configurations supported. Jetson AGX Orin has four sets of XFI MDIO pins to go with the MGBE interfaces.

CSI

Jetson AGX Orin and Jetson AGX Xavier both support 16 MIPI CSI lanes and can support the following configurations to cameras or serializers:

- ▶ 4 x4
- ▶ 3 x4 + 2 x2
- ▶ 2 x4 + 4 x2
- ▶ 1 x4 + 5 x2
- ▶ 6 x2

SDIO and SD Card

Jetson AGX Orin and Jetson AGX Xavier both bring a single SDMMC interfaces to the module pins (SDCARD pins supporting SD Card or SDIO).

Audio

Jetson AGX Orin and Jetson AGX Xavier both support up to four I2S interfaces. In addition, both support a master audio clock and both Digital Microphone (DMIC) and Digital Speaker (DSPK) interfaces.

Table 7.   Jetson AGX Orin and Jetson AGX Xavier Audio Interfaces

Pin #	Function	Jetson AGX Orin Signal Name	Orin SoC Signal Name	Jetson AGX Xavier Signal Name	Xavier SoC Signal
L14	I2S1	I2S1_CLK	GP169	I2S1_CLK	DAP1_SCLK
D8		I2S1_FS	GP172	I2S1_FS	DAP1_FS
C7		I2S1_SDOUT	GP170	I2S1_SDOUT	DAP1_DOUT
H8		I2S1_SDIN	GP171	I2S1_SDIN	DAP1_DIN
G4	I2S2	I2S2_CLK	GP122	I2S2_CLK	DAP2_SCLK
E4		I2S2_FS	GP125	I2S2_FS	DAP2_FS
F5		I2S2_DOUT	GP123	I2S2_DOUT	DAP2_DOUT
F6		I2S2_DIN	GP124	I2S2_DIN	DAP2_DIN
C59	I2S4	I2S3_SCLK	GP206_DAP4_CLK	I2S4_SCLK	DAP4_SCLK
C60		I2S3_FS	GP209_DAP4_FS	I2S4_FS	DAP4_FS
K59		I2S3_DOUT	GP207_DAP4_DOUT	I2S4_DOUT	DAP4_DOUT
J59		I2S3_DIN	GP208_DAP4_DIN	I2S4_DIN	DAP4_DIN
B58	I2S6	GPIO21	GP202_DAP6_CLK	GPIO21	DAP6_SCLK
A58		GPIO20	GP205_DAP6_FS	GPIO20	DAP6_FS
A59		GPIO05	GP203_DAP6_DOUT	GPIO05	DAP6_DOUT
B59		GPIO04	GP204_DAP6_DIN	GPIO04	DAP6_DIN
H9	Audio clock	MCLK01	GP167	MCLK01	AUD_MCLK
L15	DMIC2	GPIO14 (DMIC2_CLK)	GP164_SPI5_CS0	GPIO14 (DMIC2_CLK)	DAP3_FS
G7		GPIO13 (DMIC2_DAT)	GP163_SPI5_MOSI	GPIO13 (DMIC2_DAT)	DAP3_DIN
C61	DMIC3/	GPIO09 (DMIC3_CLK)	GP26	GPIO09 (DMIC3_CLK)	CAN1_EN
B62	DMIC5	GPIO08 (DMIC3_DAT)	GP25	GPIO08 (DMIC3_DAT)	CAN1_STB
F9	DSPK0	GPIO16 (DSPK0_CLK)	GP162_SPI5_MISO	GPIO16 (DSPK0_CLK)	DAP5_DOUT
F10		GPIO15 (DSPK0_DAT)	GP161_SPI5_CLK	GPIO15 (DSPK0_DAT)	DAP5_SCLK

Table 8.   Additional Jetson AGX Orin Audio Interfaces

Pin #	Function	Jetson AGX Orin Signal Name	Orin SoC Signal Name
F10	I2S3_SCLK	GPIO15	GP161_SPI5_CLK
L15	I2S3_LRCK	GPIO14	GP164_SPI5_CS0
F9	I2S3_SDATA_OUT	GPIO16	GP162_SPI5_MISO
G7	I2S3_SDATA_IN	GPIO13	GP163_SPI5_MOSI
J55	I2S5_SCLK	GPIO32	GP58
A55	I2S5_LRCK	GPIO34	GP69
L52	I2S5_SDATA_OUT	MOD_SHUTDOWN	GP67
K57	I2S5_SDATA_IN	PWM01	GP68
L52	DMIC1_CLK	MOD_SHUTDOWN	GP67
J55	DMIC1_DAT	GPIO32	GP58
A55	DMIC4_CLK	GPIO34	GP69
K57	DMIC4_DAT	PWM01	GP68
A55	DSPK1_CLK	GPIO34	GP69
K57	DSPK1_DAT	PWM01	GP68

Note:

1. The functions in this table are shared with other functions. Only one function can be used in a design. Ensure no conflicts exist when choosing the functions for a design.

I2C

Jetson AGX Orin and Jetson AGX Xavier both support up to eight I2C interfaces. This includes the DP_AUX pins. One of which is shared with the single DP and HDMI interface on Jetson AGX Orin or the three shared with the three DP and HDMI interfaces on Jetson AGX Xavier.

Table 9.   Jetson AGX Orin and Jetson AGX Xavier I2C Interfaces

Pin #	Function	Jetson AGX Orin Signal Name	Orin SoC Signal Name	Jetson AGX Xavier Signal Name	Xavier SoC Signal
K5	I2C1	I2C1_CLK	GP126_I2C1_CLK	I2C1_CLK	GEN1_I2C_SCL
L8		I2C1_DAT	GP127_I2C1_DAT	I2C1_DAT	GEN1_I2C_SDA
J61	I2C2	I2C2_CLK	GP13_I2C2_CLK	I2C2_CLK	GEN2_I2C_SCL
K61		I2C2_DAT	GP14_I2C2_DAT	I2C2_DAT	GEN2_I2C_SDA
F53	I2C3	I2C3_CLK	GP54_I2C3_CLK	I2C3_CLK	CAM_I2C_SCL
E53		I2C3_DAT	GP55_I2C3_DAT	I2C3_DAT	CAM_I2C_SDA
J52	I2C4	DP1_AUX_CH_P	GP75_I2C4_CLK	DP1_AUX_CH_P	DP_AUX_CH1_P
J53		DP1_AUX_CH_N	GP76_I2C4_DAT	DP1_AUX_CH_N	DP_AUX_CH1_N
A53	I2C5	I2C5_CLK	GP81_I2C9_CLK	I2C5_CLK	DP_AUX_CH3_P

Pin #	Function	Jetson AGX Orin Signal Name	Orin SoC Signal Name	Jetson AGX Xavier Signal Name	Xavier SoC Signal
C53		I2C5_DAT	GP82_I2C9_DAT	I2C5_DAT	DP_AUX_CH3_N
G53	I2C6	DP2_AUX_CH_P	SF_DPAUX01_P	DP2_AUX_CH_P	DP_AUX_CH2_P
G54		DP2_AUX_CH_N	SF_DPAUX01_N	DP2_AUX_CH_N	DP_AUX_CH2_N
F52	I2C7	DP0_AUX_CH_P	GP78_I2C7_CLK	DP0_AUX_CH_P	DP_AUX_CH0_P
F51		DP0_AUX_CH_N	GP79_I2C7_DAT	DP0_AUX_CH_N	DP_AUX_CH0_N
D61	I2C8	I2C4_CLK	GP15_I2C8_CLK	I2C4_CLK	GEN8_I2C_SCL
E60		I2C4_DAT	GP16_I2C8_DAT	I2C4_DAT	GEN8_I2C_SDA

SPI

Jetson AGX Orin has four SPI interfaces while Jetson AGX Xavier has three.

Table 10.   Jetson AGX Orin and Jetson AGX Xavier SPI Interfaces

Pin #	Function	Jetson AGX Orin Signal Name	Orin SoC Signal Name	Jetson AGX Xavier Signal Name	Xavier SoC Signal
J57	SPI1	SPI1_CLK	GP47_SPI1_CLK	SPI1_CLK	SPI1_SCK
D55		SPI1_MOSI	GP49_SPI1_MOSI	SPI1_MOSI	SPI1_MOSI
A56		SPI1_MISO	GP48_SPI1_MISO	SPI1_MISO	SPI1_MISO
E55		SPI1_CS0_N	GP50_SPI1_CS0_N	SPI1_CS0_N	SPI1_CS0
B56		SPI1_CS1_N	GP51_SPI1_CS1_N	SPI1_CS1_N	SPI1_CS1
E61	SPI2	SPI2_CLK	GP06_SPI2_CLK	SPI2_CLK	SPI2_SCK
F60		SPI2_MOSI	GP08_SPI2_MOSI	SPI2_MOSI	SPI2_MOSI
D62		SPI2_MISO	GP07_SPI2_MISO	SPI2_MISO	SPI2_MISO
D60		SPI2_CS0_N	GP09_SPI2_CS_N	SPI2_CS0_N	SPI2_CS0
F55	SPI3	SPI3_CLK	GP36_SPI3_CLK	SPI3_CLK	SPI3_SCK
G56		SPI3_MOSI	GP38_SPI3_MOSI	SPI3_MOSI	SPI3_MOSI
D56		SPI3_MISO	GP37_SPI3_MISO	SPI3_MISO	SPI3_MISO
C57		SPI3_CS0_N	GP39_SPI3_CS0_N	SPI3_CS0_N	SPI3_CS0
E56		SPI3_CS1_N	GP40_SPI3_CS1_N	SPI3_CS1_N	SPI3_CS1

Table 11.   Additional Jetson AGX Orin SPI Interfaces

Pin #	Function	Jetson AGX Orin Signal Name	Orin SoC Signal Name
L56	SPI4_SCK	THERM_ALERT_M	GP108
J4	SPI4_OUT	GPIO01	GP110
L11	SPI4_DIN	SLEEP_REQ_N	GP109
L5	SPI4_CS0	UART4_TX	GP118_UART4_TXD_BOOT1_STRAP
F10	SPI5_SCK	GPIO15	GP161_SPI5_CLK
G7	SPI5_OUT	GPIO13	GP163_SPI5_MOSI
F9	SPI5_DIN	GPIO16	GP162_SPI5_MISO
L15	SPI5_CS0	GPIO14	GP164_SPI5_CS0

Note: The functions in this table are shared with other functions. Only one function can be used in a design. Ensure no conflicts exist when choosing the functions for a design.

UART

Jetson AGX Orin and Jetson AGX Xavier both support up to five UART interfaces.

Table 12.   Jetson AGX Orin and Jetson AGX Xavier UART Interfaces

Pin #	Function	Jetson AGX Orin Signal Name	Orin SoC Signal Name	Jetson AGX Xavier Signal Name	Xavier SoC Signal
K53	UA3 (UART1)	UART1_TX	GP70_UART1_TXD_BOOT2_STRAP	UART1_TX	UART1_TX
K54		UART1_RX	GP71_UART1_RXD	UART1_RX	UART1_RX
L51		UART1_RTS	GP72_UART1_RTS_N	UART1_RTS	UART1_RTS
H54		UART1_CTS	GP73_UART1_CTS_N	UART1_CTS	UART1_CTS
J58	UB3 (UART2)	UART5_TX	GP32_UART2_TXD	UART5_TX	UART5_TX
H58		UART5_RX	GP33_UART2_RXD	UART5_RX	UART5_RX
K58		UART5_RTS	GP34_UART2_RTS_N	UART5_RTS	UART5_RTS
H57		UART5_CTS	GP35_UART2_CTS_N	UART5_CTS	UART5_CTS
H62	UC3 (UART3)	UART3_TX_DEBUG	GP11_UART3_TXD	UART3_TX_DEBUG	UART3_TX
K60		UART3_RX_DEBUG	GP12_UART3_RXD	UART3_RX_DEBUG	UART3_RX
C58	UE3 (UART5)	UART2_TX	GP41_UART5_TXD_DDRCODE1	UART2_TX	UART2_TX
C56		UART2_RX	GP42_UART5_RXD	UART2_RX	UART2_RX
G58		UART2_RTS	GP43_UART5_RTS_N_DDRCODE0	UART2_RTS	UART2_RTS
A57		UART2_CTS	GP44_UART5_CTS_N	UART2_CTS	UART2_CTS

Pin #	Function	Jetson AGX Orin Signal Name	Orin SoC Signal Name	Jetson AGX Xavier Signal Name	Xavier SoC Signal
E61	UART7 (Jetson AGX Xavier only – See Note 2)	SPI2_CLK	GP06_SPI2_CLK	SPI2_CLK (UART7_TX)	SPI2_SCK
D62		SPI2_MISO	GP07_SPI2_MISO	SPI2_MISO (UART7_RX)	SPI2_MISO
F60		SPI2_MOSI	GP08_SPI2_MOSI	SPI2_MOSI (UART7_RTS)	SPI2_MOSI
D60		SPI2_CS0_N	GP09_SPI2_CS_N	SPI2_CS0_N (UART7_CTS)	SPI2_CS0

Notes:

1. The Jetson AGX Xavier UART4_RX pin cannot be used (must be reserved and pulled to GND through 10 kohm resistor). This eliminates UART4 on Jetson AGX Xavier.

2. Jetson AGX Orin does not have UART functionality available on these pins.

Table 13.   Additional Jetson AGX Orin UART Interfaces

Pin #	Function	Jetson AGX Orin Signal Name	Orin SoC Signal Name
L5	UART4 (Jetson AGX Orin only – See Note 1)	UART4_TX	GP118_UART4_TXD_BOOT1_STRAP
L48		UART4_RX	GP119_UART4_RXD
L4		UART4_RTS	GP120_UART4_RTS_N_BOOT0_STRAP
L49		UART4_CTS	GP121_UART4_CTS_N
G53	UF3_TXD (UART6_TX)	DP2_AUX_CH_P	SF_DPAUX01_P
G54	UF3_RXD (UART6_RX)	DP2_AUX_CH_N	SF_DPAUX01_N
F13	UH3_TXD (UART8_TX)	USB0_N	HS_USB0_P0_N (see note 3)
F12	UH3_RXD (UART8_RX)	USB0_P	HS_USB0_P0_P
C10	UH3_TXD (UART8_TX)	USB1_N	HS_USB1_P0_N (see note 3)
C11	UH3_RXD (UART8_RX)	USB1_P	HS_USB1_P0_P
SBSA Compliant UARTs (see Note 4)			
C58	UI3_TXD (UART9_TX)	UART2_TX	GP41_UART5_TXD_DDRCODE1
C56	UI3_RXD (UART9_RX)	UART2_RX	GP42_UART5_RXD
H62	UJ3_TXD (UART10_TX)	UART3_TX_DEBUG	GP11_UART3_TXD
K60	UJ3_RXD (UART10_RX)	UART3_RX_DEBUG	GP12_UART3_RXD

Note:

1. The Jetson AGX Xavier UART4_RX pin cannot be used (must be reserved and pulled to GND through 10kohm resistor). This eliminates UART4 on Jetson AGX Xavier.

2. Some functions are shared with other functions. Only one function can be used in a design. Ensure no conflicts exist when choosing the functions for a design.

3. The UART8 function can be brought out on either USB0 or USB1.

4. The UART[10:9] functions support SBSA compliance. These are pin multiplexed with UART3 and UART5 functions.

PWM

Jetson AGX Orin and Jetson AGX Xavier both support up to four PWM pins.

Table 14.   Jetson AGX Orin and Jetson AGX Xavier UART Interfaces

Pin #	Function	Jetson AGX Orin Signal Name	Orin SoC Signal Name	Jetson AGX Xavier Signal Name	Xavier SoC Signal
H52	PWM1	GPIO27	GP88_PWM1	GPIO27	SOC_GPIO54
K62	PWM3	FAN_PWM	GP31_PWM3	FAN_PWM	TOUCH_CLK
L50	PWM5	GPIO35	GP115	GPIO35	SOC_GPIO12
K57	PWM8	PWM01	GP68	PWM01	SOC_GPIO44

Debug

Jetson AGX Orin and Jetson AGX Xavier both support JTAG and a debug UART.

Connector Pin Difference Details

The following table lists the pins that have different functionality between Jetson AGX Orin and Jetson AGX Xavier. For some pins, the supported function is completely different. For others, some of the functionality is the same, but additional functionality is supported. These are highlighted in magenta and comments are provided.

Table 15.   Connector Pin Function Differences

Module Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson AGX Xavier Pin Name	Xavier SoC Pin Name	Comments
H51	GPIO26	GP86_XFI0_MDC	GPIO26	SOC_GPIO51	These Jetson AGX Orin pins can be GPIOs, but support the XFI MDIO functionality if the MGBE interfaces are used.
K49	GPIO25	GP85_XFI0_MDIO	GPIO25	SOC_GPIO50	
K56	GPIO19	GP89_XFI1_MDC	GPIO19	SOC_GPIO43	
C54	GPIO33	GP87_XFI1_MDIO	GPIO33	SOC_GPIO05	
D54	GPIO03	GP84_XFI2_MDC	GPIO03	SOC_GPIO52	
J51	GPIO24	GP83_XFI2_MDIO	GPIO24	DP_AUX_CH3_HPD	
L5	UART4_TX	GP118_UART4_TXD_BOOT1_STRAP	UART4_TX	UART4_TX	Due to the issue with the UART4_RX pin on Jetson AGX Xavier, the other UART4 pins can only be used as GPIOs. Jetson AGX Orin supports UART functionality.
L48	UART4_RX	GP119_UART4_RXD	RSVD (UART4_RX)	–	
L4	UART4_RTS	GP120_UART4_RTS_N_BOOT0_STRAP	UART4_RTS	UART4_RTS	
L49	UART4_CTS	GP121_UART4_CTS_N	UART4_CTS	UART4_CTS	
D37	PMIC_BBATT	– (GP200)	RSVD	–	GP200 connected to this pin on early pre-production modules.
K52	DP0_HPD	GP80_XFI3_MDC	DP0_HPD	DP_AUX_CH0_HPD	
K51	DP1_HPD	GP77_XFI3_MDIO	DP1_HPD	DP_AUX_CH1_HPD	
J11	PEX_C2_CLKREQ_N	GP189_PCIE8_CLKREQ_N	RSVD	–	
L19	PEX_C6_CLKREQ_N	GP212_PCIE6_CLKREQ_N	RSVD	–	
B37	PEX_C7_CLKREQ_N	GP177_PCIE1_CLKREQ_N	RSVD	–	
A38	PEX_C8_CLKREQ_N	GP181_PCIE3_CLKREQ_N	RSVD	–	
K10	PEX_C2_RST_N	GP190_PCIE8_RST_N	RSVD	–	
L18	PEX_C6_RST_N	GP213_PCIE6_RST_N	RSVD	–	
B36	PEX_C7_RST_N	GP178_PCIE1_RST_N	RSVD	–	
A39	RSVD	–	RSVD	–	
B48	RSVD	–	HDMI_DP1_TX1_N	HDMI_DP1_TXDN1	
B49	RSVD	–	HDMI_DP1_TX1_P	HDMI_DP1_TXDP1	

Module Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson AGX Xavier Pin Name	Xavier SoC Pin Name	Comments
E51	RSVD	–	HDMI_DP1_TX3_N	HDMI_DP1_TXDN3	
E50	RSVD	–	HDMI_DP1_TX3_P	HDMI_DP1_TXDP3	
L59	SAFETY_PROCESSOR_ GPIO	SF_RST_N	RSVD	–	
L42	VM_EN0_N	–	RSVD	–	
L41	VM_EN1_N	–	RSVD	–	
B10	PWR_IRQ_N	SF_PWR_INT_N	RSVD	–	
J62	TEMP_SHDN_EN	–	GND	–	
B55	GPIO30	GP02	GPIO30	SOC_GPIO20	
H60	GPIO31	GP186	GPIO31	SAFE_STATE	
C38	UPHY_REFCLK4_N	HS_UPHY1_REFCLK1_N	RSVD	–	
C39	UPHY_REFCLK4_P	HS_UPHY1_REFCLK1_P	RSVD	–	
E18	PEX_CLK2_N	SF_PCIE8_CLK_N	RSVD	–	
E19	PEX_CLK2_P	SF_PCIE8_CLK_P	RSVD	–	
F33	UPHY_REFCLK3_N	SF_PCIE6_CLK_N	RSVD	–	
F32	UPHY_REFCLK3_P	SF_PCIE6_CLK_P	RSVD	–	
A48	GPIO37	SF_PCIE3_CLK_N	HDMI_DP1_TX0_N	HDMI_DP1_TXDN0	
A47	GPIO38	SF_PCIE3_CLK_P	HDMI_DP1_TX0_P	HDMI_DP1_TXDP0	
D48	PEX_CLK6_N	SF_PCIE1_CLK_N	HDMI_DP1_TX2_N	HDMI_DP1_TXDN2	
D49	PEX_CLK6_P	SF_PCIE1_CLK_P	HDMI_DP1_TX2_P	HDMI_DP1_TXDP2	
C35	UPHY_RX20_N	HS_UPHY0_L2_RX_N	RSVD	–	
C34	UPHY_RX20_P	HS_UPHY0_L2_RX_P	RSVD	–	
B32	UPHY_RX21_N	HS_UPHY0_L3_RX_N	RSVD	–	
B33	UPHY_RX21_P	HS_UPHY0_L3_RX_P	RSVD	–	
D32	UPHY_RX22_N	HS_UPHY0_L4_RX_N	RSVD	–	
D33	UPHY_RX22_P	HS_UPHY0_L4_RX_P	RSVD	–	
A35	UPHY_RX23_N	HS_UPHY0_L5_RX_N	RSVD	–	
A34	UPHY_RX23_P	HS_UPHY0_L5_RX_P	RSVD	–	
K33	UPHY_TX20_N	HS_UPHY0_L2_TX_N	RSVD	–	
K32	UPHY_TX20_P	HS_UPHY0_L2_TX_P	RSVD	–	
G34	UPHY_TX21_N	HS_UPHY0_L3_TX_N	RSVD	–	
G35	UPHY_TX21_P	HS_UPHY0_L3_TX_P	RSVD	–	
J34	UPHY_TX22_N	HS_UPHY0_L4_TX_N	RSVD	–	
J35	UPHY_TX22_P	HS_UPHY0_L4_TX_P	RSVD	–	
H33	UPHY_TX23_N	HS_UPHY0_L5_TX_N	RSVD	–	
H32	UPHY_TX23_P	HS_UPHY0_L5_TX_P	RSVD	–	
G50	RFU3	–	HDMI_DP0_TX1_N	HDMI_DP0_TXDN1	
G51	RFU4	–	HDMI_DP0_TX1_P	HDMI_DP0_TXDP1	
H48	RFU1	–	HDMI_DP0_TX0_N	HDMI_DP0_TXDN0	
H49	RFU2	–	HDMI_DP0_TX0_P	HDMI_DP0_TXDP0	
J47	RFU6	–	HDMI_DP0_TX2_P	HDMI_DP0_TXDP2	
J48	RFU5	–	HDMI_DP0_TX2_N	HDMI_DP0_TXDN2	
K46	RFU8	–	HDMI_DP0_TX3_P	HDMI_DP0_TXDP3	
K47	RFU7	–	HDMI_DP0_TX3_N	HDMI_DP0_TXDN3	