

Analog Front End Design of Contactless Smart Card for Standard ISO/IEC14443-A

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Abstract—This paper describes a set of analog front end design for contactless smart cards which complies with ISO 14443-2 Type A. It has been implemented in Globalfoundries 130nm (GF130) CMOS process. The design and implementation was manufactured by MOSIS through the Educational Program. The analog front end operates at 13.56MHz with data rate 106kbps. This paper will show the simulation using Synopsys HSPICE and the corresponding test for the CMOS process GF130.

Index Terms—CMOS technology Analog integrated circuits, Rectifiers, Transceivers, Amplitude shift keying, Modulation, Demodulation, Regulators, Clocks, Power conditioning, RFID tags, Smart cards

I. INTRODUCTION

In recent years Radio Frequency Identification systems (RFID) [1] have become very popular in many service industries, purchasing and distribution logistics, industry, manufacturing companies and material flow systems. In contrast with earlier techniques like barcodes, RFID is more favored because of its longer operation distance, higher precision, faster processing speed and storage capabilities. With it we can identify objects and store some data in a single silicon chip. This paper demonstrates the RF circuits design proposal of contactless IC card which comply with ISO/IEC14443-2 [2] and validates the topologies with measurements. This design satisfies the performance request with the neat circuits, and has been implemented with 130nm CMOS technology successfully.

II. ISO/IEC14443-2

A. Types of RF interface

ISO/IEC 14443-2 describes two types of RF interface about contactless IC cards which operate at 13.56 MHz: Type A and Type B.

In Type A, the signal from PCD (Proximity Coupling Device) to PICC (Proximity Integrated Circuit Card) is modulated in ASK (Amplitude Shift Keying) with modulation index 100%. When receiving the data from PCD, the PICC can't process the data because the absence of the clock source.

In Type B, the signal from PCD to PICC is defined to be modulated with BPSK by carrier, and the signal from PCD to PICC is modulated in ASK with modulation index 10%, which make it possible for PICC to work continuously. Therefore, the solution given by Type B could reach higher data rate, but the design of the circuits would be more complicated. The ASK index 10% is harder to detect than index 100%.

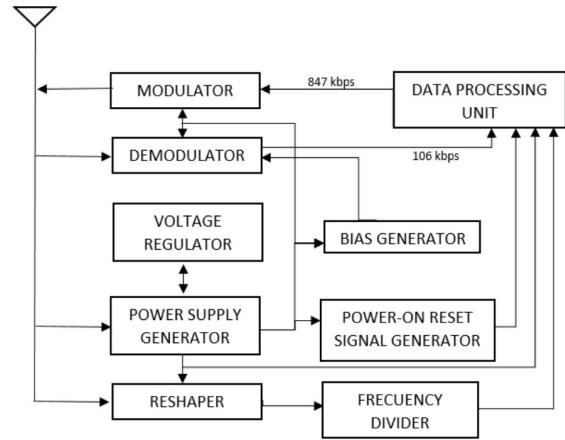


Fig. 1. Contactless IC card modules

This paper describes the circuit design for the Type A.

B. Analog Front-End Modules

The contactless IC card contains two main sections [3]: RF section and Data Processing Unit (DPU). The modules in RF section are demonstrated in Fig.1, which comprises Power Supply Generator (PSG), Clock Generator (CG), Voltage Regulator (VR), Power On Reset (POR), Modulator and Demodulator.

When the PICC enters to the RF field, the signal coupled by antenna can generate power supply through PSG. The PSG consists of a rectifier and a Shunt Regulator. The VR regulates the power of PSG and gives a constant voltage to the rest of the modules. As soon as the power supply reaches the operating condition, the POR gives a low level signal to reset all the Flip-Flops of the DPU. The modulator and demodulator are modules that let the PCD communicate with PICC.

III. IC CIRCUIT DESIGN

The previous section demonstrates the RF modules that involve the communication between PCD and PICC. This section will describe in detail each module of the analog front-end for ISO/IEC 14443A (see Fig. 2).

A. Power Supply Generator (PSG)

The Power Supply Generator splits into two parts: signal rectification and power limitation.

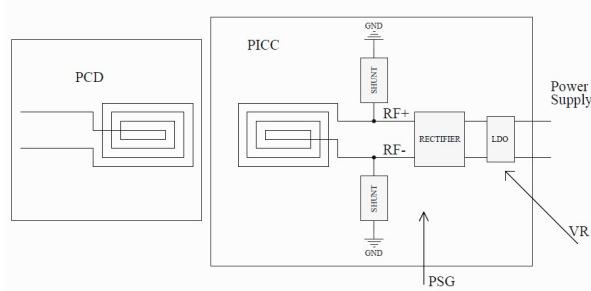


Fig. 2. PICC Analog Front-end

The first part rectifies the RF field signal to get power supply for the chip, a full NMOS bridge rectifier [4][5] was implemented in this design. And the second part consists of a Shunt resistor. The Shunt resistor is capable to limit the voltage of the antenna and protects the whole chip. ISO/IEC14443-2 requires the PICC to work when magnetic intensity between 1.5-7.5A/m rms. Therefore the PICC must work in these extreme conditions.

The simplified schematic of signal rectification is shown in Fig. 3 and power limitation (Shunt resistor) is shown in Fig. 4.

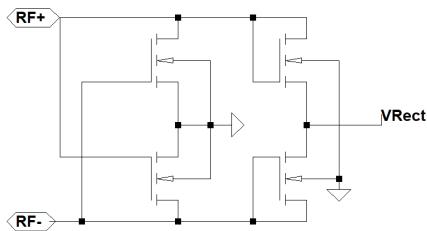


Fig. 3. NMOS Bridge Rectifier

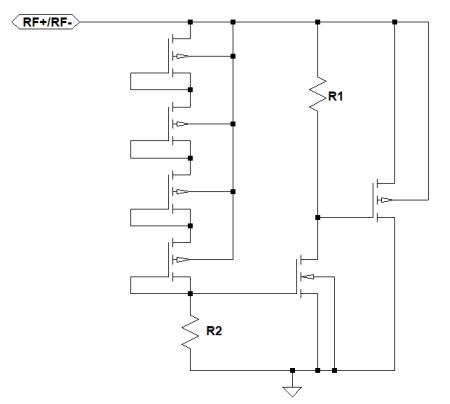


Fig. 4. Shunt Resistor

B. Clock Generator (CG)

The Clock Generator recovers the clock from the antenna and is used by the DPU. This module generates a clock source

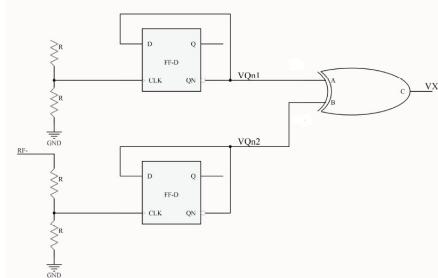


Fig. 5. Clock Generator schematic

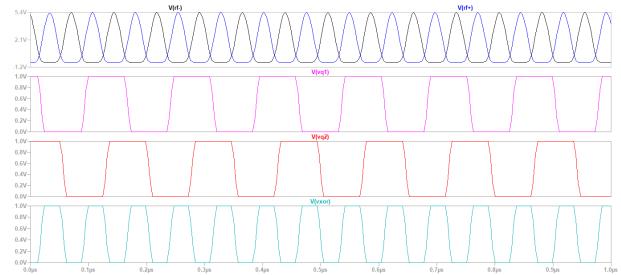


Fig. 6. Clock recovery simulation

of 13.56 MHz. Basically it consists of two FF/D (clock divider by 2) and a XOR logic gate.

The difference of phase between RF+ and RF- are 180 degrees, it is easy to take advantage of this property to recompose the clock. The simplified schematic is shown in Fig. 5 and the simulation in the Fig. 6.

A frequency divider by 4 is placed at the output of the clock generator, reducing the work frequency also reduces the power consumed. On the other hand, Carrier-Frequency/4 (3.39MHz) is used for the DPU, because the FDT (Frame Delay Time) defined in ISO/IEC14443-3 for all commands are divisor of this frequency.

C. Voltage Regulator (VR)

The Voltage Regulator [6] regulates the voltage supplied from PSG and provides a constant DC voltage at the output of this module. The VR is known as the series pass regulator, as shown in Fig. 7. It consists of 3 major parts. Operational amplifier (OP-AMP) is used as error amplifier. A series pass transistor forms a current amplifier. R1 and R2 are used as resistive voltage divider (Equation 1). The reference source Vref, in this case, is a beta multiplier [7].

$$VDD = Vref * (1 + R1/R2) \quad (1)$$

D. Modulator

The modulator [8] transmits the signal from PICC to PCD. There are two different types of load modulation: resistive and capacitive modulation. Both types create a subcarrier next to 13.56MHz. The NMOS are switched on and off in time with the encoded data. This will vary the load (resistive) or resonance frequency (capacitive) of the transponder. Resistive

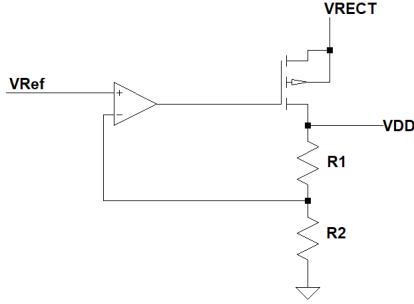


Fig. 7. Voltage Regulator schematic

modulation was adopted in this design for its simplicity. The schematic is shown in Fig. 8.

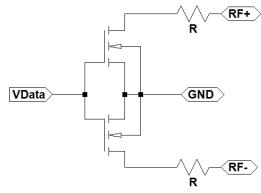


Fig. 8. Modulator schematic

E. Demodulator

The demodulator recovers the digital transmitted from PCD. An Envelope Extractor (EE) [9] is needed to extract the data. The digital signal is recovered by connecting the output of the EE with the input of the buffer. The circuit is shown in Fig. 9.

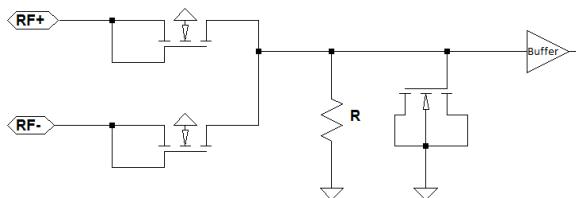


Fig. 9. Demodulator schematic

F. Power On Reset (POR)

The Power On Reset module is used to reset the digital machine and put it into idle state. It consists of a RC low pass network. When the chip enters the RF field, the VR turns on and powers all the modules. The POR module holds the voltage of the VR and delays it. This signal applies to the reset pin of the Flip-Flops in the digital machine. The schematic is demonstrated in Fig. 10.

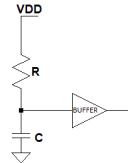


Fig. 10. POR schematic

IV. IC CIRCUIT FLOORPLANING

The corresponding layout is shown in Fig. 11, it was designed for Global Foundries 130nm. The analog Front End covers 0.3mm x 0.2mm (Fig. 11.a).

The design was shipped by MOSIS [10], it is shown in Fig. 11.b. In the next section will demonstrate the measurement of this integrated circuit and make conclusions about the results.

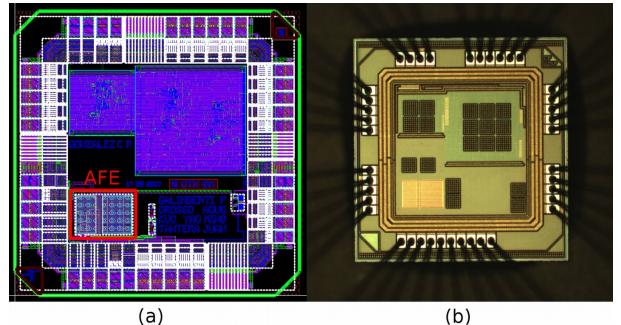


Fig. 11. (a) GF130 Layout, (b) GF130 Chip

V. MEASUREMENT & VALIDATION

In order to verify and validate the design, each module is tested and compared with simulation results. The corresponding tests verifies the feasibility of the design.

The measurement of the clock generator and a phase of the RF field (RF+) is shown in the Fig. 12.a. The wave demonstrates that the CG works well and can divide the clock 13.56MHz/4. The ripple of the clock is due to the noise of external power source which the ring pad is connected.

Fig. 12.b shows the comparison between RF+ with the output of the POR module. It can be seen the delay of the POR in relation to the input signal. This delay allows the DPU changing to the idle state.

Finally, Fig. 12.c shows the signal recovery transmitted from PCD. It demonstrates that the clock is interrupted, when a frame arrives.

VI. SUMMARY AND CONCLUSIONS

An analog front-end circuit for ISO/IEC14443A compatible RFID transponder IC was designed and implemented by using the Global Foundries 130nm (eight-metal/mim-capacitor) CMOS process. The measurement demonstrated that the transponder IC works properly (converts RF power to DC voltage, extracts the clock and data, and correctly sends

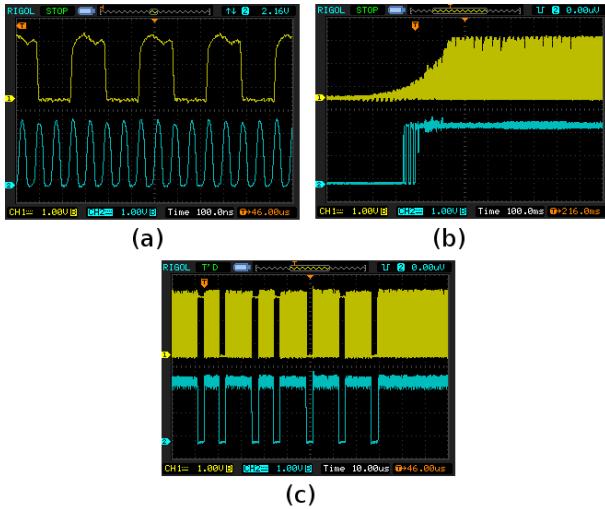


Fig. 12. (a) Clk/4 vs RF+, (b) RF+ vs POR, (c) Clk/4 vs Demodulator

data back). Using GF130 could reduce drastically the area in comparison with older technologies. This is a huge improvement compared with the existing products.

VII. ACKNOWLEDGEMENTS

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