

Analog Front-End Design of Contactless RFID Smart Card ISO/IEC14443A Standard - Compliant

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Abstract—This paper describes a set of analog front end design for contactless RFID smart cards that complies with ISO 14443-2 Type A Standard. It has been implemented using Global Foundries 130nm technology (GF130). The IC designed and implemented, presented in this paper, was then manufactured by MOSIS through the Educational Program. The analog front-end operates at 13.56MHz with a 106kbps data rate. This paper will show the simulation using Synopsys HSPICE and the corresponding test for the CMOS process GF130.

Index Terms—RFID tags, Smart cards, Rectifiers, Transceivers, Amplitude shift keying, Modulation, Demodulation, Regulators, Power conditioning

I. INTRODUCTION

In recent years, Radio Frequency Identification systems (RFID) [1] have become very popular in many service industries, purchasing and distribution logistics, industry, manufacturing companies and material flow systems. In contrast to earlier techniques like barcodes, RFID is more favored because of its longer operation distance, higher precision, faster processing speed and storage capabilities. RFID makes it possible to identify objects and store data in a single silicon chip. This paper studies the RF circuits design proposal of contactless IC card meeting ISO/IEC14443-2 [2] standard and validates topologies testing the IC. This design meets the performance request with the designed circuits, and has been successfully implemented with 130nm CMOS technology.

II. ISO/IEC14443-2

A. Types of RF interface

ISO/IEC 14443-2 describes two types of RF interface of contactless IC cards which operate at 13.56 MHz: Type A and Type B.

In Type A, the signal from the PCD (Proximity Coupling Device) to the PICC (Proximity Integrated Circuit Card) is modulated in ASK (Amplitude Shift Keying) with a modulation index of 100%. When receiving data from PCD, the PICC can not process the data because it lacks a clock source.

In Type B, the signal from PICC to PCD is defined to be modulated with BPSK by carrier, and the signal from PCD to PICC is modulated in ASK with a modulation index of 10%, making it possible for the PICC to work continuously. Therefore, even though Type B implementation would be able

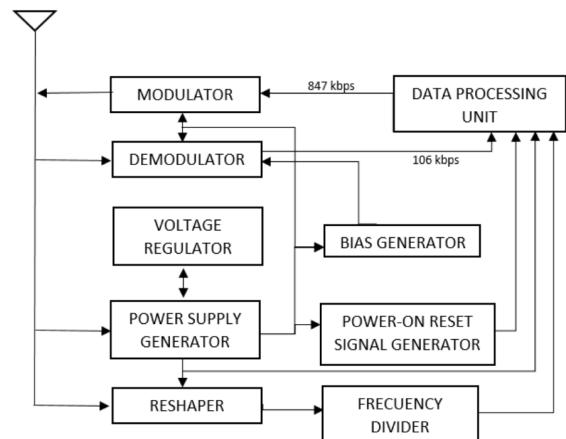


Fig. 1. Contactless IC card modules

to reach a higher data rate, its circuit design would be more complicated. The 10% ASK index is harder to detect than a 100% index.

This paper describes the circuit design for the Type A.

B. Analog Front-End Modules

The contactless IC card contains two main sections [3]: RF section and Data Processing Unit (DPU). The RF section is shown in Fig.1, and includes a Power Supply Generator (PSG), a Clock Generator (CG), a Voltage Regulator (VR), a Power On Reset (POR), a Modulator and a Demodulator.

When the PICC enters an RF field, the antenna couples the signal and powers the circuit through the PSG module. The PSG circuit contains a rectifier and a Shunt Regulator. The VR regulates the PSG power and supplies a constant voltage to the rest of the modules. As soon as power supply reaches the operating condition, the POR gives a low level signal to reset all the Flip-Flops of the DPU. Modulator and demodulator are modules that let the PCD communicate with the PICC.

III. IC CIRCUIT DESIGN

The previous section introduced the RF modules involved in the communication between the PCD and the PICC. This section will describe in detail each module of the analog front-end for ISO/IEC 14443A (see Fig. 2).

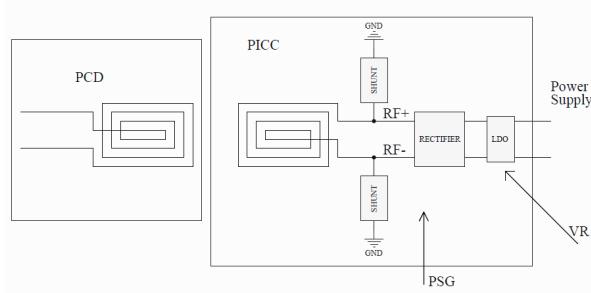


Fig. 2. PICC Analog Front-end

A. Power Supply Generator (PSG)

The Power Supply Generator is divided into two parts: signal rectification and power limitation.

The first part rectifies the RF field signal and powers the chip. A full NMOS bridge rectifier [4][5] was implemented in this design. The second part is a Shunt resistor that limits the voltage of the antenna and protects the whole chip. ISO/IEC14443-2 requires the PICC to work when magnetic intensity is between 1.5-7.5A/m rms. Therefore the PICC must be able to work under these extreme conditions.

The simplified schematic of signal rectification is shown in Fig. 3 and power limitation (Shunt resistor) is shown in Fig. 4.

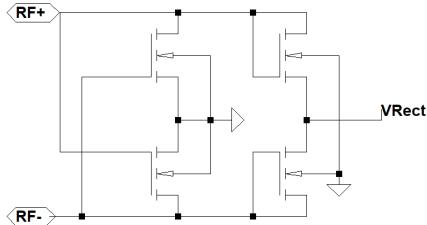


Fig. 3. NMOS Bridge Rectifier

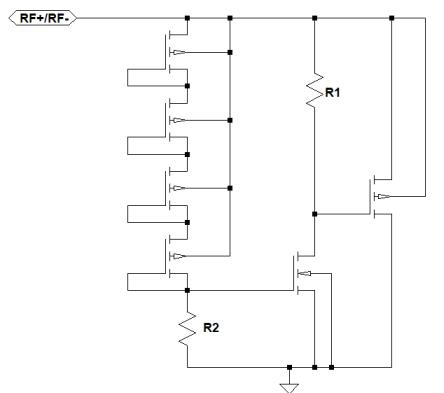


Fig. 4. Shunt Resistor

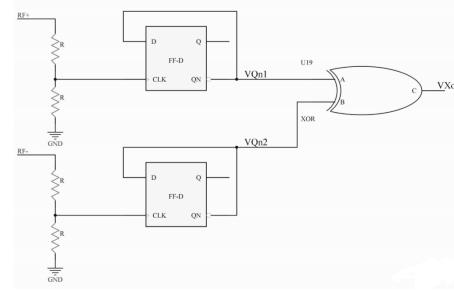


Fig. 5. Clock Generator schematic

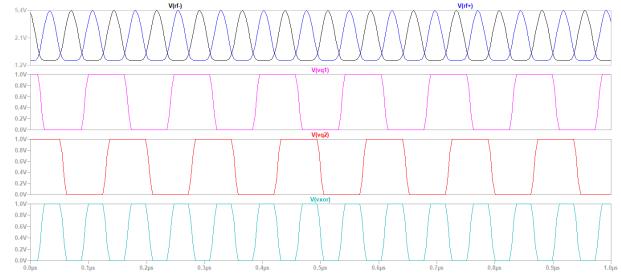


Fig. 6. Clock recovery simulation

B. Clock Generator (CG)

The Clock Generator gets the clock from the antenna and it is then used by the DPU. This module generates a 13.56MHz clock source. It consists of two D-Type Flip-Flops (Divide-by-2 clock signal) and an XOR logic gate.

The phase difference between RF+ and RF- is 180 degrees, making it quite easy to recover the clock. The simplified schematic is shown in Fig. 5 and the simulation in Fig. 6.

A frequency divider by 4 is placed at the output of the clock generator. Reducing the work frequency also reduces the power consumed. On the other hand, a Carrier-Frequency/4 (3.39MHz) is used for the DPU, because the FDT (Frame Delay Time) defined in ISO/IEC14443-3 for all commands is a divisor of this frequency.

C. Voltage Regulator (VR)

The Voltage Regulator [6] regulates the voltage supplied from PSG and provides a constant DC voltage at the output of this module. The VR is known as the series pass regulator, as shown in Fig. 7. It consists of three major parts. An operational amplifier (OP-AMP) is used as error amplifier. A series pass transistor is used as a current amplifier. R1 and R2 are used as a resistive voltage divider (Equation 1). The reference voltage source Vref, in this case, is a beta multiplier [7].

$$VDD = Vref * (1 + R1/R2) \quad (1)$$

D. Modulator

The modulator [8] carries the signal from the PICC to the PCD module. There are two different types of load modulation: resistive and capacitive modulation. Both types

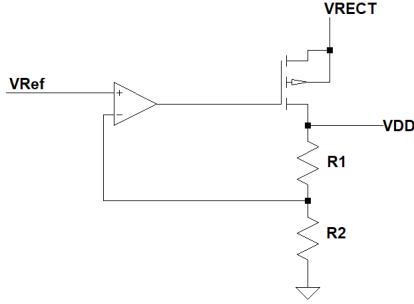


Fig. 7. Voltage Regulator schematic

create a subcarrier next to 13.56MHz. The NMOS transistors are switched on and off in time with the encoded data. This varies the load (resistive) or resonance frequency (capacitive) of the transponder. Resistive modulation was adopted in this design for its simplicity. The schematic is shown in Fig. 8.

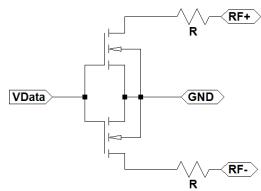


Fig. 8. Modulator schematic

E. Demodulator

The demodulator recovers the digital frame transmitted from the PCD module. An Envelope Extractor (EE) circuit [9] is needed to extract the data. The digital signal is recovered by connecting the output of the EE with the input of the buffer. The circuit is shown in Fig. 9.

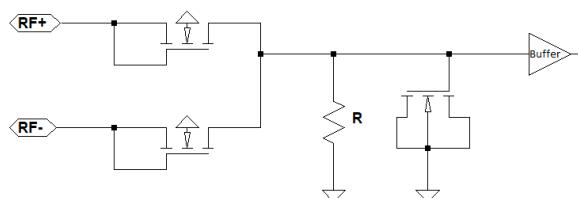


Fig. 9. Demodulator schematic

F. Power On Reset (POR)

The Power On Reset module is used to reset the digital machine and put it into an idle state. It consists of a RC low pass network. When the chip enters the RF field, the VR turns on and powers all modules. The POR module holds the voltage of the VR and delays it. This signal is applied to the reset pin of the Flip-Flops in the digital machine. The schematic is shown in Fig. 10.

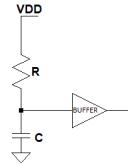


Fig. 10. POR schematic

IV. IC CIRCUIT FLOORPLANING

The corresponding layout is shown in Fig. 11. It was designed for Global Foundries 130nm CMOS process. The analog front-end covers 0.3mm x 0.2mm (Fig. 11.a).

The GF130 design, explained in this paper, was manufactured by MOSIS [10] and it is shown in Fig. 11.b. The next section will explain the measurements and tests performed on this integrated circuit and the conclusions made about the results.

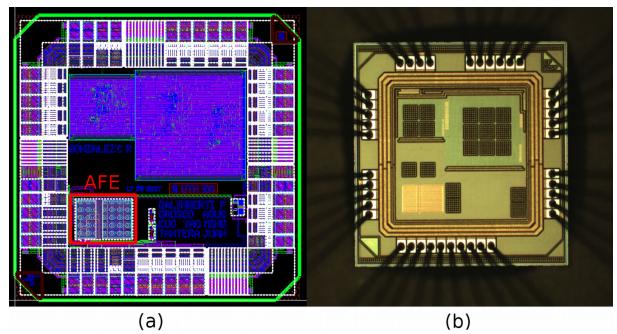


Fig. 11. (a) GF130 Layout, (b) GF130 Chip

V. MEASUREMENT & VALIDATION

In order to verify and validate the design, each module is tested and compared with simulation results. The corresponding tests verify the feasibility of the design.

Measurements of the clock generator and one phase of the RF field (RF+) are shown in the Fig. 12.a. The waveform demonstrates that the CG works as expected and in fact divides the clock frequency (13.56MHz/4). The clock signal ripple is due to the noise of the external power source to which the ring pad is connected.

Fig. 12.b shows the comparison between RF+ with the output of the POR module, where the delay of the POR in relation to the input signal. This delay allows the DPU to enter into idle state.

Finally, Fig. 12.c shows the signal recovery transmitted from the PCD. It demonstrates that the clock is interrupted whenever a frame arrives.

VI. SUMMARY AND CONCLUSIONS

An analog front-end circuit ISO/IEC14443A compliant RFID transponder IC was designed and implemented using Global Foundries 130nm (eight-metal/mim-capacitor) CMOS

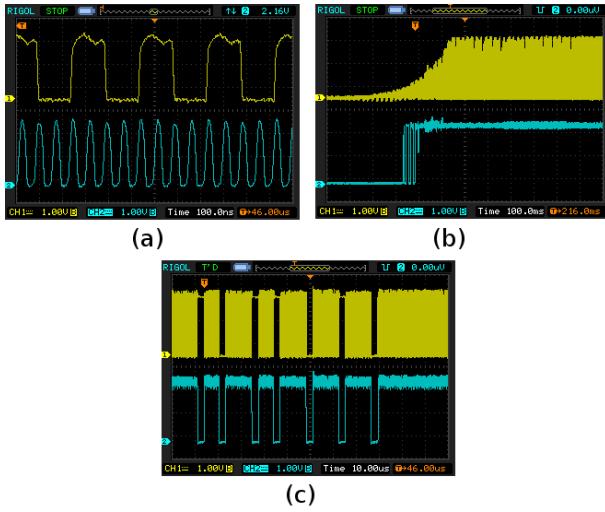


Fig. 12. (a) Clk/4 vs RF+, (b) RF+ vs POR, (c) Clk/4 vs Demodulator

process. The measurements taken demonstrated that the IC transponder works properly and as expected: converts RF power to DC voltage, extracts the clock and data and correctly sends data back. Using GF130 drastically reduced the area in comparison with older technologies, what is a significant improvement.

VII. ACKNOWLEDGEMENTS

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