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EGR 24L Introduction of Circuit Analysis Laboratory

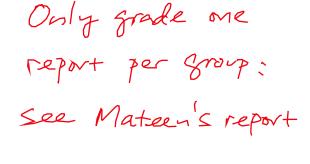
Professor Yu Zheng

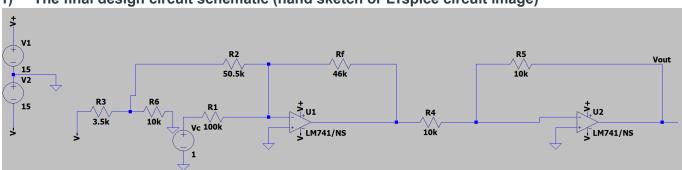
Dec 13, 2023

Group#1

Project#2

1) The final design circuit schematic (hand sketch or LTspice circuit image)





We ended up using two Op-amps, to create a summing amplifier

2) A short description of the system, explaining the various functional blocks of your system

This is the final schematic for Project 2. We went through trial and error trying to find out how to make a proper summing amplifier for this system to work. We needed to perform a linear equation using an opamp and through this setup: a summing opamp and an inverting opamp. We used this design because it clearly shows where everything is and doesn't overwhelm/confuse the group. Our target was to solve y=0.46x-9.36. A gain of 0.46 and an offset of -9.36. This system takes resisters ranging from different values and utilizes two opamps to solve the equation.

3) Test plan: a brief description of your test plan

After we calculated and determined all resistor values, we used simulator LTspice to check the Vout whether the Vout showed a valid slope that matched the requirement. This part took us two sessions to complete, and a lot of time and effort was spent trying to find the right combination of resistors to make our linear equation valid with the gain and offset.

After we obtained all resistor values and also got approved to build the circuit we also ran into an issue, the total value of of gain was off than what we expected due to all circuit components also having inner resistances. So we have to use a resistance box to adjust some of the resistor values.

4) Results

A (preassigned value) = $\underline{0.46}$; B (preassigned value) = $\underline{-9.36}$

Input voltage limits (predetermined values) are <u>__15V and -15 V</u> Measured results:

Output voltage	-15V
lower limit (V)	
Output voltage	15V
upper limit (V)	
VTC slope (V/V)	0.459989
VTC intercept	-9.36
(V)	
)-VTC plot:	
	ZV Nysouth
	3V-
	AV-
	.5V-
	-5V-
	.nv-
	.8V-
	5V-1 -10V-
	Currer 1 V(vout)
	Horz 102157259 Vert 9.1506458V Cureo 2 V(voxt)
	Horz: _10.114633mV Vet: _9.6352135V DEF (Lune2-Cursor)
	Stope 0.4599899
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VTC data table

Input voltage	Output voltage
1	-8.9
1.5	-8.66
2	-8.43
2.5	-8.21
3	-7.99
3.5	-7.75
4	-7.51
4.5	-7.3
5	-7.05
5.5	-6.82

5) Conclusions and lessons learned

In this project, we learned how to design the summing amplifier op-amp from specification with the least amount of LM471 Op-amp as possible. We also learned that a summing amplifier is a circuit that combines multiple input signals with different weights and produces a single output. We also learned how to test, debug, and adjust resistor values until we found the proper resistors that give out a proper gain and slope. The most take takeaway from this is we learned how to use a voltage divider to solve some problem that occurs in our circuit design. It was not easy to find the flaw in the design we found it last minute. However, with the help of the professor and group members, we were able to obtain a better design which helped us construct the circuit even more easily.