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EGR 24L Introduction of Circuit Analysis Laboratory

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Lab S2: Special Topic of Electronics- CMOS Logic Gates

Introduction:

In this second special lab professor introduced us to CMOS Logic gate are made of IGFET(MOSFET) transistors rather than bipolar junction transistors. CMOS gate inputs can be highly sensitive to static electricity. They can be damaged by high voltages, and they may assume any logic level if left floating. We continue our journey from previous special Lab CMOS using NMOS and PMOS to construct the circuit and use them of operate as inverter. Then, we move on to use quad NAND to construct the rest of circuits which required on spec sheet. The most significant purpose of doing CMOS Logic Gates lab is to explore and learn the relationship between discrete math (the law of logic) and logic of circuit. We apply De Morgan's laws and logic of truth table into a circuit. We explored many logic gate functions such as NAND, NOT, AND, OR and NOR gates. We verify our circuit performance by using truth table, if the condition on truth table is match to the circuit perform, it is mean that our circuit is constructed correctly. My teammate and I had learned how to convert quad NAND CD4001BM into multiple gates. It took us sometimes to figure out how it works.

In this lab, we delved into the intricacies of complexity logics that transcend the applicability of conventional algebra. Our exploration led us to uncover the underlying logic governing the operation of circuits, where inverters act as gatekeepers, toggling between binary signals of 0 and 1. This journey also unveiled the nuanced distinctions in the conditions governing various logic gates. Furthermore, we gained a comprehensive understanding of the versatile methods for constructing circuits utilizing quad NAND CMOS technology. Consequently, this laboratory experience holds immense significance as it offers a profound glimpse into the core of semiconductor technology and the inner workings of cutting-edge processor technology.

Procedure:

1) We first deep dive to explored NAND gate logic by using CMOS (NMOS and PMOS) act as inverter constructed the circuit. We know that condition of NAND gate is uniquely only when input a =1, and b=1 the output will be 0, True and True is equal False. The rest of output is 0. After we successfully constructed NAND gate with CMOS (NMOS and PMOS), we were move on to do the same thing but this time without NMOS and PMOS, we achieve by using Quad Nand.

2) We move on to use Quad Nand to construct the AND logic by applied the logic of AND gate in the truth table. We be able to achieve the proper AND circuit by used two inverter Quad Nand to achieve this. The condition of AND gate is uniquely only when input a =1, b=1, output will be 1. True and True is equal True.

3) Next, we move on to use Quad Nand to construct the OR logic by applied the logic of OR gate in the truth table. We able to achieve the proper OR circuit by applied the condition of or gate which is uniquely only when input a =0, b=0, output will be 0. False and False is equal False.

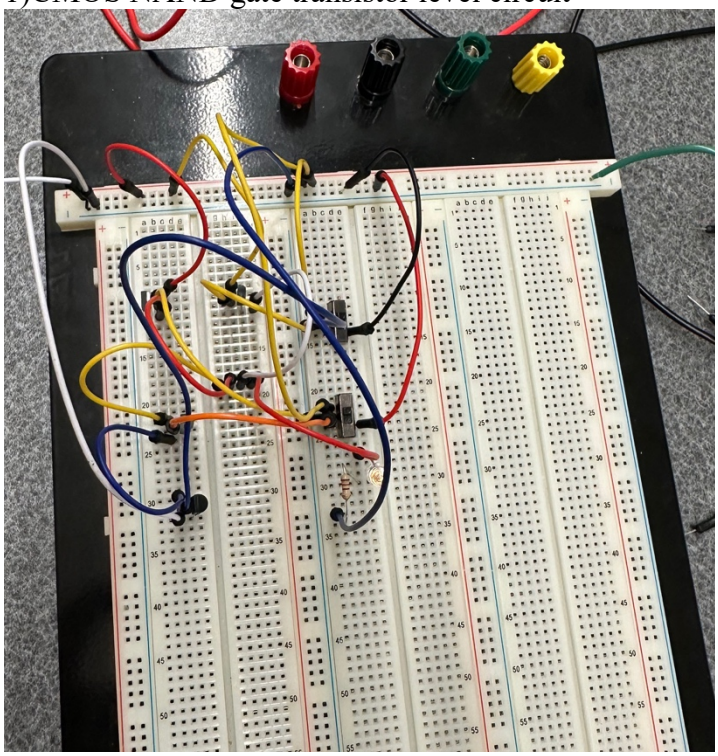
4) Last task, we move on to use Quad Nand to construct the NOR logic by applied the logic of NOR gate in the truth table. We be able to achieve the proper NOR circuit by using idea of both universal gate NAND and NOR, the condition of NOR gate which is uniquely only when input a =0, b=0, output will be 1. False and False is equal True.

Conclusion:

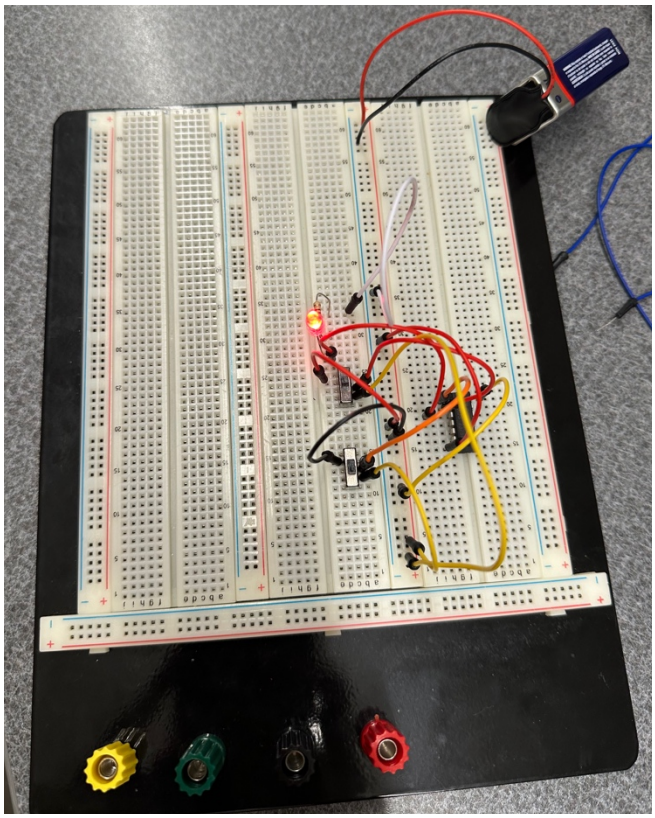
In conclusion, in the second special lab we were exploring another core fundamental knowledge of circuit which is logic gate. We get to learn how the Quad NAND work and to apply the truth table conditions to verify how logic gates work correctly. Moreover, we also understand NAND and NOR gates are universal gates because we can achieve anything by inverting these two gates. This journey was a fusion of theoretical logic from discrete mathematics and real-world circuitry, bridging the gap between abstract concepts and tangible applications. Recognizing the ubiquity of this logic in every circuit that surrounds us, we grasped the profound significance of this knowledge. In essence, Special Lab 2 emerged as a pivotal milestone in our circuit analysis journey, illuminating the intricate logic that pulses beneath the surface of every electronic marvel.

Appendixes:

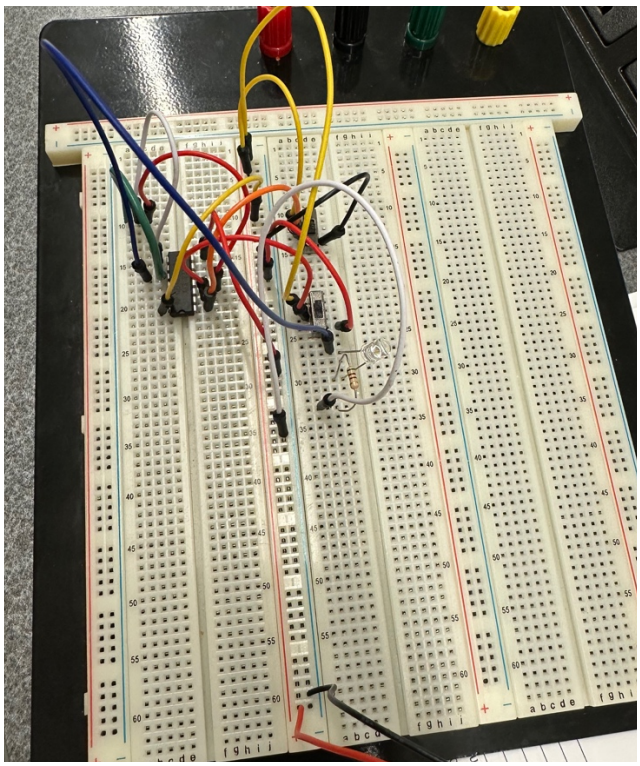
1)CMOS NAND gate transistor level circuit



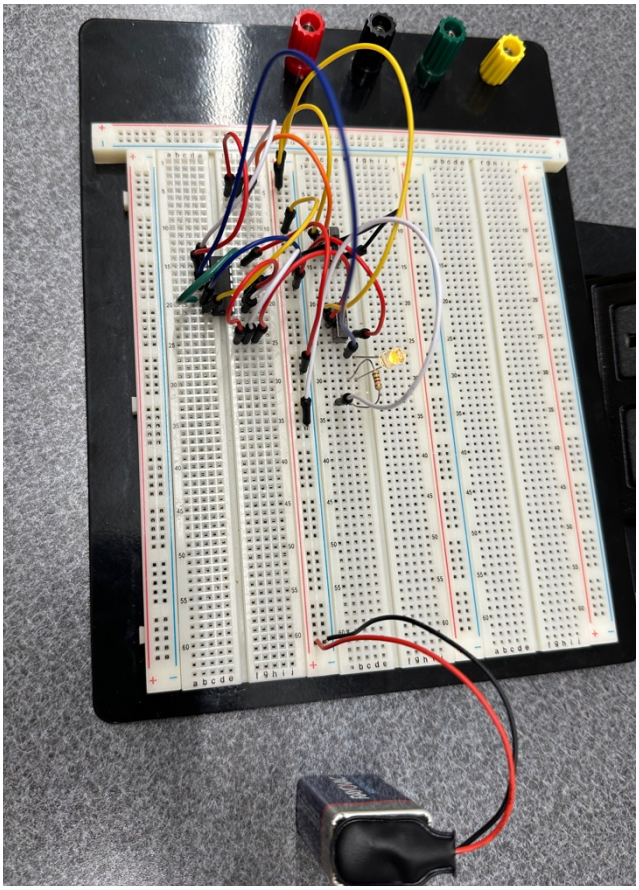
2) Inverter using QuadNAND IC



3) AND gate using QuadNAND IC



4) OR gate using QuadNAND IC



5) NOR gate using QuadNAND IC