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EGR 24L Introduction of Circuit Analysis Laboratory

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**Lab S1: Special Topic of Electronics- MOSFET, CMOS Inverter**

**Introduction:**

In this special lab professor introduced us to MOSFET (Metal Oxide Semiconductor Field Effect) including both n-channel and p channel MOS (NMOS and PMOS). MOSFET is a compact transistor that used to control the flow of electric current by regulating how much voltage flows through them. Inside MOSFET there are three metal pins: source, gate, and drain. The voltage applied to gate, the current flows from drain to source. There are three types of MOSFET but in this lab we only focus on two types which are N-Channel (NMOS) and P-Channel (PMOS).

N-Channel enhancement aka NMOS is type that allow current to flow through the channel drain and source even with zero input voltage applied across its terminals, in NMOS when $V_{gs}$is greater than the threshold voltage $V_{th}$, the transistor turn on and the voltage is close. If the threshold voltage is less than $V_{gs}$, the transistor is off and the connection between drain and source is off.

Second type is P-Channel enhancement -mode aka PMOS, this type requires a zero gate-source voltage for current conduction. Unlike NMOS, in PMOS when $V_{gs}$ is greater than $V_{th}$ the switch is off, when $V_{gs}$ is less than $V_{th}$ the switch is on.

In this lab, we embarked on a journey to unravel the inner workings of transistors, delving deep into the intricacies of MOSFETs, both N-MOS and P-MOS. Through hands-on experimentation, we not only grasped their fundamental principles and basic properties but also harnessed their transformative power in real-world applications, illuminating the path to technological innovation.

**Procedure:**

1) Part 1a: NMOS basic operation, we explore NMOS, construct the circuit follow the picture from the spec sheet. We know that when the gate to source voltage drop Vgs is below a threshold Vth, the switch will close, the current cannot flow between drop and source. After we construct the first circuit, we we record the value in excel, of Id vs Vgs and Vds vs Vgs.

2) Part 1B: PMOS basic operation. we explore PMOS, construct the circuit follow the picture from the spec sheet. Unlike NMOS, in PMOS when $V_{gs}$ is greater than $V_{th}$ the switch is off, when $V_{gs}$ is less than $V_{th}$ the switch is on. After we construct the second circuit, we record the value in excel, of Id vs Vgs and Vds vs Vgs.

3) Part2: Digital Application CMOS logic gates, logic inverter (NOT gates), in this part we will construct circuit follow the spec sheet with the concept to explore logic gate of NOT gate. We were using one NMOS and one PMOS to construct the following CMOS inverter circuit with the input sliding input switch (SPDT).

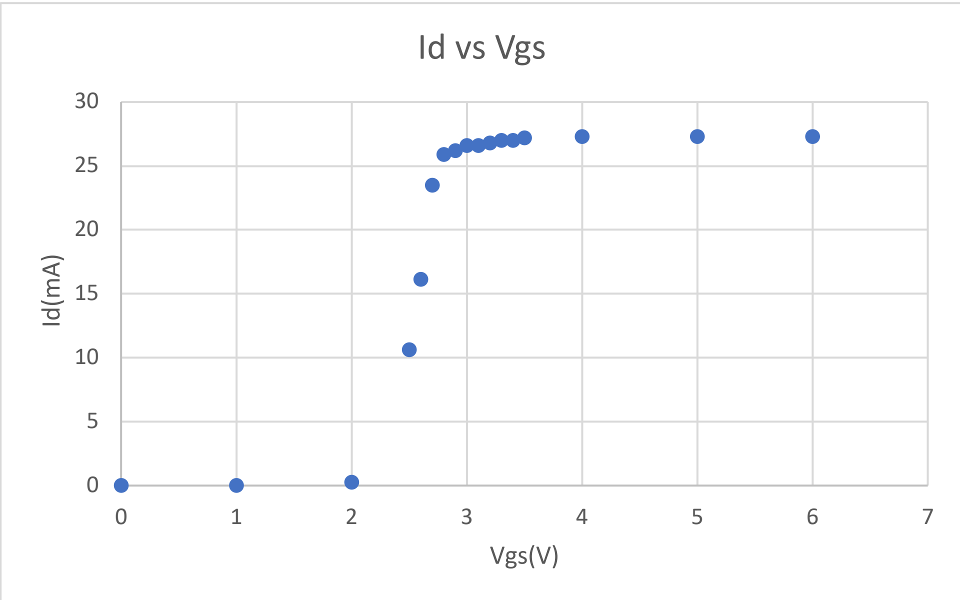
**Conclusion:**

In conclusion, in fist special lab we were exploring another core fundamental knowledge of circuit which is transistor. We get to learn how the semiconductor material work and how important of transistor. Moreover, we also dive deep to how use PMOS and NMOS create CMOS inverter circuit which we apply idea of truth table to construct and understand how the circuit work. This lab is very essential for electrical engineer to understand the process truth table logic work coordinately with circuit.

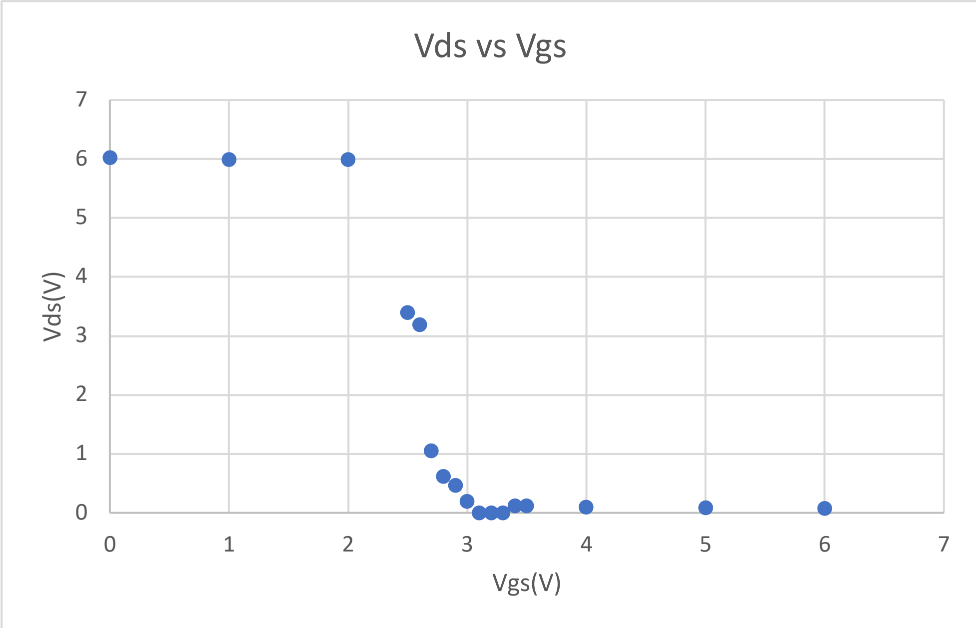
**Appendixes:**

Part 1: NMOS data table

| Id (A) | vgs (V) |
|---|---|
| 0 | 0 |
| 0 | 1 |
| 0.25 | 2 |
| 10.65 | 2.5 |
| 16.14 | 2.6 |
| 23.5 | 2.7 |
| 25.9 | 2.8 |
| 26.2 | 2.9 |
| 26.6 | 3 |
| 26.6 | 3.1 |
| 26.8 | 3.2 |
| 27 | 3.3 |
| 27 | 3.4 |
| 27.2 | 3.5 |
| 27.3 | 4 |
| 27.3 | 5 |
| 27.3 | 6 |



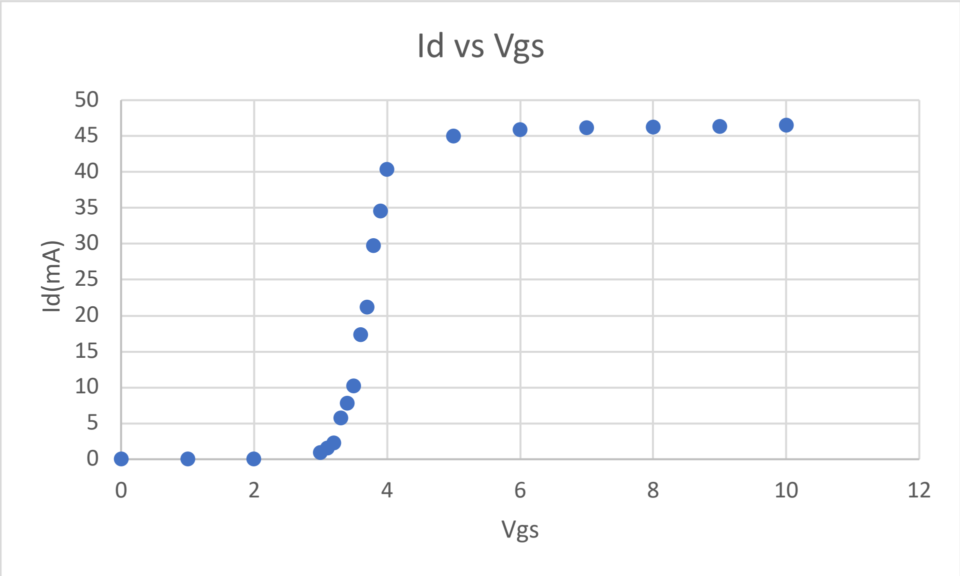
| Vds(V) | vgs (V) |
|---|---|
| 6.03 | 0 |
| 6 | 1 |
| 6 | 2 |
| 3.4 | 2.5 |
| 3.2 | 2.6 |
| 1.056 | 2.7 |
| 0.62 | 2.8 |
| 0.47 | 2.9 |
| 0.196 | 3 |
| 0.000151 | 3.1 |
| 0.000135 | 3.2 |
| 0.000130 | 3.3 |
| 0.1213 | 3.4 |
| 0.118 | 3.5 |
| 0.1034 | 4 |
| 0.088 | 5 |
| 0.0827 | 6 |



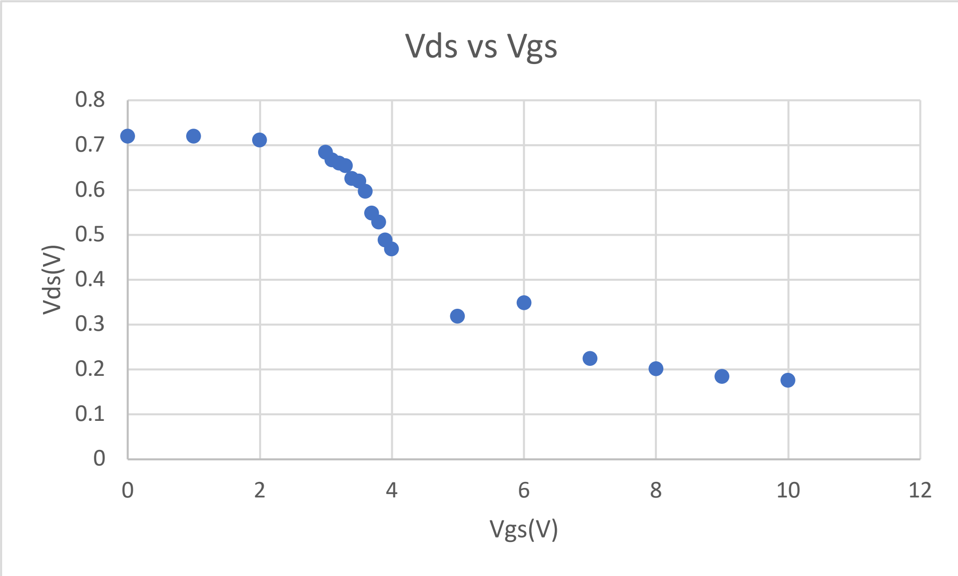

| | | |
|---|---|---|
| Id vs. Vgs plot | plese see above | |
| Vds vs. Vgs plot | Please see above | |
| Threshold voltage Vtn (V) | Please see above | |
| Full conduction Vgs (V) | Vgs > Vth | |
| When Vgs is below Vtn, the NMOS is in what mode? (conduction/non-conduction) | | Non-conductive |
| When NMOS is in non-conduction mode, it behaves like open or short circuit? | | Short circuit |
| When Vgs is above Vtn, the NMOS is in what mode? (conduction/non-conduction) | | Conductive mode |
| When NMOS is in full conduction mode, it behaves like open or short circuit? | | Open circuit |

Part 1: PMOS data table

| Id (mA) | vgs (V) |
|---|---|
| 0 | 0 |
| 0 | 1 |
| 0 | 2 |
| 0.87 | 3 |
| 1.5 | 3.1 |
| 2.23 | 3.2 |
| 5.71 | 3.3 |
| 7.8 | 3.4 |
| 10.18 | 3.5 |
| 17.3 | 3.6 |
| 21.2 | 3.7 |
| 29.7 | 3.8 |
| 34.5 | 3.9 |
| 40.3 | 4 |
| 45 | 5 |
| 45.9 | 6 |
| 46.1 | 7 |
| 46.2 | 8 |
| 46.3 | 9 |
| 46.5 | 10 |



| Vds | vgs (V) |
|---|---|
| 0.72 | 0 |
| 0.72 | 1 |
| 0.712 | 2 |
| 0.685 | 3 |
| 0.668 | 3.1 |
| 0.661 | 3.2 |
| 0.655 | 3.3 |
| 0.6263 | 3.4 |
| 0.62 | 3.5 |
| 0.598 | 3.6 |
| 0.55 | 3.7 |
| 0.53 | 3.8 |
| 0.49 | 3.9 |
| 0.47 | 4 |
| 0.32 | 5 |
| 0.35 | 6 |
| 0.225 | 7 |
| 0.202 | 8 |
| 0.186 | 9 |
| 0.1774 | 10 |




| | | |
|---|---|---|
| Id vs. Vsg plot | Please see information above | |
| Vsd vs. Vsg plot | Please see information above | |
| Threshold voltage Vtp (V) | See information above | |
| Full conduction Vsg (V) | Vgs > Vth | |
| When Vsg is below Vtp, the PMOS is in what mode? (conduction/non-conduction) | | conductive |
| When PMOS is in non-conduction mode, it behaves like open or short circuit? | | open |
| When Vsg is above Vtp, the PMOS is in what mode? (conduction/non-conduction) | | Non-conductive |
| When PMOS is in full conduction mode, it behaves like open or short circuit? | | Short circuit |

Part 2: CMOS inverter working principles.

| | | |
|---|---|---|
| Input node a’s logic value | 0 | 1 |
| Input switch togged to 0V or 5V? | 0 | 5 |
| Input node a’s voltage = 0V or 5V? | 0 | 5 |
| Input LED is on or off? | off | on |
| NMOS Vgs = 0V or 5V? | 0V | 5V |
| NMOS is conductive/non-conductive? | Non-conductive | conductive |
| Output node f is shorted to ground (Y/N)? | Y | N |
| PMOS Vsg = 0V or 5V? | 0V | 5V |
| PMOS is conductive/non-conductive? | conductive | Nonconductive |
| Output node f is shorted to 5V power rail (Y/N)? | Y | N |
| Output node f’s voltage = 0V or 5V? | 0V | 5V |
| Output LED is on or off? | off | On |
| Output node f’s logic value f = 0 or 1? | f=0 YES | f=1 YES |