GPIO Controller

																	Bi	t																	
Word Offset	Byte Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Mode
0	0	Χ	Χ	F	PIN 9		F	IN 8	3	ı	PIN 7		P	IN 6		F	PIN 5		Р	IN 4		Р	IN 3		P	PIN 2		P	IN 1		PΙ	N 0			
1	4	Χ	Χ	Р	IN 1	9	Р	IN 1	8	PIN 17			P:	IN 16	5	Р	IN 15	5	P]	[N 14	ı	P.	[N 13	3	Р	IN 12	2	PΙ	N 11		PII	V 10			
2	8	Χ	Χ	Р	IN 2	9	Р	PIN 28			PIN 27			PIN 26		Р	IN 25	5	PIN 24		ļ	Ρ]	PIN 23		PIN 22		2	PIN :			PII	PIN 20		FUNCTION	R/W
3	12	Χ	Χ	Р	IN 3	9	PIN 38			Р	IN 3	7	Ρ.	IN 36	5	Р	IN 35	5	P]	[N 34	1	Ρ.	PIN 33		P	PIN 32		PΙ	N 31		PII	N 30		000-input	IX7 W
4	16	Χ	Χ	PIN 49			Р	IN 4	8	Р	IN 47		PIN 46		5	PIN 45		5	P1	[N 44	ļ	P.	[N 43	3	P	IN 42	2	PΙ	N 41	PJ		PIN 40		001-output	
5	20	Χ	Χ	Χ	Χ	Χ	X X X			Х Х Х		Χ	х Х х		Χ	X X X		Χ	χ Х χ		Χ	PIN 53		3	PIN 52			ΡI	N 51		PIN 50				
6	24	Reserved																-																	
7	28	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0)	W
8	32	Χ	Χ	Х	Χ	Χ	Χ	Χ	Χ	Χ	Х	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	SET	
9	36	Reserved																-																	
10	40	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	-	W
11	44	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	CLEAR	
12	48																	-																	
13	52	31	30	29	28	27	26	25				21	20	19	18	17	16	15	14	13	12	11	10	9	8		6	5	4	3	2	1	0		R
14	56	Χ	Χ	Х	Χ	Χ	Χ	Χ	Χ	Χ	Х	53	52	51	50		48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	LEVEL	
15	60																Rese	rved															_		-
16	64	31	30				26			23		21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	EVENT	R/W
17	68	Χ	Χ	Х	Χ	Χ	Χ	Χ	Χ	Χ	Х	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	DETECT STATUS	
18	72																Rese																		-
19	76	31	30				26					21	20	19		17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 F	RISING EDGE	R/W
20	80	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	DETECT	
21	84																Rese									_	-	_					_		-
22	88	31	30				26			23		21	20	19		17		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	FALLING	R/W
23	92	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	53	52	51	50	49	48 Resei	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32 E	EDGE DETECT	
24	96	24	20	20	20	27	2.0	25	2.4	22	22	21	20	1.0	1.0				1.4	12	12	11	1.0	0	0	7	6	Е	4	2	2	1	0		-
25	100 104	31 X	30 X	29 X	28 X	27 X	26 X	25 X	24 X	23 X	22 X	21 53	20	19 51	18 50	17 49	16	15	14 46	13 45	12	11 43	10 42	9 41	40	7 39	6 38	37	36	35	34	33	0 22 F	HIGH DETECT	R/W
26	104	X	X	X	Ă	Ă	Ă	X	Ă	Ă	X	53	52	51	50		48 Resei	47	46	45	44	43	42	41	40	39	38	3/	30	35	34	55 .	52	ITOH DETECT	
27	112	31	30	29	28	27	26	2.5	2.4	23	22	21	20	19	18	17	I	15	1 /	13	12	11	10	9	8	7	6	Е	1	2	2	1	0		-
29	116	У Х	У Х	X X	X	27 X	26 X	25 X	24 X	X	22 X	21 53	52	51	50	49	16 48	47	14 46	45	12	43	10 42	41	40	39	38	37	36	35	34	33	32	LOW DETECT	R/W
30	120	Λ	٨	٨	٨	٨	٨	٨	٨	٨	٨	JJ	32	JΙ	שכ		Rese		40	40	44	40	42	41	40	22	20	۱ د	50	JJ	54	. دد	22	LUM DETECT	_
30	120																	vcu																	_

GPIO Controller

31	124	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		R/W
32	128	Χ	Х	Х	Χ	Χ	Х	Х	Х	Χ	Χ	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	ASYNC RISING EDGE	
33	132			Reserved																-															
34	136	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	g	8	7	6	5	4	3	2	1	0	ASYNC	R/W
35	140	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	FALLING	K/W
36	144		Reserved																EDGE	-															
37	148	Х	Х	Х	Х	Х	X	Х	Х	Х	Х	Χ	Χ	Х	Х	Χ	Х	Х	Х	X	Χ	Х	Χ	Χ	Х	Χ	Х	Х	Х	Х	Х	PU		PULL UP/DOWN ENABLE 00=off 01=pull down 10=pull up	R/W
38	152	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	PULL	R/W
39	156	Х	Х	Х	Χ	Х	Х	Х	Х	Χ	Χ	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	UP/DOWN	K/W
40	160																Rese	rved																CLOCK	-