Tz-Ching Yu

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EDUCATION

École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland

- MSc. student in Computer Science
  - GPA: 5.29 / 6
  - Relevant courses: Interactive Theorem Proving, Constructive Computer Architecture, Advanced Compiler Construction, Embedded Systems, Advanced Computer Architecture Sep 2022 –

National Taiwan University of Science and Technology, Taipei, Taiwan

- BSc. in Electronic and Computer Engineering Sep 2016 – Jun 2020
  - GPA: 4.05 / 4.3
  - Relevant courses: Microcomputer Principles and Applications, Embedded System Design, Digital Logic Design, Parallel Architectures, Real-Time Operating Systems

EXPERIENCE

École Polytechnique Fédérale de Lausanne

- Student assistant advised by Prof. Thomas Bourgeat Jul 2023 –
  - Worked on formally specifying and verifying digital circuits with Coq
- Course assistant for CS-470 Advanced Computer Architecture Feb 2024 – Jun 2024

Research Center for Information Technology Innovation, Academia Sinica

- Research assistant advised by Prof. Hsiang-Yun Cheng Jul 2020 – Nov 2020, Jul 2021 – Aug 2022
  - Worked on ReRAM, DNN accelerator, neural network sparsity, architectural design and evaluation, hardware-software co-design

PUBLICATION

- Chen-Yang Tsai, Chin-Fu Nien, **Tz-Ching Yu**, Hung-Yu Yeh, Hsiang-Yun Cheng "RePIM: Joint Exploitation of Activation and Weight Repetition for In-ReRAM DNN Acceleration," in *Proceedings of ACM/IEEE Design Automation Conference*, San Francisco, USA, Dec 2021

PROJECTS

- **Exploring the Instructional Landscape of RISC-V and Arm using CloudSuite: Differences and Insights**
  - In the project, we compares the computational characteristics of RISC-V and ARM architectures using three specific benchmarks from CloudSuite. [report] [poster]
- **Peer/Place**
  - A project inspired by r/place where players share a massive canvas and could each change the color of a pixel at a given interval. [report] [slides]
  - In the project, we used Paxos to achieve consensus and threshold cryptography for administration, and we also included SybilGuard to the system
- **Development of digital system of VGA interface and Pong game**
  - Implemented a VGA interface that takes pixels and generates signals according to the standard and a simple Pong game with Mandelbrot set as background computed using fixed-point arithmetic [slides]
- **Digital design of camera and LCD interfaces and development embedded software**
  - Designed and implemented interfaces for camera module (TRDB-D5M) and LCD module (LT24) on a FPGA board which involved pixel acquisition from the camera, recombination of each color, and storing and accessing on-chip memory through DMA [report]
- **Exploring Weight and Activation Sparsity of Deep Neural Networks for ReRAM-based Accelerator**
  - Developed techniques that speedup inference computation of ReRAM-based accelerators by 15.24× and reduce energy consumption by 96.07% given the inherent constraints of ReRAM, such as reliability of memory cells and digital-to-analog converters latency, by exploiting both weight and activation sparsity of neural networks

SKILLS

C, Python, Scala, Coq, Verilog, Bluespec, PyTorch, Git

LANGUAGES

English (C1), Mandarin (Native)