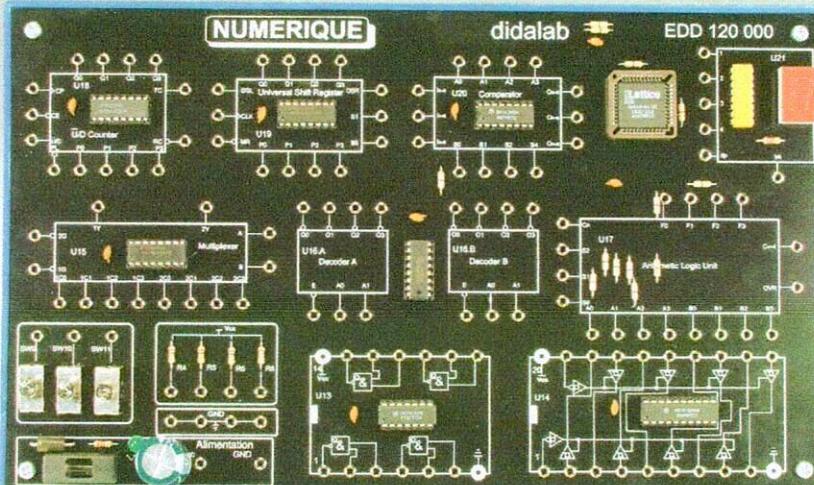


DIGITAL LOGIC

EDD 120 000



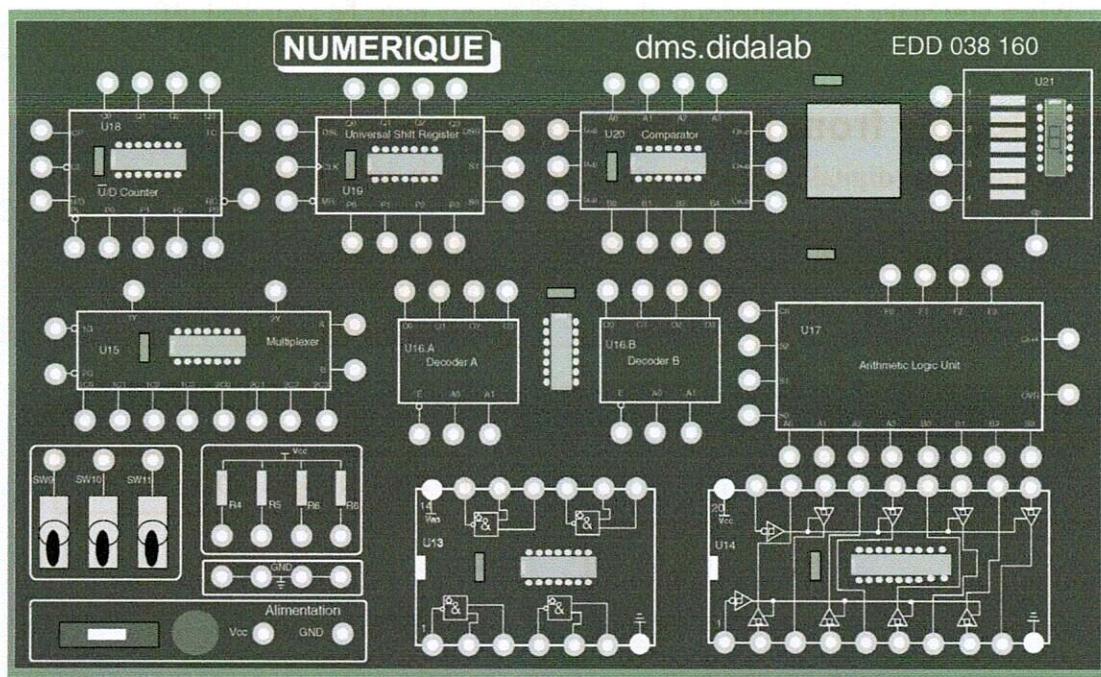
Technical Guide

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1 Presentation

The digital logic module is used to study the advanced logic circuits. It must be used with the basic logic (EDD 100 000).



The digital module (EDD 120 000) includes:

- Power supply protection (fuse and transil),
- 4 ground's sockets,
- 4 PULL-UP resistances,
- 1 Logic key generator (0 or 1),
- 1 Open collector NAND circuit,
- 3- states buffer,
- 2 multiplexers,
- 2 demultiplexers,
- 1 4-bits counter/decounter,
- 1 offset register, serial/parallel and parallel/serial,
- 1 4-bits comparator,
- 1 7-segments display with its binary/hexadecimal encoder (BCD),
- 1 8-operations Arithmetic and Logic Unit (ALU).

2 Installation

The digital module needs a 5-Vdc power supply.

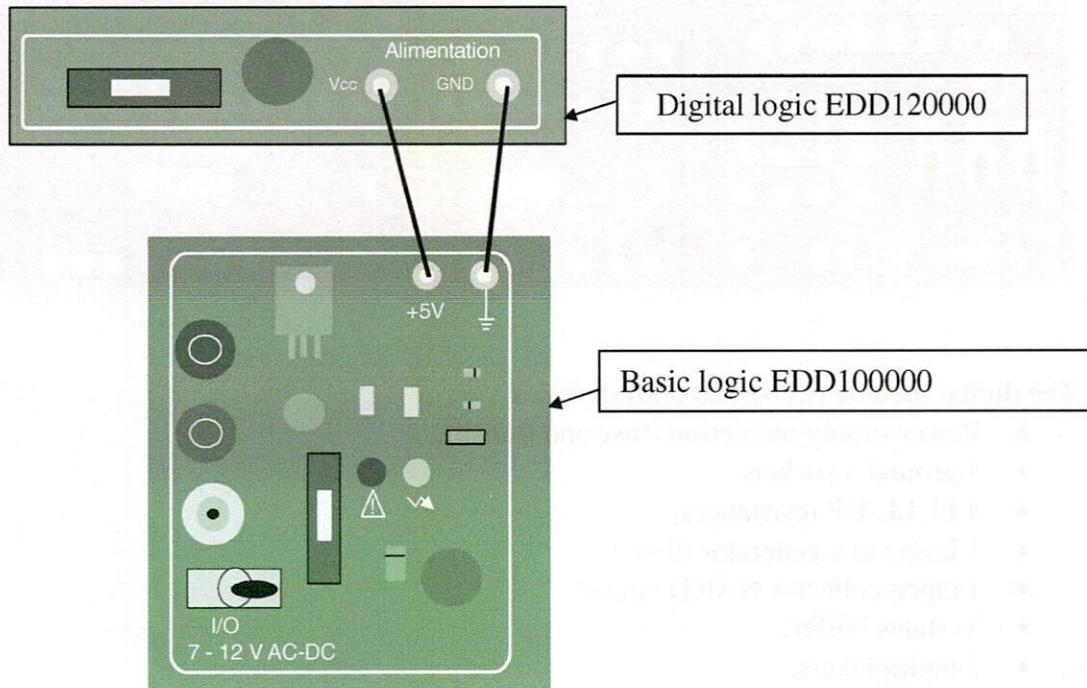
To connect the power supply, you need to use the Ø 2-mm sockets named GND and VCC.

When you make the connection, the power supply must be switched off.

2.1 Supply from the basic logic module

To supply the digital module, you have to connect it with the Ø 2-mm sockets:

Basic Logic	Digital Logic	Description
GND	GND	Ground
+5V	VCC	+5V power supply



2.2 Supply from a powersupply

If you want to supply the module with another power supply, you have to connect:

The Ground of the power supply to GND,

+5 V of the power supply to VCC.

3 Locations of the components

As the digital module is an extension of the basic logic module, the numbering of the components follows the numbering of the basic module's components

Location	Description
GND	4 Ground sockets
R4 to R6	4 PULL-UP resistances
SW9 to SW11	3 ON/OFF keys
U13	Open collector NAND cell (model 7401)
U14	3-states Buffer (model 74244)
U15	Multiplexer (model 74253)
U16A U16B	Encoder (model 74139)
U17	ALU (compatible 74382)
U18	4-bits counter/decounter (model 74191)
U19	offset register, serial/parallel and parallel/serial (model 74194)
U20	4-bits comparator (model 7485)
U21	7-segments display with its binary/hexadecimal encoder (BCD)

4 Descriptions of the components

In the following paragraphs, we give you the main characteristics of each cell. For more details, please read the DATA-SHEETS of each component.

4.1 Notation

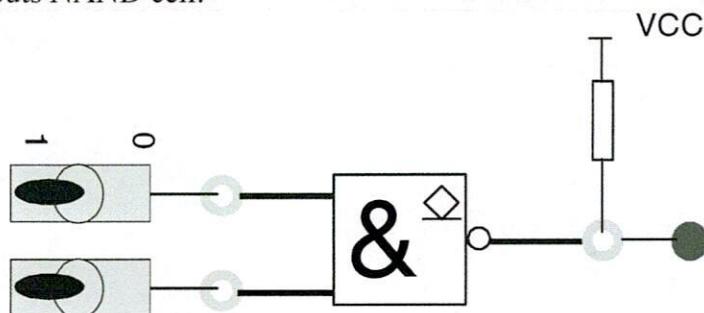
In the next paragraphs, in the truth table, we will use the following notations::

Notation	Description
0	Low logic level (0 V)
1	High logic level ($V_{CC} = +5 \text{ V}$)
X	0 or 1 State
Z	High impedance

4.2 U13 : Open collector NAND circuit

The open collector NAND cell are of the 7401 model..

Test of the 2-inputs NAND cell:

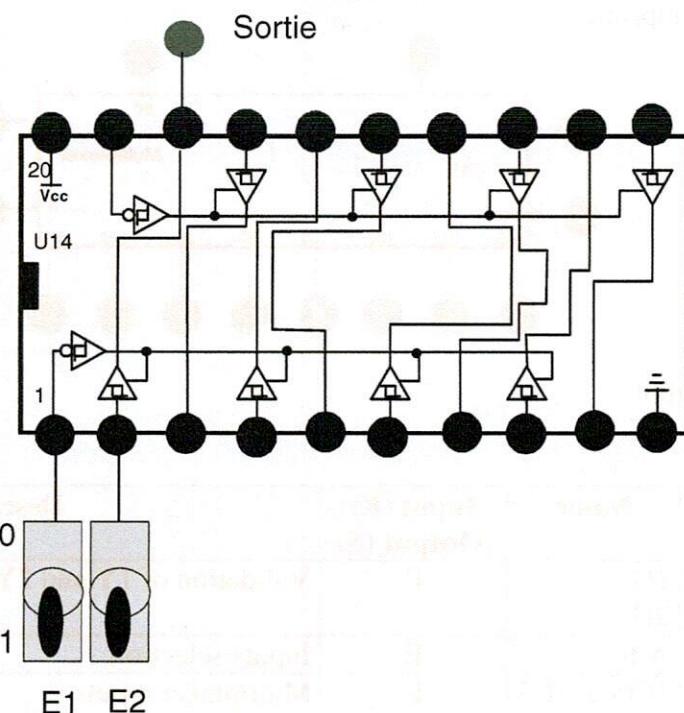


Check the following truth table:

SW1	SW2	Output state	Led state
0	0	1	Lit
0	1	1	Lit
1	0	1	Lit
1	1	0	Turned-off

4.3 U14 : 3- states Buffer

The 3-states buffer is realized with a 74244 component.
 To test the buffer cell, please make the following setting:



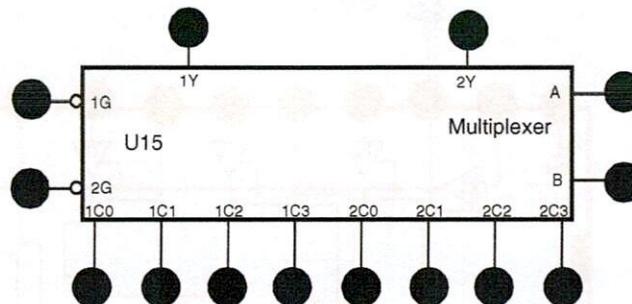
Truth table :

E1	E2	Output	Description
0	0	0	Copy of e2 input
0	1	1	
1	0	Z	High Impedance state
1	1	Z	

4.4 U15 : Multiplexer

The multiplexer is realized with a 74253 component which is a double multiplexer with 4 inputs and 2 3-states

Multiplexer imprint:



Pins' description:

Name	Input (E) /Output (S)	Description
1G 2G	E	Validation of 1Y and 2Y outputs
A,B	E	Inputs selection
1C0 à 1C3 2C0 à 2C3	E	Multiplexer inputs
1Y 2Y	S	Multiplexer outputs

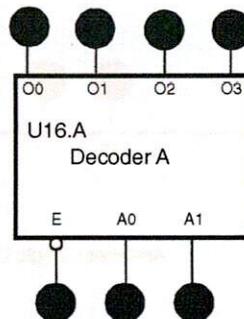
Truth table:

Inputs choice		Multiplexer Input				Output's validation	Output
A	B	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	Z
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
1	0	X	0	X	X	0	0
1	0	X	1	X	X	0	1
0	1	X	X	0	X	0	0
0	1	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

4.5 U16: Demultiplexer

The demultiplexer is realized with a 74139 components which is a double 1 / 4 demultiplexer.

Demultiplexer's imprint :



Pins' description:

Name	Input (E) /Output (S)	Description
E	E	Inputs' validation (active when at low level)
A0,A1	E	Inputs address
O0 to O3	S	Outputs (active when at low level)

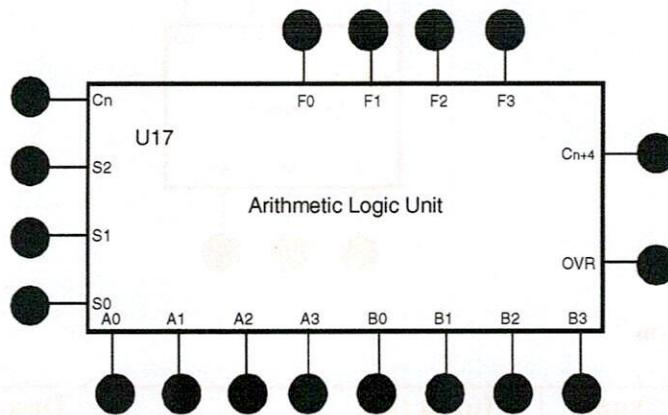
Truth table:

Inputs			Outputs			
E	A0	A1	O0	O1	O2	O3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	1	0	1	0	1	1
0	0	1	1	1	0	1
0	1	1	1	1	1	0

4.6 U17: Arithmetic and Logic Unit

The ALU is realized with an MACH.EPLD Its functioning is compatible with the 74382 component.

ALU's imprint :



Pins' description:

Name	Input (E) /Output (S)	Description
S0 to S2	E	Selection of the arithmetic or logic operation.
Cn	E	
A0 to A3 B0 to B3	E	Input value on 4 bits
F0 to F3	S	Output put value on 4 bits
Cn+4	S	Carry of the F3 cell
OVR	S	Overshoot of the 2 last cells

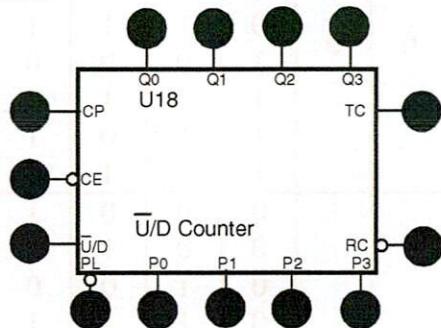
Truth table :

Function	Inputs						Outputs					
	S0	S1	S2	Cn	An	Bn	F0	F1	F2	F3	OVR	Cn+4
CLEAR	0	0	0	X	X	X	0	0	0	0	0	0
B minus A	1	0	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	1	1	1	0	1
				0	1	0	0	0	0	0	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	1	1	1	0	1
				1	1	0	1	0	0	0	0	0
A minus B	0	1	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	0
				0	1	0	0	1	1	1	0	1
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	0	0	0	0	0
				1	1	0	1	1	1	1	0	1
APLUS B	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	0	1	1	1	0	1
				1	0	0	1	0	0	0	0	0
				1	0	1	0	0	0	0	0	1
				1	1	1	1	1	1	1	0	1
A ⊕ B	0	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				X	1	1	0	0	0	0	1	1
				1	1	0	1	1	1	1	1	1
				X	0	0	0	0	0	0	0	0
A + B	1	0	1	X	0	0	0	0	0	0	0	0
				X	0	1	1	1	1	1	0	0
				X	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
				X	0	0	0	0	0	0	0	0
A . B	0	1	1	X	1	0	0	0	0	0	1	1
				X	0	1	0	0	0	0	0	0
				0	1	1	1	1	1	1	1	0
				1	1	1	1	1	1	1	1	1
				SET	1	1	1	X	X	X	1	1

4.7 U18: Counter/decounter

The binary 4-bits counter/ decounter (up/down counter) is realized with a 74191 component.

Counter/decounter 's imprint :

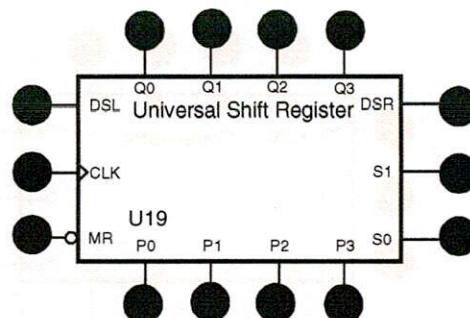


Pins' description:

Name	Input (E) /Output (S)	Description
CP	E	Clock input, active on a rising edget
CE	E	Input for the counter validation (active at level 0)
U/D	E	Operating mode: 0 : counter 1 : decounter
PL	E	Input for loading activation (active at level 0)
P0 to P3	E	Inputs for the definition of the load's value (4 bits)
Q0 à Q3	S	Counter/decounter output
RC	S	Pulse for counting and decounting
TC	S	End of count/ decount

4.8 U19 : 4- bits offset register, bidirectional

The bidirectional offset register (or shift register) is realized with a 74194 component.
Register's imprint :



Pins' description

Name	Input (E) /Output (S)	Description
S0,S1	E	Operating mode
P0-P3	E	Input parallel data
DSR	E	Serial input, right shift
DSL	E	Serial input, left shift
CLK	E	Clock input, active on rising edge.
MR	E	Zeroing Input (active at level 0)
Q0 to Q3	S	Output data on 4 bits

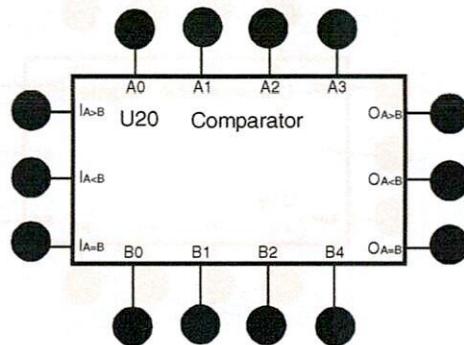
Truth table and functioning mode:

Functioning mode	Inputs						Outputs			
	MR	S1	S0	DSR	DSL	Pn	Q0	Q1	Q2	Q3
Reset	0	X	X	X	X	X	0	0	0	0
Blocked	1	0	0	X	X	X	Q0	Q1	Q2	Q3
Left shift	1	1	0	X	0	X	Q1	Q2	Q3	0
	1	1	0	X	1	X				1
Right shift	1	0	1	1	X	X	0	Q0	Q1	Q2
	1	0	1	0	X	X	1			
Parallel loading	1	1	1	X	X	Pn	P0	P1	P2	P3

4.9 U20 : 4-bits comparator

The 4-bits comparator is realized with a 7485 component.

Comparator's imprint:



Pins' description

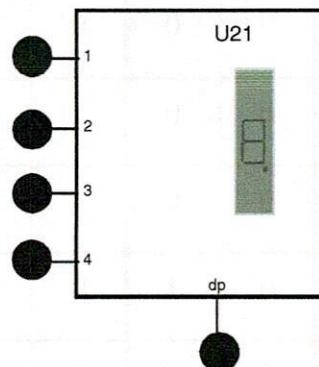
Name	Input (E) /Output (S)	Description
A0 à A3 B0 à B3	E	4-bits Input of the comparator
I a=b	E	
I a<b	E	Input of a previous comparator
I a>b	E	
O a=b	S	Active output if a=b
O a<b	S	Active output if a<b
IO a>b	S	Active output if a>b

Truth table:

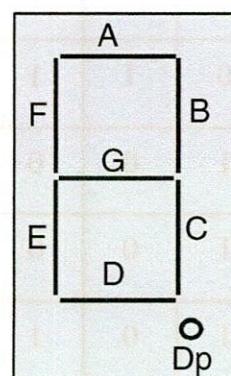
Compared Inputs				Cascade Inputs			Outputs		
A3,B3	A2,B2	A1,B1	A0,B0	Ia>b	Ia<b	Ia=b	Oa>b	Oa<b	Oa=b
A3>B3	X	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	0	1	0
A3=B3	A2>B2	X	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	0	1	0
A3=B3	A2=B2	A1>B1	X	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	0	1	0
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	A0=B0	0	1	0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	1	1	0	0	0	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	0	1	1	0

4.10 U21 : 7-segments display

The 7-segments display block includes the 7-segment display and its binary hexagonal encoder. The binary hexagonal encoder is realized with a MACH4 EPLD.



Description of the display's segments:



Pins' description

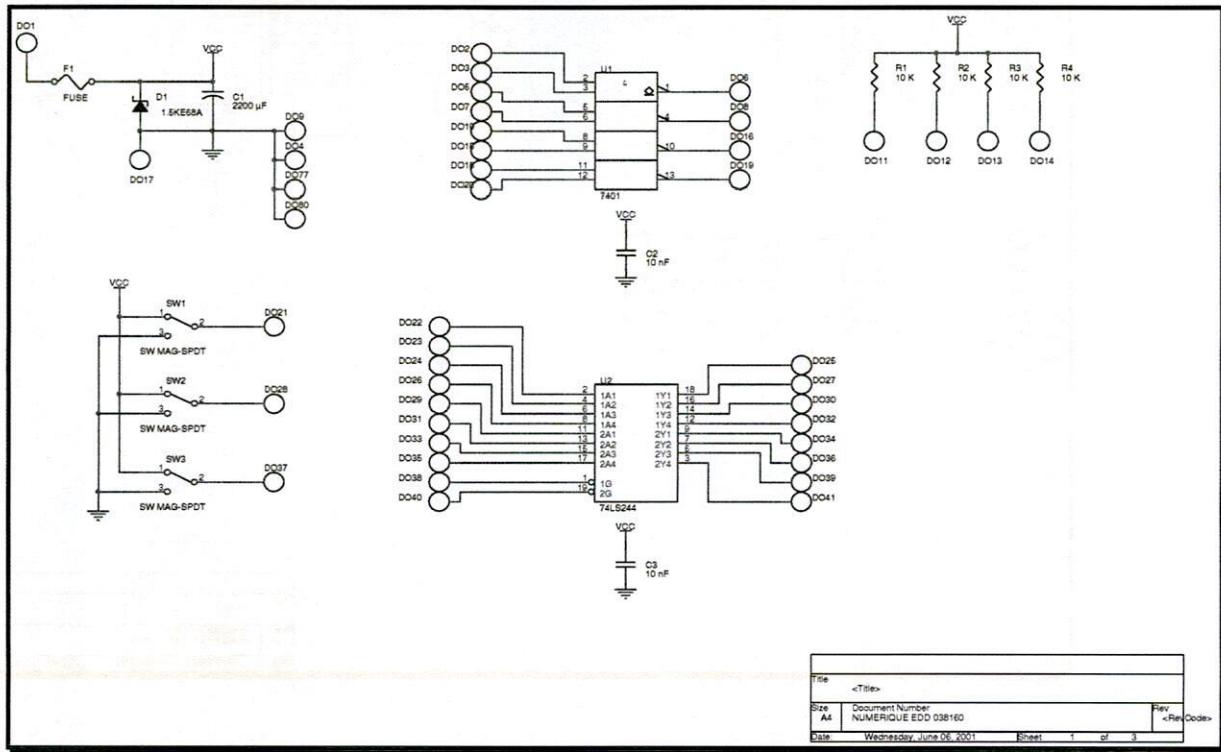
Name	Input (E) /Output (S)	Description
1 à 4	E	Binary value on 4 bits at the Binary / Hexadecimal encoder input
Dp	E	Control of the display's comma

Truth table:

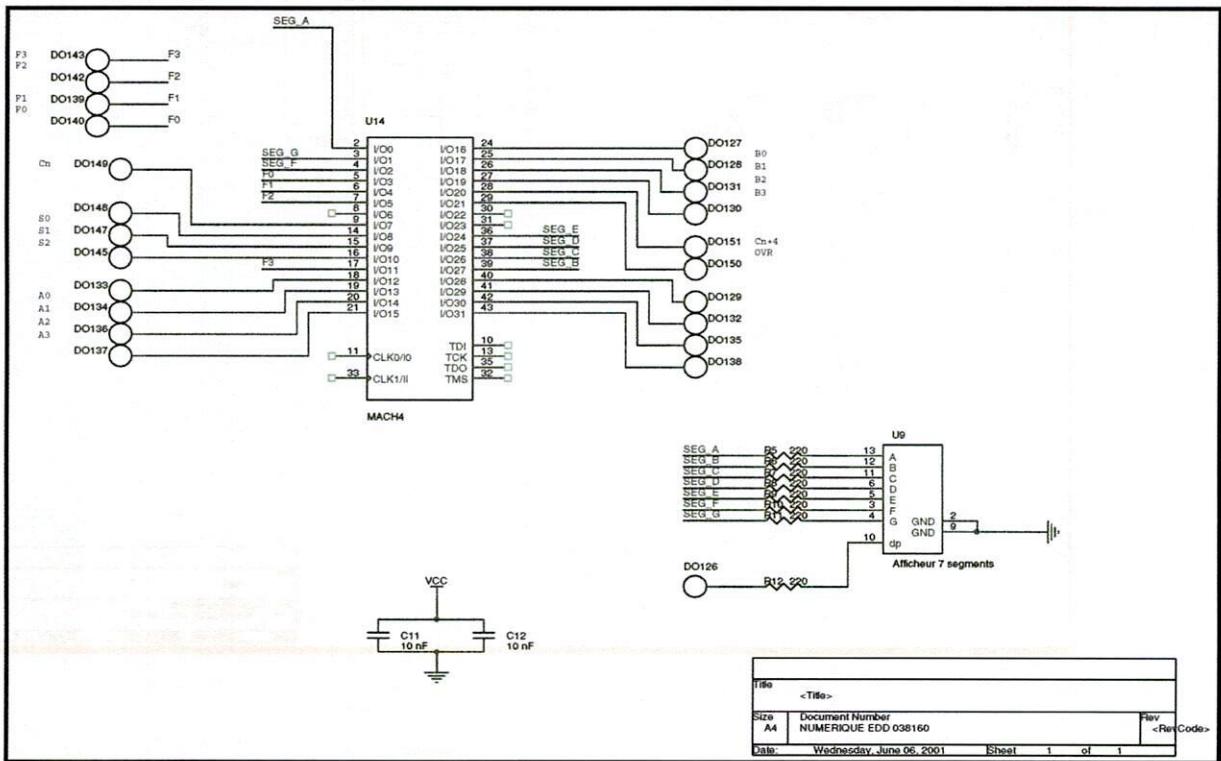
Hexadecimal value	Inputs				Display
	4	3	2	1	
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
A	1	0	1	0	0
B	1	0	1	1	1
C	1	1	0	0	2
D	1	1	0	1	3
E	1	1	1	0	4
F	1	1	1	1	5

5 Diagrams

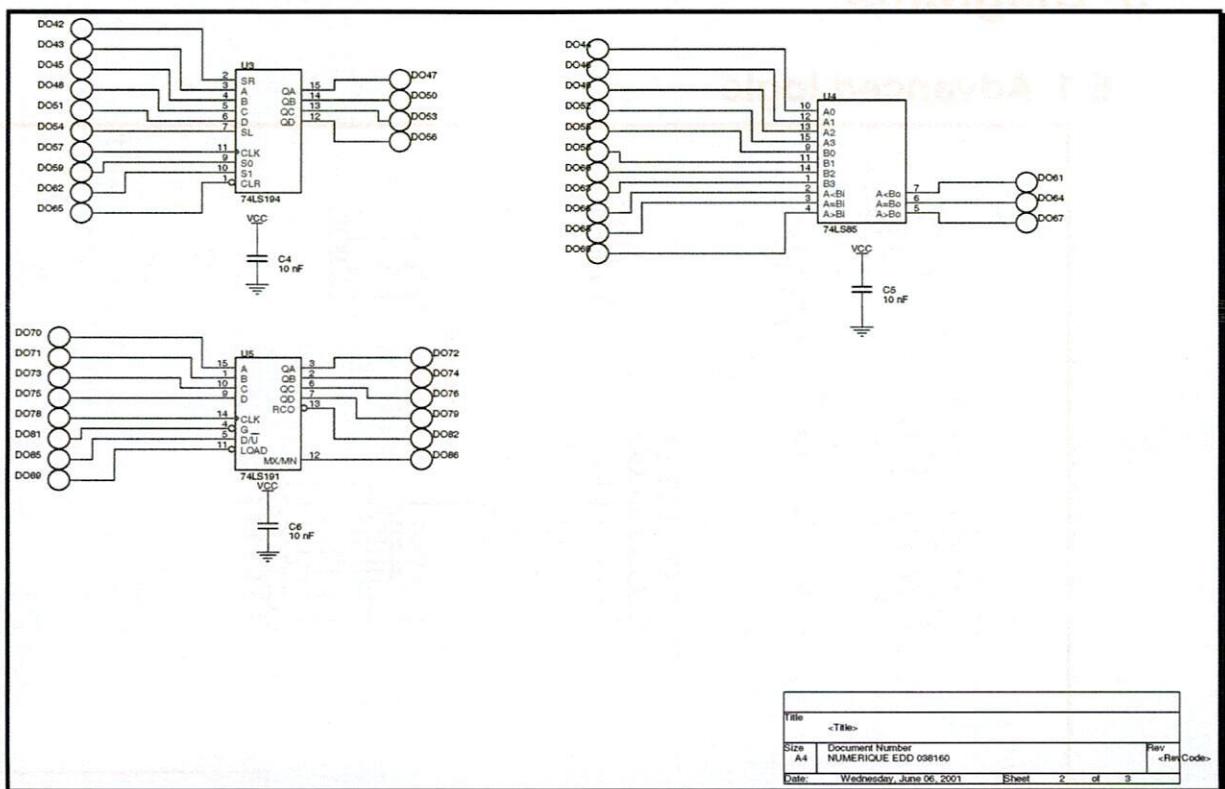
5.1 Advanced logic



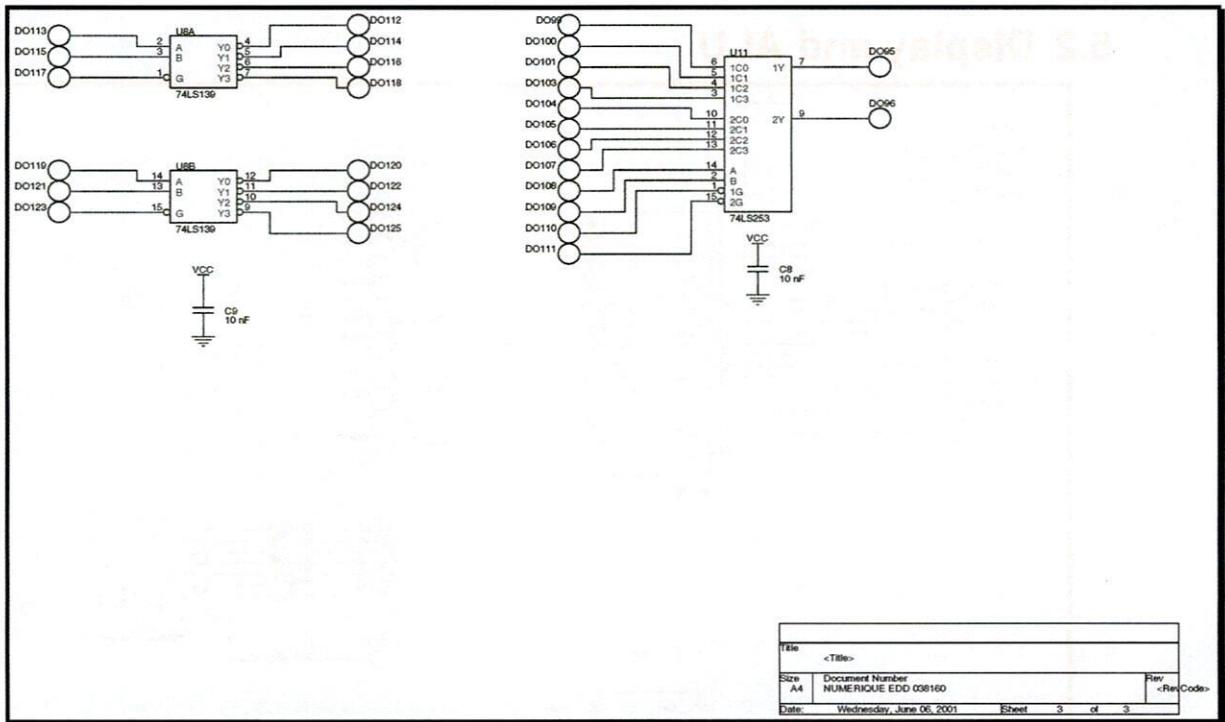
5.2 Display and ALU



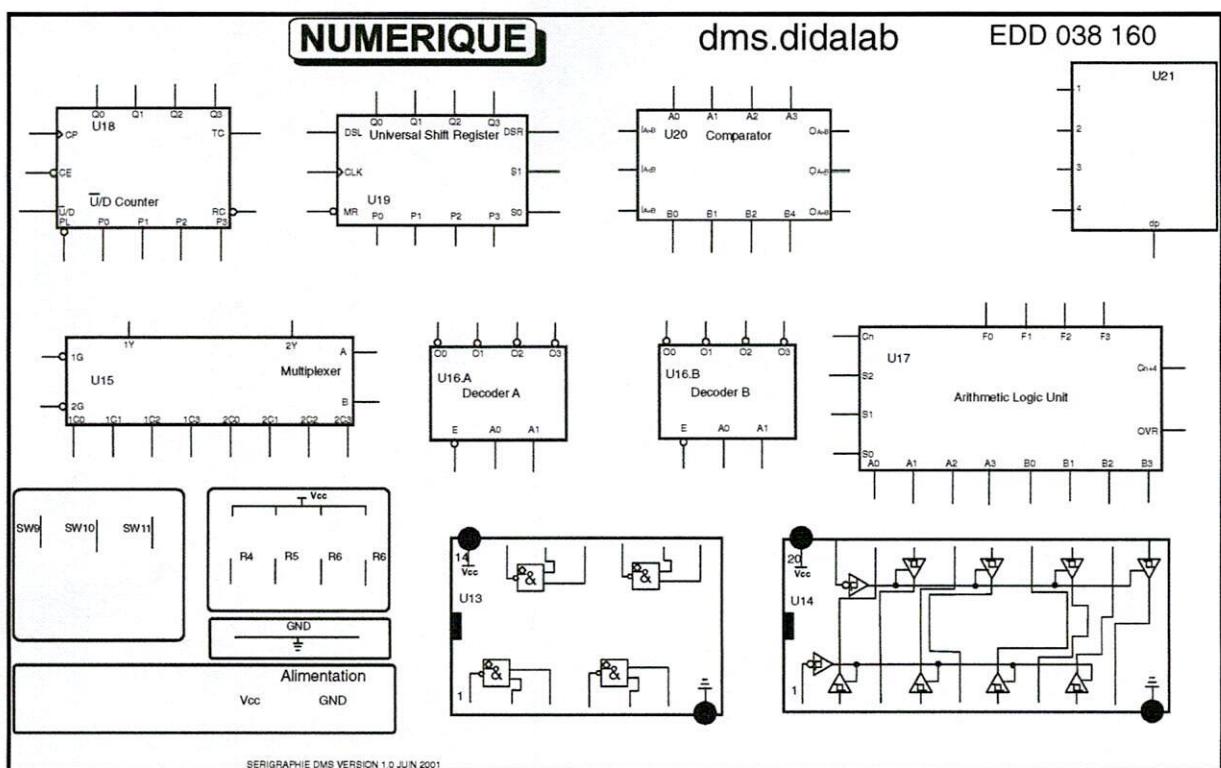
5.3 Advanced logic



5.4 Multiplexer and encoder



6 Layout



8. Figure

