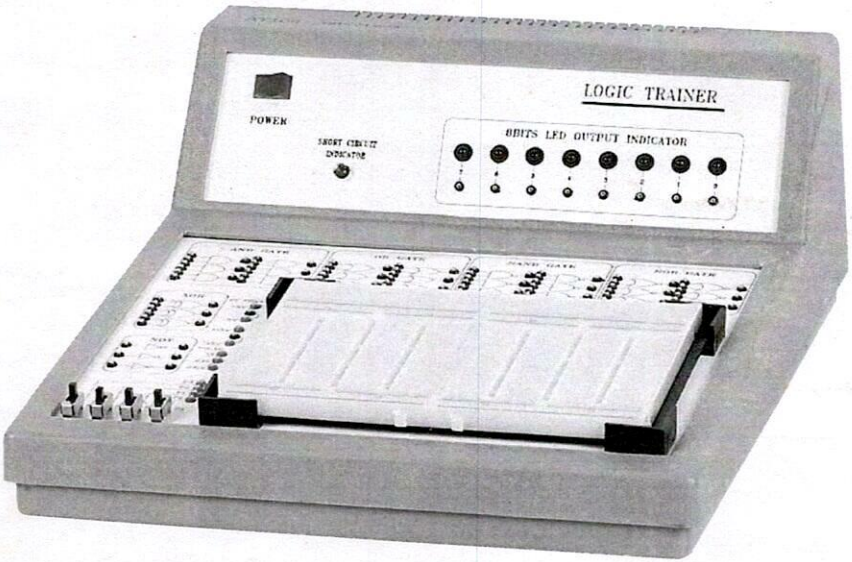
USER'S MANUAL

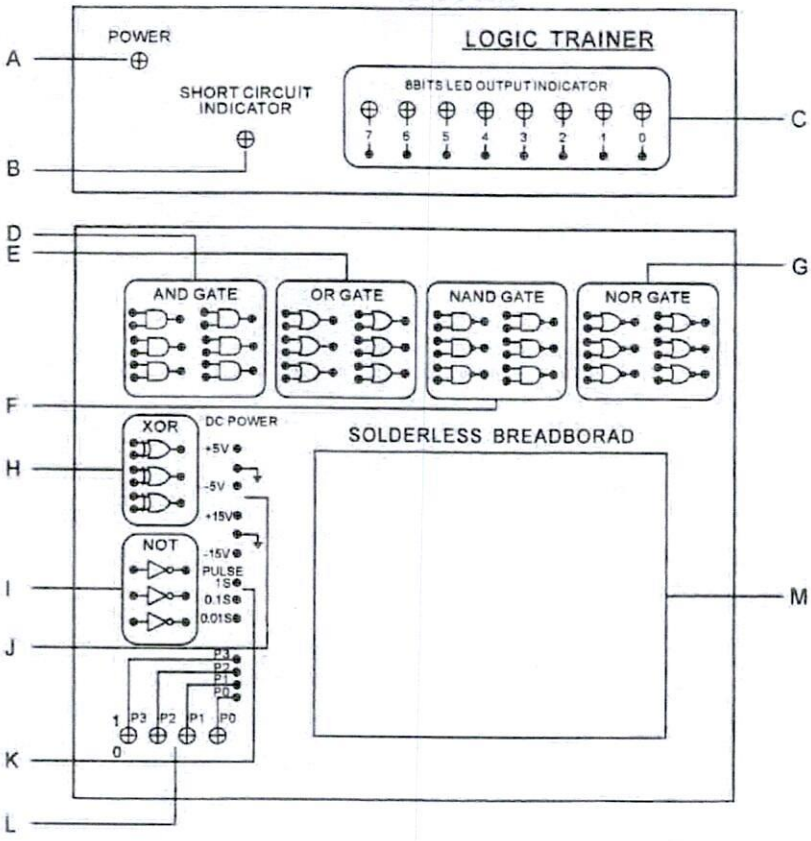


LOGIC TRAINER
REF. AT104

INDEX

WARNING

While operating the **AT104** under the low temperature and dry climate environment, please use the Anti-static Ring(AS-03A) to avoid any damage by electrostatic discharge. (Wear the band on your wrist, and connect the clip to the ground)


LOGIC TRAINER
POWER
SHORT CIRCUIT INDICATOR
8BITS LED OUTPUT INDICATOR
7 6 5 4 3 2 1 0
A
B
C
D
E
F
G
H
I
J
K
L
M
AND GATE
OR GATE
NAND GATE
NOR GATE
XOR
NOT
DC POWER
+5V
-5V
+15V
-15V
PULSE
1S
0.1S
0.01S
P3
P2
P1
P0
1
0
SOLDERLESS BREADBORAD

A- POWER SW. (ON/OFF)

B- SHORT CIRCUIT INDICATOR LED

C- 8 BITS LED OUTPUT INDICATOR

D- AND GATE UNIT

E- OR GATE UNIT

F- NAND GATE UNIT

G- NOR GATE UNIT

H- XOR GATE UNIT

I- NOT GATE UNIT

J- DC POWER SUPPLY

K- PULSE GENERATOR

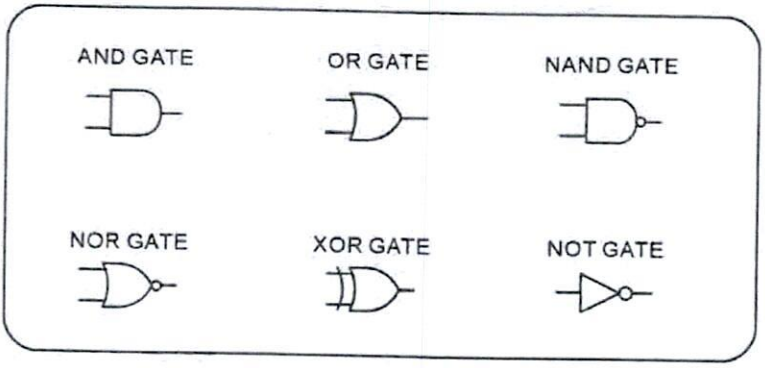
L- DEBUNCED LOGIC SW

M- SOLDERLESS BREADBOARD

SPECIFICATION

1. LOGIC GATE UNIT:

AND GATE × 6 sets, OR GATE × 6 sets, NAND GATE × 6 sets,
NOR GATE × 6 sets, XOR GATE × 3 sets, NOT GATE × 3 sets.
INPUT VOLTAGE OF HI LEVEL ≥ 2.25V
INPUT VOLTAGE OF LO LEVEL ≤ 0.8V



2. DC POWER SUPPLY:

All of the 4 sets of power supply are equipped with short circuit protection and indicator.

OUTPUT VOLTAGE	+5V/±0.25V	-5V/±0.25V
MAX. OUTPUT CURRENT	1A	500mA
LINE REGULATION	50mV	25mV
LOAD REGULATION	100mV	30mV

OUTPUT VOLTAGE	+15V/±0.75V	-15V/±0.75V
MAX. OUTPUT CURRENT	500mA	500mA
LINE REGULATION	150mV	150mV
LOAD REGULATION	150mV	150mV

3. AD-200 SOLDERLESS BREADBOARD:

Interconnected nickel plated 1896 tie points, fitting all DIP sizes and all components with lead and solid wire AWG#22-30(0.3~0.8mm).

When user has finished the experiment in manual,

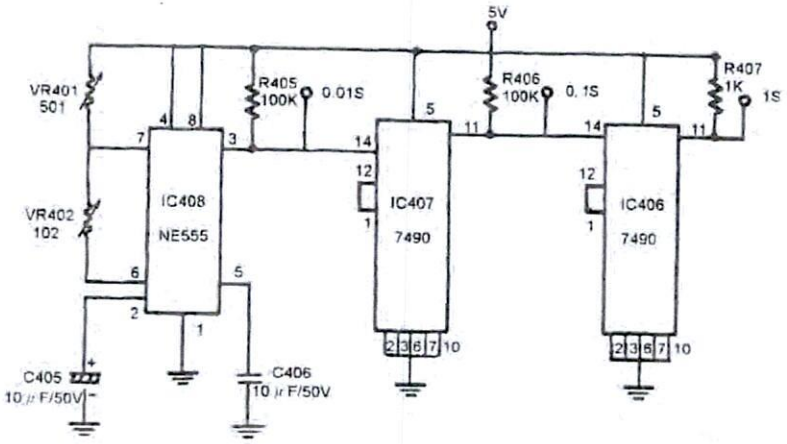
he can learn more practicle logic circuit or even his own design!

In that case, the breadboard offer him a right tool to complete the whole circuit.

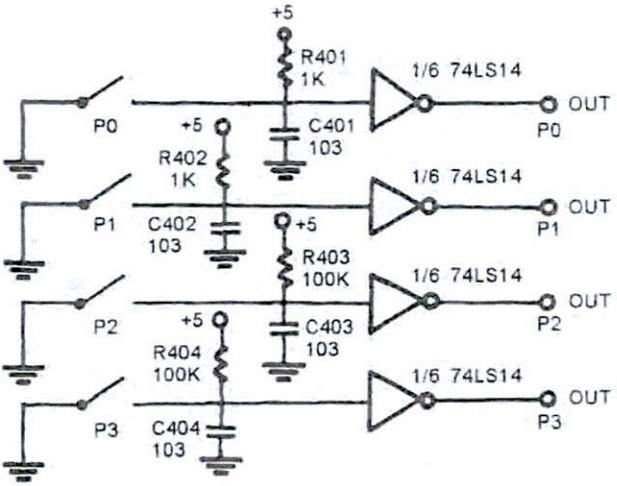
4. PULSE GENERATOR:

3 kinds of time interval: 1 sec., 0.1 sec., 0.01 sec.

Output voltage: +5V

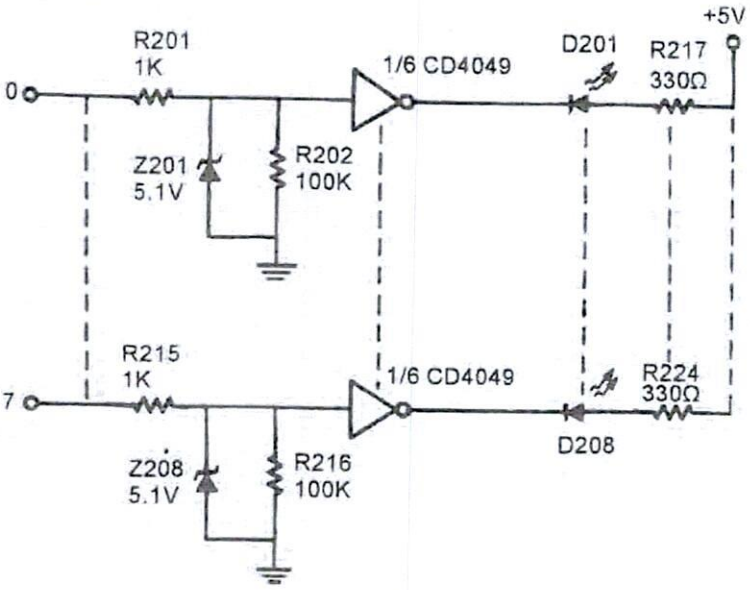


5. DEBUNCED LOGIC SW.(HI/LO)



6. 8 BITS LED OUTPUT INDICATOR:

Each LED indicator is equipped with buffer, the max. input voltage 15V DC.



CIRCUIT DIAGRAM

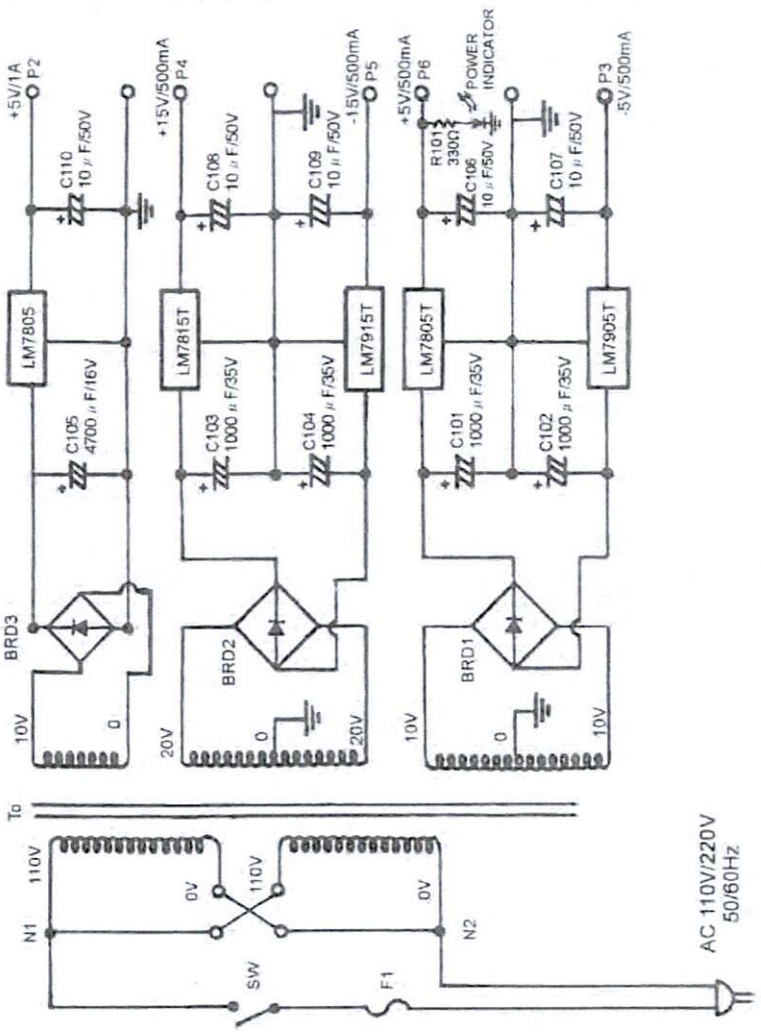


Fig. 3-1 POWER SUPPLY CIRCUIT

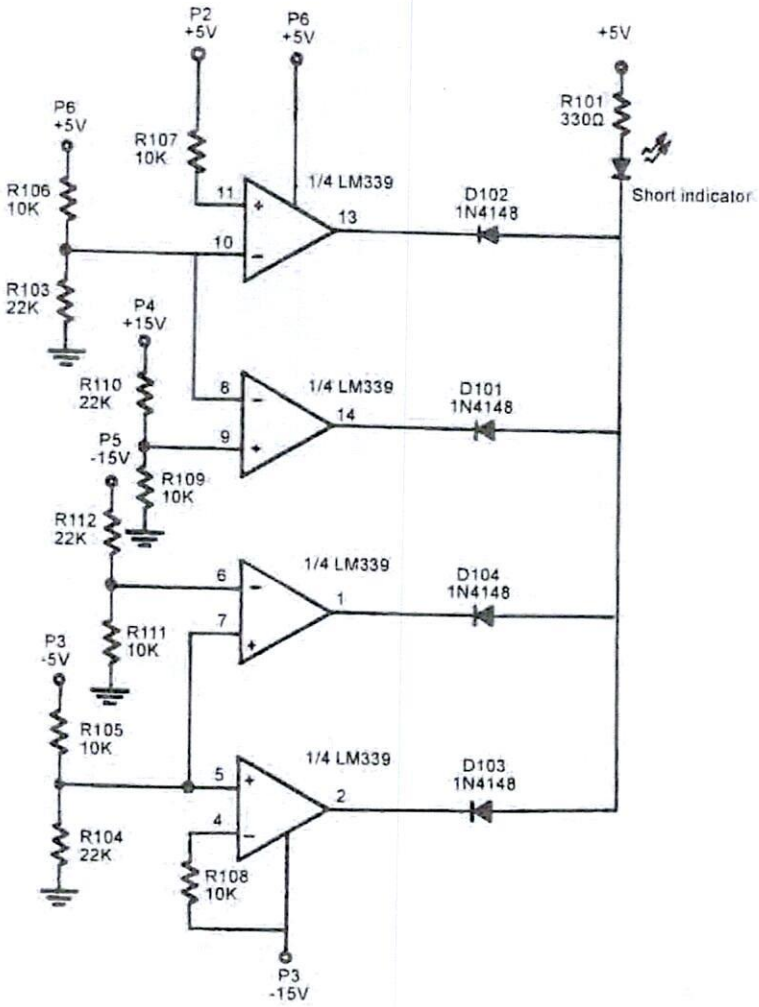
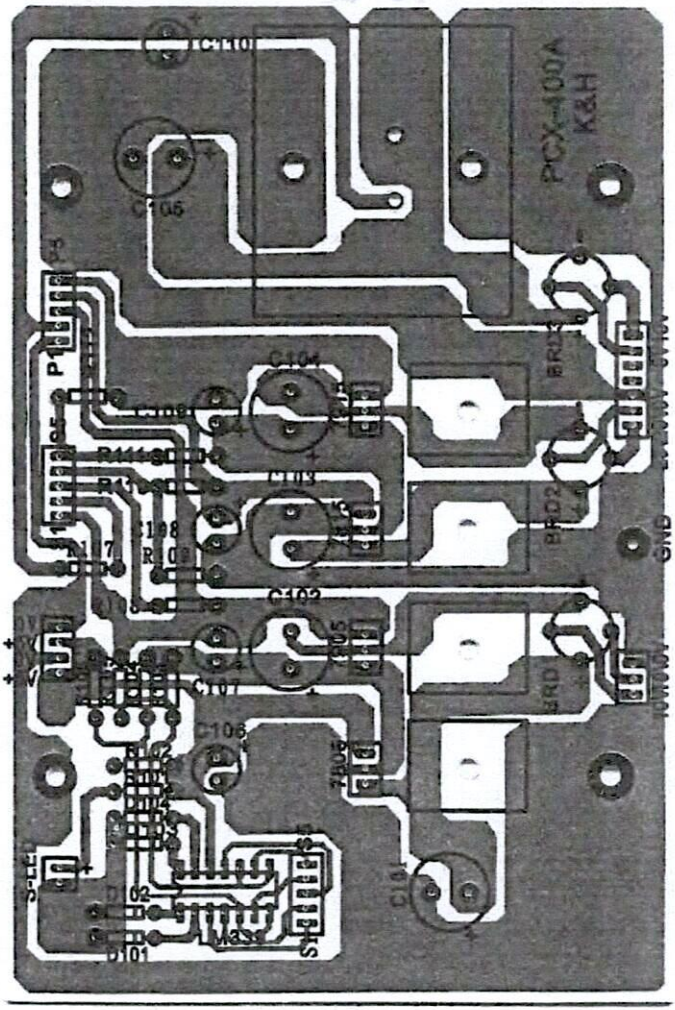


Fig. 3-2 Short circuit indicator circuit

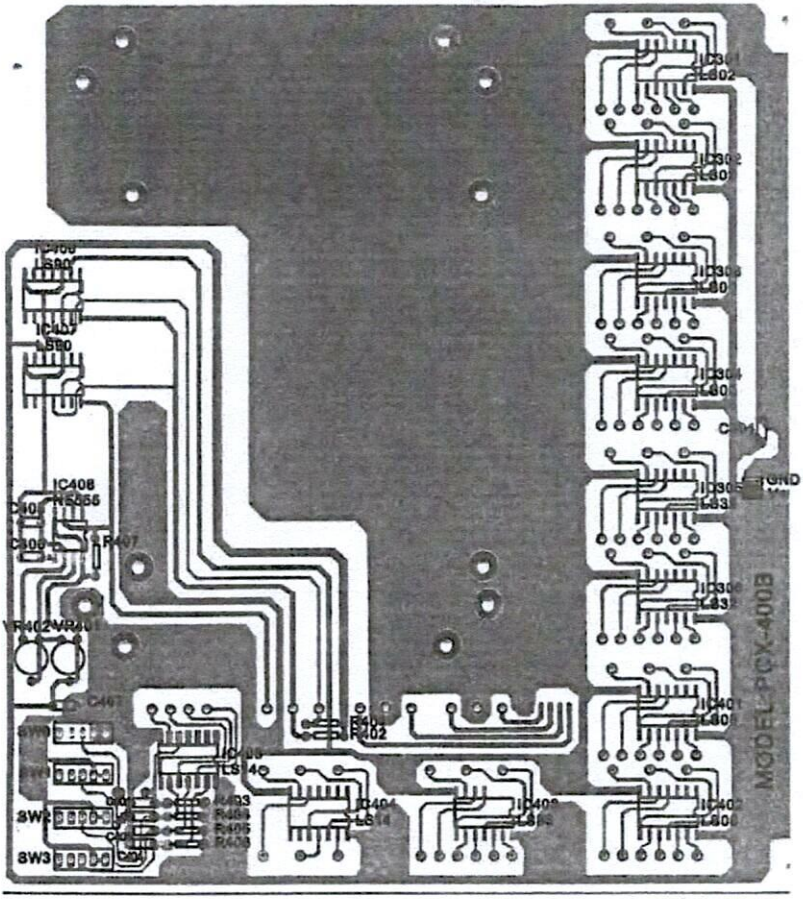
PC BOARD DIAGRAM & PARTS LIST



Power Supply P.C.B

PCX-400A PARTS LIST

SYMBOL	MODEL	DESCRIPTION
To		Transformer N: 110V/220V(50Hz/60Hz) S: 20V,0,20V(0.5A) 10V,0,10V(0.5A) 10V,0(1A)
BRD1,BRD 2,BRD3	W02	Bridge rectifier diode 220PIV(1A)
LM7805	LM7805	+5V Voltage regulator
LM7805T	LM7805T	+5V Voltage regulator
LM7905T	LM7905T	-5V Voltage regulator
LM7815T	LM7815T	+15V Voltage regulator
LM7915T	LM7915T	-15V Voltage regulator
IC101	LM339	Quadruple differential comparators
D101,D102, D103,D104	1N4148	Silicon rectifier diode
R101	330 Ω 1/4W	
R103,R104	22K Ω 1/4W	
R105,R106, R107,R108, R109	10K Ω 1/4W	
R110	22K Ω 1/4W	
R111	10K Ω 1/4W	
R112	22K Ω 1/4W	
C101,C102, C103,C104		Capacitor 1000 μ F/35V
C105		Capacitor 4700 μ F/16V
C106,C107, C108,C109, C110		Capacitor 10 μ F/50V



Basic Logic Gates and Pulse Generator P.C.B.

PCX-400B PARTS LIST

SYMBOL	MODEL	DESCRIPTION
IC301,IC302	74LS02	NOR GATE
IC303,IC304	74LS00	NAND GATE
IC305,IC306	74LS32	OR GATE
VR401	500Ω	
VR402	1KΩ	
IC401,IC402	74LS08	AND GATE
IC403	74LS86	XOR GATE
IC404,IC405	74LS14	NOT GATE
IC408	NE555	
IC407,IC406	74LS90	DECADE COUNTERS
R403,R404,R405,R406	100KΩ1/4W	
R401,R402,R407	1KΩ1/4W	
C401,C402,C403,C404 C407,C301		Capacitor 0.01 μF
C405,C406		Capacitor 10 μF /50V

PCX-400B PARTS LIST

SYMBOL	MODEL	DESCRIPTION
IC301,IC302	74LS02	NOR GATE
IC303,IC304	74LS00	NAND GATE
IC305,IC306	74LS32	OR GATE
VR401	500Ω	
VR402	1KΩ	
IC401,IC402	74LS08	AND GATE
IC403	74LS86	XOR GATE
IC404,IC405	74LS14	NOT GATE
IC408	NE555	
IC407,IC406	74LS90	DECADE COUNTERS
R403,R404,R405,R406	100KΩ1/4W	
R401,R402,R407	1KΩ1/4W	
C401,C402,C403,C404 C407,C301		Capacitor 0.01 μ F
C405,C406		Capacitor 10 μ F /50V

PCX-400C PARTS LIST

SYMBOL	MODEL	DESCRIPTION
D201,D202,D203, D204,D205,D206, D207,D208		5øR LED
IC201,IC202	CD4049	INVERTER
Z201,Z202,Z203, Z204,Z205,Z206, Z207,Z208		Zener diode: 5.1V 1/2W
R201,R203,R205, R207,R209,R211, R213,R215	1KΩ 1/4W	
R202,R204,R206, R208,R210,R212, R214,R216	100KΩ 1/4W	
R217,R218,R219, R220,R221,R222, R223,R224	300Ω 1/4W	
C201		Capacitor 0.01 μF

EXPERIMENT

A. THE PURPOSES OF THIS PROCEDURE:

1. To understand basic function of the logical gate.
2. To understand the control feature of the logical gate.

B. PRACTICE PROCEDURES AND RECORDS:

Item 1. AND GATE EXPERIMENT

Step 1:

Fig. 1-1(a) is basic AND GATE logical symble

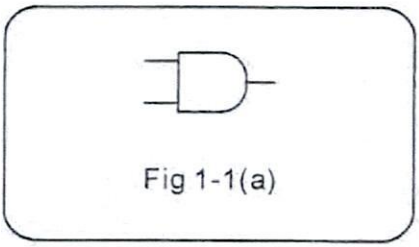


Fig 1-1(a)

Step 2:

Connect the INPUT "A", "B" to the logical switch P2, P3, connects the OUTPUT "Y" to LED display "0" as Fig. 1-1(b) circuit.

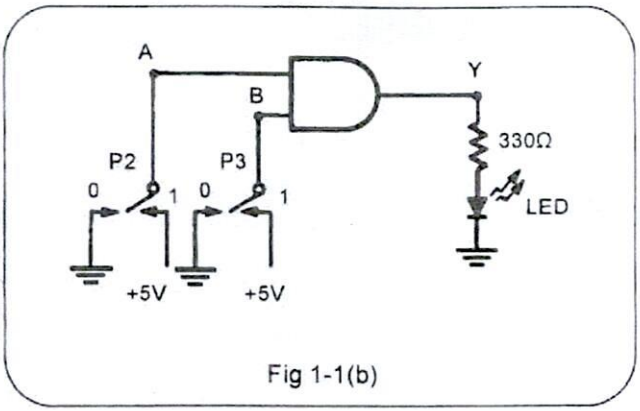


Fig 1-1(b)

Step 3:

Change both of the logical switch P2, P3 from "0", to "1" and back to "0", then observe the INPUT and OUTPUT situation, record them in Fig. 1-1(c) truth table.

Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

$Y=A \bullet B$

Fig 1-1(c)

Item 2. OR GATE EXPERIMENT

Step 1:

Fig. 2-1(a) is basic OR GATE logical symble.

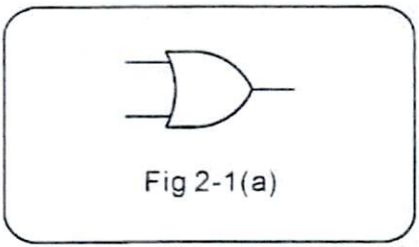


Fig 2-1(a)

Step 2:

Connect the INPUT "A", "B" to logical switch P2, P3, connect the OUTPUT "Y" to LED display "0" as Fig. 2-1(b) circuit.

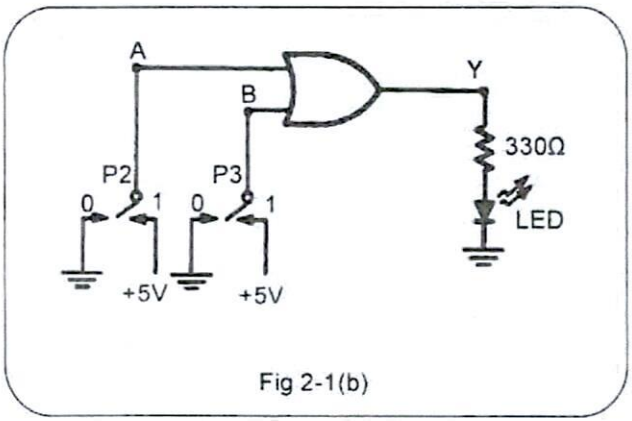


Fig 2-1(b)

Step 3:

Change both of the logical switch P2, P3 from "0" to "1" and back to "0", then observe the INPUT and OUTPUT situation record them in Fig. 2-1(c) truth table.

Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

Y=A+B

Fig 2-1(c)

Item 3. NOT GATE EXPERIMENT

Step 1:

Fig. 3-1(a) is basic NOT GATE logical symble.

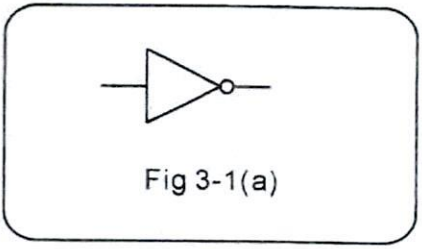


Fig 3-1(a)

Step 2:

Connect the INPUT "A" to logical switch P3, connect the OUTPUT "Y" to LED display as Fig. 3-1(b) circuit.

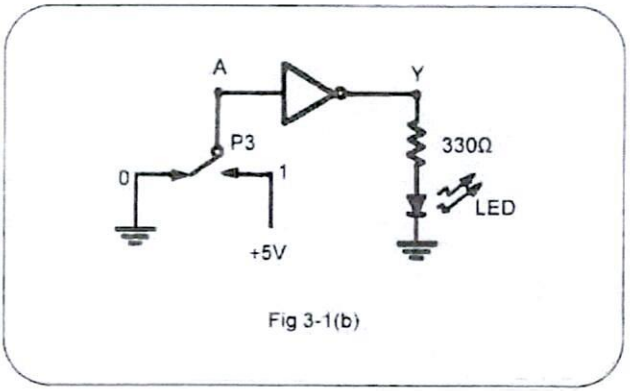


Fig 3-1(b)

Step 3:

Change the logical switch P3 from "0" to "1" and back to "0", observe the INPUT and OUTPUT situation, record them in Fig. 3-1(c) truth table.

Truth Table

A	Y
1	
0	

$Y = \overline{A}$

$Y = A \oplus B$

Fig 3-1(c)

Item 4. NAND GATE EXPERIMENT

Step 1:

Fig. 4-1(a) is basic NAND GATE logical symble.

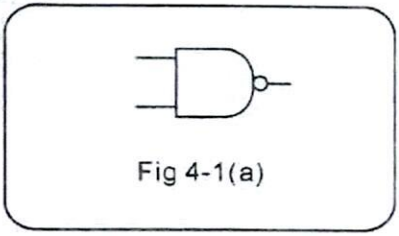


Fig 4-1(a)

Step 2:

Connect the INPUT "A", "B" to logical switch P2, P3, connect the OUTPUT "Y" to LED display, as Fig. 4-1(b) circuit.

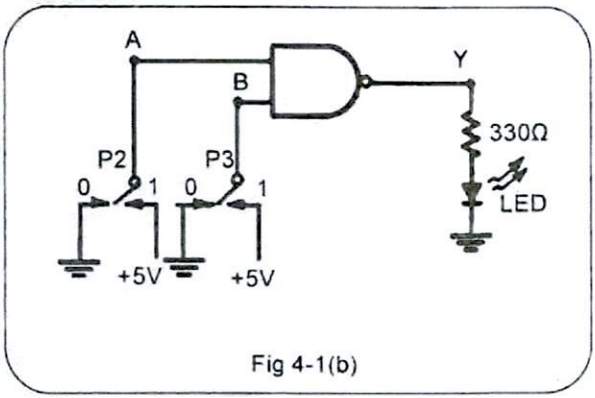


Fig 4-1(b)

Step 3:

Change both of the logical switch P2, P3 from "0" to "1" and back to "0", then observe the INPUT and OUTPUT situation record them in Fig. 4-1(c) truth table.

Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

$Y=\overline{A \bullet B}$

Fig 4-1(c)

Item 5. NOR GATE EXPERIMENT

Step1:

Fig. 5-1(a) is basic NOR GATE logical symble.

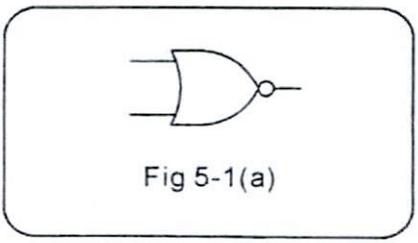


Fig 5-1(a)

Step 2:

Connect the INPUT "A", "B" to logical switch P2, P3 connect the OUTPUT "Y" to LED display as Fig. 5-1(b) circuit.

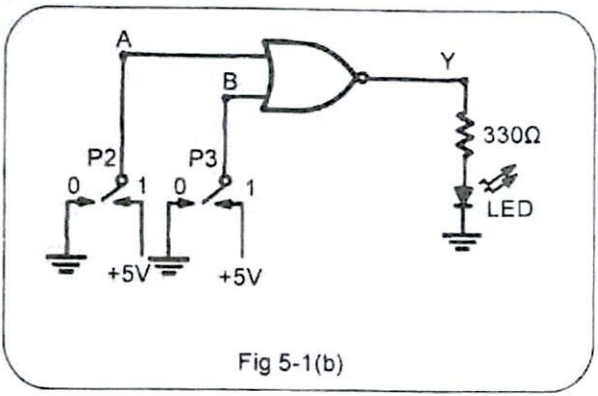


Fig 5-1(b)

Step 3:

Change both of the logical switch P2, P3 from "0" to "1" and back to "0", then observe the INPUT and OUTPUT situation, record them in Fig. 5-1(c) truth table.

Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

$Y=\overline{A+B}$

Fig 5-1(c)

Item 6. EXCLUSIVE – OR GATE EXPERIMENT

Step 1:

Fig. 6-1(a) is basic EXCLUSIVE – OR GATE logical symble.

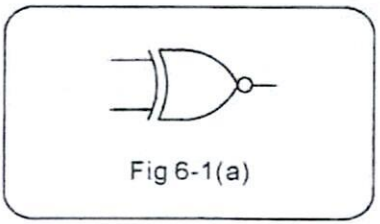


Fig 6-1(a)

Step 2:

Connect the INPUT "A", "B" to logical switch P2, P3, connect the OUTPUT "Y" to LED display, as Fig. 6-1(b) circuit.

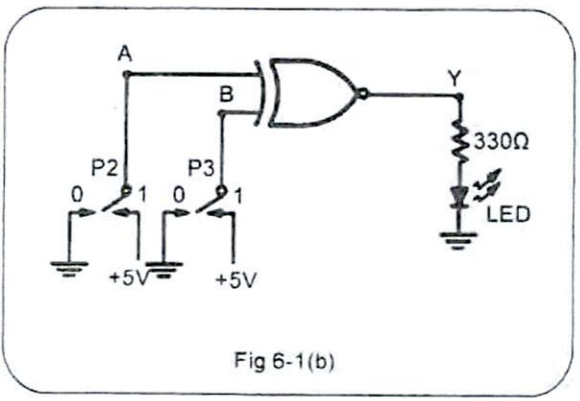


Fig 6-1(b)

Step 3:

Change both of the logical switch P2, P3 from "0" to "1" and back to "0", then observe the INPUT and OUTPUT situation, record them in Fig. 6-1(c) truth table.

Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

$Y=A \oplus B$

Fig 6-1(c)

Item 7. HALF ADDER

Step 1:

Fig. 7-1(a) is a HALF ADDER consist of AND/OR and NOT GATE circuit.

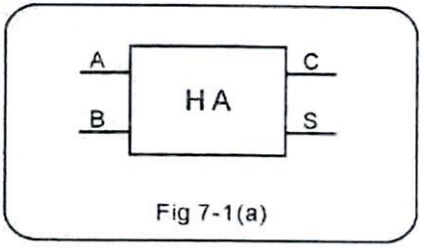


Fig 7-1(a)

Step 2:

Connect the INPUT "A", "B" to logical switch P0, P1, connect OUTPUT 1 "C" to LED(1) display, connect OUTPUT 2 "S" to LED(2) display, as Fig. 7-1(b) circuit.

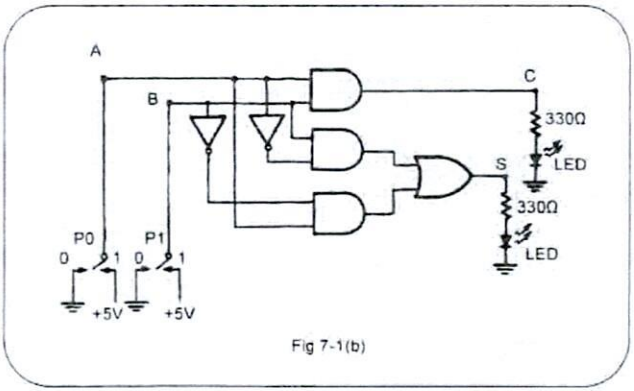


Fig 7-1(b)

Step 3:

Change both of the logical switch P0, P1 form "0" to "1" and back to "0", then observe the INPUT and OUTPUT 1, OUTPUT 2 situation, record them in Fig. 7-1(c) truth table.

Truth Table

A	B	S	C
0	0		
0	1		
1	0		
1	1		

$S=AB+AB=A\oplus B$
$C=A\bullet B$

Fig 7-1(c)

Item 8: COMPARATOR

Step 1:

Fig. 8-1(a) is a COMPARATOR consist of AND/NOR and NOT GATE circuit.

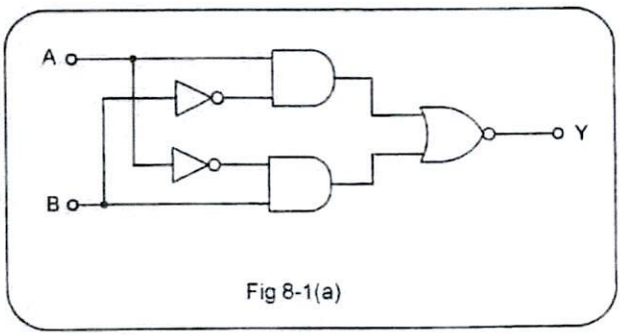


Fig 8-1(a)

Step 2:

Connect INPUT "A", "B" to logical switch P0, P1, connect OUTPUT "Y" to LED display, as Fig. 8-1(b) circuit.

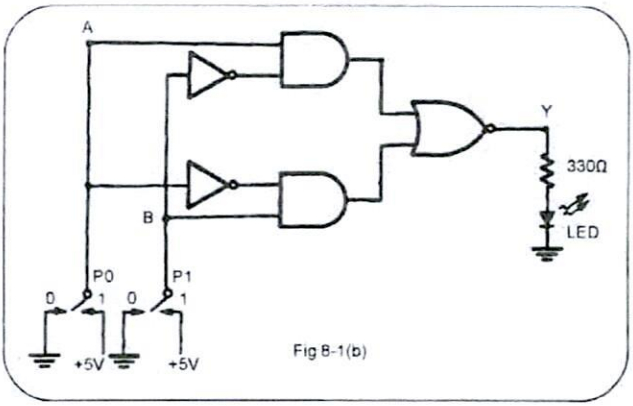


Fig 8-1(b)

Step 3:

Change both of the logical switch P0, P1 from "0" to "1" and back to "0", then observe INPUT and OUTPUT situation, record them in Fig. 8-1(c) truth table.

Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

Y:A=B

Fig 8-1(c)

Item 9: R-S CLOCKED FLIP FLOP

Step 1:

Fig. 9-1(a) is basic R-S clocked Flip Flop logical symble.

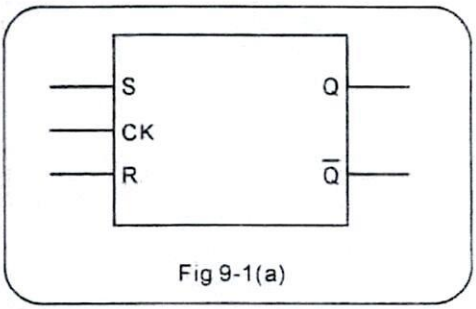


Fig 9-1(a)

Step 2:

Fig. 9-1(b) is a basic R-S Clocked Flip Flop consist of four NAND GATE circuit.

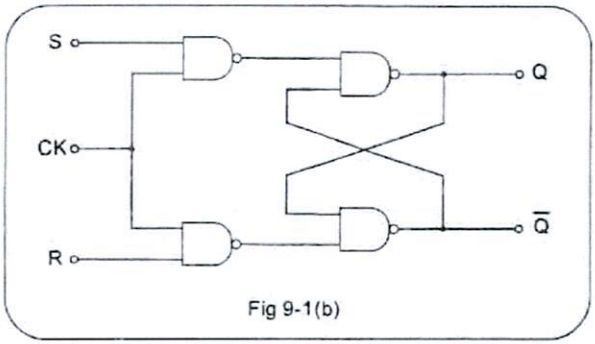


Fig 9-1(b)

Step 3:

Connect input "R", "S", "CK", to the logical switch, P3, P2, P1 connect OUTPUT "Q" to the LED(1) display, connect OUTPUT "$\overline{Q}$" to the LED(2) display, as Fig. 9-1(c) circuit.

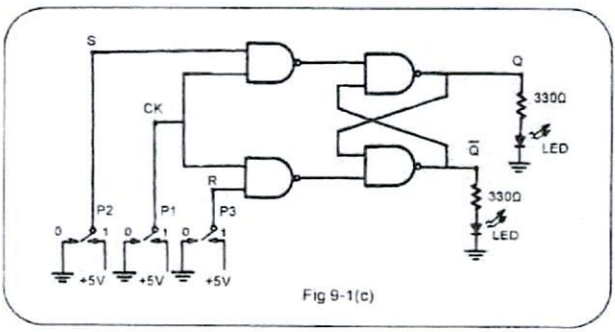


Fig 9-1(c)

Step 4:

Change both of the logical switch P3, P2, P1 from "0" to "1" and back to "0", then observe INPUT and OUTPUT "Q", OUTPUT "$\overline{Q}$" situation, record them in Fig. 9-1(d) truth table.

Truth Table

R	S	Q	$\overline{Q}$
0	1		
0	0		
1	0		
0	0		
1	1		

Fig 9-1(d)

Item 10: D FLIP FLOP

Step 1:

Fig. 10-1(a) is basic D Flip Flop symble.

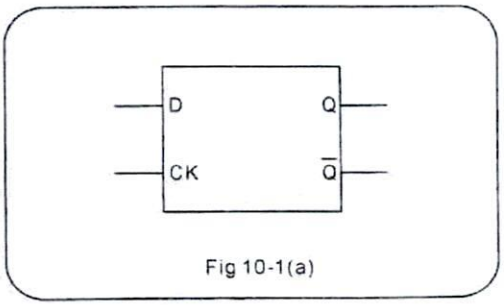


Fig 10-1(a)

Step 2:

Fig. 10-1(b) is a D Flip Flop consist of four NAND GATE and NOT GATE circuit.

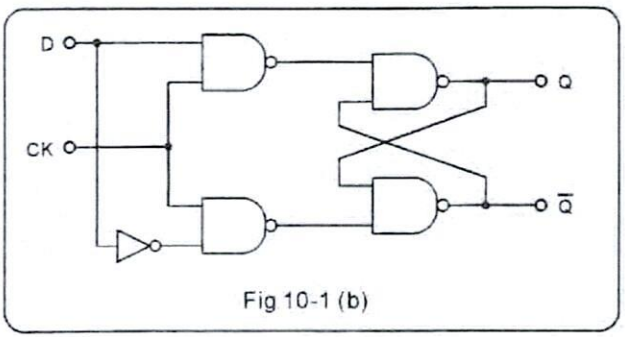


Fig 10-1 (b)

Step 3:

Connect INPUT "D", "CK" to the logical switch P2, P3, connect the OUTPUT "Q" to the LED(1) display, connect the OUTPUT "$\overline{Q}$" to the LED(2) display, as Fig. 10-1(c) circuit.

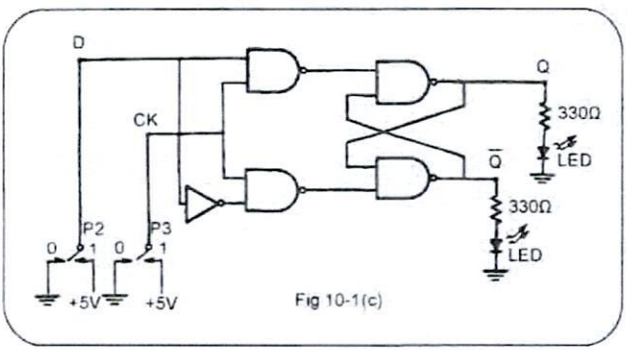


Fig 10-1(c)

Step 4:

Change both of the logical switch P2, P3 from "0" to "1" and back to "0", then observe INPUT and OUTPUT "Q", OUTPUT "$\overline{Q}$", situation, record them in Fig. 10-1(d) truth table.

Truth Table

D	Q	$\overline{Q}$
0		
1		

Fig 10-1(d)