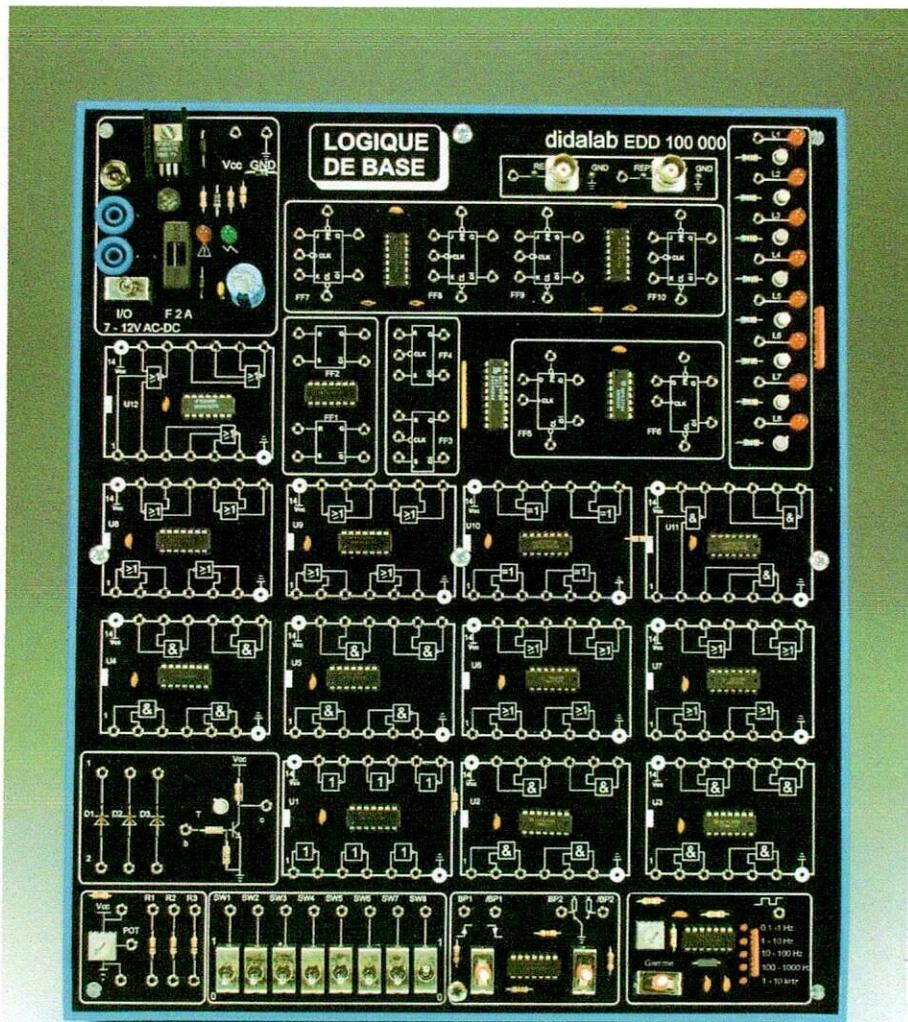


# BASIC LOGIC

## EDD 100 000



### *Technical Guide*



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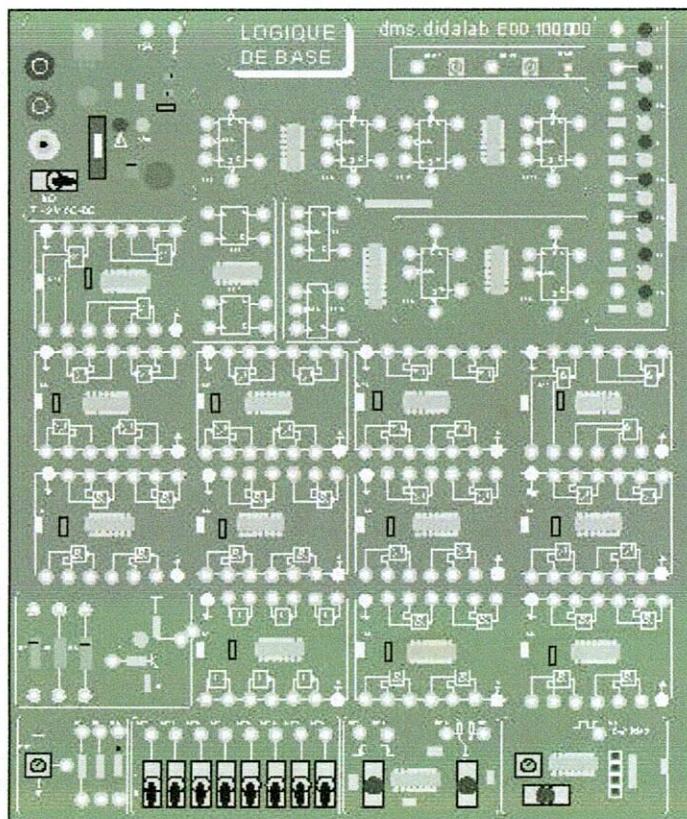
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## Presentation

The basic logic module (reference : EDD 100 000) is a module which allow the study of the main circuits in basic logic.

In the combinatory logic part, the module presents the pins connections of the integrated circuits (as manufacturers'datasheet) ; in the sequential logic, the user has got the flip-flop diagram.



The module includes :

- Power supply block, protected against voltage peaks and short-circuits,
- 8 On/Off generators,
- 1 push-button, bounce free, 1 push-button, to be connected,
- 1 adjustable clock 0,1 Hz à 10 kHz,
- 8 display leds,
- 3 resistances and 1 potentiometer,
- 3 diodes and 1 transistor,
- 6 NO,
- 8 AND with 2 inputs,
- 8 NAND with 2 inputs and 3 with 3 inputs,
- 8 OR with 2 inputs,
- 8 NOR with 2 inputs and 3 with 3 inputs,
- 4 XOR with 2 inputs.
- 2 RS and 2 RSH flip-flops,
- 2 D flip-flops,
- 4 JK flip-flops,
- 2 BNC Ø2-mm adaptators.

# 1 Use

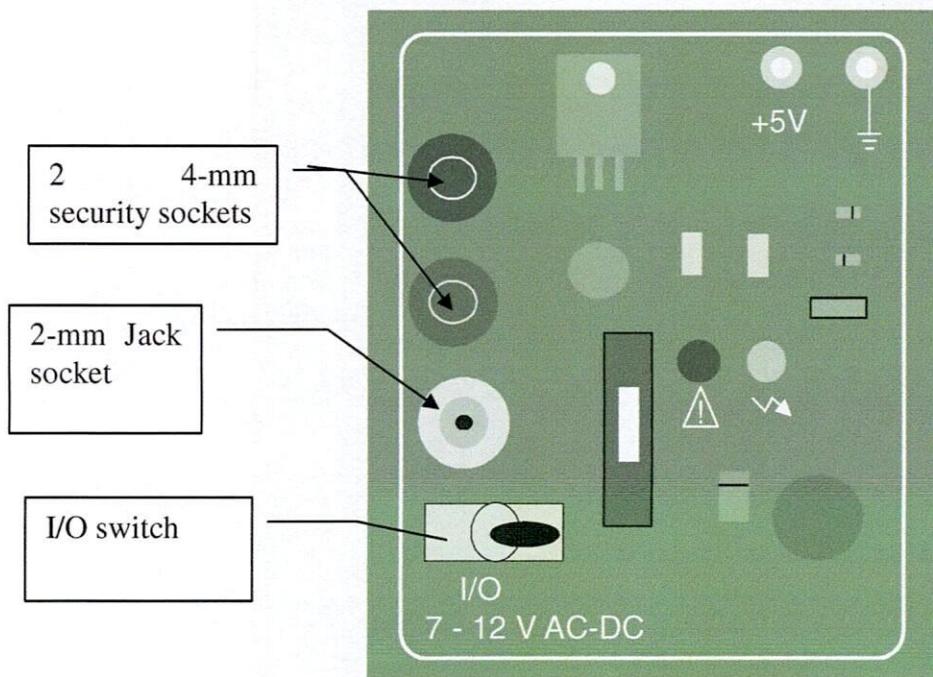
## 1.1 Câblage de l'alimentation

The module can be supplied either with a dc voltage or a ac voltage between 7 et 12 V.

There is 2 possibilities :

Using the 2-mm Jack connector

Using 2 Ø 4-mm security cords.



A **I/O** switch for switching On/Off the module.

When the module is swithched on, a green led is lit ; the red led is lit when there is a short-circuit.

## 1.2 Connecting the function-blocks

To connect the different function block, you have to use the Ø 2-mm cords.

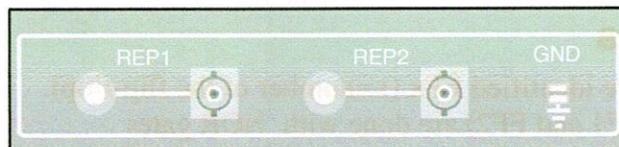
 During the connections of the blocks, the module must be switched off.

## 1.3 Connection of the measuring instruments

To use the measuring instruments (oscilloscope, frequency meter, ...), you have 2 Ø 2-mm / BNC adaptors and test-clips.

BNC shell is connected to the ground.

They are : **REP1** and **REP2**.

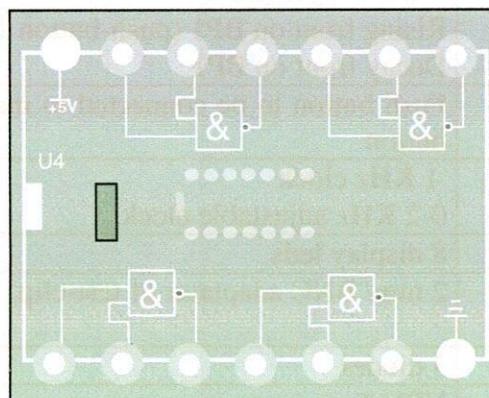


## 2 Location of the components

### 2.1 Sequential logic

They are noted **Ux** where **x** is the component number.

The pins 1 and 14 are identified. For the other pins of the component, the pin connection is as the over-view of the DIP socket.



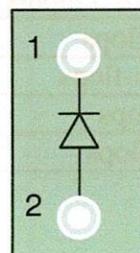
The pin for the power-supply are identified but cannot be accessed.

### 2.2 Functions : POT, R, D and T

The socket **POT** is connected to the middle point of the potentiometer.

The 3 resistances are identified **R1**, **R2**, et **R3**.

For the diodes **Dx** ( $x=\{1,2,3\}$ ), the pin 1 is connected to the cathode, the pin 2 to the anode :



For the transistor **T** (NPN kind), the socket **b** is on the base and the socket **c** on the transistor's collector.

## 2.3 Display Led

There are 8 display leds (**L1** to **L8**).

The LEDs are controlled with a NPN transistor setting.

## 2.4 Flip-flops

The flip-flops are identified **FFx** (x=number of the flip-flop).

RS flip-flops (FF1 and FF2) are done with NOR gates

RSH (FF2 and FF3) flip-flops are done with a PAL 16V8.

## 2.5 List of components

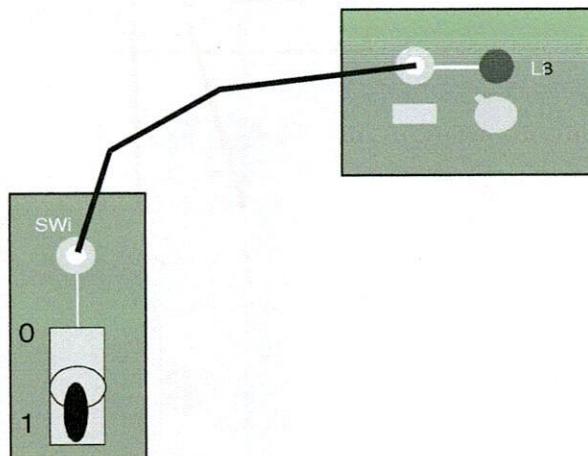
Identification	Description
<b>POT</b>	Potentiometer
<b>R1, R2, R3</b>	Resistances
<b>SW1 to SW8</b>	8 On/Off generator
<b>BP1 /BP1</b>	Rising front on BP1 (push-button 1) Decay front on BP1
<b>BP2 /BP2</b>	Push button to be connected to make a no-bounce free push-button
<b>H1</b>	1 KHz clock
<b>H2</b>	0-2 KHz adjustable clock
<b>L1 to L8</b>	8 display leds
<b>REP1</b>	2 mm/ BNC adaptator of test-clip
<b>REP2</b>	
<b>D1 to D3</b>	3 diodes
<b>T</b>	NPN Transistor
<b>U1</b>	6 NON
<b>U2, U3</b>	4 AND with 2 inputs
<b>U4, U5</b>	4 NAND with 2 inputs
<b>U6, U7</b>	4 OU with 2 inputs
<b>U8, U9</b>	4 NOR with 2 inputs s
<b>U10</b>	4 XOR with 2 inputs
<b>U11</b>	3 NAND with 3 inputs
<b>U12</b>	3 NOR with 3 inputs
<b>FF1, FF2</b>	2 RS flip-flops
<b>FF3, FF4</b>	2 RSH flip-flops
<b>FF5, FF6</b>	2 D flip-flops
<b>FF7 to FF10</b>	4 JK flip-flops

### 3 Test and description of the functions

For the tests, you'll need a voltmeter and an oscilloscope.

#### 3.1 Test of the 1/0 generators and display leds

You have to connect the outputs of the SW<sub>i</sub> generators to the inputs Li (i={1...8}) with Ø 2-mm cords.



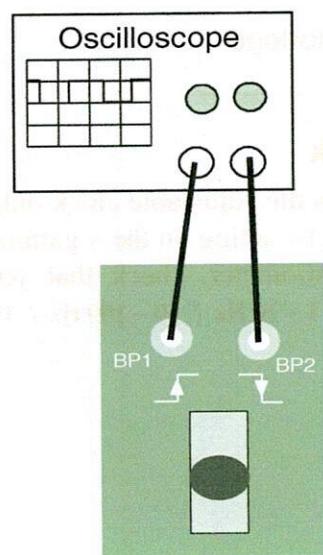
Check that :

State of the key-generator	LED
0	Not lit
1	Lit

#### 3.2 Test of the bounce free

##### 3.2.1 Test of the 1st bounce-free push button

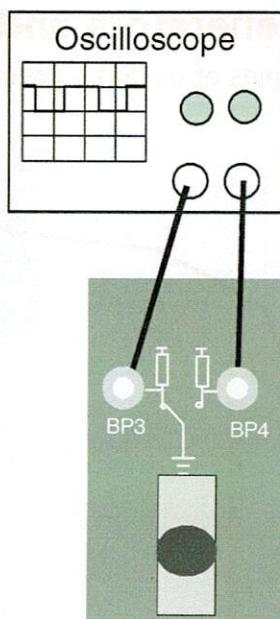
Make the following setting :



Check that the signal BP1 goes to 1 when you act on the push-button and that BP2 goes to 1 when you release the push-button.

### 3.2.2 Test of the push-button to be connected

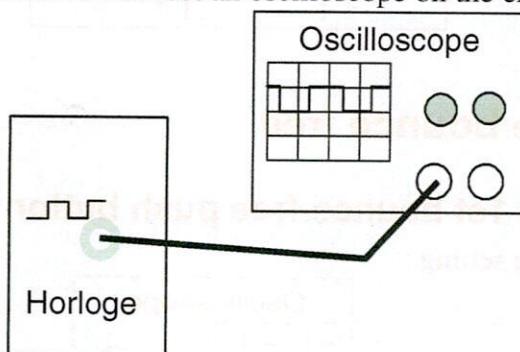
Make the following setting :



Check that BP3 and BP4 are complementary, whatever the state of the push-button.

### 3.3 Test of the clocks

To test the clocks, you have to connect an oscilloscope on the clock output:



#### 3.3.1 Adjustable clock

Connect an oscilloscope on the adjustable clock output.

Select the frequency range by acting on the « gamme » puh-button.

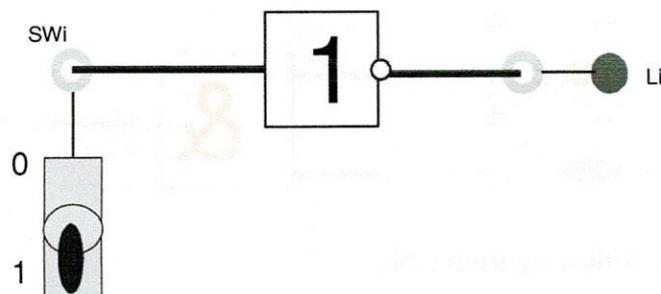
When you turn the potentiometer, check that you are setting the frequency in the selected range ( 0.1 – 1Hz / 1 – 10 Hz / 10 – 100 Hz / 100 – 1000Hz / 1 – 10 kHz ).

## 3.4 Test of the combinatory logic gates

### 3.4.1 NO gate

NO gates are realised with 7404 component.

To test the NO gate, make the following setting :



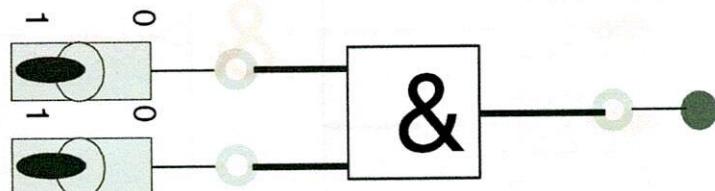
Then check the following truth table:

State of the key generator	State of the output	LED
0	1	Lit
1	0	Light off

### 3.4.2 AND gate

AND gates are realised with 7408 component.

Make the following setting



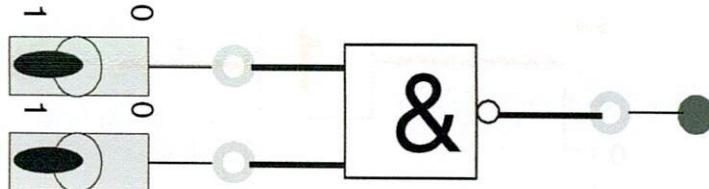
Then check the following truth table:

SW1	SW2	State of the output	LED
0	0	0	Light off
0	1	0	Light off
1	0	0	Light off
1	1	1	Lit

### 3.4.3 Cellule NAND

NAND gates are realised with 7400 component for the 2 inputs and 7410 components for the 3 inputs.

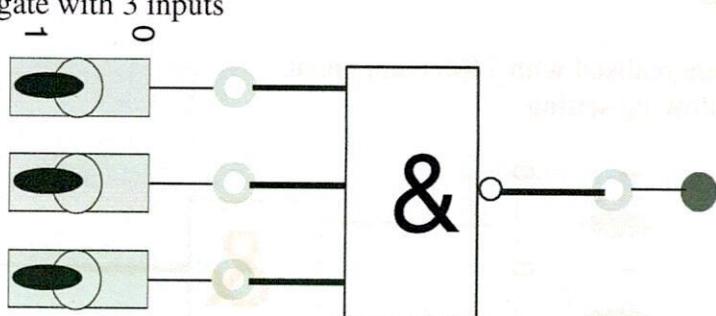
Test of NAND gate with 2 inputs



Then check the following truth table:

SW1	SW2	State of the ouput	LED
0	0	1	Lit
0	1	1	Lit
1	0	1	Lit
1	1	0	Light off

Test of NAND gate with 3 inputs



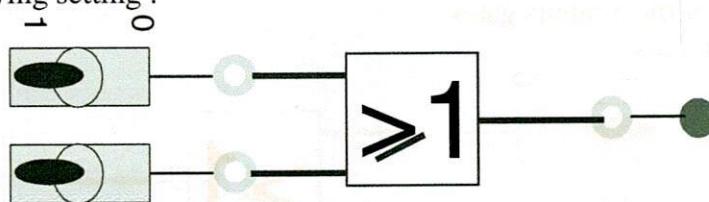
Truth table:

SW1	SW2	SW3	State of the ouput	LED
0	0	0	1	Lit
0	0	1	1	Lit
0	1	0	1	Lit
0	1	1	1	Lit
1	0	0	1	Lit
1	0	1	1	Lit
1	1	0	1	Lit
1	1	1	0	Light off

### 3.4.4 OR gate

OR gates are realised with 7432 component

Make the following setting :



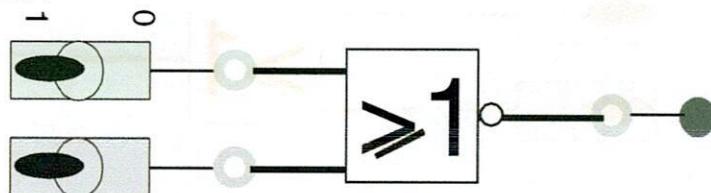
Truth table:

SW1	SW2	State of the output	LED
0	0	0	Light off
0	1	1	Lit
1	0	1	Lit
1	1	1	Lit

### 3.4.5 NOR gate

NOR gates are realised with 7402 component for the 2 inputs and with a 7427 component for the 3 inputs gates

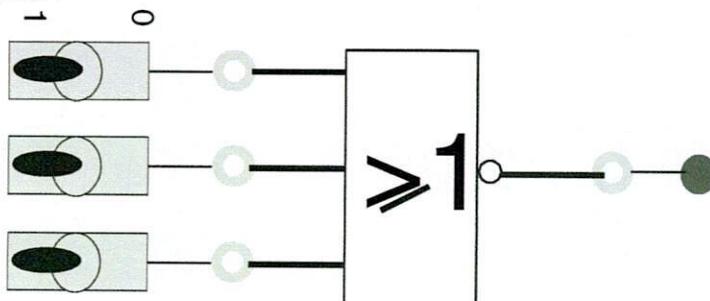
Gate with 2 inputs :



Truth table:

SW1	SW2	State of the ouput	LED
0	0	1	Lit
0	1	0	Light off
1	0	0	Light off
1	1	0	Light off

Gates with 3 inputs :



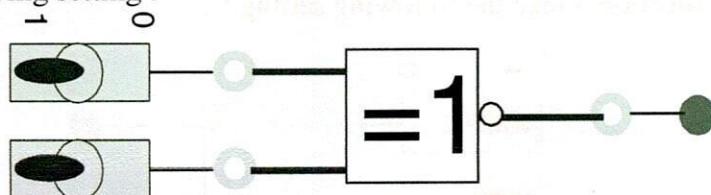
Truth table:

SW1	SW2	SW3	State of the ouput	LED
0	0	0	1	Lit
0	0	1	0	Light off
0	1	0	0	Light off
0	1	1	0	Light off
1	0	0	0	Light off
1	0	1	0	Light off
1	1	0	0	Light off
1	1	1	0	Light off

### 3.4.6 XOR gate

XOR gates are realised with 7486 component

Make the following setting :



Truth table:

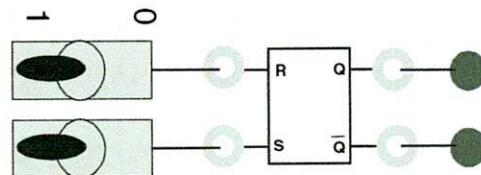
SW1	SW2	State of the output	LED
0	0	0	Light off
0	1	1	Lit
1	0	1	Lit
1	1	0	Light off

## 3.5 Test of the Flip-flops

### 3.5.1 RS Flip-flop

RS flip-flops gates are realised with 2 NOR gates.

To test RS flip-flop, Make the following setting :



Then check the following truth table:

Operating mode	Inputs		Outputs	
	R	S	Q	/Q
Memory state	0	0	Q	/Q
Switch to 0	1	0	0	1
Switch to 1	0	1	1	0
Unknown	1	1	X	X

With :

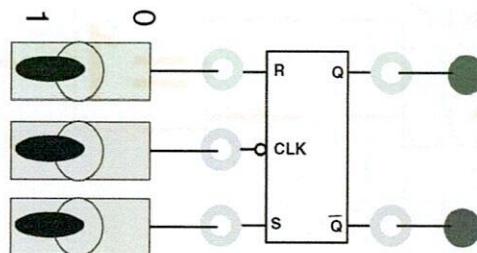
Q/Q : previous state,

X : unknown state (0 or 1).

### 3.5.2 RSH Flip-flop

RSH flip-flops are realised with PAL16V8 component

To test RSH flip-flop, make the following setting :



Then check the following truth table:

Operating mode	Inputs			Outputs	
	CLK	R	S	Q	/Q
Blocked state	1	X	X	Q	/Q
Memory state	0	0	0	Q	/Q
Switch to 0	0	1	0	0	1
Switch to 1	0	0	1	1	0
Unknown	0	1	1	X	X

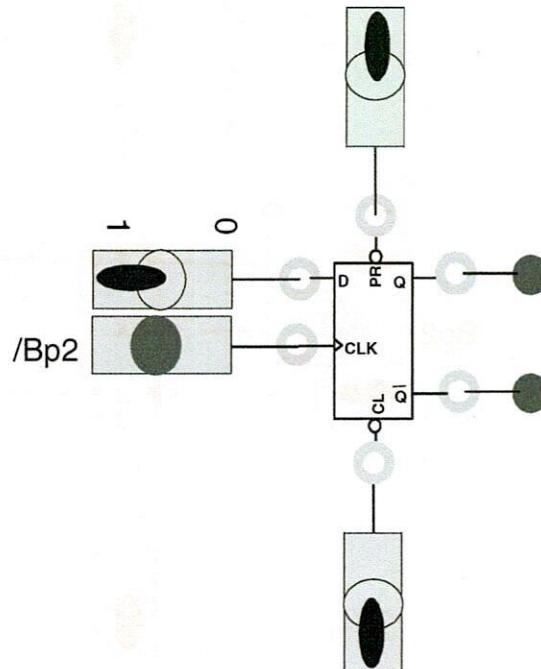
With:

- Q/Q : previous state,
- X : unknown state (0 or 1).

### 3.5.3 D Flip-flop

D flip-flop are realised with 7474 component.

To test D flip-flop, make the following setting :



For the CLK input, you have to use the bounce-free push-button on the decay front. Then check the following truth table:

Operating mode	Inputs			Outputs	
	PR	CL	D	Q	/Q
Set	0	1	X	1	0
Reset	1	0	X	0	1
Unknown	0	0	X	1	1
Switch to 1	1	1	1	1	0
Switch to 0	1	1	0	0	1

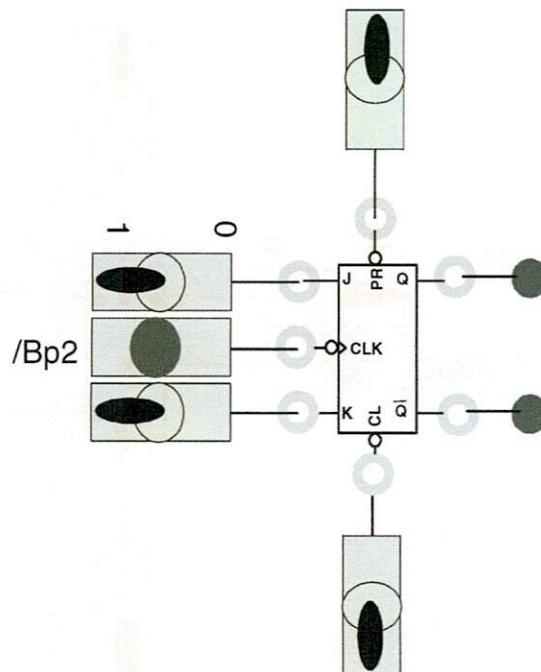
With

X : state 0 or 1.

### 3.5.4 JK Flip-flop

JK flip-flop are realised with 74112 component.

To test JK flip-flop, make the following setting :



For the CLK input, you have to use the bounce-free push-button on the decay front. Then check the following truth table:

Operating mode	Inputs				Outputs	
	PR	CL	J	K	Q	/Q
Set	0	1	X	X	1	0
Reset	1	0	X	X	0	1
Unknown	0	0	X	X	1	1
Switch to 0	1	1	0	1	0	1
Switch to 1	1	1	1	0	1	0
Blocked	1	1	0	0	q	/q

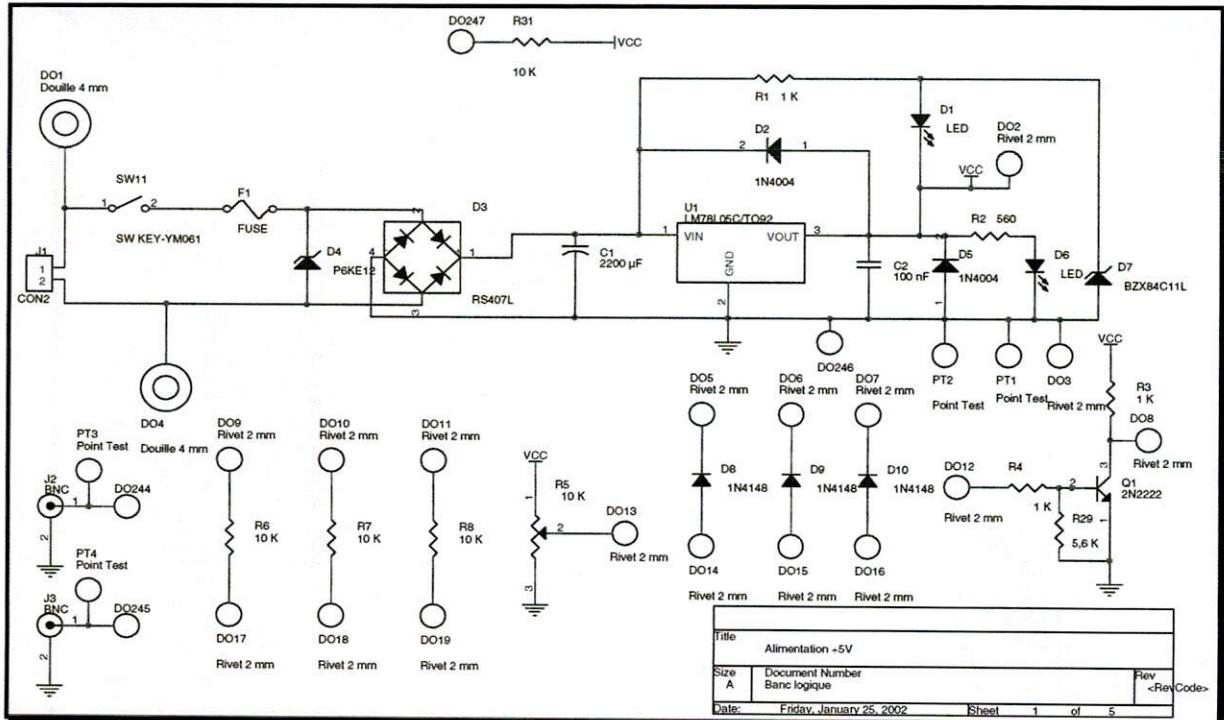
with :

x : 0 or 1 state,

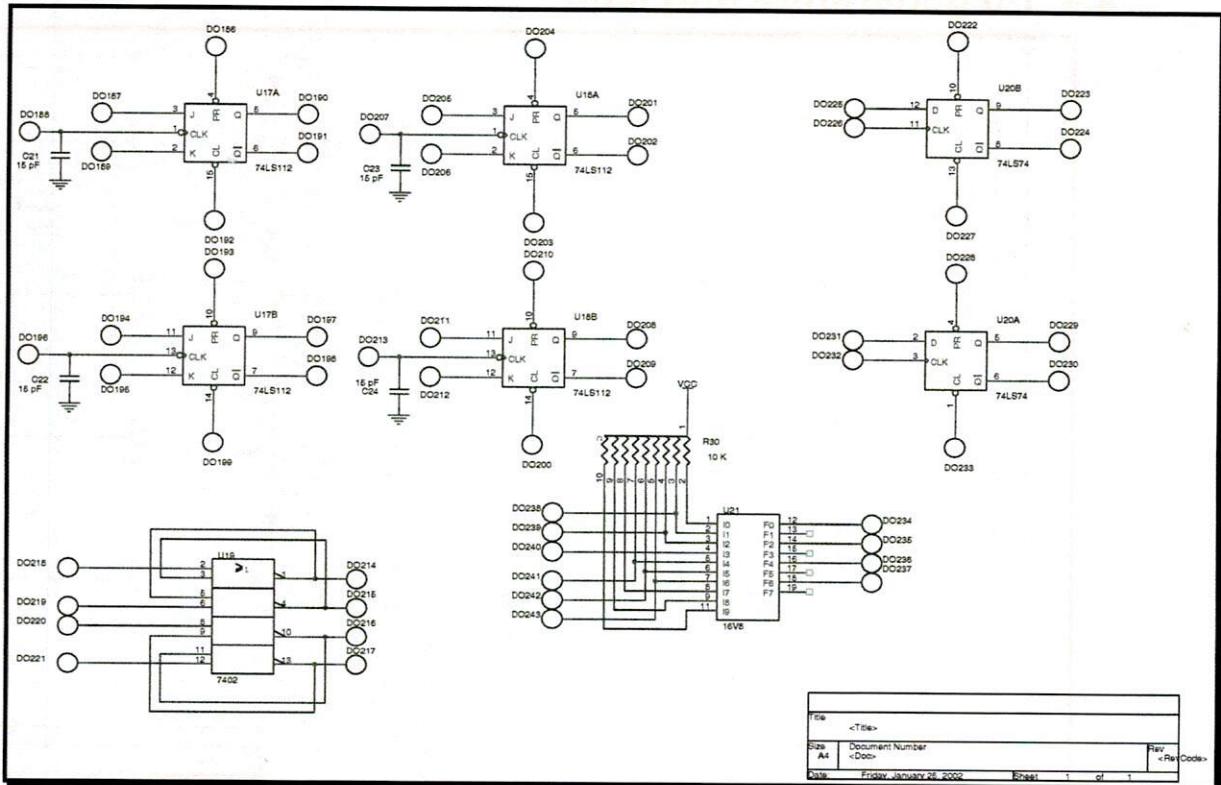
q./q : previous state.

## 4 Diagrams

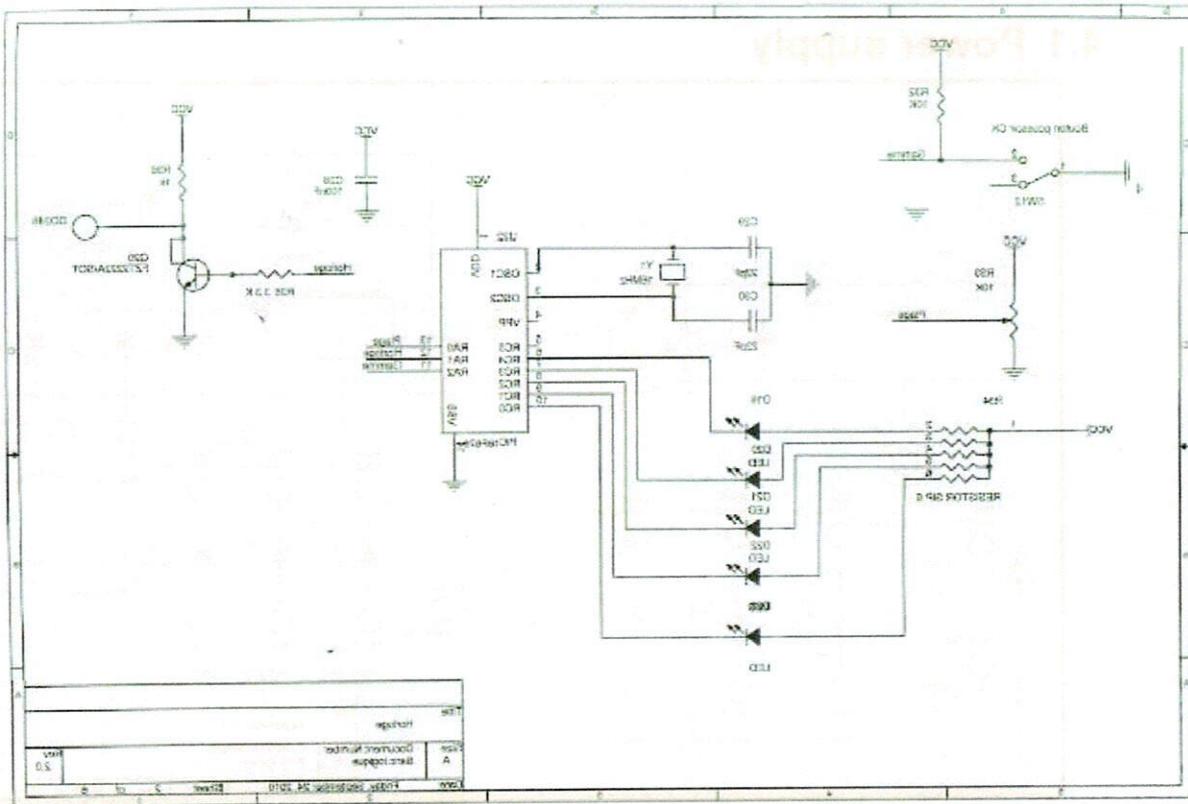
### 4.1 Power supply



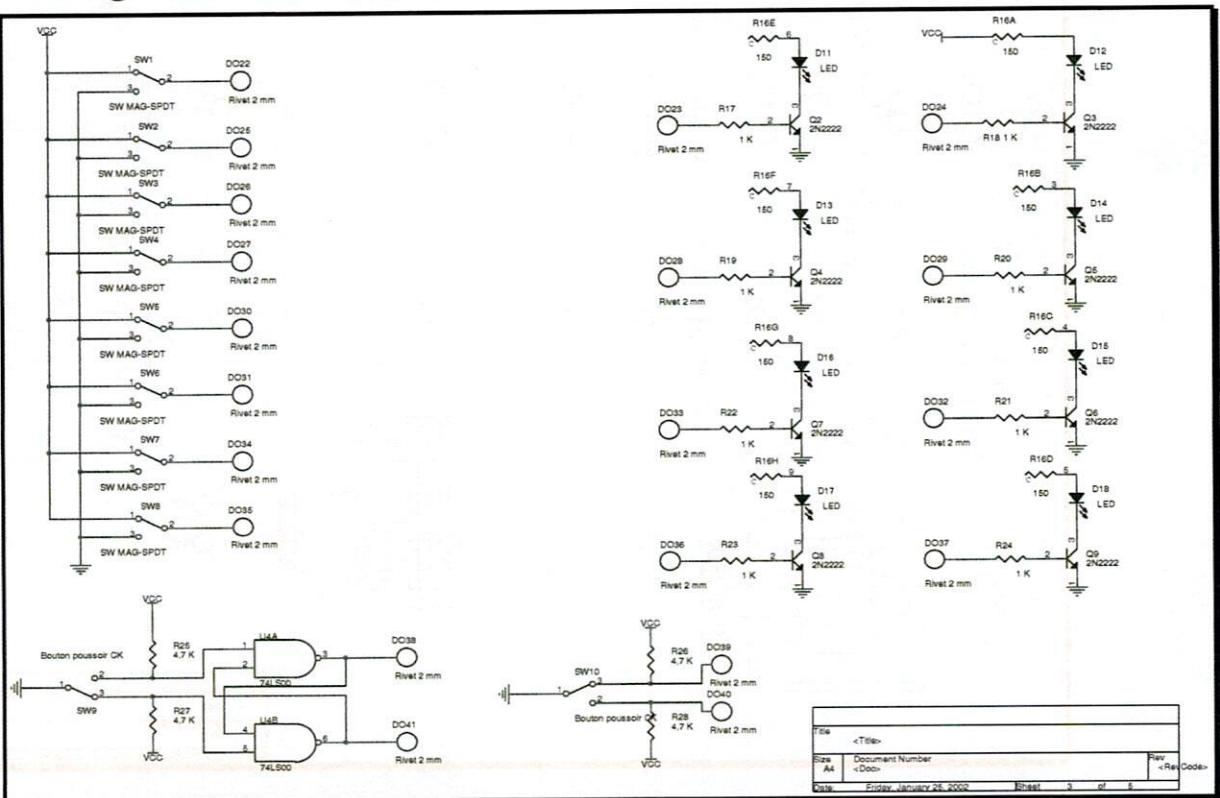
### 4.2 Flip-flops



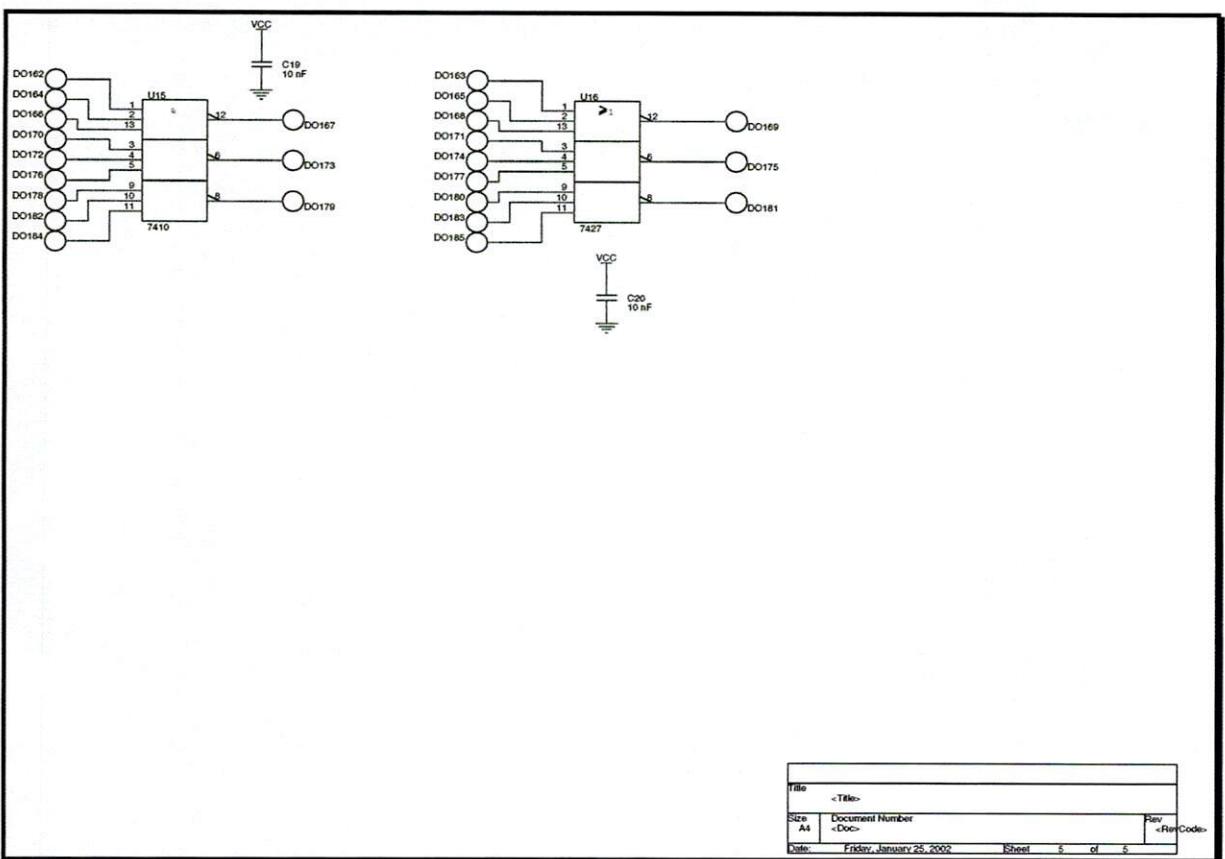
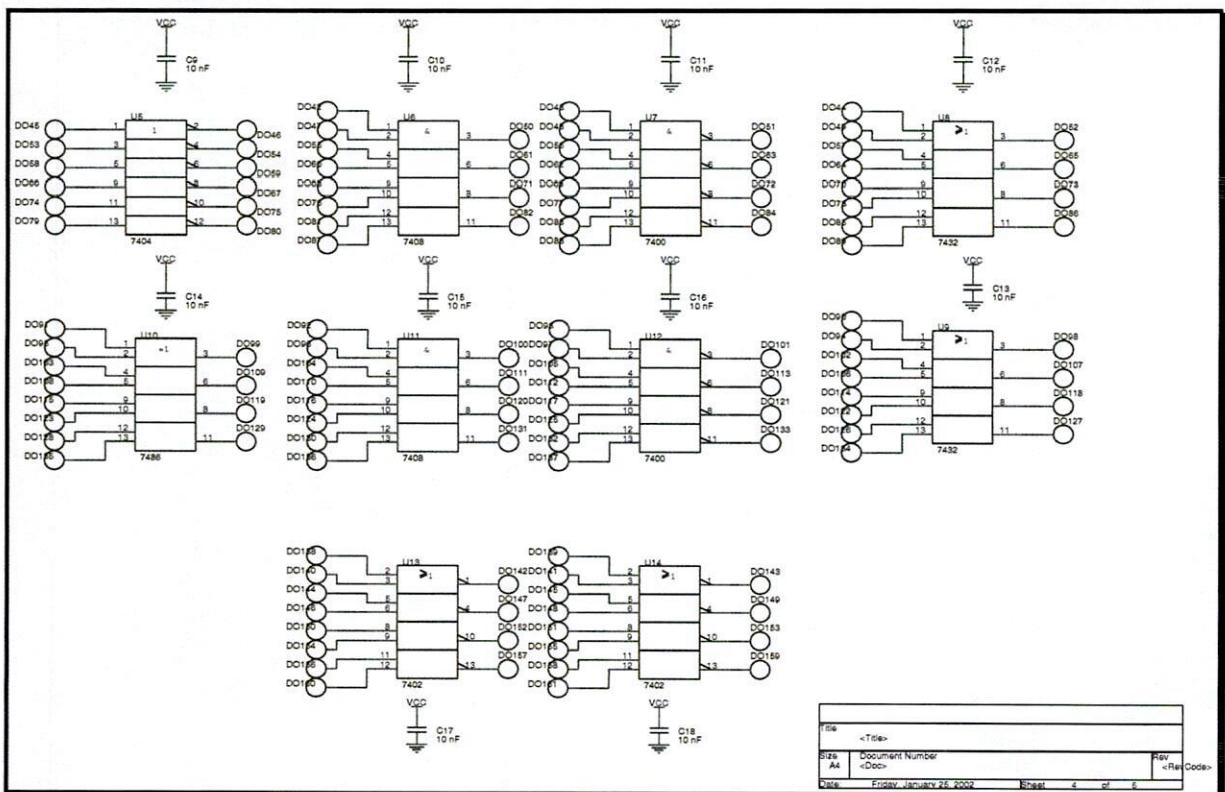
## 4.3 Clock



## 4.4 I/O generators and leds

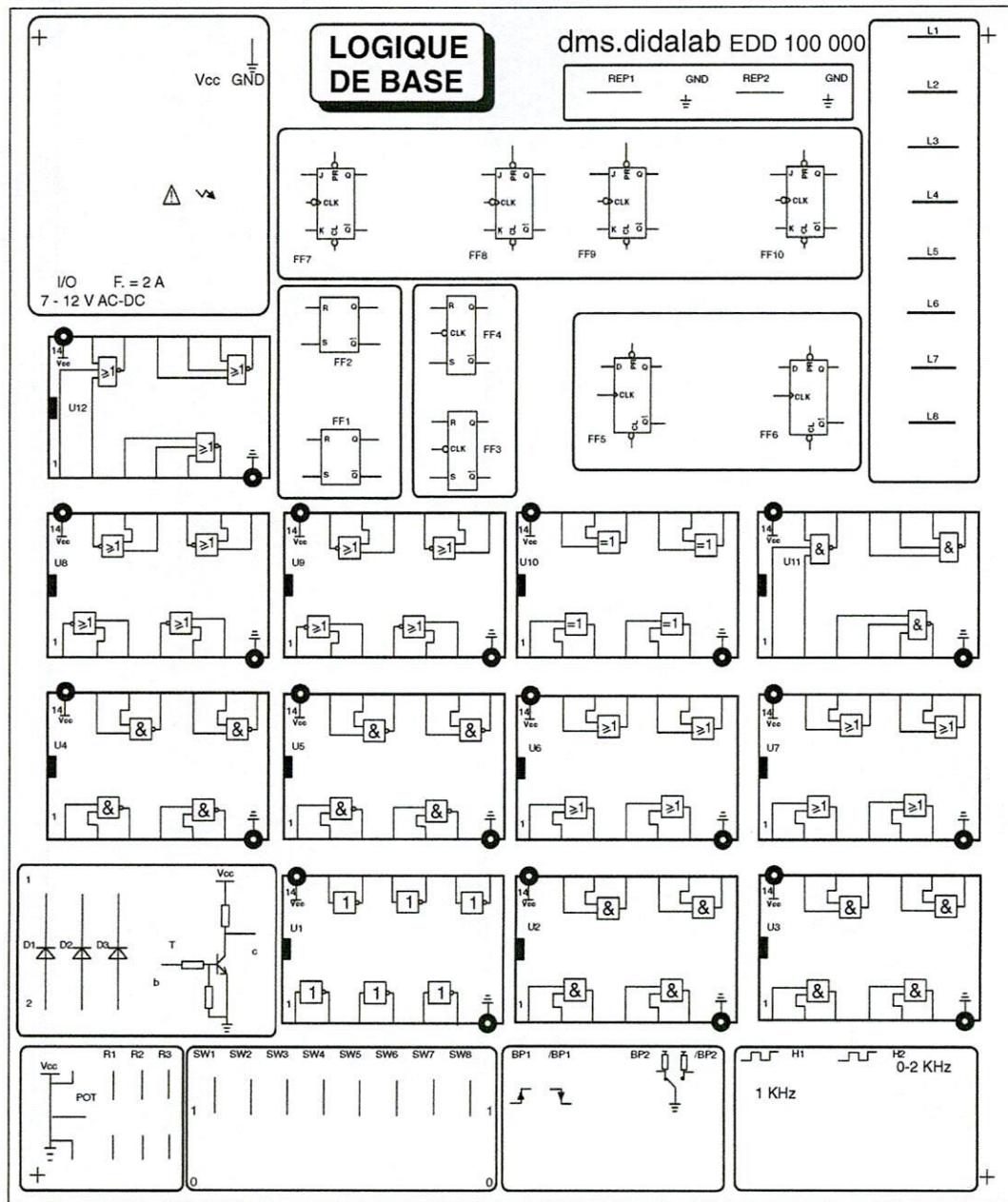


## 4.5 Logic gates





## 5 Display diagram



DMS Sérigraphie Version 1.11 Février 2002

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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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