NEC®

# 150 MHz DIVIDE-BY-16/17 LOW POWER PRESCALERS | UPB553AC

DESCRIPTION

The UPB553AC is a VHF two-modulus prescaler intended for use in measurement instrumentation and PLL Digital Tuning Systems in conjunction with UPD1700 series. Advanced bipolar process technology is utilized to realize high frequency operation with extremely low power consumptions. The device provides ÷16 and ÷17 division ratio for NEC's original pulse swallowing method, and is guaranteed to operate up to 130 MHz over the -35°C to +75°C temperature range with a Vcc variation from +4.5 to +5.5 V. An included amplifier allows it to be operated with a small amplitude signal of 150 mVp-p.

FEATURES

- High frequency operation: 150 MHz (÷16)
  130 MHz (÷17)
- NEC's original pulse swallowing operation: ÷16/÷17
- Small input amplitude: Vin = 150 m Vp-p (MIN.)
- Single supply voltage: V_{CC} = 5.0 V ±10 %
- Low supply current: I_{CC} = 8.9 mA (TYP.)
- Incorporated buffer amplifier: V_O=1.2 Vp-p (TYP.)
- Small package: 8 pin plastic dual in-line package (DIP)

PACKAGE DIMENSIONS (Unit: mm)
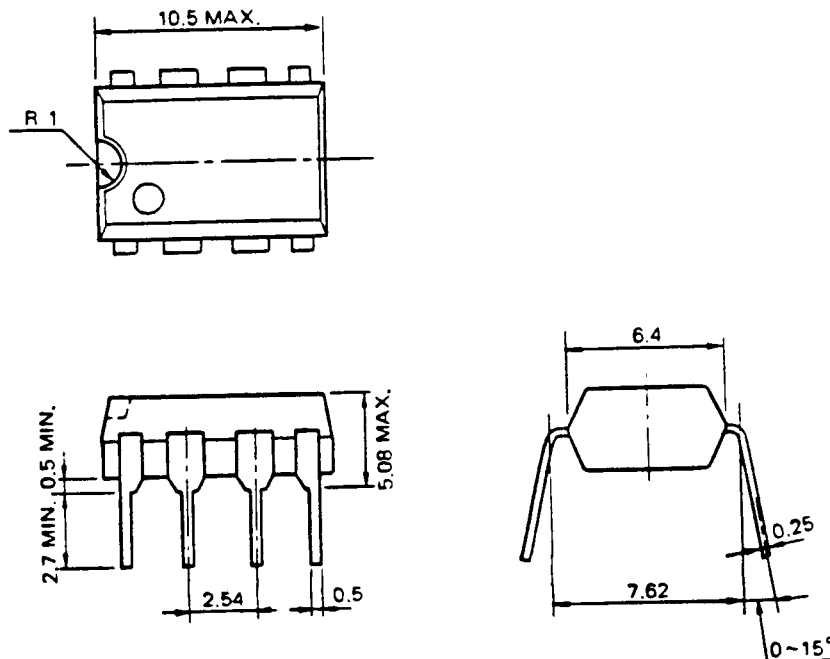
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to 6.0	V
Input Voltage	V_i	−0.5 to V_{CC}	V
Output Current	I_O	10	mA
Junction Temperature	T_j	+125	°C
Storage Temperature	T_{stg}	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	V_{CC}	4.5 to 5.5	V
Ambient Temperature	T_a	−35 to +75	°C
Output Load Capacitance	C_L	less than 10 picofarad	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10 %, T_a = −35 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Power Supply Current	I_{CC}		8.9	12.7	mA	V_{CC} = 5.0 V
Power Consumption	P_C		44.5		mW	T_a = 25 °C
Frequency Response	fin	1.0		150	MHz	Vin ≧ 0.15 Vp-p, ÷16
Frequency Response	fin	1.0		130	MHz	Vin ≧ 0.15 Vp-p, ÷17
Output Voltage	V_O	0.9	1.2		Vp-p	OUT terminal
Input Voltage	V_{in}	0.15		2.0	Vp-p	IN terminal
High Level Input Voltage	V_{IH}	$0.8V_{CC}$			V	PSC terminal
Low Level Input Voltage	V_{IL}			$0.2V_{CC}$	V	PSC terminal

Note: CHK terminal should be connected to GND.
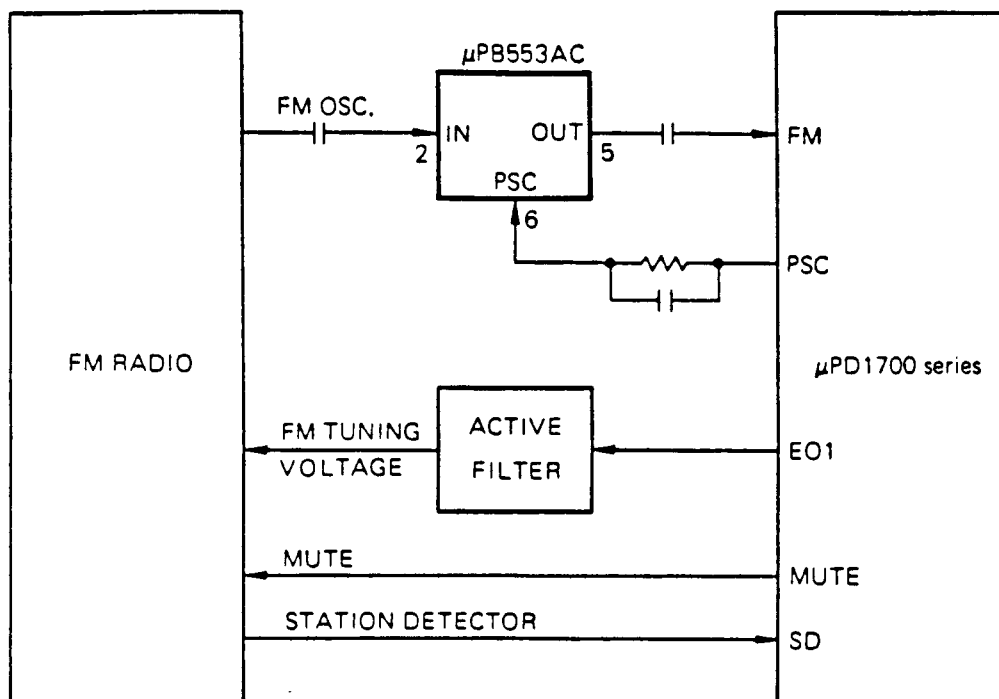
BLOCK DIAGRAM (Top View)

PSC (6)

G: CMOS to ECL Level Translator

ENABLE PULSE GENERATOR

S Q
R

X

Vcc (1)

CHK (3)

GND (4)

IN (2)

AMP

TIMING PULSE GENERATOR

T ÷16 DIVIDER Q

BUF (5) OUT

TIMING CHART

IN

CHK — INITIALIZE

PSC

X (ENABLE PULSE)

OUT

|— 17 pulses —| |— 16 pulses —|
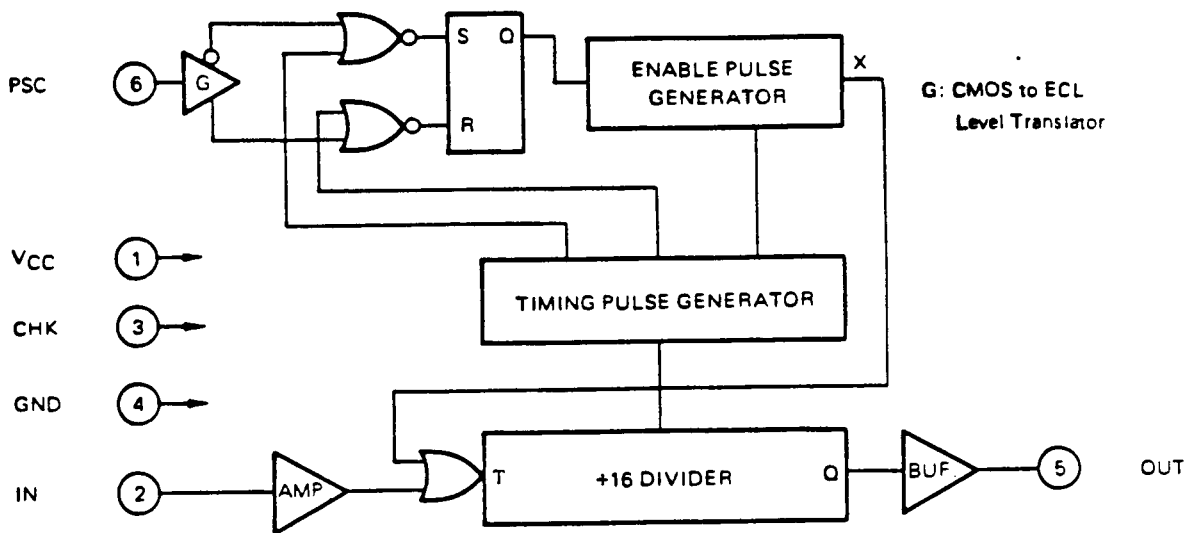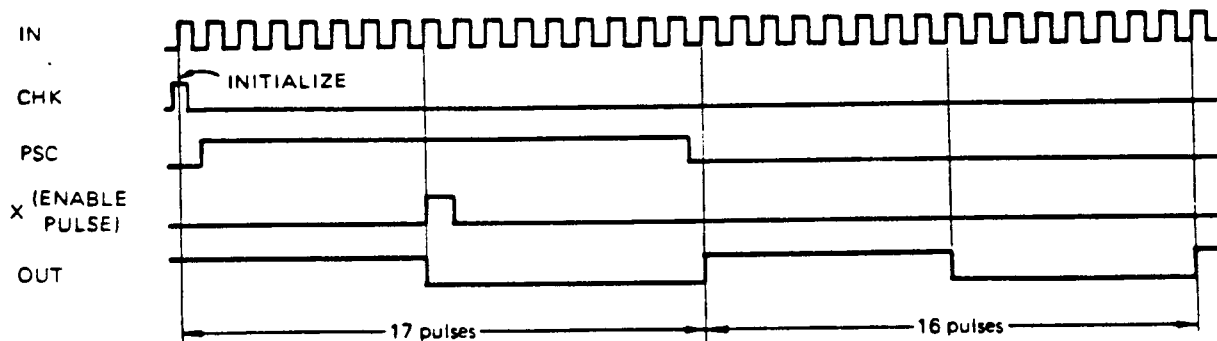
CONNECTION DIAGRAM

8 7 6 5

(Top View)

1 2 3 4
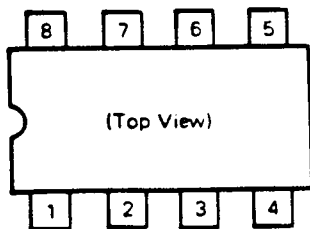
Pin Number	Symbol	Function
1	Vcc	Power Supply (Vcc)
2	IN	Signal Input
3	CHK	Check (Normally to GND)
4	GND	GND
5	OUT	Output
6	PSC	Division Ratio Control*
7	NC	No Connection
8	NC	No Connection

*: When PSC terminal fixed high or low level, the μPB553AC functions as a ÷/16 prescaler.

APPLICATION-1

APPLICATION-2

DATA SUBJECT TO CHANGE WITHOUT NOTICE-805

024286

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