Chloe Jiang‐‐ cfjiang

Lab section: 3PM TTh TA: Ehsan Hammati

Lab 3 Due: 2/7/2016

Part A:

|  |  |  |  |
| --- | --- | --- | --- |
| D | C | Q | Not Q |
| X | 0 | N/A | N/A |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 |

|  |  |  |  |
| --- | --- | --- | --- |
| D | R (Reset) | Q | Not Q |
| X | 1 | N/A | N/A |
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |

In creating the reset button for this D-latch, I had to find a way to send a 0 from the momentary button so that it can invert the output that would otherwise set off the Q instead of the Not Q. The goal was to set off the Not Q whenever the reset button was pressed no matter what, and the input had to be 0. Thus using the NOT gate to invert the 1 being sent from the button. Then I connected that to a NAND gate already in the D-latch and got my output.

**Part B:**

The read/write takes in the input for the entire circuit depending on its switch. The address space is 2. Accessibility is 212 .For word size there are 4 bits per register, and 3 registers total, that makes up 12 bits. There is no overflow in this diagram.