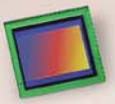
OmniVision™



datasheet

PRELIMINARY SPECIFICATION

1/3.2" CMOS QSXGA (5 megapixel) image sensor
with OmniBSI™ technology

OV5653

color CMOS QSXGA (5 megapixel) image sensor with OmniBSI™ technology

datasheet (CSP3)
PRELIMINARY SPECIFICATION

version 1.0
may 2009

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- digital still cameras
- digital video camcorders (DVC)
- PC multimedia
- cellular phones

ordering information

- **OV05653-A66A** (color, lead-free)
  66-pin CSP3

features

- 1.75 µm x 1.75 µm pixel with OmniBSI technology for high performance (high sensitivity, low crosstalk, low noise)
- optical size of 1/3.2”
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB), automatic band filter (ABF), automatic 50/60 Hz luminance detection, and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC 16-zone size/position/weight control, mirror and flip, cropping, windowing, and panning
- image quality controls: lens correction, 2-D defective pixel canceling
- support for output formats: 8-/10-bit raw RGB data
- support for video or snapshot operations
- support for LED and flash strobe mode
- support for internal and external frame synchronization for frame exposure mode
- support for horizontal and vertical sub-sampling
- standard serial SCCB interface
- digital video port (DVP) parallel output interface
- MIPI interface (two lanes), MIPI hub/secondary camera interface
- 256 bytes of embedded one-time programmable (OTP) memory
- on-chip phase lock loop (PLL)
- embedded 1.5V regulator for core power
- programmable I/O drive capability, I/O tri-state configurability
- support for black sun cancellation

key specifications

- **active array size:** 2592 x 1944
- **power supply:**
  core: 1.5V ± 5% (with embedded 1.5V regulator)
  analog: 2.6 ~ 3.0V (2.8V typical)
  I/O: 1.8V / 2.8V
- **power requirements:**
  active: 150 mA (see **table 8-3**)
  standby: 40 µA (see **table 8-3**)
- **temperature range:**
  operating: -30°C to 70°C (see **table 8-2**)
  stable image: 0°C to 50°C (see **table 8-2**)
- **output formats:** 8-/10-bit RGB RAW output
- **lens size:** 1/3.2"
- **lens chief ray angle:** 11.2° non-linear
  (see **figure 10-2**)
- **input clock frequency:** 6~27 MHz
- **S/N ratio:** 37 dB
- **dynamic range:** 69 dB
- **maximum image transfer rate:**
  QSXGA (2592x1944): 15 fps
  1080p: 30 fps
  720p: 60 fps
  VGA (640x480): 90 fps
  QVGA (320x240): 120 fps
- **sensitivity:** 1300mV/(Lux-sec)
- **shutter:** rolling shutter
- **maximum exposure interval:** 1968 x t_{ROW}
- **pixel size:** 1.75 µm x 1.75 µm
- **well capacity:** 7.5Ke^-
- **dark current:** <8 mV/sec at 60°C
- **fixed pattern noise (FPN):** 1% of $V_{PEAK-TO-PEAK}$
- **image area:** 4592 µm x 3423 µm
- **package dimensions:** 6505 µm x 6005 µm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV5653 image sensor. The package information is shown in **section 9**.

table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description	default SCCB status
A1	AGND	ground	analog ground	
A2	TM	input	test mode	
A3	DOVDD	power	digital pad power	
A4	RESET_B	input	input with pull up resistor	
A5	STROBE	output	frame exposure output indicator	
A6	SGND	ground	array ground	
A7	SVDD	power	array power	
A8	VHT	power	reference	
A9	VN	power	reference	
A10	NC	–	no connect	–
B1	SIOD	I/O	SCCB interface data pin	input
B2	AVDD	power	analog power	
B3	VSYNC	I/O	video output vertical signal or video data input	input
B4	FREX	I/O	frame exposure input / mechanical shutter output	input
B5	PWDN	input	input with pull down resistor	
B6	SGND	ground	array ground	
B7	SVDD	power	array power	
B8	VH	power	reference	
B9	AVDD	power	analog power	
B10	AVDD	power	analog power	
C2	MDP2	output	MIPI data positive output	
C3	SIOC	input	SCCB interface input clock	
C9	AGND	ground	analog ground	
C10	AGND	ground	analog ground	

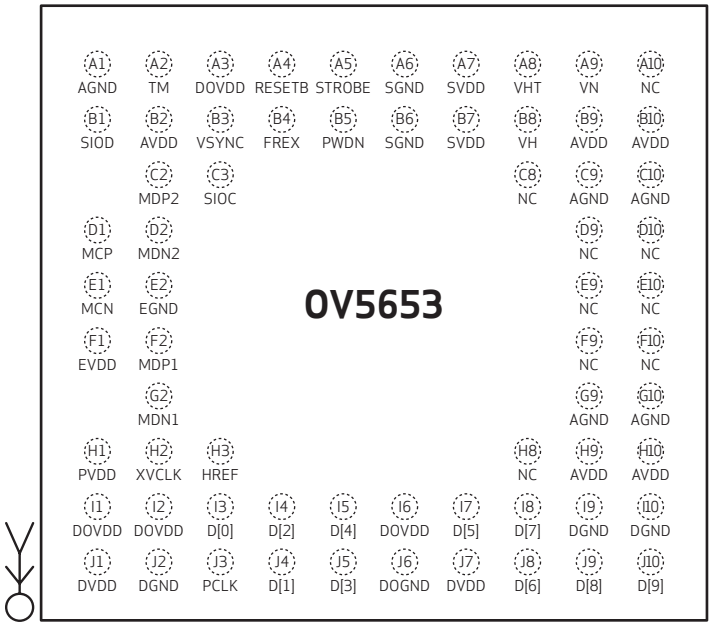
table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description	default SCCB status
D1	MCP	output	MIPI clock positive output	
D2	MDN2	output	MIPI data negative output	
E1	MCN	output	MIPI clock negative output	
E2	EGND	ground	MIPI analog ground	
F1	EVDD	power	MIPI analog power	
F2	MDP1	output	MIPI data positive output	
G2	MDN1	output	MIPI data negative output	
G9	AGND	ground	analog ground	
G10	AGND	ground	analog ground	
H1	PVDD	power	PLL analog power	
H2	XVCLK	input	system clock input	
H3	HREF	I/O	video output horizontal signal or video data input	input
H9	AVDD	power	analog power	
H10	AVDD	power	analog power	
I1	DOVDD	power	digital pad power	
I2	DOVDD	power	digital pad power	
I3	D0	I/O	video data output or video data input	input
I4	D2	I/O	video data output	input
I5	D4	I/O	video data output	input
I6	DOVDD	power	digital pad power	
I7	D5	I/O	video data output	input
I8	D7	I/O	video data output	input
I9	DGND	ground	digital logic ground	
I10	DGND	ground	digital logic ground	
J1	DVDD	power	digital logic power	
J2	DGND	ground	digital logic ground	
J3	PCLK	output	video output clock	
J4	D1	I/O	video data output or video data input	input
J5	D3	I/O	video data output	input

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description	default SCCB status
J6	DOGND	ground	ground	
J7	DVDD	power	digital logic power	
J8	D6	I/O	video data output	input
J9	D8	I/O	video data output	input
J10	D9	I/O	video data output	input

figure 1-1 pin diagram



5653_CSP_DS_1_1

table 1-2 configuration under various conditions

	RESET[a]	RESET[b]	post-RESET	standby	PD (power down pin = 1)
VSYNC	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
HREF	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
PCLK	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
D[9:0]	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
FREX	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
STROBE	high-z	high-z	input by default (configurable)	high-z by default (configurable)	high-z by default (configurable)
XVCLK	high-z	input	input	input	high-z
SIOD	open drain	I/O	I/O	I/O	open drain
SIOC	high-z	input	input	input	high-z
MCP	0	output	output	0	0
MCN	0	output	output	0	0
MDP1	high-z	high-z	output	high-z	high-z
MDN1	high-z	high-z	output	high-z	high-z
MDP2	high-z	high-z	output	high-z	high-z
MDN2	high-z	high-z	output	high-z	high-z

a. some customer assume PWDN pin = 1 when chip power up

b. PWDN pin = 0 when chip power up

2 system level description

2.1 overview

The OV5653 is a low voltage, high performance, 5 megapixel CMOS image sensor that provides 2592x1944 video output using OmniBSI™ technology. It provide multiple resolution raw images via the control of the serial camera control bus or MIPI interface.

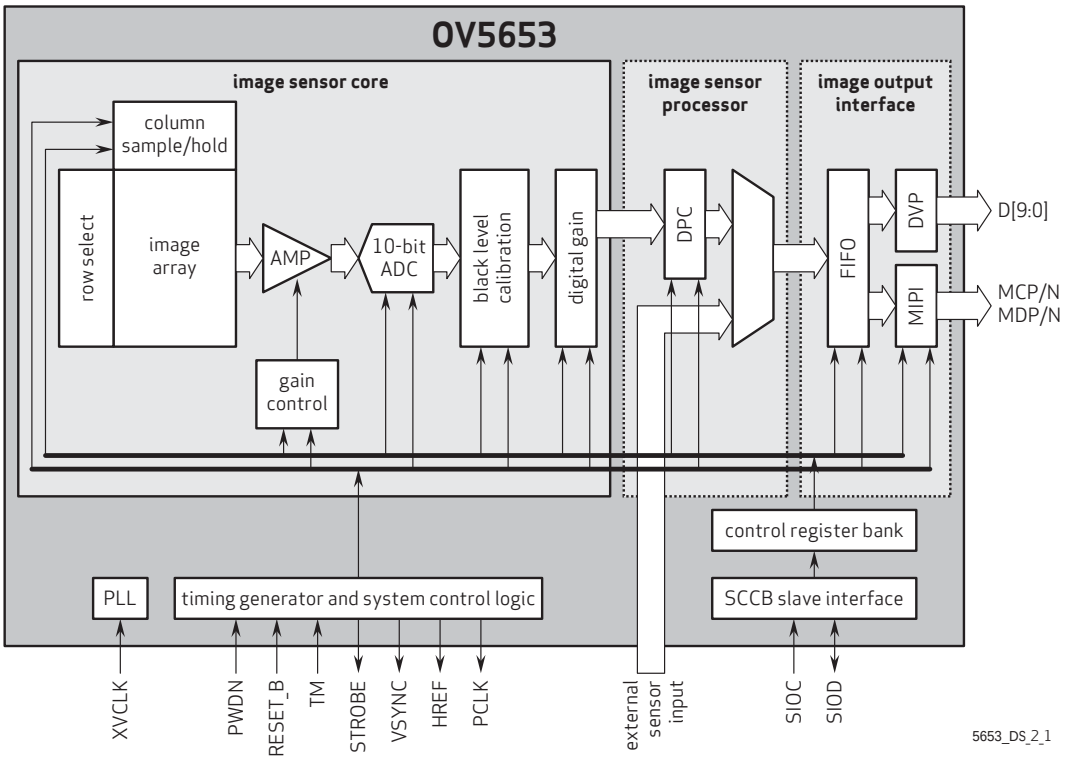
The OV5653 has an image array capable of operating up to 15 fps in 2592x1944 resolution with user control of image quality, data transfer, camera functions through the SCCB interface. The OV5653 use innovative OmniBSI technology to improve the sensor performance without the physical and optical trade-off.

For customized application, the OV5653 includes a one-time programmable (OTP) memory.

2.2 architecture

The OV5653 sensor core generates streaming pixel data at a constant frame rate, indicated by HREF and VSYNC. **figure 2-1** shows the functional block of the OV5653 image sensor. **figure 2.3** shows an example application of OV5653 sensor.

figure 2-1 OV5653 block diagram



2.3 format and frame rate

table 2-1 format and frame rate

format	resolution	frame rate	scaling method	pixel clock
5 Mpixel	2592x1944	15 fps	–	96 MHz
1080p	1920x1080	30 fps	cropping	96 MHz
720p	1280x720	60 fps	cropping and subsampling	96 MHz
VGA	640x480	90 fps	cropping and subsampling	96 MHz
1280x960	1280x960	30 fps	cropping and subsampling	96 MHz

2.4 I/O control

2.4.1 system clock control

The PLL is inside the chip which generates minimum 96 MHz clock from 6~27 MHz input clock. A programmable clock divider is embedded to generate different frame rate timing.

2.5 power up sequence

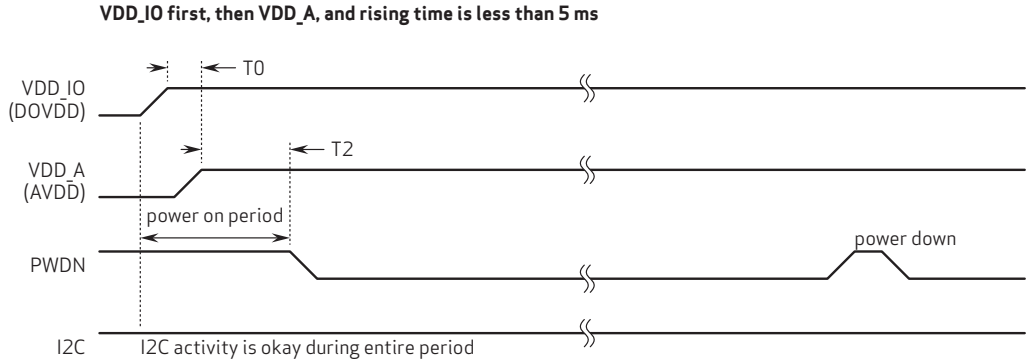
Based on the system power configuration (1.8V or 2.8V for I/O power, using external DVDD or internal DVDD, the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred. If 2.8V is used for I/O power, due to a high voltage drop at the internal DVDD regulator, there is a potential heat issue. Hence, for a 2.8V power system, OmniVision recommends using an external DVDD source. Due to the higher power down current when using an external DVDD source, OmniVision strongly recommends cutting off all powers, including the external DVDD, when the sensor is not in use in the case of 2.8V I/O and external DVDD.

2.5.1 power up with internal DVDD

For powering up with the internal DVDD and I2C access during the power ON period, the following conditions must occur:

1. if V_{DD-IO} and V_{DD-A} are turned ON at the same time, make sure V_{DD-IO} becomes stable before V_{DD-A} becomes stable
2. PWDN is active high with an asynchronized design (does not need clock)
3. PWDN must go high during the power up period
4. for PWDN to go low, power up must first become stable (AVDD to PWDN $\geq$ 5 ms)
5. RESET_B is active low with an asynchronized design
6. state of RESET_B does not matter during power up period once DOVDD is up
7. master clock XVCLK should provide at least 1 ms before host accesses sensor's I2C
8. host can access I2C bus (if shared) during entire period. 20 ms after PWDN goes low or 20 ms after RESET_B goes high if reset is inserted after PWDN goes low, host can access sensor's I2C to initialize sensor

figure 2-2 power up timing with internal DVDD



note T0 ≥ 0 ms: delay from VDD_IO stable to VDD_A stable
T2 ≥ 5 ms: delay from VDD_A stable to sensor power up stable

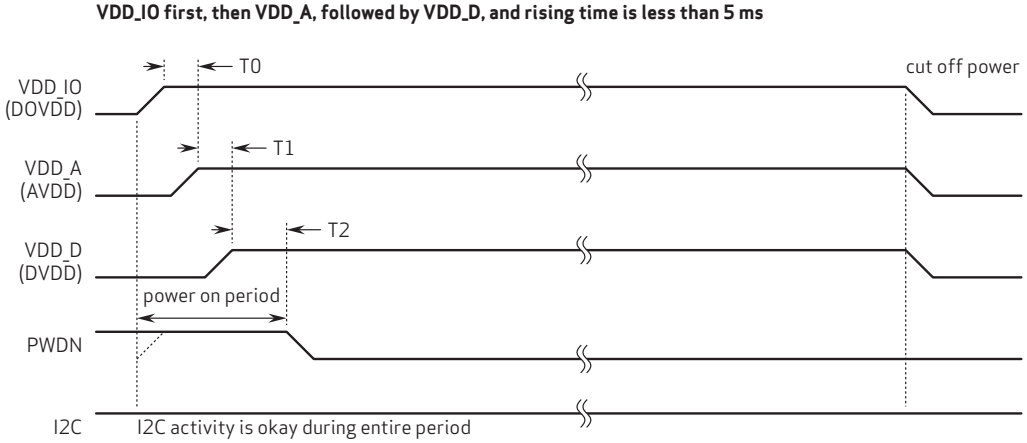
5653_DS_2_3

2.5.2 power up with external DVDD source

For powering up with an external DVDD source and I2C access during the power ON period, the following conditions must occur:

1. if V_{DD-IO} and V_{DD-A} are turned ON at the same time, make sure V_{DD-IO} becomes stable before V_{DD-A} becomes stable
2. if V_{DD-A} and V_{DD-D} are turned ON at the same time, make sure V_{DD-A} becomes stable before V_{DD-D} becomes stable
3. PWDN is active high with an asynchronized design (does not need clock)
4. for PWDN to go low, power up must first become stable (DVDD to PWDN $\geq$ 5 ms)
5. all powers are cut off when the camera is not in use (power down mode is not recommended
6. RESET_B is active low with an asynchronized design
7. state of RESET_B does not matter during power up period once DOVDD is up
8. master clock XVCLK should provide at least 1 ms before host accesses sensor's I2C
9. host can access I2C bus (if shared) during entire period. 20 ms after PWDN goes low or 20 ms after RESET_B goes high if reset is inserted after PWDN goes high, host can access sensor's I2C to initialize sensor

figure 2-3 power up timing with external DVDD source



note T0 ≥ 0 ms: delay from VDD_IO stable to VDD_A stable
T1 ≥ 0 ms: delay from VDD_A stable to VDD_D stable
T2 ≥ 5 ms: delay from VDD_D stable to sensor power up stable

5653_DS_2_4

2.6 reset

The OV5653 sensor includes a RESET_B pin that forces a complete hardware reset when it is pulled low (GND). The OV5653 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register 0x3008[7] to high.

The whole chip will be reset during power up. Manually applying a hard reset upon power up is recommended even though the on-chip power up reset is included. The hard reset is active low with an asynchronized design. The reset pulse width should be greater than or equal to 1 ms.

2.7 standby and sleep

Two suspend modes are available for the OV5653:

- hardware standby
- SCCB software sleep

To initiate hardware standby mode, the PWDN pin must be tied to high. When this occurs, the OV5653 internal device clock is halted and all internal counters are reset and registers are maintained. Executing a software power down (0x3008[6]) through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

3 /block level description

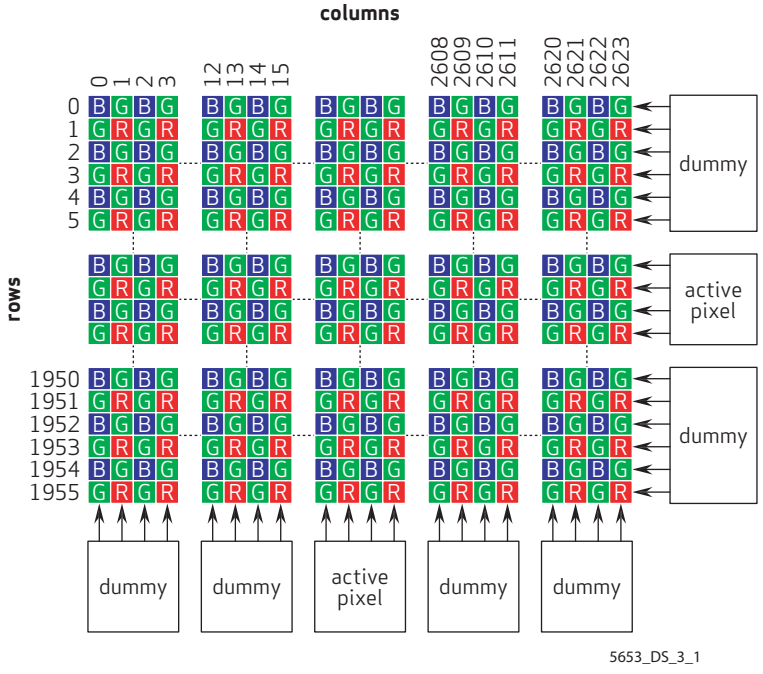
3.1 pixel array structure

The OV5653 sensor has an image array of 2624 columns by 1956 rows (5,132,544 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 5,132,544 pixels, 5,038,848 (2592x1944) are active pixels and can be output. The other pixels are used for black level calibration and interpolation. The center 2592x1944 is suggested to be output from the whole active pixel array. The backend processor can use the boundary pixels for additional processing.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



3.2 binning

OV5653 supports 2x2 binning for better SNR in low light conditions, see **table 3-1** for horizontal and vertical binning registers.

table 3-1 horizontal and vertical binning registers

address	register name	description
0x370D	ANALOG CONTROL D	Bit[6]: Vertical binning 0: Disable 1: Enable
0x3621	ARRAY CONTROL 01	Bit[7]: Horizontal binning/sub-sampling 0: Disable 1: Enable
0x3818	TIMING TC REG 18	Bit[0]: Vertical 2x sub-sampling 0: Disable 1: Enable

Sub-sampling is also necessary when using binning (see **section note**).

In addition, sensor timing adjustment is necessary after applying binning. Please consult your local FAE for details.

note
If only horizontal sub-sampling no horizontal binning is required, please also set 0x3621[6] to 1'b1.

figure 3-2 example of 2x2 binning

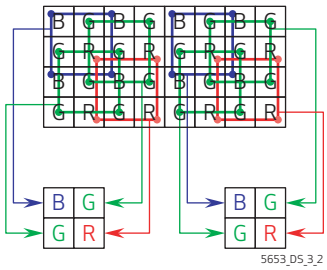


table 3-2 binning registers

address	register name	default value	R/W	description
0x3621	ARRAY CONTROL 01	0x00	RW	Bit[7]: Horizontal binning enable Bit[6]: Horizontal subsampling
0x370D	ANALOG CONTROL D	0x04	RW	Bit[6]: Vertical binning enable

table 3-3 example settings

2x2 binning	2x2 subsampling
6C 3621 AF	6C 3621 EF
6C 370D 42	6C 370D 02
6C 3818 C1	6C 3818 C1
2x1 binning	**2x1 subsampling**
6C 3621 EF	6C 3621 AF
6C 370D 42	6C 370D 02
6C 3818 C1	6C 3818 C1

3.3 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

3.4 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC. It can operate at up to 27 MHz and is fully synchronous to the pixel clock. The actual conversion rate is determined by the frame rate.

4 image sensor core digital functions

4.1 mirror and flip

The OV5653 provides mirror and flip read-out modes, which respectively reverse the sensor data read-out order horizontally and vertically (see **figure 4-1**). In flip mode, the OV5653 does not need additional settings because the ISP block will auto-detect whether the pixel is in the red line or blue line and make the necessary adjustments. For the mirror function, it is also necessary to set register 0x505A, 0x505B and 0x381A.

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

5653_DS_4_1

note
after applying mirror function ISP LENC offset (0x505A and 0x505B) should also be adjusted.

table 4-1 mirror flip control registers

address	register name	default value	R/W	description
0x3818	TIMING TC REG18	0x80	RW	Timing Control Bit[6]: Mirror Bit[5]: Vertical flip

4.2 image windowing

An image windowing area is defined by four parameters, HS (horizontal start), HW (horizontal width), VS (vertical start), and VH (vertical height). By properly setting the parameters, any portion or size within the sensor array can be defined as an visible area. This windowing is achieved by simply masking the pixels outside the defined window; thus, it will not affect the original timing.

figure 4-2 image windowing

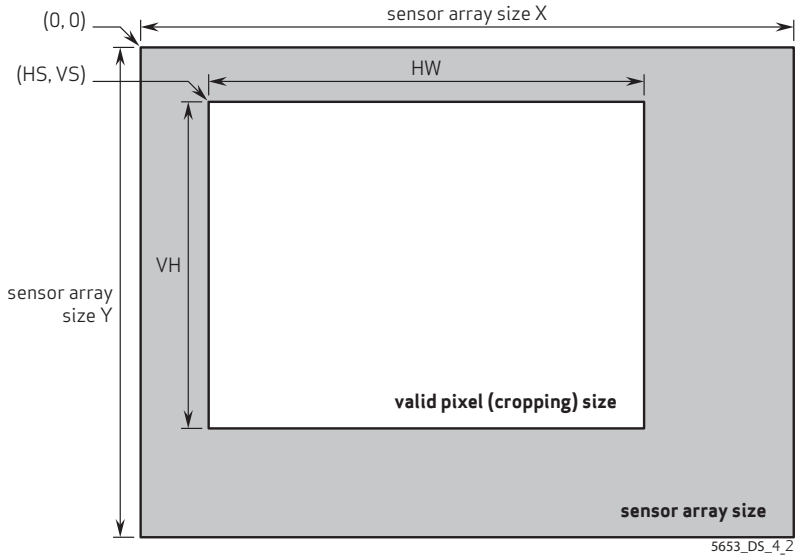


table 4-2 MIPI control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	TIMING CONTROL HS	0x01	RW	HREF Horizontal Start Point High Byte Bit[3:0]: Horizontal start point[11:8]
0x3801	TIMING CONTROL HS	0xB4	RW	HREF Horizontal Start Point Low Byte Bit[7:0]: Horizontal start point[7:0]
0x3802	TIMING CONTROL VS	0x00	RW	HREF Vertical Start Point High Byte Bit[3:0]: Vertical start point[11:8]
0x3803	TIMING CONTROL VS	0x0A	RW	HREF Vertical Start Point Low Byte Bit[7:0]: Vertical start point[7:0]
0x3804	TIMING HW	0x0D	RW	HREF Horizontal Width High Byte Bit[3:0]: Horizontal width[11:8]

table 4-2 MIPI control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3805	TIMING HW	0xA0	RW	HREF Horizontal Width Low Byte Bit[7:0]: Horizontal width[7:0]
0x3806	TIMING VH	0x0A	RW	HREF Vertical Height High Byte Bit[3:0]: Vertical height[11:8]
0x3807	TIMING VH	0x38	RW	HREF Vertical Height Low Byte Bit[7:0]: Vertical height[7:0]

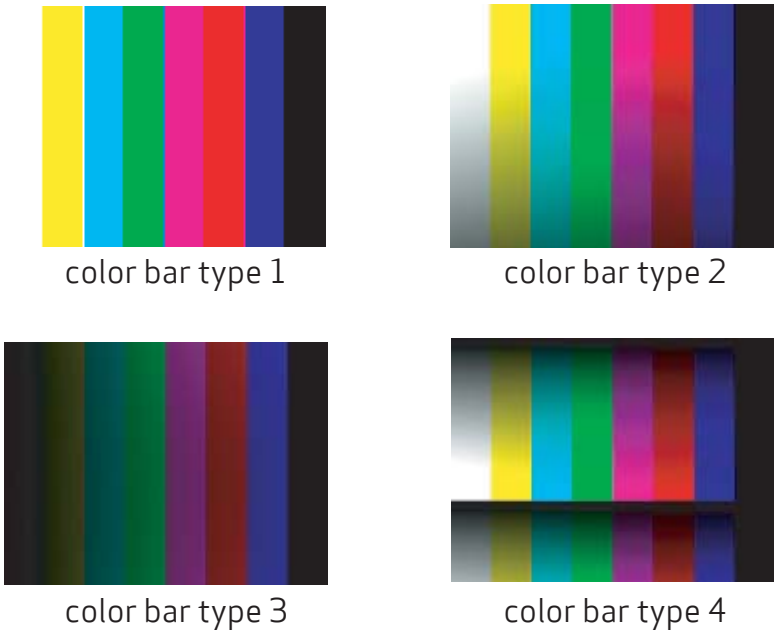
4.3 test pattern

For testing purposes, the OV5653 offers three types of test patterns, color bar, square and random data.The OV5653 also offers two effects: transparent effect and rolling bar effect. The function is enabled by 0x503D[7]. The output type of test pattern is controlled by test_pattern_type (0x503D[7]) register.

4.3.1 color bar

There are four types of color bars shown in **figure 4-3**. The output type of color the color bar can be selected by bar style register 0x503D[5:4].

figure 4-3 color bar types



4.3.2 square

There are two types of square: color square and black-white square. The squ_bw register (0x503E[3]) decides which type of square will be output.

figure 4-4 color, black and white square bars

5653_DS_4_4

4.3.3 random data

There are two types of random data test pattern: frame-changing and frame-fixed random data. The output type of random data is decided by rnd_same register 0x503D[6]. The random seed is set by rnd_seed register 0x503E[7:4].

4.3.4 transparent effect

The transparent effect is enabled by transparent-mode register 0x503E[2]. If this register is set, the transparent test pattern will be gotten. **figure 4-5** is a example which shows a transparent color bar image.

figure 4-5 transparent effect

5653_DS_4_5

4.3.5 rolling bar effect

The rolling bar is set by rolling-bar register 0x503D[2]. If it is set, a inverted-color rolling bar will roll from up to down. **figure 4-6** is a example which shows a rolling bar on color bar image.

figure 4-6 rolling bar effect

rolling bar effect

5653_DS_4_6

table 4-3 test pattern registers

address	register name	default value	R/W	description
0x503D	ISP CTRL3D	0x00	RW	Bit[7]: test_pattern_en 0: Disable 1: Enable Bit[6]: rnd_same 0: Frame changing random data pattern 1: Frame-fixed random data pattern Bit[5:4]: bar_style When set to different value, the different type color bar will be output Bit[2]: rolling_bar 0: Disable rolling bar 1: Enable rolling bar
0x503E	ISP CTRL3E	0x00	RW	Bit[7:4]: rnd_seed Initial seed for random data pattern Bit[3]: squ_bw_mode 0: Output square is color square 1: Output square is black- white square Bit[2]: transparent_mode 0: Disable 1: Enable Bit[1:0]: test_pattern_type 00: Color bar 01: Square 10: Random data 11: Input data

4.4 50/60Hz detection

4.4.1 overview

When the integration time is not an integer multiple of the period of light intensity, the image will flicker. The function of the detector is to detect whether the sensor is under a 50 Hz or 60 Hz light source so that the basic step of integration time can be determined. Contact your local OmniVision FAE for auto detection settings.

4.4.2 threshold mode

To avoid judgment flicker, two threshold modes, sum threshold and counter threshold, have been added.

- sum threshold: threshold is not constant, but rather a variable according to its conditions.
- counter threshold: judgment result will not be changed until the counter reaches a certain number that the user can set by a register.

table 4-4 50/60 Hz detection control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3C00	5060HZ CTRL00	0x00	RW	Bit[5]: th_time_div Threshold time divide 0: Disable 1: Enable Bit[4]: row_limit_en Row limit enable 0: Disable 1: Enable Bit[3]: reverse_sigma_en Reverse sigma enable 0: Disable 1: Enable Bit[2]: band_def Band50 default value 0: 60 Hz as default value 1: 50 Hz as default value Bit[1:0]: time_cnt_thresh Threshold time count 00: 1s 01: 2s 10: 4s 11: 8s

table 4-4 50/60 Hz detection control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3C01	5060HZ CTRL01	0x00	RW	Bit[7]: band_man_en Band detection manual mode 0: Manual mode disable 1: Manual mode enable Bit[6]: band_begin_rst Band begin reset enable 0: Disable 1: Enable Bit[5]: sum_auto_mode Sum auto mode enable 0: Disable 1: Enable Bit[4]: band_cnt_en Band counter enable 0: Disable 1: Enable Bit[3:0]: band_cnt_thresh Counter threshold for band change
0x3C02	5060HZ CTRL02	0x00	RW	Bit[7:6]: th_low_limit Bit[5:0]: th_low_light
0x3C03	LOW LIGHT CNT THRESH	0x00	RW	Bit[7:0]: low_light_cnt_thresh
0x3C04	SUM LOW THRESH	0x20	RW	Bit[7:0]: sum_low_thresh
0x3C05	SUM HIGH THRESH	0x70	RW	Bit[7:0]: sum_high_thresh
0x3C06	LM1 THRESH	0x00	RW	Bit[7:0]: lm1_thresh[15:8]
0x3C07	LM1 THRESH	0x00	RW	Bit[7:0]: lm1_thresh[7:0]
0x3C08	LM2 THRESH	0x01	RW	Bit[7:0]: lm2_thresh[15:8]
0x3C09	LM2 THRESH	0x2C	RW	Bit[7:0]: lm2_thresh[7:0]
0x3C0A	SAMPLE NUM	0x4E	RW	Bit[7:0]: sample_number[15:8]
0x3C0B	SAMPLE NUM	0x1F	RW	Bit[7:0]: sample_number[7:0]
0x3C0C	5060HZ CTRL0C	–	R	Bit[0]: band50 0: Detection result is 60 Hz 1: Detection result is 50 Hz

4.5 AEC and AGC algorithms

4.5.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-5**

table 4-5 AEC/AGC control function registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3500	LONG EXPO	0x00	RW	Bit[3:0]: long_exposure[19:16] long_exposure in unit of 1/16 line
0x3501	LONG EXPO	0x00	RW	Bit[7:0]: long_exposure[15:8] long_exposure in unit of 1/16 line
0x3502	LONG EXPO	0x20	RW	Bit[7:0]: long_exposure[7:0] long_exposure in unit of 1/16 line
0x3503	MANUAL CTRL	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Gain latch timing delay x0: Gain has no latch delay 01: Gain delay of 1 frame 11: Gain delay of 2 frames Bit[3]: Not used Bit[2]: Debug mode Bit[1]: AGC manual 0: Auto enable 1: Manual enable Bit[0]: AEC manual 0: Auto enable 1: Manual enable
0x3508	LONG GAIN	0x00	RW	Bit[0]: long_gain[8]
0x3509	LONG GAIN	0x00	RW	Bit[7:0]: long_gain[7:0]
0x350A	AGC ADJ	0x00	RW	Gain Output to Sensor Bit[0]: Gain high bit Gain = (0x350B[6]+1) × (0x350B[5]+1) × (0x350B[4]+1) × (0x350B[3:0]/16+1)
0x350B	AGC ADJ	0x00	RW	Gain Output to Sensor Bit[7:0]: Gain low bits Gain = (0x350B[6]+1) × (0x350B[5]+1) × (0x350B[4]+1) × (0x350B[3:0]/16+1)
0x350C	VTS DIFF	0x06	RW	Bit[7:0]: vts_diff[15:8] Changing this value is not recommended

table 4-5 AEC/AGC control function registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x350D	VTS DIFF	0x18	RW	Bit[7:0]: vts_diff[7:0] Changing this value is not recommended

For the average-based AEC/AGC algorithm, the measured window is horizontally and vertically adjustable and divided by sixteen (4x4) zones (see **figure 4-8**). Each zone (or block) is 1/16th of the image and has a 4-bit weight in calculating the average luminance (YAVG). The 4-bit weight could be n/16 where n is from 0 to 15. The final YAVG is the weighted average of the sixteen zones.

4.5.2 average-based algorithm

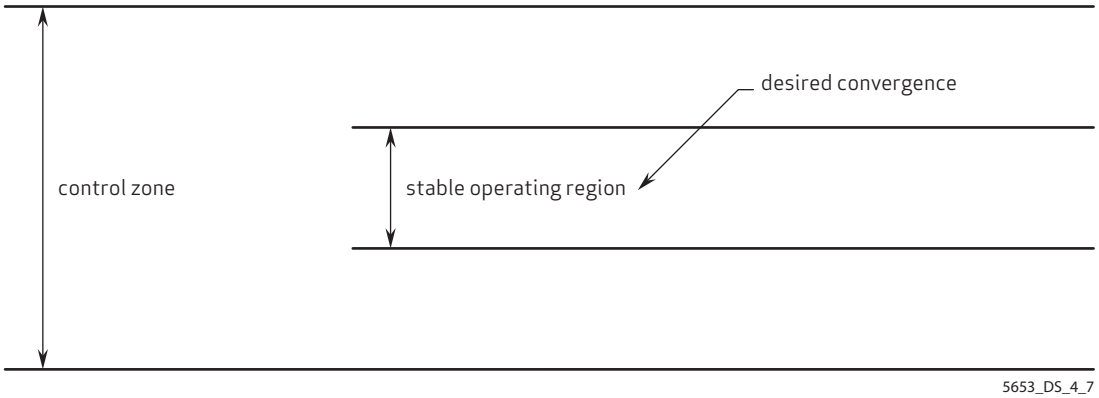
The average-based AEC controls image luminance using registers **WPT** (0x3A0F), **BPT** (0x3A10), **WPT2** (0x3A1B), and **BPT2** (0x3A1E). In average-based mode, the value of register **WPT** (0x3A0F) indicates the high threshold value, and the value of register **BPT** (0x3A10) indicates the low threshold value. The value of register **WPT2** (0x3A1B) indicates the high threshold value for image change from stable state to unstable state and the value of register **BPT2** (0x3A1E) indicates the low threshold value for image change from stable state to unstable state. When the target image luminance average value AVG ({0x5690[1:0], 0x5691[7:2]}) is within the range specified by registers **WPT2** (0x3A1B) and **BPT2** (0x3A1E), the AEC keeps the image exposure and gain. When register AVG ({0x5690[1:0], 0x5691[7:2]}) is greater than the value in register **WPT2** (0x3A1B), the AEC will decrease the image exposure and gain until it falls into the range of {0x3A10, 0x3A0F}. When register AVG ({0x5690[1:0], 0x5691[7:2]}) is less than the value in register **BPT2** (0x3A1E), the AEC will increase the image exposure and gain until it falls into the range of {0x3A10, 0x3A0F}. Accordingly, the value in register **WPT** (0x3A0F) should be greater than the value in register **BPT** (0x3A10). The gap between the values of registers **WPT2** (0x3A1B) and **BPT2** (0x3A1E) controls the image stability.

The AEC function supports both manual and auto speed selections in order to bring the image exposure into the range set by the values in registers **WPT** (0x3A0F) and **BPT** (0x3A10). For manual mode, the speed supports both normal and fast speed selection. AEC set to normal mode will allow for the slowest step increment or decrement in the image exposure to maintain the specified range. AEC set to fast mode will provide for an approximate ten-step increment or decrement in the image exposure to maintain the specified range. For auto mode, the speed step will automatically be adjusted according to the difference between the target and present values. The auto ratio of steps can be set by register bits AEC CTRL05[4:0] (0x3A05); thus, the AEC speed can be adjusted automatically by the image average value or controlled manually.

Register **HIGH VPT** (0x3A11) and register **LOW VPT** (0x3A1F) controls the fast AEC range in manual speed selection made. If the target image AVG ({0x5690[1:0], 0x5691[7:2]}) is greater than **HIGH VPT** (0x3A11), AEC will decrease by half. If register AVG ({0x5690[1:0], 0x5691[7:2]}) is less than **LOW VPT** (0x3A1F), AEC will double.

As shown in **figure 4-7**, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size of fast and slow conditions.

figure 4-7 desired convergence



As for auto mode, the AEC will automatically calculate the steps needed based on the difference between target and current values. So, the outer control zone is meaningless for this mode.

table 4-6 AEC/AGC control function registers

address	register name	default value	R/W	description
0x3A0F	WPT	0x78	RW	Bit[7:0]: WPT Stable Range High Limit (enter)
0x3A10	BPT	0x68	RW	Bit[7:0]: BPT Stable Range Low Limit (enter)
0x3A11	HIGH VPT	0xD0	RW	Bit[7:0]: vpt_high Fast zone high limit when step ratio auto mode is disabled
0x3A1B	WPT2	0x78	RW	Bit[7:0]: wpt2 Stable Range High Limit (from stable state to unstable state)
0x3A1E	BPT2	0x68	RW	Bit[7:0]: bpt2 Stable Range Low Limit (from stable state to unstable state)
0x3A1F	LOW VPT	0x40	RW	Bit[7:0]: vpt_low Fast zone low limit when step ratio auto mode is disabled

4.5.3 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. By properly setting x_start, x_end, y_start, and y_end as shown in **figure 4-8**, a 4x4 grid average window is defined. It will automatically divide each zone into 4x4 zones. The average value is the weighted average of the 16 sections. **table 4-7** lists the corresponding registers.

figure 4-8 average-based window definition

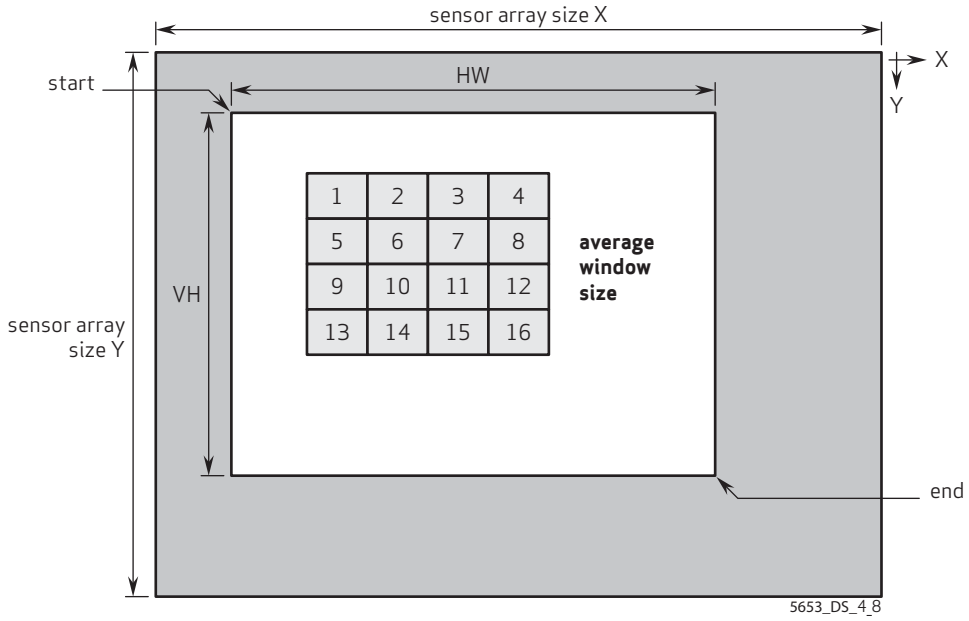


table 4-7 AEC/AGC control function registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5680	XSTART	0x00	RW	Bit[7:4]: Not used Bit[3:0]: x_start[11:8] Horizontal start position for average window high byte
0x5681	XSTART	0x00	RW	Bit[7:0]: x_start[7:0] Horizontal start position for average window low byte
0x5682	XEND	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: x_end[11:8] Horizontal end position for average window high byte
0x5683	XEND	0x20	RW	Bit[7:0]: x_end[7:0] Horizontal end position for average window low byte

table 4-7 AEC/AGC control function registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5684	YSTART	0x00	RW	Bit[7:4]: Not used Bit[3:0]: y_start[11:8] Vertical start position for average window high byte
0x5685	YSTART	0x00	RW	Bit[7:0]: y_start[7:0] Vertical start position for average window low byte
0x5686	YEND	0x07	RW	Bit[7:4]: Not used Bit[3:0]: y_end11:8] Vertical end position for average window high byte
0x5687	YEND	0x98	RW	Bit[7:0]: y_end[7:0] Vertical end position for average window low byte
0x5688	WEIGHT00	0xFF	RW	Bit[7:4]: Window1 weight Bit[3:0]: Window0 weight
0x5689	WEIGHT01	0xFF	RW	Bit[7:4]: Window3 weight Bit[3:0]: Window2 weight
0x568A	WEIGHT02	0xFF	RW	Bit[7:4]: Window5 weight Bit[3:0]: Window4 weight
0x568B	WEIGHT03	0xFF	RW	Bit[7:4]: Window7 weight Bit[3:0]: Window6 weight
0x568C	WEIGHT04	0xFF	RW	Bit[7:4]: Window9 weight Bit[3:0]: Window8 weight
0x568D	WEIGHT05	0xFF	RW	Bit[7:4]: Window11 weight Bit[3:0]: Window10 weight
0x568E	WEIGHT06	0xFF	RW	Bit[7:4]: Window13 weight Bit[3:0]: Window12 weight
0x568F	WEIGHT07	0xFF	RW	Bit[7:4]: Window15 weight Bit[3:0]: Window14 weight
0x5690	AVG	–	R	Bit[1:0]: Average[9:8]
0x5691	AVG	–	R	Bit[7:0]: Average[7:0]
0x5693	AVG CTRL00	0x00	RW	Bit[7:3]: Not used Bit[2]: flip_auto_chg 0: Disable 1: Enable Bit[1]: mirror_auto_chg 0: Disable 1: Enable Bit[0]: sub_win_en 0: Disable sub window, the average window will be set with output sizes 1: Enable sub window, the average window will be set by XSTART, XEND, YSTART and YEND

4.6 AEC/AGC steps

The AEC and AGC work together to obtain adequate exposure/gain based on the current environmental illumination. In order to achieve the best signal to noise ratio (SNR), extending the exposure time is always preferred rather than raising the gain when the current illumination is getting brighter. Vice versa, under dark conditions, the action to decrease the gain is always taken prior to shortening the exposure time.

4.6.1 auto exposure control (AEC)

The function of the AEC is to calculate the necessary integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain the same.

In extremely bright situations, the LAEC activates, allowing integration time to be less than one row. In extremely dark situations, the night mode activates, allowing integration time to be larger than one frame.

To avoid image flickering under a periodic light source, the integration time can be adjusted in steps of integer multiples of the period of the light source. This new AEC step system is called the banding filter, suggesting that the exposure time is not continuous but falls in some steps.

4.6.2 LAEC

If the integration time is only one row period but the image is too bright, AEC will enter LAEC mode. Within LAEC, the integration time can be further decreased to the minimum of 1/16 row. LAEC ON/OFF can be set in register bit 0x3A00[6].

4.6.3 night mode

The OV5653 supports long integration time larger than one frame in dark conditions. This is achieved by slowing down the original frame rate and waiting for exposure. Night mode ceiling can be set in register bits {0x3A02[19:16], 0x3A03[15:8], 0x3A04[7:0]}. Night mode can be disabled by setting register bit 0x3A00[2] to 0. Also, when in night mode, the increase and decrease step can be based on either band or frames, depending on register 0x3A05[6]. The minimum increase/decrease step can be one band.

4.6.4 banding mode ON with AEC

In Banding ON mode, the exposure time will fall in steps of integer multiples of the period of light intensity. This design is to reject image flickering when the light source is not steady but periodical.

For a given light flickering frequency, the band step can be expressed in units of row period.

Band Step = 'period of light intensity' × 'frame rate' × 'rows per frame'.

The band steps for 50Hz and 60Hz light sources can be set in registers {0x3A08[5:0], 0x3A09[7:0]} and {0x3A0A[5:0], 0x3A0B[7:0]}, respectively. Banding mode can be enabled by set 0x3A00[5].

4.6.5 banding mode OFF with AEC

When banding mode is OFF, integration time increases/decreases as normal. It is not necessarily multiples of band steps.

4.6.6 manual exposure control

To manually change exposure value, you must first 0x3503[0] to enable manual exposure control. The exposure value in registers 0x3500~0x3502 is in units of 1/16line. OV5653only supports 0.n line exposure but does not support m.n line exposure, m is positive integer.

4.6.7 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise. Thus, AGC usually starts after AEC is full. However, in cases where adjacent AEC step changes are too large (>1/16), AGC steps should be inserted in between; otherwise, the integration time will keep switching between two adjacent steps and the image flickers.

4.6.8 manual gain control

To manually change gain, first set register bit 0x3503[1] to enable manual control, then change the values in {0x350A[0], 0x350B[7:0]} for the manual gain. The OV5653 has a 16x analog gain.

4.6.9 integration time between 1-16 rows

When integration time is less than 16 rows, the changes between adjacent AEC steps are larger than 1/16, which may possibly make the image oscillate between two AEC levels; thus, some AGC steps are added in between.

4.6.10 gain insertion between AEC banding steps

When banding mode is ON, the integration time changes in step of the period of light intensity. For the first 16 band steps, since the exposure time change between adjacent steps is larger than 1/16, AGC steps are inserted to ensure image stability.

4.6.11 gain insertion between night mode steps

Between night mode steps (e.g., integration time = 1 frame and 2 frames), AGC steps are inserted to ensure no adjacent step change is larger than 1/16.

4.6.12 when AEC reaches maximum

When AEC reaches its maximum step while the image is still too dark, the gain starts to increase until the new frame average falls into the stable range or AGC reaches its maximum step. The AGC ceiling can be set in {0x3A18[9:8], 0x3A19[7:0]}.

table 4-8 AEC registers

address	register name	default value	R/W	description
0x3A00	AEC CTRL00	0x78	RW	Bit[6]: Less one line mode Bit[5]: Band function Bit[2]: Night mode
0x3A02	MAX EXPO 60	0x03	RW	Bit[3:0]: Maximum exposure[19:16] max_expo in unit of 1/16 line
0x3A03	MAX EXPO 60	0xD8	RW	Bit[7:0]: Maximum exposure[15:8] max_expo in unit of 1/16 line
0x3A04	MAX EXPO 60	0x00	RW	Bit[7:0]: Maximum exposure[7:0] max_expo in unit of 1/16 line
0x3A05	AEC CTRL05	0x30	RW	Bit[6]: frame_insert 0: In night mode, insert step based on band 1: In night mode, insert step based on frame
0x3A08	B50 STEP	0x12	RW	Bit[5:0]: b50_step[13:8] b50_step in unit of 1/16 line
0x3A09	B50 STEP	0x70	RW	Bit[7:0]: b50_step[7:0] b50_step in unit of 1/16 line[a]
0x3A0A	B60 STEP	0x0F	RW	Bit[5:0]: b60_step[13:8] b60_step in unit of 1/16 line[a]
0x3A0B	B60 STEP	0x60	RW	Bit[7:0]: b60_step[7:0] b60_step in unit of 1/16 line
0x3A18	AEC GAIN CEILING	0x03	RW	Bit[0]: gain_ceiling[8]
0x3A19	AEC GAIN CEILING	0xE0	RW	Bit[7:0]: gain_ceiling[7:0]

a. The lowest four bits must be zeros, since OV5653 does not support m.n line integration time (m.n are positive integers)

4.7 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration. There are three main functions of the BLC:

- combining two ADC data paths into one data path
- adjusting all normal pixel values based on the values of the black levels
- applying multiplication to all pixel values based on digital gain

The target of BLC level can be set by registers 0x4006 and 0x4007.

table 4-9 BLC control functions

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x09	RW	Bit[0]: BLC enable 0: Disable 1: Enable
0x4006	BLACKLEVEL TARGET	0x00	RW	Bit[1:0]: l_target_blacklevel[9:8]
0x4007	BLACKLEVEL TARGET	0x10	RW	Bit[7:0]: l_target_blacklevel[7:0]

4.8 strobe flash and frame exposure

4.8.1 strobe flash control

The strobe signal is programmable. It supports both LED and Xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB interface. Flash modules are triggered by the rising edge by default or by the falling edge if the signal polarity is changed. It supports the following flashlight modes (see **table 4-10**).

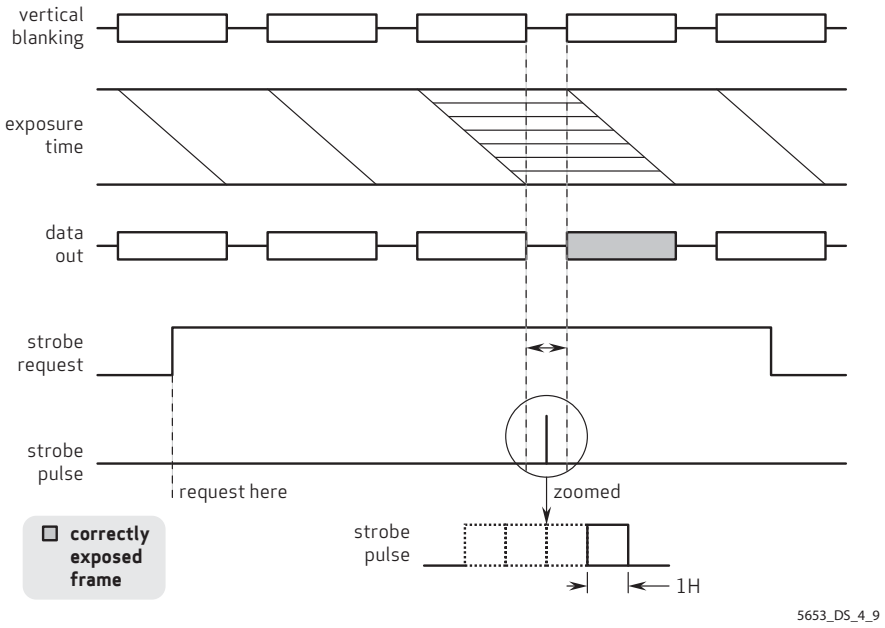
table 4-10 flashlight modes

mode	output	AEC / AGC	AWB
xenon	one-pulse	no	no
LED 1	pulse	no	no
LED 2	pulse	no	yes
LED 3	continuous	yes	yes

4.9 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see **figure 4-9**). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H, depending on register 0x3B00[3:2], where H is one row period.

figure 4-9 xenon flash mode



4.9.1 LED1 & 2 mode

Two frames after the strobe request is submitted, the third frame is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set correctly (see **figure 4-10**). If end request is not sent, the strobe signal is activated intermittently until the strobe end request is set (see **figure 4-11**). The number of skipped frames is programmable using registers {0x3A1C, 0x3A1D}.

figure 4-10 LED 1 & 2 mode - one pulse output

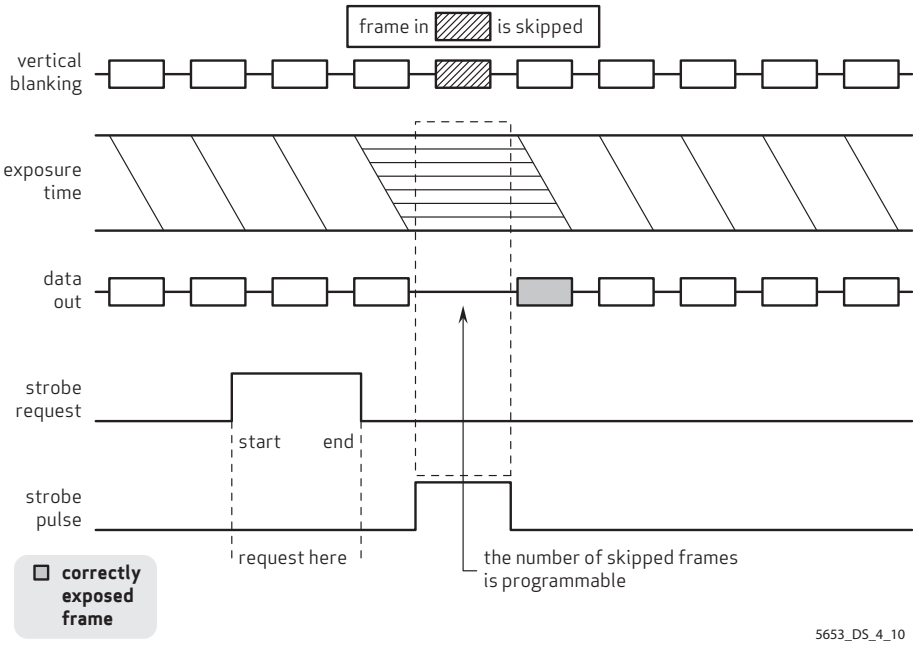
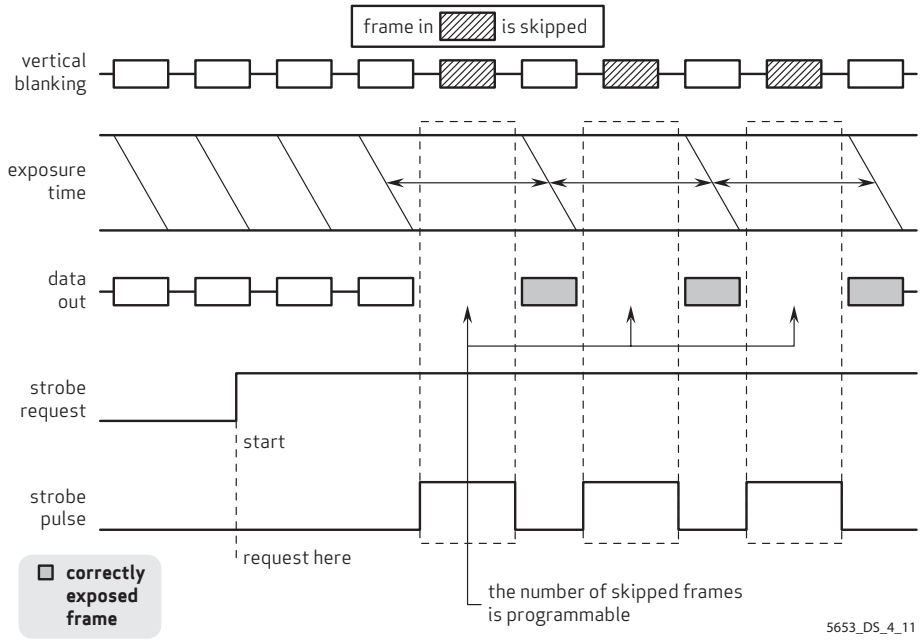


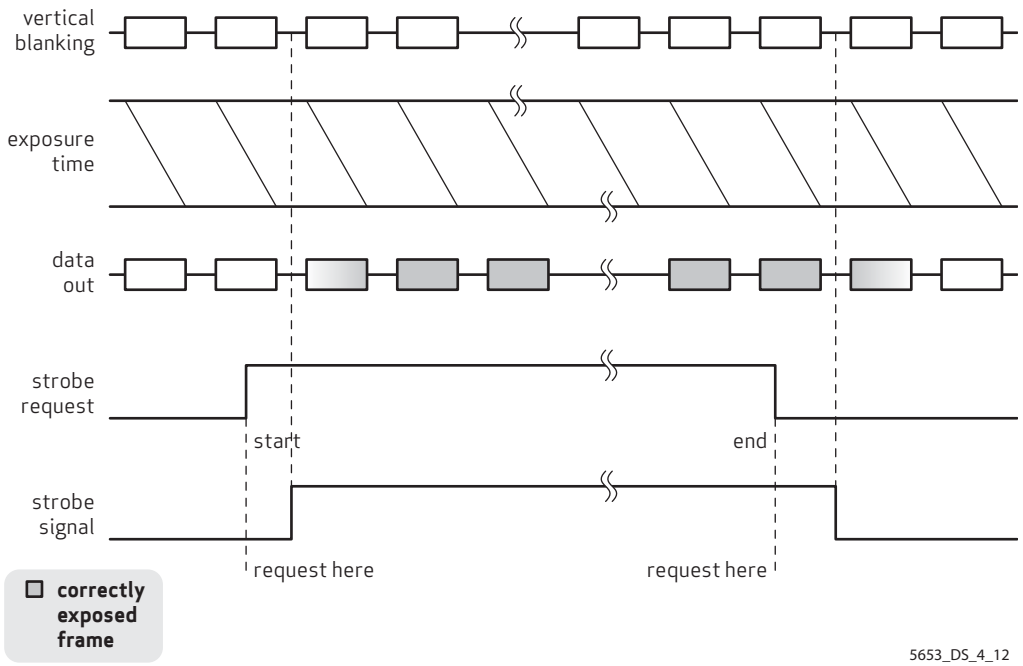
figure 4-11 LED 1 & 2 mode - multiple pulse output



4.9.2 LED 3 mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see **figure 4-12**).

figure 4-12 LED 3 mode



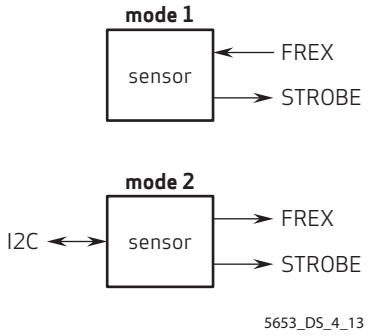
4.10 frame exposure (FREX) mode

4.10.1 FREX control

The OV5653 supports two modes of FREX (see **figure 4-13**). In FREX mode, whole frame pixels start integration at the same time, rather than integrating row by row. After the user-defined exposure time (either by external control in mode 1 or registers {0x3811, 0x3B04, 0x3B05} in mode 2), the shutter closes, preventing further integration and the image begins to read out. After the readout finishes, the shutter opens again and the sensor resumes normal mode, waiting for the next FREX request. In mode 1, the FREX pin is configured as an input while it is configured as an output in mode 2. In both mode 1 and mode 2, the strobe output is irrelevant with the rolling strobe function. The strobe function of rolling shutter mode and FREX/shutter mode do not work at the same time.

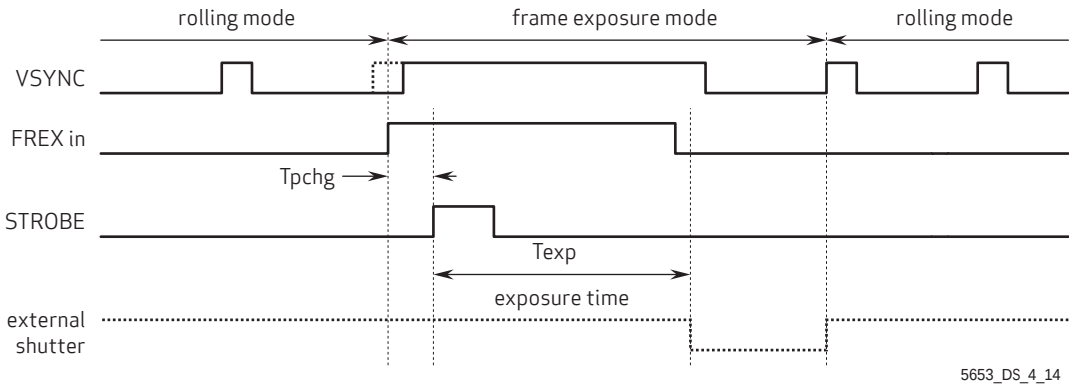
note After frame exposure mode, the first output frame is invalid because of improper exposure during the readout time of the frame exposure image. From the second output frame, the images become normal.

figure 4-13 FREX modes



Mode 1 (see **figure 4-14**) frame exposure and shutter control requests come from the external system via the FREX pin. The sensor will send a strobe output signal to control the flash light.

figure 4-14 FREX mode 1 timing diagram



Example setting:

6C 3B07 08;	FREX mode 1 selection
6C 3017 7F;	FREX mode selection: input
6C 3016 02;	STROBE output enable
6C 3705 D0;	FREX internal timing requirement
6C 370E 08;	FREX internal timing requirement
6C 3709 10;	FREX internal timing requirement
6C 302C 00;	Unlock FREX pin

Mode 2 (see **figure 4-15** and **figure 4-16**) frame exposure request comes from the external system via the I2C register 0x3B08[0]. The sensor outputs two signals, shutter control signal through the FREX pin and strobe signal through the STROBE pin. When the sensor is in FREX mode 2, by default the FREX output signal maintains a high status until the signal is triggered. After trigger the FREX pin outputs a low control signal. The polarity of the FREX output signal can be changed by setting 0x3B07[2] to 1'b1.

Frame exposure time is defined by {0x3811[7:0], 0x3B04[7:0], 0x3B05[7:0]} with one step equal to 128tp/bit. If OV5653 works at 96MHz, each step is equal to 1.33µs and the minimum exposure time is 1.33µs with 0x3811 = 0x00, 0x3B04 = 0x00 and 0x3B05 = 0x01; the maximum exposure time is 22.37s with 0x3811 = 0xFF, 0x3B04 = 0xFF and 0x3B05 = 0xFF.

A shutter delay time is defined by {0x3822[4:0], 0x3823[7:0]} to compensate for the mechanical shutter delay. One step is equal to 128tp/bit. The minimum shutter delay time is 0 with 0x3822 = 0x00 and 0x3823 = 0x00. With PCLK = 96MHz, each step is equal to 1.33µs and the maximum shutter delay is 10.92ms with 0x3822 = 0x1F and 0x3823 = 0xFF.

In **figure 4-15** and **figure 4-16** control of the relationship between shutter delay and the exposure time is realized by the following timing control. For FREXOUT signal, $T_1 - T_0 = T_{exp} + T_{pchg}$; For FTX signal, $T_2 - T_0 = T_{delay}$

table 4-11 FREX mode 2 timing point description

timing point	description
T_0	end of I^2C request
T_1	beginning of FREX output
T_2	beginning of global reset
T_3	end of global reset (beginning of exposure)
T_4	external shutter close (end of exposure)

T_1 may be in front of or behind T_2 based on whether the T_{delay} is longer than $T_{pchg} + T_{exp}$ ($T_1 > T_2$ see **figure 4-15**) or T_{delay} is shorter than $T_{pchg} + T_{exp}$ ($T_1 < T_2$ see **figure 4-16**).

figure 4-15 FREX mode 2 timing diagram (when shutter delay is longer than exposure time)

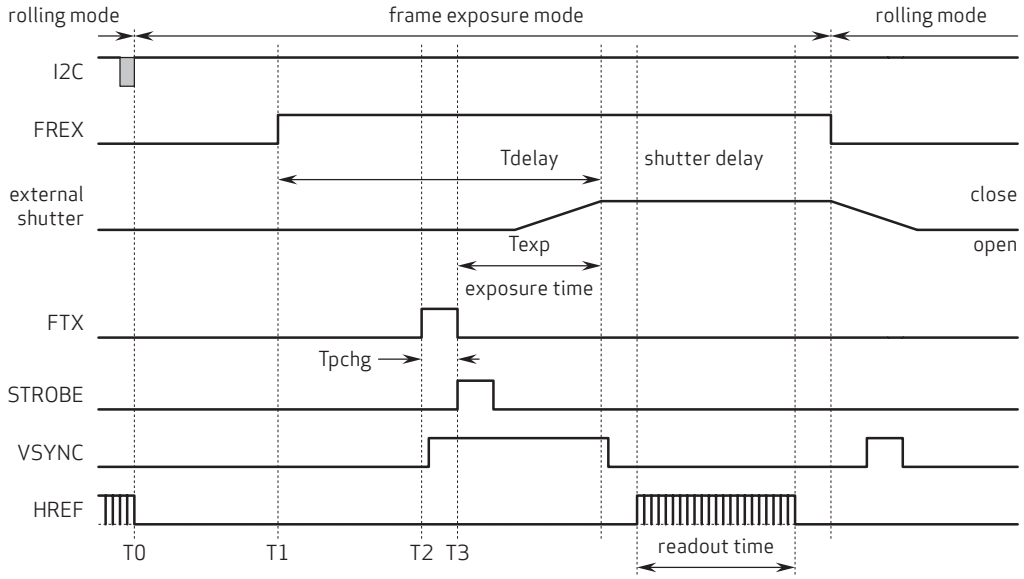
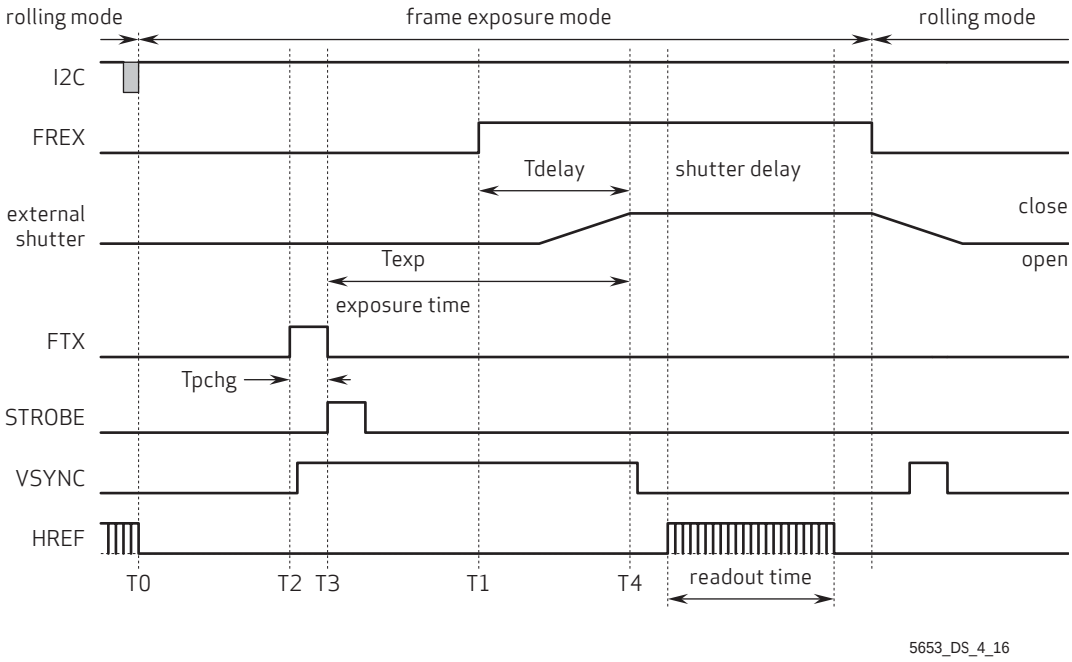


figure 4-16 FREX mode 2 timing diagram (when shutter delay is shorter than exposure time)



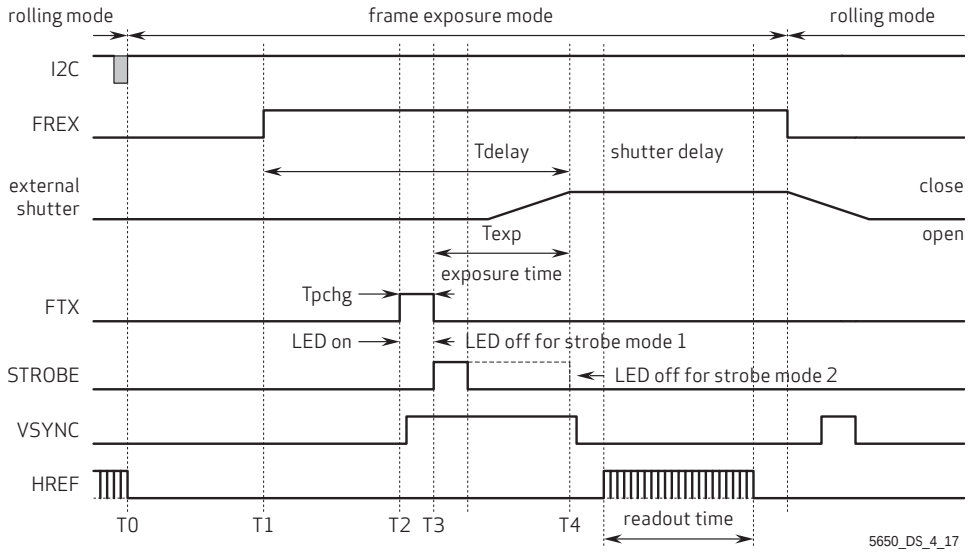
Example setting (see **figure 4-15**):

6C 3B07 0D;	FREX mode 2 selection and FREX polarity selection
6C 3017 FF;	FREX mode selection: output
6C 3016 02;	STROBE output enable
6C 3705 D0;	FREX internal timing requirement
6C 370E 08;	FREX internal timing requirement
6C 3709 10;	FREX internal timing requirement
6C 3811 00;	
6C 3B04 04;	
6C 3B05 00;	with PCLK = 96MHz, exposure time = 1.37ms
6C 3822 08;	
6C 3823 00;	with PCLK = 96MHz, shutter delay = 2.72ms
6C 3B08 01;	I^2C FREX trigger

4.10.2 STROBE control in FREX mode

In FREX mode, two modes of STROBE control are provided in OV5653 (see **figure 4-17**). The first mode provides controllable STROBE output high signal (0x3B06 [4] to 1'b0) from 0 to 15 tp (0x3B06 [3:0]). The second mode provides STROBE output high signal (0x3B06 [4] to 1'b1) during whole exposure period.

figure 4-17 STROBE control in FREX mode



4.11 FREX strobe flash control

See **table 4-12** for FREX strobe control functions.

table 4-12 FREX strobe control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Strobe Control Bit[7]: Strobe request ON/OFF 0: OFF/BLC 1: ON Bit[6]: Strobe pulse reverse Bit[3:2]: width_in_xenon 00: 1H 01: 2H 10: 3H 11: 4H Bit[1:0]: Strobe mode 00: xenon 01: LED 1 10: LED 2 11: LED 3
0x3B06	FREX CTRL	0x04	RW	FREX Control Bit[4]: STROBE mode selection in FREX mode 0: Strobe width controlled by 0x3B06[3:0] 1: Strobe width same as exposure time Bit[3:0]: Strobe width unit is line
0x3B07	FREX MODE SEL	0x08	RW	FREX Mode Select Bit[2]: FREX signal polarity Bit[1:0]: FREX mode select 00: FREX strobe mode 1 01: FREX strobe mode 2 1x: Rolling strobe
0x3B08	FREX EXPLORE REQ	0x00	RW	Strobe FREX Explore Request

table 4-12 FREX strobe control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B09	FREX SHUTTER DELAY	0X02	RW	Bit[2:0]: FREX to first HREF delay (minimum 11.5 lines delay) 000: Minimum lines delay 001: 8 lines delay + minimum lines delay 010: 16 lines delay + minimum lines delay 011: 32 lines delay + minimum lines delay 100: 64 lines delay + minimum lines delay 101: 128 lines delay + minimum lines delay 110: B_FF_FD pixels delay + minimum lines delay 111: F_FF_FF pixels delay + minimum lines delay
0x3016	PAD OUTPUT ENABLE0	0x00	RW	Bit[1]: STROBE output enable
0X3017	SC PAD OEN1	0x00	RW	Input/Output Control (0: input; 1: output) Bit[7]: FREX output enable
0x3817	TIMMING TC REG17	0x24	RW	Timing Control 17 Bit[3]: Sensor output enable before and after frame exposure mode Bit[2:0]: Frame precharge length 000: 1/16 line 001: 1/8 line 010: 1/4 line 011: 1/2 line 100: 1 line 101: 2 line 110: 4 line 111: 8 line
0x3811	R_FRAME_EXP1	0xF0	RW	Bit[7:0]: Frame exposure time[23:16]
0x3B04	R_FRAME_EXP2	0x04	RW	Bit[7:0]: Frame exposure time[15:8]
0x3B05	R_FRAME_EXP3	0x00	RW	Bit[7:0]: Frame exposure time[7:0]
0x3822	R_SHUTTER_DLY	0x03	RW	Bit[4:0]: Shutter delay compensation[12:8]
0x3823	R_SHUTTER_DLY	0x03	RW	Bit[7:0]: Shutter delay compensation[7:0]

4.12 one-time programmable (OTP) memory

The OV5653 supports a maximum of 256 bytes of one-time programmable (OTP) memory to store chip identification and manufacturing information. It can be controlled through the SCCB. **table 4-13** summarizes the corresponding registers.0x3D00 is the sub address, since there are 256 bytes OTP: 0x00: byte 1, 0x01: byte2...0xFF: byte 256. After setting sub address, the data can be loaded and dumped from 0x3D04. 0x00 ~ 0x04 are reserved for OmniVision and 0x05 ~ 0xFF are for customer use.

table 4-13 OTP control registers[a]

address	register name	default value	R/W	description
0x3D00	OTP SUB-ADDRESS	0x00	RW	OTP sub address
0x3D04	OTP DATA	0x00	RW	OTP dump/load data

a. AVDD normal operating voltage range is 2.6V to 3.0V. During OTP programming, an AVDD voltage range of 2.5V ± 10% is required.

Example setting:

Write OTP (write 0xFF into OTP byte 11th; 0xFC into OTP byte 12th)

6C 3D00 10

6C 3D04 FF

6C 3D00 11

6C 3D04 FC

Read OTP (read the values of OTP byte 11th and byte 12th)

6C 3D00 10

6D 3D04

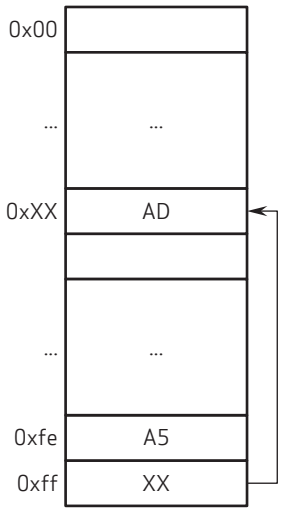
6C 3D00 11

6D 3D04

4.12.1 OTP auto load

OTP memory can be used to automatically load sensor register when power up. In addition, the settings stored in OTP can be manually loaded after power up.

figure 4-18 OTP memory



5650_DS_4_18

If auto load function is used, the data in 0xFE must be 0xA5 as a head byte. Data in 0xFF is the address of the start OTP address where the settings stored. This data, 0xXX can be any number except 0xFE and 0xFF. In the OTP memory following 0xXX, two series of data can be recognized as valid settings:

4.12.1.1 single register write

table 4-14 single register

OTP address	data
0xXX	0xAD
0xXX + 1	address_high_byte
0xXX + 2	address_high_byte
0xXX + 3	data

This series of OTP value will write {data} into register {address_high_byte, address_low_byte}

4.12.1.2 multiple register write

table 4-15 multiple register with address in sequence

OTP address	data
0xXX	0xAD
0xXX+1	address_high_byte
0xXX+2	address_low_byte
0xXX+3	data0
0xXX+4	0x5Y
0xXX+5	data1
…	…
0xXX+4+Y	dataY

This series of OTP value will write {data0, data1,…,dataY} into register {address_high_byte,address_low_byte}, {address_high_byte,address_low_byte+1}…{address_high_byte,address_low_byte+Y},

When power up, the valid setting data stored in the OTP memory starting from the address in 0xFF will be auto loaded. After power up, it is also possible to load settings from any address of OTP specified by the data in 0x31F0. This function is enabled by writing 0x31F1[7] to 1'b0. The loading process can be triggered by first writing 0x3102[2] to 1'b1 then 1'b0. By doing this, several block of settings can be stored and recovered from OTP at any time.

Example settings:

(After writing OTP with following settings, during power up, the register 0x3503 will be set as 0x03. The auto load settings will be saved in the OTP memory beginning with OTP address 0x80.)

6C 3D00 FE

6C 3D04 A5

6C 3D00 FF

6C 3D04 80; specify the OTP starting address for auto load

;single register write

6C 3D00 80

6C 3D04 AD; sign of address

6C 3D00 81

6C 3D04 35; high byte of sensor register address

6C 3D00 82

6C 3D04 03; low byte of sensor register address

6C 3D00 83

6C 3D04 03; value loading into 0x3503

; multi-register write

6C 3D00 87

6C 3D04 AD

6C 3D00 88

6C 3D04 35

6C 3D00 89

6C 3D04 00

6C 3D00 8A

6C 3D04 00

6C 3D00 8B

6C 3D04 52

6C 3D00 8C

6C 3D04 7a

6C 3D00 8D

6C 3D04 A0

(After power up, with the following setting, the registers 0x3500, 0x3501 and 0x3502 will be set as 0x00, 0x7A and 0xA0)

6C 31F0 87; specify the starting OTP address

6C 31F1 10; clear bit 7

6C 3102 04; trigger the OTP load

6C 3102 00; trigger the OTP load

table 4-16 OTP control functions

address	register name	default value	R/W	description
0x31F0	OTP LD START ADDRESS	0x00	RW	OTP Manual Load Start Address
0x31F1	OTP DELAY	0x90	RW	Strobe Control Bit[7]: OTP Manual load start address disable 0: Enable 1: Disable

5 image sensor processor digital functions

5.1 ISP general controls

table 5-1 ISP general control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x86	RW	Bit[7]: lenc_en 0: Disable 1: Enable Bit[2]: bc_en 0: Disable 1: Enable Bit[1]: wc_en 0: Disable 1: Enable
0x5001	ISP CTRL01	0x01	RW	Bit[0]: awb_en 0: Disable 1: Enable
0x5002	ISP CTRL02	0x00	RW	Bit[1]: vap_en 0: Disable 1: Enable
0x5025	ISP CTRL25	0x00	RW	Bit[1:0]: avg_sel 00: Inputs of average module are from WINC 01: Inputs of average module are from VAP 10: Inputs of average module are from AWBG 11: Inputs of average module are from LENC
0x503D	ISP CTRL3D	0x00	RW	Bit[7]: test_pattern_en 0: Disable 1: Enable Bit[6]: rnd_same 0: Frame-changing random data pattern 1: Frame-fixed random data pattern Bit[5:4]: bar_style When set to different value, the different type color bar will be output Bit[2]: rolling_bar 0: Disable rolling bar 1: Enable rolling bar

table 5-1 ISP general control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x503E	ISP CTRL3E	0x00	RW	Bit[7:4]: rnd_seed Initial seed for random data pattern Bit[3]: squ_bw_mode 0: Output square is color square 1: Output square is black-white square Bit[2]: transparent_mode 0: Disable 1: Enable Bit[1:0]: test_pattern_type 00: Color bar 01: Square 10: Random data 11: Input data
0x5046	ISP CTRL46	0x09	RW	Bit[3]: awbg_en 0: Disable 1: Enable Bit[0]: isp_en 0: Disable 1: Enable

5.2 lens correction (LENC)

The main purpose of the LENC is to compensate for lens imperfection. According to the area where each pixel is located, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature. The LENC correcting curve automatic calculation according sensor gain is also added so that the LENC can adapt with the sensor gain. Also, the LENC supports the subsample function in both horizontal and vertical directions.

table 5-2 LENC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x86	RW	Bit[7]: lenc_en 0: Disable 1: Enable
0x505A	ISP LENC OFFX MAN	0x00	RW	Bit[3:0]: LENC x_offset manual high byte[11:8]
0x505B	ISP LENC OFFX MAN	0x00	RW	Bit[7:0]: LENC x_offset manual low byte[7:0]

table 5-2 LENC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x505C	ISP LENC OFFY MAN	0x00	RW	Bit[3:0]: LENC y_offset manual high byte[11:8]
0x505D	ISP LENC OFFY MAN	0x00	RW	Bit[7:0]: LENC y_offset manual low byte[7:0]
0x5800~ 0x5823	GMTRX	–	RW	Bit[6:0]: green_matrix
0x5824~ 0x583C	BMTRX	–	RW	Bit[4:0]: blue_matrix
0x583D~ 0x5855	RMTRX	–	RW	Bit[4:0]: red_matrix
0x5856	MAX GAIN	0x40	RW	Bit[7:0]: max_gain
0x5857	MIN GAIN	0x20	RW	Bit[7:0]: min_gain
0x5858	MIN Q	0x18	RW	Bit[6:0]: min_q
0x5859	LENC CTRL59	0x0D	RW	Bit[3]: ADDBLC 0: Disable BLC add back function 1: Enable BLC add back function Bit[2]: blc_en 0: Disable BLC function 1: Enable BLC function Bit[0]: autoq_en 0: Used constant Q (0x40) 1: Used calculated Q
0x585A	BR HSCALE	0x01	RW	Bit[3:0]: br_hscale[11:8] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x585B	BR HSCAL	0x2B	RW	Bit[7:0]: br_hscale[7:0] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x585C	BR VSCALE	0x01	RW	Bit[2:0]: br_vscale[10:8] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block

table 5-2 LENC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x585D	BR VSCALE	0x92	RW	Bit[7:0]: br_vscale[7:0] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x585E	G HSCALE	0x01	RW	Bit[3:0]: g_hscale[11:8] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x585F	G HSCAL	0x8F	RW	Bit[7:0]: g_hscale[7:0] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5860	G VSCALE	0x01	RW	Bit[2:0]: g_vscale[10:8] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5861	G VSCALE	0x0C	RW	Bit[7:0]: g_vscale[7:0] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block

5.3 defect pixel cancellation (DPC)

Due to processes and other reasons, pixel defects in the sensor array will occur. Thus, these bad or wounded pixels will generate wrong color values. The main purpose of Defect Pixel Cancellation (DPC) function is to remove the effect caused by these bad or wounded pixels. Also, some special functions are available for those pixels located at the image boundary. To remove the defect pixel effect correctly, the proper threshold should first be determined.

table 5-3 defect pixel cancellation registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x86	RW	Bit[2]: bc_en Black pixel correction enable 0: Disable 1: Enable Bit[1]: wc_en White pixel correction enable 0: Disable 1: Enable
0x5780	DPC CTRL00	0x77	RW	Bit[2]: smooth_en Enable using average G values when doing recovery Bit[1]: sc_en 0: Disable same channel detection 1: Enable same channel detection Bit[0]: dc_en 0: Disable different channel detection 1: Enable different channel detection
0x5781	DPC THRE	0x30	RW	Bit[7:0]: thre Threshold value used in recovery
0x5784	DPC CTRL02	0x03	RW	Bit[2:0]: gainbd_pwr[2:0] Range in [0, 5]
0x5785	RSVD	–	–	Reserved
0x5786	DPC GAIN LIST1	0x08	RW	Bit[6:0]: gain_list1[6:0] Used in auto mode
0x5787	DPC GAIN LIST2	0x20	RW	Bit[6:0]: gain_list2[6:0] Used in auto mode
0x5788	DPC WTHRE LIST0	0x20	RW	Bit[6:0]: wthre_list0[6:0] Used for wthre calculation in auto mode

table 5-3 defect pixel cancellation registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5789	DPC WTHRE LIST1	0x18	RW	Bit[6:0]: wthre_list1[6:0] Used for wthre calculation in auto mode
0x578A	DPC WTHRE LIST2	0x08	RW	Bit[6:0]: wthre_list2[6:0] Used for wthre calculation in auto mode
0x578B	DPC WTHRE LIST3	0x04	RW	Bit[6:0]: wthre_list3[6:0] Used for wthre calculation in auto mode
0x578C	DPC BTHRE LIST0	0x40	RW	Bit[7:0]: bthre_list0[7:0] Used for bthre calculation in auto mode
0x578D	DPC BTHRE LIST1	0x20	RW	Bit[7:0]: bthre_list1[7:0] Used for bthre calculation in auto mode
0x578E	DPC BTHRE LIST2	0x08	RW	Bit[7:0]: bthre_list2[7:0] Used for bthre calculation in auto mode
0x578F	DPC BTHRE LIST3	0x04	RW	Bit[7:0]: bthre_list3[7:0] Used for bthre calculation in auto mode

5.4 auto white balance (AWB)

The main function of Auto White Balance (AWB) is the process of removing unrealistic color casts so that objects which appear white in person are rendered white in the image or video. Thus, the AWB makes sure that the white color is always a white color in different color temperatures. It supports manual white balance and auto white balance. For auto white balance, simple AWB is supplied. For auto white balance, the adjust option is also provided for the customer.

table 5-4 AWB control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x01	RW	Bit[0]: awb_en 0: Disable 1: Enable
0x5046	ISP CTRL46	0x09	RW	Bit[3]: awb_gain_en 0: Disable 1: Enable
0x5180	AWB CTRL	0x00	RW	Bit[6]: fast_awb 0: Disable fast AWB calculation function 1: Enable fast AWB calculation function
0x5181	AWB DELTA	0x20	RW	Bit[5:0]: awb_delta Delta value to increase or decrease the gains
0x5182	STABLE RANGE	0x04	RW	Bit[7:0]: stable_range
0x5183	STABLE RANGEW	0x08	RW	Bit[7:0]: stable_rangew Wide stable range
0x5184	FRAME CNT	0x02	RW	Bit[3:0]: frame_cnt AWB is updated once every frame_cnt frames
0x518C	RED GAIN LIMIT	0xF0	RW	Bit[7:4]: red_gain_up_limit Bit[3:0]: red_gain_dn_limit They are only the highest 4 bits of limitation. Max red gain is {red_gan_up_limit,ff} Min red gain is {red_gain_dn_limit,00}

table 5-4 AWB control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x518D	GREEN GAIN LIMIT	0xF0	RW	Bit[7:4]: green_gain_up_limit Bit[3:0]: green_gain_dn_limit They are only the highest 4 bits of limitation. Max green gain is {green_gan_up_limit,ff} Min green gain is {green_gain_dn_limit,00}
0x518E	BLUE GAIN LIMIT	0xF0	RW	Bit[7:4]: blue_gain_up_limit Bit[3:0]: blue_gain_dn_limit They are only the highest 4 bits of limitation. Max blue gain is {blue_gan_up_limit,ff} Min blue gain is {blue_gain_dn_limit,00}
0x3400	AWB RED GAIN	0x04	RW	Bit[3:0]: RED gain[11:8]
0x3401	AWB RED GAIN	0x00	RW	Bit[7:0]: RED gain[7:0]
0x3402	AWB GREEN GAIN	0x04	RW	Bit[3:0]: GREEN gain[11:8]
0x3403	AWB GREEB GAIN	0x00	RW	Bit[7:0]: GREEN gain[7:0]
0x3404	AWB BLUE GAIN	0x04	RW	Bit[3:0]: BLUE gain[11:8]
0x3405	AWB BLUE GAIN	0x00	RW	Bit[7:0]: BLUE gain[7:0]
0x3406	AWB MANUAL CTRL	0x00	RW	Bit[0]: AWB gain manual control enable

5.5 VarioPixel (VAP)

The VarioPixel™ module can decrease the width of the original image by 1/2 or 1/4. It supports three modes which selects either the first, second, or average value of a pair of pixels to compose the new image.

table 5-5 defect pixel cancellation registers

address	register name	default value	R/W	description
0x5002	ISP CTRL02	0x02	RW	Bit[2]: vap_en 0: Disable debug mode 1: Enable debug mode
0x5900	VAP CTRL00	0x01	RW	Bit[5]: sum_en for even-line and even-column pixels 0: Drop mode 1: Sum mode Bit[4]: sum_en for even-line and odd-column pixels 0: Drop mode 1: Sum mode Bit[3]: sum_en for odd-line and even-column pixels 0: Drop mode 1: Sum mode Bit[2]: sum_en for odd-line and odd-column pixels 0: Drop mode 1: Sum mode Bit[1]: hsub4_drop_mode 0: Output first pixel of first group and second pixel of third group This option only plays its role in 1:4 horizontal sub-sample drop mode 1: Output the first group of 4 group Bit[0]: avg_en 0: Limitation mode 1: Average mode
0x5901	VAP CTRL01	0x00	RW	Bit[3:2]: hsub_coef Horizontal sub-sample coefficient 00: Sub-sample 1 01: Sub-sample 2 1x: Sub-sample 4 Bit[1:0]: vsub_coef Vertical sub-sample coefficient Changing this value is not recommended 00: Sub-sample 1 01: Sub-sample 2 1x: Sub-sample 4

6 image sensor output interface digital functions

6.1 system control

System control registers include clock, reset control, and PLL configure. Individual modules can be reset or clock gated by setting the appropriate registers.

table 6-1 system control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x3000	SYSTEM RESET00	0x20	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset BIST Bit[6:5]: Not used Bit[4]: Reset OTP memory Bit[3]: Reset STB Bit[2]: Reset 5060Hz Bit[1]: Reset timing control Bit[0]: Reset array control
0x3001	SYSTEM RESET01	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset AWB registers Bit[6]: Not used Bit[5]: Reset ISP Bit[4]: Reset FC Bit[3]: Reset CIF Bit[2]: Reset BLC Bit[1]: Reset AEC registers Bit[0]: Reset AEC
0x3002	SYSTEM RESET02	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset VFIFO Bit[6]: Not used Bit[5]: Reset FORMAT Bit[4:1]: Not used Bit[0]: Reset average
0x3003	SYSTEM RESET03	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[3]: Reset MIPI receiver Bit[2]: Reset ISP FC Bit[1]: Reset MIPI Bit[0]: Reset DVP

table 6-1 system control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x3004	CLOCK ENABLE00	0xDF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable BIST clock Bit[6:5]: Not used Bit[4]: Enable OTP clock Bit[3]: Enable strobe clock Bit[2]: Enable 5060 Hz detection clock Bit[1]: Enable timing control clock Bit[0]: Enable array control clock
0x3005	CLOCK ENABLE01	0xFF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable AWB register clock Bit[6]: Not used Bit[5]: Enable ISP clock Bit[4]: Enable FC clock Bit[3]: Enable CIF clock Bit[2]: Enable BLC clock Bit[1]: Enable AEC register clock Bit[0]: Enable AEC clock
0x3006	CLOCK ENABLE02	0xFF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Not used Bit[6]: Enable format clock Bit[5:1]: Not used Bit[0]: Enable average clock
0x3007	CLOCK ENABLE03	0x3F	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[5]: Enable ISP_FC clock Bit[4]: Enable MIPI PCLK clock Bit[3]: Enable MIPI clock Bit[2]: Enable DVP clock Bit[1]: Enable VFIFO PCLK clock Bit[0]: Enable VFIFO SCLK clock
0x3008	SYSTEM CTRL0	0x02	RW	Bit[7]: Reset registers Bit[6]: Register power down Bit[5]: Not used Bit[4]: sc_srb_clk_syn_en Bit[3]: iso_susp_sel_o Bit[2]: MIPI_rst_msk_o Bit[1]: MIPI_susp_msk_o Bit[0]: MIPI_rst_sel_o
0x3009	SC_MIPI_PCLK_DIV_CTRL	0x01	RW	Bit[7]: MIPI_pdiv_sepa Bit[6]: Not used Bit[5:0]: MIPI PCLK divider
0x300A	CHIP ID	–	R	Chip ID High Byte

table 6-1 system control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x300B	CHIP ID	–	R	Chip ID Low Byte
0x300C	RSVD	–	–	Reserved
0x300D	SC_SD_SDIV	0x22	RW	Bit[2:0]: r_sdiv, divider for 50/60 detection
0x300E	SC_MIPI_SC_CTRL0	0x18	RW	Bit[7:5]: Not used Bit[4]: r_phy_pd_MIPI 1: Power down PHY HS TX Bit[3]: r_phy_pd_lprx 1: Power down PHY LP RX module Bit[2]: MIPI_en 0: DVP enable 1: MIPI enable Bit[1]: MIPI_susp_reg 1: MIPI system suspends registers Bit[0]: lane_dis_op 0: Use ~MIPI release 1/2 and lane_disable 1/2 to disable two data lanes 1: Use lane disable 1/2 to disable two data lane
0x300F	PLL CTRL 00	0x8E	RW	Bit[7:6]: R_SELD5 00: Bypass 01: Divide by 1 10: Divide by 4 11: Divide by 5 Bit[5:3]: Debug mode Bit[2]: R_DIVL 0: One lane, divide by 2 1: Two lanes, divide by1 Bit[1:0]: R_SELD2P5 00: Bypass 01: Divide by 1 10: Divide by 2 11: Divide by 2.5
0x3010	PLL CTRL 01	0x10	RW	Bit[7:4]: R_DIVS, Sdiv Bit[3:0]: R_DIVM, Mdiv
0x3011	PLL CTRL 02	0x10	RW	Bit[7]: PLL bypass Bit[5:0]: R_DIVP, pll_div

table 6-1 system control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x3012	PLL CTRL 03	0x02	RW	Bit[2:0]: R_PREDIV 000: Divide by 1 001: Divide by 1.5 010: Divide by 2 011: Divide by 2.5 100: Divide by 3. 101: Divide by 4 110: Divide by 6 111: Divide by 8
0x3015	RSVD	–	–	Reserved
0x3016	PAD OUTPUT ENABLE0	0x00	RW	Bit[1]: STROBE output enable Bit[0]: SIOD output enable
0x3017	PAD OUTPUT ENABLE1	0x00	RW	Bit[7]: FREX output enable Bit[6]: VSYNC output enable Bit[5]: HREF output enable Bit[4]: PCLK output enable Bit[3:0]: D[9:6] output enable
0x3018	PAD OUTPUT ENABLE2	0x00	RW	Bit[7:2]: D[5:0] output enable
0x3019	PAD OUTPUT0	0x00	RW	Bit[1]: STROBE Bit[0]: SIOD
0x301A	PAD OUTPUT1	0x00	RW	Bit[7]: FREX Bit[6]: VSYNC Bit[5]: HREF Bit[4]: PCLK Bit[3:0]: D[9:6]
0x301B	PAD OUTPUT2	0x00	RW	Bit[7:2]: D[5:0]
0x301C	PAD SELECT 0	0x00	RW	Bit[1]: I/O STROBE select Bit[0]: I/O SIOD select
0x301D	PAD SELECT 1	0x00	RW	Bit[7]: I/O FREX select Bit[6]: I/O VSYNC select Bit[5]: I/O HREF select Bit[4]: I/O PCLK select Bit[3:0]: I/O D[9:6] select
0x301E	PAD SELECT 2	0x00	RW	Bit[7:2]: I/O D[5:0] select
0x301F	SRAM0 SELECT	0x00	RW	System Control Selects SRAM0
0x3020	SRAM1 SELECT	0x00	RW	System Control Selects SRAM1
0x3021	SRAM2 SELECT	0x00	RW	System Control Selects SRAM2
0x3022	SRAM TEST VALUE0	0xFF	RW	System SRAM Test Value 0

table 6-1 system control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x3023	SRAM TEST VALUE1	0x09	RW	System SRAM Test Value 1
0x3024~ 0x302B	RSVD	–	–	Reserved
0x302C	SYSTEM PAD CTRL	0x02	RW	Bit[7]: pd_dato_en Bit[6:3]: iP2X3v[3:0] Bit[2]: man_rst_pon Bit[1]: FREX enable, active low
0x302D	SYSTEM MIPI CTRL1	0x10	RW	Bit[7:6]: High speed common mode voltage Bit[5:4]: Driving strength of low speed transmitter Bit[3]: Bias current reduction Bit[2]: CD input low voltage Bit[1]: CD input high voltage-dummy Bit[0]: Valid delay-dummy
0x302E	SYSTEM MIPI CTRL 0	0x00	RW	Bit[2]: Bypass the latch of hs_enable Bit[1:0]: Bias current adjustment
0x302F	DVP CCLK DIV	0x02	RW	System DVP CCLK divider Bit[5:0]: Divider for external CCLK
0x3030	POWER CTRL 0	0x00	RW	sc_a_pwc_pk_o[7:0] Bit[7]: bp_npump Bypass N pump Bit[6]: bp_ppump Bypass P pump Bit[5]: Bypass regulator Bit[4]: Bypass small regulator Bit[3:0]: dio[3:0]
0x3031	POWER CTRL 1	0x00	RW	sc_a_pwc_pk_o[15:8] Bit[7:4]: vrbg[3:0] Bit[2]: pd_bias Bit[1]: pd_other Bit[0]: pd_vmrst
0x3032	POWER CTRL 2	0x00	RW	sc_a_pwc_pk_o[23:16] Bit[3:0]: vrbglp[3:0] bandgap_lp trimming bits
0x3033	SC_RSV0	0x03	RW	Bit[4]: dis_srb_rst_o Disable reset for SRB when clock switches, active high Bit[1]: frex_ef_sel Bit[0]: cen_global_o
0x3034	SC_MARK1_CNT	0x10	RW	MIPI ULPS Resume Mark1 Detect Length

table 6-1 system control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x3035	SC_FREX_RST_MASK0	0xFF	RW	Bit[7]: frex_mask_aec Bit[6]: frex_mask_blc Bit[5]: frex_mask_tc Bit[4]: frex_mask_isp_fc Bit[3]: frex_mask_isp Bit[1]: frex_mask_avg
0x3036	SC_FREX_RST_MASK1	0x00	RW	Bit[3]: frex_mask_vfifo Bit[2]: frex_mask_dvp Bit[1]: frex_mask_MIPI Bit[0]: frex_mask_MIPI_phy
0x3037	RSVD	–	–	Reserved
0x3040	SC_IO_PAD_IN0	–	R	sc_io_pad_in[23:16]
0x3041	SC_IO_PAD_IN1	–	R	sc_io_pad_in[15:8]
0x3042	SC_IO_PAD_IN2	–	R	sc_io_pad_in[7:0]
0x3043	SC_IO_PAD_IN3	–	R	sc_io_pad_in[31:24]

6.2 SCCB

table 6-2 system control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3100	SCCB ID	0x6C	RW	SCCB Slave ID
0x3101	SCCB CTRL	0x03	RW	Bit[1]: en_ss_addr_inc Bit[0]: sccb_en_o
0x3102	SCCB_SYSREG	0x00	RW	For SCCB Access Only Bit[6]: ctrl_rst_MIPIsc Bit[5]: ctrl_rst_srb Bit[4]: ctrl_rst_sccb_s Bit[3]: ctrl_rst_pon_sccb_s Bit[2]: ctrl_rst_clkmod Bit[1]: ctrl_MIPI_phy_rst_o Bit[0]: ctrl_pll_rst_o

table 6-2 system control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3103	SCCB_PWUP_DIS	0x91	RW	For SCCB Access Only Bit[7]: pad_no_sda_oen Bit[4]: r_srb_clk_syn_en Bit[3]: pwup_dis2 Bit[2]: pwup_dis1 Bit[1]: PLL clock select 0: System clock from PAD 1: System clock from PLL Bit[0]: pwup_dis0
0x3104	SCCB_PADCLK_DIV	0x01	RW	For SCCB Access Only Bit[5:0]: padclk_div
0x3105	SCCB_SRB_HOST_ INPUT_DIS	0xFF	RW	For SCCB Access Only Bit[7]: ctrl_reg_ms Bit[6]: ctrl_awb_done Bit[5]: ctrl_vts_done Bit[4]: ctrl_agc_done Bit[3]: ctrl_aec_done Bit[2]: ctrl_MIPI_host Bit[0]: ctrl_bist_host
0x3106	R_WS_BEGIN	0x03	RW	R_WS_BEGIN
0x3107	R_WS_WIDTH	0x03	RW	R_WS_WIDTH
0x3108	SCCB_PRE_CONTRL	0x00	RW	Bit[7]: bypass_start_stop Bit[6:5]: serial_signal_dly2_dly3_dly4_ select 00: dly2d 01: dly3d 1x: dly4d Bit[4]: bypass_filter Bit[3:0]: gate_glitch_width
0x3109	SCCB_PRE_START_ STOP_CONTRL	0x03	RW	Bit[3:0]: start_top_ctrl
0x310A	SCCB_CTRL_OPTION	0x1D	RW	Bit[4:3]: r_reload_ctrl Bit[2]: r_msk_glitch Bit[1]: r_bit8_adr_en Bit[0]: r_msk_stop
0x310B	SCCB_FILTER	0x00	RW	Bit[7:4]: r_sda_num Bit[3:0]: r_scl_num
0x31F0	CS_OTP_LD_ST_ADDR	0x00	RW	Bit[7:0]: OTP ID start address
0x31F1	CS_OTP_DELAY	0x90	RW	Bit[7:0]: OTP delay
0x31FF	CS_SCCB	0x01	RW	Bit[0]: SCCB select 0: Old SCCB 1: New SCCB

6.3 group hold

table 6-3 group hold control registers

address	register name	default value	R/W	description
0x3200	SRM_GRUP_ADR0	0x00	RW	srm_group_adr0
0x3201	SRM_GRUP_ADR1	0x40	RW	srm_group_adr1
0x3202	SRM_GRUP_ADR2	0x80	RW	srm_group_adr2
0x3203	SRM_GRUP_ADR3	0xC0	RW	srm_group_adr3
0x3204~ 0x320A	RSVD	–	–	Reserved
0x320B	SRM_GRUP_LEN0	0x00	RW	srm_group_len0
0x320C	SRM_GRUP_LEN1	0x00	RW	srm_group_len1
0x320D	SRM_GRUP_LEN3	0x00	RW	srm_group_len2
0x320E	SRM_GRUP_LEN3	0x00	RW	srm_group_len3
0x320F~ 0x3211	GROUP WRITE CONTROL REGISTERS	–	–	Group Write Register Changing these values is not recommended
0x3212	SRM_GRUP_ACCESS	0x00	W	Bit[7]: group_hold Bit[6]: group_access_tm Bit[5]: group_launch Bit[4]: group_hold_end Bit[3:0]: group_id, 0~3 (groups for register access)
0x3213	SRM_GRUP_STATUS	–	R	Bit[7]: Store default Bit[6]: Restore Bit[5]: grp_hold Bit[4]: grp_launch Bit[3]: grp_write_o Bit[2:0]: grp_sel
0x3214	SRM_RAM_CTRL	0x00	RW	Bit[6]: sel_iso 1: Enable iso recover at power down mode Bit[5]: sram_clk Bit[4]: sram_rst Bit[3]: sram_cen Bit[2]: sram_wen Bit[1]: sram_dat Bit[0]: sram_adr

6.4 PRAM_MC_PRAM_CTRLL

table 6-4 PRAM_MC_PRAM_CTRLL control registers

address	register name	default value	R/W	description
0x3300	PRAM_MC_PRAM_ CTRL1	0x00	RW	Bit[6]: sel_iso_in_sleep Bit[5]: iso_clk_in_sleep Bit[4]: iso_rst_in_sleep Bit[3]: iso_cen_in_sleep Bit[2]: iso_wen_in_sleep Bit[1]: iso_dat_in_sleep Bit[0]: iso_adr_in_sleep

6.5 timing control

table 6-5 timing control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3800	TIMING HS	0x01	RW	HREF Start Point Bit[3:0]: timing_hs[11:8]
0x3801	TIMING HS	0xB4	RW	HREF Start Point Bit[7:0]: timing_hs[7:0]
0x3802	TIMING VS	0x00	RW	VREF Start Point Bit[3:0]: timing_vs[11:8]
0x3803	TIMING VS	0x0A	RW	VREF Start Point Bit[7:0]: timing_vs[7:0]
0x3804	TIMING HW	0x0A	RW	HREF Width Bit[3:0]: Timing_hw[11:8]
0x3805	TIMING HW	0x20	RW	HREF Width Bit[7:0]: timing_hw[7:0]
0x3806	TIMING VH	0x07	RW	VREF Height Bit[3:0]: timing_vh[11:8]
0x3807	TIMING VH	0x98	RW	VREF Height Bit[7:0]: timing_vh[7:0]
0x3808	TIMING DVP HO	0x0A	RW	DVP Horizontal Output Size Bit[3:0]: timing_dvpho[11:8]
0x3809	TIMING DVP HO	0x20	RW	DVP Horizontal Output Size Bit[7:0]: timing_dvpho[7:0]

table 6-5 timing control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x380A	TIMING DVP VO	0x07	RW	DVP Vertical Output Size Bit[3:0]: timing_dvpvo[11:8]
0x380B	TIMING DVP VO	0x98	RW	DVP Vertical Output Size Bit[7:0]: timing_dvpvo[7:0]
0x380C	TIMING HTS	0x0C	RW	Total Horizontal Size Bit[4:0]: timing_hts[12:8]
0x380D	TIMING HTS	0x2C	RW	Total Horizontal Size Bit[7:0]: timing_hts[7:0]
0x380E	TIMING VTS	0x07	RW	Total Vertical Size Bit[3:0]: timing_vts[11:8]
0x380F	TIMING VTS	0xB0	RW	Total Vertical Size Bit[7:0]: timing_vts[7:0]
0x3810	TIMING HVOFFS	0xC2	RW	Bit[7:4]: hoffs[3:0] Bit[3:0]: voffs[3:0]
0x3811~ 0x3813	GROUP TIMING CONTROL REGISTERS	–	–	Timing Control Registers
0x3814	TIMING TC REG 14	0x01	RW	Bit[7]: ext_vs_re Bit[6]: ext_yuv422_en Bit[5]: ext_snr_en Bit[4:0]: External PCLK to SCLK ratio
0x3815	TIMING TC REG 15	0x02	RW	Bit[7]: dvpshp Bit[5]: rip_sof_en Bit[4:0]: PCLK to SCLK ratio
0x3816	TIMING TC REG 16	0x0A	RW	SOF to HREF Delay (number of pixel count)
0x3817	TIMING TC REG 17	0x24	RW	Bit[7:4]: vs_int_r Origin of timing Bit[3]: Frame exposure HREF Bit[2:0]: Frame precharge length
0x3818	TIMING TC REG 18	0x80	RW	Bit[7]: dkhf Bit[6]: mirror Bit[5]: vflip Bit[1]: vsub4 Bit[0]: vsub2

table 6-5 timing control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3819	TIMING TC REG 19	0x80	RW	Bit[7:4]: SOF to HREF delay (number of line count) Bit[3]: vfifo_hsize_sel Bit[2]: vfifo_vsize_sel Bit[1:0]: vts_ctrl 00: From vts_aeclat 01: From reg_vts 10: From vts_i 11: From vts_vs
0x381A	TIMING TC HS MIRR ADJ	0x00	RW	Bit[7]: hs_mirror_offset_cs 0: Add hs_mirror_offset 1: Subtract hs_mirror_offset Bit[6:0]: hs_mirror_offset
0x381B	TIMING TC VS FLIP ADJ	0x00	RW	Bit[7]: vs_flip_offset_cs 0: Add vs_flip_offset 1: Subtract vs_flip_offset Bit[6:0]: vs_flip_offset
0x381C	TIMING TC REG 1C	0x20	RW	Bit[7]: VGA preview md Bit[6]: first_l Bit[5]: en_fram_mask_for_grp_wr Bit[4]: r_crop_en Bit[3:0]: tc_vs_crop_h
0x381D	TIMING TC VS CROP L	0x0A	RW	Bit[7:0]: tc_vs_crop_l
0x381E	TIMING TC VH CROP	0x01	RW	Bit[3:0]: vh_crop_h
0x381F	TIMING TC VH CROP	0x20	RW	Bit[7:0]: vh_crop_l
0x3820	TIMING TC REG 20	0x00	RW	Bit[7]: Enable HS crop via x_address Bit[6]: xaddr_hrefB Bit[4:0]: tc_hs_crop[7:0]
0x3821	TIMING TC REG 21	0x00	RW	Bit[5:0]: tc_hw_crop[5:0]
0x3824	TIMING HREFST MAN HIGH	0x01	RW	Bit[5]: hvs_man Bit[4:0]: hrefst_man_h
0x3825	TIMING HREFST MAN LOW	0xB4	RW	Bit[7:0]: hrefst_man_l
0x3826	TIMING VREF1 ST MAN HIGH	0x00	RW	Bit[7:0]: vref1_man_h[15:8]
0x3827	TIMING VREF1 ST MAN LOW	0x0A	RW	Bit[7:0]: vref1_man_l[7:0]
0x3828	TIMING SNR X OFFSET	–	R	Sensor X Offset High Byte
0x3829	TIMING SNR X OFFSET	–	R	Sensor X Offset Low Byte
0x382A	TIMING SNR Y OFFSET	–	R	Sensor Y Offset High Byte
0x382B	TIMING SNR Y OFFSET	–	R	Sensor Y Offset Low Byte

table 6-5 timing control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x382C	TIMING HSYNC START	0x00	RW	Bit[3:0]: hsync_start_h
0x382D	TIMING HSYNC START	0x00	RW	Bit[7:0]: hsync_start_l
0x382E	TIMING HSYNC WIDTH	0x00	RW	HSYNC Width
0x3830	TIMING TC REG 30	0x50	RW	Bit[7]: Digtal gain manual enable Bit[6]: Digital gain sel In OV5650, Please fix this bit to be 1'b1. Bit[5:4]: Gain mapping sel In OV5650, please fix these bits to be 2'b01 Bit[1:0]: Manual digital gain
0x3831	TIMING TC REG 31	0x00	RW	Bit[0]: r_vflip_color
0x3832	TIMING TC REG 32	0x00	RW	Bit[3:0]: x_addr_start[11:8]
0x3833	TIMING TC REG 33	0x00	RW	Bit[7:0]: x_addr_start[7:0]
0x3834	TIMING TC REG 34	0x0A	RW	Bit[3:0]: x_addr_end[11:8]
0x3835	TIMING TC REG 35	0x3F	RW	Bit[7:0]: x_addr_end[7:0]
0x3836	TIMING HVPAD	0x00	RW	Bit[7:4]: hpad Bit[3:0]: vpad
0x3850	TIMING TC REG 50	0x00	RW	Bit[1:0]: cshiftgolo[9:8]
0x3851	TIMING TC REG 51	0x00	RW	Bit[7:0]: cshiftgolo[7:0]

6.6 strobe

table 6-6 strobe control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE	0x00	RW	Bit[7]: Strobe ON Bit[6]: Reverse Bit[3:2]: width_in_xenon Bit[1:0]: Mode select 00: Xenon 01: LED1 10: LED2 11: LED3
0x3B04	STROBE FREX EXP HIGH	0x04	RW	Bit[7:0]: frex_exp[15:8] address

table 6-6 strobe control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B05	STROBE FREX EXP LOW	0x00	RW	Bit[7:0]: frex_exp[7:0]
0x3B06	STROBE FREX CTRL 0	0x04	RW	Bit[7:4]: frex_fm_dly Bit[3:0]: frex_strb_wid[3:0]
0x3B07	STROBE FREX MODE SELECT	0x08	RW	Bit[2]: FREX polarity 0: Low 1: High Bit[1:0]: Mode select 00: frex_strobe mode1 01: frex_strobe mode2 1x: Rolling strobe
0x3B08	STROBE FREX EXP REQ	0x00	RW	Bit[0]: frex_exp_req
0x3B09	FREX SHUTTER DELAY	0x02	RW	Bit[2:0]: FREX end option

6.7 camera interface (CIF)

The camera interface (CIF) is used to receive external sensor image data through the DVP.

table 6-7 CIF control registers

address	register name	default value	R/W	description
0x4100	CIF CTRL 00	0x00	RW	Reverse External Sensor Input Polarity Bit[7]: Source select 0: From external DVP input 1: From MIPI receiver Bit[6]: End-of-Frame signal select Bit[5]: Reverse VSYNC polarity Bit[4]: Reverse HREF polarity Bit[3]: Reverse PCLK polarity Bit[2]: Reverse RBLUE polarity Bit[1]: Reverse ptn_RBLUE polarity Bit[0]: Reverse CIF RBLUE polarity

6.8 frame control (FC)

Frame control (FC) is used to mask some specified frame by setting the appropriate registers.

table 6-8 frame control registers

address	register name	default value	R/W	description
0x4200	FRAME CONTROL00	0x00	RW	Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: Frame counter reset
0x4201	FRAME CONTROL01	0x00	RW	Control Passed Frame Number Bit[3:0]: Frame ON number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode
0x4202	FRAME CONTROL02	0x00	RW	Control Masked Frame Number Bit[3:0]: Frame OFF number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode
0x4203	FRAME CONTROL03	0x00	RW	Bit[6]: rblue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.9 format description

Format control converts the internal data format into the desired output format including YUV, RGB, or RAW.

table 6-9 format control registers

address	register name	default value	R/W	description
0x4302	FORMAT YMAX	0x00	RW	Bit[3:0]: ymax high 4 bits
0x4303	FORMAT YMAX	0xFF	RW	Bit[7:0]: ymax low byte
0x4304	FORMAT YMIN	0x00	RW	Bit[3:0]: ymin high 4 bits
0x4305	FORMAT YMIN	0x00	RW	Bit[7:0]: ymin low byte
0x4306	FORMAT UMAX	0x00	RW	Bit[3:0]: umax high 4 bits
0x4307	FORMAT UMAX	0xFF	RW	Bit[7:0]: umax low byte
0x4308	FORMAT UMIN	0x00	RW	Bit[3:0]: umin high 4 bits
0x4309	FORMAT UMIN	0x00	RW	Bit[7:0]: umin low byte
0x430A	FORMAT VMAX	0x00	RW	Bit[3:0]: vmax high 4 bits
0x430B	FORMAT VMAX	0xFF	RW	Bit[7:0]: vmax low byte
0x430C	FORMAT VMIN	0x00	RW	Bit[3:0]: vmin high 4 bits
0x430D	FORMAT VMIN	0x00	RW	Bit[7:0]: vmin low byte

6.10 digital video port (DVP)

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported and extended features including compression mode, HSYNC mode, CCIR656 mode, and test pattern output. The DVP is also used to receive the video data from an external camera, which will be sent out through the OV5653 MIPI interface.

table 6-10 system control registers

address	register name	default value	R/W	description
0x4700	DVP MODE SELECT	0x04	RW	Bit[3]: CCIR v select Bit[2]: CCIR f select Bit[1]: CCIR656 mode enable Bit[0]: HSYNC mode enable
0x4701	DVP VSYNC WIDTH CONTRL	0x01	RW	VSYNC Width (in terms of number of lines)
0x4702	DVP_HSYVSY_NEG_WIDTH	0x01	RW	VSYNC Width (pixel count, high byte)
0x4703	DVP_HSYVSY_NEG_WIDTH	0x00	RW	VSYNC Width (pixel count, low byte)
0x4704	DVP VSYNC MODE	0x00	RW	Bit[3:2]: r_vsyncount_sel Bit[1]: r_vsync3_mod Bit[0]: r_vsync2_mod
0x4705	DVP_EOF_VSYNC DELAY	0x00	RW	SOF/EOF Negative Edge to VSYNC Positive Edge Delay, High Byte
0x4706	DVP_EOF_VSYNC DELAY	0x00	RW	SOF/EOF Negative Edge to VSYNC Positive Edge Delay, Middle Byte
0x4707	DVP_EOF_VSYNC DELAY	0x00	RW	SOF/EOF Negative Edge to VSYNC Positive Edge Delay, Low Byte
0x4708	DVP_POL_CTRL	0x01	RW	Bit[7]: Clock DDR mode enable Bit[5]: VSYNC gated clock enable Bit[4]: HREF gated clock enable Bit[3]: No first for FIFO Bit[2]: HREF polarity reverse Bit[1]: VSYNC polarity reverse Bit[0]: PCLK polarity reverse
0x4709	BIT_TEST_PATTERN	0x00	RW	Bit[7]: FIFO bypass mode Bit[6:4]: Data bit swap Bit[3]: Bit test mode Bit[2]: 10-bit test Bit[1]: 8-bit test Bit[0]: Bit test enable
0x470A	DVP_BYP_CTRL	0x00	RW	Bypass Control High Byte
0x470B	DVP_BYP_CTRL	0x00	RW	Bypass Control Low Byte
0x470C	DVP_BYP_SEL	0x00	RW	Bit[4]: HREF select Bit[3:0]: Bypass select

6.10.1 DVP timing

figure 6-1 DVP timing diagram

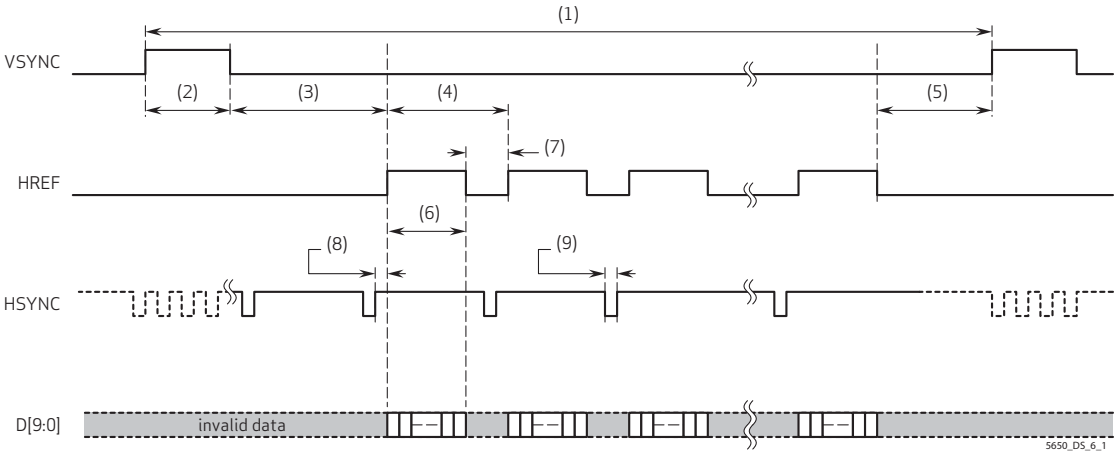


table 6-11 DVP timing specifications (sheet 1 of 2)

mode	timing
5 Megapixel 2592x1944	(1) 6132288 tp (3112x1968) (2) 3372 tp (3) 28365 tp (4) 3116 tp (5) 43571 tp (6) 2592 tp (7) 524 tp (8) 0 tp (9) 524 tp
1080p 1920x1080	(1) 2795328 tp (2532X1104) (2) 6958 tp (3) 5666 tp (4) 2532 tp (5) 48756 tp (6) 1920 tp (7) 612 tp (8) 0 tp (9) 612 tp
982p 1744x982	(1) 2370136 tp (2) 6500 tp (3) 5224 tp (4) 2356 tp (5) 45412 tp (6) 1744 tp (7) 612 tp (8) 0 tp (9) 612 tp

note
The timing values shown in **table 6-11** may vary depending upon register settings.

table 6-11 DVP timing specifications (sheet 2 of 2)

mode	timing
720p 1280x720	(1) 1407648 tp (2) 2148 tp (3) 17438 tp (4) 1892 tp (5) 26434 tp (6) 1280 tp (7) 612 tp (8) 0 tp (9) 612 tp
VGA 640x480	(1) 476784 tp (946x504) (2) 1202 tp (3) 8592 tp (4) 946 tp (5) 13216 tp (6) 640 tp (7) 306 tp (8) 0 tp (9) 306 tp
QVGA 320x240	(1) 124872 tp (2) 729 tp (3) 4169 tp (4) 473 tp (5) 6607 tp (6) 320 tp (7) 153 tp (8) 0 tp (9) 153 tp
5 Megapixel 2592x1944	(1) 6132288 tp (3112x1968) (2) 3372 tp (3) 28365 tp (4) 3116 tp (5) 43571 tp (6) 2592 tp (7) 524 tp (8) 0 tp (9) 524 tp
1080p 1920x1080	(1) 2795328 tp (2532x1104) (2) 6958 tp (3) 5666 tp (4) 2532 tp (5) 48756 tp (6) 1920 tp (7) 612 tp (8) 0 tp (9) 612 tp

6.11 mobile industry processor interface (MIPI)

MIPI provides a single uni-directional clock lane and two bi-directional data lane solution for communication links between components inside a mobile device. The two data lanes have full support for HS (uni-directional) and LP (bi-directional) data transfer mode. Contact your local OmniVision FAE for more details.

table 6-12 MIPI transmitter registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[6]: ck_mark1_en 1: Enable clock lane mark1 when resume Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Lane select 0: Use lane1 as default data lane 1: Use lane2 as default data lane Bit[2]: Idle status 0: MIPI bus will be LP00 when no packet to transmit 1: MIPI bus will be LP11 when no packet to transmit Bit[1]: Clock lane first bits 0: Output 0x55 1: Output 0xAA Bit[0]: Clock lane dis 1: Manually set clock lane to low power mode

table 6-12 MIPI transmitter registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x4801	MIPI CTRL 01	0x03	RW	MIPI Control 01 Bit[7]: Long packet data type manual enable 0: Use MIPI_dt 1: Use dt_man_o as long packet data (see register **0x4814**[5:0]) Bit[6]: Short packet data type manual enable 1: Use dt_spkt as short packet data (see register **0x4815**[5:0]) Bit[5]: Short packet WORD COUNTER manual enable 0: Use frame counter or line counter 1: Select spkt_wc_reg_o (see {**0x4812**, **0x4813**}) Bit[4]: PH bit order for ECC 0: {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]} Bit[3]: PH byte order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[2]: PH byte order2 for ECC 0: {DI,WC} 1: {WC,DI} Bit[1]: mark1_en1 1: After each rst release, lane 1 should send mark1 for wkup_dly_o when MIPI_sys_susp =1 Bit[0]: mark1_en2 1: After each rst release, lane 2 should send mark1 for wkup_dly_o when MIPI_sys_susp=1

table 6-12 MIPI transmitter registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x4802	MIPI CTRL 02	0x00	RW	MIPI Control 02 Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail.min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI CTRL 03	0x5F	RW	MIPI Control 03 Bit[3]: Enable LP CD when HS transmits for lane1 0: Disable 1: Enable Bit[2]: Enable LP CD when HS transmits for lane2 0: Disable 1: Enable Bit[1]: Enable LP CD when LP transmits for lane2 0: Disable 1: Enable Bit[0]: Enable LP CD when LP transmits for lane1 0: Disable 1: Enable

table 6-12 MIPI transmitter registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x4804	MIPI CTRL 04	0x8D	RW	MIPI Control 04 Bit[4]: Enable MIPI LP receiver to read/write registers 0: Disable - RX LP data will write to VFIFO 1: Enable Bit[3]: Address read/write register will auto add 1 0: Disable 1: Enable Bit[2]: LP TX lane select 0: Select lane1 to transmit LP data 1: Select lane2 to transmit LP data
0x4805	MIPI CTRL 05	0x10	RW	MIPI Control 05 Bit[7]: MIPI lane2 disable 1: Disable MIPI data lane2, lane2 will be LP00 Bit[6]: MIPI lane1 disable 1: Disable MIPI data lane1, lane1 will be LP00 Bit[2]: MIPI read/write registers disable 1: Disable MIPI access to SRB
0x4810	MIPI MAX FRAME COUNT	0xFF	RW	High Byte of Max Frame Count of Frame Sync Short Packet
0x4811	MIPI MAX FRAME COUNT	0xFF	RW	Low Byte of Max Frame Count of Frame Sync Short Packet
0x4812	MIPI_SPKT_WC_ REG	0x00	RW	High Byte of Short Packet Word Counter, Manual Mode
0x4813	MIPI_SPKT_WC_ REG	0x00	RW	Low Byte of Short Packet Word Counter, Manual Mode
0x4814	MIPI CTRL14	0x2A	RW	MIPI Control 14 Bit[7:6]: Virtual channel of MIPI Bit[5:0]: Data type in manual mode
0x4815	MIPI_DT_SPKT	0x00	RW	Bit[6]: pclk_div 0: Use rising edge of MIPI_pclk_o to generate MIPI bus to PHY 1: Use falling edge of MIPI_pclk_o to generate MIPI bus to PHY
0x4818	MIPI_HS_ZER_MIN	0x00	RW	High byte of the minimum value for hs_zero, unit ns
0x4819	MIPI_HS_ZER_MIN	0x96	RW	Low byte of the minimum value for hs_zero, unit ns hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	MIPI_HS_TRAIL_MIN	0x00	RW	High byte of the minimum value for hs_trail, unit ns

table 6-12 MIPI transmitter registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x481B	MIPI_HS_TRAIL_MIN	0x3C	RW	Low byte of the minimum value for hs_trail, hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	MIPI_CLK_ZER_MIN	0x01	RW	High byte of the minimum value for clk_zero, unit ns
0x481D	MIPI_CLK_ZER_MIN	0x86	RW	Low byte of the minimum value for clk_zero, clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	MIPI_CLK_PREPARE_MIN	0x00	RW	High byte of the minimum value for clk_prepare, unit ns Bit[1:0]: clk_prepare_min[9:8]
0x481F	MIPI_CLK_PREPARE_MIN	0x3C	RW	Low byte of the minimum value for clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_o
0x4820	MIPI_CLK_POST_MIN	0x00	RW	High byte of the minimum value for clk_post, unit ns Bit[1:0]: clk_post_min[9:8]
0x4821	MIPI_CLK_POST_MIN	0x56	RW	Low byte of the minimum value for clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_o
0x4822	MIPI_CLK_TRAIL_MIN	0x00	RW	High byte of the minimum value for clk_trail, unit ns Bit[1:0]: clk_trail_min[9:8]
0x4823	MIPI_CLK_TRAIL_MIN	0x3C	RW	Low byte of the minimum value for clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	MIPI_LPX_P_MIN	0x00	RW	High byte of the minimum value for lpx_p, unit ns Bit[1:0]: lpx_p_min[9:8]
0x4825	MIPI_LPX_P_MIN	0x32	RW	Low byte of the minimum value for lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	MIPI_HS_PREPARE_MIN	0x00	RW	High byte of the minimum value for hs_prepare, unit ns Bit[1:0]: hs_prepare_min[9:8]
0x4827	MIPI_HS_PREPARE_MIN	0x32	RW	Low byte of the minimum value for hs_prepare hs_prepare_real = hs_prepare_min_o + Tui*ui_hs_prepare_min_o
0x4828	MIPI_HS_EXIT_MIN	0x00	RW	High byte of the minimum value for hs_exit, unit ns Bit[1:0]: hs_exit_min[9:8]
0x4829	MIPI_HS_EXIT_MIN	0x64	RW	Low byte of the minimum value for hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	MIPI_UI_HS_ZER_MIN	0x05	RW	Minimum UI Value of hs_zero, unit UI
0x482B	MIPI_UI_HS_TRAIL_MIN	0x04	RW	Minimum UI Value of hs_trail, unit UI
0x482C	MIPI_UI_CLK_ZER_MIN	0x00	RW	Minimum UI Value of clk_zero, unit UI

table 6-12 MIPI transmitter registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x482D	MIPI_UI_CLK_PREPARE_MIN	0x00	RW	Minimum UI Value of clk_prepare, unit UI
0x482E	MIPI_UI_CLK_POST_MIN	0x34	RW	Minimum UI Value of clk_post, unit UI
0x482F	MIPI_UI_CLK_TRAIL_MIN	0x00	RW	Minimum UI Value of clk_trail, unit UI
0x4830	MIPI_UI_LPX_P_MIN	0x00	RW	Minimum UI Value of lpx_p, unit UI
0x4831	MIPI_UI_HS_PREPARE_MIN	0x04	RW	Minimum UI Value of hs_prepare, unit UI
0x4832	MIPI_UI_HS_EXIT_MIN	0x00	RW	Minimum UI Value of hs_exit, unit UI
0x4833	MIPI_REG_MIN	0x00	RW	MIPI register address, lower bound (high byte) Address range of MIPI R/W registers is from MIPI_reg_min to MIPI_reg_max
0x4834	MIPI_REG_MIN	0x00	RW	MIPI Register Address, Lower Bound (Low Byte)
0x4835	MIPI_REG_MAX	0xFF	RW	MIPI Register Address, Upper Bound (High Byte)
0x4836	MIPI_REG_MAX	0xFF	RW	MIPI Register Address, Upper Bound (Low Byte)
0x4837	MIPI_PCLK_PERIOD	0x10	RW	Period of pclk2x, pclk_div = 1, and 1-bit decimal
0x4838	MIPI_WKUP_DLY	0x02	RW	Wakeup Delay for MIPI
0x483A	MIPI_DIR_DLY	0x08	RW	Change LP Direction Delay/2 after LP11
0x483B	MIPI_LP_GPIO	0x33	RW	Bit[7]: lp_sel1 0: Generate MIPI_lp_dir1_o automatically 1: Use lp_dir_man1 as MIPI_lp_dir1_o Bit[6]: lp_dir_man1 0: Input 1: Output Bit[5]: lp_p1_o Bit[4]: lp_n1_o Bit[3]: lp_sel2 0: Generate MIPI_lp_dir2_o automatically 1: Use lp_dir_man2 as MIPI_lp_dir2_o Bit[2]: lp_dir_man2 0: Input 1: Output Bit[1]: lp_p2_o Bit[0]: lp_n2_o
0x483C	MIPI CTRL 33	0x4F	RW	Bit[7:4]: t_lpx, unit: sclk cycles Bit[3:0]: t_clk_pre, unit: sclk cycles

table 6-12 MIPI transmitter registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x483D	MIPI_T_TA_GO	0x10	RW	t_ta_go, unit: sclk cycles
0x483E	MIPI_T_TA_SURE	0x06	RW	t_ta_sure, unit: sclk cycles
0x483F	MIPI_T_TA_GET	0x14	RW	t_ta_get, unit: sclk cycles
0x4846	MIPI_CLIP_MAX	0x0F	RW	High Byte of the Maximum Value of MIPI Output Data Bit[3:0]: MIPI_clip_max[11:8]
0x4847	MIPI_CLIP_MAX	0xFF	RW	Low Byte of the Maximum Value of MIPI Output Data Bit[7:0]: MIPI_clip_max[7:0]
0x4848	MIPI_CLIP_MIN	0x00	RW	High Byte of the Minimum Value of MIPI Output Data Bit[3:0]: MIPI_clip_min[11:8]
0x4849	MIPI_CLIP_MIN	0x00	RW	Low Byte of the Minimum Value of MIPI Output Data Bit[7:0]: MIPI_clip_min[7:0]
0x4850	MIPI_REG_INTR_MAN	0x00	RW	Writing to this register will generate a pulse of one sclk period for micro-controller interrupt
0x4851	MIPI_REG_TX_WR	0x00	RW	Writing to this register will generate a pulse of one SCLK period to MIPI_TX_LP_TX; the register write data will be sent out through MIPI ESCAPE mode
0x4852	MIPI_REG_TX_STOP	0x00	RW	Writing to this register will generate a pulse of one sclk period to MIPI_TX_LP_TX; MIPI_TX_LP_TX will go back to stop state.
0x4853	MIPI_REG_TA_ACK	0x00	RW	Writing to this register will generate a pulse of one sclk period to MIPI_TX_LP_TX to receive Turnaround command
0x4854	MIPI_REG_TA_REQ	0x00	RW	Writing to this register will generate a pulse of one sclk period to MIPI_TX_LP_TX to send Turnaround command
0x4860	MIPI CTRL 60	–	R	MIPI Read/Write Only Bit[0]: MIPI_dis_me 0: Enable MIPI read/write registers 1: Disable MIPI read/write registers
0x4861	MIPI_HD_SK_REG0	–	R	MIPI Read/Write, SCCB and MCU Read Only
0x4862	MIPI_HD_SK_REG1	–	R	MIPI Read/Write, SCCB and MCU Read Only
0x4863	MIPI_HD_SK_REG2	–	R	MIPI Read/Write, SCCB and MCU Read Only
0x4864	MIPI_HD_SK_REG3	–	R	MIPI Read/Write, SCCB and MCU Read Only

table 6-12 MIPI transmitter registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x4865	MIPI_ST	–	R	Bit[5]: lp_rx_sel_i 1: MIPI_LP_RX receives LP data Bit[4]: tx_busy_i 1: MIPI_TX_LP_TX is busy sending LP data Bit[3]: MIPI_lp_p1_i MIPI low power input for lane 1p Bit[2]: MIPI_lp_n1_i MIPI low power input for lane 1n Bit[1]: MIPI_lp_p2_i MIPI low power input for lane 2p Bit[0]: MIPI_lp_n2_i MIPI low power input for lane 2n

7 register tables

The following tables provide descriptions of the device control registers contained in the OV5653. For all registers enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x6C for write and 0x6D for read.

table 7-1 system control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x3000	SYSTEM RESET00	0x20	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset BIST Bit[6:5]: Not used Bit[4]: Reset OTP memory Bit[3]: Reset STB Bit[2]: Reset 5060HZ Bit[1]: Reset timing control Bit[0]: Reset array control
0x3001	SYSTEM RESET01	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset AWB registers Bit[6]: Not used Bit[5]: Reset ISP Bit[4]: Reset FC Bit[3]: Reset CIF Bit[2]: Reset BLC Bit[1]: Reset AEC registers Bit[0]: Reset AEC
0x3002	SYSTEM RESET02	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7]: Reset VFIFO Bit[6]: Not used Bit[5]: Reset FORMAT Bit[4:1]: Not used Bit[0]: Reset average
0x3003	SYSTEM RESET03	0x00	RW	Reset for Individual Block (0: enable block; 1: reset block) Bit[7:4]: Not used Bit[3]: Reset MIPI receiver Bit[2]: Reset ISP FC Bit[1]: Reset MIPI Bit[0]: Reset DVP

table 7-1 system control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x3004	CLOCK ENABLE00	0xDF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable BIST clock Bit[6:5]: Not used Bit[4]: Enable OTP clock Bit[3]: Enable strobe clock Bit[2]: Enable 5060 Hz detection clock Bit[1]: Enable timing control clock Bit[0]: Enable array control clock
0x3005	CLOCK ENABLE01	0xFF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Enable AWB register clock Bit[6]: Not used Bit[5]: Enable ISP clock Bit[4]: Enable FC clock Bit[3]: Enable CIF clock Bit[2]: Enable BLC clock Bit[1]: Enable AEC register clock Bit[0]: Enable AEC clock
0x3006	CLOCK ENABLE02	0xFF	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[7]: Not used Bit[6]: Enable format clock Bit[5:1]: Not used Bit[0]: Enable average clock
0x3007	CLOCK ENABLE03	0x3F	RW	Clock Enable Control (0: disable clock; 1: enable clock) Bit[5]: Enable ISP_FC clock Bit[4]: Enable MIPI PCLK clock Bit[3]: Enable MIPI clock Bit[2]: Enable DVP clock Bit[1]: Enable VFIFO PCLK clock Bit[0]: Enable VFIFO SCLK clock
0x3008	SYSTEM CTRL0	0x02	RW	Bit[7]: Reset registers Bit[6]: Register power down Bit[5]: Not used Bit[4]: sc_srb_clk_syn_en Bit[3]: iso_susp_sel_o Bit[2]: MIPI_rst_msk_o Bit[1]: MIPI_susp_msk_o Bit[0]: MIPI_rst_sel_o
0x3009	SC_MIPI_PCLK_DIV_CTRL	0x01	RW	Bit[7]: MIPI_pdiv_sepa Bit[6]: Not used Bit[5:0]: MIPI PCLK divider
0x300A	CHIP ID	–	R	Chip ID High Byte

table 7-1 system control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x300B	CHIP ID	–	R	Chip ID Low Byte
0x300C	RSVD	–	–	Reserved
0x300D	SC_SD_SDIV	0x22	RW	Bit[7:3]: Debug mode Bit[2:0]: r_sdiv, divider for 50/60 detection
0x300E	SC_MIPI_SC_CTRL0	0x18	RW	Bit[7:5]: Not used Bit[4]: r_phy_pd_MIPI 1: Power down PHY HS TX Bit[3]: r_phy_pd_lprx 1: Power down PHY LP RX module Bit[2]: MIPI_en 0: DVP enable 1: MIPI enable Bit[1]: MIPI_susp_reg 1: MIPI system suspends registers Bit[0]: lane_dis_op 0: Use ~MIPI release 1/2 and lane_disable 1/2 to disable two data lanes 1: Use lane disable 1/2 to disable two data lane
0x300F	PLL CTRL 00	0x8E	RW	Bit[7:6]: R_SELD5 00: Bypass 01: Divide by 1 10: Divide by 4 11: Divide by 5 Bit[5:3]: Debug mode Bit[2]: R_DIVL 0: One lane, divide by 2 1: Two lanes, divide by1 Bit[1:0]: R_SELD2P5 00: Bypass 01: Divide by 1 10: Divide by 2 11: Divide by 2.5
0x3010	PLL CTRL 01	0x10	RW	Bit[7:4]: R_DIVS, Sdiv Bit[3:0]: R_DIVM, Mdiv
0x3011	PLL CTRL 02	0x10	RW	Bit[7]: PLL bypass Bit[6]: Debug mode Bit[5:0]: R_DIVP, pll_div

table 7-1 system control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x3012	PLL CTRL 03	0x02	RW	Bit[7:3]: Debug mode Bit[2:0]: R_PREDIV 000: Divide by 1 001: Divide by 1.5 010: Divide by 2 011: Divide by 2.5 100: Divide by 3. 101: Divide by 4 110: Divide by 6 111: Divide by 8
0x3013~ 0x3015	RSVD	–	–	Reserved
0x3016	PAD OUTPUT ENABLE0	0x00	RW	Bit[7:2]: Debug mode Bit[1]: STROBE output enable Bit[0]: SIOD output enable
0x3017	PAD OUTPUT ENABLE1	0x00	RW	Bit[7]: FREX output enable Bit[6]: VSYNC output enable Bit[5]: HREF output enable Bit[4]: PCLK output enable Bit[3:0]: D[9:6] output enable
0x3018	PAD OUTPUT ENABLE2	0x00	RW	Bit[7:2]: D[5:0] output enable Bit[1:0]: Debug mode
0x3019	PAD OUTPUT0	0x00	RW	Bit[7:2]: Debug mode Bit[1]: STROBE Bit[0]: SIOD
0x301A	PAD OUTPUT1	0x00	RW	Bit[7]: FREX Bit[6]: VSYNC Bit[5]: HREF Bit[4]: PCLK Bit[3:0]: D[9:6]
0x301B	PAD OUTPUT2	0x00	RW	Bit[7:2]: D[5:0] Bit[1:0]: Debug mode
0x301C	PAD SELECT 0	0x00	RW	Bit[7:2]: Debug mode Bit[1]: I/O STROBE select Bit[0]: I/O SIOD select
0x301D	PAD SELECT 1	0x00	RW	Bit[7]: I/O FREX select Bit[6]: I/O VSYNC select Bit[5]: I/O HREF select Bit[4]: I/O PCLK select Bit[3:0]: I/O D[9:6] select
0x301E	PAD SELECT 2	0x00	RW	Bit[7:2]: I/O D[5:0] select Bit[1:0]: Debug mode

table 7-1 system control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x301F	SRAM0 SELECT	0x00	RW	System Control Selects SRAM0
0x3020	SRAM1 SELECT	0x00	RW	System Control Selects SRAM1
0x3021	SRAM2 SELECT	0x00	RW	System Control Selects SRAM2
0x3022	SRAM TEST VALUE0	0xFF	RW	System SRAM Test Value 0
0x3023	SRAM TEST VALUE1	0x09	RW	System SRAM Test Value 1
0x3024~ 0x302B	RSVD	–	–	Reserved
0x302C	SYSTEM PAD CTRL	0x02	RW	Bit[7]: pd_dato_en Bit[6:3]: iP2X3v[3:0] Bit[2]: man_rst_pon Bit[1]: FREX enable, active low Bit[0]: Debug mode
0x302D	SYSTEM MIPI CTRL1	0x10	RW	Bit[7:6]: High speed common mode voltage Bit[5:4]: Driving strength of low speed transmitter Bit[3]: Bias current reduction Bit[2]: CD input low voltage Bit[1]: CD input high voltage-dummy Bit[0]: Valid delay-dummy
0x302E	SYSTEM MIPI CTRL 0	0x00	RW	Bit[7:3]: Debug mode Bit[2]: Bypass the latch of hs_enable Bit[1:0]: Bias current adjustment
0x302F	DVP CCLK DIV	0x02	RW	System DVP CCLK Divider Bit[5:0]: Divider for external CCLK
0x3030	POWER CTRL 0	0x00	RW	sc_a_pwc_pk_o[7:0] Bit[7]: bp_npump Bypass N pump Bit[6]: bp_ppump Bypass P pump Bit[5:4]: Debug mode Bit[3:0]: dio[3:0]
0x3031	POWER CTRL 1	0x00	RW	sc_a_pwc_pk_o[15:8] Bit[7:4]: vrbg[3:0] Bit[3]: Debug mode Bit[2]: pd_bias Bit[1]: pd_other Bit[0]: pd_vmrst

table 7-1 system control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x3032	POWER CTRL 2	0x00	RW	sc_a_pwc_pk_o[23:16] Bit[7:4]: Debug mode Bit[3:0]: vrbglp[3:0] bandgap_lp trimming bits
0x3033	SC_RSV0	0x03	RW	Bit[7:5]: Debug mode Bit[4]: dis_srb_rst_o Disable reset for SRB when clock switches, active high Bit[3:2]: Debug mode Bit[1]: frex_ef_sel Bit[0]: cen_global_o
0x3034	SC_MARK1_CNT	0x10	RW	MIPI ULPS Resume Mark1 Detect Length
0x3035	SC_FREX_RST_MASK0	0xFF	RW	Bit[7]: frex_mask_aec Bit[6]: frex_mask_blc Bit[5]: frex_mask_tc Bit[4]: frex_mask_isp_fc Bit[3]: frex_mask_isp Bit[2]: Debug mode Bit[1]: frex_mask_avg Bit[0]: Debug mode
0x3036	SC_FREX_RST_MASK1	0x00	RW	Bit[7:4]: Debug mode Bit[3]: frex_mask_vfifo Bit[2]: frex_mask_dvp Bit[1]: frex_mask_MIPI Bit[0]: frex_mask_MIPI_phy
0x3037	RSVD	–	–	Reserved
0x3040	SC_IO_PAD_IN0	–	R	sc_io_pad_in[23:16]
0x3041	SC_IO_PAD_IN1	–	R	sc_io_pad_in[15:8]
0x3042	SC_IO_PAD_IN2	–	R	sc_io_pad_in[7:0]
0x3043	SC_IO_PAD_IN3	–	R	sc_io_pad_in[31:24]

table 7-2 system control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3100	SCCB ID	0x6C	RW	SCCB Slave ID
0x3101	SCCB CTRL	0x03	RW	Bit[7:2]: Debug mode Bit[1]: en_ss_addr_inc Bit[0]: sccb_en_o
0x3102	SCCB_SYSREG	0x00	RW	For SCCB Access Only Bit[7]: Debug mode Bit[6]: ctrl_rst_MIPIsc Bit[5]: ctrl_rst_srb Bit[4]: ctrl_rst_sccb_s Bit[3]: ctrl_rst_pon_sccb_s Bit[2]: ctrl_rst_clkmod Bit[1]: ctrl_MIPI_phy_rst_o Bit[0]: ctrl_pll_rst_o
0x3103	SCCB_PWUP_DIS	0x91	RW	For SCCB Access Only Bit[7]: pad_no_sda_oen Bit[6:5]: Debug mode Bit[4]: r_srb_clk_syn_en Bit[3]: pwup_dis2 Bit[2]: pwup_dis1 Bit[1]: PLL clock select 0: System clock from PAD 1: System clock from PLL Bit[0]: pwup_dis0
0x3104	SCCB_PADCLK_DIV	0x01	RW	For SCCB Access Only Bit[5:0]: padclk_div
0x3105	SCCB_SRB_HOST_INPUT_DIS	0xFF	RW	For SCCB Access Only Bit[7]: ctrl_reg_ms Bit[6]: ctrl_awb_done Bit[5]: ctrl_vts_done Bit[4]: ctrl_agc_done Bit[3]: ctrl_aec_done Bit[2]: ctrl_MIPI_host Bit[1]: Debug mode Bit[0]: ctrl_bist_host
0x3106	R_WS_BEGIN	0x03	RW	R_WS_BEGIN
0x3107	R_WS_WIDTH	0x03	RW	R_WS_WIDTH
0x3108	SCCB_PRE_CONTRL	0x00	RW	Bit[7]: bypass_start_stop Bit[6:5]: serial_signal_dly2_dly3_dly4_select 00: dly2d 01: dly3d 1x: dly4d Bit[4]: bypass_filter Bit[3:0]: gate_glitch_width

table 7-2 system control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3109	SCCB_PRE_START_STOP_CONTRL	0x03	RW	Bit[7:4]: Debug mode Bit[3:0]: start_top_ctrl
0x310A	SCCB_CTRL_OPTION	0x1D	RW	Bit[7:5]: Debug mode Bit[4:3]: r_reload_ctrl Bit[2]: r_msk_glitch Bit[1]: r_bit8_adr_en Bit[0]: r_msk_stop
0x310B	SCCB_FILTER	0x00	RW	Bit[7:4]: r_sda_num Bit[3:0]: r_scl_num
0x310C~0x31EF	RSVD	–	–	Reserved
0x31F0	OTP LD START ADDRESS	0x00	RW	OTP Manual Load Start Address
0x31F1	OTP DELAY	0x90	RW	Strobe Control Bit[7]: OTP Manual load start address disable 0: ENABLE 1: DISABLE Bit[6:0]: Not used
0x31F2~0x31FE	RSVD	–	–	Reserved
0x31FF	CS_SCCB	0x01	RW	Bit[7:1]: Debug mode Bit[0]: SCCB select 0: Old SCCB 1: New SCCB

table 7-3 group hold control registers

address	register name	default value	R/W	description
0x3200	SRM_GRUP_ADR0	0x00	RW	srm_group_adr0
0x3201	SRM_GRUP_ADR1	0x40	RW	srm_group_adr1
0x3202	SRM_GRUP_ADR2	0x80	RW	srm_group_adr2
0x3203	SRM_GRUP_ADR3	0xC0	RW	srm_group_adr3
0x3204~ 0x320A	RSVD	–	–	Reserved
0x320B	SRM_GRUP_LEN0	0x00	RW	srm_group_len0
0x320C	SRM_GRUP_LEN1	0x00	RW	srm_group_len1
0x320D	SRM_GRUP_LEN3	0x00	RW	srm_group_len2
0x320E	SRM_GRUP_LEN3	0x00	RW	srm_group_len3
0x320F~ 0x3211	GROUP WRITE CONTROL REGISTERS	–	–	Group write registers Changing these values is not recommended
0x3212	SRM_GRUP_ACCESS	0x00	W	Bit[7]: group_hold Bit[6]: group_access_tm Bit[5]: group_launch Bit[4]: group_hold_end Bit[3:0]: group_id, 0~3 (groups for register access)
0x3213	SRM_GRUP_STATUS	–	R	Bit[7]: Store default Bit[6]: Restore Bit[5]: grp_hold Bit[4]: grp_launch Bit[3]: grp_write_o Bit[2:0]: grp_sel
0x3214	SRM_RAM_CTRL	0x00	RW	Bit[7]: Debug mode Bit[6]: sel_iso 1: Enable iso recover at power down mode Bit[5]: sram_clk Bit[4]: sram_rst Bit[3]: sram_cen Bit[2]: sram_wen Bit[1]: sram_dat Bit[0]: sram_adr

table 7-4 PRAM_MC_PRAM_CTRLL control registers

address	register name	default value	R/W	description
0x3300	PRAM_MC_PRAM_CTRL1	0x00	RW	Bit[7]: Debug mode Bit[6]: sel_iso_in_sleep Bit[5]: iso_clk_in_sleep Bit[4]: iso_rst_in_sleep Bit[3]: iso_cen_in_sleep Bit[2]: iso_wen_in_sleep Bit[1]: iso_dat_in_sleep Bit[0]: iso_adr_in_sleep

table 7-5 AWB gain control registers

address	register name	default value	R/W	description
0x3400	AWB RED GAIN	0x04	RW	Bit[3:0]: RED gain[11:8]
0x3401	AWB RED GAIN	0x00	RW	Bit[7:0]: RED gain[7:0]
0x3402	AWB GREEN GAIN	0x04	RW	Bit[3:0]: GREEN gain[11:8]
0x3403	AWB GREEB GAIN	0x00	RW	Bit[7:0]: GREEN gain[7:0]
0x3404	AWB BLUE GAIN	0x04	RW	Bit[3:0]: BLUE gain[11:8]
0x3405	AWB BLUE GAIN	0x00	RW	Bit[7:0]: BLUE gain[7:0]
0x3406	AWB MANUAL CTRL	0x00	RW	Bit[0]: AWB gain manual control enable

table 7-6 AEC/AGC control function registers

address	register name	default value	R/W	description
0x3500	LONG EXPO	0x00	RW	Bit[7:4]: Not used Bit[3:0]: long_exposure[19:16]
0x3501	LONG EXPO	0x00	RW	Bit[7:0]: long_exposure[15:8]
0x3502	LONG EXPO	0x20	RW	Bit[7:0]: long_exposure[7:0]
0x3503	MANUAL CTRL	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Gain latch timing delay x0: Gain has no latch delay 01: Gain delay of 1 frame 11: Gain delay of 2 frames Bit[3]: Not used Bit[2]: Debug mode Bit[1]: AGC manual 0: Auto enable 1: Manual enable Bit[0]: AEC manual 0: Auto enable 1: Manual enable
0x3508	LONG GAIN	0x00	RW	Bit[7:1]: Debug mode Bit[0]: long_gain[8]
0x3509	LONG GAIN	0x00	RW	Bit[7:0]: long_gain[7:0]
0x350A	AGC ADJ	0x00	RW	Bit[7:1]: Debug mode Bit[0]: Gain high bit Gain = (0x350B[6]+1) × (0x350B[5]+1) × (0x350B[4]+1) × (0x350B[3:0]/16+1)
0x350B	AGC ADJ	0x00	RW	Bit[7:0]: Gain low bits Gain = (0x350B[6]+1) × (0x350B[5]+1) × (0x350B[4]+1) × (0x350B[3:0]/16+1)
0x350C	VTS DIFF	0x06	RW	Bit[7:0]: vts_diff[15:8] Changing this value is not recommended
0x350D	VTS DIFF	0x18	RW	Bit[7:0]: vts_diff[7:0] Changing this value is not recommended

table 7-7 sensor control registers

address	register name	default value	R/W	description
0x3600~ 0x3620	ANALOG CONTROL REGISTERS	–	RW	Analog Control Registers
0x3621	ARRAY CONTROL 01	0x00	RW	Array Control 01 Bit[7]: Horizontal binning enable Bit[6]: Horizontal subsampling Bit[5:0]: Debug mode
0x3622~ 0x3634	ANALOG CONTROL REGISTERS	–	RW	Analog Control Registers
0x3700~ 0x370C	ANALOG CONTROL REGISTERS	–	RW	Analog Control Registers
0x370D	ANALOG CONTROL D	0x04	RW	Analog Control Bit[7]: Debug mode Changing this value is not allowed Bit[6]: Vertical binning enable Bit[5:0]: Debug mode Changing this value is not allowed
0x370E~ 0x3715	ANALOG CONTROL REGISTERS	–	RW	Analog Control Registers

table 7-8 timing control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x3800	TIMING HS	0x01	RW	HREF Start Point Bit[7:4]: Debug mode Bit[3:0]: timing_hs[11:8]
0x3801	TIMING HS	0xB4	RW	HREF Start Point Bit[7:0]: timing_hs[7:0]
0x3802	TIMING VS	0x00	RW	VREF Start Point Bit[7:4]: Debug mode Bit[3:0]: timing_vs[11:8]
0x3803	TIMING VS	0x0A	RW	VREF Start Point Bit[7:0]: timing_vs[7:0]
0x3804	TIMING HW	0x0A	RW	HREF Width Bit[7:4]: Debug mode Bit[3:0]: timing_hw[11:8]
0x3805	TIMING HW	0x20	RW	HREF Width Bit[7:0]: timing_hw[7:0]

table 7-8 timing control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x3806	TIMING VH	0x07	RW	VREF Height Bit[7:4]: Debug mode Bit[3:0]: timing_vh[11:8]
0x3807	TIMING VH	0x98	RW	VREF Height Bit[7:0]: timing_vh[7:0]
0x3808	TIMING DVP HO	0x0A	RW	DVP Horizontal Output Size Bit[7:4]: Debug mode Bit[3:0]: timing_dvpho[11:8]
0x3809	TIMING DVP HO	0x20	RW	DVP Horizontal Output Size Bit[7:0]: timing_dvpho[7:0]
0x380A	TIMING DVP VO	0x07	RW	DVP Vertical Output Size Bit[7:4]: Debug mode Bit[3:0]: timing_dvpvo[11:8]
0x380B	TIMING DVP VO	0x98	RW	DVP vertical output size Bit[7:0]: timing_dvpvo[7:0]
0x380C	TIMING HTS	0x0C	RW	Total Horizontal Size Bit[7:5]: Debug mode Bit[4:0]: timing_hts[12:8]
0x380D	TIMING HTS	0x2C	RW	Total Horizontal Size Bit[7:0]: timing_hts[7:0]
0x380E	TIMING VTS	0x07	RW	Total Vertical Size Bit[3:0]: timing_vts[11:8]
0x380F	TIMING VTS	0xB0	RW	Total Vertical Size Bit[7:0]: timing_vts[7:0]
0x3810	TIMING HVOFFS	0xC2	RW	Bit[7:4]: hoffs[3:0] Bit[3:0]: voffs[3:0]
0x3811	R_FRAME_EXP1	0xF0	RW	Bit[7:0]: Frame exposure time[23:16]
0x3812~ 0x3813	GROUP TIMING CONTROL REGISTERS	–	–	Timing Control Registers
0x3814	TIMING TC REG 14	0x01	RW	Bit[7]: ext_vs_re Bit[6]: ext_yuv422_en Bit[5]: ext_snr_en Bit[4:0]: Debug mode
0x3815	TIMING TC REG 15	0x02	RW	Bit[7]: dvpshp Bit[6]: Debug mode Bit[5]: rip_sof_en Bit[4:0]: Debug mode
0x3816	TIMING TC REG 16	0x0A	RW	SOF to HREF Delay (number of pixel count)

table 7-8 timing control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x3817	TIMING TC REG 17	0x24	RW	Bit[7:4]: vs_int_r Origin of timing Bit[3]: Frame exposure href Bit[2:0]: Frame precharge length
0x3818	TIMING TC REG 18	0x80	RW	Bit[7]: dkhf Bit[6]: mirror Bit[5]: vflip Bit[4:2]: Debug mode Bit[1]: vsub4 Bit[0]: vsub2
0x3819	TIMING TC REG 19	0x80	RW	Bit[7:4]: SOF to HREF delay (number of line count) Bit[3]: vfifo_hsize_sel Bit[2]: vfifo_vsize_sel Bit[1:0]: vts_ctrl 00: From vts_aeclat 01: From reg_vts 10: From vts_i 11: From vts_vs
0x381A	TIMING TC HS MIRR ADJ	0x00	RW	Bit[7]: hs_mirror_offset_cs 0: Add hs_mirror_offset 1: Subtract hs_mirror_offset Bit[6:0]: hs_mirror_offset
0x381B	TIMING TC VS FLIP ADJ	0x00	RW	Bit[7]: vs_flip_offset_cs 0: Add vs_flip_offset 1: Subtract vs_flip_offset Bit[6:0]: vs_flip_offset
0x381C	TIMING TC REG 1C	0x20	RW	Bit[7]: VGA preview md Bit[6]: first_l Bit[5]: en_fram_mask_for_grp_wr Bit[4]: r_crop_en Bit[3:0]: tc_vs_crop_h
0x381D	TIMING TC VS CROP L	0x0A	RW	Bit[7:0]: tc_vs_crop_l
0x381E	TIMING TC VH CROP	0x01	RW	Bit[3:0]: vh_crop_h
0x381F	TIMING TC VH CROP	0x20	RW	Bit[7:0]: vh_crop_l
0x3820	TIMING TC REG 20	0x00	RW	Bit[7]: Enable hs crop via x_address Bit[6]: xaddr_hrefB Bit[5]: Debug mode Bit[4:0]: tc_hs_crop[4:0]
0x3821	TIMING TC REG 21	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: tc_hw_crop[5:0]

table 7-8 timing control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x3822	R_SHUTTER_DLY	0x03	RW	Bit[7:5]: Not used Bit[4:0]: Shutter delay compensation[12:8]
0x3823	R_SHUTTER_DLY	0x03	RW	Bit[7:0]: Shutter delay compensation[7:0]
0x3824	TIMING HREFST MAN HIGH	0x01	RW	Bit[7:6]: Debug mode Bit[5]: hvs_man Bit[4:0]: hrefst_man_h
0x3825	TIMING HREFST MAN LOW	0xB4	RW	Bit[7:0]: hrefst_man_l
0x3826	TIMING VREF1 ST MAN HIGH	0x00	RW	Bit[7:0]: vref1_man_h[15:8]
0x3827	TIMING VREF1 ST MAN LOW	0x0A	RW	Bit[7:0]: vref1_man_l[7:0]
0x3828	TIMING SNR X OFFSET	–	R	Sensor X Offset High Byte
0x3829	TIMING SNR X OFFSET	–	R	Sensor X Offset Low Byte
0x382A	TIMING SNR Y OFFSET	–	R	Sensor Y Offset High Byte
0x382B	TIMING SNR Y OFFSET	–	R	Sensor Y Offset Low Byte
0x382C	TIMING HSYNC START	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: hsync_start_h
0x382D	TIMING HSYNC START	0x00	RW	Bit[7:0]: hsync_start_l
0x382E	TIMING HSYNC WIDTH	0x00	RW	HSYNC Width
0x3830	TIMING TC REG 30	0x50	RW	Bit[7]: Digtal gain manual enable Bit[6]: Digital gain select Bit[5:4]: Gain mapping select Bit[3:2]: Not used Bit[1:0]: Manual digital gain
0x3831	TIMING TC REG 31	0x00	RW	Bit[7:1]: Debug mode Bit[0]: r_vflip_color
0x3832	TIMING TC REG 32	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: x_addr_start[11:8]
0x3833	TIMING TC REG 33	0x00	RW	Bit[7:0]: x_addr_start[7:0]
0x3834	TIMING TC REG 34	0x0A	RW	Bit[7:4]: Debug mode Bit[3:0]: x_addr_end[11:8]
0x3835	TIMING TC REG 35	0x3F	RW	Bit[7:0]: x_addr_end[7:0]
0x3836	TIMING HVPAD	0x00	RW	Bit[7:4]: hpad Bit[3:0]: vpad

table 7-8 timing control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x3850	TIMING TC REG 50	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: cshiftgolo[9:8]
0x3851	TIMING TC REG 51	0x00	RW	Bit[7:0]: cshiftgolo[7:0]

table 7-9 AEC registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3A00	AEC CTRL00	0x78	RW	Bit[7]: Debug mode Bit[6]: Less one line mode Bit[5]: Band function Bit[4]: Band low limit mode Bit[3]: Debug mode Bit[2]: Night mode Bit[1]: Debug mode Bit[0]: Freeze
0x3A01	MIN EXPO	0x04	RW	Bit[7:0]: Minimum expo
0x3A02	MAX EXPO 60	0x03	RW	Bit[7:4]: Debug mode Bit[3:0]: Maximum expo[19:16]
0x3A03	MAX EXPO 60	0xD8	RW	Bit[7:0]: max expo[15:8]
0x3A04	MAX EXPO 60	0x00	RW	Bit[7:0]: max expo[7:0]
0x3A05	AEC CTRL05	0x30	RW	Bit[7]: f50_reverse 0: Hold 50, 60Hz detect input 1: Switch 50, 60Hz detect input Bit[6]: frame_insert 0: In night mode, insert step based on band 1: In night mode, insert step based on frame Bit[5]: Debug mode Bit[4:0]: step_auto_ratio In step auto mode, step ratio setting to adjust speed
0x3A06	AEC CTRL06	0x10	RW	Bit[7]: Debug mode Bit[6]: pclk_div4 0: Disabled 1: Vsub4, clock divided by 4 Bit[5]: pclk_div2 0: Disabled 1: Vsub2, clock divided by 2 Bit[4:0]: Debug mode

table 7-9 AEC registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3A07	RSVD	–	–	Reserved
0x3A08	B50 STEP	0x12	RW	Bit[7:6]: Debug mode Bit[5:0]: b50_step[13:8]
0x3A09	B50 STEP	0x70	RW	Bit[7:0]: b50_step[7:0]
0x3A0A	B60 STEP	0x0F	RW	Bit[7:6]: Debug mode Bit[5:0]: b60_step[13:8]
0x3A0B	B60 STEP	0x60	RW	Bit[7:0]: b60_step[7:0]
0x3A0C	AEC CTRL0C	0xE4	RW	Bit[7:4]: e1_max Decimal line high limit zone Bit[3:0]: e1_min Decimal line low limit zone
0x3A0D	B60 MAX	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: b60_max
0x3A0E	B50 MAX	0x06	RW	Bit[7:6]: Debug mode Bit[5:0]: b50_max
0x3A0F	WPT	0x78	RW	Bit[7:0]: WPT Stable range high limit (enter)
0x3A10	BPT	0x68	RW	Bit[7:0]: BPT Stable range low limit (enter)
0x3A11	HIGH VPT	0xD0	RW	Bit[7:0]: vpt_high
0x3A12	DEBUG MODE	–	–	Debug Mode
0x3A13	PRE GAIN	0x50	RW	Bit[7]: Not used Bit[6]: Pre-gain enable Bit[5:0]: Pre-gain value
0x3A14	MAX EXPO 50	0x03	RW	Bit[7:4]: Debug mode Bit[3:0]: max expo[19:16]
0x3A15	MAX EXPO 50	0x75	RW	Bit[7:0]: Maximum expo[15:8]
0x3A16	MAX EXPO 50	0x00	RW	Bit[7:0]: Maximum expo[7:0]
0x3A17	NIGHT MODE GAIN BASE	0x89	RW	Bit[7:2]: Debug mode Bit[1:0]: gnight_thre 00: 0x00 01: 0x10 10: 0x30 11: 0x70
0x3A18	AEC GAIN CEILING	0x03	RW	Bit[7:1]: Debug mode Bit[0]: gain_ceiling[8]

table 7-9 AEC registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3A19	AEC GAIN CEILING	0xE0	RW	Bit[7:0]: gain_ceiling[7:0]
0x3A1A	DIFF MAX	0x04	RW	Bit[7:0]: diff_max
0x3A1B	WPT2	0x78	RW	Bit[7:0]: wpt2 Stable range high limit (go out)
0x3A1C	LED ADD ROW	0x06	RW	Bit[7:0]: led_add_row[15:8] Exposure values added when strobe is on
0x3A1D	LED ADD ROW	0x18	RW	Bit[7:0]: led_add_row[7:0] Exposure values added when strobe is on
0x3A1E	BPT2	0x68	RW	Bit[7:0]: bpt2 Stable range low limit (go out)
0x3A1F	LOW VPT	0x40	RW	Bit[7:0]: vpt_low Step manual mode, fast zone low limit
0x3A20	RSVD	–	–	Reserved

table 7-10 strobe control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE	0x00	RW	Bit[7]: Strobe on Bit[6]: Reverse Bit[5:4]: Debug mode Bit[3:2]: width_in_xenon Bit[1:0]: Mode 00: Xenon 01: LED1 10: LED2 11: LED3
0x3B01~ 0x3B03	NOT USED	–	–	Bit[7:0]: Not used
0x3B04	R_FRAME_EXP2	0x04	RW	Bit[7:0]: Frame exposure time[15:8]
0x3B05	R_FRAME_EXP3	0x00	RW	Bit[7:0]: Frame exposure time[7:0]

table 7-10 strobe control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B06	STROBE FREX CTRL 0	0x04	RW	Bit[7:5]: Not used Bit[4]: STROBE mode selection in FREX mode 0: strobe width controlled by 0x3B06[3:0] 1: strobe width same as exposure time Bit[3:0]: Strobe width unit is tp
0x3B07	STROBE FREX MODE SELECT	0x08	RW	Bit[7:3]: Debug mode Bit[2]: FREX polarity 0: Low 1: High Bit[1:0]: FREX mode select 00: FREX strobe mode 1 01: FREX strobe mode 2 1x: Rolling strobe
0x3B08	STROBE FREX EXP REQ	0x00	RW	Bit[7:1]: Debug mode Bit[0]: frex_exp_req
0x3B09	FREX SHUTTER DELAY	0x02	RW	Bit[7:3]: Not used Bit[2:0]: FREX to first HREF delay (minimum 11.5 lines delay) 000: Minimum lines delay 001: 8 lines delay + minimum lines delay 010: 16 lines delay + minimum lines delay 011: 32 lines delay + minimum lines delay 100: 64 lines delay + minimum lines delay 101: 128 lines delay + minimum lines delay 110: B_FF_FD pixels delay + minimum lines delay 111: F_FF_FF pixels delay + minimum lines delay

table 7-11 D5060 registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3C00	5060HZ CTRL00	0x00	RW	Bit[7:6]: Debug mode Bit[5]: th_time_div Threshold time divide 0: Disable 1: Enable Bit[4]: row_limit_en Row limit enable 0: Disable 1: Enable Bit[3]: reverse_sigma_en Reverse sigma enable 0: Disable 1: Enable Bit[2]: band_def Band50 default value 0: 60 Hz as default value 1: 50 Hz as default value Bit[1:0]: time_cnt_thresh Threshold time count 00: 1s 01: 2s 10: 4s 11: 8s
0x3C01	5060HZ CTRL01	0x00	RW	Bit[7]: Debug mode Bit[6]: band_begin_rst Band begin reset enable 0: Disable 1: Enable Bit[5]: sum_auto_mode Sum auto mode enable 0: Disable 1: Enable Bit[4]: band_cnt_en Band counter enable 0: Disable 1: Enable Bit[3:0]: band_cnt_thresh The counter threshold for band change
0x3C02	5060HZ CTRL02	0x00	RW	Bit[7:6]: th_low_limit Bit[5:0]: th_low_light No detection under low light
0x3C03	LOW LIGHT CNT THRESH	0x00	RW	Bit[7:0]: low_light_cnt_thresh
0x3C04	SUM LOW THRESH	0x20	RW	Bit[7:0]: sum_low_thresh

table 7-11 D5060 registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3C05	SUM HIGH THRESH	0x70	RW	Bit[7:0]: sum_high_thresh
0x3C06	LM1 THRESH	0x00	RW	Bit[7:0]: lm1_th[15:8]
0x3C07	LM1 THRESH	0x00	RW	Bit[7:0]: lm1_th[7:0]
0x3C08	LM2 THRESH	0x01	RW	Bit[7:0]: lm2_th[15:8]
0x3C09	LM2 THRESH	0x2C	RW	Bit[7:0]: lm2_th[7:0]
0x3C0A	SAMPLE NUM	0x4E	RW	Bit[7:0]: sample_number[15:8]
0x3C0B	SAMPLE NUM	0x1F	RW	Bit[7:0]: sample_number[7:0]
0x3C0C	5060HZ CTRL0C	–	R	Bit[7:4]: band_cnt_r Bit[3:2]: Debug mode Bit[1]: sum50_60_sign Sign bit of sum50_60 Bit[0]: band50 0: 60Hz light 1: 50Hz light
0x3C0D~ 0x3C1E	RSVD	–	–	Reserved

table 7-12 OTP control registers

address	register name	default value	R/W	description
0x3D00	OTP SUB-ADDRESS	0x00	RW	OTP Sub Address
0x3D04	OTP DATA	0x00	RW	OTP Dump/load Data

table 7-13 BIST registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3E00	START ADDR	0x00	RW	Bit[7:0]: start_address[15:8]
0x3E01	START ADDR	0x00	RW	Bit[7:0]: start_address[7:0]
0x3E02	END ADDR	0x0F	RW	Bit[7:0]: end_address[15:8]
0x3E03	END ADDR	0xDB	RW	Bit[7:0]: end_address[7:0]

table 7-13 BIST registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3E04	OPERATION NUM	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: op_num Operation number, its range is [2,14]
0x3E05	SPECIAL DATA	0x00	RW	Bit[7:0]: special_data Data written into memory in special mode
0x3E06	SRAM ID	0x03	RW	Bit[7:6]: Debug mode Bit[5:0]: sram_id ID of selected SRAM
0x3E07	BIST CTRL07	0x20	RW	Bit[7]: Start its rising edge triggers BIST start signal Bit[6]: Restart In manual mode, its rising edge triggers BIST start signal Bit[5]: test_mode 0: Manual mode 1: Auto mode Bit[4]: special_mode When this is set, BIST will write/read data in special data register (0x3E05) Bit[3]: readonly_mode When this is set, all memories can only be read Bit[1:0]: Debug mode
0x3E08	ERR ADDR	–	R	Bit[7:0]: error_address[15:8]
0x3E09	ERR ADDR	–	R	Bit[7:0]: error_address[7:0]
0x3E0A	ERR DATA	–	R	Bit[7:0]: err_data
0x3E0B	REF DATA	–	R	Bit[7:0]: ref_data
0x3E0C	BIST CTRL0C	–	R	Bit[7:5]: Debug mode Bit[4]: Busy Bit[2:0]: err_type
0x3E0D~ 0x3E0E	RSVD	–	–	Reserved
0x3E0F	RESULT	–	R	Bit[7:6]: Debug mode Bit[3]: memory_dpc1 BIST test result Bit[2]: memory_dpc0 BIST test result Bit[1]: memory_vfifo BIST test result Bit[0]: memory_mc_iram BIST test result

table 7-13 BIST registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3E10	BIST CTRL10	0x00	RW	Bit[7:5]: vfifo_test_mode 001: sequence_read_mode 010: sequence_write_mode 011: single_read_write_mode 100: single_read_mode Bit[4:2]: reg_byte Byte of single_read_write_mode or single_read mode Bit[1:0]: Debug mode
0x3E11	VFIFO DATA WR	0x00	RW	Bit[7:0]: vfifo_data_write
0x3E12	VFIFO RD REQ	NA	RW	Bit[7:0]: vfifo_read_req When reg_sel signal is high, the value is set by input SCCB data; else, the value will be 0
0x3E13	VFIFO DATA RD	–	R	Bit[7:0]: vfifo_data_read
0x3E14	BIST DONE	–	R	Bit[7:1]: Debug mode Bit[0]: bist_done When this is written to be 1, the bist_done_clear will be 1

table 7-14 BLC registers

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x09	RW	Bit[7:1]: Debug mode Bit[1]: freeze_en If this is set, the offsets keep the original values Bit[0]: Enable 0: Disable BLC 1: Enable BLC
0x4001~ 0x4005	RSVD	–	RW	Reserved
0x4006	LONG TARGET MSB	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: l_target_blacklevel[9:8]
0x4007	LONG TARGET LSB	0x10	RW	Bit[7:0]: l_target_blacklevel[7:0]
0x4008~ 0x401C	RSVD	–	RW	Reserved
0x401D	BLC CTRL1D	0x00	RW	Bit[7:6]: Debug mode Bit[5:4]: update_mode Bit[3:2]: Debug mode Bit[1]: format_change_en Bit[0]: frame_up_flag
0x401E	FRAME CNT	0x1E	RW	Bit[7:0]: frame_cnt

table 7-15 CIF control registers

address	register name	default value	R/W	description
0x4100	CIF CTRL 00	0x00	RW	Reverse External Sensor Input Polarity Bit[7]: Source select 0: From external DVP input 1: From MIPI receiver Bit[6]: End-of-frame signal select Bit[5]: Reverse VSYNC polarity Bit[4]: Reverse HREF polarity Bit[3]: Reverse PCLK polarity Bit[2]: Reverse RBLUE polarity Bit[1]: Reverse ptn_RBLUE polarity Bit[0]: Reverse CIF RBLUE polarity

table 7-16 frame control registers

address	register name	default value	R/W	description
0x4200	FRAME CONTROL00	0x00	RW	Bit[7:3]: Debug mode Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: Frame counter reset
0x4201	FRAME CONTROL01	0x00	RW	Passed Frame Number Bit[7:4]: Debug mode Bit[3:0]: Frame ON number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode
0x4202	FRAME CONTROL02	0x00	RW	Masked Frame Number Bit[7:4]: Debug mode Bit[3:0]: Frame OFF number When both ON and OFF numbers are set to 0x00, frame control is in bypass mode
0x4203	FRAME CONTROL03	0x00	RW	Bit[7]: Debug mode Bit[6]: rblue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

table 7-17 format control registers

address	register name	default value	R/W	description
0x4302	FORMAT YMAX	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: ymax high 4 bits
0x4303	FORMAT YMAX	0xFF	RW	Bit[7:0]: ymax low byte
0x4304	FORMAT YMIN	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: ymin high 4 bits
0x4305	FORMAT YMIN	0x00	RW	Bit[7:0]: ymin low byte
0x4306	FORMAT UMAX	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: umax high 4 bits
0x4307	FORMAT UMAX	0xFF	RW	Bit[7:0]: umax low byte
0x4308	FORMAT UMIN	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: umin high 4 bits
0x4309	FORMAT UMIN	0x00	RW	Bit[7:0]: umin low byte
0x430A	FORMAT VMAX	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: vmax high 4 bits
0x430B	FORMAT VMAX	0xFF	RW	Bit[7:0]: vmax low byte
0x430C	FORMAT VMIN	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: vmin high 4 bits
0x430D	FORMAT VMIN	0x00	RW	Bit[7:0]: vmin low byte

table 7-18 system control registers

address	register name	default value	R/W	description
0x4700	DVP MODE SELECT	0x04	RW	Bit[7:4]: Debug mode Bit[3]: CCIR v select Bit[2]: CCIR f select Bit[1]: CCIR656 mode enable Bit[0]: HSYNC mode enable
0x4701	DVP VSYNC WIDTH CONTRL	0x01	RW	VSYNC Width (in terms of number of lines)
0x4702	DVP_HSYVSY_ NEG_WIDTH	0x01	RW	VSYNC Width (pixel count, high byte)
0x4703	DVP_HSYVSY_ NEG_WIDTH	0x00	RW	VSYNC Width (pixel count, low byte)
0x4704	DVP VSYNC MODE	0x00	RW	Bit[7:4]: Debug mode Bit[3:2]: r_vsyncount_sel Bit[1]: r_vsync3_mod Bit[0]: r_vsync2_mod
0x4705	DVP_EOF_VSYNC DELAY	0x00	RW	SOF/EOF Negative Edge to VSYNC Positive Edge Delay, High Byte
0x4706	DVP_EOF_VSYNC DELAY	0x00	RW	SOF/EOF Negative Edge to VSYNC Positive Edge Delay, Middle Byte
0x4707	DVP_EOF_VSYNC DELAY	0x00	RW	SOF/EOF Negative Edge to VSYNC Positive Edge Delay, Low Byte
0x4708	DVP_POL_CTRL	0x01	RW	Bit[7]: Clock DDR mode enable Bit[6]: Debug mode Bit[5]: VSYNC gated clock enable Bit[4]: HREF gated clock enable Bit[3]: No first for FIFO Bit[2]: HREF polarity reverse Bit[1]: VSYNC polarity reverse Bit[0]: PCLK polarity reverse
0x4709	BIT_TEST_PATTERN	0x00	RW	Bit[7]: FIFO bypass mode Bit[6:4]: Data bit swap Bit[3]: Bit test mode Bit[2]: 10-bit bit test Bit[1]: 8-bit bit test Bit[0]: Bit test enable
0x470A	DVP_BYP_CTRL	0x00	RW	Bypass Control High Byte
0x470B	DVP_BYP_CTRL	0x00	RW	Bypass Control Low Byte
0x470C	DVP_BYP_SEL	0x00	RW	Bit[7:5]: Debug mode Bit[4]: HREF select Bit[3:0]: Bypass select

table 7-19 MIPI transmitter registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[7]: Debug mode Bit[6]: ck_mark1_en 1: Enable clock lane mark1 when resume Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Lane select 0: Use lane1 as default data lane 1: Use lane2 as default data lane Bit[2]: Idle status 0: MIPI bus will be LP00 when no packet to transmit 1: MIPI bus will be LP11 when no packet to transmit Bit[1]: Clock lane first bits 0: Output 0x55 1: Output 0xAA Bit[0]: Clock lane dis 1: Manually set clock lane to low power mode

table 7-19 MIPI transmitter registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x4801	MIPI CTRL 01	0x03	RW	MIPI Control 01 Bit[7]: Long packet data type manual enable 0: Use MIPI_dt 1: Use dt_man_o as long packet data (see register **0x4814**[5:0]) Bit[6]: Short packet data type manual enable 1: Use dt_spkt as short packet data (see register **0x4815**[5:0]) Bit[5]: Short packet WORD COUNTER manual enable 0: Use frame counter or line counter 1: Select spkt_wc_reg_o (see {**0x4812**, **0x4813**}) Bit[4]: PH bit order for ECC 0: {DI[7:0],WC[7:0],WC[15:8]} 1: {DI[0:7],WC[0:7],WC[8:15]} Bit[3]: PH byte order for ECC 0: {DI,WC_l,WC_h} 1: {DI,WC_h,WC_l} Bit[2]: PH byte order2 for ECC 0: {DI,WC} 1: {WC,DI} Bit[1]: mark1_en1 1: after each rst release, lane 1 should send mark1 for wkup_dly_o when MIPI_sys_susp =1 Bit[0]: mark1_en2 1: after each rst release, lane 2 should send mark1 for wkup_dly_o when MIPI_sys_susp=1

table 7-19 MIPI transmitter registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x4802	MIPI CTRL 02	0x00	RW	MIPI Control 02 Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail.min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]

table 7-19 MIPI transmitter registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x4803	MIPI CTRL 03	0x5F	RW	MIPI Control 03 Bit[7:4]: Debug mode Bit[3]: Enable LP CD when HS transmits for lane1 0: Disable 1: Enable Bit[2]: Enable LP CD when HS transmits for lane2 0: Disable 1: Enable Bit[1]: Enable LP CD when LP transmits for lane2 0: Disable 1: Enable Bit[0]: Enable LP CD when LP transmits for lane1 0: Disable 1: Enable
0x4804	MIPI CTRL 04	0x8D	RW	MIPI Control 04 Bit[7:5]: Debug mode Bit[4]: Enable MIPI LP receiver to read/write registers 0: Disable - RX LP data will write to VFIFO 1: Enable Bit[3]: Address read/write register will auto add 1 1: Enable Bit[2]: LP TX lane select 0: Select lane1 to transmit LP data 1: Select lane2 to transmit LP data
0x4805	MIPI CTRL 05	0x10	RW	MIPI Control 05 Bit[7]: MIPI lane2 disable 1: Disable MIPI data lane2, lane2 will be LP00 Bit[6]: MIPI lane1 disable 1: Disable MIPI data lane1, lane1 will be LP00 Bit[2]: MIPI read/write registers disable 1: Disable MIPI access to SRB
0x4810	MIPI MAX FRAME COUNT	0xFF	RW	High Byte of Max Frame Count of Frame Sync Short Packet
0x4811	MIPI MAX FRAME COUNT	0xFF	RW	Low Byte of Max Frame Count of Frame Sync Short Packet
0x4812	MIPI_SPKT_WC_REG	0x00	RW	High Byte of Short Packet Word Counter, Manual Mode

table 7-19 MIPI transmitter registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x4813	MIPI_SPKT_WC_REG	0x00	RW	Low Byte of Short Packet Word Counter, Manual Mode
0x4814	MIPI CTRL14	0x2A	RW	MIPI Control 14 Bit[7:6]: Virtual channel of MIPI Bit[5:0]: Data type in manual mode
0x4815	MIPI_DT_SPKT	0x00	RW	Bit[7]: Debug mode Bit[6]: pclk_div 0: Use rising edge of MIPI_pclk_o to generate MIPI bus to PHY 1: Use falling edge of MIPI_pclk_o to generate MIPI bus to PHY
0x4818	MIPI_HS_ZER_MIN	0x00	RW	High byte of the minimum value for hs_zero, unit ns
0x4819	MIPI_HS_ZER_MIN	0x96	RW	Low byte of the minimum value for hs_zero, unit ns hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	MIPI_HS_TRAIL_MIN	0x00	RW	High byte of the minimum value for hs_trail, unit ns
0x481B	MIPI_HS_TRAIL_MIN	0x3C	RW	Low byte of the minimum value for hs_trail, hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	MIPI_CLK_ZER_MIN	0x01	RW	High byte of the minimum value for clk_zero, unit ns
0x481D	MIPI_CLK_ZER_MIN	0x86	RW	Low byte of the minimum value for clk_zero, clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	MIPI_CLK_PREPARE_MIN	0x00	RW	High byte of the minimum value for clk_prepare, unit ns Bit[1:0]: clk_prepare_min[9:8]
0x481F	MIPI_CLK_PREPARE_MIN	0x3C	RW	Low byte of the minimum value for clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_o
0x4820	MIPI_CLK_POST_MIN	0x00	RW	High byte of the minimum value for clk_post, unit ns Bit[1:0]: clk_post_min[9:8]
0x4821	MIPI_CLK_POST_MIN	0x56	RW	Low byte of the minimum value for clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_o
0x4822	MIPI_CLK_TRAIL_MIN	0x00	RW	High byte of the minimum value for clk_trail, unit ns Bit[1:0]: clk_trail_min[9:8]

table 7-19 MIPI transmitter registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x4823	MIPI_CLK_TRAIL_MIN	0x3C	RW	Low byte of the minimum value for clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	MIPI_LPX_P_MIN	0x00	RW	High byte of the minimum value for lpx_p, unit ns Bit[1:0]: lpx_p_min[9:8]
0x4825	MIPI_LPX_P_MIN	0x32	RW	Low byte of the minimum value for lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	MIPI_HS_PREPARE_MIN	0x00	RW	High byte of the minimum value for hs_prepare, unit ns Bit[1:0]: hs_prepare_min[9:8]
0x4827	MIPI_HS_PREPARE_MIN	0x32	RW	Low byte of the minimum value for hs_prepare hs_prepare_real = hs_prepare_min_o + Tui*ui_hs_prepare_min_o
0x4828	MIPI_HS_EXIT_MIN	0x00	RW	High byte of the minimum value for hs_exit, unit ns Bit[1:0]: hs_exit_min[9:8]
0x4829	MIPI_HS_EXIT_MIN	0x64	RW	Low byte of the minimum value for hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	MIPI_UI_HS_ZER_MIN	0x05	RW	Minimum UI Value of hs_zero, unit UI
0x482B	MIPI_UI_HS_TRAIL_MIN	0x04	RW	Minimum UI Value of hs_trail, unit UI
0x482C	MIPI_UI_CLK_ZER_MIN	0x00	RW	Minimum UI Value of clk_zero, unit UI
0x482D	MIPI_UI_CLK_PREPARE _MIN	0x00	RW	Minimum UI Value of clk_prepare, unit UI
0x482E	MIPI_UI_CLK_POST_MIN	0x34	RW	Minimum UI Value of clk_post, unit UI
0x482F	MIPI_UI_CLK_TRAIL_MIN	0x00	RW	Minimum UI Value of clk_trail, unit UI
0x4830	MIPI_UI_LPX_P_MIN	0x00	RW	Minimum UI Value of lpx_p, unit UI
0x4831	MIPI_UI_HS_PREPARE_ MIN	0x04	RW	Minimum UI Value of hs_prepare, unit UI
0x4832	MIPI_UI_HS_EXIT_MIN	0x00	RW	Minimum UI Value of hs_exit, unit UI
0x4833	MIPI_REG_MIN	0x00	RW	MIPI register address, lower bound (high byte) The address range of MIPI R/W registers is from MIPI_reg_min to MIPI_reg_max
0x4834	MIPI_REG_MIN	0x00	RW	MIPI Register Address, Lower Bound Low Byte
0x4835	MIPI_REG_MAX	0xFF	RW	MIPI Register Address, Upper Bound High Byte
0x4836	MIPI_REG_MAX	0xFF	RW	MIPI Register Address, Upper Bound Low Byte

table 7-19 MIPI transmitter registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x4837	MIPI_PCLK_PERIOD	0x10	RW	Period of pclk2x, pclk_div = 1, and 1bit decimal
0x4838	MIPI_WKUP_DLY	0x02	RW	Wakeup Delay for MIPI
0x483A	MIPI_DIR_DLY	0x08	RW	Change LP Direction Delay/2 after LP11
0x483B	MIPI_LP_GPIO	0x33	RW	Bit[7]: lp_sel1 0: Generate MIPI_lp_dir1_o automatically 1: Use lp_dir_man1 as MIPI_lp_dir1_o Bit[6]: lp_dir_man1 0: Input 1: Output Bit[5]: lp_p1_o Bit[4]: lp_n1_o Bit[3]: lp_sel2 0: Generate MIPI_lp_dir2_o automatically 1: Use lp_dir_man2 as MIPI_lp_dir2_o Bit[2]: lp_dir_man2 0: Input 1: Output Bit[1]: lp_p2_o Bit[0]: lp_n2_o
0x483C	MIPI CTRL 33	0x4F	RW	Bit[7:4]: t_lpx, unit: sclk cycles Bit[3:0]: t_clk_pre, unit: sclk cycles
0x483D	MIPI_T_TA_GO	0x10	RW	t_ta_go, unit: sclk cycles
0x483E	MIPI_T_TA_SURE	0x06	RW	t_ta_sure, unit: sclk cycles
0x483F	MIPI_T_TA_GET	0x14	RW	t_ta_get, unit: sclk cycles
0x4846	MIPI_CLIP_MAX	0x0F	RW	High Byte of the Maximum Value of MIPI Output Data Bit[7:4]: Debug mode Bit[3:0]: MIPI_clip_max[11:8]
0x4847	MIPI_CLIP_MAX	0xFF	RW	Low byte of the maximum value of MIPI output data Bit[7:0]: MIPI_clip_max[7:0]
0x4848	MIPI_CLIP_MIN	0x00	RW	High byte of the minimum value of MIPI output data Bit[7:4]: Debug mode Bit[3:0]: MIPI_clip_min[11:8]
0x4849	MIPI_CLIP_MIN	0x00	RW	Low byte of the minimum value of MIPI output data Bit[7:0]: MIPI_clip_min[7:0]
0x4850	MIPI_REG_INTR_MAN	0x00	RW	Write this register will generate a pulse of one sclk period for micro-controller interrupt

table 7-19 MIPI transmitter registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x4851	MIPI_REG_TX_WR	0x00	RW	Write this register will generate a pulse of one sclk period to MIPI_TX_LP_TX; the register write data will be sent out through MIPI ESCAPE mode
0x4852	MIPI_REG_TX_STOP	0x00	RW	Write this register will generate a pulse of one sclk period to MIPI_TX_LP_TX; MIPI_TX_LP_TX will go back to stop state.
0x4853	MIPI_REG_TA_ACK	0x00	RW	Write this register will generate a pulse of one sclk period to MIPI_TX_LP_TX to receive Turnaround command
0x4854	MIPI_REG_TA_REQ	0x00	RW	Write this register will generate a pulse of one sclk period to MIPI_TX_LP_TX to send Turnaround command
0x4860	MIPI CTRL 60	–	R	MIPI Read/Write Only Bit[7:1]: Debug mode Bit[0]: MIPI_dis_me 0: Enable MIPI read/write registers 1: Disable MIPI read/write registers
0x4861	MIPI_HD_SK_REG0	–	R	MIPI Read/Write, SCCB and MCU read only
0x4862	MIPI_HD_SK_REG1	–	R	MIPI Read/Write, SCCB and MCU read only
0x4863	MIPI_HD_SK_REG2	–	R	MIPI Read/Write, SCCB and MCU read only
0x4864	MIPI_HD_SK_REG3	–	R	MIPI Read/Write, SCCB and MCU read only
0x4865	MIPI_ST	–	R	Bit[7:6]: Debug mode Bit[5]: lp_rx_sel_i 1: MIPI_LP_RX receives LP data Bit[4]: tx_busy_i 1: MIPI_TX_LP_TX is busy sending LP data Bit[3]: MIPI_lp_p1_i MIPI low power input for lane 1p Bit[2]: MIPI_lp_n1_i MIPI low power input for lane 1n Bit[1]: MIPI_lp_p2_i MIPI low power input for lane 2p Bit[0]: MIPI_lp_n2_i MIPI low power input for lane 2n

table 7-20 ISP TOP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x86	RW	Bit[7]: lenc_en 0: Disable 1: Enable Bit[6]: remove cross tail enable 0: Disable 1: Enable Bit[5]: anti-artifact_en 0: Disable 1: Enable Bit[4]: tail_en 0: Disable 1: Enable Bit[3]: cross_en 0: Disable 1: Enable Bit[2]: bc_en 0: Disable 1: Enable Bit[1]: wc_en 0: Disable 1: Enable Bit[0]: Not used
0x5001	ISP CTRL01	0x01	RW	Bit[7:1]: Debug mode Bit[0]: awb_en 0: Disable 1: Enable
0x5002	ISP CTRL02	0x00	RW	Bit[7:2]: Debug mode Bit[1]: vap_en 0: Disable 1: Enable Bit[0]: Debug mode
0x5005~ 0x501B	RSVD	–	–	Reserved
0x5025	ISP CTRL25	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: avg_sel 00: Inputs of AVG module are from WINC 01: Inputs of AVG module are from VAP 10: Inputs of AVG module are from AWBG 11: Inputs of AVG module are from LENC

table 7-20 ISP TOP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x503D	ISP CTRL3D	0x00	RW	Bit[7]: test_pattern_en 0: Disable 1: Enable Bit[6]]: rnd_same 0: Frame-changing random data pattern 1: Frame-fixed random data pattern Bit[5:4]: bar_style When set to different value, the different type color bar will be output Bit[3]: Debug mode Bit[2]: rolling_bar 0: Disable rolling bar 1: Enable rolling bar Bit[1:0]: Debug mode
0x503E	ISP CTRL3E	0x00	RW	Bit[7:4]: rnd_seed Initial seed for random data pattern Bit[3]: squ_bw_mode 0: Output square is color square 1: Output square is black- white square Bit[2]: transparent_mode 0: Disable 1: Enable Bit[1:0]: test_pattern_type 00: Color bar 01: Random data 10: Square
0x5046	ISP CTRL46	0x09	RW	Bit[7:4]: Debug mode Bit[3]: awbg_en 0: Disable 1: Enable Bit[2:1]: Debug mode Bit[0]: isp_en 0: Disable 1: Enable

table 7-21 AWB registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5180	AWB CTRL	0x00	RW	Bit[7]: Debug mode Bit[6]: fast_awb 0: Disable fast AWB calculation function 1: Enable fast AWB calculation function Bit[5:0]: Debug mode
0x5181	AWB DELTA	0x20	RW	Bit[7:6]: Debug mode Bit[5:0]: awb_delta Delta value to increase or decrease the gains
0x5182	STABLE RANGE	0x04	RW	Bit[7:0]: stable_range
0x5183	STABLE RANGEW	0x08	RW	Bit[7:0]: stable_rangew Wide stable range
0x5184	FRAME CNT	0x02	RW	Bit[7:4]: Debug mode Bit[3:0]: frame_cnt AWB is updated once every frame_cnt frames
0x5185~ 0x518B	RSVD	–	–	Reserved
0x518C	RED GAIN LIMIT	0xF0	RW	Bit[7:4]: red_gain_up_limit Bit[3:0]: red_gain_dn_limit They are only the highest 4 bits of limitation. Maximum red gain is {red_gan_up_limit,FF} Minimum red gain is {red_gain_dn_limit,00}
0x518D	GREEN GAIN LIMIT	0xF0	RW	Bit[7:4]: green_gain_up_limit Bit[3:0]: green_gain_dn_limit They are only the highest 4 bits of limitation. Maximum green gain is {green_gan_up_limit,FF} Minimum green gain is {green_gain_dn_limit,00}
0x518E	BLUE GAIN LIMIT	0xF0	RW	Bit[7:4]: blue_gain_up_limit Bit[3:0]: blue_gain_dn_limit They are only the highest 4 bits of limitation. Maximum blue gain is {blue_gan_up_limit,FF} Minimum blue gain is {blue_gain_dn_limit,00}

table 7-21 AWB registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x518F~ 0x51BD	RSVD	–	–	Reserved
0x51BE	CAL DONE	–	R	Bit[7:1]: Debug mode Bit[0]: awb_cal_done

table 7-22 YAVG registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5680	XSTART	0x00	RW	Bit[7:4]: Not used Bit[3:0]: x_start[11:8] Horizontal start position for average window high byte
0x5681	XSTART	0x00	RW	Bit[7:0]: x_start[7:0] Horizontal start position for average window low byte
0x5682	XEND	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: x_end[11:8] Horizontal end position for average window high byte
0x5683	XEND	0x20	RW	Bit[7:0]: x_end[7:0] Horizontal end position for average window low byte
0x5684	YSTART	0x00	RW	Bit[7:4]: Not used Bit[3:0]: y_start[11:8] Vertical start position for average window high byte
0x5685	YSTART	0x00	RW	Bit[7:0]: y_start[7:0] Vertical start position for average window low byte
0x5686	YEND	0x07	RW	Bit[7:3]: Not used Bit[2:0]: y_end[10:8] Vertical end position for average window high byte
0x5687	YEND	0x98	RW	Bit[7:0]: y_end[7:0] Vertical end position for average window low byte
0x5688	WEIGHT00	0xFF	RW	Bit[7:4]: window1_weight Bit[3:0]: window0_weight

table 7-22 YAVG registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5689	WEIGHT01	0xFF	RW	Bit[7:4]: window3_weight Bit[3:0]: window2_weight
0x568A	WEIGHT02	0xFF	RW	Bit[7:4]: window5_weight Bit[3:0]: window4_weight
0x568B	WEIGHT03	0xFF	RW	Bit[7:4]: window7_weight Bit[3:0]: window6_weight
0x568C	WEIGHT04	0xFF	RW	Bit[7:4]: window9_weight Bit[3:0]: window8_weight
0x568D	WEIGHT05	0xFF	RW	Bit[7:4]: window11_weight Bit[3:0]: window10_weight
0x568E	WEIGHT06	0xFF	RW	Bit[7:4]: window13_weight Bit[3:0]: window12_weight
0x568F	WEIGHT07	0xFF	RW	Bit[7:4]: window15_weight Bit[3:0]: window14_weight
0x5690	AVG	–	R	Bit[7:2]: Not used Bit[1:0]: Average[9:8]
0x5691	AVG	–	R	Bit[7:0]: Average[7:0]
0x5692	RSVD	–	–	Reserved
0x5693	AVG CTRL00	0x00	RW	Bit[7:3]: Not used Bit[2]: flip_auto_chg 0: Disable 1: Enable Bit[1]: mirror_auto_chg 0: Disable 1: Enable Bit[0]: sun_win_en 0: Disable sub window, the average window will be set with output sizes 1: Enable sub window, the average window will be set by XSTART, XEND, YSTART and YEND

table 7-23 DPC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5780	DPC CTRL00	0x77	RW	Bit[7]: Debug mode Bit[6]: detail_en 0: Disable detail detection method 1: Enable detail detection method Bit[5:3]: Debug mode Bit[2]: smooth_en Enable using average G values when doing recovery Bit[1]: sc_en 0: Disable same channel detection 1: Enable same channel detection Bit[0]: dc_en 0: Disable different channel detection 1: Enable different channel detection
0x5781	DPC THRE	0x30	RW	Bit[7:0]: Threshold Threshold value used in recovery
0x5782~ 0x5783	RSVD	–	–	Reserved
0x5784	DPC CTRL02	0x03	RW	Bit[7:3]: Debug mode Bit[2:0]: gainbd_pwr[2:0] Range is [0, 5]
0x5785	RSVD	–	–	Reserved
0x5786	DPC GAIN LIST1	0x08	RW	Bit[6:0]: gain_list1[6:0] Used in auto mode
0x5787	DPC GAIN LIST2	0x20	RW	Bit[6:0]: gain_list2[6:0] Used in auto mode
0x5788	DPC WTHRE LIST0	0x20	RW	Bit[6:0]: wthre_list0[6:0] Used for wthre calculation in auto mode
0x5789	DPC WTHRE LIST1	0x18	RW	Bit[6:0]: wthre_list1[6:0] Used for wthre calculation in auto mode
0x578A	DPC WTHRE LIST2	0x08	RW	Bit[6:0]: wthre_list2[6:0] Used for wthre calculation in auto mode

table 7-23 DPC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x578B	DPC WTHRE LIST3	0x04	RW	Bit[6:0]: wthre_list3[6:0] Used for wthre calculation in auto mode
0x578C	DPC BTHRE LIST0	0x40	RW	Bit[7:0]: bthre_list0[7:0] Used for bthre calculation in auto mode
0x578D	DPC BTHRE LIST1	0x20	RW	Bit[7:0]: bthre_list1[7:0] Used for bthre calculation in auto mode
0x578E	DPC BTHRE LIST2	0x08	RW	Bit[7:0]: bthre_list2[7:0] Used for bthre calculation in auto mode
0x578F	DPC BTHRE LIST3	0x04	RW	Bit[7:0]: bthre_list3[7:0] Used for bthre calculation in auto mode

table 7-24 LENC registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x505A	ISP LENC OFFX MAN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: LENC x_offset manual high byte[11:8]
0x505B	ISP LENC OFFX MAN	0x00	RW	Bit[7:0]: LENC x_offset manual low byte[7:0]
0x505C	ISP LENC OFFY MAN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: LENC y_offset manual high byte[11:8]
0x505D	ISP LENC OFFY MAN	0x00	RW	Bit[7:0]: LENC y_offset manual low byte[7:0]
0x5800	GMTRX00	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_00
0x5801	GMTRX01	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_01
0x5802	GMTRX02	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_02
0x5803	GMTRX03	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_03

table 7-24 LENC registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x5804	GMTRX04	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_04
0x5805	GMTRX05	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_05
0x5806	GMTRX10	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_10
0x5807	GMTRX11	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_11
0x5808	GMTRX12	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_12
0x5809	GMTRX13	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_13
0x580A	GMTRX14	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_14
0x580B	GMTRX15	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_15
0x580C	GMTRX20	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_20
0x580D	GMTRX21	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_21
0x580E	GMTRX22	0x00	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_22
0x580F	GMTRX23	0x00	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_23
0x5810	GMTRX24	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_24
0x5811	GMTRX25	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_25
0x5812	GMTRX30	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_30
0x5813	GMTRX31	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_31
0x5814	GMTRX32	0x00	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_32
0x5815	GMTRX33	0x00	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_33
0x5816	GMTRX34	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_34

table 7-24 LENC registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x5817	GMTRX35	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_35
0x5818	GMTRX40	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_40
0x5819	GMTRX41	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_41
0x581A	GMTRX42	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_42
0x581B	GMTRX43	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_43
0x581C	GMTRX44	0x10	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_44
0x581D	GMTRX45	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_45
0x581E	GMTRX50	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_50
0x581F	GMTRX51	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_51
0x5820	GMTRX52	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_52
0x5821	GMTRX53	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_53
0x5822	GMTRX54	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_54
0x5823	GMTRX55	0x20	RW	Bit[7]: Debug mode Bit[6:0]: green_matrix_55
0x5824	BMTRX00	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_00
0x5825	BMTRX01	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_01
0x5826	BMTRX02	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_02
0x5827	BMTRX03	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_03
0x5828	BMTRX04	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_04
0x5829	BMTRX10	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_10

table 7-24 LENC registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x582A	BMTRX11	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_11
0x582B	BMTRX12	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_12
0x582C	BMTRX13	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_13
0x582D	BMTRX14	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_14
0x582E	BMTRX20	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_20
0x582F	BMTRX21	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_21
0x5830	BMTRX22	0x10	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_22
0x5831	BMTRX23	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_23
0x5832	BMTRX24	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_24
0x5833	BMTRX30	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_30
0x5834	BMTRX31	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_31
0x5835	BMTRX32	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_32
0x5836	BMTRX33	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_33
0x5837	BMTRX34	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_34
0x5838	BMTRX40	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_40
0x5839	BMTRX41	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_41
0x583A	BMTRX42	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_42
0x583B	BMTRX43	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_43
0x583C	BMTRX44	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: blue_matrix_44

table 7-24 LENC registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x583D	RMTRX00	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_00
0x583E	RMTRX01	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_01
0x583F	RMTRX02	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_02
0x5840	RMTRX03	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_03
0x5841	RMTRX04	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_04
0x5842	RMTRX10	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_10
0x5843	RMTRX11	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_11
0x5844	RMTRX12	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_12
0x5845	RMTRX13	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_13
0x5846	RMTRX14	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_14
0x5847	RMTRX20	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_20
0x5848	RMTRX21	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_21
0x5849	RMTRX22	0x10	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_22
0x584A	RMTRX23	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_23
0x584B	RMTRX24	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_24
0x584C	RMTRX30	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_30
0x584D	RMTRX31	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_31
0x584E	RMTRX32	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_32
0x584F	RMTRX33	0x12	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_33

table 7-24 LENC registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x5850	RMTRX34	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_34
0x5851	RMTRX40	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_40
0x5852	RMTRX41	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_41
0x5853	RMTRX42	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_42
0x5854	RMTRX43	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_43
0x5855	RMTRX44	0x14	RW	Bit[7:5]: Debug mode Bit[4:0]: red_matrix_44
0x5856	MAX GAIN	0x40	RW	Bit[7:0]: max_gain
0x5857	MIN GAIN	0x20	RW	Bit[7:0]: min_gain
0x5858	MIN Q	0x18	RW	Bit[7]: Debug mode Bit[6:0]: min_q
0x5859	LENC CTRL59	0x0D	RW	Bit[7:4]: Debug mode Bit[3]: ADDBLC 0: Disable BLC add back function 1: Enable BLC add back function Bit[2]: blc_en 0: Disable BLC function 1: Enable BLC function Bit[1]: Debug mode Bit[0]: autoq_en 0: Used constant Q (0x40) 1: Used calculated Q
0x585A	BR HSCALE	0x01	RW	Bit[7:4]: Debug mode Bit[3:0]: br_hscale[10:8] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x585B	BR HSCAL	0x2B	RW	Bit[7:0]: br_hscale[7:0] Reciprocal of horizontal step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block

table 7-24 LENC registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x585C	BR VSCALE	0x01	RW	Bit[7:3]: Debug mode Bit[2:0]: br_vscale[10:8] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x585D	BR VSCALE	0x92	RW	Bit[7:0]: br_vscale[7:0] Reciprocal of vertical step for BR channel. BR channel in whole image is divided into 5x5 blocks. The step is used to point to the border of the adjacent block
0x585E	G HSCALE	0x01	RW	Bit[7:4]: Debug mode Bit[3:0]: g_hscale[10:8] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x585F	G HSCAL	0x8F	RW	Bit[7:0]: g_hscale[7:0] Reciprocal of horizontal step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5860	G VSCALE	0x01	RW	Bit[7:3]: Debug mode Bit[2:0]: g_vscale[10:8] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5861	G VSCALE	0x0C	RW	Bit[7:0]: g_vscale[7:0] Reciprocal of vertical step for G channel. G channel in whole image is divided into 6x6 blocks. The step is used to point to the border of the adjacent block
0x5862~ 0x5876	RSVD	–	–	Reserved

table 7-25 VAP registers

address	register name	default value	R/W	description
0x5900	VAP CTRL00	0x01	RW	Bit[7:6]: Debug mode Bit[5]: sum_en for even-line and even-column pixels 0: Drop mode 1: Sum mode Bit[4]: sum_en for even-line and odd-column pixels 0: Drop mode 1: Sum mode Bit[3]: sum_en for odd-line and even-column pixels 0: Drop mode 1: Sum mode Bit[2]: sum_en for odd-line and odd-column pixels 0: Drop mode 1: Sum mode Bit[1]: hsub4_drop_mode 0: Output first pixel of first group and second pixel of third group This option only plays its role in 1:4 horizontal sub-sample drop mode 1: Output the first group of 4 group Bit[0]: avg_en 0: Limitation mode 1: Average mode
0x5901	VAP CTRL01	0x00	RW	Bit[7:4]: Debug mode Bit[3:2]: hsub_coef Horizontal sub-sample coefficient 00: Sub-sample 1 01: Sub-sample 2 1x: Sub-sample 4 Bit[1:0]: vsub_coef Vertical sub-sample coefficient Changing this value is not recommended

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		±200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature range[a]	-30°C to +70°C
stable image temperature range[b]	0°C to +50°C

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-30°C < T_A < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-S}	supply voltage (pixel)	2.6	2.8	3.0	V
V_{DD-DO}	supply voltage (digital I/O)	1.7	1.8/2.8	3.0	V
V_{DD-D}	supply voltage (digital core)[a]	1.425	1.5	1.575	V
V_{DD-E}	supply voltage (MIPI)	1.425	1.5	1.575	V
I_{DD-A}	active (operating) current 2592 x 1944 @ 15 fps[b]		70	80	mA
I_{DD-DO}			80	100	mA
I_{DD-A}	active (operating) current 720p @ 30fps[b]		70	80	mA
I_{DD-DO}			55	70	mA
I_{DD-A}	active (operating) current 720p @ 60fps[b]		70	80	mA
I_{DD-DO}			70	90	mA
I_{DD-A}	active (operating) current VGA @ 30fps[b]		70	80	mA
I_{DD-DO}			45	55	mA
I_{DD-A}	active (operating) current VGA @ 60fps[b]		70	80	mA
I_{DD-DO}			60	75	mA
$I_{DDS-SCCB}$[c]	standby current		40	60	µA
$I_{DDS-PWDN}$			40	60	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[d]	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}[d]	SIOC and SIOD	1.26	1.8	2.3	V

a. when internal regulator is bypassed

b. using internal regulator for DVDD and short DVDD with EVDD; DOVDD = 2.8V, The currents are for DVP output. MIPI output will results 5%-10% lower active current on I_{DD-DO}

c. external clock is stopped during measurement

d. based on DOVDD = 1.8V

8.4 AC characteristics

table 8-4 AC characteristics (T_A = 25°C, V_{DD-A} = 2.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		48		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	settling time for hardware reset			<1	ms
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-5 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using the internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

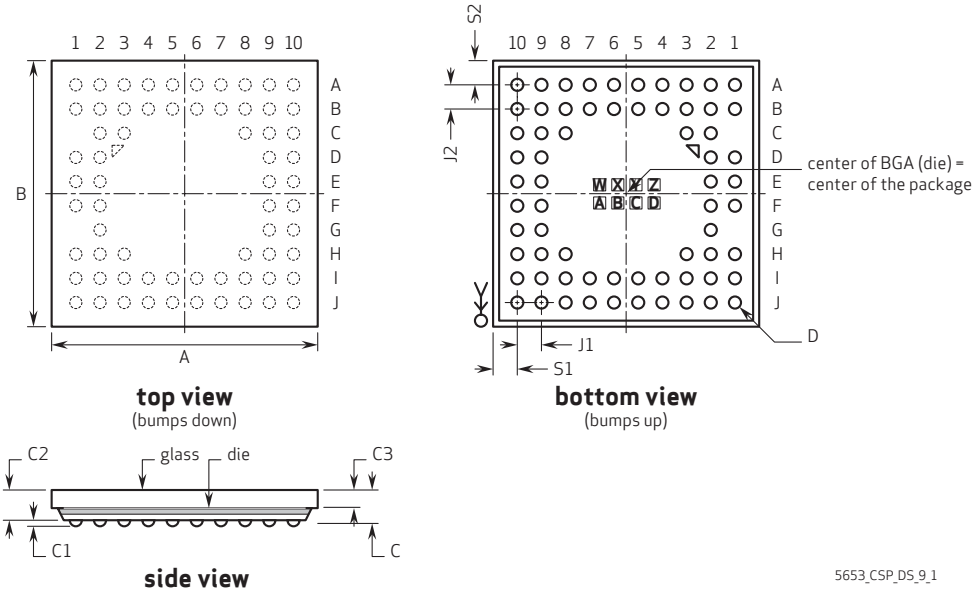


table 9-1 package dimensions (sheet 1 of 2)

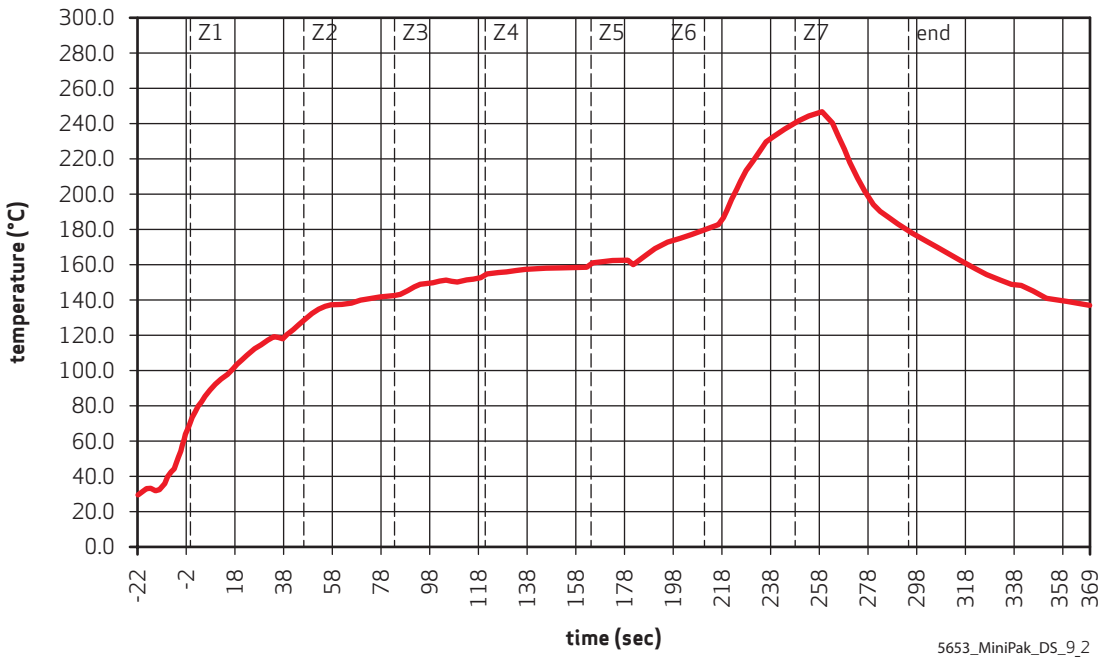
parameter	symbol	min	typ	max	unit
package body dimension x	A	6480	6505	6530	µm
package body dimension y	B	5980	6005	6030	µm
package height	C	690	750	810	µm
ball height	C1	100	130	160	µm
package body thickness	C2	575	620	665	µm
thickness of glass surface to wafer	C3	425	445	465	µm
ball diameter	D	220	250	280	µm
total pin count	N		66 (9 NC)		
pin count x-axis	N1		10		

table 9-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
pin count y-axis	N2		10		
pins pitch x-axis	J1		600		µm
pins pitch y-axis	J2		540		µm
edge-to-pin center distance analog x	S1	523	553	583	µm
edge-to-pin center distance analog y	S2	543	573	603	µm

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note

The OV5653 uses a lead-free package.

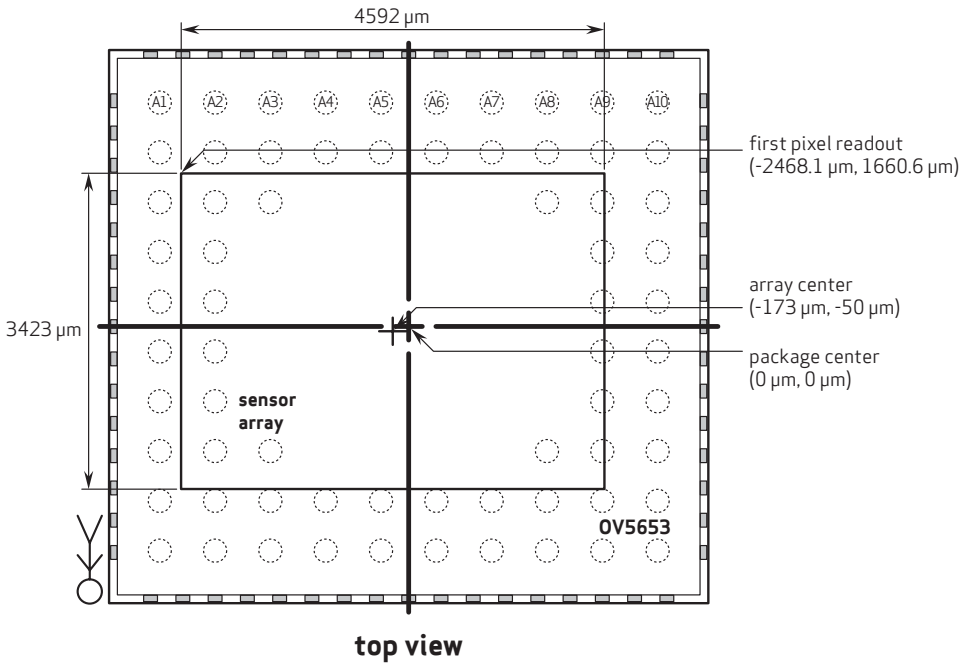
table 9-2 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

5653_CSP_DS_10_1

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A10 oriented down on the PCB.

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

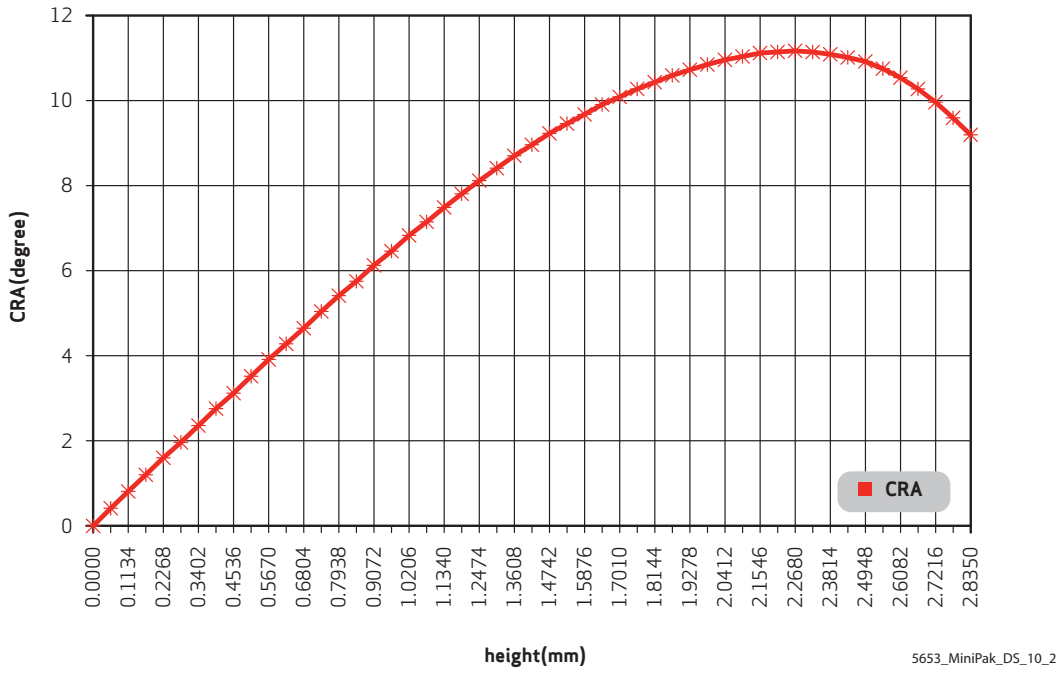


table 10-1 CRA versus image height plot (sheet 1 of 3)

field (%)	image height (mm)	CRA (degrees)
0	0	0
0.02	0.0567	0.393
0.04	0.1134	0.7857
0.06	0.1701	1.178
0.08	0.2268	1.5697
0.1	0.2835	1.9604
0.12	0.3402	2.3501
0.14	0.3969	2.7384
0.16	0.4536	3.1251

table 10-1 CRA versus image height plot (sheet 2 of 3)

field (%)	image height (mm)	CRA (degrees)
0.18	0.5103	3.51
0.2	0.567	3.8928
0.22	0.6237	4.273
0.24	0.6804	4.6503
0.26	0.7371	5.0242
0.28	0.7938	5.3941
0.3	0.8505	5.7593
0.32	0.9072	6.119
0.34	0.9639	6.4725
0.36	1.0206	6.8188
0.38	1.0773	7.157
0.4	1.134	7.4862
0.42	1.1907	7.8054
0.44	1.2474	8.1136
0.46	1.3041	8.4101
0.48	1.3608	8.6939
0.5	1.4175	8.9646
0.52	1.4742	9.2214
0.54	1.5309	9.4641
0.56	1.5876	9.6922
0.58	1.6443	9.9055
0.6	1.701	10.104
0.62	1.7577	10.2876
0.64	1.8144	10.4559
0.66	1.8711	10.6089
0.68	1.9278	10.746
0.7	1.9845	10.8666
0.72	2.0412	10.9697
0.74	2.0979	11.0539
0.76	2.1546	11.1175

table 10-1 CRA versus image height plot (sheet 3 of 3)

field (%)	image height (mm)	CRA (degrees)
0.78	2.2113	11.1581
0.8	2.268	11.173
0.82	2.3247	11.1592
0.84	2.3814	11.113
0.86	2.4381	11.0325
0.88	2.4948	10.9136
0.9	2.5515	10.7501
0.92	2.6082	10.5379
0.94	2.6649	10.274
0.96	2.7216	9.9582
0.98	2.7783	9.5958
1	2.835	9.2034

revision history

version 1.0 07.15.2009

- initial release

the clear advantage™

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