Challenge #28: Memristor Modeling and Simulation

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Overview:

This project simulates a memristor device and visualizes the I-V characteristic known as the pinched hysteresis loop using a simplified Biolek memristor model.

The aim is to demonstrate how memristors exhibit synaptic-like behavior in neuromorphic computing by observing their nonlinear current-voltage response.

Challenge Description:

Memristors are emerging circuit elements critical for neuromorphic systems, functioning as electronic synapses.

Their resistance changes based on the history of voltage and current, enabling nonvolatile memory and learning behavior such as STDP (Spike Timing-Dependent Plasticity).

Objective:

- Implement a memristor model (Biolek).
- Apply sinusoidal voltage input.
- Visualize the resulting I-V curve that exhibits a pinched hysteresis loop.

Simulation Parameters

- ON resistance (Ron): 100 Ohms
- OFF resistance (Roff): 16000 Ohms
- Memristor width (D): 10 nm
- Ion mobility (v): 1e-14 m2/V.s
- Time step (dt): 0.0001 seconds
- Total duration (T): 2 seconds

- Input: Sinusoidal voltage

The simulation integrates the state variable over time using the applied sinusoidal voltage.

The memristance is computed based on the state variable and used to determine the current.

The simulation tracks both voltage and current, ultimately producing an I-V plot.

Expected Output:

The I-V curve should form a characteristic 'pinched hysteresis loop' that passes through the origin, a hallmark of memristor behavior. This demonstrates the nonlinear and history-dependent nature of memristive devices.

Simulated I-V Curve (Pinched Hysteresis Loop)