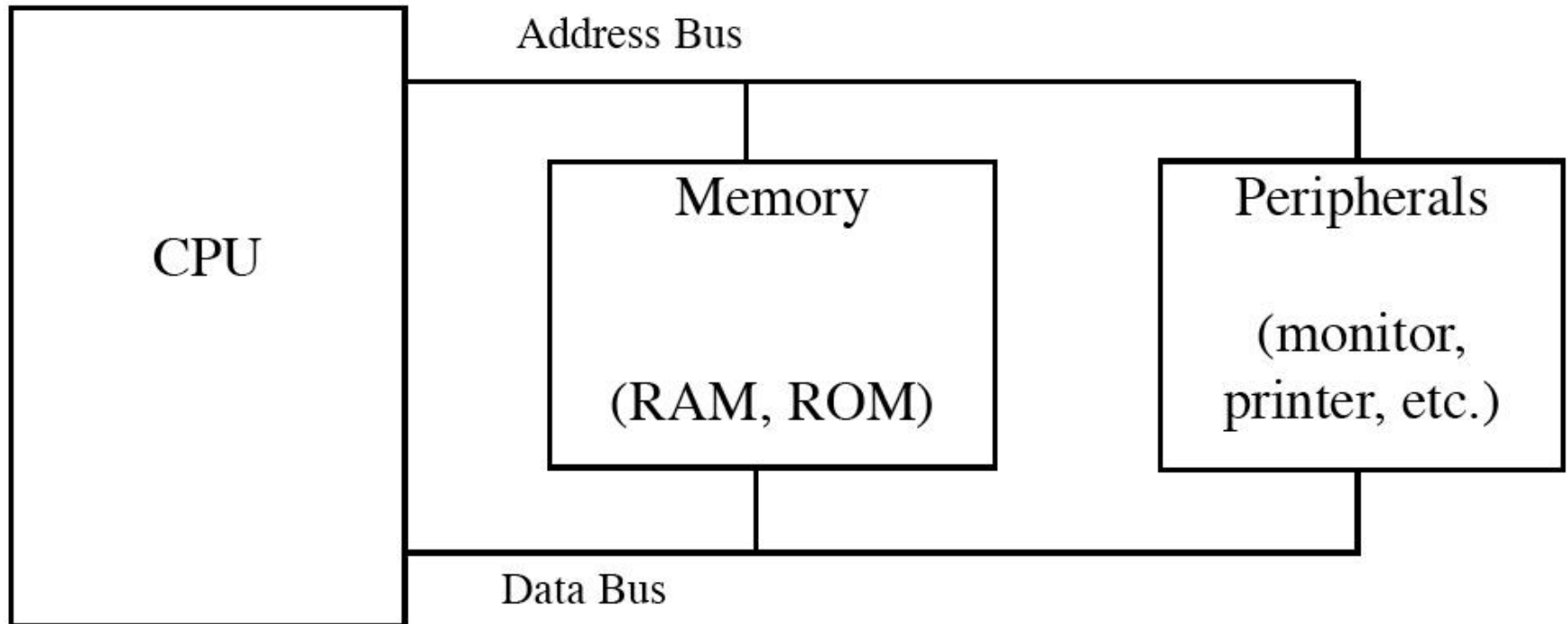
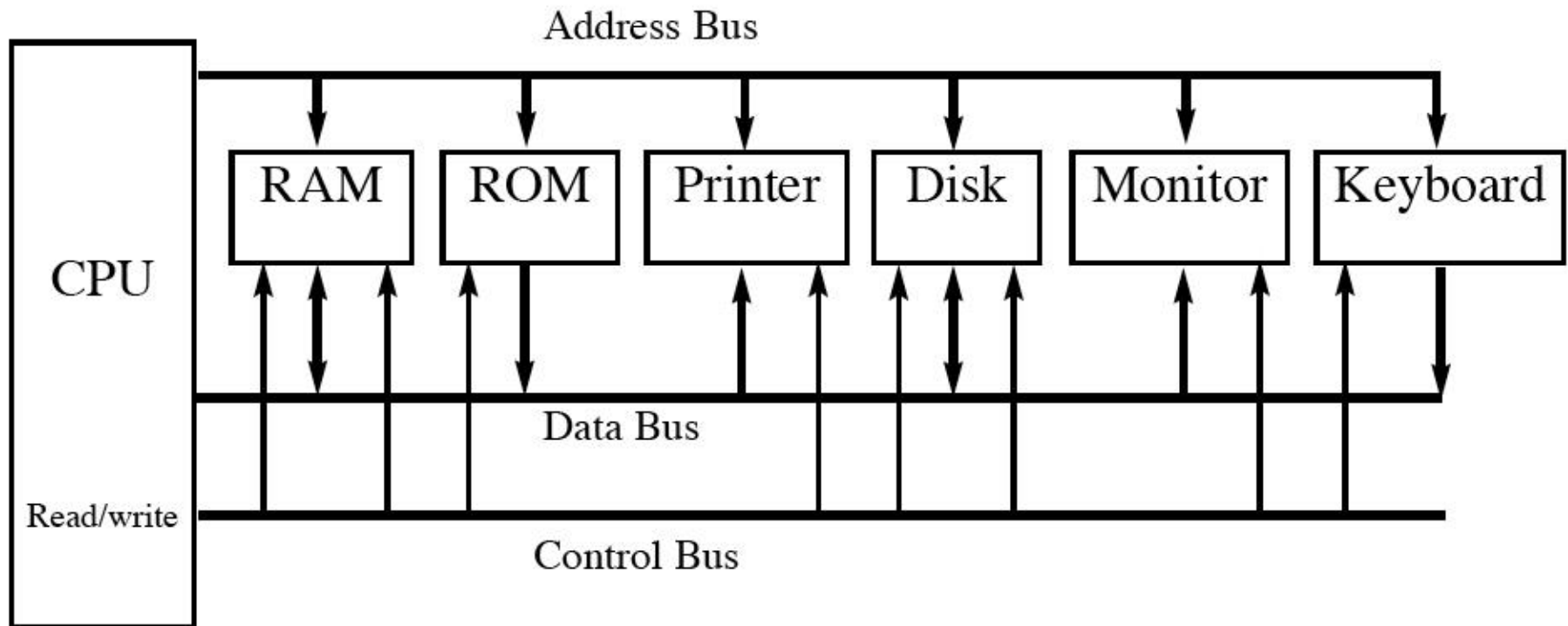


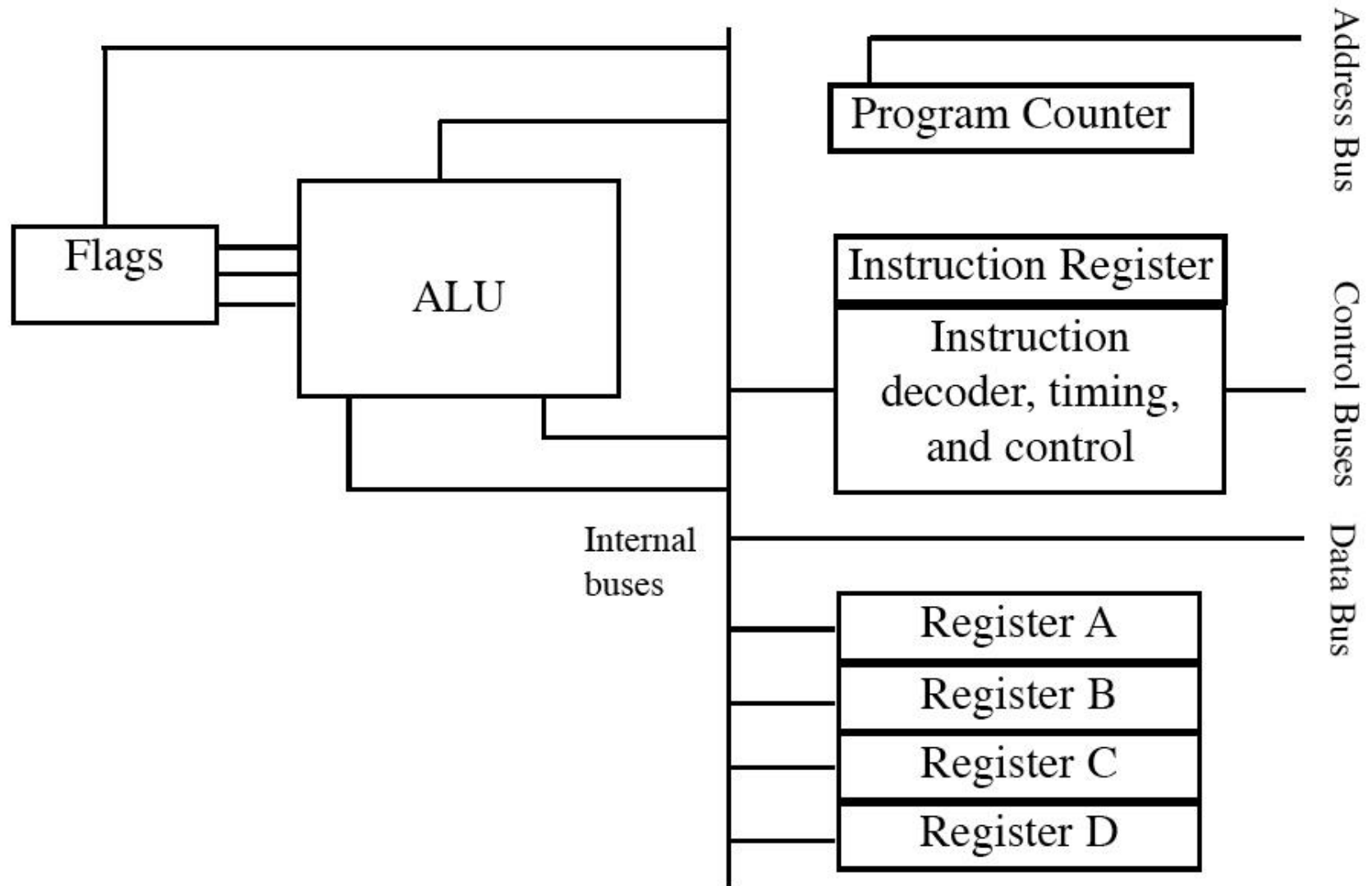
# Basic Computer Organization



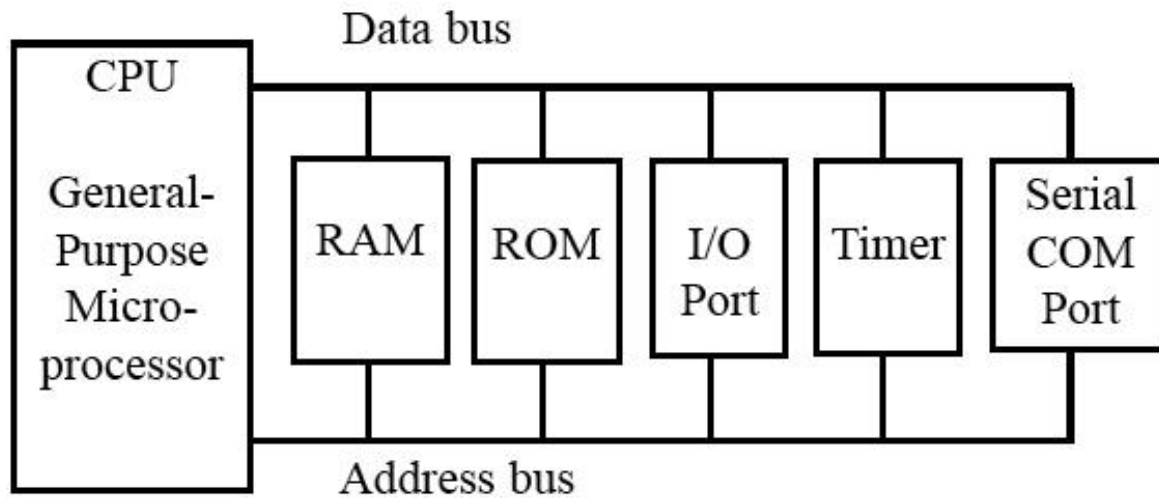
# Internal Organization of Computers with Peripherals



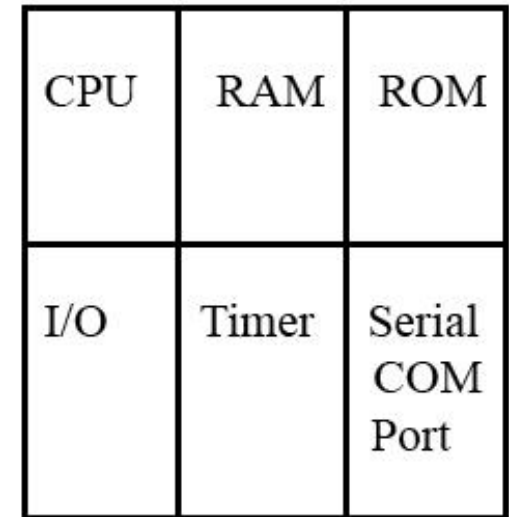
# Internal Block Diagram of a CPU



# Microprocessor System Contrasted Vs Microcontroller System

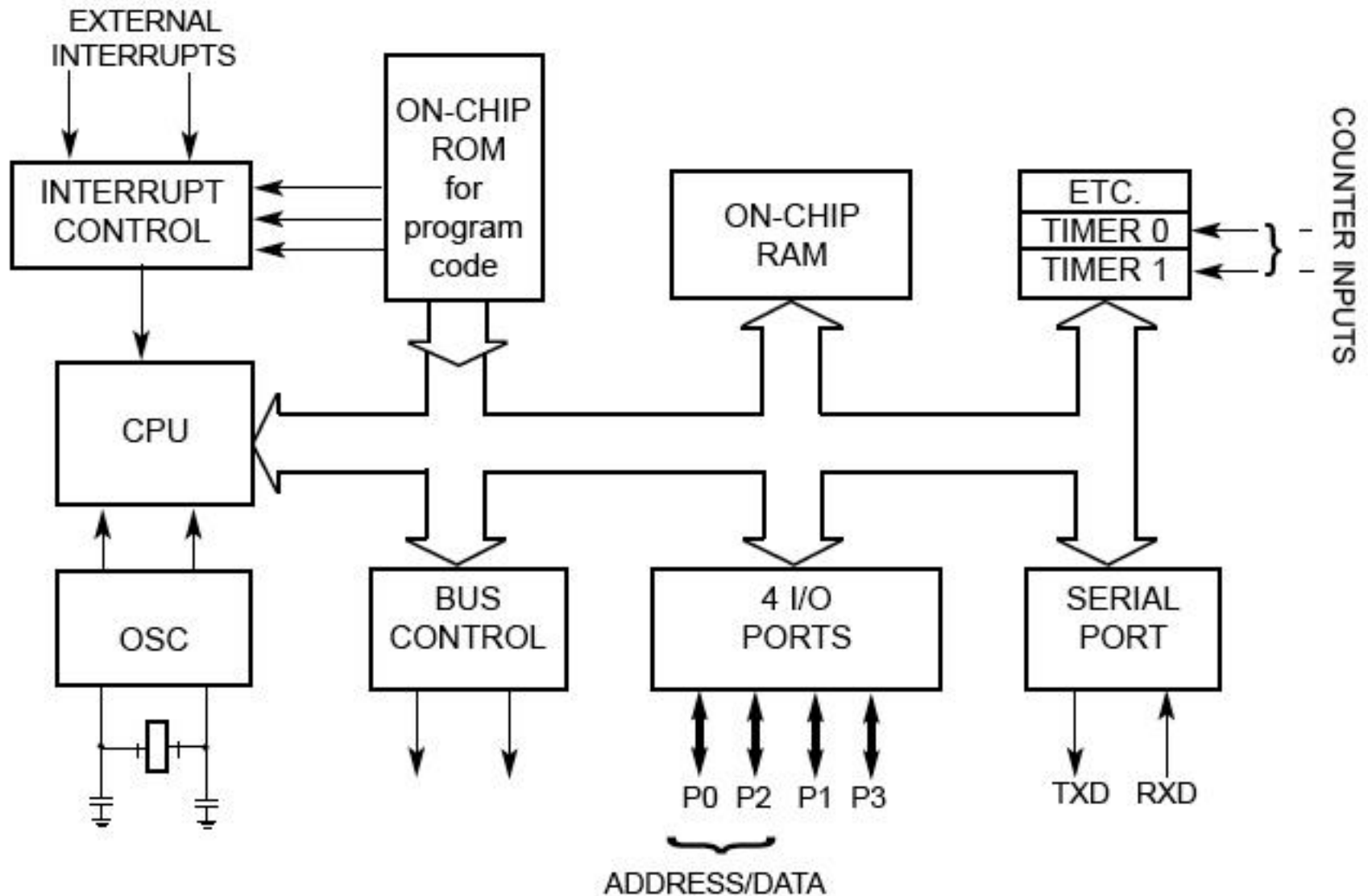


(a) General-Purpose Microprocessor System



(b) Microcontroller

# Inside the 8051 Microcontroller Block Diagram



# Examples

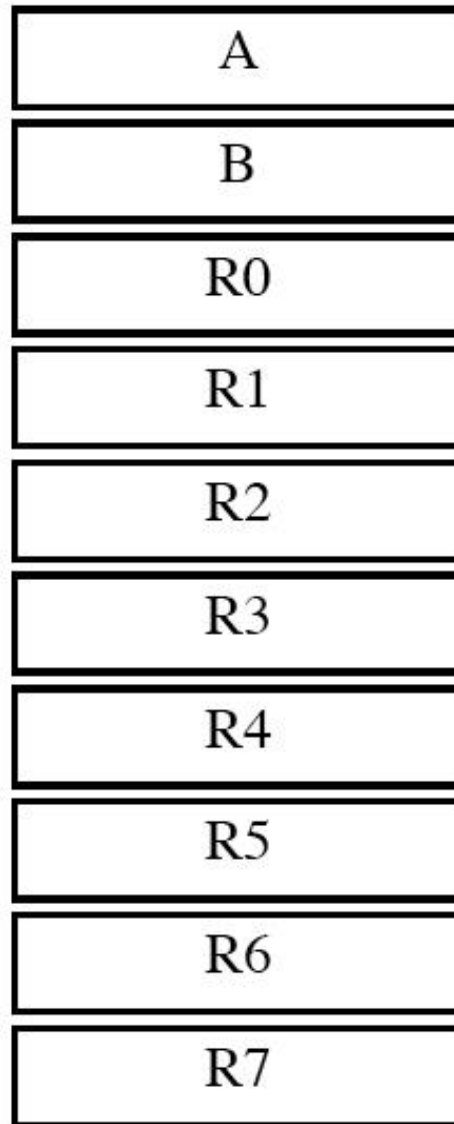
Feature	8051	8052	8031
ROM (on-chip program space in bytes)	4K	8K	0K
RAM (bytes)	128	256	128
Timers	2	3	2
I/O pins	32	32	32
Serial port	1	1	1
Interrupt sources	6	8	6

Part Number	ROM	RAM	I/O pins	Timer	Interrupt	V <sub>CC</sub>	Packaging
AT89C51	4K	128	32	2	6	5V	40
AT89LV51	4K	128	32	2	6	3V	40
AT89C1051	1K	64	15	1	3	3V	20
AT89C2051	2K	128	15	2	6	3V	20
AT89C52	8K	128	32	3	8	5V	40
AT89LV52	8K	128	32	3	8	3V	40

*Note:* “C” in the part number indicates CMOS.

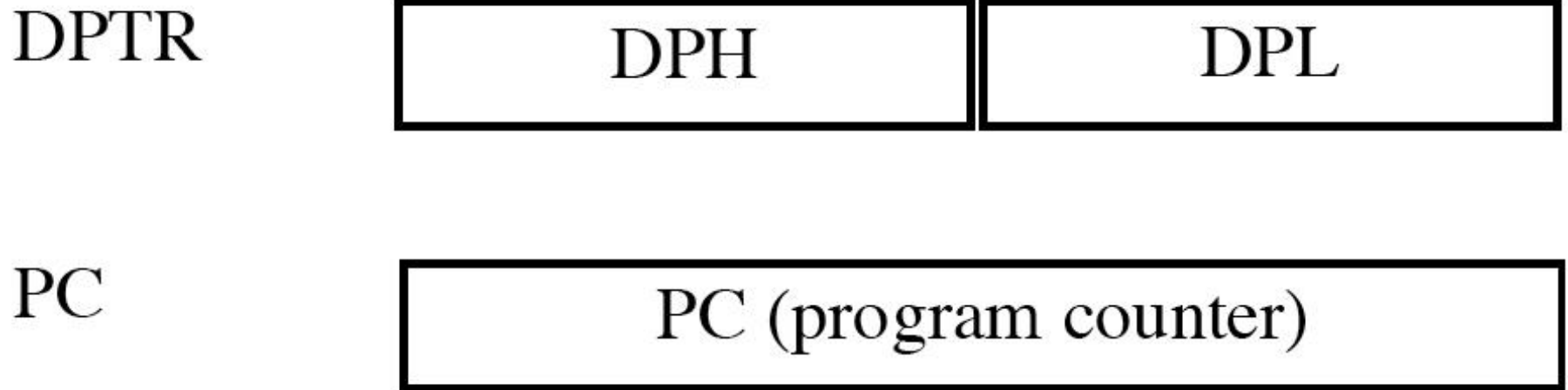
# Memory Organisation

# Registers As a Memory

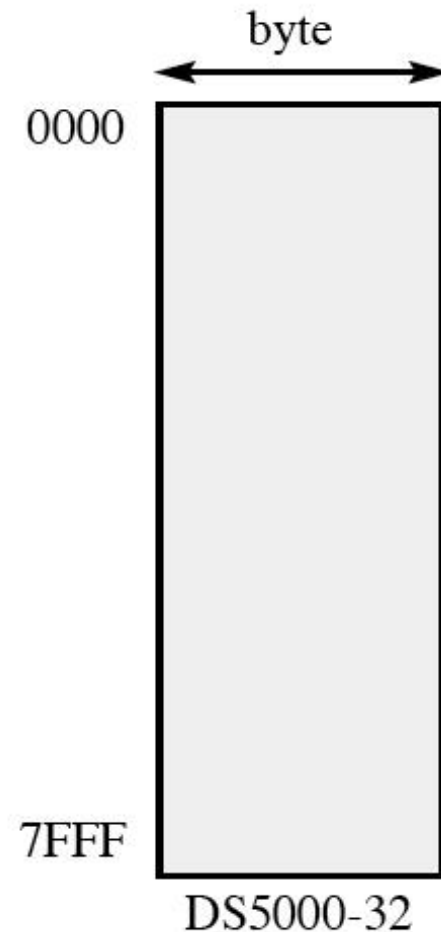
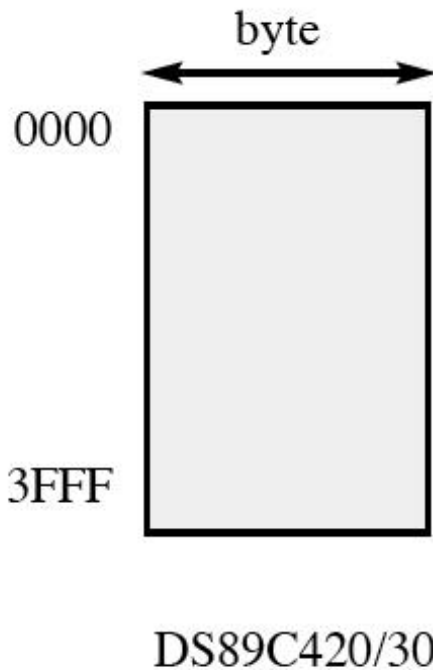
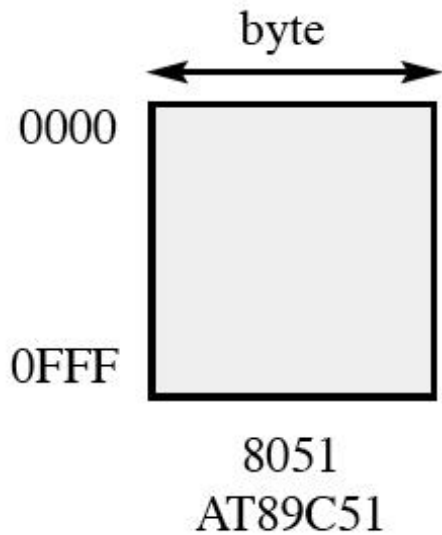




**Figure 2–1b** Some 8051 16-bit Registers



# Address Range -ROM



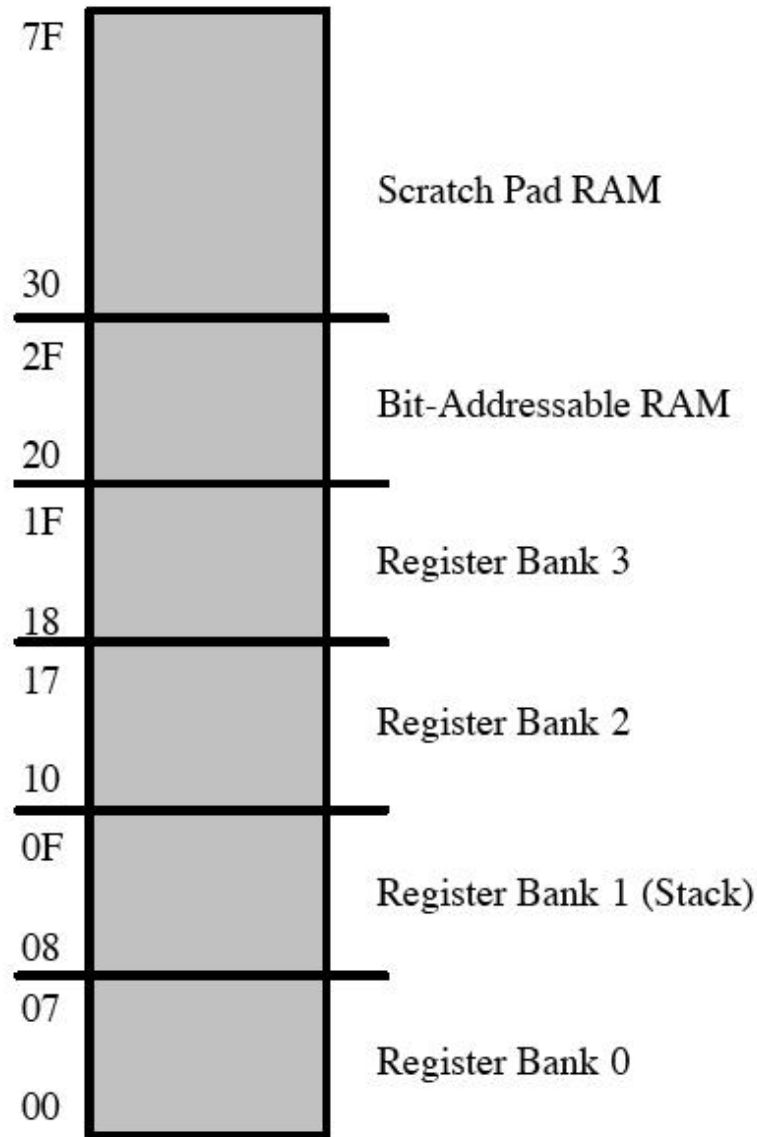
**Figure 2–4** Bits of the PSW Register

CY	AC	F0	RS1	RS0	OV	--	P
----	----	----	-----	-----	----	----	---

CY	PSW.7	Carry flag.
AC	PSW.6	Auxiliary carry flag.
F0	PSW.5	Available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1.
RS0	PSW.3	Register Bank selector bit 0.
OV	PSW.2	Overflow flag.
--	PSW.1	User-definable bit.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of 1 bits in the accumulator.

RS1	RS0	Register Bank	Address
0	0	0	00H - 07H
0	1	1	08H - 0FH
1	0	2	10H - 17H
1	1	3	18H - 1FH

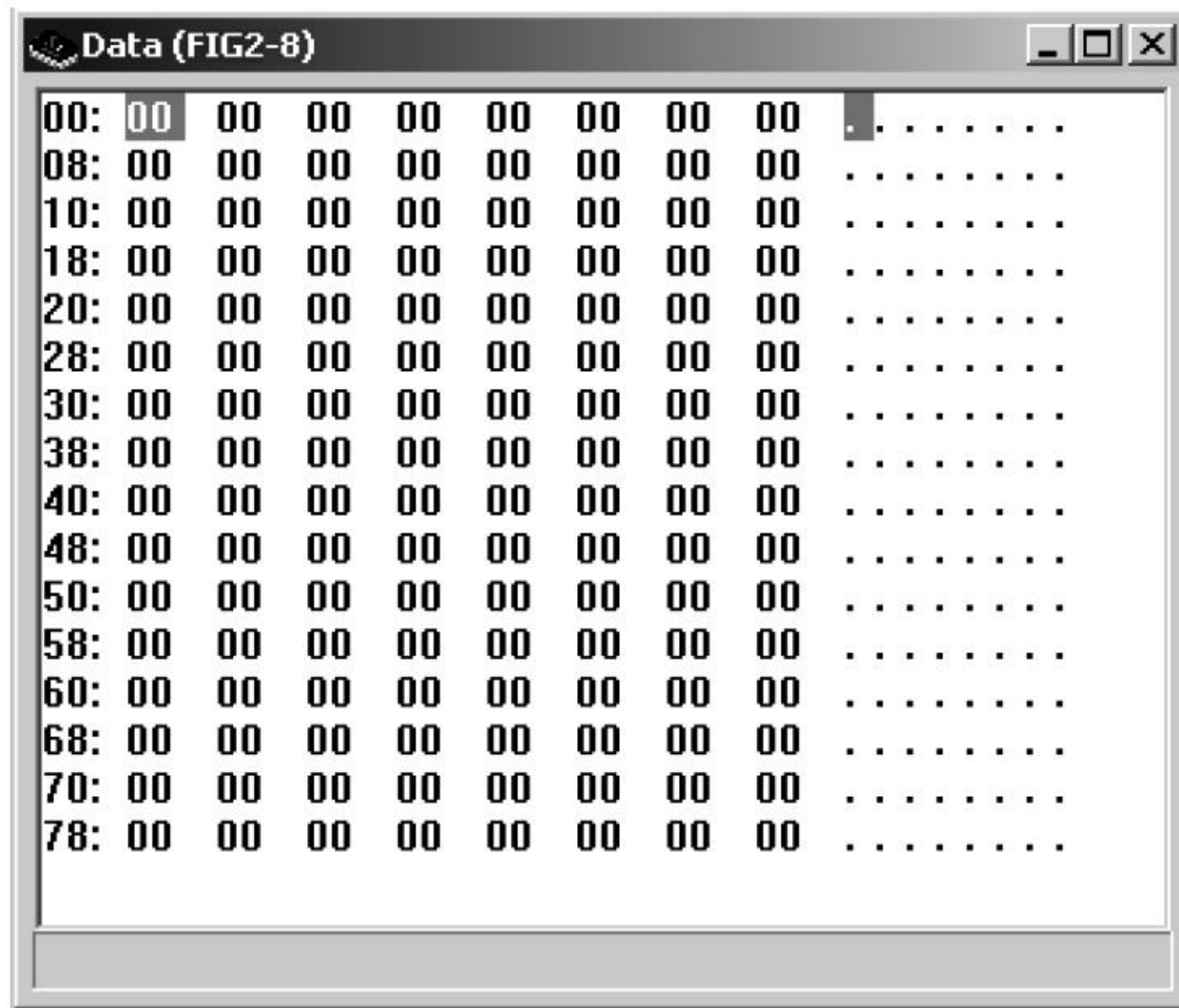
# RAM Organization



# Register Banks and their RAM Addresses

Bank 0		Bank 1		Bank 2		Bank 3	
7	R7	F	R7	17	R7	1F	R7
6	R6	E	R6	16	R6	1E	R6
5	R5	D	R5	15	R5	1D	R5
4	R4	C	R4	14	R4	1C	R4
3	R3	B	R3	13	R3	1B	R3
2	R2	A	R2	12	R2	1A	R2
1	R1	9	R1	11	R1	19	R1
0	R0	8	R0	10	R0	18	R0

**Figure 2–8** 128-Byte Memory Space from ProView 32 Simulator

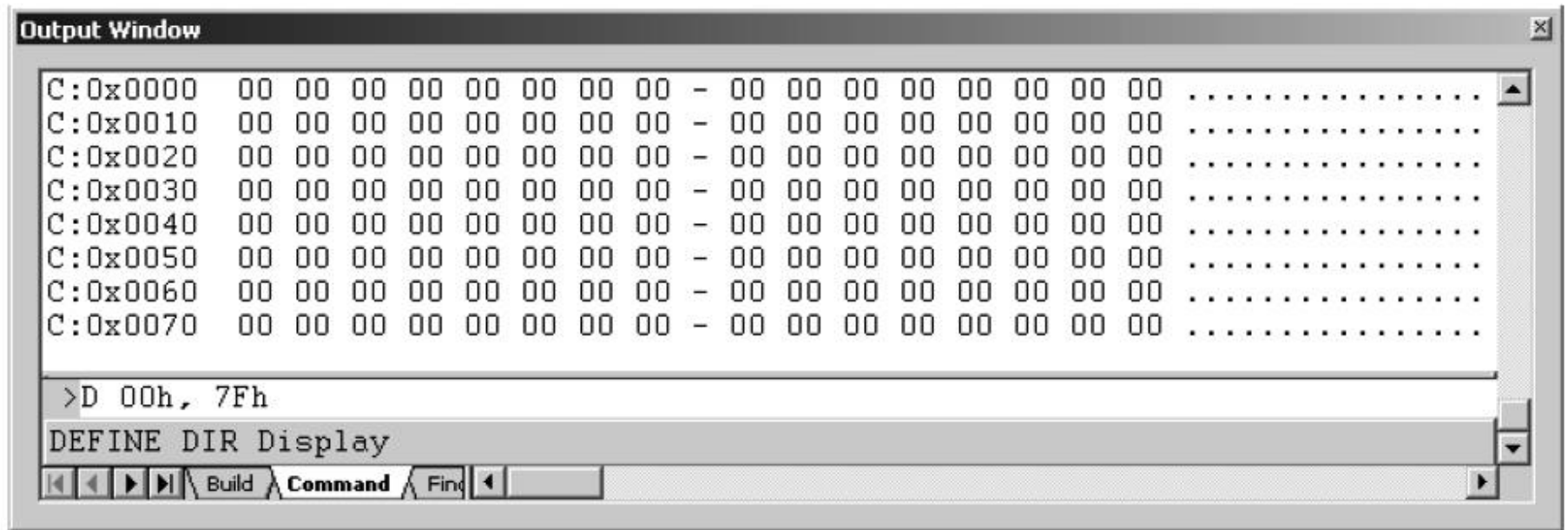


Address	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	...
00:	00	00	00	00	00	00	00	00	.
08:	00	00	00	00	00	00	00	00	.
10:	00	00	00	00	00	00	00	00	.
18:	00	00	00	00	00	00	00	00	.
20:	00	00	00	00	00	00	00	00	.
28:	00	00	00	00	00	00	00	00	.
30:	00	00	00	00	00	00	00	00	.
38:	00	00	00	00	00	00	00	00	.
40:	00	00	00	00	00	00	00	00	.
48:	00	00	00	00	00	00	00	00	.
50:	00	00	00	00	00	00	00	00	.
58:	00	00	00	00	00	00	00	00	.
60:	00	00	00	00	00	00	00	00	.
68:	00	00	00	00	00	00	00	00	.
70:	00	00	00	00	00	00	00	00	.
78:	00	00	00	00	00	00	00	00	.

**Figure 2–9** Register's Screen from Keil Simulator

Register	Value
<input type="checkbox"/> Regs	
r0	0x00
r1	0x00
r2	0x00
r3	0x00
r4	0x00
r5	0x00
r6	0x00
r7	0x00
<input type="checkbox"/> Sys	
a	0x00
b	0x00
sp	0x07
sp_max	0x07
dptr	0x0000
PC \$	C:0x0000
states	0
sec	0.00000000
<input checked="" type="checkbox"/> psw	0x00

**Figure 2–10** 128-Byte Memory Space from Keil Simulator





**Table 2–1** Instructions That Affect Flag Bits

<b>Instruction</b>	<b>CY</b>	<b>OV</b>	<b>AC</b>
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
ORL C, /bit	X		
MOV C, bit	X		
CJNE	X		

*Note:* X can be 0 or 1.

**Table 2–2** PSW Bits Bank Selection

	<b>RS1 (PSW.4)</b>	<b>RS0 (PSW.3)</b>
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1