0.35 V time-domain-based instrumentation amplifier

R. Mohan, L. Yan, G. Gielen, C. Van Hoof and R.F. Yazicioglu

A time-domain-based amplifier concept is proposed to obtain high-voltage gains with low power consumption and at an ultra-low supply voltage of 0.35 V. A prototype instrumentation amplifier designed using the proposed technique in the 180 nm technology consumes 210 nW of power and 0.1 mm^2 of the active area.

Introduction: Generic platforms with multiple sensor interfaces and long lifetimes require ultra-low-power mixed-signal system-on-chips (SoCs). Until now, the SoC power consumption, dominated by computation power, has been reduced by scaling the digital and memory voltage supply (VDD) to <0.5 V [1]. However, to reduce it further, the analogue power consumption must be reduced. But the power consumption of the analogue readout cannot be reduced by scaling VDD without trading-off the precision operation. This leads to the design of complicated power management circuits which further reduce the power efficiency [2].

The challenge of implementing a precision, low-voltage, low-power analogue readout can be explained as follows. Generally, a high-gain operational amplifier (opamp) that is used to implement the instrumentation amplifier (IA) core dominates the power consumption. High-gain opamps are needed for IA precision and gain accuracy. Traditionally, a high-voltage gain is obtained by converting the input voltage to a current (g_m) and back to the voltage via an impedance R_o, to give an overall gain of $g_m{\cdot}R_o$ (simple differential amplifier, Fig. 1*a*). Van Helleputte *et al.* [3] use a cascode structure to implement a large R_o and thereby obtain a large gain. This technique is not suited to a VDD < 0.5 V due to the limited voltage headroom present for the output signal swing. Alternatively, cascading low gain stages will be power hungry as the first stage will need a large gain, and hence a large bias current to increase g_m. Muller *et al.* [4] use a cascade structure along with partial positive-feedback (to implement a large g_m) to obtain gain. Although, this is preferred over a simple cascade solution, it is still power inefficient and offers a limited increase in gain (open-loop gain ~32 dB). Moreover, cascading increases the biasing and frequency compensation circuitry which will further increase the power consumption.

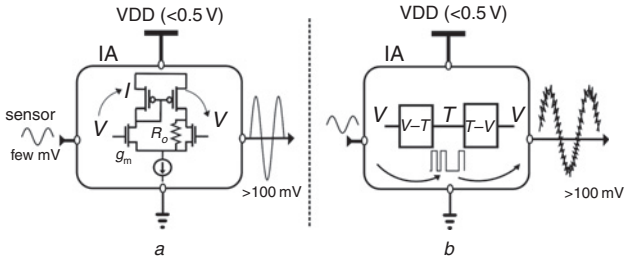

Fig. 1 *Conceptual implementation of obtaining voltage gain*

a Traditional implementation
b Time-domain concept implementation

In this Letter, we present an IA based on the time-domain opamp architecture which can operate at a VDD < 0.5 V and consumes low power. We demonstrate that the gain of the proposed opamp depends on the unity-gain bandwidth and not on output impedances. Therefore, the operation is not limited by the voltage supply to a first order. We effectively demonstrate IA operation down to 0.35 V. The IA consumes 210 nW of power.

Concept: Time-domain circuits have been well known for efficient operation in other applications such as class-D amplifiers and analogue-to-digital converters. However, as will be shown next, this technique cannot be used as is for a sensor readout.

Fig. 1*b* shows the working principle of the time-domain operation. The input voltage is converted into a time-domain signal (represented by a pulse width modulation (PWM) signal) via a voltage–time converter (*V*–*T*). The PWM signal is converted back to the voltage domain via a time–voltage converter (*T*–*V*) to complete the amplification. Consider the block-level schematic in Fig. 2. *V*–*T* block is implemented by a latched comparator with reset frequency f_s. The *T*–*V* is implemented by a charge-pump (CP) integrator. Neglect the dotted feedback loop for now. In the well-known form of *V*–*T* conversion, the input voltage, V_i, is compared with a triangular signal, V_{ramp} with slope m_1. When V_{ramp} crosses V_i, the comparator output (V_{comp}) flips to give a time-domain signal, *T*. The CP then integrates a current I_b onto a capacitor C_L (thereby generating a ramp of slope m_2) for time *T* to convert it back to the voltage domain and complete the amplification. The amplified output signal will contain high-frequency spurs which can be filtered out later in the signal chain. The gain can easily be set by the ratio of the two ramps

$$\text{gain} = \frac{V_o}{V_i} = \frac{dT}{dV_i} \cdot \frac{dV_o}{dT} \sim \left(\frac{m_2}{m_1}\right) \tag{1}$$

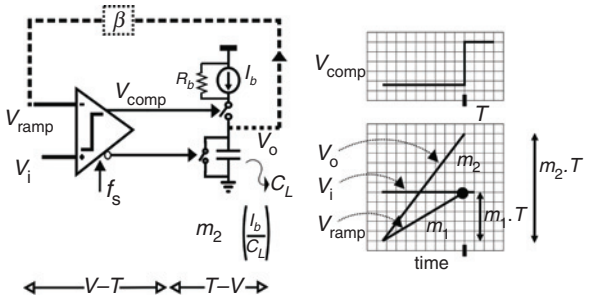

Fig. 2 *Proposed concept of obtaining voltage gain and timing diagram*

This time-domain approach will face two significant limitations when applied to the sensor readout. (i) An accurate, low noise V_{ramp} with an amplitude swing comparable with V_i will be required so that the dynamic range of the readout is not limited. (ii) The CP will not function as a 'true' integrator at near DC frequencies (<2 kHz) as extremely high current source shunt resistances, $R_b > 1$ GΩ, will be required which is not possible for VDD < 0.5 V and thereby limit the gain (1). Both these limitations can be overcome if we introduce a feedback path (denoted by the dotted line in Fig. 2). The circuit now functions similar to an asynchronous delta modulator [5]. It will generate its own reference signal with slope $m_1 = m_2 * \beta$, where β is the feedback scaling factor. The overall gain of the architecture is derived to be

$$\text{gain} = \frac{V_o}{V_i} = \frac{1}{\beta} \cdot \frac{\text{gain}_{OL}}{1 + \text{gain}_{OL}} \sim \frac{1}{\beta} \forall\, \text{gain}_{OL} \gg 1 \tag{2}$$

$$\text{gain}_{OL} \sim \frac{1}{\beta} \cdot \left(\frac{\pi f_s^2}{\omega_u}\right) \tag{3}$$

where gain_{OL} is the small-signal open-loop gain, τ is the time constant of the CP and ω_u is the unity-gain bandwidth of the latch transistors of the comparator. The gain depends on f_s and ω_u (3). The advantages of the approach can now be discussed. Irrespective of the gain of the CP, a high gain can be implemented by choosing the appropriate f_s and ω_u. The low-frequency noise of the ramp m_2 will be suppressed by the comparator gain and hence the accuracy requirements for the reference signal will be greatly relaxed. Since ω_u depends on the transconductance and the output capacitance, the gain can be set independent of VDD, without requiring the stacking of transistors and thus the opamp can be operated at low VDD. Although, increasing f_s and ω_u to increase gain may require an increase in current, the latching action of the comparator and a low VDD will ensure a lower power consumption than a traditional voltage gain opamp.

To maximise gain_{OL} and hence the overall gain, ω_u should be as small as possible for a given f_s (3). In this respect, the design of the comparator differs from its conventional applications, wherein ω_u should be as large as possible irrespective of f_s. The value of τ in (3) will be decided by the slew-rate requirement at the output node. The maximum obtainable gain will be decided by the maximum possible f_s. Since the noise of the latch is inversely proportional to f_s [6], it will place an upper limit on the value of f_s.

IA implementation and measurement: To demonstrate the capabilities of the opamp, a prototype fully integrated and differential IA with capacitive feedback has been designed and is presented (Fig. 3). Central to the concept of the time domain opamp is the implementation of a low-voltage, high-frequency comparator. For this, a structure similar to a double-tail latched amplifier [7] is chosen and designed according to (3). In this design, f_s is 1 MHz. The noise of the comparator will need to be suppressed. The effect of the charge kick-back of the comparator will also need to be reduced as it will lead to an increase in nonlinearity. This is done by introducing a preamplifier with gain A prior to the latch. The input-referred noise (IRN) will now be decided by the preamplifier. Thanks to the architecture, A need not be high, as required in conventional cascade opamps. Hence, the preamplifier does not need a large bias current, thereby saving power. A should be just high enough to suppress the latch non-idealities (~20 dB in this design). The preamplifier also acts as an anti-alias filter prior to the sampling at the comparator stage. The jitter of f_s does not matter due to the differential nature of the structure. The switches of the CP integrator are designed using transmission gates and are sized so as to minimise the effect of charge injection. Pseudo-resistors ensure that the input-referred DC offset is not amplified as it will limit the linearity of the current sources in the CP.

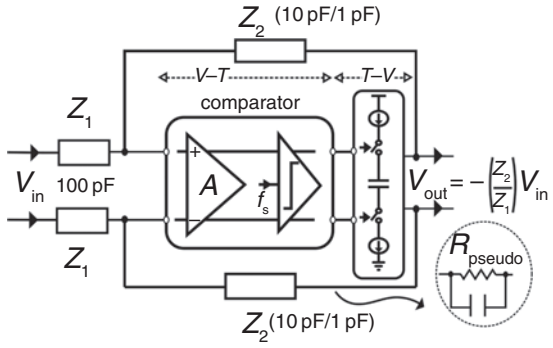

Fig. 3 *Proposed time-domain IA*

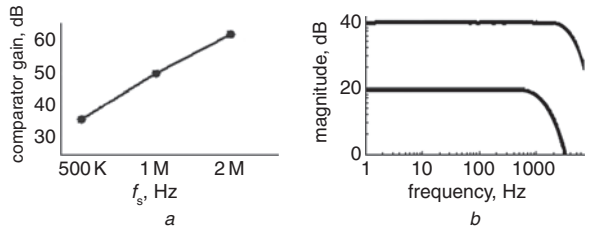

Fig. 4 *Comparator gain and overall IA gain*

a Simulated PSS open-loop DC gain of comparator in Fig. 3
b Measured overall IA gain for $f_s = 1$ MHz

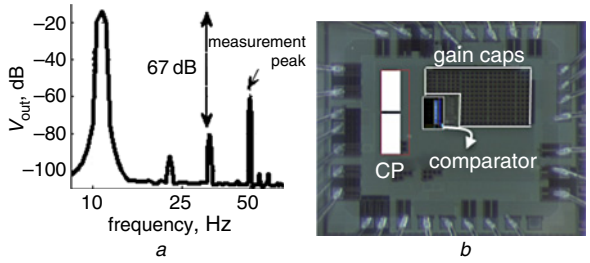

Fig. 5 *Frequency spectrum and chip photograph*

a Measured frequency spectrum for 200 mVpp output at 11 Hz
b Chip photograph

The design is implemented in 180 nm technology, and occupies a core area (without the feedback impedances) of 0.1 mm^2. It functions at 0.35 V and consumes 210 nW of power. To verify (3), Fig. 4*a* shows the simulated comparator gain, obtained through periodic steady-state (PSS) analysis, for $f_s = 500$ kHz, 1 and 2 MHz and $1/\beta = 100$. As can be observed, the gain increases by ~4× (12 dB) while doubling f_s. Fig. 4*b* shows the measured magnitude response of the complete IA for overall gains of 20 and 40 dB. The gain is changed by changing the value of the feedback capacitors. The lowpass cutoff frequency is lower for a gain of 20 dB as the load capacitance at V_{out}, which includes the feedback capacitance, increases. Fig. 5*a* shows the measured frequency spectrum for an 11 Hz signal for a 200 mV_{pp} output amplitude. The IA achieves a SFDR of 67 dB. The chip photograph is shown in Fig. 5*b*. Table 1 summarises the measurement results obtained and compares them with the existing state-of-the-art. The presented architecture operates with the lowest supply voltage and the lowest power consumption.

Table 1: Summary and comparison of measurement results

Parameter	This work	[4]	[3]
Opamp type	Time-based	Cascade, positive feedback	Cascode
Voltage supply (V)	0.35	0.5	1.2
Overall gain (dB)	20/40	[a]32 (open-loop gain)	37
Power	210 nW	4.13 µW	6 µW
Thermal IRN floor (nV/rtHz)	130	43	130
Total harmonic distortion	0.3% at 11 Hz (output 90% VDD)	2% at 2 kHz	1% (output 90% VDD)
Active area (mm^2)	0.1	0.008	1.48 ([a]estimated)
Technology (nm)	180	65	180

Conclusion: We have demonstrated a time-domain-based IA architecture that can be operated at supply voltages as low as 0.35 V while consuming only 210 nW. This is relevant towards achieving low-voltage, low-power, analogue readout for sensor SoCs with long lifetimes.

8 July 2014
doi: 10.1049/el.2014.2471

R. Mohan, L. Yan, G. Gielen, C. Van Hoof and R.F. Yazicioglu (*IMEC, Kapeldreef 75, Leuven 3001, Belgium*)

E-mail: rachit.mohan@imec.be

G. Gielen: Also with K.U. Leuven, Naamsestraat 22, Leuven 3000, Belgium

References

1 Zhang, Y., Zhang, F., Shakhsheer, Y., Silver, J.D., Klinefelter, A., Nagaraju, M., Boley, J., Pandey, J., Shrivastava, A., Carlson, E.J., Wood, A., Calhoun, B.H., and Otis, B.P.: 'A batteryless 19 µW MICS/ISM-band energy harvesting body sensor node SoC for ExG applications', *IEEE J. Solid-State Circuits*, 2013, **48**, (1), pp. 199–213
2 Carlson, E., Strunz, K., and Otis, B.: '20 mV input boost converter for thermoelectric energy harvesting'. 2009 Symp. on VLSI Circuits, Kyoto, Japan, June 2009, pp. 162–163
3 Van Helleputte, N., Kim, S., Kim, H., Kim, J.P., Van Hoof, C., and Yazicioglu, R.F.: 'A 160 µA biopotential acquisition IC with fully integrated IA and motion artifact suppression', *IEEE Trans. Biomed. Circuits Syst.*, 2012, **6**, (6), pp. 552–561
4 Muller, R., Gambini, S., and Rabaey, J.M.: 'A 0.013 mm^2, 5 µW, DC-coupled neural signal acquisition IC with 0.5 V supply', *IEEE J. Solid-State Circuits*, 2012, **47**, (1), pp. 232–243
5 Booton, R.C.: 'Nonlinear control systems with random inputs', *IRE Trans. Circuit Theory*, 1954, **1**, (1), pp. 9–18
6 Allen, P., and Holberg, D.: 'CMOS analog circuit design' (Oxford University Press, New York, 2002, 2nd edn)
7 Schinkel, D., Mensink, E., Klumperink, E., Van Tuijl, E., and Nauta, B.: 'A double-tail latch-type voltage sense amplifier with 18 ps setup + hold time'. IEEE Int. Solid-State Circuits Conf., ISSCC 2007, Dig. Tech. Pap., San Francisco, CA, USA, February 2007, pp. 314–605