28.5 A 0.6V 0.015mm² Time-Based Biomedical Readout for Ambulatory Applications in 40nm CMOS

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Emerging applications in personal healthcare require sensor SoCs with low area, low power and a high dynamic range. Design in small-scale technologies can reduce the power and area of digital processing. However, due to the accompanied reduced supply voltage (V_{DD}), the analog front-end (AFE) faces significant challenges in maintaining a large dynamic range in a power- and area-efficient manner [1-3]. A large dynamic range is important to handle the large signals expected during motion [1]. In this paper, we demonstrate a 0.6V ECG readout in 40nm technology for ambulatory applications. It can handle up to 40mV$_{pp}$ AC-signal and up to 300mV DC-electrode offset while consuming 3.3µW power and 0.015mm² area. These results are achieved by implementing a time-domain-based readout architecture that focuses on scalable design techniques and especially avoids high-gain opamps and large passives. The AFE achieves more than 5× increase in AC dynamic range compared with previous work with similar silicon area and similar V_{DD} [2], without compromising on the power consumption (see Fig. 28.5.6).

Figure 28.5.1 illustrates the block diagram of the time-based AFE (T-AFE). The input voltage is converted into a 2b differential digital output via a time-based ADC (T-ADC) and then decimated by an off-chip cascaded-integrator-comb (CIC) filter to obtain the ECG signal and the heart-rate information. An on-chip digital DC-offset loop also takes in the 2b digital output and feeds it back to the T-ADC input to reduce the input offset via a DAC. A key benefit of T-ADC is that its dynamic range is decoupled from V_{DD}, unlike voltage-based ADCs, allowing it to handle larger amplitude signals at low V_{DD}. Furthermore, direct interface of the T-ADC to the sensors enables us to avoid instrumentation amplifiers and buffers that do not scale well with technology [4], whereas the mixed-signal feedback avoids large AC-coupling capacitors, saving area [2].

Although, time-based ADCs exist [4], their power consumption is too high to be used in ambulatory biomedical applications and their implementation is not suited for technology scaling. We propose a low-power T-ADC architecture. Figure 28.5.2 shows the conceptual diagram of the traditional [4] and the proposed T-ADC. In the traditional concept, the input signal, x, is converted into a time-domain pulse-width modulated (PWM) signal, p, by comparing it to a reference ramp signal denoted by x_r and then converted into a digital value by passing it through a simple digital low-pass filter. For proper operation, the frequency of x_r needs to be much higher than that of x and the comparator should have negligible delay. These requirements lead to a power-consuming implementation because both the comparator and the ramp generator have to handle a large dynamic range at relatively high frequencies (>1MHz). We propose utilizing a closed-loop implementation of the above approach (Fig. 28.5.2). The loop functions similarly to a hysteretic delta modulator. Since the loop is nonlinear, it oscillates at a certain frequency to generate its own ramp signal, and the output of the comparator is a PWM signal as before. However now, at low frequencies, the DC-loop-gain of the feedback loop ensures a virtual ground at the comparator input. Thus, unlike [4], the comparator and the ramp integrator do not have to handle a large dynamic range. This allows us to utilize a dynamic comparator (sample frequency f_{clk}) to implement a low-power, high-speed comparator. The effect of noise folding can be reduced by adding a preamplifier. The output of the comparator is then converted to a digital value by passing it through a digital filter $H_1(z)$. In the present work, the CIC filter (Fig. 28.5.1) implements $H_1(z)$. The maximum x that can be handled is determined by the maximum time deviation at the output, i.e., the PWM time period, is set by the input signal frequency, as opposed to V_{DD} in a traditional voltage-based ADC. The input-referred noise is determined by the noise floor, which comprises quantization noise, and the device noise of the comparator and H(s).

Figure 28.5.3 depicts the block-level implementation of the T-ADC. It comprises of pseudo-differential stages, with each stage implementing the closed-loop concept presented above. The charge-pump integrators (CP) implement the 1b DAC and H(s).The DC-offset is reduced at the input of the T-ADC by the digital reduction loop and a 7b binary-weighted current DAC. The reset counter implements the digital integrator that is required to obtain the DC-offset information from the output of the T-ADC. Chopping is used to reduce the flicker noise while keeping the area of the transistors small. The gate-leakage current at the input transistors of the comparator increase the input-referred noise and reduce the input impedance. Hence, thick-oxide transistors are used at the input. However, this leads to an increased threshold voltage (0.55V) and thereby reduces the maximum input signal swing that the input stage can handle. The pseudo-differential architecture is employed so as to halve the signal swing seen by each stage. A significant challenge of a pseudo-differential architecture is the reduction of the feedback integrator noise. We implement a resistor to shunt the current noise of CP and I-DAC and reduce the voltage noise at low frequencies. While, this limits the signal swing to some extent, it does not compromise the required dynamic range.

Figure 28.5.4 shows the transistor-level schematic of the comparator. To implement a low-voltage, high-speed comparator, a low-voltage latched comparator with a simple differential amplifier as a preamplifier is designed. To save area, the anti-alias filter is implemented by the parasitic capacitances at the drain node of the preamplifier. Monte-Carlo simulations confirm that the effect of PVT variations do not considerably impact the effect of noise folding. The quantization noise floor is reduced by increasing f_{clk} to 25MHz. A low V_{DD}, small-scale technology and dynamic operation ensure that the power consumption of the comparator is low (1.6µW). To minimize the clock generator power, the required clock accuracy is minimized by placing the clock transistors at common-mode nodes. This, along with chopping, ensures that the required accuracy (<600ps$_{pp}$) is well within the range that is required in a standard digital circuit [5].

The design is implemented in TSMC 40nm CMOS process at 0.6V. The core area of the complete T-AFE is 0.015mm² while consuming 3.3µW of power. Figure 28.5.5 shows the input-referred noise (IRN) spectrum of the T-AFE. The noise increases slightly at larger offsets due to increase in current noise from the offset DAC, but remains within the range required by the application [6]. Figure 28.5.5 also shows an FFT plot for a 5mV$_{pp}$ input signal and a measured ECG signal. To verify the large dynamic range capability, the system is evaluated by acquiring an ECG signal from the noise-stress database [7]. The system does not saturate and maintains a good beat detection capability even in presence of large motion (~40mV$_{pp}$).

Figure 28.5.6 shows the performance and the comparison with state-of-the-art solutions. The proposed AFE can handle an increase in AC dynamic range of input signals while keeping the V_{DD} and the area very low and the noise specifications within acceptable biomedical signal acquisition limits. These specifications not only enable development of low cost, low power multi-sensor SoCs for ambulatory medical applications, but also at the same time open further avenues for <40nm AFE design.

References:

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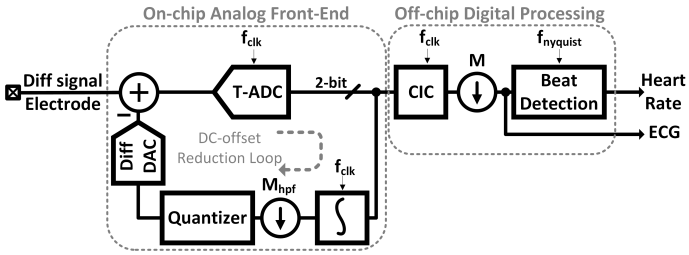
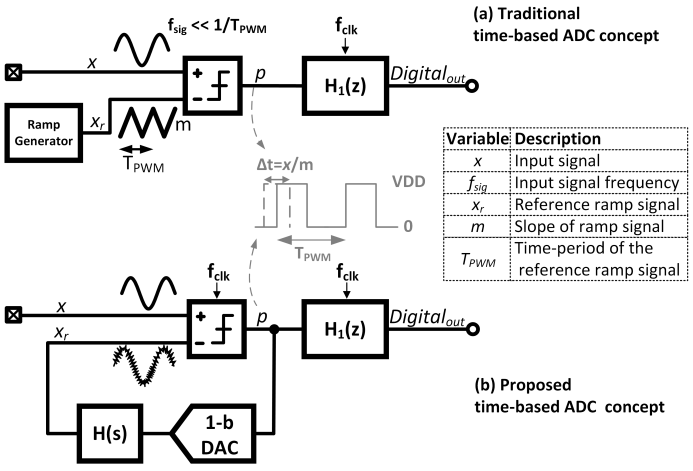


Figure 28.5.1: Time-domain-based analog front-end (T-AFE).



Variable	Description
x	Input signal
f_{sig}	Input signal frequency
x_r	Reference ramp signal
m	Slope of ramp signal
T_{PWM}	Time-period of the reference ramp signal

Figure 28.5.2: Conceptual block diagram of traditional (above) and proposed (below) time-based ADC.

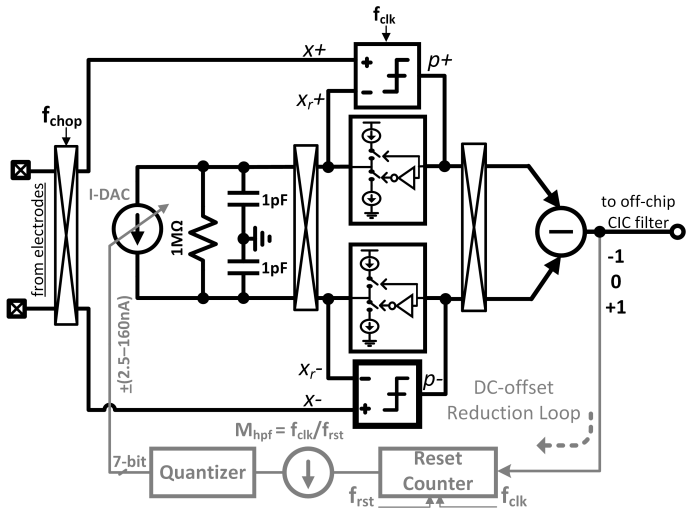


Figure 28.5.3: Implemented block-level architecture of the time-domain ADC and the DC-offset reduction loop.

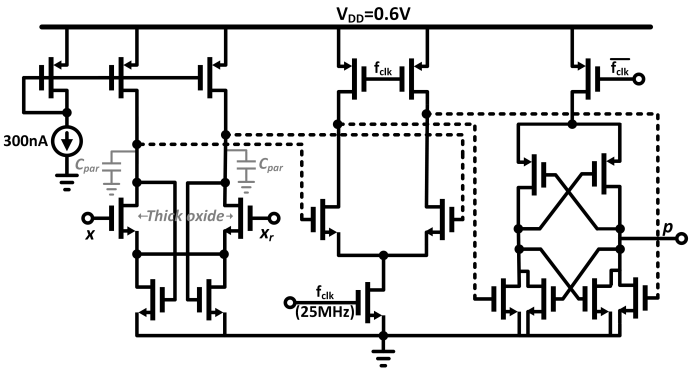


Figure 28.5.4: Schematic of the comparator.

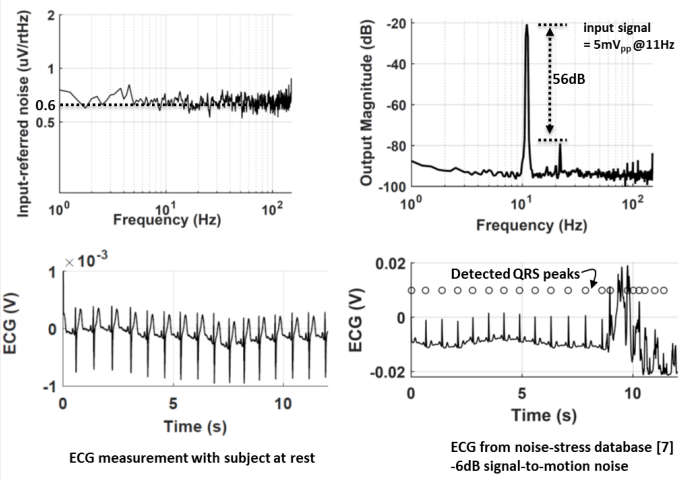


Figure 28.5.5: Measured results of the time-based AFE.

	[2]	[1]	[3]	This Work
Technology (nm)	65	180	65	40
Voltage Supply (V)	0.5	1.2	1	0.6
Offset (mV)	±50	±400	50	±150
AC Input signal	<1.7 mV_{pp} *	30 mV_{pp}	10 mV_{pp}	40 mV_{pp}
Area (mm^2)	0.013	>1.48 + 1μF off-chip	0.2	0.015
Power (μW)	5	~50	2.1	3.3
Input Impedance	(Pseudo-resistor)	> 500 MΩ	30 MΩ	~50 MΩ
Integrated Noise ($μV_{rms}$)	7.4 * @ (1Hz-150Hz)	0.612 @ (0.5Hz-150Hz)	10 * @ (1Hz-150Hz)	7.8 (offset < ±50mV) 20 (offset < ±150mV) @ (1Hz-150Hz)
Bandwidth (Hz)	300	150	500	150
THD	2% @ 0.6mV_{pp} input	0.6% @ 35mV_{pp} input	-	1 %@ 40mV_{pp} input
Application	Neural (LFP)	ECG	Mainly WSN	ECG
Remarks	AFE	AFE	Only IA	AFE

*extrapolated

Figure 28.5.6: Performance summary and comparison to state-of-the-art designs.

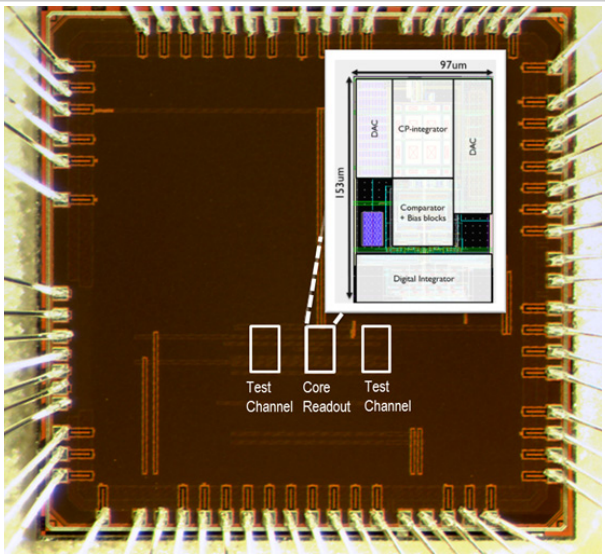


Figure 28.5.7: Chip photograph with inset showing the core layout.

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