

OUTPUT

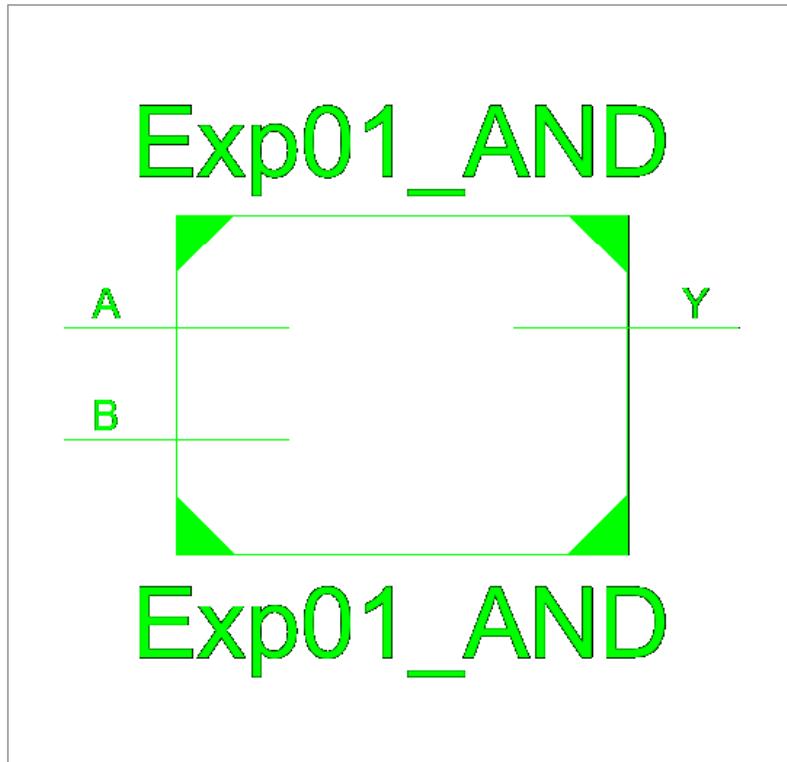


Figure 1: AND Gate RTL Schematic Block

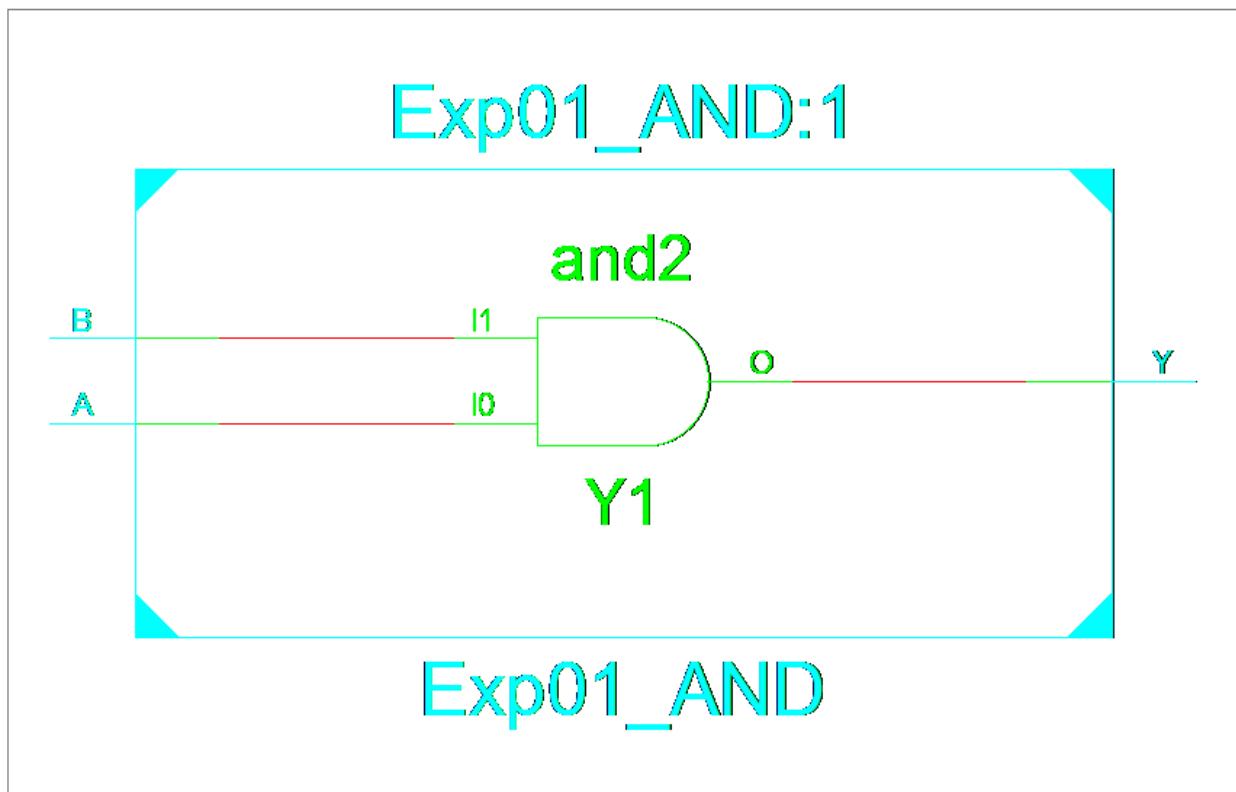


Figure 2: AND Gate RTL Schematic Diagram

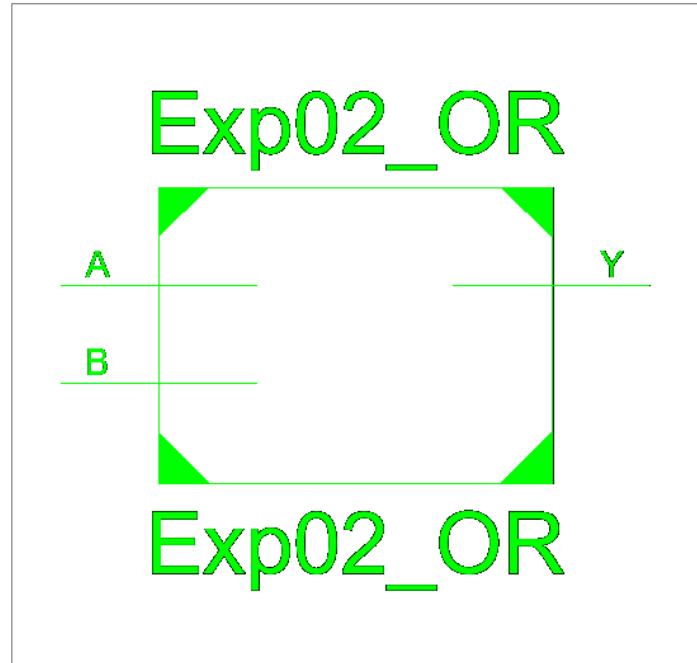


Figure 3: OR Gate RTL Schematic Block

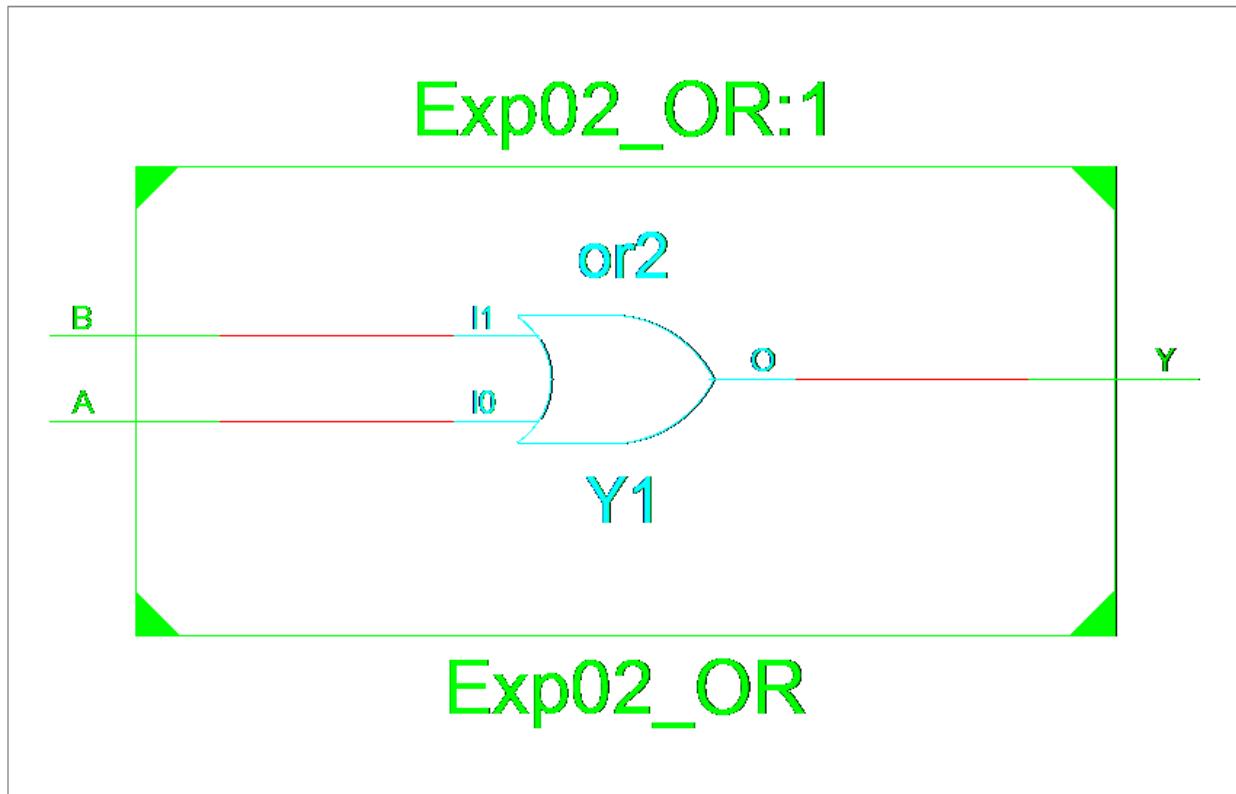
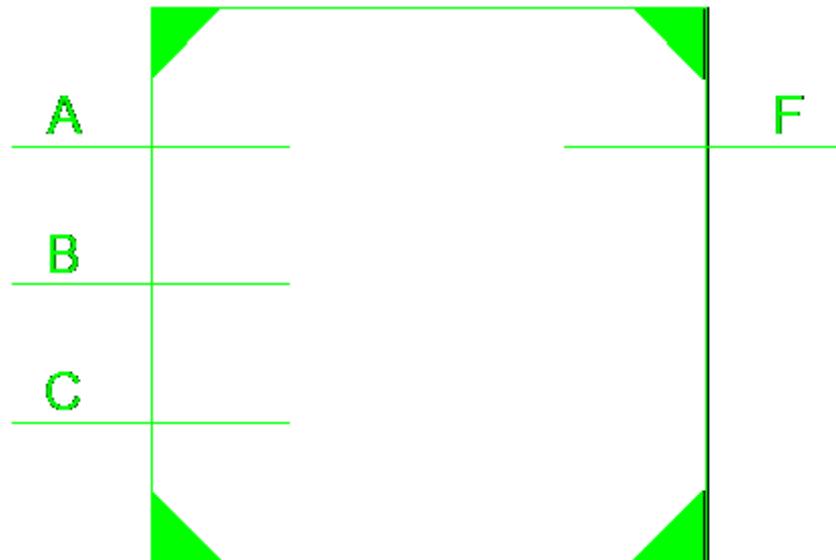


Figure 4: OR Gate RTL Schematic Diagram

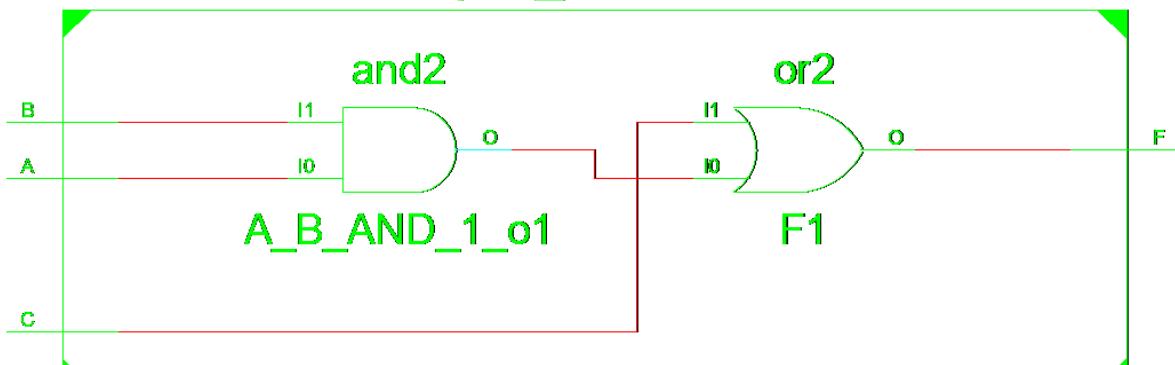
Exp03_Function



Exp03_Function

Figure 5: AB + C RTL Schematic Block

Exp03_Function:1



Exp03_Function

Figure 6: $F = AB + C$ RTL Schematic Diagram

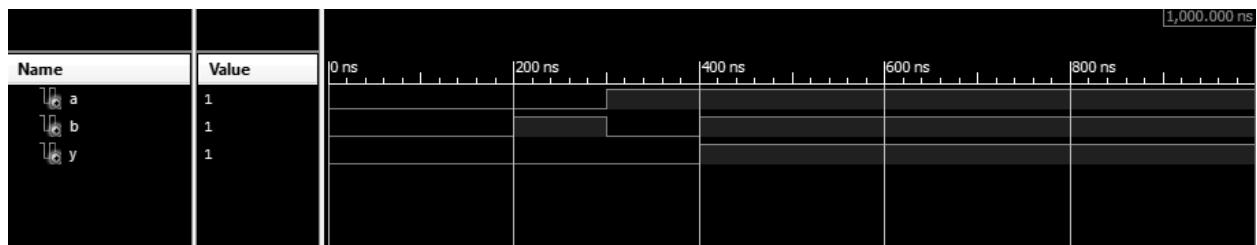


Figure 7: Test Bench of AND Gate

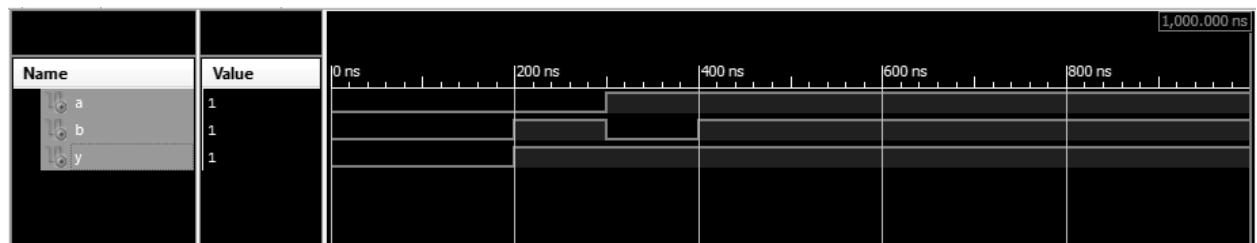


Figure 8: Test Bench of OR Gate



Figure 9: Test Bench of $F = AB + C$