ASSIGNMENT SET – IV

Submission before 30/11/2020 at 00:00:00 hrs

Assignment Set IV has to done after completing the Assignment Set I II & III successfully. If you haven't done the Assignment Set I II & III, please do this after completing Assignment Set I II & III.

With universal logic gates, any Boolean function can implement without the need of any other logic gates. The NAND's and NOR 's are said to be universal logic gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate, and are universal logic gates used in all integrated circuits (IC) digital logic families.

The objective of the assignment- IV is to club ALU and the memory to implement complex mathematical functions given below for 16-bit integer numbers and fractions may be discarded. The sequential chips that are used to implement the RAM in the assignment set III from the memory unit used in an actual system. The only building blocks that you can use are NAND gates and primitive Data flip-flops (DFFs), chips that you need to build on top of them must be from ASSIGNMENT-I & ASSIGNMENT-II using NAND gates only. Your design should make use of 16-bit Program Counter (PC) as and when required.

The tool you need for this project is the ModelSim - Intel FPGA Starter Edition. All the chips should implement using HDL Verilog.

The mathematical expressions depicted below are said to be complex, the operands *X* and *Y* can store in *R0* & *R1 (i.e., the two top RAM locations) respectively. The inputs of your program are the current values stored in R0 and R1. Your program computes the respective operation (+, -, *, %, /) and stores the result in R2.*

1. X*Y
2. (X+Y)*(X-Y)
3. (X%Y)
4. (X/Y)
5. (X)%(X-Y)