

Active charge collection strategy for radiation environment at device level

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Abstract—This work proposes a new methodology to improve the charge collection of an impacting ion in a FinFET in order to avoid this charge to affect device sensitive nodes. An internal electric field drives the charge generated by the ion track out of the sensitive device terminals. The simulations performed with TCAD tools in 22nm FinFET devices show that the amount of charge collected by these terminals can be reduced up to 37% by adopting the introduced methodology.

Index Terms—Charge Collection, Soft Error, Single Event Effects, Single Bit Upset, Multiple Bit Upset, Single Event Upset.

I. INTRODUCTION

THE aggressive scaling of CMOS technology has greatly increased the susceptibility to radiation-induced soft error effects (SEE) due to the low level of charge stored in the devices and low signal-to-noise margins [1].

Single-event upset error rate (SER) is strongly influenced by the sensitive area, so as technologies advance to deeper nodes, the SER is reduced. However, the reduced distances between transistors make multiple transistors vulnerable to a single ion strike resulting in multiple upsets [2].

The dynamics of the charge generated in a device by a radiation particle is well known [3]. The ion track leaves a dense plasma of electron-hole pairs along its path. If the electron-hole plasma is generated in a region with an electric field, electrons and holes are separated and a current spike is observed at the circuit node as free carriers are collected. This current spike has two components: a prompt component due to charge collection in the original depletion region and the funnel region [3], and a delayed component due to carrier diffusion up to the depletion region where it is quickly collected by the junction electric field.

It has been very well documented that the well configuration has a great impact on the collected charge by the active devices [4]–[10]. An example can be found in [2], where different well configurations are analyzed in three technology nodes, having

an apparently inconsistent behavior due to different charge collection mechanisms. In this context, the present work introduces an efficient mechanism to reduce the charge collected by active devices.

Thus, the structure of the paper is as follows: Section II introduces the device models and the simulation environment used to simulate the charge collection process. Section III presents the proposed technique oriented to the reduction of the charge collected by the active devices. Section IV analyzes the improvement in the case of multiple upsets, and finally, Section V presents the general conclusions.

II. SIMULATION FRAMEWORK

Three-dimensional (3D) Technology Computer Aided Design (TCAD) simulations of devices are useful and adequate in providing insight into physical mechanisms and failure modes due to single-event effects. In this work, 3D TCAD simulations [11] were used to investigate charge collection mechanisms and single-event transient (SET) pulse widths at the nanoscale node analyzed (22 nm).

The devices evaluated here are components of a high-performance 22 nm bulk-FinFET process. The structure of PFin and NFin devices is shown in Fig. 1. Both devices have been calibrated to fulfill the ITRS high performance requirements for the technology node evaluated in this work [12]. Electrical characteristics such as drain current vs. gate voltage (I_D-V_G), drain current vs. drain-source voltage (I_D-V_{DS}), and threshold voltage (V_T) were also calibrated to achieve the performance published in [13].

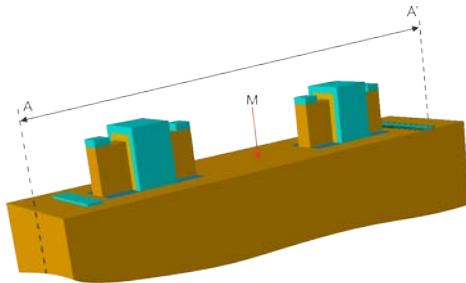


Fig. 1. Structure of the devices PFet an NFet in 22nm technology. Left device is the PFet

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The substrate contact used in the structure is the widest possible to increase charge collection from substrate contact [14], [15].

In all the simulations, the following physical models are used: Fermi-Dirac statistics, band-gap narrowing effect, doping dependent SRH recombination and Auger recombination, the impact of doping, electric field, carrier-carrier scattering and interface scattering on mobility, and Hydrodynamic model for carrier transport.

The electron-hole pair column created in the device by the ion strike is modeled using a carrier-generation function which has an exponential radial distribution with a characteristic radius of 10 nm. The time distribution of the ion track has a Gaussian shape, centered on 6 ps and with a characteristic width of 2 ps. The linear energy transfer (LET) value is kept constant along the track, and in all cases has been chosen of 5 MeV-cm²/mg.

The drain terminal of the N-type devices is constantly biased at the power supply voltage of 1 V, and the source and gate of the P-type devices, also, biased at this power supply voltage. The deposited charge is calculated considering the Gaussian distribution of the ion track and the 3-D geometry of the silicon body. The collected charge is given by the current integration over the time.

III. IMPROVED CHARGE COLLECTION

In this section, our study concentrates on the NFet device. The goal of the proposal is to collect the generated charge by the ion track out of the sensitive terminals. Sensitive terminals are only those that process information, i.e., the drain node of the device.

For this purpose, an electric field is created inside the well structure to redirect the charge generated outside the sensitive terminals, and finally collected it by an additional terminal. Two approaches have been considered: in the first one, a horizontal electric field crosses in the longitudinal direction from drain to source under the device; in the second, a vertical electric field from the channel of device to the substrate.

A. Longitudinal Electric Field

To create a longitudinal electric field, two well ties are added at each side of the device, one with N⁺ doping and the other with P⁺, as shown in Fig. 2.

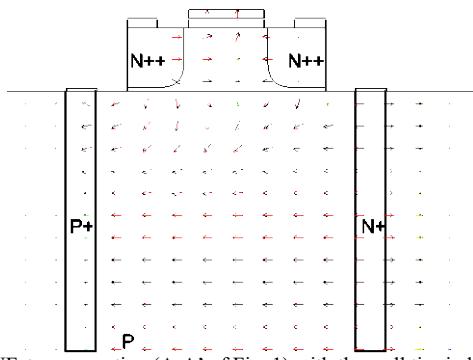


Fig. 2. NFet cross section (A-A' of Fig. 1) with the well ties in both sides of the device. Arrows point out direction and intensity of the electric field.

The generated longitudinal electric field is shown in the same

figure. The direction and intensity of the electric field are given by the arrows. In this approach, both positive and negative charges are respectively collected by the added N⁺ and P⁺ ties pushed by the created electric field.

Related to traditional design, this approach only requires the fabrication of an additional terminal for the N⁺ tie, because the P⁺ tie match up the substrate bias. The electric field without these ties, that is, the conventional solution, is only driven by the device, which in both cases is biased off.

To compare this proposal charge collection with the one in the conventional device, the ion track has been applied over the drain, in three situations: i) the first one, with a single tie to bias the substrate (conventional solution), ii) the second one with the well ties as drawn in Fig. 2, and iii) the third one biasing the N⁺ tie to V_{dd} in order to increase the internal electric field. The drain current collected in the three situations is shown in Fig. 3.

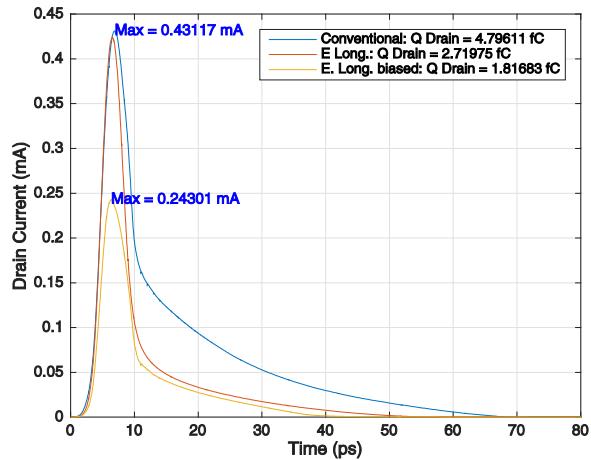


Fig. 3. Comparison of the collected drain current in the N device after a strike in the drain terminal, with longitudinal electric field, biased longitudinal electric field, and without any technique to reduce charge collection (conventional).

The total charge collected in the drain with the longitudinal solution, is reduced to a 57% compared to the traditional approach, and with the tie biased, the reduction is of 37% compared to the traditional approach. The effect of the electric field can be observed after 10 ps, when the carrier diffusion is the main current source in the traditional design. Until 10 ps (the prompt component), the collected charge originates from the original depletion and the funnel region. This current spike is reduced only with the ties biased, due to the higher electric field generated.

Also, it has been analyzed the current in the source terminal in the three cases, and is reduced in the same proportion as the drain, but in the case of the biased tie where an abnormal high leakage current was observed (0.16 μ A). This is due to the proximity of the N⁺ tie to the source, as the depletion area grows and merges with the source area. The distance of the tie was increased and the leakage current was set to a normal value.

To check the effect of different ions, simulations have also been performed with LET of 20 MeV-cm²/mg, obtaining reductions of charge collection in the same proportion.

B. Vertical Electric Field

In the second approach, a vertical electric field is created by an N+ layer in the back side of the N device. In this case, the electric field is from the added N+ region to the NFin. For the P device, the added region is P+, and the electric field PFet to the P+ region PFet. In Fig. 4 the new P device configuration is shown.

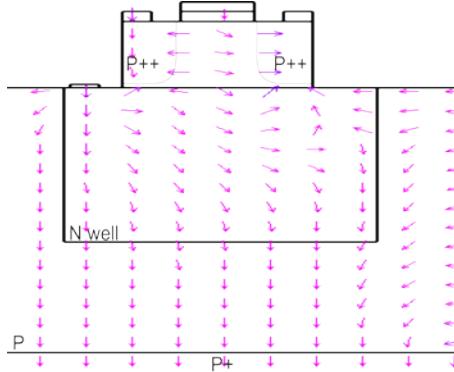


Fig. 4. Internal electric field with an added P+ layer under the P device.

Experiments equivalent to the ones in the previous study have been performed with the N device. The three drain currents shown in Fig. 5 correspond to the N traditional device, the same device with the additional layer, and the third one, with the same region biased.

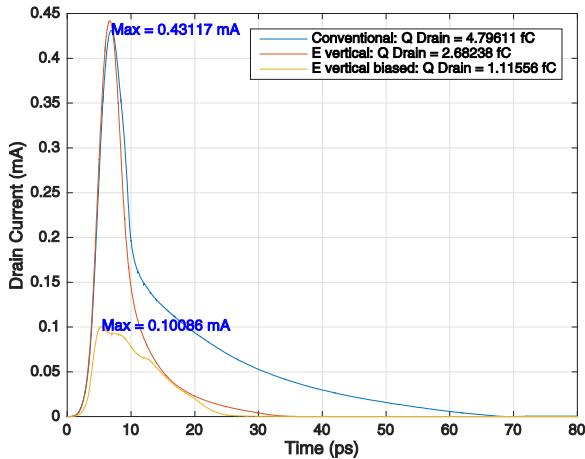


Fig. 5. Comparison of the collected drain current in the N device after a strike in the drain terminal, with a N+ layer under the device, the N+ layer biased to V_{dd} , and without any technique to reduce charge collection..

For these configurations, the improvement is quite similar to previous with tie, slightly decreasing the charge collected with a region added. For this configuration, it has not observed a considerable increase in the leakage current between the new region and the source, as happened in the longitudinal electric field.

A drawback in both configurations (transversal and longitudinal electric field) is the additional leakage current created by the insertion of a new PN junction (around 40 nA). This leakage current is highly dependent of the doping level in the added regions. For the transverse field, the impact on the overhead area is lower because no additional elements are needed between devices.

IV. MULTIPLE UPSETS SIMULATIONS RESULTS

The continuous shrinkage of technological nodes involves an increase in multiple upsets, taking a relevant importance at the nanoscale[2]. To test the effect of the approaches presented so far on multiple upset events, two devices were simulated, one PFN and the other one NFIN, as close as possible (Fig. 1), and both in OFF state. Strikes in each device are generated, and the drain current is obtained in the other device (Fig. 6 and 7). Drain current collected in the impacted device are exactly equal to those obtained in Fig. 3 and 5. The vertical electric field approach was considered for this study since it has less area consumption penalty, and a better radiation robustness.

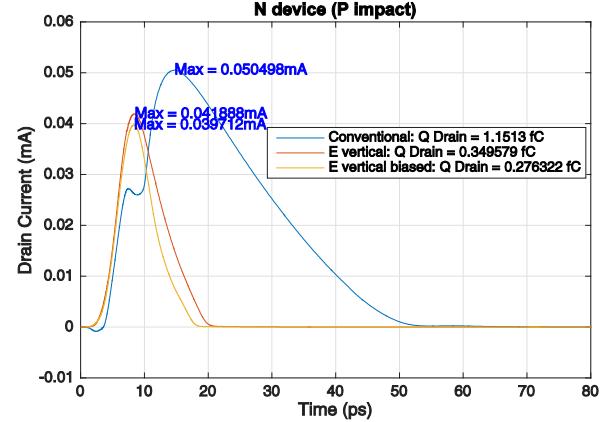


Fig. 6. Drain current in the N device with a strike in the drain of the P device. Both devices in OFF state.

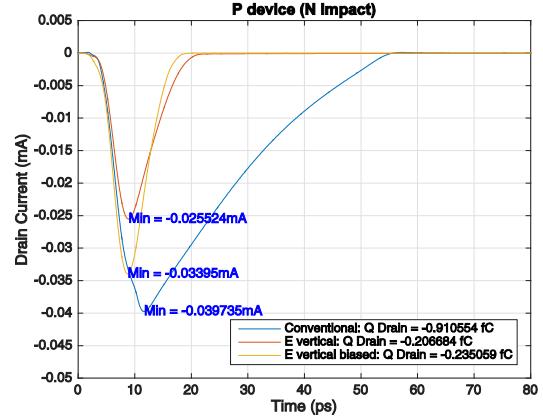


Fig. 7. Drain current in the P device after a strike in the drain of the N device. Both devices in OFF state.

For both devices the peak current is reduced around a 20%, and the total charge collected by the N device is practically reduced about 75%. Furthermore, a great charge reduction is observed in the P device, when the N device is impacted. In this case the recollected charge is 80% lower than in the traditional case.

To show the efficiency of the proposed charge collection method, impacts at different points outside any device have been considered. The results shown in Fig. 8 and 9 are the drain current when the track input point is the arrow M in Fig. 1. This

point is equidistant from the two devices.

The additional layer presents a reduction of the drain peak current, greater with this layer biased, but, again there is a considerable reduction of charge collection with values of a 37% lower than without any technique to reduce the charge generated.

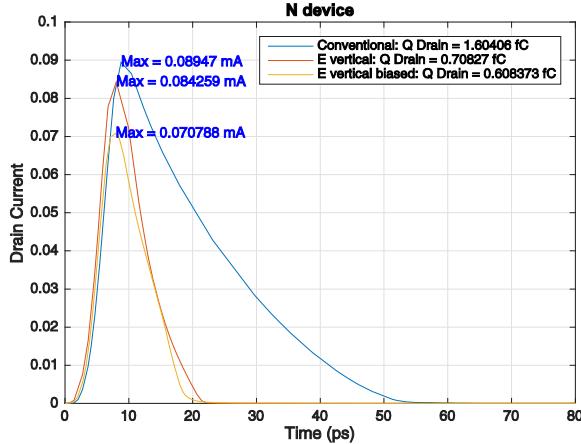


Fig. 8. Drain current in the N device with a strike in a equidistant point from the two devices.

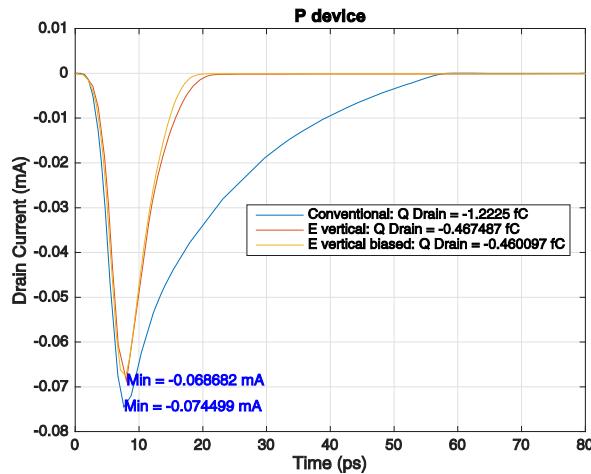


Fig. 9. Drain current in the P device after a strike in a equidistant point from the two devices.

V. CONCLUSIONS

Two approaches have been presented to reduce the charge collected on the sensitive terminals of a FinFET device and which has been produced by an ion track. Both proposals are based on the creation of an electric field that allows excess carriers to be redirected upon impact to terminals that do not affect the information processed by the devices. The first one generates a longitudinal electric field via two tie with a P+ and N+ doping profile at both sides of the device. This solution requires a higher area overhead than the second solution, which generates a vertical electric field in the device, with the inclusion of a layer in the back side of the bulk, with a P+

doping profile under the PFin, and N+ under the N device.

A disadvantage of both solutions is the introduction of an PN junction, with the consequent increasing of the leakage current (around 40 nA). In both cases, the collected charge collected by the sensitive terminals has been reduced up to a 75% in P device, and in any of the situations observed is not less than 37%.

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