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K.V.G COLLEGE OF ENGINEERING, SULLIA, D.K. – 574 327  
(AFFILIATED TO VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI)



# DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING



## SCHEME, SYLLABUS & QUESTION PAPERS

SEMESTER: III

ACADEMIC YEAR: 2024-25

STUDENT NAME: \_\_\_\_\_

University Seat No.: \_\_\_\_\_



**VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI**  
**B.E. in Electronics and Communication Engineering**  
**Scheme of Teaching and Examinations 2022**

III SEMESTER																	
Sl. No	Course	Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Total Marks	Credits			
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks						
L	T	P	SDA														
1	PCC	BMATEC301	AV Mathematics-III for EC Engineering	TD-Maths PSB - Maths	3	0	0		03	50	50	100	3				
2	IPCC	BEC302	Digital System Design using Verilog	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4				
3	IPCC	BEC303	Electronic Principles and Circuits	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4				
4	PCC	BEC304	Network Analysis	TD: ECE PSB: ECE	3	0	0		03	50	50	100	3				
5	PCCL	BECL305	Analog and Digital Systems Design Lab	TD: ECE PSB: ECE	0	0	2		03	50	50	100	1				
6	ESC	BXX306x	ESC/ETC/PLC	TD: PSB:	3	0	0		03	50	50	100	3				
7	UHV	BSCK307	Social Connect and Responsibility	Any Department	0	0	2		01	100	---	100	1				
8	AEC/ SEC	BXX358x	Ability Enhancement Course/Skill Enhancement Course- III	If the course is a Theory				01		50	50	100	1				
				1	0	0		02									
				If a course is a laboratory													
9	MC	BNSK359	National Service Scheme (NSS)	NSS coordinator	0	0	2			100	---	100	0				
		BPEK359	Physical Education (PE) (Sports and Athletics)	Physical Education Director													
		BYOK359	Yoga	Yoga Teacher													
										<b>Total</b>	<b>550</b>	<b>350</b>	<b>900</b>	<b>20</b>			

**PCC:** Professional Core Course, **PCCL:** Professional Core Course laboratory, **UHV:** Universal Human Value Course, **MC:** Mandatory Course (Non-credit), **AEC:** Ability Enhancement Course, **SEC:** Skill Enhancement Course, **L:** Lecture, **T:** Tutorial, **P:** Practical **S=SDA:** Skill Development Activity, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Evaluation.K :This letter in the course code indicates common to all the stream of engineering. **ESC:** Engineering Science Course, **ETC:** Emerging

**Professional Core Course (IPCC):** Refers to Professional Core Course Theory Integrated with practical's of the same course. Credit for IPCC can be 04 and its Teaching– Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-23 may please be referred.

**National Service Scheme /Physical Education/Yoga:** All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course is mandatory for the award of degree.

<b>AV MATHEMATICS-III FOR EC ENGINEERING</b>		Semester	3
Course Code	<b>BMATEC301</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		
<b>Module-1: Fourier series and practical harmonic analysis</b>			
Periodic functions, Dirichlet's condition. Fourier series expansion of functions with period $2\pi$ and with arbitrary period: periodic rectangular wave, Half-wave rectifier, rectangular pulse, Saw tooth wave. Half-range Fourier series. Triangle and half range expansions, Practical harmonic analysis, variation of periodic current. <b>(8 hours)</b>			
<b>Module-2: Infinite Fourier Transforms</b>			
Infinite Fourier transforms, Fourier cosine and sine transforms, Inverse Fourier transforms, Inverse Fourier cosine and sine transforms, discrete Fourier transform (DFT), Fast Fourier transform (FFT). <b>(8 hours)</b>			
<b>Module-3: Z Transforms</b>			
Definition, Z-transforms of basic sequences and standard functions. Properties: Linearity, scaling, first and second shifting, multiplication by n. Initial and final value theorem. Inverse Z-transforms. Application to difference equations. <b>(8 hours)</b>			
<b>Module-4: Ordinary Differential Equations of Higher Order</b>			
Higher-order linear ODEs with constant coefficients - Inverse differential operator, problems. Linear differential equations with variable Coefficients-Cauchy's and Legendre's differential equations-Problems. Application of linear differential equations to L-C circuit and L-C-R circuit. <b>(8 hours)</b>			
<b>Module-5: Curve fitting, Correlation, and Regressions</b>			
Principles of least squares, Curve fitting by the method of least squares in the form $y = a + bx$ , $y = a + bx + cx^2$ , and $y = ax^b$ . Correlation, Coefficient of correlation, Lines of regression, Angle between regression lines, standard error of estimate, rank correlation. <b>(8 hours)</b>			
<b>Text Books:</b>			
1. <b>B. S. Grewal:</b> "Higher Engineering Mathematics", Khanna Publishers, 44 <sup>th</sup> Ed., 2021. 2. <b>E. Kreyszig:</b> "Advanced Engineering Mathematics", John Wiley & Sons, 10 <sup>th</sup> Ed., 2018.			
<b>Reference Books:</b>			
1. <b>V. Ramana:</b> "Higher Engineering Mathematics" McGraw-Hill Education, 11 <sup>th</sup> Ed., 2017 2. <b>Srimanta Pal &amp; Subodh C.Bhunia:</b> "Engineering Mathematics" Oxford University Press, 3 <sup>rd</sup> Ed., 2016. 3. <b>N.P Bali and Manish Goyal:</b> "A Textbook of Engineering Mathematics" Laxmi Publications, 10 <sup>th</sup> Ed., 2022. 4. <b>C. Ray Wylie, Louis C. Barrett:</b> "Advanced Engineering Mathematics" McGraw-Hill Book Co., New York, 6 <sup>th</sup> Ed., 2017. 5. <b>Gupta C.B, Sing S.R and Mukesh Kumar:</b> "Engineering Mathematic for Semester I and II", McGraw Hill Education(India) Pvt. Ltd 2015. 6. <b>H.K. Dass and Er. Rajnish Verma:</b> "Higher Engineering Mathematics" S.Chand Publication, 3 <sup>rd</sup> Ed., 2014. 7. <b>James Stewart:</b> "Calculus" Cengage Publications, 7 <sup>th</sup> Ed., 2019.			

## Model Question Paper-II (CBCS Scheme)

**USN**

### Third Semester B.E Degree Examination

#### **AV-MATHEMATICS FOR EC ENGINEERING STREAM (BMATEC301)**

**TIME: 03 Hours**

**Max.Marks:100**

Note: (i) Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

(ii) Statistical tables and Mathematics Formula handbooks are allowed.

<b>Module -1</b>			M	L	C
Q.01	a	Find the Fourier series expansion of $f(x) = \begin{cases} x & : 0 \leq x \leq \pi \\ 2\pi - x & : \pi \leq x \leq 2\pi \end{cases}$ .	6	L2	CO1
	b	Expand $f(x) = 2x - 1$ as a Cosine half range Fourier series in $0 < x < 1$ .	7	L2	CO1
	c	Obtain the constant term and the first coefficients of cosine and sine terms in the Fourier series expansion for the following data:	7	L3	CO1
<b>OR</b>					
Q.02	a	Obtain the Fourier series for the triangular wave function $f(x) = \begin{cases} \pi + x, & \text{for } -\pi \leq x \leq 0 \\ \pi - x, & \text{for } 0 \leq x \leq \pi \end{cases}$	6	L2	CO1
	b	Obtain a half range sine series for $f(x) = (x-1)^2$ in $(0, 1)$	7	L2	CO1
	c	Obtain the constant term and coefficients of first cosine and sine terms in the expansion of y from the following table	7	L3	CO1
<b>Module-2</b>					
Q. 03	a	Find the Fourier Transform of the function $f(x) = \begin{cases} 1, & \text{for }  x  \leq a \\ 0, & \text{for }  x  > a \end{cases}$ Hence evaluate (i) $\int_0^\infty \frac{\sin ax \cos sx}{x} dx$ , (ii) $\int_0^\infty \frac{\sin ax}{x} dx$ .	6	L2	CO2

	b	<p>Find the Fourier cosine Transform of the function <math>f(x) = e^{-a x }</math>.  Hence evaluate <math>\int_0^\infty \frac{\cos mx}{a^2 + x^2} dx</math>.</p>	7	L2	CO2
	c	Find the Transform of the sequence $f = [0, 1, 4, 9]^T$ of four values using Fast Fourier Transform.	7	L3	CO2
<b>OR</b>					
Q.04	a	Find the complex Fourier Transform of the function $f(x) = e^{-a^2x^2}$ , $a > 0$	6	L2	CO2
	b	Find the Fourier sine Transform of the function $f(x) = \begin{cases} 4x, & \text{for } 0 < x < 1 \\ 4-x, & \text{for } 1 < x < 4 \\ 0, & \text{for } x > 4 \end{cases}$	7	L1	CO2
	c	Obtain the inverse Fourier cosine Transform of the function $F_c(s) = \frac{\sin as}{s}$ , $a > 0$	7	L3	CO2
<b>Module-3</b>					
Q. 05	a	Find the Z-transform of: i) $\sin hn\theta$ ; ii) $\cos n\theta$	6	L2	CO3
	b	Find the inverse Z-transform of $\frac{z^2 + z}{z^3 + 6z^2 + 11z + 6}$	7	L3	CO3
	c	Solve the difference equation using Z-transform $u_{n+2} + 4u_{n+1} + 3u_n = 3^n$ , with $u_0 = 0$ & $u_1 = 1$	7	L3	CO3
<b>OR</b>					
Q. 06	a	Find the Z-transform of $a^n n^2 + 4 \sin\left(\frac{n\pi}{4}\right) + 5$	6	L2	CO3
	b	Find the Inverse Z-transform of $\frac{z^3 - 20z}{(z-2)^3(z-4)}$	7	L3	CO3
	c	If $Z(u_n) = \frac{2z^2 + 3z + 4}{(z-3)^3}$ , $ z  > 3$ . Find $u_1, u_2$ & $u_3$	7	L3	CO3
<b>Module-4</b>					
Q. 07	a	Solve $4D^4 - 4D^3 - 23D^2 + 12D + 36 = 0$ .	6	L2	CO4
	b	Solve $\frac{d^2y}{dx^2} - 4y = \cosh(2x-1) + 3^x$ .	7	L2	CO4
	c	Solve $x^3 \frac{d^3y}{dx^3} + 2x^2 \frac{d^2y}{dx^2} + 2y = 10\left(x + \frac{1}{x}\right)$	7	L3	CO4
<b>OR</b>					
Q. 08	a	Solve $\frac{d^2y}{dx^2} + 4 \frac{dy}{dx} + 4y = 3 \sin x + 4 \cos x$	6	L2	CO4

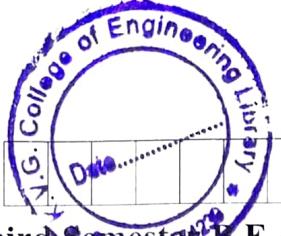
	b	Solve $(2x+3)^2 \frac{d^2y}{dx^2} - (2x+3) \frac{dy}{dx} - 12y = 6x$ .	7	L2	CO4
	c	An alternating E.M.F. $E \sin pt$ is applied to a circuit at $t = 0$ . Given the equation for the current $i$ as $L \frac{d^2i}{dt^2} + R \frac{di}{dt} + \frac{i}{c} = pE \sin pt$ , find $i$ when (i) $CR^2 > 4L$ (ii) $CR^2 < 4L$	7	L3	CO4

### Module-5

Q. 09	a	Find a least square straight line for the following data <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>x</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td></tr> <tr> <td>y</td><td>6</td><td>4</td><td>3</td><td>5</td><td>4</td><td>2</td></tr> </table>	x	1	2	3	4	5	6	y	6	4	3	5	4	2	6	L2	CO5								
x	1	2	3	4	5	6																					
y	6	4	3	5	4	2																					
	b	If the coefficient of correlation between the variables $x$ and $y$ is 0.5 and the acute angle between their lines of regression is $\tan^{-1}\left(\frac{3}{8}\right)$ , show that $\sigma_x = \frac{1}{2}\sigma_y$	7	L2	CO5																						
	c	Determine rank correlation for the following data which shows the marks obtained in two quizzes in mathematics <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>Marks in first quiz X</td> <td>6</td> <td>5</td> <td>8</td> <td>8</td> <td>7</td> <td>6</td> <td>10</td> <td>4</td> <td>9</td> <td>7</td> </tr> <tr> <td>Marks in second quiz Y</td> <td>8</td> <td>7</td> <td>7</td> <td>10</td> <td>5</td> <td>8</td> <td>10</td> <td>6</td> <td>8</td> <td>6</td> </tr> </table>	Marks in first quiz X	6	5	8	8	7	6	10	4	9	7	Marks in second quiz Y	8	7	7	10	5	8	10	6	8	6	7	L3	CO5
Marks in first quiz X	6	5	8	8	7	6	10	4	9	7																	
Marks in second quiz Y	8	7	7	10	5	8	10	6	8	6																	

**OR**

Q. 10	a	Find a least square quadratic curve for the following data <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>x</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>6</td><td>7</td><td>8</td></tr> <tr> <td>y</td><td>12</td><td>10.5</td><td>10</td><td>8</td><td>7</td><td>2</td><td>8.5</td><td>9</td></tr> </table> Estimate $y$ at $x = 6.5$	x	0	1	2	3	4	6	7	8	y	12	10.5	10	8	7	2	8.5	9	6	L2	CO5
x	0	1	2	3	4	6	7	8															
y	12	10.5	10	8	7	2	8.5	9															
	b	For the following data find the correlation coefficient between $x$ and $y$ . <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>x</td> <td>6</td> <td>5</td> <td>8</td> <td>8</td> <td>7</td> <td>6</td> </tr> <tr> <td>y</td> <td>8</td> <td>7</td> <td>7</td> <td>10</td> <td>5</td> <td>8</td> </tr> </table> Also find the standard error estimates.	x	6	5	8	8	7	6	y	8	7	7	10	5	8	7	L3	CO5				
x	6	5	8	8	7	6																	
y	8	7	7	10	5	8																	
	c	Find the two regression lines from the following data <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>x</td> <td>1</td> <td>2</td> <td>3</td> <td>4</td> <td>5</td> <td>6</td> </tr> <tr> <td>y</td> <td>14</td> <td>12</td> <td>16</td> <td>11</td> <td>14</td> <td>12</td> </tr> </table>	x	1	2	3	4	5	6	y	14	12	16	11	14	12	7	L3	CO5				
x	1	2	3	4	5	6																	
y	14	12	16	11	14	12																	



# **CBCS SCHEME**

BMA TEC301/BEC/BBM301

USN

**AV Mathematics – III for EC/BM Engineering**

Time: 3 hrs.

Max. Marks: 100

- Note:** 1. Answer any FIVE full questions, choosing ONE full question from each module.  
2. M : Marks , L: Bloom's level , C: Course outcomes.  
3. Statistical table and handbook permitted.  
4. Use of VTU Mathematics handbook is permitted.

Module – 1			M	L	C																
Q.1	a.	Obtain the Fourier series of $f(x) = \frac{\pi - x}{2}$ in $0 < x < 2\pi$ . Hence deduce that $1 - \frac{1}{3} + \frac{1}{5} - \frac{1}{7} + \dots = \frac{\pi}{4}$ .	6	L2	CO1																
	b.	Expand $f(x) = 2x-1$ as a Cosine half range Fourier series in $0 < x < 1$ .	7	L2	CO1																
	c.	Compute the First harmonics of the Fourier series of $f(x)$ . Given the table	7	L3	CO1																
		<table border="1"> <tr> <td>x</td><td>0</td><td><math>\frac{\pi}{3}</math></td><td><math>\frac{2\pi}{3}</math></td><td><math>\pi</math></td><td><math>\frac{4\pi}{3}</math></td><td><math>\frac{5\pi}{3}</math></td><td><math>2\pi</math></td></tr> <tr> <td><math>f(x)</math></td><td>1.0</td><td>1.4</td><td>1.9</td><td>1.7</td><td>1.5</td><td>1.2</td><td>1.0</td></tr> </table>	x	0	$\frac{\pi}{3}$	$\frac{2\pi}{3}$	$\pi$	$\frac{4\pi}{3}$	$\frac{5\pi}{3}$	$2\pi$	$f(x)$	1.0	1.4	1.9	1.7	1.5	1.2	1.0			
x	0	$\frac{\pi}{3}$	$\frac{2\pi}{3}$	$\pi$	$\frac{4\pi}{3}$	$\frac{5\pi}{3}$	$2\pi$														
$f(x)$	1.0	1.4	1.9	1.7	1.5	1.2	1.0														

OR

<b>Q.2</b>	a.	Obtain the Fourier series of $f(x) =  x $ in $(-\ell, \ell)$ .	6	L2	CO1																
	b.	Obtain the Cosine half range Fourier series of $f(x) = x^2$ in $0 < x < \pi$ .	7	L3	CO1																
	c.	Express Y as a Fourier Cosine series upto second harmonics. Given the table : <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>x</td><td>0</td><td>2</td><td>4</td><td>6</td><td>8</td><td>10</td><td>12</td></tr> <tr> <td>y</td><td>9.0</td><td>18.2</td><td>24.4</td><td>27.8</td><td>27.5</td><td>22.0</td><td>9.0</td></tr> </table>	x	0	2	4	6	8	10	12	y	9.0	18.2	24.4	27.8	27.5	22.0	9.0	7	L3	CO1
x	0	2	4	6	8	10	12														
y	9.0	18.2	24.4	27.8	27.5	22.0	9.0														

Module - 2

<b>Q.3</b>	a. Find the Fourier transform of $f(x) = e^{- x }$ .	<b>6</b>	<b>L2</b>	<b>CO2</b>
	b. Find the Fourier Cosine and Sine transform of $f(x) = e^{-\alpha x}$ , $\alpha > 0$ .	<b>7</b>	<b>L3</b>	<b>CO2</b>
c.	i) Find a Discrete Fourier transform of the single $f = [3, 4, 5, 5]^T$ . ii) Find the Inverse Discrete Fourier transform of the single obtained in part (i).	<b>7</b>	<b>L3</b>	<b>CO2</b>

OR

Q.4	<p>a. Find the Fourier transform of <math>f(x) = \begin{cases} 1- x  &amp; \text{for }  x  \leq 1 \\ 0 &amp; \text{for }  x  &gt; 1 \end{cases}</math> and hence deduce that <math>\int_0^\pi \frac{\sin^2 t}{t^2} dt = \frac{\pi}{2}</math>.</p>	6	L2	CO2
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b.	Obtain the Fourier Cosine transform of $f(x) = \begin{cases} 4x & , 0 < x < 1 \\ 4-x & , 1 < x < 4 \\ 0 & , x > 4 \end{cases}$	7	L3	CO2
c.	Solve the Integral equation $\int_0^{\infty} f(\theta) \cos \alpha \theta d\theta = \begin{cases} 1-\alpha & , 0 \leq \alpha \leq 1 \\ 0 & , \alpha > 1 \end{cases}$ and hence evaluate $\int_0^{\pi} \frac{\sin^2 t}{t^2} dt$ .	7	L3	CO2

**Module - 3**

Q.5	a. Find the Z - transform of i) $\cos n\theta$ ii) $\sin n\theta$ .	6	L2	CO3
	b. Find the Inverse Z - transform of $\frac{z^2 - 8z}{(z-4)^2}$ .	7	L3	CO3
	c. Solve the difference equation $y_{n+2} - 4y_n = 0$ . Given that $y_0 = 0$ and $y_1 = 2$ .	7	L3	CO3

**OR**

Q.6	a. Find the Z - transform of $2n + \sin\left(\frac{n\pi}{4}\right) + 1$ .	6	L2	CO3
	b. Compute the Inverse Z - transform of $\frac{3z^2 + 2z}{(5z-1)(5z+2)}$ .	7	L3	CO3
	c. Solve the difference equation $u_{n+2} + 6u_{n+1} + 9u_n = 2^n$ with $u_0 = u_1 = 0$ , using Z - transforms.	7	L3	CO3

**Module - 4**

Q.7	a. Solve $(D^4 - m^4)y = 0$ .	6	L2	CO4
	b. Solve $(D^2 - 2D + 1)y = \sin x + e^x$ .	7	L3	CO4
	c. Solve $x \frac{d^3y}{dx^3} + \frac{d^2y}{dx^2} = \frac{1}{x}$ .	7	L3	CO4

**OR**

Q.8	a. Solve $\frac{d^3y}{dx^3} + 8y = x^4 + 2x + 1$ .	6	L2	CO4
	b. Solve the Legendre's form of Linear equation. $(1+x)^2 \frac{d^2y}{dx^2} + (1+x) \frac{dy}{dx} + y = \sin 2 [\log(1+x)]$ .	7	L3	CO4
	c. In the LCR circuit the charge $q$ on a plate of condenser is given by $L \frac{d^2q}{dt^2} + R \frac{dq}{dt} + \frac{q}{C} = E \sin pt$ . Solve the above equation.	7	L3	CO4

**Module - 5**

Q.9	a.	Find a Least square straight line for the following data :	6	L2	CO5										
		<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>x</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td></tr> <tr><td>y</td><td>6</td><td>4</td><td>3</td><td>5</td><td>4</td><td>2</td></tr> </table>				x	1	2	3	4	5	6	y	6	4
x	1	2	3	4	5	6									
y	6	4	3	5	4	2									
b.	In a partially destroyed laboratory record, the lines of regression of y on x and x on y are available as $4x - 5y + 33 = 0$ and $20x - 9y = 107$ . Calculate $\bar{x}$ , $\bar{y}$ and coefficient of correlation between x and y.														

- c. Ten competition in a beauty contest are ranked by two judges A and B in the following order. Calculate the rank correlation coefficient.

ID No. of competition	1	2	3	4	5	6	7	8	9	10
Judge A	1	6	5	10	3	2	4	9	7	8
Judge B	6	4	9	8	1	2	3	10	5	7

**OR**

Q.10	a.	Fit a parabola for the data in the form $y = ax^2 + bx + c$ .	6	L2	CO5								
		<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>x</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td></tr> <tr><td>y</td><td>10</td><td>12</td><td>13</td><td>16</td><td>19</td></tr> </table>				x	1	2	3	4	5	y	10
x	1	2	3	4	5								
y	10	12	13	16	19								

b.	The following table gives the heights of Father (x) and Sons (y) :	7	L3	CO5														
	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>x</td><td>65</td><td>66</td><td>67</td><td>67</td><td>68</td><td>69</td><td>70</td><td>72</td></tr> <tr><td>y</td><td>67</td><td>68</td><td>65</td><td>68</td><td>72</td><td>72</td><td>69</td><td>71</td></tr> </table>				x	65	66	67	67	68	69	70	72	y	67	68	65	68
x	65	66	67	67	68	69	70	72										
y	67	68	65	68	72	72	69	71										

Find the lines of regression and hence calculate the co-efficient of correlation.

c.	Determine the rank correlation for the following data which shows the marks obtained in two quizzes in mathematics.	7	L3	CO5																		
	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>Marks in first quiz X</td><td>6</td><td>5</td><td>8</td><td>8</td><td>7</td><td>6</td><td>10</td><td>4</td><td>9</td><td>7</td></tr> <tr><td>Marks in first quiz Y</td><td>8</td><td>7</td><td>7</td><td>10</td><td>5</td><td>8</td><td>10</td><td>6</td><td>8</td><td>6</td></tr> </table>				Marks in first quiz X	6	5	8	8	7	6	10	4	9	7	Marks in first quiz Y	8	7	7	10	5	8
Marks in first quiz X	6	5	8	8	7	6	10	4	9	7												
Marks in first quiz Y	8	7	7	10	5	8	10	6	8	6												

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<b>DIGITAL SYSTEM DESIGN USING VERILOG</b>		Semester	3		
Course Code	<b>BEC302</b>	CIE Marks	50		
Teaching Hours/Week (L:T:P: S)	3:0:2	SEE Marks	50		
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100		
Credits	04	Exam Hours	03		
Examination nature (SEE)	Theory/Practical	<b>MODULE-1</b>			
<b>Principles of Combinational Logic:</b> Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-up to 4 variables, Quine-Mc-Cluskey Minimization Technique. Quine-Mc-Cluskey using Don't Care Terms. (Section3.1to3.5 of Text1).					
<b>MODULE-2</b>					
<b>Logic Design with MSI Components and Programmable Logic Devices:</b> Binary Adders and SubTRACTors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section5.1to5.7 of Text 2)					
<b>MODULE-3</b>					
<b>Flip-Flops and its Applications:</b> The Master-Slave Flip-flops (Pulse-Triggered flip-flops):SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, J K, D and SR flip-flops. (Section 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text2)					
<b>MODULE-4</b>					
<b>Introduction to Verilog:</b> Structure of Verilog module, Operators, Data Types, Styles of Description. (Section1.1to1.6.2, 1.6.4 (only Verilog),2 of Text 3)					
<b>Verilog Data flow description:</b> Highlights of Data flow description, Structure of Data flow description. (Section2.1to2.2(only Verilog) of Text3)					
<b>MODULE-5</b>					
<b>Verilog Behavioral description:</b> Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (only Verilog) of Text 3)					
<b>Verilog Structural description:</b> Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder. (Section4.1 to 4.2 of Text 3)					

## PRACTICAL COMPONENT OF IPCC

(Experiments can be conducted either using any circuit simulation software or discrete components)

S.N.	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program
2	To realize Adder/Subtractor (Full/half)circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a)Gray to binary and vice versa b)Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description:8:1mux, 8:3encoder, Priority encoder
6	To realize using Verilog Behavioral description:1:8Demux, 3:8 decoder,2 -bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a) JK type b) SR type c) T type and d) D type
8	To realize Counters-up/down (BCD and binary) using Verilog Behavioral description.

### Demonstration Experiments (For CIE only-not to be included for SEE)

Use FPGA/CPLD kits for down loading Verilog codes and check the output for interfacing experiments.

9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

### Text Books:

- 1.Digital Logic Applications and Design by John M Yarbrough, Thomson Learning,2001.
- 2.Digital Principles and Design by Donald DGivone, McGrawHill, 2002.
- 3.HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dream Tech Press.

### Reference Books:

- 1.Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
- 2.Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2007
- 3.Fundamentals of HDL by Cyril PR, Pearson/Sanguine2010

**Model Question Paper-I with effect from 2023-24 (CBCS Scheme)**

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**Third Semester B.E. Degree Examination**  
**Digital System Design using Verilog**

**TIME: 03 Hours****Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

<b>Module -1</b>			*Bloom's Taxonomy Level	Marks
Q.01	a	Design a logic circuit that has 4 inputs, the output will only be high, when the majority of the inputs are high. Use k-map to simplify		L3
	b	Simplify the given Boolean function using Quine MC Cluskey find the prime and essential prime implicants and also verify with K-map $f(A,B,C,D)=\sum m(0,1,4,5,7,8,13,15) + d(2)$	L3	10
<b>OR</b>				
Q.02	a	Simplify the following expression using K-map. Implement the simplified expression using basic gates only $f(a,b,c,d)=\prod M(0,2,3,4,5,12,13)+d(8,10)$	L3	10
	b	Define the following terms with example. Minterm, Maxterm	L1	04
	c	Place the following equation into proper canonical form $P = f(a,b,c) = ab' + bc$ $T = f(a,b,c) = (a+b)(b'+c)$	L3	06
<b>Module-2</b>				
Q. 03	a	Design two bit magnitude comparator and write truth table, relevant expression and logic diagram.	L3	08
	b	Implement the following functions using 3:8 decoder $f1(a,b,c) = \sum m(1,3,5)$ $f2(a,b,c) = \sum m(0,1,6)$	L3	6
	c	Implement $Y=ad+bc'+bd$ using 4:1 mux considering A and B as a select line.	L3	6
<b>OR</b>				
Q.04	a	Explain 4-bit carry look ahead adder with neat diagram and relevant expressions.	L2	10
	b	Implement the following Boolean function using 8:1 multiplexer and 4:1 multiplexer $f(a,b,c,d) = \sum m(0,1,5,6,10,12,14,15)$ .	L3	10
<b>Module-3</b>				
Q. 05	a	Explain the working of Master-Slave JK flip-flop with functional table and timing diagram.	L2	10
	b	Explain Universal Shift Register with the help of logic diagram, mode control table.	L2	10
<b>OR</b>				
Q. 06	a	Derive Characteristic equation for SR,T,D and JK flip-flop with the help of function table	L2	10
	b	Design a Synchronous Mod-6 counter using SR flip-flop for the sequence 0-2-3-6-5-1.	L3	10

<b>Module-4</b>			
Q. 07	a	Realize the 2x1 Multiplexer with active low enable and also write the Verilog program by considering delay time to the signal assignment statements with simulation waveform.	L3 10
	b	Realize the Full Subtractor circuit using Verilog data flow description.	L3 10
OR			
Q. 08	a	List all the data types available in Verilog HDL and explain any four data types with examples.	L2 10
	b	Explain arithmetic and logical operator with example.	L2 10
<b>Module-5</b>			
Q. 09	a	Realize the D-Latch Behavioral description code with circuit diagram, waveform.	L3 10
	b	Write a Verilog structural code for four bit ripple carry adder.	L3 10
OR			
Q. 10	a	Explain with syntax of the following sequential statements in Verilog. i) For-loop ii) While-loop iii) Repeat iv)Forever	L2 8
	b	Write a Verilog program for 8:1 MUX using case statement.	L3 6
	c	Realize the JK flip-flop using Verilog Behavioral description.	L3 6

**Model Question Paper-II with effect from 2023-24 (CBCS Scheme)**

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**Third Semester B.E. Degree Examination**  
**Digital System Design using Verilog**

**TIME: 03 Hours****Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

<b>Module -1</b>			*Bloom's Taxonomy Level	Marks
Q.01	a	What is combinational circuit? Design a combinational logic circuit with three input variables that will produce logic 1 output when more than one input variables are logic 1.		L2
	b	Convert the following Boolean function into canonical minterm and maxterm form in decimal format $R = f(a, b, c) = a + b(a + c) + bc$	L2	06
	c	Find all the prime implicants and essential prime implicants for the following function using k-map method. (i) $M = f(a, b, c, d) = \Sigma(1,5,7,8,9,10,11,13,15)$ (ii) $Y = f(a, b, c, d) = \pi(0,2,3,8,9,10,12,14)$	L3	08
OR				
Q.02	a	. Simplify the following Boolean functions using K-map (i) $Y = f(a, b, c, d) = \pi(0,1,4,5,8,9,11) + d(2,10)$ (ii) $M = f(w, x, y, z) = \Sigma(0,1,2,4,5,6,8,9,12,13,14)$	L3	10
	b	Solve the following Boolean function by using QM minimization technique $P = f(w, x, y, z) = \Sigma(2,3,4,5,13,15) + d(8,9,10,11)$ Verify using K-map method	L3	10
<b>Module-2</b>				
Q. 03	a	Implement the following functions using 3:8 decoder along with OR and/or NOR gates. In each case the gates should be selected so as to minimize their total number of inputs. (a) $f_1(X_2, X_1, X_0) = \Sigma m(0,2,4,6,7)$ and $f_2(X_2, X_1, X_0) = \Sigma m(1,3,5,6,7)$ (b) $f_1(X_2, X_1, X_0) = \Pi M(0,2,4,6,7)$ and $f_2(X_2, X_1, X_0) = \Pi M(1,3,7)$	L3	07
	b	Construct single decade decimal adder with necessary correction circuit design.	L2	08
	c	Design a one-bit comparator circuit.	L2	05
OR				
Q.04	a	Construct the following function $S = f(a,b,c,d) = \Sigma(1,4,5,7,8,9,14,15)$ using (a)8:1 Mux and (b)16:1 Mux	L2	07
	b	Construct the functional table for 4 to 2 line priority encoder with a valid output, assigning highest priority to highest bit position or input with highest index and obtain the minimal sum expressions for the outputs.	L2	07
	c	Implement a Full adder using PAL	L2	06
<b>Module-3</b>				
Q. 05	a	Explain the working of Master-Slave JK flip-flop with functional table and timing diagram	L2	08
	b	Derive the characteristic equations of SR and D Flipflops	L2	04
	c	Make use of negative edge triggered T -Flip Flops to describe the working	L2	08

		of 4-bit binary ripple counter. Also draw the timing diagram.		
OR				
Q. 06	a	Make use of 4-bit shift register circuit to explain the following modes of operations: SISO, SIPO, PISO and PIPO.	L2	08
	b	Develop a mod-5 synchronous counter with the sequence 0,2,6,3,1 using T -Flip Flops.	L3	07
	c	Explain the working of Ring counter with necessary diagram and equations.	L2	05
<b>Module-4</b>				
Q. 07	a	List all the data types available in Verilog HDL. Explain any three data types with examples.	L2	08
	b	Explain three modeling styles available in Verilog with half adder example	L2	07
	c	(ii)Evaluate the following: i)A * B ii) A + B iii) A << 2 iv) {A [3], B} Given: A=0011 B= 0100	L2	05
OR				
Q. 08	a	Explain the Signal declaration and Assignment Statements in Verilog data-flow description.	L1	06
	b	Realize D latch with active high enable and also write the Verilog program by considering delay time to the signal assignment statements with simulation waveforms.	L2	08
	c	Write a verilog dataflow model for full adder	L2	06
<b>Module-5</b>				
Q. 09	a	Write a verilog behavioural description for 8:1 mux along with the design and timing diagrams.	L2	08
	b	Explain different case statements available in verilog with syntax and necessary examples	L2	06
	c	Realize the Binary up-down counter using verilog behavioral description.	L2	06
OR				
Q. 10	a	Explain with syntax of the following sequential statements in Verilog. i) For-loop ii) While-loop iii) Repeat	L2	06
	b	Write a structural description of 3-bit ripple carry adder	L2	08
	c	Write a verilog code for 2x1 mux using If Else statement	L2	06

# CBCS SCHEME

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BEC302

## Third Semester B.E./B.Tech. Degree Examination, Dec.2023/Jan.2024

### Digital System Design Using Verilog

Time: 3 hrs.

Max. Marks: 100

*Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.*

*2. M : Marks , L: Bloom's level , C: Course outcomes.*

Module – 1			M	L	C
Q.1	a.	Develop a truth table of logic which takes two , 2 – bit binary numbers as its input and generate on output equal to 1, when the sum of the two numbers is odd.	7	L1	CO1
	b.	Convert the following Boolean function into : i) $f(abc) = (\bar{a} + b)(b + \bar{c})$ – Min term canonical form. ii) $f(xyz) = x + \bar{x}\bar{z}(y + \bar{z})$ – Max term canonical form.	7	L1	CO1
	c.	List the difference between Prime implicant and Essential prime implicant.	6	L1	CO1

#### OR

Q.2	a.	Simplify the given Boolean function using Quine Mc Cluskey Minimization Technique for the function $R = f(abcd) = \Sigma(0, 1, 2, 6, 7, 9, 10, 12) + dc(3, 5)$ .	10	L1	CO1
	b.	Find the minimal sum and minimal product for the given function using K – map method for the function $R = f(abcd) = \Sigma m(0, 1, 3, 7, 8, 12) + dc(5, 10, 13, 14)$ .	10	L1	CO1

#### Module – 2

Q.3	a.	List the difference between decoder and encoder and implement full adder using IC – 74138.	10	L3	CO2
	b.	What is Comparator? Design a 2 – bit digital comparator.	10	L3	CO2

#### OR

Q.4	a.	Realize the Boolean function $P = f(wxyz) = \Sigma(0, 1, 5, 6, 7, 10, 15)$ using i) 8 : 1 MUX      ii) 4 : 1 MUX.	10	L2	CO2
	b.	With neat logic diagram, explain carry ahead adder.	10	L2	CO2

#### Module – 3

Q.5	a.	Explain the working of master slave JK flip flop with help of Logic diagram , Function table , Logic symbol and Timing diagram.	10	L1	CO3
	b.	Obtain the characteristic equation for : i) SR flip - flop      ii) J – K – flip - flop      iii) D – flip - flop iv) T – flip - flop.	10	L2	CO3

#### OR

<b>Q.6</b>	<b>a.</b>	Design a Synchronous 3 – bit up counter using J K – flip - flop.	<b>10</b>	<b>L4</b>	<b>CO3</b>
	<b>b.</b>	Design a 4 – bit universal shift register using positive edge triggered D – flip - flop and 4 : 1 MUX , to operate as shown in table below :	<b>10</b>	<b>L4</b>	<b>CO3</b>

S <sub>1</sub>	S <sub>0</sub>	Register Operation
0	0	- Hold
0	1	- Shift right
1	0	- Shift left
1	1	- Parallel load operation

**Module – 4**

<b>Q.7</b>	<b>a.</b>	Illustrate the structure and verilog module and write a verilog code for Half – adder using structural model.	<b>10</b>	<b>L3</b>	<b>CO4</b>
	<b>b.</b>	What are different types of operators used in HDL with example?	<b>10</b>	<b>L2</b>	<b>CO4</b>

**OR**

<b>Q.8</b>	<b>a.</b>	Illustrate the structure of Data flow description with example.	<b>10</b>	<b>L3</b>	<b>CO4</b>
	<b>b.</b>	Write the syntax of conditional signal assignment statement. Write a code for 4 : 1 MUX using conditional signal statement.	<b>10</b>	<b>L2</b>	<b>CO4</b>

**Module – 5**

<b>Q.9</b>	<b>a.</b>	Write the structure of Verilog behavioral description.	<b>6</b>	<b>L2</b>	<b>CO4</b>
	<b>b.</b>	Write the syntax of IF statement with example.	<b>7</b>	<b>L2</b>	<b>CO4</b>
	<b>c.</b>	Write a code for D – Latch using Behavioral description.	<b>7</b>	<b>L2</b>	<b>CO4</b>

**OR**

<b>Q.10</b>	<b>a.</b>	Write the syntax of While loop statement with example.	<b>10</b>	<b>L2</b>	<b>CO4</b>
	<b>b.</b>	Write a verilog code of a 3 – bit ripple carry adder using Structural description method.	<b>10</b>	<b>L2</b>	<b>CO4</b>

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<b>ELECTRONIC PRINCIPLES AND CIRCUITS</b>		Semester	3
Course Code	<b>BEC303</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3
Examination nature (SEE)	Theory/Practical		
<b>MODULE-1</b>			
<b>Transistor Biasing:</b> Voltage Divider Bias, VDB Analysis, VDB Load line and Q point, Two supply Emitter Bias, Other types of Bias.			
<b>BJT AC models:</b> Base Biased Amplifier, Emitter Biased Amplifier, Small Signal Operation, AC Beta, AC Resistance of the emitter diode, two transistor models, Analyzing an amplifier, H parameters, Relations between R and H parameters.			
<b>Voltage Amplifiers:</b> Voltage gain, Loading effect of Input Impedance.			
<b>CC Amplifiers:</b> CC Amplifier, Output impedance. [Text1]			
<b>MODULE-2</b>			
<b>MOSFET:</b> Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor. Small signal operation and modelling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.			
<b>MOSFET Amplifier configuration:</b> Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance, The Common Gate Amplifier, Source follower. [Text 2]			
<b>MODULE-3</b>			
<b>Linear OP-Amp Circuits:</b> Summing Amplifier and D/A Converter, Nonlinear Op-amp Circuits: Comparator with zero reference, Comparator with non-zero references. Comparator with Hysteresis.			
<b>Oscillator:</b> Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator.			
<b>The 555 timer:</b> Monostable Operation, Astable Operation. [Text1]			
<b>MODULE-4</b>			
<b>Negative Feedback:</b> Four Types of Negative Feedback, VCVS Voltage gain, Other VCVS Equations, ICVS Amplifier, VCIS Amplifier, ICIS Amplifier (No Mathematical Derivation).			
<b>Active Filters:</b> Ideal Responses, First Order Stages, VCVS Unity Gain Second Order Low Pass Filters, VCVS Equal Component Low Pass Filters, VCVS High Pass Filters, MFB Band Pass Filters, Band stop Filters. [Text1]			
<b>MODULE-5</b>			
<b>Power Amplifiers:</b> Amplifier terms, Two load lines, Class A Operation, Class B operation, Class B push pull emitter follower, Class C Operation.			
<b>Thyristors:</b> The four-layer Diode, SCR, SCR Phase control, Bidirectional Thyristors, IGBTs, Other Thyristors. [Text1]			

**PRACTICAL COMPONENT OF IPCC***(Experiments can be conducted either using any circuit simulation software or discrete components)*

Sl.NO	Experiments
1	Design and Test (i) Bridge Rectifier with Capacitor Input Filter (ii) Zener voltage regulator
2	Design and Test Biased Clippers – a)Positive, b) Negative , c) Positive-Negative Positive and Negative Clampers with and without Reference.
3	Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.
4	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.
5	Design and test Emitter Follower
6	Design and plot the frequency response of Common Source JFET/MOSFET amplifier
7	Test the OP-Amp Comparator with zero and non-zero reference and obtain the Hysteresis curve.
8	Design and test Full wave Controlled rectifier using RC triggering circuit.
9	Design and test Precision Half wave and full wave rectifiers using OP-Amp
10	Design and test RC phase shift oscillator

**Text Books**

1. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017, ISBN:978-0- 07-063424-4.
2. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6th Edition, Oxford, 2015.ISBN:978-0-19-808913-1

**Model Question Paper-I with effect from 2023-24 (CBCS Scheme)**

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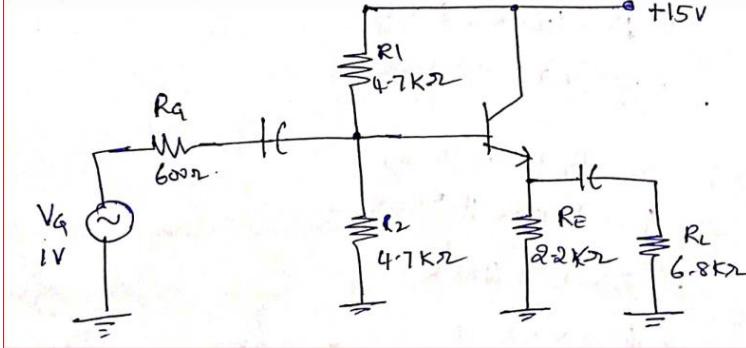
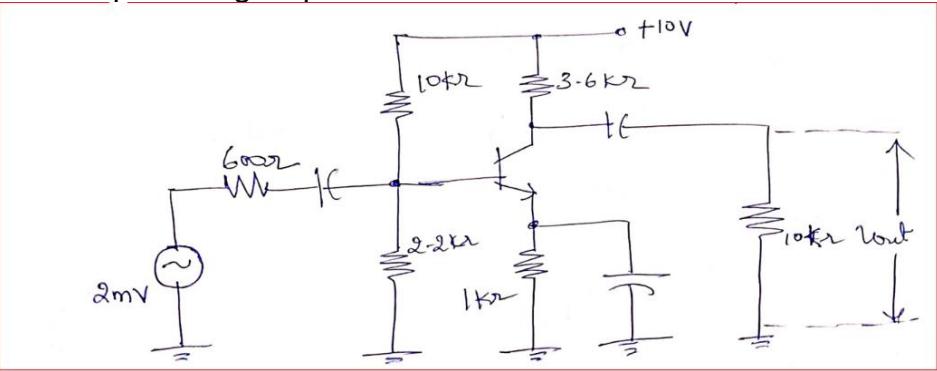
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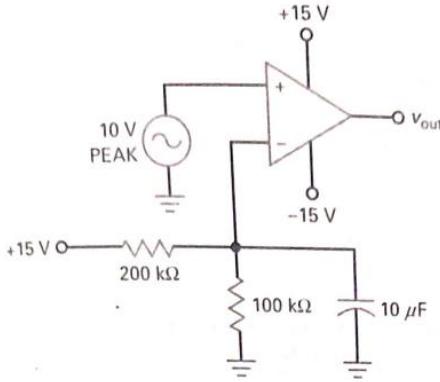
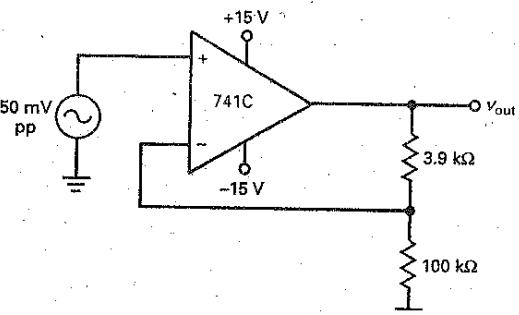
**Third Semester B.E. Degree Examination**  
**Electronic Principles and circuits**

TIME: 03 Hours

Max. Marks: 100

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

Q.No	Question	Marks	Bloom's Level
<b>MODULE-1</b>			
1	<p>a. Develop an expression for the operating point <math>I_C</math> and <math>V_{CE}</math> for the voltage divider bias circuit using approximate analysis. Also Calculate the operation point for the VDB circuit given <math>V_{cc}=10V</math>, <math>R_1=10K\Omega</math>, <math>R_2=2.2K\Omega</math>, <math>R_c= 3.6K\Omega</math>, <math>R_E= 1K\Omega</math></p> <p>b. For the circuit shown in Fig 1b, determine the voltage gain and ac load voltage if <math>\beta = 150</math></p> 	10	L3
	<b>Fig 1b</b>		
<b>OR</b>			
2	<p>a. Design the voltage divider bias circuit to meet the following specifications <math>V_{cc}=10V</math>, <math>V_{CE}</math> at mid point, stiff voltage divider, collector current <math>1mA</math>, <math>\beta_{dc} = 70 - 200</math></p> <p>b. For the circuit shown below in Fig 2b, the ac generator has an internal resistance of <math>600\Omega</math> for a voltage divider circuit. Determine the output voltage if <math>\beta = 300</math></p> 	10	L3
	<b>Fig 2b</b>		
<b>MODULE-2</b>			
3	a. With neat circuit diagrams, explain biasing of MOSFET by fixing the	10	L3

	gate voltage b. With neat circuit diagram, develop an expression for voltage gain, input impedance and output impedance for common gate amplifier.	10	L3
<b>OR</b>			
4	a. Develop an expression for drain to source voltage for a MOSFET amplifier using drain to gate feedback resistor.	10	L3
	b. Develop an expression for transconductance in terms of drain current and overdrive voltage.	4	L3
	c. With neat circuit diagram, develop an expression for voltage gain, input impedance and output impedance for common source amplifier without source resistance.	6	L3
<b>MODULE-3</b>			
5	a. With neat circuit diagram, explain the operation of R-2R DAC	7	L2
	b. For the circuit shown in Fig 5b, the input voltage is a sine wave with peak value of 10V. Determine the trip point. Also plot the input output waveform	7	L3
	 <p>Fig 5b</p>		
<b>OR</b>			
6	a. With neat circuit diagram, internal diagram of 555 timer and waveforms explain the operation of astable multivibrator.	10	L3
	b. With neat circuit diagram, explain the operation of wein bridge oscillator	10	L3
<b>MODULE-4</b>			
7	a. Classify negative feedback amplifiers and explain each with neat block diagram.	10	L3
	b. Calculate the feedback fraction, ideal closed loop gain, percentage error and exact closed loop voltage gain. Use AOL = 100,000 for 741C	5	L3
			
<b>OR</b>			
8	a. Classify the filters and explain the ideal response for each of the	10	L3

	filters. b. With neat circuit diagrams, explain the operation of first order low pass filter and high pass filter		
<b>MODULE-5</b>			
<b>9</b>	a. With neat circuit diagram and waveform explain SCR phase control using RC circuit	<b>10</b>	<b>L3</b>
	b. With neat circuit diagram, explain the operation of UJT and hence explain how it is used as relaxation oscillator.	<b>10</b>	<b>L3</b>
<b>OR</b>			
<b>10</b>	Make use of break over characteristics to explain the operation of 4 layer diode	<b>10</b>	<b>L3</b>
	Write short notes on IGBT	<b>5</b>	<b>L3</b>
	Explain bi-directional thyristors in brief.	<b>5</b>	<b>L3</b>

# CBCS SCHEME

USN

BEC303

## Third Semester B.E./B.Tech. Degree Examination, Dec.2023/Jan.2024

### Electronic Principles and Circuits

Time: 3 hrs.

Max. Marks: 100

*Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.*

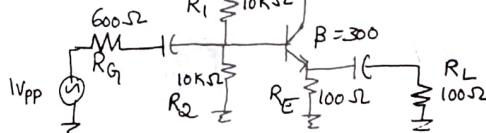
*2. M : Marks , L: Bloom's level , C: Course outcomes.*

<b>Module – 1</b>			M	L	C
<b>Q.1</b>	a.	Explain the simplified analysis of a voltage divider bias circuit of a transistor. Also list the steps in analysis.	8	L1	CO1
	b.	Analyze a VDB Amplifier circuit with respect to DC circuit, AC - $\pi$ model, AC – T model.	7	L3	CO1
	c.	Design a positive and negative biased clipper circuit.	5	L3	CO1

**OR**

<b>Q.2</b>	a.	With the importance of Coupling capacitor, explain the Base – Biased amplifier circuit. Support your answer with base current , collector current and collector voltage. Also draw its voltage waveforms.	10	L3	CO1
	b.	Explain the basic idea of Common – Collector (CC) amplifier. Give the mathematical relation of AC. Emitter resistance ( $r_e$ ) , Voltage Gain ( $A_v$ ) , Input impedance of the base ( $Z_{in(base)}$ ) and Input impedance of the stage ( $Z_{in(stage)}$ ).	6	L2	CO1
	c.	Calculate the output impedance for the circuit below, given $V_{BQ} = 15V$ .	4	L2	CO1

Fig. Q2(c)



**Module – 2**

<b>Q.3</b>	a.	Biasing by fixing $V_{GS}$ is not a good approach to bias a MOSFET. Why? Explain biasing by fixing $V_G$ and connecting a resistance in the source for MOSFET.	8	L2	CO2
	b.	Design a fixed $V_G$ and resistance in the source biasing circuit, to establish drain current $I_D = 0.5mA$ , $V_t = 1V$ , $K_n^1 W/K = 1mA/V^2$ , $\lambda = 0$ . Use power supply $V_{DD} = 15V$ .	5	L3	CO2
	c.	Obtain the transfer and drain characteristics of n – channel MOSFET and calculate Drain resistance ( $r_d$ ) , Mutual conductance ( $gm$ ) and Amplification factor ( $\mu$ ).	7	L2	CO2

**OR**

<b>Q.4</b>	a.	Illustrate the development of T – equivalent circuit model for the MOSFET.	6	L2	CO2
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	b.	Draw and explain the small signal equivalent model for Common – Source amplifier without source resistance and write the equation for $R_{in}$ , $R_{out}$ , $A_v$ and $G_v$ .	8	L2	CO2
	c.	For a Common Gate (CG) amplifier circuit , given $g_m = 1\text{mA/V}$ , $R_D = 15\text{k}\Omega$ , $R_L = 15\text{K}\Omega$ , $R_{sig} = 50\Omega$ , $R_G = 4.7\mu\Omega$ . Find $R_{in}$ , $R_{out}$ , $A_{vo}$ , $A_v$ and $G_v$ .	6	L2	CO2

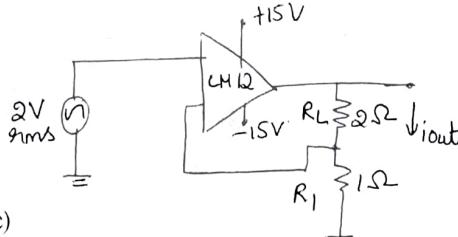
**Module – 3**

Q.5	a.	Explain how an Op – amp summer circuit be configured to function as a subtractor.	5	L1	CO3
	b.	How does the design and configuration of an Op – amp R/2R DAC contribute to its accuracy and performance in converting digital signals to analog signals?	8	L2	CO3
	c.	Design and draw the frequency response of common source JFET / MOSFET amplifier.	7	L2	CO3

**OR**

Q.6	a.	Describe the working of inverting Schmitt trigger circuit. How is Schmitt trigger different from regular comparator circuit? Explain with the help of Hysteresis curve.	8	L2	CO3
	b.	Explain the working of Colpitts Oscillator with CE connection.	6	L2	CO3
	c.	Explain the Monostable operation of 555 timers.	6	L2	CO3

**Module – 4**

Q.7	a.	Explain the four types of Negative feedback amplifier.	8	L1	CO4
	b.	Explain the VCVS amplifier. Obtain its exact closed – loop voltage gain and Ideal Closed – Loop Voltage gain. Also define Gain stability , Closed loop input impedance and Closed loop output impedance of a VCVS amplifier.	8	L2	CO4
	c.	Calculate the load power , load current for the given VCIS amplifier circuit.   Fig. Q7(c)	4	L2	CO4

**OR**

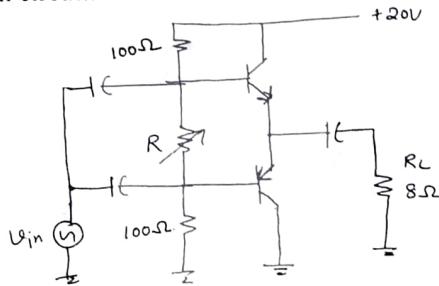
Q.8	a.	Explain the Ideal response of filters.	8	L1	CO4
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	b. Determine the pole frequency, Q, Cutoff frequency and 3 - dB frequency, for the filter circuit given below :	5	L2	CO4
	<p>Fig. Q8(b)</p> <p>Given <math>K_0 = 0.99</math>, <math>K_C = 1.38</math>, <math>K_3 = 1.54</math>.</p>			
	c. Design a Halfwave and Fullwave precision rectifier using Op - amp.	7	L3	CO4

**Module - 5**

Q.9	a. Explain class A amplifier , interns of its power gain, Output power , Power dissipation and efficiency.	8	L1	CO5
	b. Explain class B push pull emitter follower amplifier. How can the crossover distortion be eliminated?	8	L1	CO5
	c. Calculate the maximum transistor power dissipation and maximum output power for the given circuit.	4	L2	CO5

Fig. Q9(c)

**OR**

Q.10	a. What is an SCR? With the help of basic SCR circuit, explain the gate triggering.	6	L1	CO5
	b. Explain the phase control method of TRIAC, along with the voltage waveforms.	7	L1	CO5
	c. Design a full wave controlled rectifier circuit using RC triggering.	7	L3	CO5

\* \* \* \* \*

<b>NETWORK ANALYSIS</b>		Semester	3
Course Code	<b>BEC304</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		
<b>Module-1</b>			
<b>Basic Concepts:</b> Practical sources, Source transformations, Network reduction using Star - Delta transformation, Loop and node analysis with linearly dependent and independent sources for DC and AC networks.			
<b>Module-2</b>			
<b>Network Theorems:</b> Superposition, Millman's theorems, Thevenin's and Norton's theorems, Maximum Power transfer theorem.			
<b>Module-3</b>			
<b>Transient behavior and initial conditions:</b> Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.			
<b>Module-4</b>			
<b>Laplace Transformation &amp;Applications:</b> Solution of networks, step, ramp and impulse responses, waveform Synthesis.			
<b>Module-5</b>			
<b>Two port network parameters:</b> Definition of Z, Y, h and Transmission parameters, modelling with these parameters, relationship between parameters sets.			
<b>Resonance: Series Resonance:</b> Variation of Current and Voltage with Frequency, Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor, Selectivity with Variable Capacitance, Selectivity with Variable Inductance.			
<b>Parallel Resonance:</b> Selectivity and Bandwidth, Maximum Impedance Conditions with C, Land f Variable, current in Anti-Resonant Circuit, The General Case-Resistance Present in both Branches.			
<p><b>Text Books:</b></p> <ol style="list-style-type: none"> <li>1. M.E.Van Valkenburg (2000), Network Analysis, Prentice Hall of India, 3<sup>rd</sup>edition, 2000, ISBN:9780136110958.</li> <li>2. Roy Choudhury-Networks and Systems, 2nd edition, New Age International Publications, 2006, ISBN: 9788122427677</li> </ol> <p><b>Reference Books:</b></p> <ol style="list-style-type: none"> <li>1. Hayt, Kemmerly and Durbin-Engineering Circuit Analysis, TMH 7<sup>th</sup> Edition, 2010.</li> <li>2. J.David Irwin/ R.Mark Nelms- Basic Engineering Circuit Analysis JohnWiley,8<sup>th</sup>ed,2006.</li> <li>3. Charles K Alexander and Mathew NO Sadiku-Fundamentals of Electric Circuits, Tata McGraw-Hill,3rc1 Ed,2009.</li> </ol>			

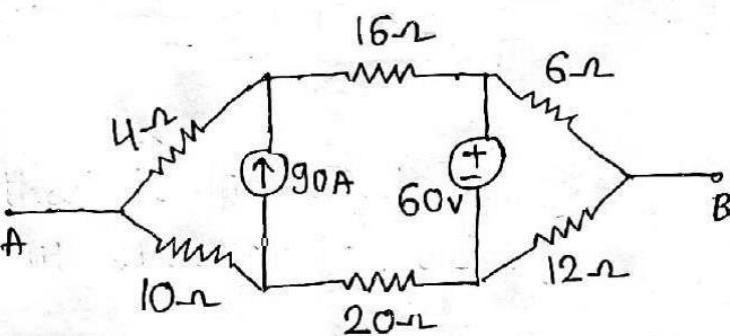
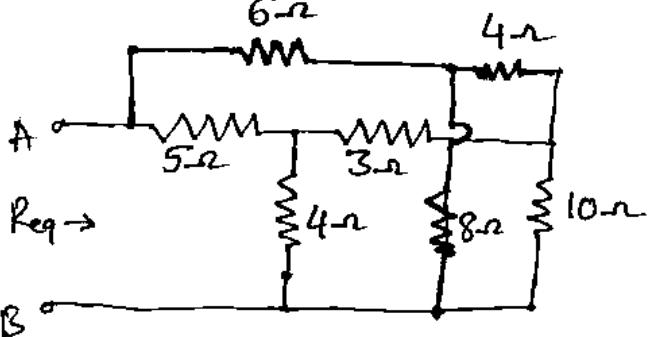
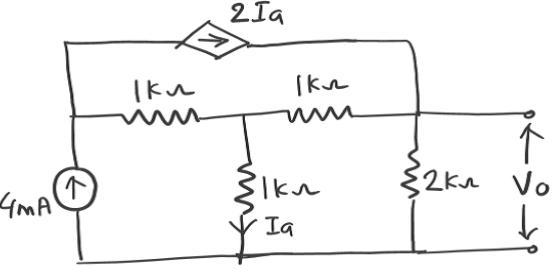
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**Third Semester B.E. Degree Examination**  
**Network Analysis**

**TIME: 03 Hours****Max. Marks: 100**

Note: Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**

Module -1			*Bloom's Taxonomy Level	Marks
Q.01	a	b		
		Reduce the Network shown in Fig. 1(a), to a single voltage source in series with a resistance using source shifting and source transformation.	L3	7
		 <p style="text-align: center;"><b>Fig. Q1(a)</b></p>		
	b	Find equivalent resistance between A and B using star delta transformation for the network shown in Fig. 1(b).	L2	7
		 <p style="text-align: center;"><b>Fig. Q1(b)</b></p>		
	c	Determine $V_o$ using mesh analysis for the network shown in Fig. 1(c) below.	L3	6
		 <p style="text-align: center;"><b>Fig. Q1(c)</b></p>		
OR				

Q.02	a	<p>Find <math>V_x</math> in the network shown in Fig. 2(a) using Node analysis.</p> <p>Fig. Q2(a)</p>	L3	7
	b	<p>Find the equivalent resistance between a and b using star delta transformation for the circuit shown in Fig. 2(b)</p> <p>Fig. Q2(b)</p>	L2	7
	c	<p>Determine Voltage <math>V_3</math> in the circuit shown in Fig. 2(c) using mesh analysis.</p> <p>Fig. Q2(c)</p>	L3	6
<b>Module-2</b>				
Q. 03	a	<p>Find current <math>I_x</math>, in the circuit shown in Fig. 3(a) using superposition theorem.</p> <p>Fig. Q3(a)</p>	L3	10

- b Find Thevenin's equivalent at terminals A and B for the circuit shown in Fig. 3(b).

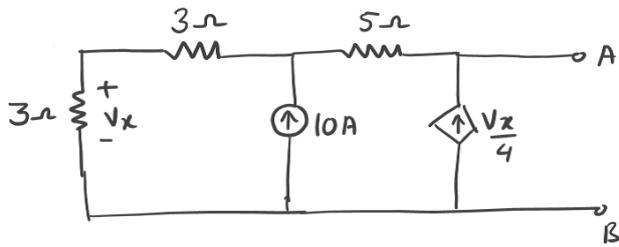


Fig. Q3(b)

**OR**

- Q.04 a Determine the current through the load resistance in the circuit shown in Fig. 4(a) using Norton's theorem

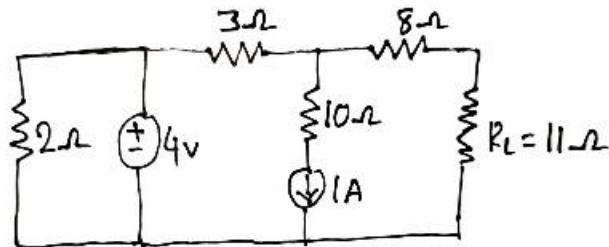


Fig. Q4(a)

- b Find the value of  $Z_L$  for which maximum power transfer occurs in the network shown in Fig. 4(b).

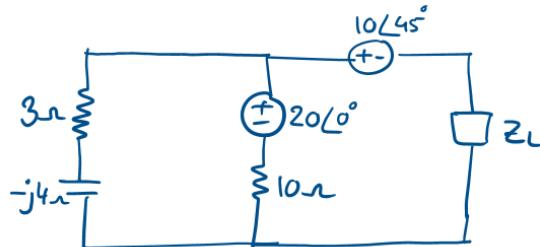


Fig. Q4(b)

- c State Millman's Theorem

**Module-3**

- Q. 05 a In the network shown in Fig. 5(a), a steady state is reached with the switch k open. At time  $t=0+$ , the switch is closed. Determine the value of  $V_a(0-)$  and  $V_a(0+)$ .

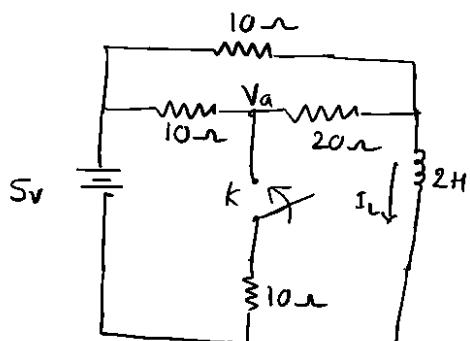


Fig. Q5(a)

L3

10

	b	<p>For the circuit shown in Fig. 5(b), the switch 'S' is changed from position 1 to 2 at <math>t = 0</math>, the steady state is reached at position 1.</p> <p>Find the value of <math>i</math>, <math>\frac{di}{dt}</math>, <math>\frac{d^2i}{dt^2}</math> at <math>t = 0^+</math>. Assume that the capacitor is initially uncharged.</p>	L3	10
		<b>OR</b>		
Q. 06	a	<p>For the circuit shown in Fig. 6(a), has zero capacitor voltage and zero inductor current when the switch k is open. At <math>t=0</math>, the switch k is closed. Solve for</p> <p>i) <math>v_1</math> and <math>v_2</math> at <math>t = 0^+</math> ii) <math>\frac{dv_1}{dt}</math> and <math>\frac{dv_2}{dt}</math> at <math>t = 0^+</math></p>	L3	10
	b	<p>For the network shown in Fig. 6(b), the network is steady state with switch k closed. At <math>t = 0</math>, switch is opened. Determine voltage across switch <math>V_k</math>, <math>\frac{dV_k}{dt}</math>, at <math>t = 0^+</math>.</p>	L3	10
		<b>Module-4</b>		
Q. 07	a	<p>In the circuit shown in Fig. 7(a), the source voltage is <math>V(t) = 50\sin 250t</math> V. Using Laplace Transform determine current when switch k is closed at <math>t=0</math>.</p>	L3	10

- b Determine the Laplace transform of the waveform shown in Fig. 7(b).

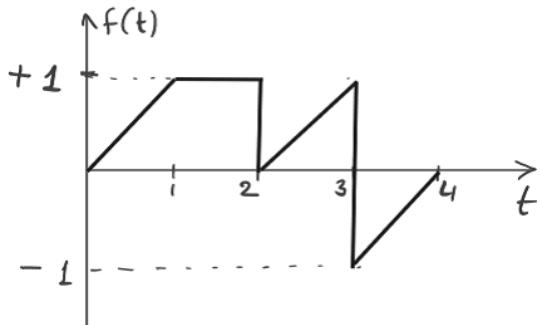


Fig. Q7(b)

**OR**

- Q. 08 a Determine  $v_c(t)$  and the current  $i_c(t)$  for  $t \geq 0$  for the circuit shown in Fig. 8(a).

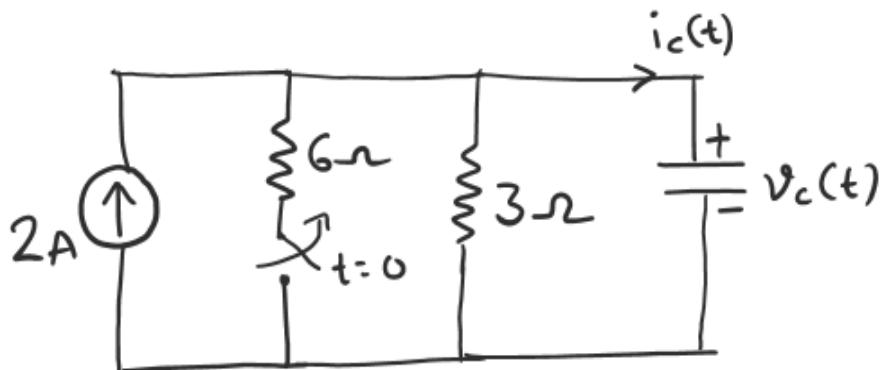


Fig. Q8(a)

- b Determine the Laplace transform of periodic saw tooth waveform for the circuit shown in Fig. 8(b).

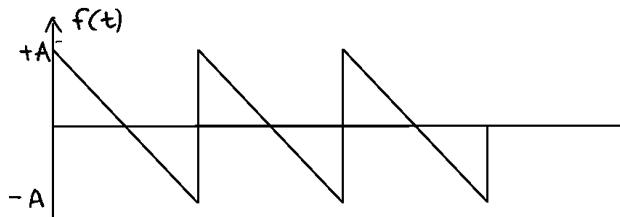


Fig. Q8(b)

**Module-5**

- Q. 09 a Find Z and T parameters for the circuit shown in Fig. 9(a).

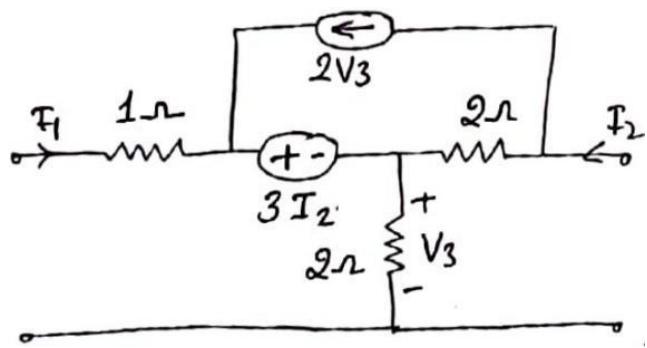


Fig. Q9(a)

	b	Obtain the impedance parameters in terms of Hybrid parameters.	L2	6
	c	A coil of $20\Omega$ resistance has inductance of $0.2H$ and is connected in parallel with capacitance of $100\mu F$ . Find the resonant frequency at which circuit will act as non-inductive resistance. Also find dynamic resistance	L2	7
OR				
Q. 10	a	Determine Transmission parameters for the circuit shown in Fig. 10(a).	L2	7
<p style="text-align: center;"><b>Fig. Q10(a)</b></p>				
	b	Express Z parameters in terms of Transmission (ABCD) parameters	L2	6
	c	A 400Hz AC source is connected in series with a capacitor and a coil whose resistance and inductance are $20m\Omega$ and $6mH$ respectively. If the circuit is in resonance at 200Hz, Find i Value of Capacitor ii Voltage across capacitor. iii Maximum energy stored. iv Half power frequencies	L2	7



# CBCS SCHEME

(9)

USN

BEC304

## Third Semester B.E./B.Tech. Degree Examination, Dec.2023/Jan.2024

### Network Analysis

Time: 3 hrs.

Max. Marks: 100

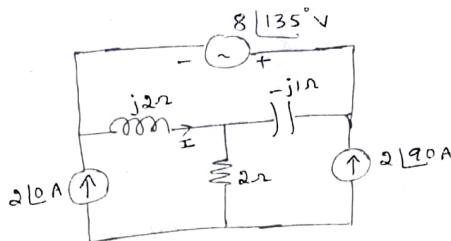
*Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.  
2. M : Marks , L: Bloom's level , C: Course outcomes.*

Module - 1			M	L	C
Q.1	a.	Explain the classification of electrical networks.	8	L2	CO1
	b.	For the network shown in Fig. Q1(b), find the current through load resistor 'R' using loop analysis.	6	L3	CO1
	c.	For the network shown in Fig. Q1(c), find the equivalent resistance between the terminals A - B using Star – Delta transformation.	6	L3	CO1
OR					
Q.2	a.	Derive an expression for the equivalent impedances between the terminals for Delta – Star transformation.	6	L2	CO1
	b.	Use modal analysis to find the value of voltage ' $V_x$ ' in the circuit shown in Fig. Q2(b), such that the current through $(2 + j3)\Omega$ impedance is zero.	7	L3	CO1
	c.	Determine the current through $12\Omega$ resistor shown in Fig. Q2(c), using Source Shifting / Transformation method.	7	L3	CO1

## Module - 2

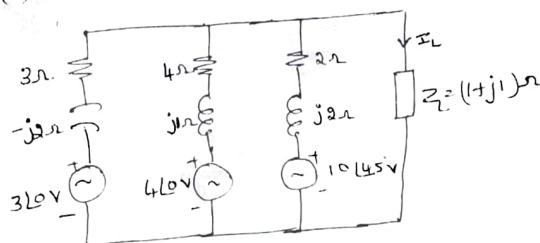
Q.3	a.	Using Superposition theorem, obtain the current 'I' for the network shown in Fig. Q3(a).	10	L2	CO1
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Fig. Q3(a)



b.	Using Millman's theorem, calculate the current through the load in the circuit shown in Fig. Q3(b).	10	L3	CO2
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Fig. Q3(b)

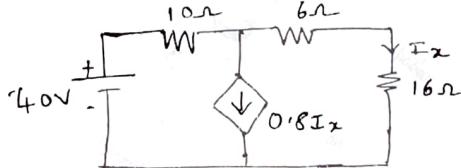


OR

Q.4	a.	State and explain Norton's theorem.	6	L2	CO2
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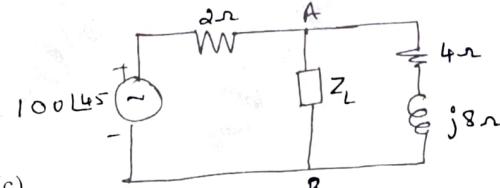
b.	For the network shown in Fig. Q4(b), find the current through $16\Omega$ resistor using Thevenin's theorem.	7	L3	CO2
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Fig. Q4(b)



c.	For the network shown in Fig. Q4(c), find the value of $Z_L$ for which maximum power transfer occurs. Also find the maximum power.	7	L3	CO2
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Fig. Q4(c)



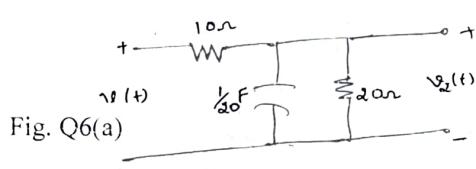
## Module - 3

Q.5	a.	Explain the initial and final conditions in basic elements.	6	L2	CO3
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	b.	For the circuit shown in Fig. Q5(b), the switch 'K' is changing the position from 1 to 2 at $t = 0$ . Steady state condition has been reached at position 1. Find the value of $i$ , $\frac{di}{dt}$ , $\frac{d^2i}{dt^2}$ at $t = 0^+$ .	8	L3	CO3
	c.	Obtain an expression for transient response $i(t)$ of a series R – L circuit when excited by DC supply.	6	L2	CO3

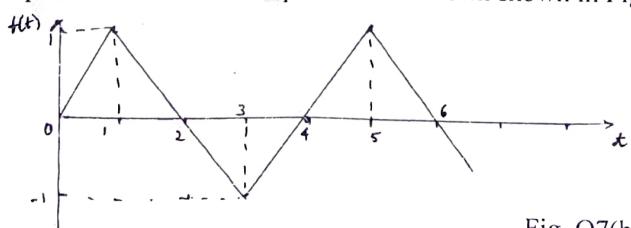
OR

Q.6	a.	In the circuit shown in Fig. Q6(a), $v_1(t) = e^{-t}$ for $t \geq 0$ and zero for all $t < 0$ . If the capacitor is initially uncharged, determine the value of $v_2(t)$ , $\frac{dv_2(t)}{dt}$ , $\frac{d^2v_2(t)}{dt^2}$ and $\frac{d^3v_2(t)}{dt^3}$ at $t = 0^+$ .	10	L3	CO3
	b.	For the circuit shown in Fig. Q6(b), the switch is closed at $t = 0$ . Determine $i$ , $\frac{di}{dt}$ , $\frac{d^2i}{dt^2}$ and $\frac{d^3i}{dt^3}$ at $t = 0^+$ .	10	L3	CO3

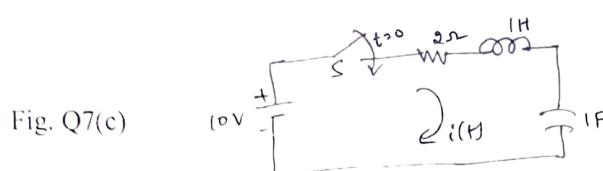


## Module - 4

Q.7	a.	State and prove Initial Value Theorem.	6	L2	CO3
	b.	Find the Laplace Transform of the periodic waveform shown in Fig. Q7(b).	8	L3	CO3



- c. Using Laplace transform, determine the current  $i(t)$  in the circuit shown in Fig. Q7(c), when the switch 'S' is closed at  $t = 0$ . Assume zero initial conditions.



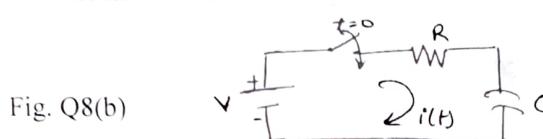
6 L3 CO3

**OR**

- Q.8 a. State and prove differentiator by 'S' domain property.

6 L2 CO3

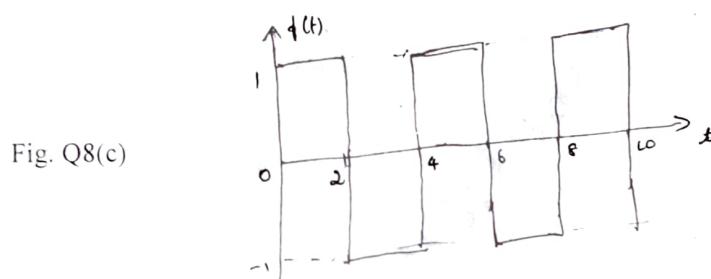
- b. In the circuit shown in Fig. Q8(b), the switch is closed at  $t = 0$ . Obtain the expression for the current.



6 L3 CO3

- c. Obtain the Laplace Transform of the square wave shown in Fig. Q8(c).

8 L3 CO3

**Module – 5**

- Q.9 a. What are Impedance and Hybrid parameters? Derive the expression for the same.

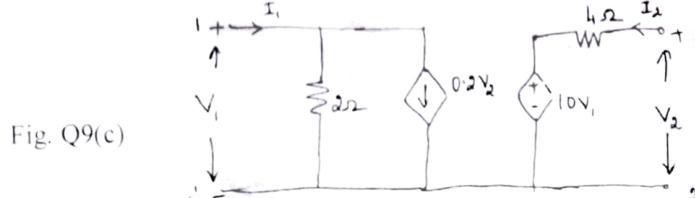
8 L2 CO4

- b. Derive an expression for Transmission parameters in terms of Z – parameters.

5 L2 CO4

- c. For the circuit shown in Fig. Q9(c), find Y – parameters.

7 L3 CO4



- Q.10 a. Derive an expression for bandwidth of a series Resonant circuit.

7 L2 CO5

	b. A series RLC circuit consists of a resistance of $1\text{ k}\Omega$ and an inductance of $100\text{mH}$ in series with capacitance of $10\text{PF}$ connected across $100\text{V}$ supply. Determine i) Resonant frequency ii) Quality factor iii) Maximum current in the circuit iv) Bandwidth v) Half power frequencies v) Selectivity factor.	7	L3	CO5
c.	For the circuit shown in Fig. Q10(c), find i) Resonant frequency ii) Quality factor iii) Bandwidth iv) Impedance at resonance v) Current at resonance.	6	L3	CO5

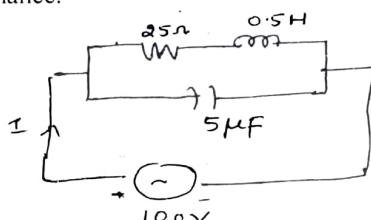


Fig. Q10(c)

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<b>COMPUTER ORGANIZATION AND ARCHITECTURE</b>		Semester	3		
Course Code	<b>BEC306C</b>	CIE Marks	50		
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50		
Total Hours of Pedagogy	40	Total Marks	100		
Credits	03	Exam Hours	3		
Examination type (SEE)	Theory	<b>Module-1</b>			
<p><b>Basic Structure of Computers:</b> Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance -Processor Clock, Basic Performance Equation (up to 1.6.2 of Chap1 of Text).</p> <p><b>Machine Instructions and Programs:</b> Numbers, Arithmetic Operations and Characters, IEEE standard for Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing (up to 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text).</p>					
<b>Module-2</b>					
Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions (from 2.4.7 of Chap2, except 2.9.3, 2.11 & 2.12 of Text).					
<b>Module-3</b>					
<p><b>Input/ Output Organization:</b> Accessing I/O Devices, Interrupts -Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access (up to 4.2.4 and 4.4 except 4.4.1 of Chap 4 of Text).</p>					
<b>Module-4</b>					
<p><b>Memory System:</b> Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage- Magnetic Hard Disks (5.1, 5.2, 5.2.1, 5.2.2, 5.2.3, 5.3, 5.5 (except 5.5.1 to 5.5.4), 5.7 (except 5.7.1), 5.9, 5.9.1 of Chap 5 of Text).</p>					
<b>Module-5</b>					
<p><b>Basic Processing Unit:</b> Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Microprogrammed Control (up to 7.5 except 7.5.1 to 7.5.6 of Chap 7 of Text).</p>					
<p><b>Text Book:</b></p> <ol style="list-style-type: none"> <li>Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5<sup>th</sup> Edition, Tata McGrawHill, 2002.</li> </ol> <p><b>Reference Books:</b></p> <ol style="list-style-type: none"> <li>David A. Patterson, John L. Hennessy: Computer Organization and Design-The Hardware/ Software Interface ARM Edition, 4<sup>th</sup> Edition, Elsevier, 2009.</li> <li>William Stallings: Computer Organization &amp; Architecture, 7<sup>th</sup> Edition, PHI, 2006.</li> <li>Vincent P. Heuring &amp; Harry F. Jordan: Computer Systems Design and Architecture, 2<sup>nd</sup> Edition, Pearson Education, 2004.</li> </ol>					

**Model Question Paper with effect from 2023-24 (CBCS  
2022 Scheme)**

USN

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**Third Semester B.E. Degree Examination  
Subject Title: COMPUTER ORGANISATION  
& ARCHITECTURE**

Time :03 Hours

Max Marks:100

**Note:** Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

<b>Module -1</b>			<b>RBL</b>	<b>COs</b>	<b>Marks</b>	<b>PO</b>
Q.01	a	With a neat diagram, describe the functional units of a computer	L2	1	8	1
	b	Explain little endian and big endian byte address assignment with a neat diagram. Show how the number 34761395 is stored using these methods.	L2	1	6	1,2
	c	With a neat diagram, discuss the operation concepts in a computer highlighting the role of PC, MAR, MDR & IR	L2	1	6	1,2
<b>OR</b>						
Q.02	a	Explain the IEEE standard used for single & double precision floating point number representation with examples	L2	1	8	1,2
	b	Perform the subtraction on the following pairs of numbers using 5-bit signed 2's complement format. Determine about overflow in each case i) +12 and +9 ii) -15 and -9 iii) +10 and -8	L3	1	6	1,2
	c	Discuss the following with an example i) Three-address instruction ii) Two-address instruction iii) One-address instruction	L2	1	6	1,2
<b>Module-2</b>						
Q. 03	a	Describe the following addressing modes with an example i) Register ii) Direct iii) Indirect iv) Index	L2	2	8	1,2
	b	Define Stack, Explain push & pop operations on stack with neat diagram and examples	L1	2	6	1
	c	Consider a register R1 to size 16-bits with initial data 5876d. With neat diagram, depict the output in each case after performing the following operations i) LshiftL #2,R1 ii) AshiftR #1,R1 iii) RotateR #1,R1	L2	2	6	1,2
<b>OR</b>						
Q.04	a	Consider a database of marks scored by students in 3 tests stored in memory starting at address LIST. Each student record consists of student ID followed by marks in 3 tests. Assume each of there to be 4 bytes in size. There are 50 students in the class & this value is stored at location NUM  i) Sketch the memory map showing all details	L3	2	10	2,3

		ii) Develop an ALP using indexed addressing mode to compute the sum of scores by all the students in Test 2 and store the results in location SUM. Write appropriate comments				
	b	Define subroutine. With a program segment illustrate parameter passing using registers	L2	2	6	1,2
	c	Explain memory operations with examples	L2	2	4	1,2
<b>Module-3</b>						
Q. 05	a	Define interrupt. Point out & explain the various ways of enabling & disabling interrupts	L2	3	10	1,2
	b	Explain operation of DMA with neat diagram	L2	3	6	1,2
	c	Write a explanatory note on interrupt hardware	L1	3	4	1,2
OR						
Q. 06	a	Illustrate interrupt priority scheme with neat diagram	L2	3	8	1,2
	b	Distinguish between memory mapped I/O and standard I/O write a program segment to read a line of text from keyboard & display it.	L2	3	6	1,2
	c	Explain the concept of Vectored Interrupt	L2	3	6	1,2
<b>Module-4</b>						
Q. 07	a	With a neat diagram, explain the principal of working of magnetic disk	L2	4	10	1,2
	b	Explain the internal organization of 2M x 8 DRAM chip with neat diagram	L2	4	10	1,2
OR						
Q. 08	a	Illustrate Internal structure of static memory	L3	4	10	1,2
	b	With a neat diagram, explain virtual memory organization	L2	4	10	1,2
<b>Module - 5</b>						
Q. 09	a	Explain Single bus organization of the datapath inside a processor with neat diagram	L2	5	10	1,2
	b	Develop the complete control sequence for the execution of instruction Add (R3), R1	L3	5	10	2,3
OR						
Q. 10	a	Describe Three-bus organization of the datapath with a neat diagram.	L2	5	10	1,2
	b	Discuss Hardwired control unit organization with relevant diagram	L2	5	10	1,2

**Model Question Paper-I with effect from 2023-24 (CBCS Scheme)**

USN

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**Third Semester B.E. Degree Examination**  
**COMPUTER ORGANIZATION AND ARCHITECTURE**

**TIME: 03 Hours****Max. Marks: 100**Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

<b>Module -1</b>			*Bloom's Taxonomy Level	Marks
Q.01	a	Explain the operation of computer with neat block diagram		L2
	b	Write a program to evaluate the arithmetic statement $Y = (A+B)*(C+D)$ using three address, two address, one address, zero address instruction.	L3	8M
	c	Write a short note on i) Basic performance equation ii) Clock rate	L2	6M
OR				
Q.02	a	Explain Bus structure architecture with neat diagram.	L2	6M
	b	Illustrate Instruction and sequencing with an example.	L3	8M
	c	Explain the memory operation.	L2	6M
<b>Module-2</b>				
Q. 03	a	Define Addressing Modes? Explain various types of addressing modes with example.	L2	10M
	b	Define Subroutine and parameter passing, Explain how to pass the parameter by value & by reference.	L2	10M
OR				
Q.04	a	What are assembler directives? Explain any five assembler directives.	L2	10M
	b	Explain shift & rotate operation with example.	L2	10M
<b>Module-3</b>				
Q. 05	a	What is Bus Arbitration? Explain centralized and distributed arbitration method with neat diagram.	L2	10M
	b	With relevant diagram, discuss the implementation of interrupt priority using individual interrupt request.	L2	10M
OR				
Q. 06	a	Explain DMA techniques and its importance.	L2	10M
	b	Define Interrupt? Point out and explain the various ways of enabling and disabling interrupts.	L2	10M
<b>Module-4</b>				
Q. 07	a	Explain the connection of the main memory to the processor.	L2	10M
	b	Explain the internal organization of 1Mx1 dynamic memory chip with neat diagram.	L2	10M
OR				
Q. 08	a	Explain the Memory hierarchy in computer system.	L2	10M
	b	Explain the magnetic disk principle with neat diagram	L2	10M
<b>Module-5</b>				
Q. 09	a	Explain single Bus Organization with neat diagram	L2	10M
	b	Write a steps involved in execution of an instruction. And explain the control sequence for execution of the instruction Add(R3),R1	L3	10M
OR				
Q. 10	a	Explain complete processor with neat diagram	L2	10M
	b	Explain the organization of micro programmed control unit with neat diagram. And show how to organize control unit for handling conditional branching.	L3	10M

5

# CBCS SCHEME

USN 

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BEC306C

## Third Semester B.E./B.Tech. Degree Examination, Dec.2023/Jan.2024

### Computer Organization and Architecture

Time: 3 hrs.

Max. Marks: 100

- Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.  
2. M : Marks , L: Bloom's level , C: Course outcomes.*

Module – 1			M	L	C
Q.1	a.	With a neat diagram, explain basic operational concept of computer.	10	L1	CO1
	b.	Explain following with an example : i) Three address instruction ii) Two-address instruction iii) One-address instruction	06	L1	CO1
	c.	Explain Big Endian and Little Endian with neat diagram.	04	L1	CO1

OR

Q.2	a.	Discuss IEEE standard for single precision and double precision floating point numbers with example.	08	L1	CO1
	b.	What is system software? List functions of system software and explain how the processor is shared between user program and os routine.	08	L1	CO1
	c.	Explain computer basic performance equation.	04	L1	CO1

Module – 2

Q.3	a.	What is an addressing mode? Explain any five types of addressing modes with example.	10	L1	CO2
	b.	Write a program to add 'n' number using indirect addressing mode.	05	L2	CO2
	c.	Explain stack operations.	05	L2	CO2

OR

Q.4	a.	What are assembler directives? Explain various assembler directives used in assembly language program.	08	L2	CO2
	b.	Explain subroutine linkage with an example using linkage register.	06	L2	CO2
	c.	Explain the shift and rotate operations with example.	06	L2	CO2

Module – 3

Q.5	a.	Showing register configuration in I/O Interface, Explain program controlled input/output with program.	08	L2	CO2
	b.	Explain the registers involved in DMA interface.	06	L2	CO2
	c.	What is an interrupt? Explain interrupt hardware.	06	L2	CO2

OR

Q.6	a.	Explain the following method of handling interrupts from multiple devices. i) Daisy chain method      ii) Priority structure	08	L2	CO3
	b.	What is Bus arbitration? Explain centralized bus arbitration mechanism with a neat diagram.	08	L2	CO3
	c.	Explain the concept of vectored interrupt.	04	L2	CO3

Module – 4

Q.7	a.	Explain internal organization of 16×8 memory chip.	08	L2	CO4
	b.	With a neat diagram, explain working principle of magnetic disk.	06	L2	CO4
	c.	With a neat diagram, explain virtual memory organization.	06	L2	CO2

OR

Q.8	a.	Explain the internal organization of 2Mx8 DRAM chip with neat diagram.	08	L2	CO3
	b.	Explain a static RAM cell with a neat diagram.	06	L2	CO3
	c.	Discuss the concept of cache memory.	06	L2	CO3

**Module – 5**

<b>Q.9</b>	<b>a.</b>	Explain with neat diagram, Single Bus organization of data path inside a processor.	<b>08</b>	<b>L2</b>	<b>CO4</b>
	<b>b.</b>	Discuss the control sequence for execution of instruction ADD (R3), R1.	<b>06</b>	<b>L2</b>	<b>CO4</b>
	<b>c.</b>	Describe the organization of hardwired control unit.	<b>06</b>	<b>L2</b>	<b>CO4</b>
<b>OR</b>					
<b>Q.10</b>	<b>a.</b>	Explain multiple bus/three bus organization with a neat diagram.	<b>10</b>	<b>L2</b>	<b>CO5</b>
	<b>b.</b>	What is microprogrammed control? Explain its basic organization with suitable diagram and example.	<b>10</b>	<b>L2</b>	<b>CO5</b>

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<b>ANALOG AND DIGITAL SYSTEMS DESIGN LABORATORY</b>		Semester	3
Course Code	<b>BECL305</b>	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		
<b>S.N.</b>	<b>Experiments (All the experiments has to be conducted using discrete components)</b>		
1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.		
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator		
3	Design and set up the circuits using OP-Amp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator		
4	Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod-16		
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor & Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).		
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa		
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.		
8	Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192		
	<b>Demonstration Experiments ( For CIE )</b>		
9	Design and Test the second order Active Filters and plot the frequency response, i) Low pass and Highpass Filter ii) Bandpass and Bandstop Filter		
10	Design and test the following using 555 timer i) Monostable Multivibrator ii) Astable Multivibrator		
11	Design and Test a Regulated Power supply		
12	Design and test an audio amplifier by connecting a microphone input and observe the output using a loud speaker.		

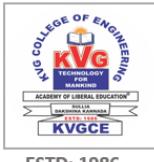
#### **Suggested Learning Resources:**

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual", 5th Edition, 2009, Oxford University Press.
2. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition.

<b>TYPESETTING USING LaTeX</b>		Semester	03
Course Code	BECL358E	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Note: Open-source editors like TeXnikCenter, TeXstudio, Texmaker or any other equivalent editors should be used for creating documents in the Latex environment

S.N.	Experiments																											
1	Create a simple document that consists of 2 sections [Section1, Section2], and a paragraph with dummy text in each section. Also include header [title of document] and footer [institute name, page number] in the document.																											
2	Create a document that displays the sample Abstract/Summary.																											
3	Create a simple title page of the VTU project Report [Use suitable Logos and text formatting].																											
4	Create the Certificate Page of the Report [Use suitable commands to leave the blank spaces for user entry].																											
5	Create a document that contains the following table with proper labels. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">S.No</th> <th rowspan="2">USN</th> <th rowspan="2">Student Name</th> <th colspan="3">Marks</th> </tr> <tr> <th>Subject1</th> <th>Subject2</th> <th>Subject3</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>4XX22XX001</td> <td>Name1</td> <td>89</td> <td>60</td> <td>90</td> </tr> <tr> <td>2</td> <td>4XX22XX002</td> <td>Name2</td> <td>78</td> <td>45</td> <td>98</td> </tr> <tr> <td>3</td> <td>4XX22XX003</td> <td>Name3</td> <td>67</td> <td>55</td> <td>59</td> </tr> </tbody> </table>	S.No	USN	Student Name	Marks			Subject1	Subject2	Subject3	1	4XX22XX001	Name1	89	60	90	2	4XX22XX002	Name2	78	45	98	3	4XX22XX003	Name3	67	55	59
S.No	USN				Student Name	Marks																						
		Subject1	Subject2	Subject3																								
1	4XX22XX001	Name1	89	60	90																							
2	4XX22XX002	Name2	78	45	98																							
3	4XX22XX003	Name3	67	55	59																							
6	Include the side-by-side graphics/pictures/figures in the document by using the subfigure concept.																											
7	Create a document that consists of the following two mathematical equations: $x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$ $= \frac{-2 \pm \sqrt{2^2 - 4*(1)*(-8)}}{2*1}$ $= \frac{-2 \pm \sqrt{4+32}}{2}$ $\varphi_\sigma^\lambda A_t = \sum_{\pi \in C_t} \text{sgn}(\pi) \varphi_\sigma^\lambda \varphi_\pi^\lambda$ $= \sum_{\tau \in C_{\sigma t}} \text{sgn}(\sigma^{-1} \tau \sigma) \varphi_\sigma^\lambda \varphi_{\sigma^{-1} \tau \sigma}^\lambda$ $= A_{\sigma t} \varphi_\sigma^\lambda$																											
8	Demonstrate the presentation of Numbered theorems, definitions, corollaries, and lemmas in the document.																											
9	Create a document that consists of two paragraphs with a minimum of 10 citations in it and display the reference in the section.																											
10	Develop a simple tree diagram or hierarchical structure in the document with appropriate labels using the Tikz library.																											
11	Develop a document to present an algorithm using algorithm/algorithms/algorithms2e library.																											
12	(a) Develop a short technical report by using suitable commands and formats of user choice. (b) Develop an article as per standard format(like IEEE Template)																											
<b>Suggested Learning Resources</b>																												
<ul style="list-style-type: none"> <li>BOOK: A Short Introduction to LaTeX BY FIRUZA KARMALI (AIBARA), A book for beginners, 2019</li> <li>BOOK: Formatting Information: A Beginner's Introduction to Typesetting with LaTeX, BY PETER FLYNN, Comprehensive TeX Archive Network (2005)</li> <li>LaTeX TUTORIAL: [<a href="https://latex-tutorial.com/tutorials/">https://latex-tutorial.com/tutorials/</a>]</li> <li>LaTeX TUTORIAL: [<a href="https://www.javatpoint.com/latex">https://www.javatpoint.com/latex</a>]</li> </ul>																												



ESTD: 1986

# KVG

## COLLEGE OF ENGINEERING

Kurunjibag, Sullia, Dakshina Kannada, Karnataka, INDIA-574 327  
 (Approved by AICTE New Delhi, Affiliated to VTU Belagavi)



www.kvgengg.com

### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**DEPARTMENT VISION:** To create Innovative, Ethical and Sociable Electronics and Communication Engineers

**DEPARTMENT MISSION:**

- ❖ **M1.** Implement Academic Process through University Syllabus and Identified Curriculum Gaps
- ❖ **M2.** Provide platforms for team building, Leadership Skills in the student community through Motivation and Communication.
- ❖ **M3.** Build Ethical and Leadership skills through Interactions with the outside world

### TIMETABLE FOR THE ACADEMIC YEAR 2024-25 (ODD SEMESTER)

**BRANCH/SEM/SECTION:E&CE/III      ROOM NO:LH303      W.E.F:19/08/2024**

TIME DAY	08:55- 09:50	09:50- 10:45	10:45- 11:05	11:05- 12:00	12:00- 01:00	01:00- 02:00	02:00- 02:55	02:55- 03:50	03:50- 04:45	
MON	1L	3L	TEA B R E A K	6L	4L	LUNCH B R E A K	5B3/7A			
TUE	4L	6L		2L	1L		4T	3P	9	
WED	5B1/7B			5B1/7B	3L		1L	2P	8	
THU	6L	1L		4T	2L		5B2			
FRI	3L	2L		6L	4L		12			
SAT	2L	3P		10	13		-	-	-	

1.BMATEC301: AV Mathematics-III for EC Engineering (AKM) 2.BEC302: Digital System Design using Verilog (STJ) 3.BEC303: Electronic Principles and Circuits (SM) 4.BEC304: Network Analysis (DPS) 5.BECL305: Analog and Digital Systems Design Lab(STJ) 6.BEC306C: Computer Organization and Architecture(KSP) 7. BECL358E: Typesetting Using LaTeX (ADS)	8.BSCK307: Social Connect and Responsibility (ADS) 9.BNSK359:BPEK359/BYOK359: NSS/PE/YOGA (STJ) 10. Tutorial Class 11. Remedial Class 12.Association Activity 13. Student Mentoring
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KSP: Dr. Kusumadhara S 9448315022	SM: Dr. Savitha M 9449332086	BHK: Dr. Bhagya H K 8296301700	STJ: Prof. Sathyajith M 8762909060
LPC: Prof. Lokesh P C 9164863489	ADS: Prof. Adarsha D 9731157034	DPS: Prof. Deepthi P S 9611472632	AKM: Prof. Ashritha K M 9483482401

(Prof.LOKESH P C)  
COORDINATOR

(Dr.KUSUMADHARA S)  
H.O.D E&CE

(Dr.PRAJNA M R)  
ACADEMIC DEAN

(Dr.SURESHA V)  
PRINCIPAL

### INSTITUTE VISION:

To be a Notable Engineering College Recognized for Academics, Innovation and the Societal Relevance and Impact of its Pursuits.

### INSTITUTE MISSION:

- ❖ **M1.** Educate our Students Committed to the Service and Ethical Application of Science and Technology.
- ❖ **M2.** Provide Resources to our Faculty and Students to Enhance Engineering Knowledge through Industry - Institute Interactions.
- ❖ **M3.** Practice Diversity and Inclusion amongst our Stakeholders through Rural and Societal Outreach.