CS223 Laboratory Assignment 5

Traffic Light System

Section 1: Mon 08:30-12:20 in EA-Z04
Section 2: Tue 08:30-12:20 in EA-Z04
Section 3: Thu 08:30-12:20 in EA-Z04
Section 4: Mon 13:30-17:20 in EA-Z04
Section 5: Fri 08:30-12:20 in EA-Z04
Section 6: Tue 13:30-17:20 in EA-Z04

Location: EA Z04 (in the EA building, straight ahead past the elevators)
Groups: Each student will do the lab individually. Group size = 1

- # Preliminary Design Report

A number of tasks in today's lab need advanced preparation. You should make your report as neat as possible, with a cover page and pages for the System Verilog codes. If you handwrite anything, it should be neat and legible. You may need a copy of your designs and Verilog programs with you in the lab: to work with, to refer to, to possibly correct and change, to discuss with the TA, to use in debugging.
A cover page that includes the following (in order from the top): course name and code number, the number of the lab, the name and ID number, and the date of you submit the report.
Your report should include your design code, testbench, and also parts a, b, c in the simulation section of the lab manual.

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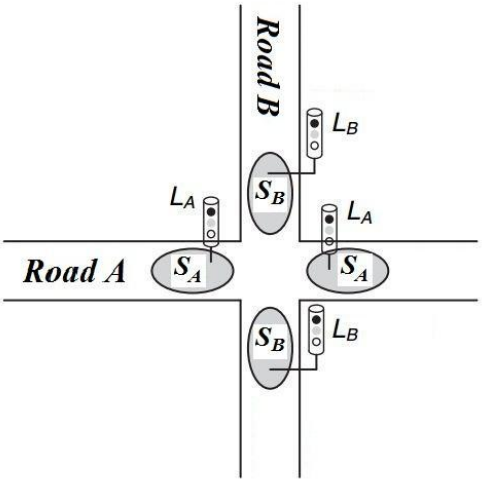
In a community, people need stop signs and traffic lights to slow down drivers from going too fast. If there were no traffic lights or stop signs, people's lives would be in danger from divers going too fast. These devices also play a role in road safety. While accidents still occur at intersections, these crashes may'e been prevented by the drivers yielding to the traffic lights and improving the traffic lights timings. To reduce danger at the intersections, the time for switching red light to green light and green light to red light should be regulated carefully. Studies show if both lights are red for 3 seconds before either light turns green again prevents a huge amount of accidents in traffic.

The traffic light system is similar to the example on pages 124-129 in the textbook. The roads in which intersect are Road A and Road B. There are sensors SA and SB installed in each road to sense the traffic. Each sensor will be TRUE if traffic is present and FALSE if the road is empty. There are two traffic lights LA and LB to control the traffic. The lights may change every 3 seconds depending on the sensors. If a sensor output is TRUE the lights will not change until it is set to FALSE. If a light is green and the sensor is false it will turn yellow and

then red. Both lights will be red for 3 seconds and then the red light will turn yellow for 3 seconds and then turn green.



a) Sketch your improved Moore machine state transition diagram, state encodings, state transition table, output table, next state, and output equations, and your Finite State Machine schematic.
b) How many flip-flops do you need to implement this problem?
c) Redesign your outputs using decoders.

- # Simulation

Enter Verilog module to Xilinx ISE software and select simulation mode. Prepare a testbench using the Verilog Test Fixture of the ISE software. In the simulation, try all possible variations through SA and SB sensors and observe the LA and LB traffic lights.

- # Implementation on FPGA

In this part, you are going to implement your code on FPGA.

1) Slow down the clock to 3 seconds to see the change in the lights.

2) Use LEDs on the BASYS board for outputs of LA and LB traffic lights.
Red : *** (three leds)
Green: ** (two leds)
Yellow: * (one led)

3) The SA and SB sensors will be two left-most buttons. The sensor will be active when as long as the button is set to 1.

Now test your code and show the result to your TA.

Cleanup!

Clean up your lab station, and return all the parts, etc. Throw away any parts that do not work. Save your project on a flash memory stick. Delete the Xilinx Project you created and any files you created today so that the computer is in the same state that you found it. Now turn off the computer, and leave your lab workstation for others the way you would like to find it—clean and organized.