Bilkent University

Department of Computer Science

CS 224

# Preliminary Work

# Lab 6

# Section 2

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Date of the lab: 27th of April, Wednesday, 13:30 – 17:20

**Part 1**

**1.)**

| No. | Cache Size KB | N way Cache | Word Size (no. of bits) | Block Size (no. of words) | No. of Sets | Tag Size in bits | Index Size (Set no.) in bits | Block Offset size in bits[1] | Byte Offset size in bits[2] | Block Replacement Policy Needed (Yes/No) |
|---|---|---|---|---|---|---|---|---|---|---|
| **1** | 64 | 1 | 32 | 4 | $2^{12}$ | **15** | **12** | **2** | **2** | **No** |
| **2** | 64 | 2 | 32 | 4 | $2^{11}$ | **16** | **11** | **2** | **2** | **Yes** |
| **3** | 64 | 4 | 32 | 8 | $2^{9}$ | **17** | **9** | **3** | **2** | **Yes** |
| **4** | 64 | Full | 32 | 8 | $2^{0}$ | **26** | **0** | **3** | **2** | **Yes** |
| **9** | 128 | 1 | 16 | 4 | $2^{14}$ | **14** | **14** | **2** | **1** | **No** |
| **10** | 128 | 2 | 16 | 4 | $2^{13}$ | **15** | **13** | **2** | **1** | **Yes** |
| **11** | 128 | 4 | 16 | 16 | $2^{10}$ | **16** | **10** | **4** | **1** | **Yes** |
| **12** | 128 | Full | 16 | 16 | $2^{0}$ | **26** | **0** | **4** | **1** | **Yes** |

**2.)**

**a.)**

| Instruction | Iteration No. | | | | |
|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** |
| **lw $t1, 0x24($0)** | **Compulsory Miss** | **Conflict** | **Conflict** | **Conflict** | **Conflict** |
| **lw $t2, 0xAC($0)** | **Compulsory Miss** | **Conflict** | **Conflict** | **Conflict** | **Conflict** |
| **lw $t3, 0xC8($0)** | **Compulsory Miss** | **Conflict** | **Conflict** | **Conflict** | **Conflict** |

**b.)**

As block size is 4 words, 2 bits are needed for block offset.

Set bits are only 1 bit and byte offset are 2 bits. So, target is 27 bits.

Total Bits: (1 * 2 + 27 * 2 + 8 * 32) * 2 = **624 bits**

**c.)**

**1** 8:1 MULTIPLEXER

**2** EQUALITY COMPARATORS

**2** AND gates

**1** OR gate

**3.)**

**a.)**

| Instruction | Iteration No. | | | | |
|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** |
| **lw $t1, 0x24($0)** | **Compulsory Miss** | **Capacity** | **Capacity** | **Capacity** | **Capacity** |
| **lw $t2, 0xAC($0)** | **Compulsory Miss** | **Capacity** | **Capacity** | **Capacity** | **Capacity** |
| **lw $t3, 0xC8($0)** | **Capacity** | **Capacity** | **Capacity** | **Capacity** | **Capacity** |

**b.)**

**Set:** 0 bits

**Block offset:** 0 bits

**Target:** 30 bits

**Total Bits:** 2 * (1 + 30 + 32) + 1 = **127 bits (1 bit for U bit in LRU Calculation)**

**c.)**

**1** 2:1 MULTIPLEXER

**2** EQUALITY COMPARATORS

**2** AND gates

**1** OR gate

**4.)**

L1: 2 Clock Cycles

L2: 4 Clock Cycles

MM: 20 Clock Cycles

$AMAT = t_{L1} + MR_{L1}(t_{L2} + MR_{L2} * t_{MM})$

AMAT = 2 + 0.1 * (4 + 0.05 * 20) = **2.5 clock cycles**

Clock rate of 2Hz means clock period of 0.5 ns

**Required Time** = $0.5 * 2.5 * 10^{10}$ = **12.5 s**