TI Designs

Hall-Effect Proximity Sensor with PNP or NPN Output

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00244	Design Folder
TIDA-00188	Design Folder
MSP430FR5969	Product Folder
DRV5013	Product Folder
SN65HVD101	Product Folder
SN65HVS882	Product Folder

TI E2E™ Community

ASK Our Analog Experts

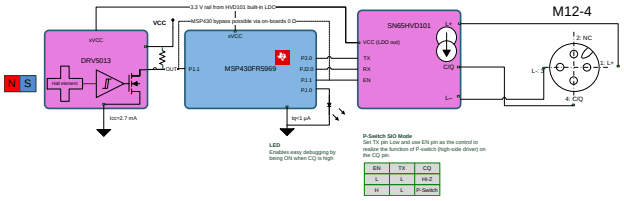
WEBENCH® Calculator Tools

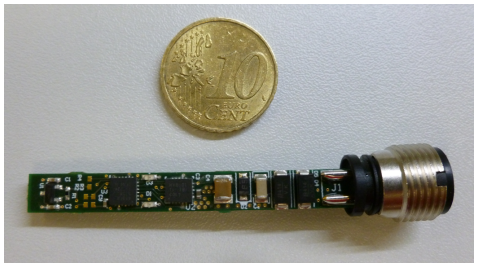
Design Features

- Hall-Effect Latch Sensor with PNP or NPN Transmitter
- Hall-Effect Latch Sensors Offer Superior Stability of the Proximity Detection
- Hall-Effect Latch Sensors are Perfectly Suited to SIO Transmitter Interfaces
- MSP430-Based Solution for Easy IO-Link Upgrade (see TIDA-00188)

Featured Applications

- Factory Automation and Process Control
- Building Automation
- Sensors and Field Transmitters
- Portable Instrumentation





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

1.1 Introduction to SIO and Hall-Effect Sensing

CAUTION

To facilitate a grounds-up solicit input/output (SIO) sub-system project, this section provides a quick overview of the SIO interface. Do not under any conditions consider this document a reference, and only the reference documents should be used once passed the initial phase of the project.

1.1.1 SIO (IEC 61131-2)

SIO is the industry name for the standard IEC61131-2 [1]. This standard has been since enhanced by IEC61131-9 [2] that defines single-drop digital communication interface mode (SDCI).

The IEC61131-2 proximity switch is defined by switching characteristics clearly defining zones with current and voltage related to a *ON* state and zones defined as *OFF* states as well as clearing the guard band between those two zones to avoid possible confusions (see Figure 1).

For more details on the input stage for SIO, please refer to [2].

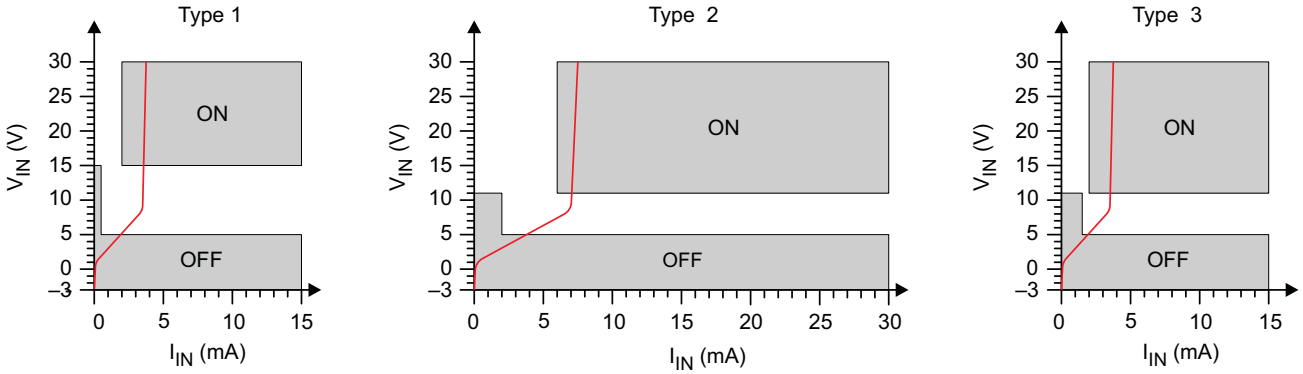


Figure 1. Switching Characteristics for IEC61131-2 Type 1, 2, and 3 Proximity Switches

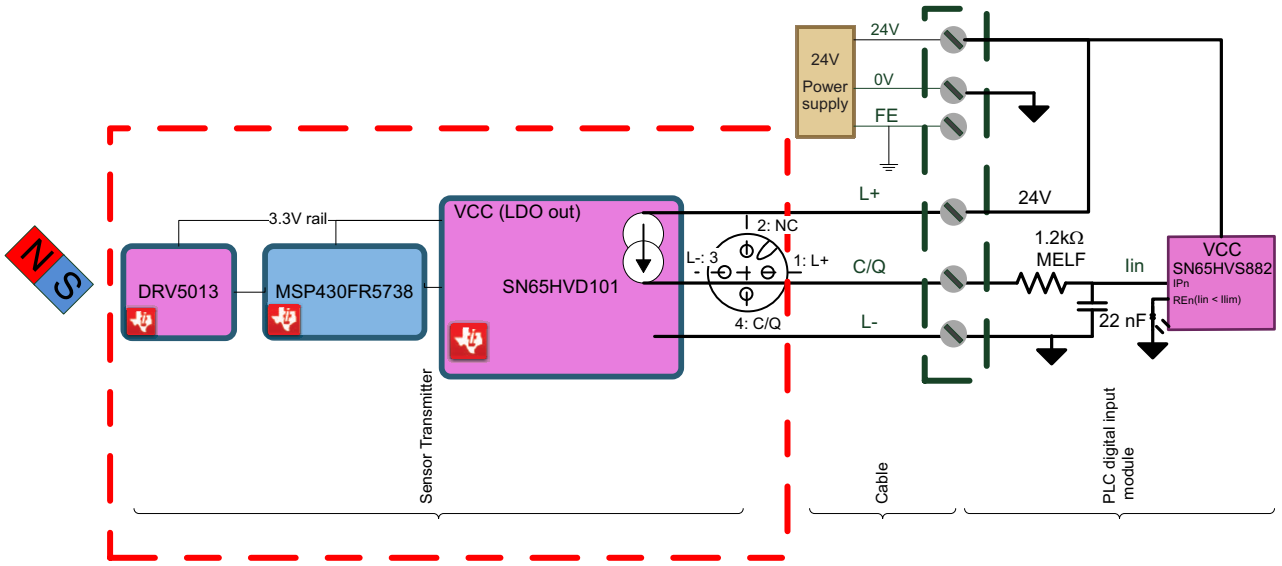


Figure 2. Total System Including Transmitter and PLC Digital Input

1.1.2 Hall-Effect Sensors

Hall-effect sensing is a sensing technology that detects the presence of a magnetic field. This technology is mainly used to sense position, speed, and acceleration.

The output is linear depending on the magnetic flux, but normally the flux is not proportional to the distance, which is why Figure 3 looks like 1/x.

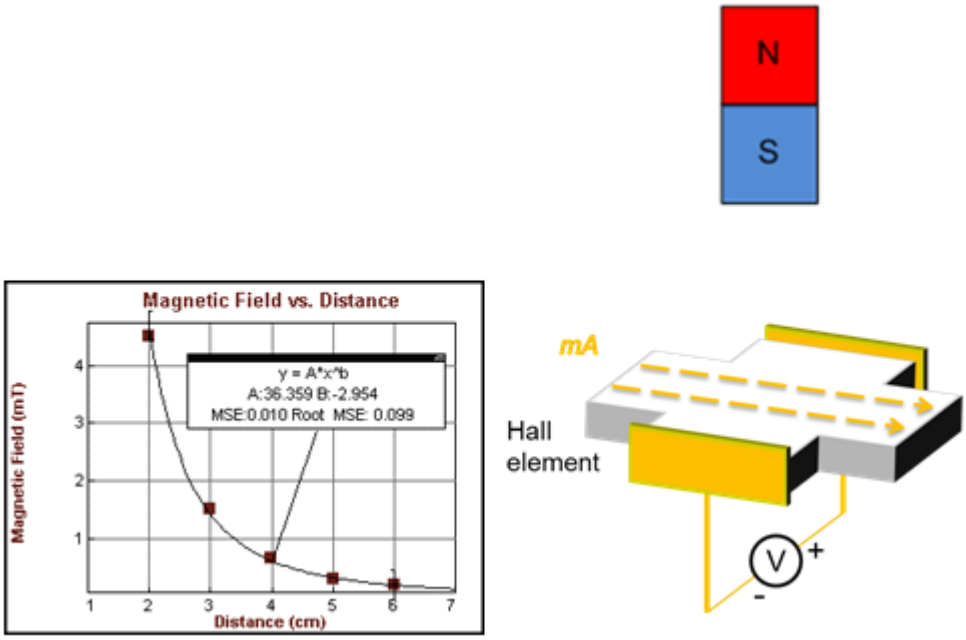


Figure 3. Hall-Effect Sensing Illustrated

1.1.2.1 Common Terminology and Conventions Used

- Standard convention to indicate polarity
  - North pole: denoted by a negative magnetic field
  - South pole: denoted by a positive magnetic field

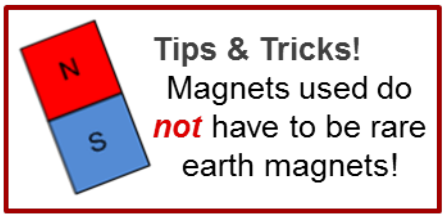


Figure 4. Magnets Tips and Tricks 1

- B_{OP}: Magnetic field (“B” field) operate point, as B field increases, B_{OP} is the threshold when the output goes Low-Z
- B_{RP}: Magnetic field (“B” field) release point, as B field decreases, B_{RP} is the threshold when the output goes High-Z. B_{RP} is of opposite leading sign (main difference between latch and switch)
- B_{HYS}: Magnetic field hysteresis = $B_{OP} – B_{RP}$
  - Prevents magnetic-field noise from accidentally tripping the output between B_{OP} and B_{RP}

- B_O: Magnetic field offset = (B_{OP} – B_{RP}) / 2
  - The center point of thresholds
  - Another parameter / equation used to define hysteresis of the sensor
- Linear sensitivity: The voltage gain per magnetic field strength, in mV/mT
- Zero magnetic field outputs V_Q, the quiescent voltage output
- Magnetic (B) field sensitivity:
  - Parameters used for digital Hall-effect sensors: B_{OP} and B_{RP}
  - Parameter used for analog Hall-effect sensors: mV/mT – Magnetic field strength is affected by
    - Shape, magnetization, and composition of the magnetic object
    - Distance from object to Hall-effect sensor

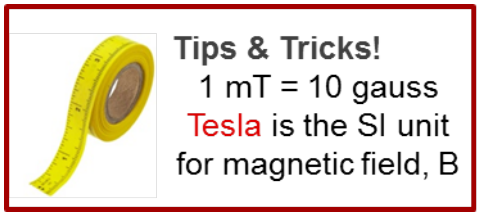


Figure 5. Magnets Tips and Tricks 2

- Higher sensitivity corresponds to a lower number:
  - For example, a 3-mT B_{OP} sensor is more sensitive than a 150-mT B_{OP} sensor
  - A 3-mT Hall-effect sensor will hit its trip point much sooner than the 150-mT Hall-effect sensor as a magnet is brought closer to the sensor
- Required sensitivity depends on the design
  - Highly sensitive Hall-effect sensors can sometimes help to cut down system cost, allowing designs to use cheaper (lower strength) magnets
  - To prevent magnetic-field noise from potentially tripping the sensor sooner than required, some applications require less sensitive Hall-effect sensors in its design

1.1.2.2 Hall-Effect Sensor Sensitive Axis Different Usage

Head-on sensing is the most usual way to test a Hall-effect sensor transmitter. It involves taking a permanent magnet and bringing a pole up to the sensing part to activate it. Usually in a head-on operation, the sensitive axis of the Hall-effect sensor is parallel to the axis of the magnet.

If the field strength was plotted over the distance (airgap), in what is often referred to as a flux map, one would have a rapidly decreasing curve as the distance increases.

Slide-by sensing is another way to use Hall-effect sensor transmitter. In this configuration, the magnet north-south axis and the sensitive axis of the Hall-effect sensors are parallel but the magnet is moving in a plane orthogonal to that axis. This system can be particularly useful to detect when a system is passing it is out of range position. When the Hall-effect sensor detects the maximum field, it should trigger a system notification that a moving part moved out of the designated area.

While both head-on and slide-by sensing provide relative information, some systems will need absolute information in which case null-point sensing is used. For this, one has to think of the Hall-effect sensor being equally distanced from the south and north pole of the magnet. When equally distanced it will see a “zero field” and as soon as the magnet moves, one pole will get closer to the Hall-effect sensor and the other pole will move away, creating a resulting field either positive or negative.

1.1.2.3 Hall-Effect Sensor Sensitive Usage

While Hall-effect sensing now has a broad range of usage in the industry, the goal of this section is to illustrate a few usual applications for engineers needing to design such systems for a first time.

Figure 6 is an example of a float sensing through a ring magnet, when the float part where the hall-sensor is mounted is in the middle of the ring magnet, the flux will be nill, which allows to detect very accurately a level.

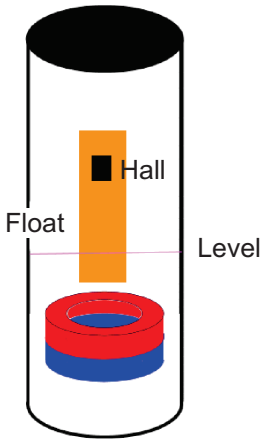


Figure 6. Float Sensing Through a Ring Magnet

Figure 7 is an example of linear sensing, when the hall sensor that moves along the axis d is inside the magnets it will see a null field.

Figure 8 is an example of angle sensing.

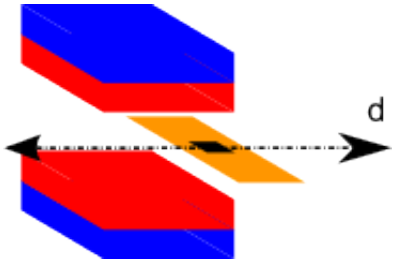


Figure 7. Example of Linear Sensing

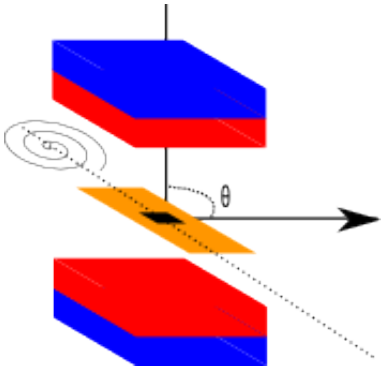
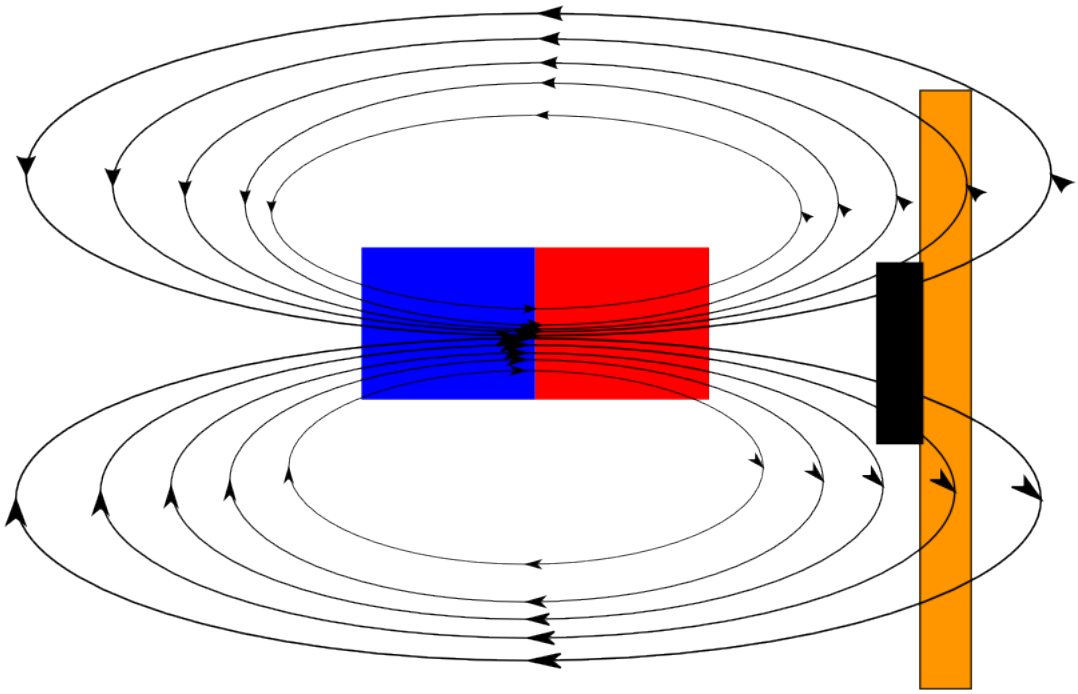


Figure 8. Example of Angle Sensing

Figure 9 are examples of proximity sensing of a metal obstacle based on hall-sensing. When there is no metal obstacle (top diagram), the hall sensor will “see” the field and output a voltage accordingly. When there is a metal obstacle (bottom diagram), the field will be concentrated in the metal and the hall sensor will not see the field any longer.



no metal obstacle, hall sensors sees the field

metal obstacle, hall sensors does not see the field

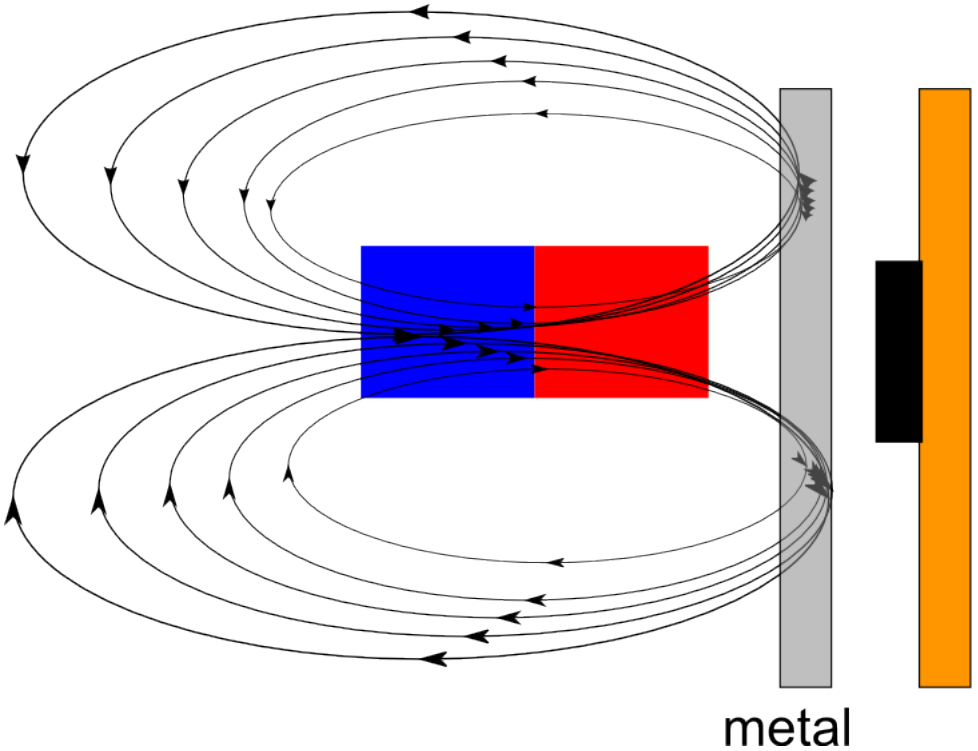


Figure 9. Metal Obstacle Detection

1.1.2.4 Physics of Hall-Effect Sensors

NOTE: Temperature coefficients: TI Hall-effect sensor all have temperature compensation so are far less sensitive to temperature effects than physics would make the raw sensor.

Hall-effect sensors have a slight temperature dependency which could create measurement artefact over a broad range of temperature. The consequence is often mentioned in % change in sensitivity per kelvin (K).

1.2 System Overview

The system provides a hall-sensor IC which then can drive the SIO level via the MSP430 or directly the SN65HVD101 (via 0 ohm resistors options on the PCB).

The system also provides button to allow an easy upgrade of the hall-sensor for linear based hall sensor to set the threshold by the users. Also, the LED on the board allow easy debug by providing a visual mirror of the CQ line.

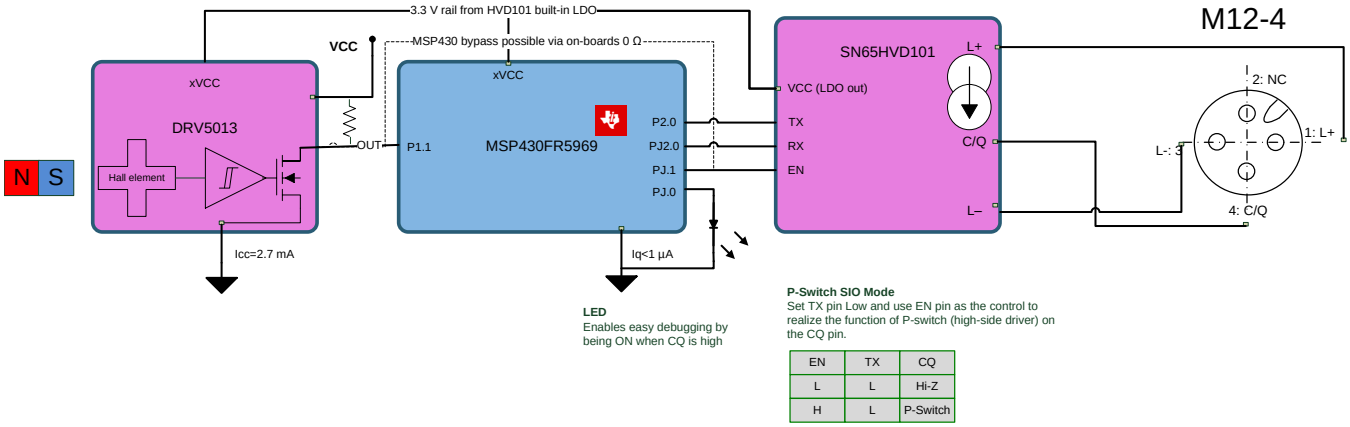


Figure 10. Hall-Effect Proximity Sensing with SIO Transmitter Interface Subsystem Overview (System Block Diagram)

1.3 Possible Variants

1.3.1 IO-Link Capability

The design was intended to enable an easy transition between SIO and IO-Link. For this reason, the similarities with TIDA-00188 were maximized to enable easy porting of the IO-Link stack to TIDA-00244.

1.3.2 SIO Transmitter and Hall-Effect Only

The TI Design has an option to bypass the MSP430 and control the state of the C/Q line directly from the Hall-Effect Sensor.

2 Design Features

2.1 Hardware

For an IEC61131-2 proximity sensor, the current source capability of the output stage should be large enough to be compatible with a broad range of digital inputs.

Assuming a 3.6mA current input limit on the digital input (Ilim) and a typical 1.2 kΩ, the switching voltage should be for a type 3 (most frequent type of sensor based on semiconductor), compatible with Figure 1. Given the SN65HVD101 VRQL parameter being a voltage drop of 2V maximum for VCC of 18V and more, then the digital input VINmin of 11V is met.

2.1.1 Hall-Effect Sensing System Considerations

Unlike a purely electro-mechanical system, Hall-effect sensing projects require taking into consideration the three major sources of variability to achieve a capable design achieving its target peak to peak performance distribution within the desired range:

- The characteristics of the magnetic materials and lot to lot distribution of the magnets used in the final system
- The magnetic parameters of the sensor IC (provided by Texas Instruments Hall-effect sensing data sheets and integrated in an electronics system by electronics engineering)
- Mechanical tolerance (provided by the mechanical engineering)

While electronics and mechanical tolerances can be fairly well documented, it is reported that the majority of data sheets for magnetic materials may not provide upper and lower limits for many critical parameters nor variations over temperature [4].

2.1.2 Magnetic Field Calculator

2.1.2.1 Theoretical Field Calculator

The magnetic field around an infinitely long, straight conductor, carrying a current I at a radius of r is given by:

$$B = \frac{\mu_0 I}{2\pi r}$$

The magnetic field at the center of a closed circular loop of wire of radius r carrying a current of I is given by:

$$B = \frac{\mu_0 I}{2r}$$

2.1.2.2 Online Field Calculator

Refer to http://www.dextermag.com/resource-center/magnetic-field-calculators.

2.2 Software

Selection of MCU enables configuration over IO-Link (even though the present project does not focus on this, for IO-Link refer to TIDA-00188) for rapid prototyping, but also enables usage from Texas Instruments other Hall-effect sensors and possible set-up of thresholds for switching the transmitter output.

2.3 Power and Protection Design

The IO-Link device design is powered off the IO-Link interface by way of the L+ (24-V nominal) and L- (GND) terminals. According to the IO-Link interface and system specification [2], an IO-Link device must be able to operate with a supply voltage ranging from 18 V to 30 V.

The IO-Link PHY SN65HVD101 (U2) used in the design operates with supply voltages from 9 V to 30 V, providing a lot of margin compared to 18 to 30 V. The IO-Link PHY SN65HVD101 integrates a linear voltage regulator powering internal parts of the PHY itself. The linear voltage regular also powers the MSP430 (U3) device and the ADS1220 (U1) device. The linear regulator is set-up to provide a 3.3-V rail (VCC) on its VCCOUT-terminal by grounding the VCCSET-terminal (terminal 1 of U2).

The IO-Link PHY (U2) provides three indicator outputs (PWR_OK, CUR_OK, and TEMP_OK) which signal fault conditions of the power supply (undervoltage condition of VCC or L+). The three indicator outputs also signal overcurrent in or out of the CQ-pin. The three indicator outputs also signal over-temperature of the die by driving the respective terminals to a logic LOW state, while the outputs have a high impedance under normal operating conditions. The indicator output signals are fed into the MSP430 (U3) device.

The L+ and CQ pins of the SN65HVD101 device offer a ±40-V absolute maximum steady voltage rating, which is furthermore extended to ±50 V for transients with pulse width less than 100 µs.

The IO-Link PHY (U2) margin and the ability of the PHY to withstand even negative voltages ease the design because of the robustness of the solution against ESD and Burst and Surges as defined in the Standards IEC 61000-4-2, IEC 6100-4-4, and IEC 6100-4-5.

The design uses an additional transient protection circuitry consisting of the TVS diodes (D6, D7, D8) and bypass capacitors C10, C12 and C13 to be in compliance with Standards IEC 61000-4-2, IEC 6100-4-4, and IEC 6100-4-5.

The IO-Link specification does not require a surge transient test (IEC61000-4-5) because of the limitation of maximum cable length to 20 meters. However, the use of the design in applications using digital input or output and with cable lengths exceeding 30 m requires surge testing. The design uses the assumption that the surge test is the most severe of the three transient test cases. The design also uses the assumption that the surge test is the test with the highest energy level. Therefore, special care was used in selecting the right transient voltage suppressor (TVS) as a clamping device.

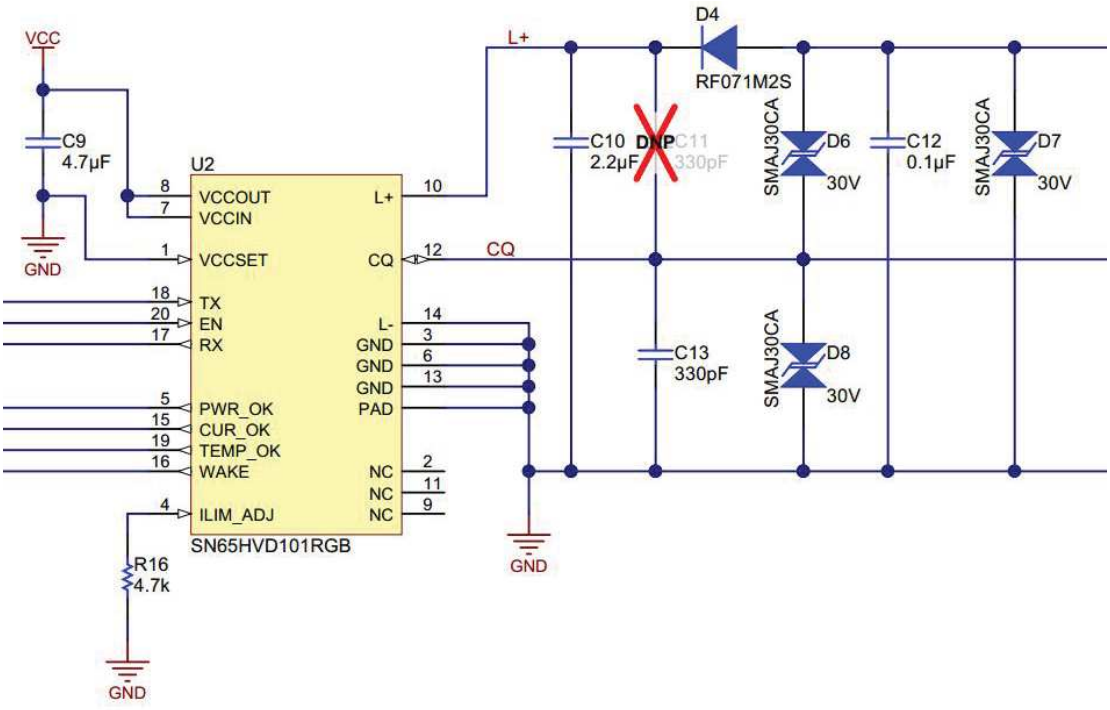


Figure 11. Power and Data Interface with Protection Circuitry

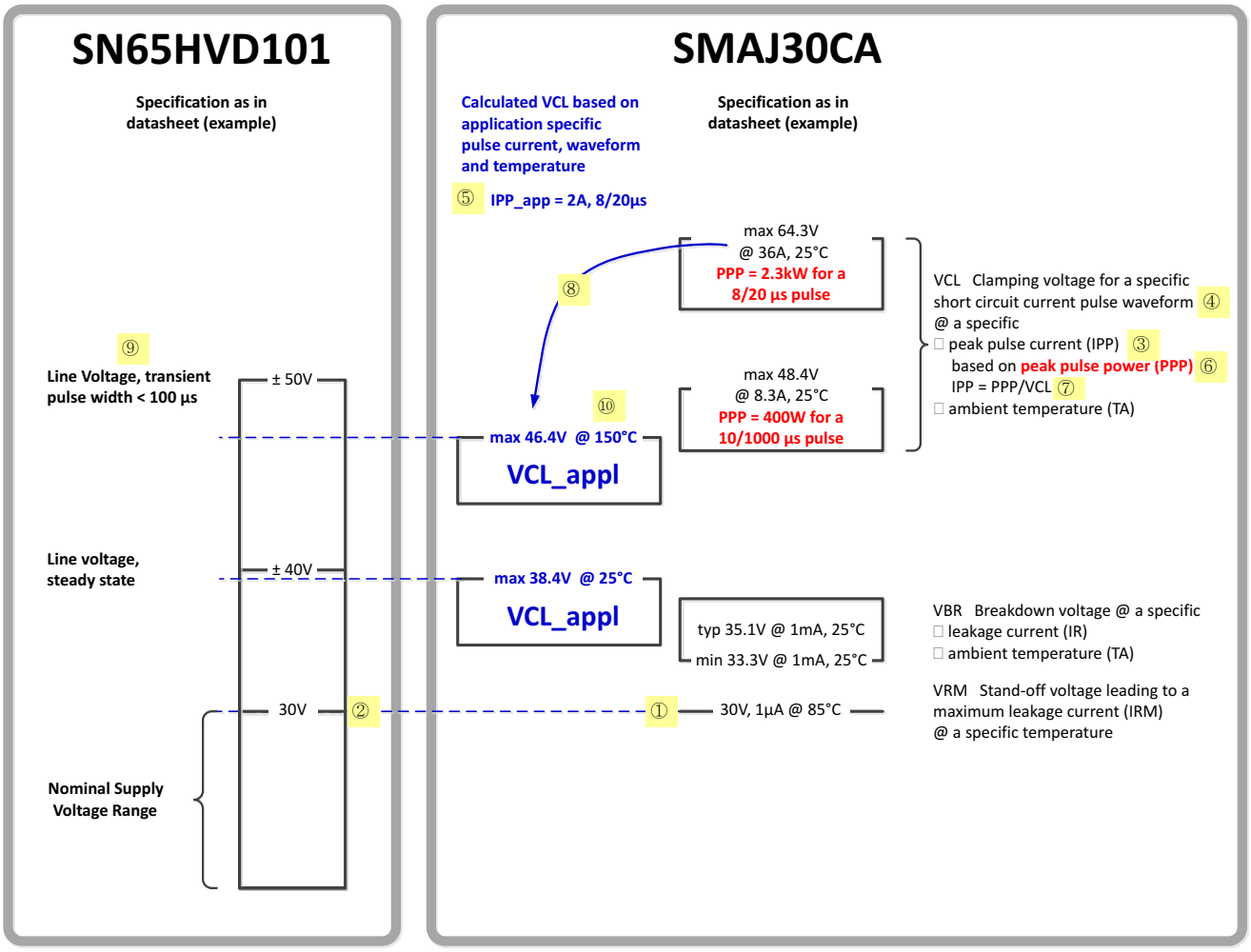


Figure 12. SN65HVD101 Device and SMAJ30CA Device

In order to choose TVS Diodes appropriately, three requirements must be satisfied:

1. VRM, the TVS' stand-off voltage ① (the voltage when the TVS does not conduct) must be greater than or equal to the transceiver's maximum signal and supply voltage of 30 V ② to prevent the TVS from conducting during normal operation.
2. IPP, the TVS' peak pulse current ③ at the short circuit pulse waveform ④ must be greater than the application-specific peak pulse current IPP_app ⑤. The open circuit voltage of the combination wave generator (surge generator) and the impedance of the generator and the coupling device determines the application-specific peak pulse current IPP_app ⑤. Most TVS' specify the IPP for a 10/1000 µs pulse only. However, the pulse used for the surge test is mostly an 8/20 µs pulse. In this case, the pulse rating curve in the datasheet can be used to derive the peak pulse power PPP ⑥ for a specific pulse width of 20 µs. IPP can then be derived ⑦ by dividing the PPP by the estimated clamping voltage VCL at this IPP level. The VCL for an 8/20 µs pulse will be much larger than the VCL for the 10/1000 µs pulse. It is recommended to contact the TVS manufacturer when estimated values are used unless there is a large margin between IPP and IPP_app.
3. When the TVS conducts and becomes low-impedance to shunt the surge current to ground, the TVS' application-specific clamping voltage VCL_appl ⑧ must be lower than the transceiver's maximum transient stand-off voltage ⑨ of ±50 V. To obtain the application specific clamping voltage, the TVS' VCL needs to be reduced according to the reduction of the TVS' IPP to the application specific IPP_app. Some data sheets provide the differential resistance for the specific pulse waveform, which helps greatly to determine the reduction of the TVS' IPP to the application specific IPP_app. If differential resistance for the specific pulse waveform is not supplied and if there is not enough margin, the TVS manufacturer should be contacted. The VBR and VCL voltages in the TVS' data sheets are often given for an ambient temperature of 25°C only. Because those voltages usually have a positive temperature coefficient, the VCL values need to be corrected accordingly to ensure that requirement 3. is fulfilled even at the maximum ambient temperature of the application specific case and under the conditions of multiple repetitive surges which heat up ⑩ the TVS. The temperature coefficient is given in most data sheets.

For the special case of this small size IO-Link device design, a 1.2 µs/50 µs 1 kV pulse applied by way of a 500 Ω impedance has been considered according to IEC 60255-5. The resulting peak current through the clamping device (TVS) is then roughly 1 kV / 500 Ω = 2 A . The SMAJ30CA device is a bidirectional TVS and fulfills the above mentioned requirements by clamping voltages with both polarities. The SMAJ30CA device has a stand-off voltage VRM of 30 V, a minimum breakdown voltage VBR of 33.3 V, and an application specific clamping voltage of roughly 46.3 V at the 2-A current level and at a junction temperature of 150°C.

In case of other end applications, the more severe requirements of IEC61000-4-5 (using coupling impedances of 40 Ω + 2 Ω) may be applicable. The open circuit voltage of this surge pulse has the same 1.2 µs/50 µs double exponential waveform, resulting in an 8/20 µs short circuit current shape of the combination wave generator used in this test. The reduced 40 Ω + 2 Ω coupling impedance (compared to the 500 Ω) increases the peak current at a 1 kV surge level to roughly 1 kV / 42 Ω = 23.8 A.

D4 provides an additional level of reverse polarity protection. While the SN65HVD101 device can withstand negative voltages up to –40 V (in steady state) and up to –50 V (transient) as expressed previously, the diode avoids the supply voltage bypass capacitor C10 being discharged during a negative pulse. The diode enables that the design will recover much faster from such a negative surge event.

3 Block Diagram

3.1 Hardware

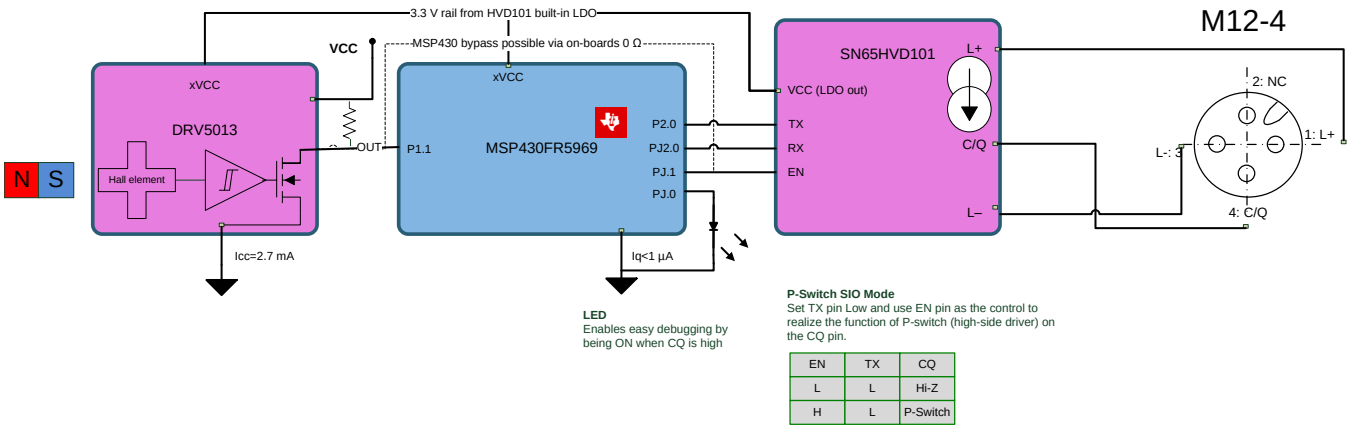


Figure 13. System Block Diagram

3.2 Software

The software is simplified to initialize the hardware and scan the input of the MSP430 from the Hall sensor to update the C/Q line.

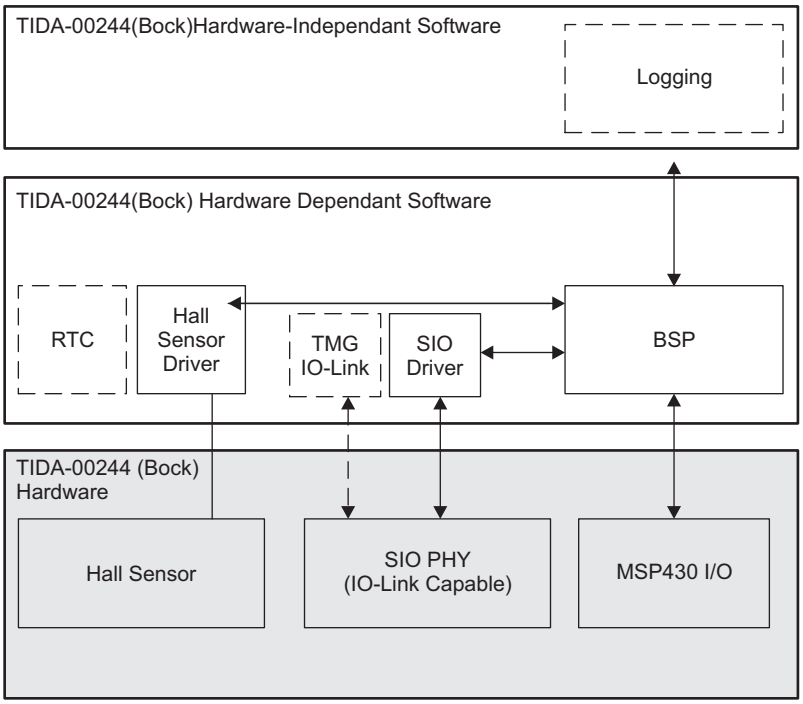


Figure 14. TIDA-00244 Software Architecture

4 Circuit Design and Component Selection

4.1 SN65HVD101

SN65HVD101 Key Features

- Configurable CQ Output: Push-Pull, High-Side, or Low-Side for SIO Mode
- Remote Wake-Up Indicator
- Current Limit Indicator
- Power-Good Indicator
- Over-temperature Protection
- Reverse Polarity Protection
- Configurable Current Limits
- 9-V to 36-V Supply Range
- Tolerant to 50-V Peak Line Voltage
- 3.3-V/5-V Configurable Integrated LDO
- 20-pin QFN Package, 4 mm × 3.5 mm

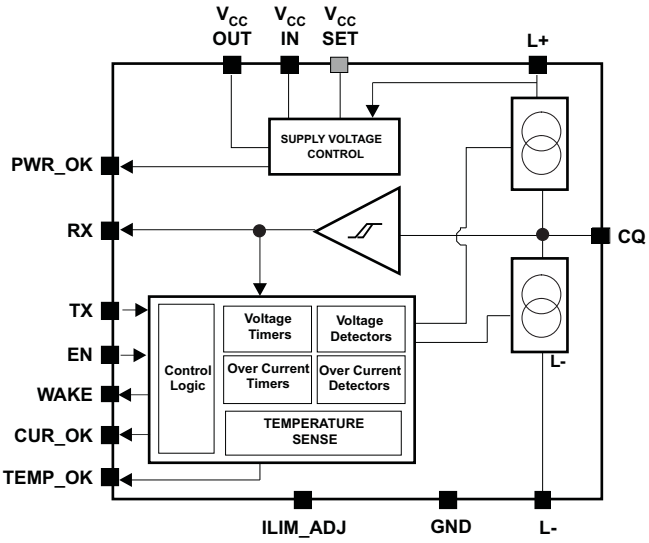


Figure 15. SN65HVD101 (SIO PHY for Device Nodes) Block Diagram

4.2 MSP430FR5738

MSP430FR5738 key features:

- Embedded MCU 16-b RISC Architecture up to 24-MHz clock
- Wide supply voltage range (2 to 3.6 V)
- Optimized ultra low-power modes (81.4 µA / MHz in active and 320 nA in Shutdown (LPM4.5))
- Ultra low-power Ferroelectric RAM
- 16-KB Nonvolatile Memory
- Ultra low-power Writes
- Fast Write at 125 ns per Word (16 KB in 1 ms)
- Built in Error Coding and Correction (ECC) and MPU
- Universal Memory = Program + Data + Storage
- 1015 Write Cycle Endurance
- Intelligent Digital Peripherals
- 32-b Hardware multiplier (MPY)
- Channel internal DMA
- RTC with calendar and alarm functions
- 16-Bit Cyclic Redundancy Checker (CRC)
- High-Performance Analog
- Enhanced Serial Communication

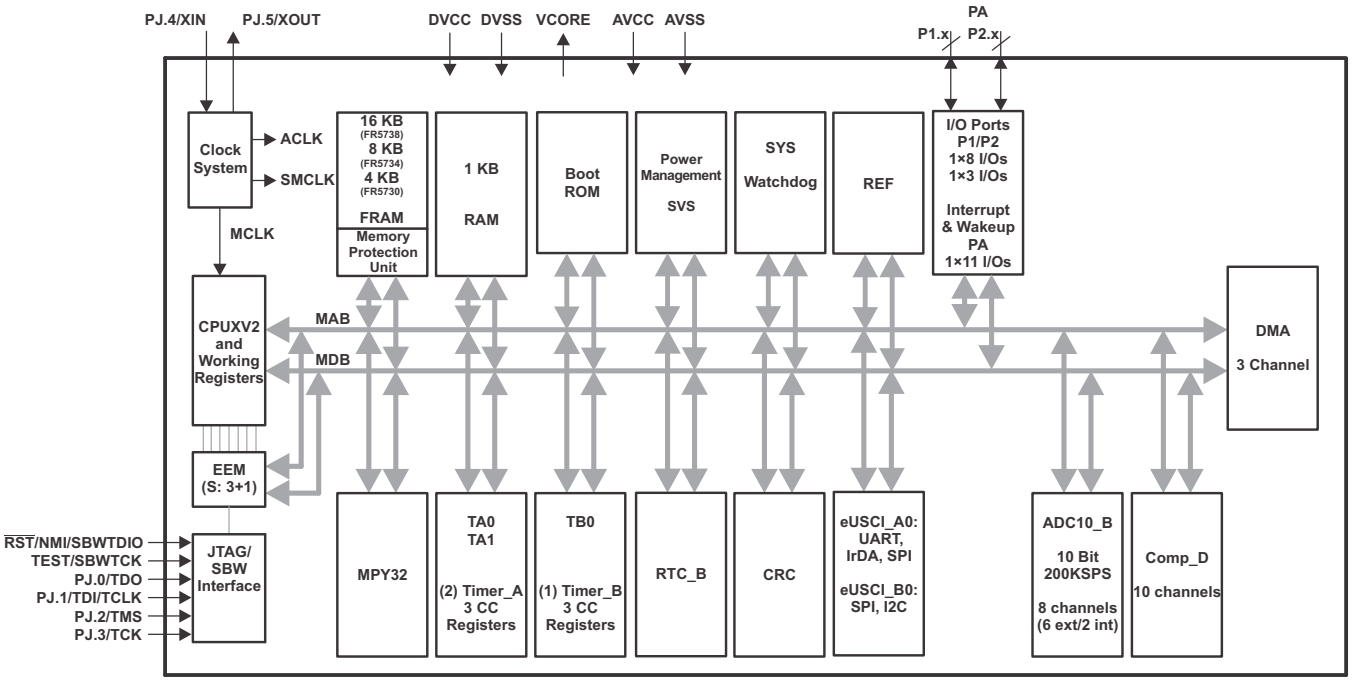


Figure 16. MSP430FR5738 Block Diagram

4.3 DRV5013

DRV5013 key features:

- Digital Bipolar-Latch Hall Sensor
- Superior Temperature Stability
  - B_{OP} ±10% Over Temperature
  - High Sensitivity Options (B_{OP} and B_{RP})
    - ±2.3 mT
    - ±4.6 mT
    - ±9.2 mT
  - Supports a Wide Voltage Range
    - 2.5 to 38 V
  - Operation from Unregulated Supply
  - Wide Operating Temperature Range
    - TA = –40°C to 125°C
  - Open Drain Output
    - Up to 30-mA Current Sink
  - Fast Power-On
    - 35 µs
  - Small Package and Footprint
    - Surface Mount 3-Terminal SOT-23 (DBZ)
    - 2,92 × 2,37 mm
  - Through-Hole 3-Terminal SIP (LPG)
    - 4 × 3.15 mm
  - Protection Features
    - Reverse Supply Protection (up to –22 V)
    - Supports up to 40-V Load Dump
    - Output Short-Circuit Protection
    - Output Current Limitation

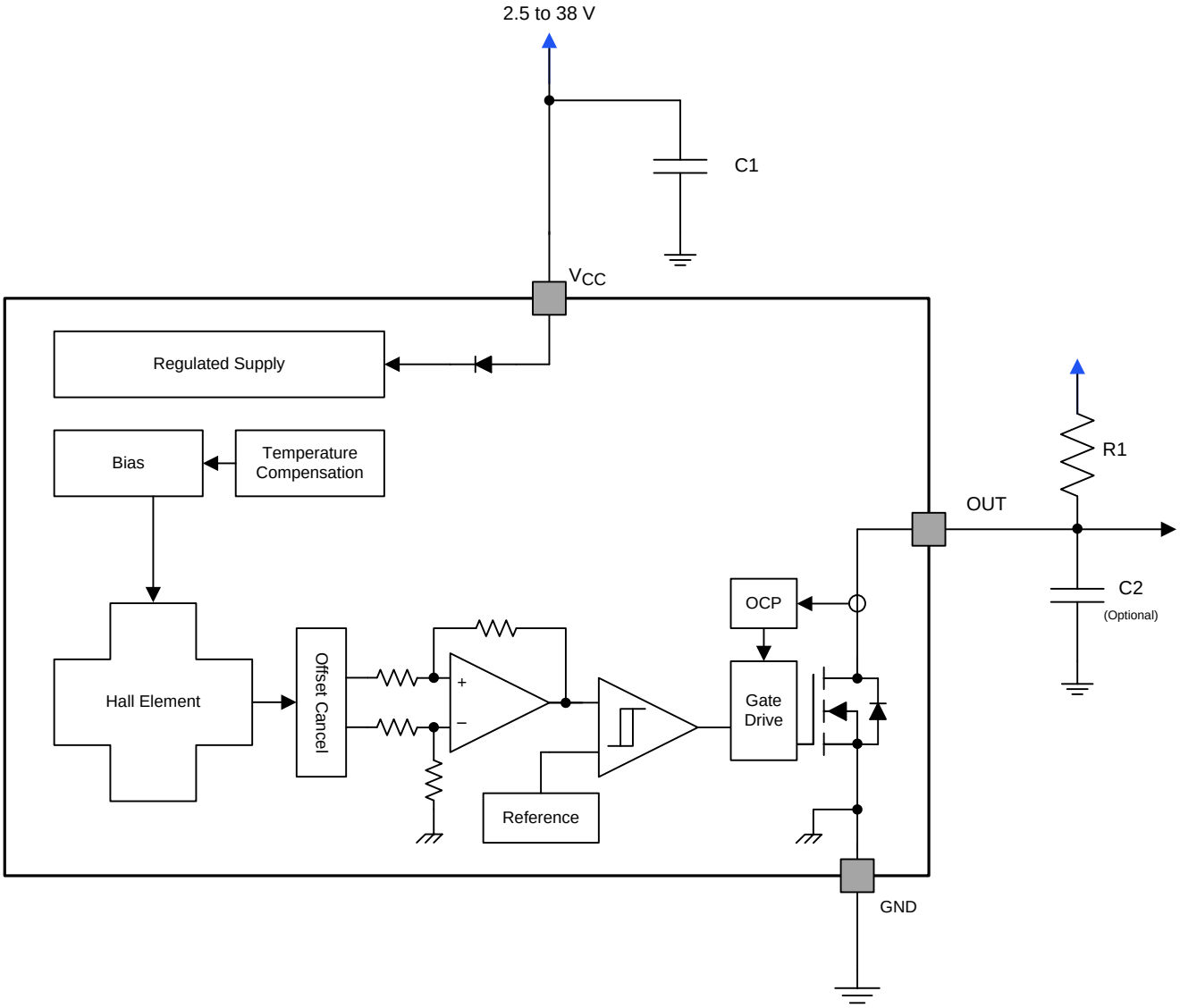


Figure 17. DRV5013 Block Diagram

5 Software Description

This code is designed to implement a proximity transmitter application using the DRV5103 to receive data from magnet proximity and send out status latch reading on an SIO signal using the SN65HVD101.

5.1 Doxygen Documentation

5.1.1 File List

Here is a list of all files with brief descriptions:

[installation folder]/tida-00244_HALL_SIO/src/BSP.c

[installation folder]/tida-00244_HALL_SIO/src/bsp.h

[installation folder]/tida-00244_HALL_SIO/src/main.c

5.1.2 File Documentation

[installation folder]/tida-00244_HALL_SIO/src/BSP.c File Reference

5.1.3 Functions

- **void BSP_Init_TIDA00244 ()**
  Will provide all the hardware initialization, see **BSP.h** for supported hardware platforms.
- **void BSP_Init (void)**

5.1.4 Function Documentation

void BSP_Init (void)

Definition at line 58 of file BSP.c.

Here is the call graph for this function:

5.1.5 void BSP_Init_TIDA00244 ()

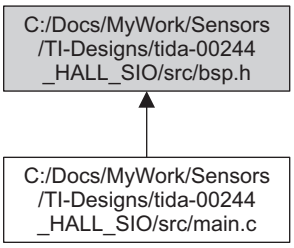
Will provide all the hardware initialization, see **BSP.h** for supported hardware platforms. It should be noted that while multiple hardware configuration may be supported, only TIDA-00244 will be used for validation. Mileage on other configuration may vary!

Definition at line 48 of file BSP.c.

Here is the caller graph for this function:

5.2 [installation folder]/tida-00244_HALL_SIO/src/bsp.h File Reference

This illustration shows which files directly or indirectly include this file:



5.2.1 Macros

#define **TIDA00244**

5.2.2 Functions

- **void BSP_Init_TIDA00244 ()**
  Will provide all the hardware initialization, see **BSP.h** for supported hardware platforms.
- **void BSP_Init (void)**

5.2.3 Macro Definition Documentation

#define TIDA00244

Definition at line 45 of file bsp.h.

5.2.4 Function Documentation

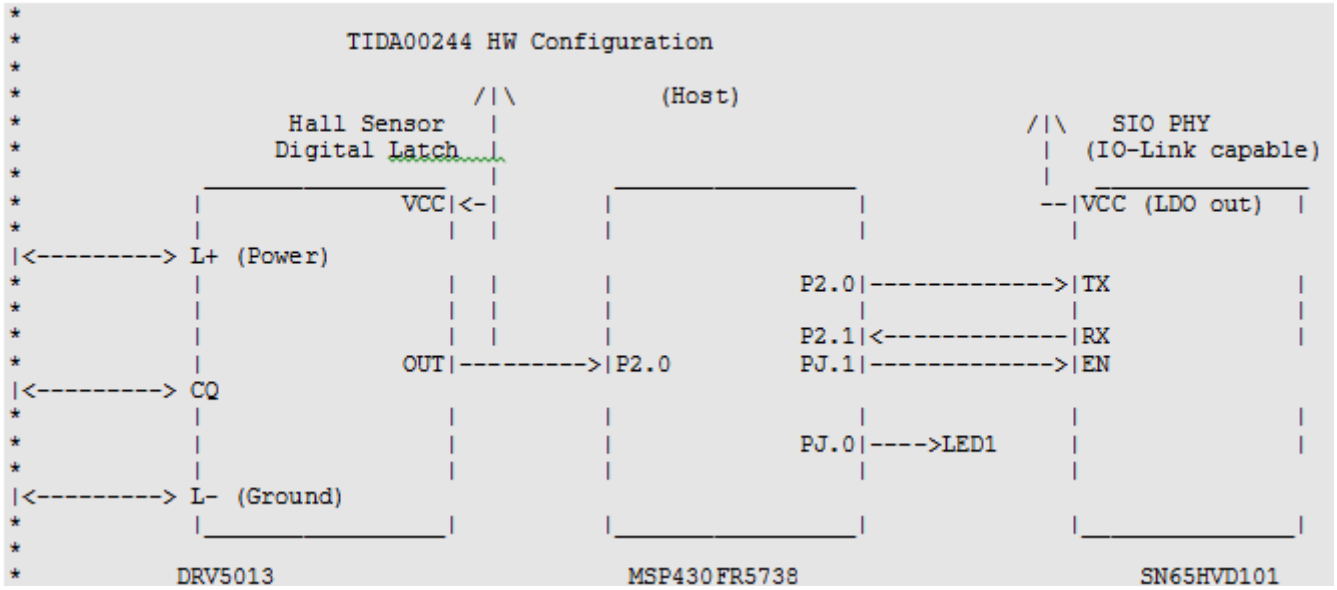
void BSP_Init (void)

Definition at line 58 of file BSP.c.

Here is the call graph for this function:

5.2.5 void BSP_Init_TIDA00244 ()

Will provide all the hardware initialization, see **BSP.h** for supported hardware platforms.



It should be noted that while multiple hardware configuration may be supported, only TIDA-00244 will be used for validation. Mileage on other configuration my vary !

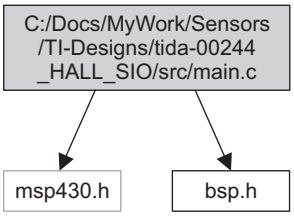
Definition at line 48 of file BSP.c.

Here is the caller graph for this function:

5.3 [installation folder]/tida-00244_HALL_SIO/src/main.c File Reference

```
#include <msp430.h>
#include "bsp.h"
```

Include dependency graph for main.c:



5.3.1 Functions

int **main** (void)

5.3.2 Function Documentation

int main (void)

if Hall sensor output is high

drive LED

drive CQ line low

Definition at line 54 of file main.c.

5.4 Design for Test

To enable fast testing and rapid prototyping, the design includes the following features in addition to the core functions:

1. LED indicating C/Q-line status
2. JTAG interface for debugging and programming

5.4.1 JTAG Interface for Debugging and Programming

For MSP430 Firmware updates, Code Composer Studio is recommended. Code Composer Studio™ (CCStudio) is an integrated development environment (IDE) for Texas Instruments (TI) embedded processor families. CCStudio comprises a suite of tools used to develop and debug embedded applications. It includes compilers for each of TI's device families, source code editor, project build environment, debugger, profiler, simulators, real-time operating system and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. For Programming and Debugging, the MSP430FR5738 implements an Embedded Emulation Module (EEM). It is accessed and controlled through either 4-wire JTAG mode or Spy-Bi-Wire mode. On this Reference Design, the Spy-Bi-Wire mode is supported only. For more details on how the features of the EEM can be used together with Code Composer Studio (CCS), see Advanced Debugging Using the Enhanced Emulation Module Application Report (SLAA393). The 2-wire interface is made up of the SBWTCK (Spy-Bi-Wire test clock) and SBWTDIO (Spy-Bi-Wire test data input/output) pins. The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this pin is internally pulled to ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the RST/NMI pin of the device. For Programming and debugging purposes, the SBWTCK, SBWTDIO, VCC, and GND from the Debugger needs to be connected on J2.

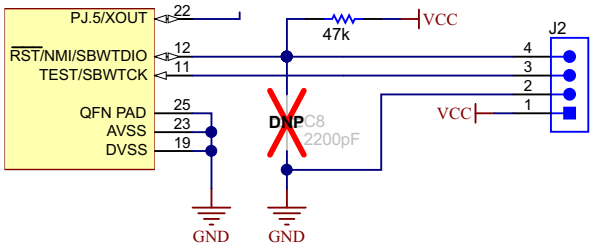


Figure 18. JTAG Connection

With the proper connections, a MSP430 Debugger Interface (such as the MSP-FET430UIF) can be used to program and debug code on the reference design.

CAUTION

Power during Debugging

Special care should be taken during debug to avoid damages due to different power domain in conflicts (4-mA to 20-mA loop power and debugger tools power), read following section carefully.

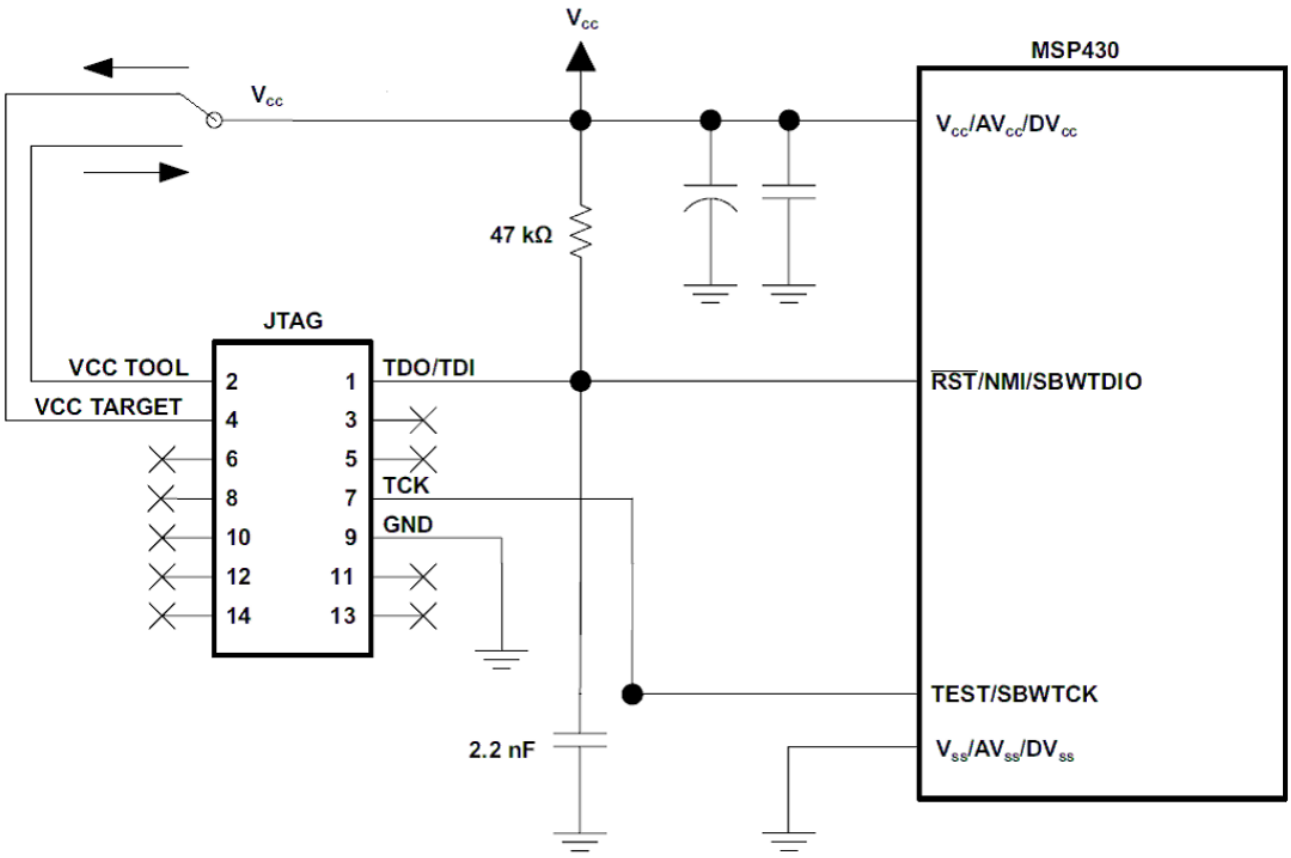


Figure 19. MSP-FET430UIF Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

6 Test Setup

To test the board in switch mode, we added a 2 kOhms resistor between C/Q and L+.

The equipment used for testing is:

- Hp 34401 ampmeter
- Agilent e3631a power supply
- Tectronix tds5034b - oscilloscope

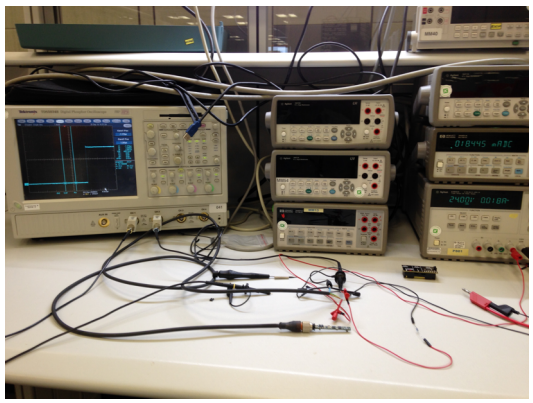


Figure 20. Test Setup

7 Test Results

7.1 Propagation Delay

Figure 21 shows the delay across the MSP430. From the rising edge of the Hall sensor output (visible on Ch1 in yellow) to the falling edge of the CQ (visible on Ch2 in blue), you can see a delay of 14.4µs.

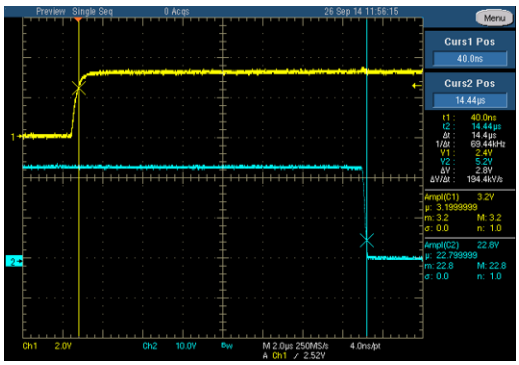


Figure 21. Propagation Delay Across MCU and Output Stage

7.2 Signal Slopes

When zooming on the signal in Figure 21, we can measure on Figure 22, a rising edge on the output of the DRV5013 of 351ns for the transition from 20% to 80%. Similarly on the falling edge of the C/Q line, we can measure on Figure 23, a time from 80% to 20% of 161ns.

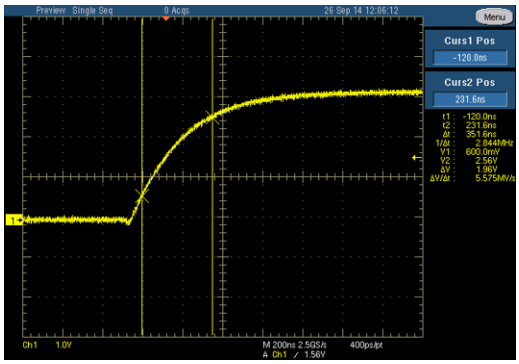


Figure 22. DRV5013 Rising Edge

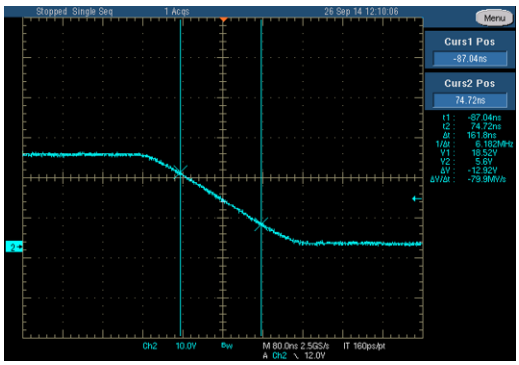


Figure 23. C/Q Line Falling Edge

7.3 Power Consumption

The power consumption of the system is plotted in Figure 24, where the L+ voltage is varied between 18V and 33V.

Two curves are visible, when the LED is OFF (equivalent to the field has been below B_{OP} of DRV5013) and when the LED is ON (when the field has been above B_{RP}).

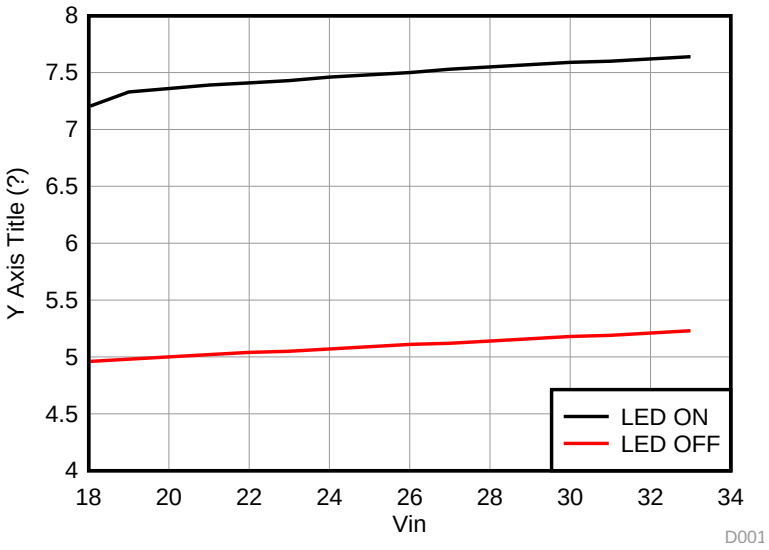


Figure 24. Power Consumption Graphs

8 Design Files

8.1 Bill of Materials

Table 1 lists the bill of materials (BOM).

Table 1. Bill of Materials

Item #	Designator	Qty	Value	Part Number	Manufacturer	Description	Package Reference
1	C1	1	680pF	GRM155R71H681KA01D	MuRata	CAP, CERM, 680pF, 50V, +/-10%, X7R, 0402	0402
2	C2	1	0.022µF	GRM155R71C223KA01D	MuRata	CAP, CERM, 0.022µF, 16V, +/-10%, X7R, 0402	0402
3	C3, C12	2	4.7µF	C1005X5R0J475M050BC	TDK	CAP, CERM, 4.7µF, 6.3V, +/-20%, X5R, 0402	0402
4	C4	1	2.2µF	GRM32ER72A225KA35L	MuRata	CAP, CERM, 2.2µF, 100V, +/-10%, X7R, 1210	1210
5	C6	1	0.1µF	12061C104JAT2A	AVX	CAP, CERM, 0.1µF, 100V, +/-5%, X7R, 1206	1206
6	C7	1	330pF	GRM155R72A331KA01D	MuRata	CAP, CERM, 330pF, 100V, +/-10%, X7R, 0402	0402
7	C9	1	0.47µF	GRM155R60J474KE19D	MuRata	CAP, CERM, 0.47µF, 6.3V, +/-10%, X5R, 0402	0402
8	C10	1	0.1µF	C1005X5R0J104K	TDK	CAP, CERM, 0.1µF, 6.3V, +/-10%, X5R, 0402	0402
9	D1	1	Yellow	LY L29K-J1K2-26-Z	OSRAM	LED, Yellow, SMD	LED, 1.3x0.65x0.8mm
10	D2	1	200V	RF071M2S	Rohm	Diode, Ultrafast, 200V, 1A, SOD-123	SOD-123
11	D3	1	Green	LG L29K-G2J1-24-Z	OSRAM	LED, Green, SMD	1.7x0.65x0.8mm
12	D4, D5, D6	3	30V	SMAJ30CA	Bourns	Diode, TVS, Bi, 30V, 400W, SMA	SMA
13	J1	1		09 0431 212 04	Binder-Connector	M12 Socket, 4Pos, TH	M12 Conn D12x14.3
14	J2	1		850-10-004-40-001000	Mill-Max	Header, 4x1, 50mil, R/A, SMT	Header, 50mil, R/A,SMT
15	R1	1	10.0k	CRCW040210K0FKED	Vishay-Dale	RES, 10.0k ohm, 1%, 0.063W, 0402	0402
16	R5, R6	2	820	CRCW0402820RJNED	Vishay-Dale	RES, 820 ohm, 5%, 0.063W, 0402	0402
17	R7	1	47k	CRCW040247K0JNED	Vishay-Dale	RES, 47k ohm, 5%, 0.063W, 0402	0402
18	R8	1	4.7k	CRCW04024K70JNED	Vishay-Dale	RES, 4.7k ohm, 5%, 0.063W, 0402	0402
19	S1	1		SKRKAEE010	Alps	Switch, Push Button, SMD	2.9x2x3.9mm SMD

Table 1. Bill of Materials (continued)

Item #	Designator	Qty	Value	Part Number	Manufacturer	Description	Package Reference
20	U1	1		DRV5013ADQDBZ	Texas Instruments	Digital-Latch Hall Effect Sensor, DBZ0003A	DBZ0003A
21	U2	1		SN65HVD101RGB	Texas Instruments	IO-LINK PHY for Device Nodes, RGB0020A	RGB0020A
22	U3	1		MSP430FR5738IRGE	Texas Instruments	24 MHz Mixed Signal Microcontroller, 1024 B SRAM and 17 GPIOs, -40 to 85 °C, RGE0024G	RGE0024G
23	C5	0	330pF	GRM155R72A331KA01D	MuRata	CAP, CERM, 330pF, 100V, +/-10%, X7R, 0402	0402
24	C8	0	2200pF	GRM155R70J222KA01D	MuRata	CAP, CERM, 2200pF, 6.3V, +/-10%, X7R, 0402	0402
25	C11	0	0.1µF	C1005X5R0J104K	TDK	CAP, CERM, 0.1µF, 6.3V, +/-10%, X5R, 0402	0402
26	R2, R3, R4	0	0	CRCW04020000Z0ED	Vishay-Dale	RES, 0 ohm, 5%, 0.063W, 0402	0402

8.2 Schematics

The schematics are presented in the following order: TIDA-00244.

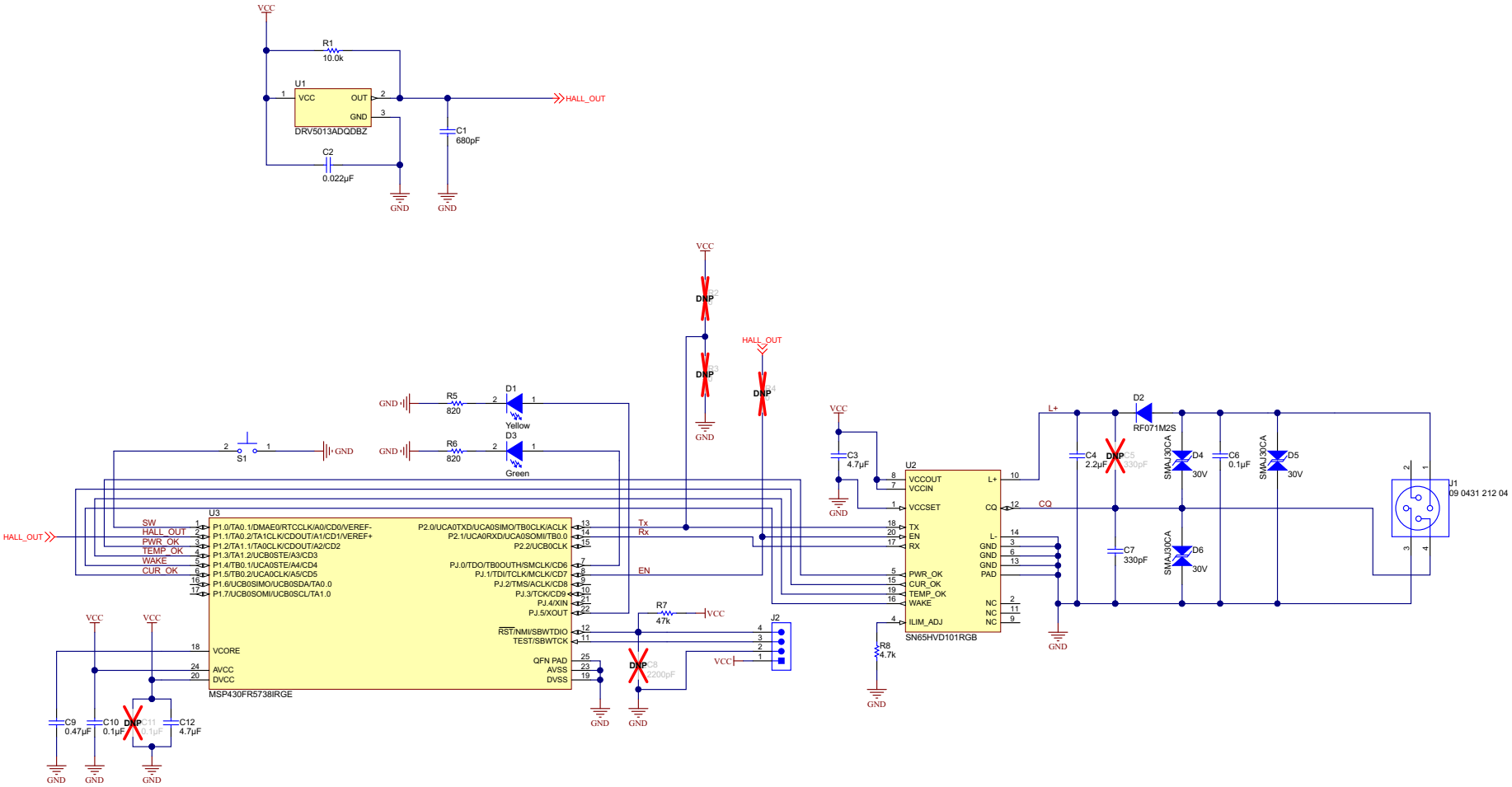


Figure 25. Proximity Switch and I/O-Link Schematic

8.3 PCB Layer Plots

To download the layer plots, see the design files at TIDA-00244.

Figure 26. Top Overlay

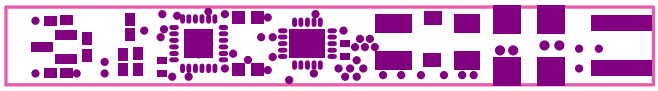


Figure 27. Top Solder Mask

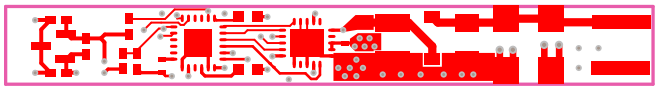


Figure 28. Top Layer

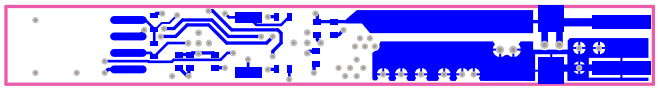


Figure 29. Bottom Layer

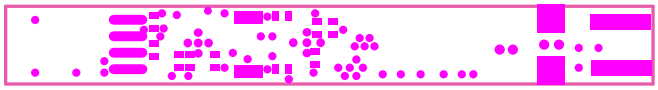


Figure 30. Bottom Solder Mask

Figure 31. Bottom Overlay

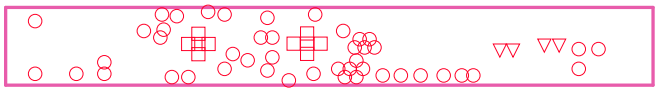


Figure 32. Drill Drawing

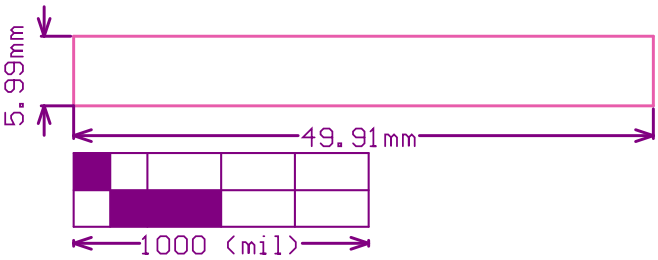


Figure 33. Board Dimensions

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00244.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00244.

8.6 Assembly Drawings

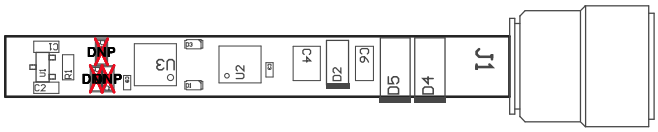


Figure 34. Assembly Drawing Top

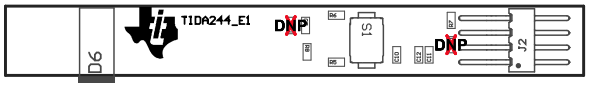


Figure 35. Assembly Drawing Bottom

9 Software Files

To download the software files, see the design files at TIDA-00244.

10 References

1. IEC, IEC 61131-2 Programmable controllers – Part 2: Equipment requirements and tests, 2007.
2. Community, IO-LINK, IO-Link Interface and System Specification v1.1.2, IO-LINK Community, 2013.
3. SN65HVS882 datasheet (SLAS601)
4. E. Ramsden, Hall-Effect Sensors: Theory and Application, Second Edition, Newnes, 2006.
5. TIDA-00188

11 Terminology

SIO: standard input/output (digital switching mode) [IEC 61131-2]

SDCI: single-drop digital communication interface

Hall-effect: A Hall-effect sensor is a transducer leveraging certain material whose property is to generate a voltage proportional to the magnetic field they are exposed to.

sensitive axis : axis going through and orthogonal to the plane where the Hall-effect sensing element has been placed.

12 About the Author

MATTHIEU CHEVRIER is a systems architect at Texas Instruments, where he is responsible for defining and developing reference design solutions for the industrial segment. Matthieu brings to this role his extensive experience in embedded system designs in both hardware (power management, mixed signal, and so on) and software (such as low level drivers, RTOS, and compilers). Matthieu earned his master of science in electrical engineering (MSEE) from Supélec, an Ivy League university in France. Matthieu holds patents from IPO, EPO, and USPTO.

ALEXANDER WEILER is a systems architect at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Alexander brings to this role his extensive experience in high-speed digital, low-noise analog, and RF system-level design expertise. Alexander earned his diploma in electrical engineering (Dipl.-Ing. (FH)) from the University of Applied Science in Karlsruhe, Germany.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265