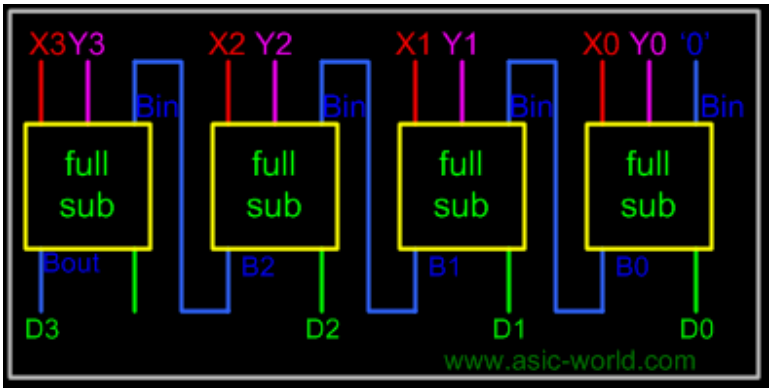
4 BIT SUBSTRACTOR

4-bit parallel substractor

Parallel binary subtracter can be implemented by cascading several full-subtracters. Implementation and associated problems are those of a parallel binary adder, seen before in parallel binary adder section.

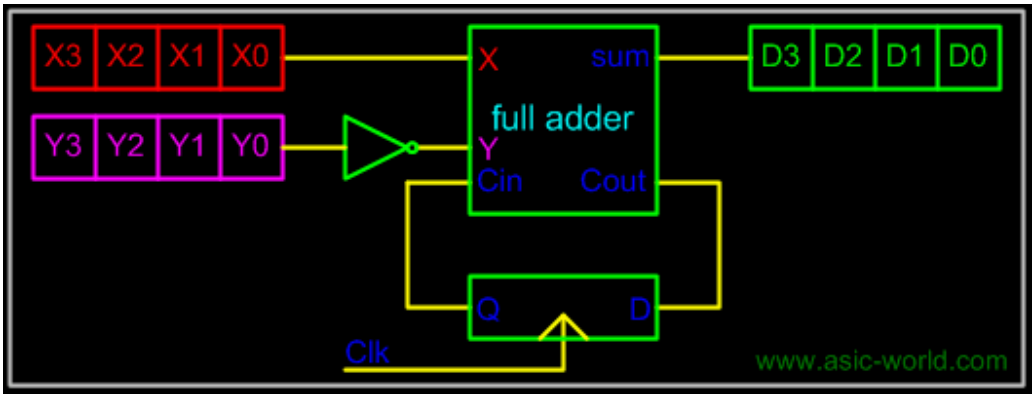
Below is the block level representation of a 4-bit parallel binary subtracter, which subtracts 4-bit Y3Y2Y1Y0 from 4-bit X3X2X1X0. It has 4-bit difference output D3D2D1D0 with borrow output Bout.



4-bit serial substractor

A serial subtracter can be obtained by converting the serial adder using the 2's complement system. The subtrahend is stored in the Y register and must be 2's complemented before it is added to the minuend stored in the X register.

The circuit for a 4-bit serial subtracter using full-adder is shown in the figure below


X3
X2
X1
X0
Y3
Y2
Y1
Y0
X
sum
full adder
Y
Cin
Cout
D3
D2
D1
D0
Q
D
Clk
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