SR LATCH

An SR latch is shown in figure. The latch Truth table is shown in the following table. The two inputs, S and R denote ``set'' and ``reset'' respectively. The latch has memory, and the present output is dependent on the state of the latch. Thus the output at n^{th} instant, denoted by Q_n is dependent on output at $(n-1)^{th}$ instant, denoted by Q_{n-1}.

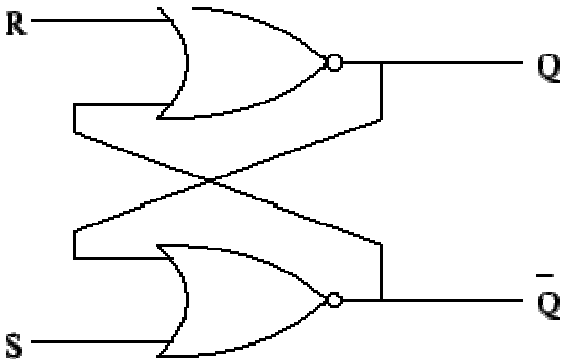


Figure: Construction of a latch from NOR gates

S	R	Q_n	$\overline{Q_n}$
1	0	1	0
0	1	0	1
1	1	0	0
0	0	Q_{n-1}	$\overline{Q_{n-1}}$

Note that in $SR=11$ state, both Q_n and $\overline{Q_n}$ are 0, which seems absurd. Thus, conventionally, the state $SR=11$ is said to be ``not allowed''.

A similar latch, known as $\overline{SR}$ latch is constructed using NAND gates (as opposed to NOR gates for SR latch). The students should again check that the working of the latch coheres with that of the truth table.

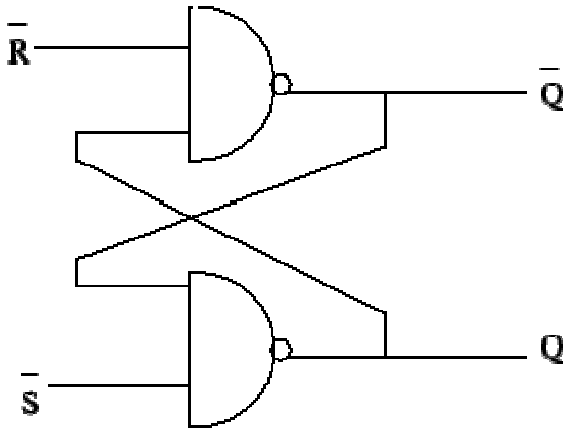


Figure: Construction of a latch from NAND gates

$\overline{S}$	$\overline{R}$	Q_n	$\overline{Q_n}$
0	1	1	0
1	0	0	1
0	0	1	1
1	1	Q_{n-1}	$\overline{Q_{n-1}}$

To avoid ``race'' between the inputs, to have a control on when the input affects the latch, the circuit is often implemented.

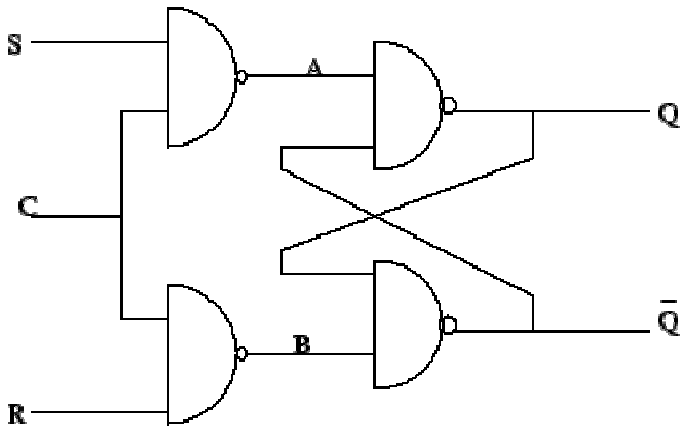
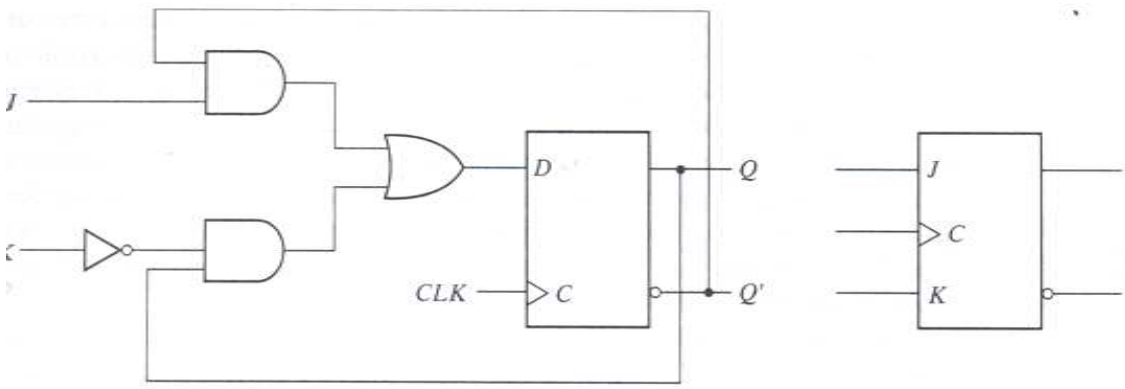


Figure: Circuit to avoid ``race'' condition

The inputs have an effect on the latch only when $C = 1$, otherwise, the previous state is maintained. The input C may be a clock, so that whatever transitions in S and R take place before the clock C changes to 1 do not affect the outputs, and only when the inputs have become stable is the system affected.

Basic flip-flops Triggering And Excitation Tables

The behavior of the master-slave flip-flop just described dictates that the output may change only during the negative edge of the clock. It is also possible to design the circuit so that the flip-flop output changes on the positive edge of the clock. This happens in a flip-flop that has an additional inverter between the CLK terminal and the junction between the other inverter and input C of the master latch. Such flip-flop is triggered with a negative pulse, so that the negative edge of the clock affects the master and the positive edge affects the slave and the output terminal.



There are three operations that can be preformed with a flip-flop: set it to 1, reset it to 0, or complement its output. The JK flip-flop performs all three operations. The circuit diagram of a JK flip-flop constructed with a D flip-flop and gates is shown in Fig 1 (a). The J input sets the flip-flop to 1, the K input resets it to 0, and when both inputs are enabled the output is complemented. This can be verified by investigating the circuit applied to the D input:

$$D = JQ' + K'Q$$

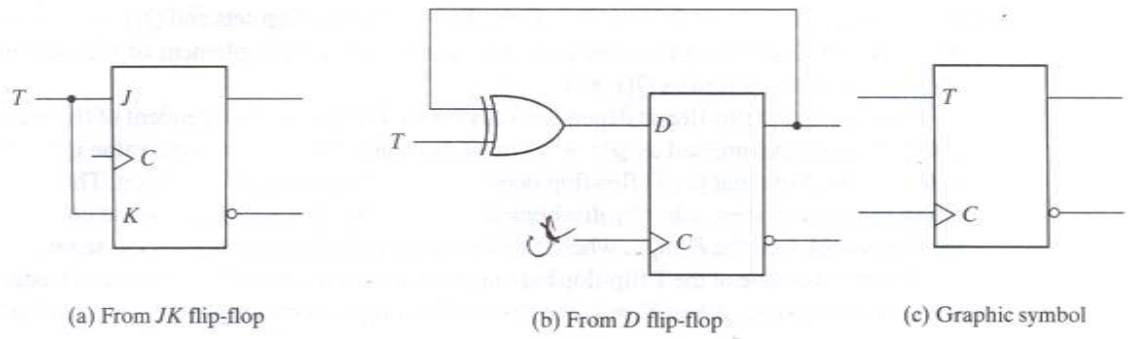
When J = 1 and K = 0, D = Q' + Q = 1, so the next clock edge sets the output to 1. When J = 0 and K = 1, D = 0, so the next clock edge resets the output to 0. When both J = K = 1, D = Q', the next clock edge complements the output. When both J = K = 0, D = Q, the clock edge leaves the output unchanged. The graphic symbol for the JK flip-flop is shown in Fig 1. It is similar to the graphic symbol of the D flip-flop, except that now the inputs are marked J and K.

The T (toggle) flip-flop is a complementing flip-flop and can be obtained from a JK flip-flop when inputs J and K are tied together. This is shown in Fig 2 (a). When T = 0 (J = K = 0) a clock edge does not change the output. When T = 1 (J = K =1) a clock edge complements the output. The complementing flip-flop and an exclusive-OR gate as shown n Fig 2 (b). The expression for the D input is

$$D = T\,Q = TQ' + T'Q$$

When T = 0, then D = Q, and there is no change in the output. When T = 1, then D = Q' and the output complements. The graphic symbol for this flip-flop has a T symbol in the input.

Fig



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

Characteristic Tables

A characteristic table defines the logic properties of a flip-flop by describing its operation in tabular form.

Flip-Flop Characteristic Tables

JK Flip-Flop

J	K	$Q(t+1)$	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip-Flop

D	$Q(t+1)$	
0	0	Reset
1	1	Set

T Flip-Flop

T	$Q(t+1)$	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Characteristic Equation

The logic properties of a flip-flop as described in the characteristic table can be expressed also algebraically with a characteristic equation. For the D flip-flop, we have the characteristic equation

$$D(t + 1) = D$$

It states that the next state of the output will be equal to the value of input D in the present state. The characteristic equation for the JK flip-flop can be derived from the characteristic table or from the circuit of Fig 1. We obtain

$$Q(t + 1) = JQ' + K'Q$$

Where Q is the value of the flip-flop output prior to the application of a clock edge. The characteristic equation for the T flip-flop is obtained from the circuit of Fig 2

$$Q(t + 1) = T Q = TQ' + T'Q$$