COMBINATIONAL LOGIC CIRCUITS

Combinational logic circuit is a circuit whose output depends only on the present input not on the previous outputs. It circuits perform various arithmetic functions such as Addition, Subtraction.

Design Using Conventional Logic Gates

A combinational circuit that performs the addition of two bits is called a half adder. One that, performs the addition of three bits (two significant bits and a previous carry) is a full adder.

Half Adder

The input variables designate the augend and addend bits; the output variable produce the sum and carry. We assign symbols x and y to the two inputs and S (for sum) and C (for carry) to the outputs. The truth table for the half adder is listed in Table 1. The C output is 1 only when both inputs are 1. The S output represents the least significant bit of the sum.

The simplified Boolean functions for the two outputs can be obtained directly from the truth table. The simplified sum of products expressions are

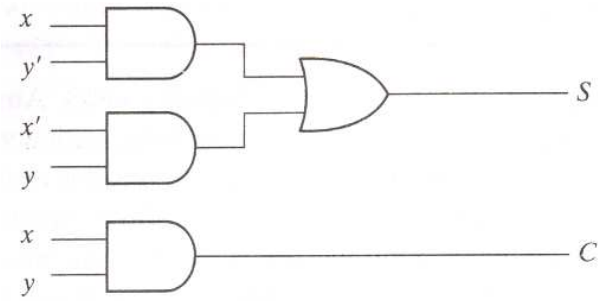
$$S = x'y + xy'$$

$$C = xy$$

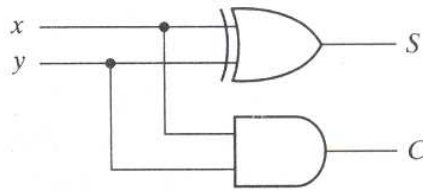
The logic diagram of the half adder implemented in sum of products is shown in Fig 2 (a). It can be also implemented with an exclusive-OR and an AND gate as shown in Fig 2 (b).

Half Adder

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



(a) $S = xy' + x'y$
$C = xy$



(b) $S = x \oplus y$
$C = xy$

Full-Adder

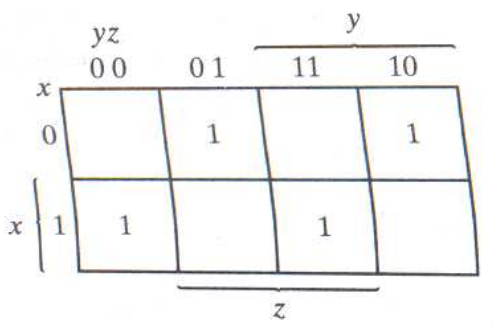
A full-adder is a combinational circuit that forms the arithmetic sum of three bits. It consists of three inputs and two outputs. Two of the input variables, denoted by x and y, represent the two significant bits to be added. The third input, z, represents the carry form the previous lower significant position. Two outputs are necessary because the arithmetic sum of three binary digits ranges in value from 0 to 3, and binary 2 or 3 needs two digits. The two outputs are designated by the symbols S for sum and C for carry. The binary variables S gives the value of the least significant bit of the sum. The binary variable C gives the output carry. The truth table of the full adder is listed in table 2.

Fig

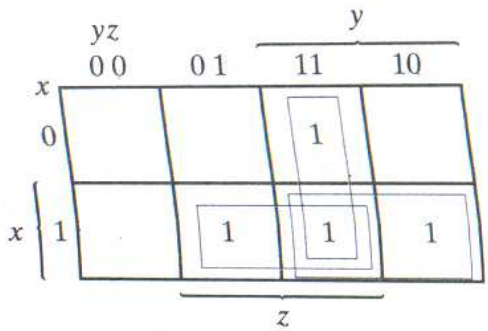
Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Fig



$S = x'y'z + x'yz' + xy'z' + xyz$



$C = xy + xz + yz$

$\Rightarrow C = xy + xy'z + x'yz$

The maps for the outputs of the full adder are shown in Fig 3. The simplified expressions are

S = x'y'z + x'yz' + xy'z' + xyz

C = xy + xz + yz

The logic diagram for the full adder implemented in sum of products is shown in Fig 3. It can be also implemented with two half adders and one OR gate, as shown in Fig 4. The S output from the second half adcder is the exclusive-OR of z and the output of the first half adder, giving

$$S = z \quad (x \ y)$$
$$= z'(xy' + x'y) + z(xy' + x'y)'$$
$$= z(xy' + x'y) + z(xy + x'y')$$
$$= xy'z' + x'yz' + zxy + x'y'z$$

The carry output is

$$C = z(xy' + x'y) + xy = xy'z + x'yz + xy$$

Fig