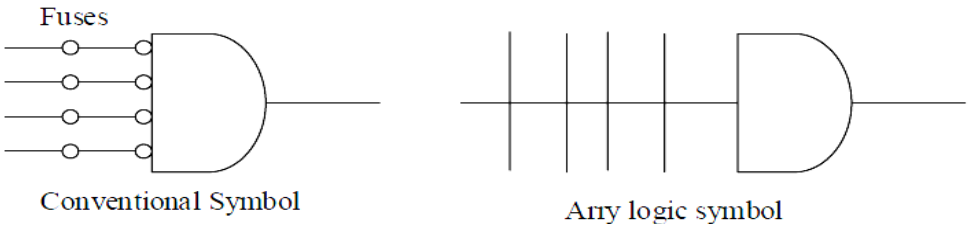
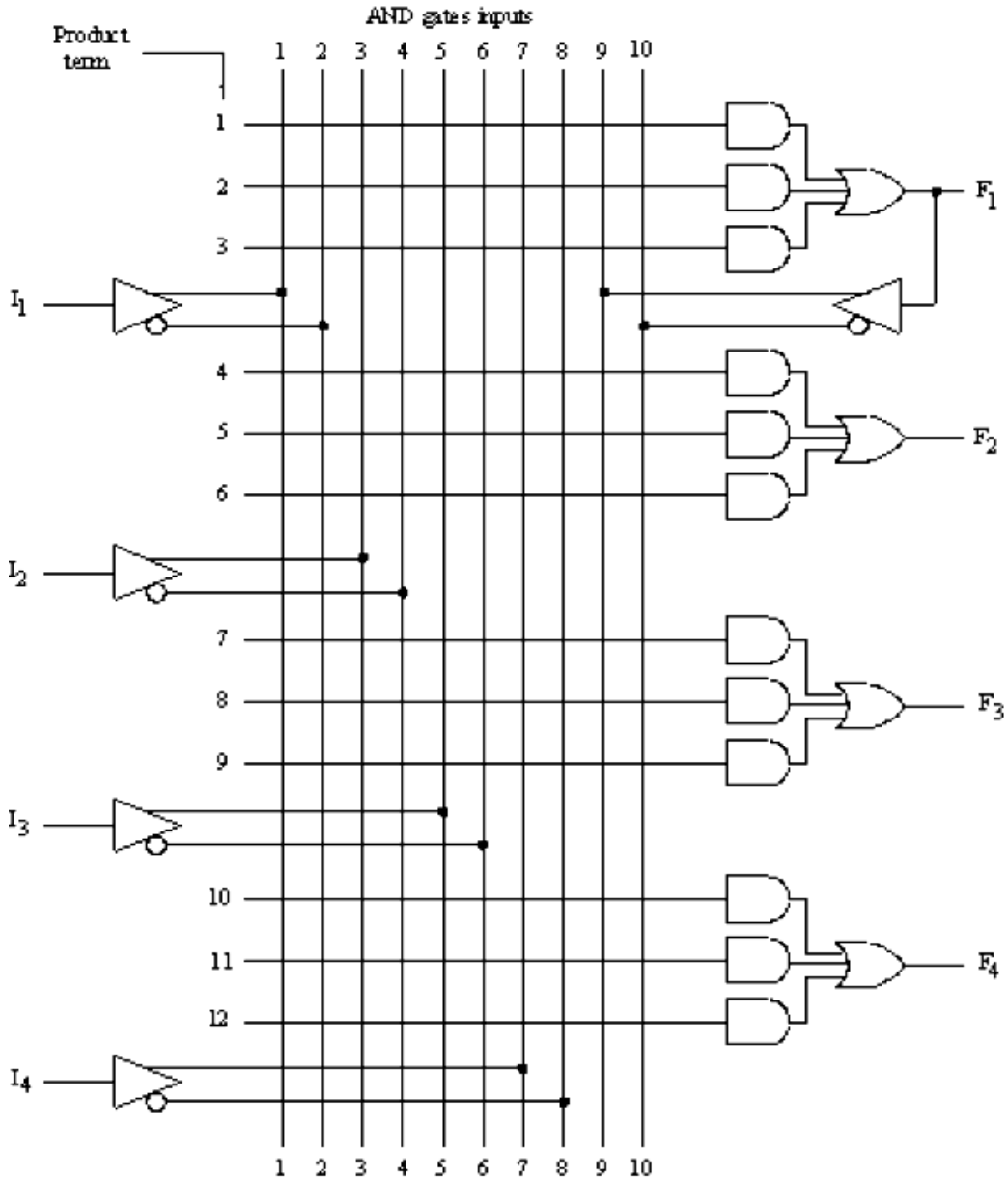
PROGRAMMABLE ARRAY LOGIC

The programmable array logic (PAL) is a programmable logic device with a fixed OR array and a programmable AND array because only the AND gates are programmable; the PAL is easier to program, but is not as flexible as the PLA. In PAL the conventional symbol is simply represented by a Array logic symbol as shown below



Array logic symbol uses a single horizontal line connected to the gate input and multiple vertical lines to indicate the individual inputs. Each intersection between a vertical line and the common horizontal line has fused connection. We can draw the array logic for the OR gate or any other type of multiple input gate.

Below figure shows the array logic configuration of typical PALS it has four inputs and our outputs. Each input has a buffer and an inverter gate. Note that the two gates are shown with one composite graphic symbol with normal and complement outputs. There are four sections in the unit, each being composed of a three wide AND-OR array. This is the term used to indicate that there are three programmable AND gates in each section and one fixed OR gate. Each AND gate has 10 fused programmable inputs. This is shown in the diagram by 10 vertical lines intersecting each horizontal line. The horizontal line symbolizes the multiple-input configuration of the AND gate. One of the outputs is connected to a buffer inverter gate and then fed back into the inputs of the AND gates through the fuses.


AND gates inputs
Product term
1 2 3 4 5 6 7 8 9 10
1
2
3
4
5
6
7
8
9
10
11
12
I1
I2
I3
I4
F1
F2
F3
F4