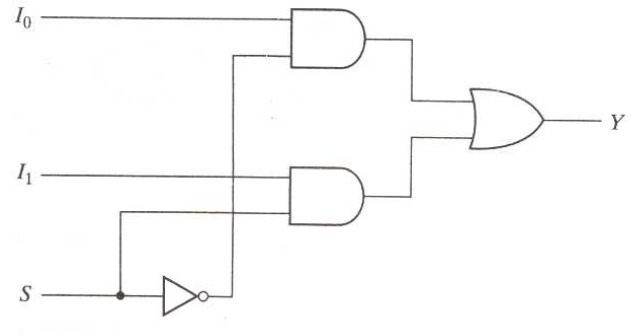
MULTIPLEXERS

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.

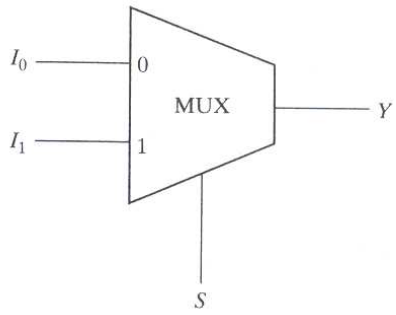
A 2-to-1-line multiplexer connects one of two 1-bit sources to a common to a common destination as shown in Fig 1. The circuit has two data input lines, one output line, and one selection line S. When S = 0, the upper AND gate is enabled and I0 has a path to the output. When S = 1 the lower AND gate ius enabled and I! has a path to the output. The multiplexer acts like an electronic switch that selects one of two sources. The block diagram of a multiplexer is sometimes depicted using a wedge-shaped symbol as shown in Fig 1 (B). It suggests visually how a selected one of multiple data sources is directed into a single destination. The multiplexer is often labeled as MUX in block diagrams

A 4-to-1-line multiplexer is shown in Fig 2. Each of the four inputs, I_0 through, I_0 through I_3, is applied to one input of an AND gate. Selection lines S_1 and S_0 are decoded to select a particular AND gate. The outputs of the AND gates are applied to a single OR gate that provided the 1-line output. The function table lists the input that is passed to the output for each combination of the binary selection values. To demonstrate the circuit operation, consider the case when $S_1S_0 = 10$. The AND gate associated with input I_2 has two of its inputs equal to 1 and the third input connected to I_2. The other three AND gates have at least one input equal to 0, which makes their outputs equal to 0. The OR gate output is now equal to the value of I2, providing a path from the selected input to the Output. A multiplexer is also called a data selector, since it selects one of many inputs and steers the binary information to the output line.

Fig



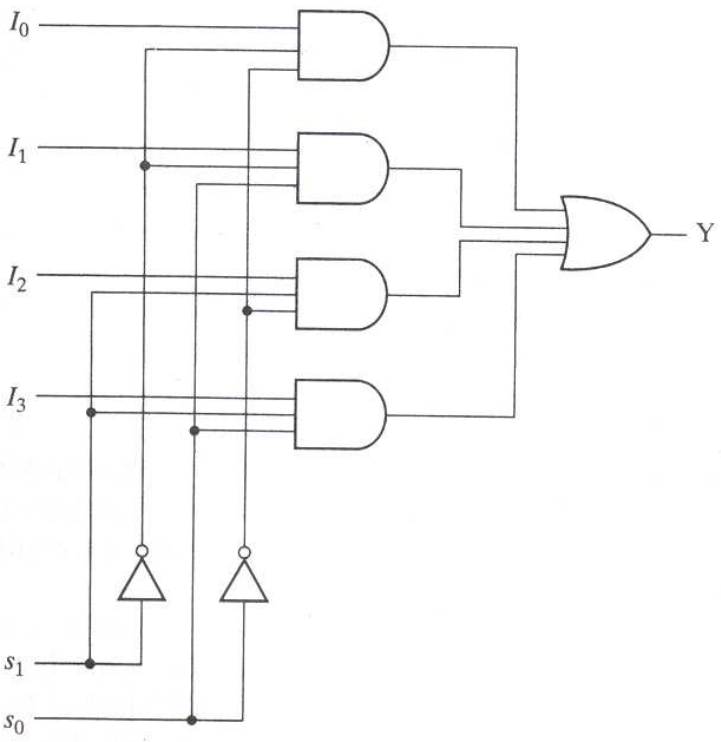
(a) Logic diagram



(b) Block diagram

The AND gates and inverters in the multiplexer resemble a decoder circuit and, indeed, they decode the selection input lines. In general, a 2^n-to-1-line multiplexer is constructed from an n-to-2^n decoder by adding to it 2n input lines, one to each AND gate. The outputs of the AND gates are applied to a single OR gate. The size of a multiplexer is specified by the number 2n of its data input lines and the single output line. The n selection lines are implied from the 2n data lines. As in decoders, multiplexers may have

Fig



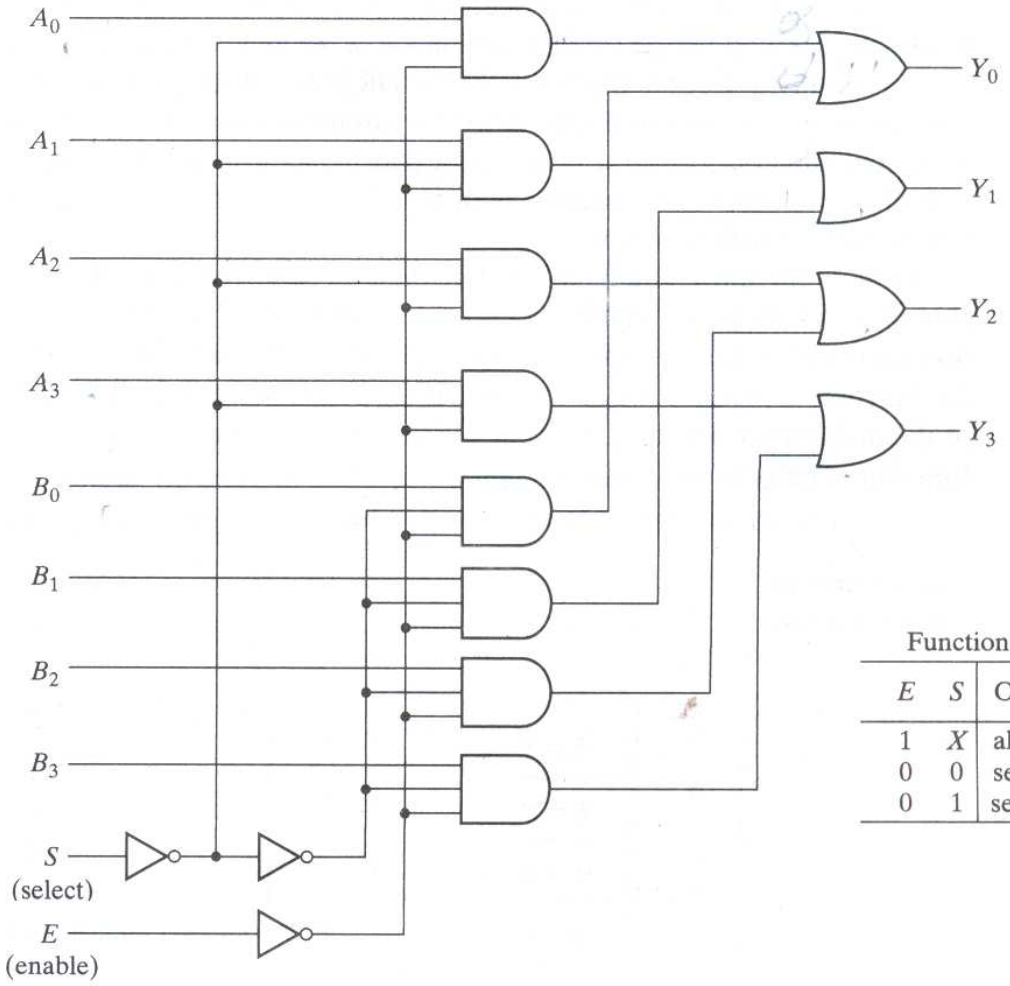
(a) Logic diagram

s_1	s_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(b) Function table

An enable input to control the operation of the unit. When the enable input is in the inactive state, the outputs are disabled, and when it is in the active state, the circuit functions as a normal multiplexer.

Multiplexer circuit can be combined with common selection inputs to provide multiple bit selection logic. As an illustration, a quadruple 2-to-1-line multiplexers are shown in Fig 3. The circuit has four multiplexers, each capable of selecting one of two input lines. Output Y_0 can be selected to come from either input A_0 or B_0. Similarly, output Y1 may have the value of A_1 or B_1, and so on. Input selection line S selects one of the lines in each of the four multiplexers. The enable input E must be active for normal operation. Although the circuit contains four 2-to-1-line multiplexers, we are more likely to view it as a circuit that selects one of two 4-bits sets of data lines. As shown in the function table, the units is enable when E = 0. Then, if S = 0, the four A inputs have a path to the four outputs. On the other hand, if S = 1, the four B inputs are applied to the outputs. The outputs have all 0's when E = 1, regardless of the value of S



Function table

E	S	Output Y
1	X	all 0's
0	0	select A
0	1	select B