

PROBLEMS

1.Design a Gray-to Excess-3 Code converter using NAND gates

Ans. Gray to Excess3 code converter:

Decimal	Binary Equivalent	Gray Code			Excess-3 Code			
		G_2	G_1	G_0	E_3	E_2	E_1	E_0
0	0 0 0	0	0	0	0	0	1	1
1	0 0 1	0	0	1	0	1	0	0
2	0 1 0	0	1	1	0	1	0	1
3	0 1 1	0	1	0	0	1	1	0
4	1 0 0	1	1	0	0	1	1	1
5	1 0 1	1	1	1	1	0	0	0
6	1 1 0	1	0	1	1	0	0	1
7	1 1 1	1	0	0	1	0	1	0

K-maps for Excess 3-codes are

For $E_3 \rightarrow$

		$G_1 G_0$			
		$\bar{G}_1 \bar{G}_0$	$\bar{G}_1 G_0$	$G_1 \bar{G}_0$	$G_1 G_0$
G_2	\bar{G}_2	0	0	0	0
	G_2	1	1	1	0

$$\therefore E_3 = G_2 \bar{G}_1 + G_2 G_0$$

For $E_2 \rightarrow$

		$G_1 G_0$			
		$\bar{G}_1 \bar{G}_0$	$\bar{G}_1 G_0$	$G_1 \bar{G}_0$	$G_1 G_0$
G_2	\bar{G}_2	0	1	1	1
	G_2	0	0	0	1

$$\therefore E_2 = \bar{G}_2 G_0 + G_1 \bar{G}_0$$

For $E_1 \rightarrow$

G_2	$G_1\bar{G}_0$	$\bar{G}_1\bar{G}_0$	\bar{G}_1G_0	G_1G_0	$G_1\bar{G}_0$
	\bar{G}_2	1	0	0	1
G_2	\bar{G}_2	1	0	0	1

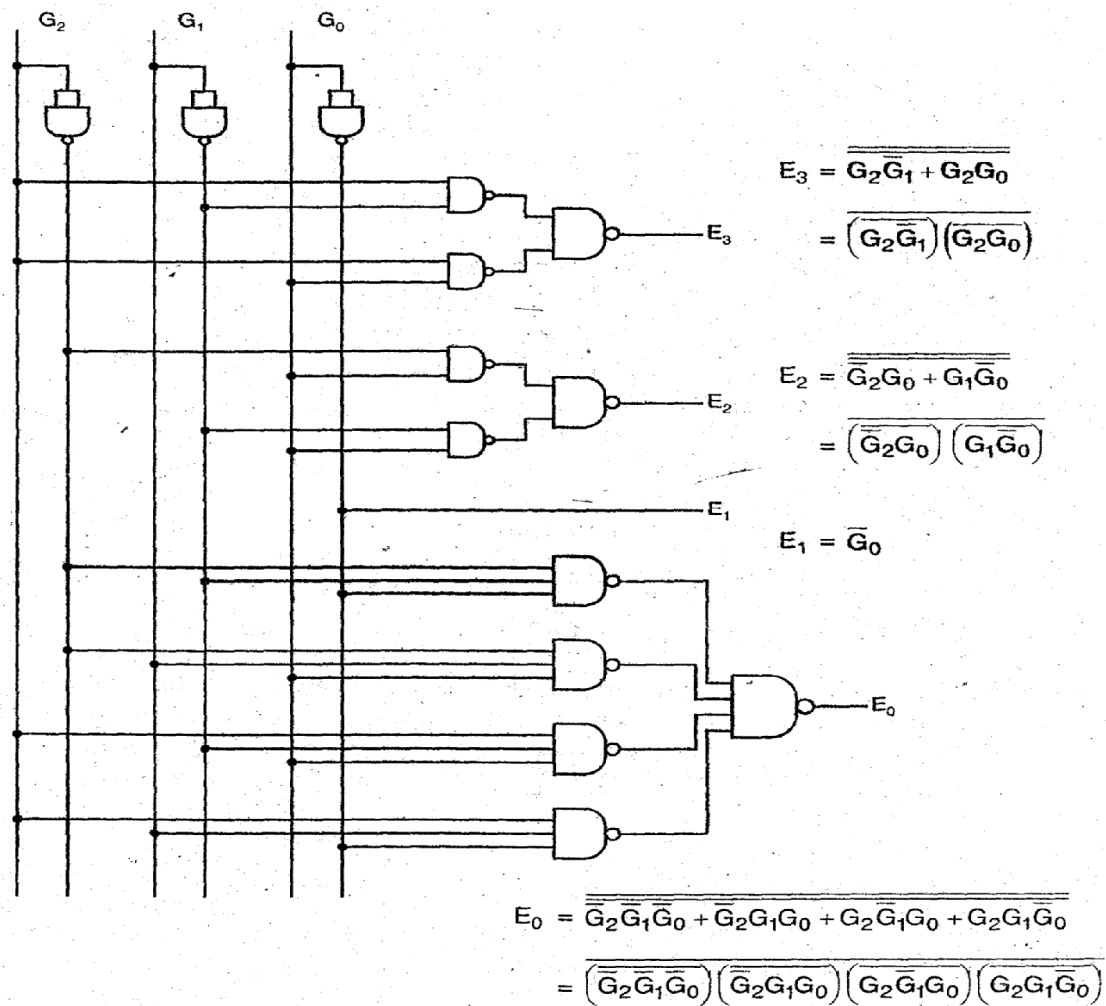
$$\therefore E_1 = \bar{G}_0$$

For $E_0 \rightarrow$

G_2	$G_1\bar{G}_0$	$\bar{G}_1\bar{G}_0$	\bar{G}_1G_0	G_1G_0	$G_1\bar{G}_0$
	\bar{G}_2	1	0	1	0
G_2	\bar{G}_2	0	1	0	1

$$\therefore E_0 = \bar{G}_2\bar{G}_1\bar{G}_0 + \bar{G}_2G_1G_0 + G_2\bar{G}_1G_0 + G_2G_1\bar{G}_0$$

Circuit Diagram:



3. Design 3 bit Gray Code to binary converters

Ans. The truth table for 3 bit Gray Code to binary conversion is as shown:

Decimal Equipment	Gray Code			Binary Code		
	G_2	G_1	G_0	B_2	B_1	B_0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
3	0	1	1	0	1	0
2	0	1	0	0	1	1
6	1	1	0	1	0	0
7	1	1	1	1	0	1
5	1	0	1	1	1	0
4	1	0	0	1	1	1

K-Maps:

For B_2 :

$G_1 G_0$		$\bar{G}_1 \bar{G}_0$	$\bar{G}_1 G_0$	$G_1 G_0$	$G_1 \bar{G}_0$	
		\bar{G}_2	G_2	\bar{G}_2	G_2	
\bar{G}_2	0	0	0	0	2	$\therefore B_2 = G_2$
G_2	1	1	1	1	6	

For B_1 :

$G_1 G_0$		$\bar{G}_1 \bar{G}_0$	$\bar{G}_1 G_0$	$G_1 G_0$	$G_1 \bar{G}_0$	
		\bar{G}_2	G_2	\bar{G}_2	G_2	
\bar{G}_2	0	0	1	1	2	$\therefore B_1 = \bar{G}_2 G_1 + G_2 \bar{G}_1$ $B_1 = G_1 \oplus G_2$
G_2	1	1	0	0	6	

For B_0 :

$G_1 G_0$	$\bar{G}_1 \bar{G}_0$	$\bar{G}_1 G_0$	$G_1 G_0$	$G_1 \bar{G}_0$
G_2				
\bar{G}_2	0 0	1 1	0 3	1 2
G_2	1 4	0 5	1 7	0 6

$$\begin{aligned}
 \therefore B_0 &= \bar{G}_2 \bar{G}_1 G_0 + \bar{G}_2 G_1 \bar{G}_0 + \\
 &\quad G_2 \bar{G}_1 \bar{G}_0 + G_2 G_1 G_0 \\
 &= \bar{G}_2 (\bar{G}_1 G_0 + G_1 \bar{G}_0) + G_2 (\bar{G}_1 \bar{G}_0 + G_1 G_0) \\
 &= \bar{G}_2 (G_1 \oplus G_0) + G_2 (G_1 \odot G_0) \\
 &= \bar{G}_2 (G_1 \oplus G_0) + G_2 (\overline{G_1 \oplus G_0}) \\
 \therefore B_0 &= G_1 \oplus G_0 \oplus G_2.
 \end{aligned}$$

Circuit Implementation is as shown:

