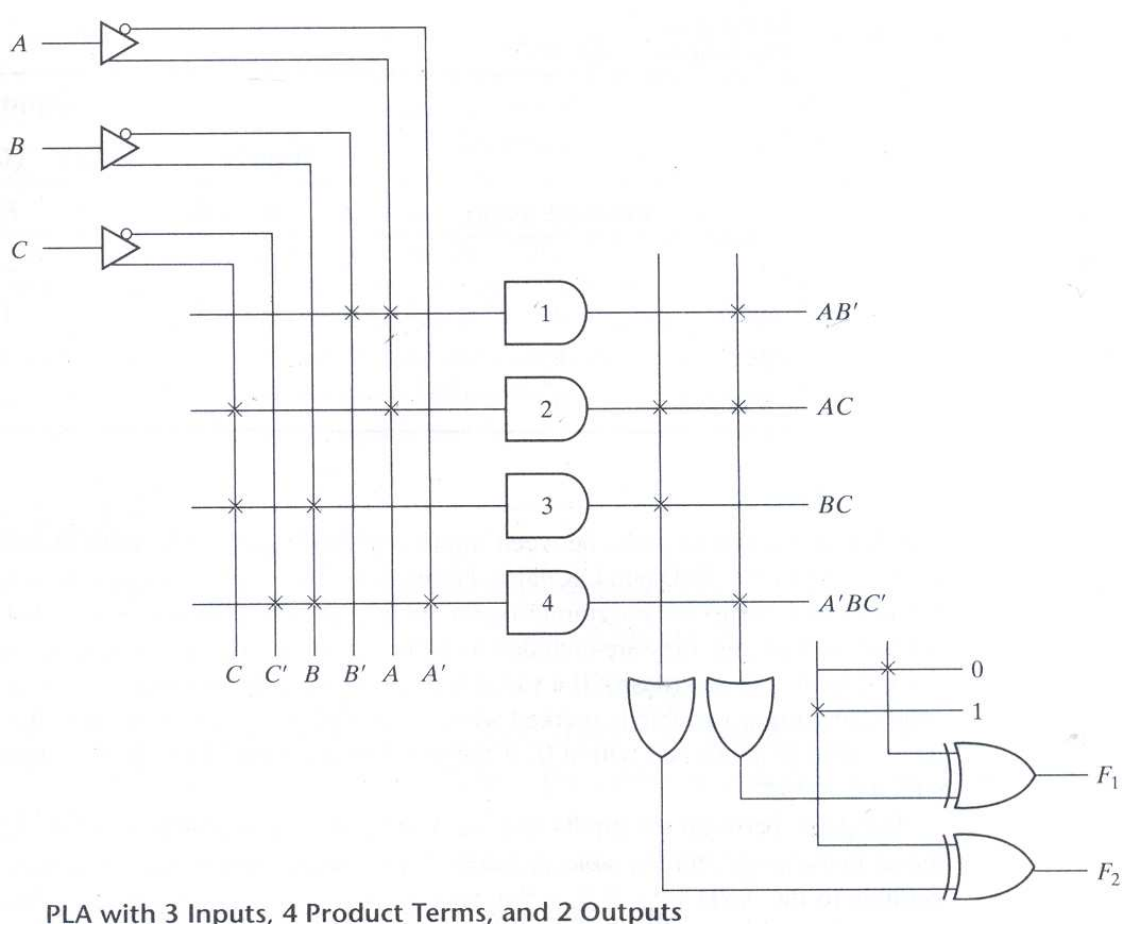
PLA, PLD

The programmable logic array (PLA) is similar to the PROM in concept except that the PLA does not provide full decoding of the variable and does not generate all the minterms. The decoder is replaced by an array of AND gates that can be programmed to generate any product term of the input variables. The product terms are then connected to OR gates to provide the sum of products for the required Boolean functions.



PLA with 3 Inputs, 4 Product Terms, and 2 Outputs

The internal logic of a PLA with three inputs and two outputs is shown in Fig 1. The diagram uses the array logic graphic symbols for complex circuits. Each input goes through a buffer and an inverter shown in the diagram with a composite graphic symbol, which has both the true and complement outputs. Each input and its complement are connected to the inputs of each AND gate as indicated by the intersections between the

vertical and horizontal lines. The outputs of the AND gates are connected to the inputs of each OR gate. The output of the OR gate goes to an XOR gate where the other input can

Be programmed to receive a signal equal to either logic 1 or 0. The output is inverted when XOR input is connected to 1 (Since x 1 = x'). The output does not change when the XOR input is connected to 0 (since x 0 = x). The particular Boolean functions implemented in the PLA of Fig 1 are

F_1 = AB' +AC + A'BC'

F_2 = (AC +BC)

The product terms generated in each AND gate are listed along the output of the gate in the diagram. The product term is determined from the inputs whose crosspoints are connected and marked with a ×. The output of an OR gate gives the logic sum of the selected product terms. The output may be complemented or left in its true form depending on the connection for one of the XOR gate inputs.

PLA, Programmable Table

The PLA programming table consists of three sections. The first section lists the product terms numerically. The second section specifies the required paths between inputs and AND gates. The third section specifies the paths between the And and OR gates. For each output variable, we may have a T (for true) or C (for complement) for programming the XOR gate. The product terms listed on the left are not part of the table: they are included for reference only. For each product term, the inputs are marked with 1, 0 or – (dash). If a variable in the product term appears in its true form, the corresponding input variable is marked with a 1. If it is appears complemented, the corresponding input variable is marked with a 0. If the variable is absent in the product term, it is marked with a dash.

PLA Programming Table

		Inputs			Outputs (T)	(C)
	Product Term	**A**	**B**	**C**	F_1	F_2
AB′	1	1	0	–	1	–
AC	2	1	–	1	1	1
BC	3	–	1	1	–	1
A′BC′	4	0	1	0	1	–