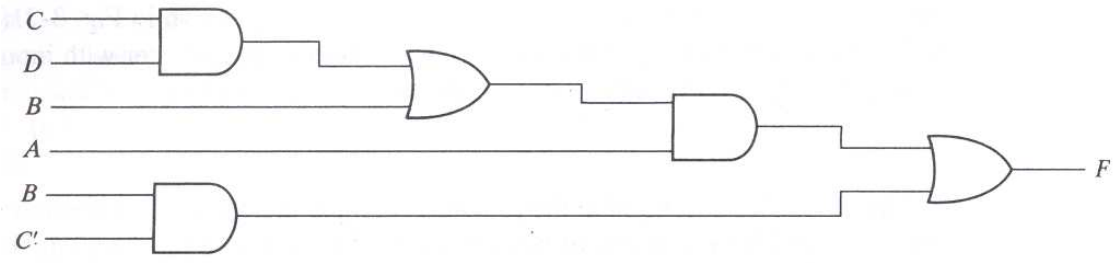
MULTILEVEL NAND/NOR REALIZATIONS

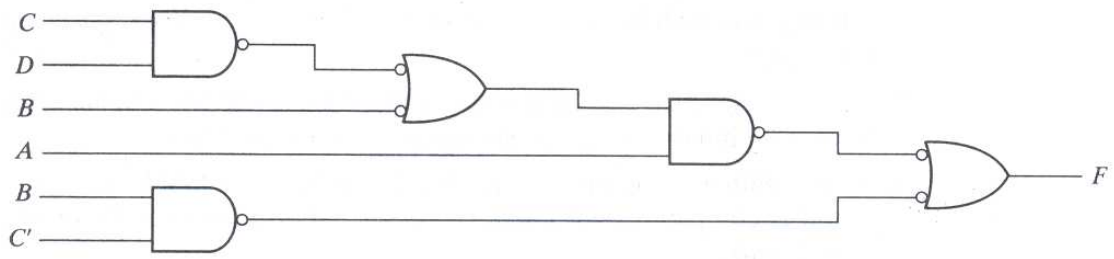
The general procedure for converting a multilevel AND_OR diagram into an all-NAND diagram using mixed notation is as follows:

1.Convert all AND gates to NAND gates with AND-invert graphic symbols

2. Convert all OR gates to NAND gates with invert-OR graphic symbols



(a) AND-OR gates



(a) NAND gates

FIGURE 3-22
Implementing $F = A(CD + B) + BC'$

3. Check all the bubbles in the diagram. For every bubble that is not compensated by an-other small circle along the same line, insert an inverter (one-input NAND gate) or complement the input literal.

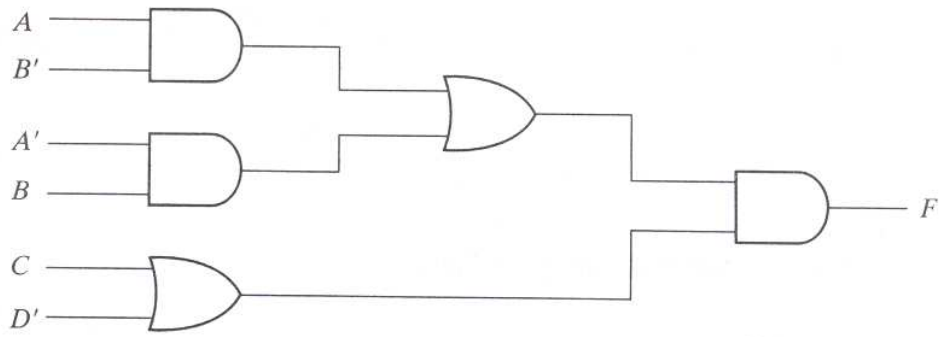
Consider the multilevel Boolean function

F = (AB’ + A’B)(C + D’)

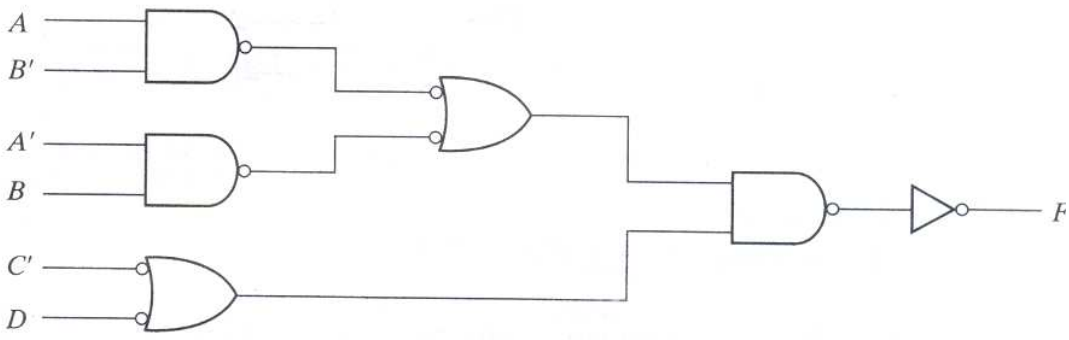
The NAD-OR implementation is shown in Fig 2 (a) with three levels of gating. The conversion into NAND with mixed notation is presented in part (b) of the diagram. The two additional bubbles associated with inputs C and D' cause these two literals to be complemented to C' and D. The bubble in the output NAND gate complements the output value, so we need to insert an inverter gate at the output in order to complement the signal again and get the original value.

NOR Implementation

The NOR operation is the dual of the NAND operation. Therefore, all procedures and rules for NOR logic are the dual of the corresponding procedures and rules developed for NAND logic. The NOR gate is another universal gate that can be used to implement any Boolean function. The implementation of the complement. OR, and AND operations with NOR gates is shown in Fig 3. The complement operation is obtained from a one-input NOR gate that behaves exactly like an inverter. The OR operation requires two NOR Gates and the AND operation is obtained with a NOR gate that has inverters in each input.



(a) AND-OR gates



(b) NAND gates

FIGURE 3-23
Implementing $F = (AB' + A'B)(C + D')$

The two graphic symbols for the mixed notation are shown in Fig 4. The OR-invert symbol defines the NOR operation as an OR followed by a complement. The invert-AND symbol complements each input and then performs and AND operation. The two symbols designate the same NOR operation and are logically identical because of DeMorgan's theorem

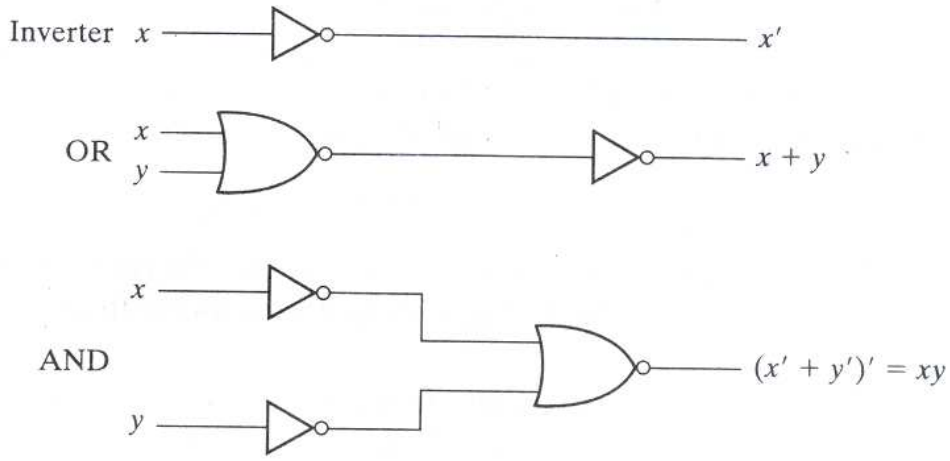


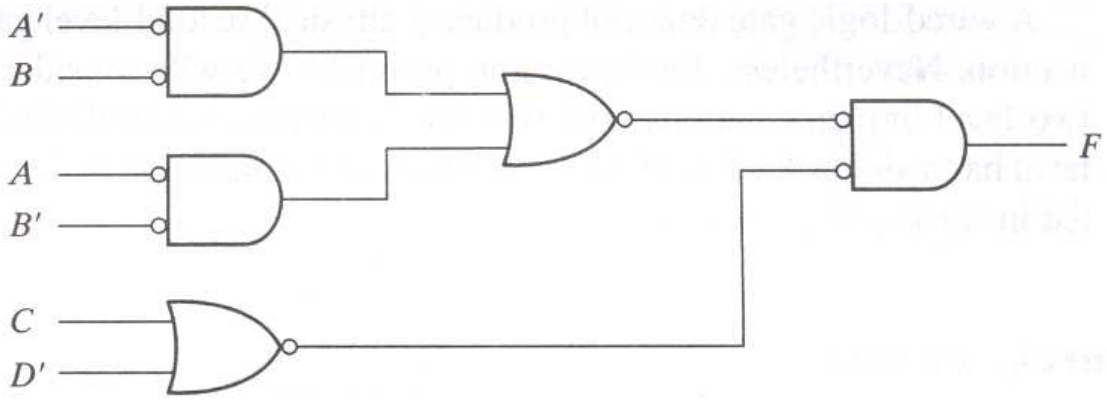
FIGURE 3-24
Logic Operations with NOR Gates

The procedure for converting a multilevel AND-OR diagram to an all NOR diagram is similar to the one presented for NAND gates. For the NOR case, we must convert each OR gate to an OR- invert symbol and each AND gate to an invert-AND symbol. Any bubble that is not compensated by another bubble along the same line needs an inverter or the complement of the input literal.

The transformation of the AND-OR diagram of Fig 2 (a) into a NOR diagram is shown in Fig 4. The Boolean function for this circuit is

F = (AB' + A'B)(C + D')

The equivalent AND-OR diagram can be recognized from the NOR diagram by removing all the bubbles. To compensate for the bubbles in four inputs, it is necessary to complement the corresponding input literals.


A′
B
A
B′
C
D′
F