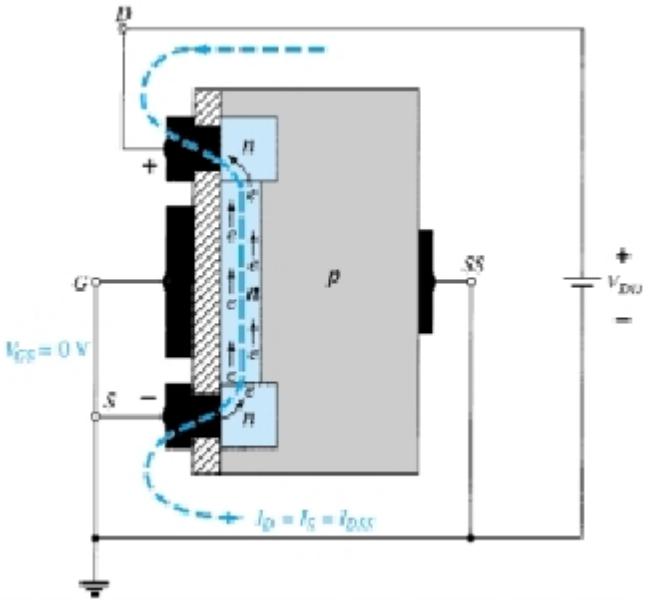
MOSFET

There are two types of FETs: JFETs and MOS-FETs. MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation, while the label MOSFET stands for metal-oxide-semiconductor-field-effect transistor. Since there are differences in the characteristics and operation of each type of MOSFET, they are covered in separate sections. In this section we examine the depletion-type MOSFET, which happens to have characteristics similar to those of a JFET between cutoff and saturation at IDSS but then has the added feature of characteristics that extend into the region of opposite polarity for VGS.

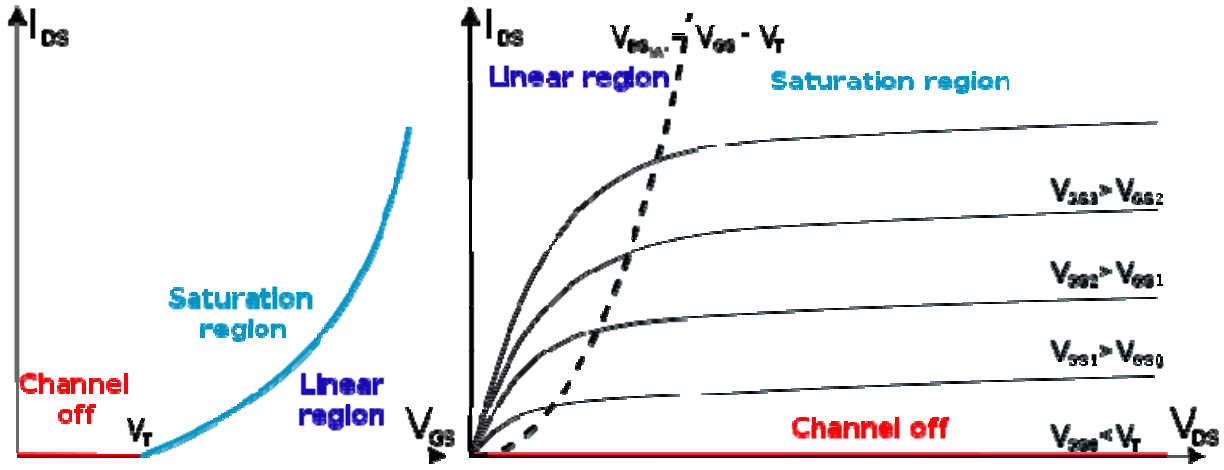
depleation type mosfet

Basic Operation and Characteristics

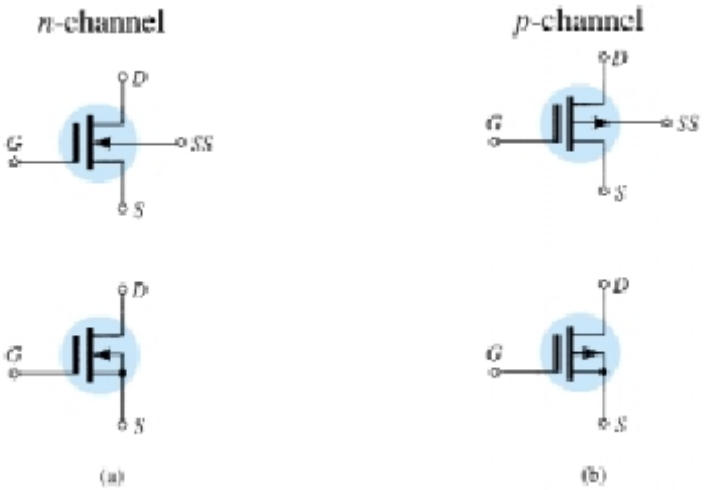
In the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage VDS is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the chan-nel of the JFET. In fact, the resulting current with VGS IDSS, as shown in Fig



VGS has been set at a negative voltage such as The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract) as shown in Fig. 5.26. Depending on the magnitude of the negative bias established by VGS, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher the rate of recombination. The resulting level of drain cur- rent is therefore reduced with increasing negative bias for VGS as shown in Fig.



SYMBOLS OF MOSFET



enhancement-type mosfet

Although there are some similarities in construction and mode of operation between depletion-type and enhancement-type MOSFETs, the characteristics of the enhance-ment-type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to-source voltage reaches a specific magnitude. In particular, current control in an n-channel device is now effected by a positive gate-to-source voltage rather than the range of negative voltages encountered for n-channel JFETs and n-channel depletion-type MOSFETs.

If VGS is set at 0 V and a voltage applied between the drain and source of the deviceof Fig. 5.31, the absence of an n-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion-type MOSFET and JFET where ID IDSS. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the n-doped regions) if a path fails to exist between the two. With VDS some positive voltage, VGS at 0 V,and terminal SS directly connected to the source, there are in fact two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source In Fig. 5.32 both VDS and VGS have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source.

The positive potential at the gate will pressure the holes (since like charges repel) in the p-substrate along the edge of the SiO2 layer to leave the area and enter deeper regions of the p-substrate, as shown in the figure. The result is a depletion region near the SiO2 insulating layer void of holes. However, the electrons in the p-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO2 layer. The SiO2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As VGS increases in magnitude, the concentration of electrons near the SiO2 surface increases until eventually the induced n-type region can support a measurable flow between drain and source. The level of VGS that results in the significant increase in drain current is called the threshold voltage and is given the symbol VT. On specification sheets it is referred to as VGS(Th), although VT is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent

with VGS=0V

Enhanced by the application of a positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET. Both depletion- and enhancement-type MOS-FETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.