AMPLIFIER DESIGN

Example-2 (Emitter-Resistor Amplifier Design)

Design an emitter-resistor amplifier as shown in fig. 2 to drive a 2 KΩ load using a pnp silicon transistor, V_{CC} = -24V, β = 200, A_v = -10, and V_{BE} = -0.7 V. Determine all element values and calculate A_i, R_{in}, I_{CQ} and the maximum undistorted symmetrical output voltage swing for three values of R_C as given below:

1. $R_C = R_{load}$
2. $R_C = 0.1\ R_{load}$
3. $R_C = 10\ R_{load}$

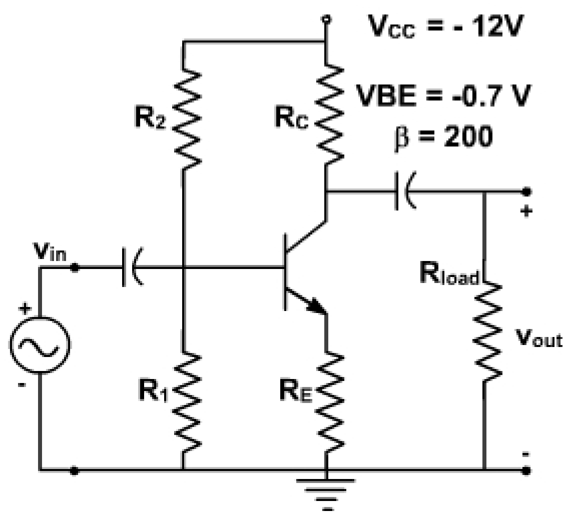

Fig. 2

Solution:

(a) $R_C = R_{load}$

We use the various equations derived in revious lecture in order to derive the parameters of the circuit.

From the voltage gain, we can solve for R'_E.

$$A_v = -10 = -\frac{R_{load} \| R_C}{r_e + R_E} = -\frac{2K\Omega \| 2K\Omega}{r_e + R_E}$$

So $R'_E = r_e + R_E = 100\ \Omega$

We can find the quiescent value of the collector current I_C form the collector-emitter loop using the equation for the condition of maximum output swing.

$$I_{CQ} = \frac{V_{CC}}{R_{dc} + R_{ac}} = -7.5\ mA$$

Therefore, $r_E' = \frac{25 \times 10^{-3}}{7.5 \times 10^{-3}} = 3.33\Omega$

This is small enough that we shall ignore it to find that $R_E = 100\ \Omega$. Since we now know β and R_E. We can use the design guideline.

$R_B = 0.1\ \beta\ R_E = 2\ k\ \Omega$

As designed earlier, the biasing circuitry can be designed in the same manner and given by

$V_{BB} = -1.52$ V

$R_1 = 2.14$ K Ω

$R_2 = 3.6$ K Ω

The maximum undistorted symmetrical peak to peak output swing is then

V_{out} (P-P) = 1.8 I_{CQ} ($R_{load} \| R_C$) = 13.5 V

Thus current gain $A_i = -9.1$

and input impedance $R_{in} = 1.82$ K Ω

(b) $R_C = 0.1\ R_{load}$

we repeat the steps of parts (a) to find

R_C =200 Ω	R_i = 390 Ω
I_{CQ} =-57.4 mA	R_2 =4.7K Ω
r'_e = 0.45 Ω	v_{out}(p-p) = 18.7 V
R_B = 360 Ω	A_i = -1.64
V_{BB} = -1.84 V	R_{in} = 327 Ω

(C) R_C =10 R_{load}

Once again, we follow the steps of part (a) to find

R_C =20 K Ω	R_1 =3.28K Ω
I_{CQ} =-1.07 mA	R_2 = 85.6K Ω
r'_e = 24.2 Ω	v_{out}(p-p) = 3.9 V
R_B = 3.64K Ω	A_i =-14.5
V_{BB} = -0.886 V	R_{in} = 2.91K W

We now compare the results obtained Table-I for the purpose of making the best choice for R_C.

	I_{CQ}	A_i	R_{in}	v_{out}(p-p)
$R_C = R_{load}$	-7.5 mA	-9.1	1.82K W	13.5 V
$R_C = 0.1\ R_{load}$	-57.4 mA	-1.64	327 W	20.8 V
$R_C = 10\ R_{load}$	-1.07mA	-14.5	2.91W	3.9 V

Table - 1 Comparsion for the three selections of R_C

It indicates that of the three given ratios of R_C to R_{load}, $R_C = R_{load}$ has the most desirable performance in the CE amplifier stage.

It can be used as a guide to develop a reasonable designs. In most cases, this choice will provide performance that meets specifications. In some applications, it may be necessary to do additional analysis to find the optimum ratio of R_C to R_{load}.