Successive approximation ADC

Most Commonly used in medium to high speed Converters Based on approximating the input signal with binary code and then successively revising this approximation until best approximation is achieved SAR (Successive Approximation Register) holds the current binary value.

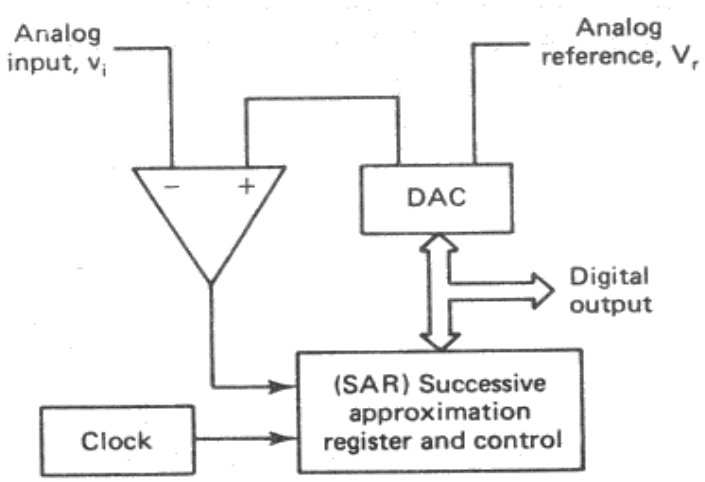

Figure 5.8

The successive approximation Analog to digital converter circuit typically consists of four chief sub circuits:

1. A sample and hold circuit to acquire the input voltage (V_{in}).
2. An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR).
3. A successive approximation register sub circuit designed to supply an approximate digital code of V_{in} to the internal DAC.
4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with V_{in}.

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC).

Mathematically, let $V_{in} = xV_{ref}$, so x in [-1, 1] is the normalized input voltage. The objective is to approximately digitize x to an accuracy of $1/2^n$. The algorithm proceeds as follows:

1. Initial approximation $x_0 = 0$.
2. ith approximation $x_i = x_{i-1} - s(x_{i-1} - x)/2^i$.

Where, s(x) is the signum-function(sgn(x)) (+1 for $x \geq 0$, -1 for $x < 0$). It follows using mathematical induction that $|x_n - x| \leq 1/2^n$.

As shown in the above algorithm, a SAR ADC requires:

1. An input voltage source V_{in}.
2. A reference voltage source V_{ref} to normalize the input.
3. A DAC to convert the ith approximation x_i to a voltage.
4. A Comparator to perform the function $s(x_i - x)$ by comparing the DAC's voltage with the input voltage.
5. A Register to store the output of the comparator and apply $x_{i-1} - s(x_{i-1} - x)/2^i$.