LDIC Applications Unit6

## **CMOS**

## **CMOS:-**

MOSFET's are two types

- 1. N channel mosfet
- 2. P channel mosfet

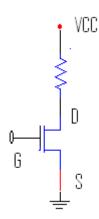


Figure 6.14

It is used a on off condition switch. If the voltage at gate is more than the source voltage then it is called as on switch

If the gate voltage is less than the source voltage then it is simply acts as a off switch

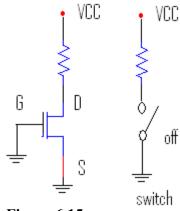


Figure 6.15

## **CMOS INVERTER**

In MOSFET the source and drain can be interchanged. CMOS means complementary metal oxide semi conduction, complementary it contains both P channel MOSFET & N channel

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MOSFET, if P channel is in off condition then N channel is in on state & vice versa, P channel MOSFET are called as pull up transistor

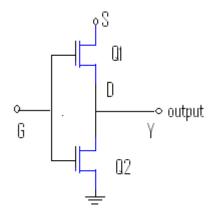


Figure 6.16

V<sub>CC</sub> is applied to the MOSFET. Bcoz it pulls the output to the high level.

When A = 1,  $Q_1$  is OFF, &  $Q_2$  is ON, the output is pulled to low level, the output is directly connected to ground with ON resistance of  $Q_2$ , output, Y = 0.

When A = 0,  $Q_1$  is ON, &  $Q_2$  is OFF then Y = 1 (since output is pulled up to high level through ON resistance

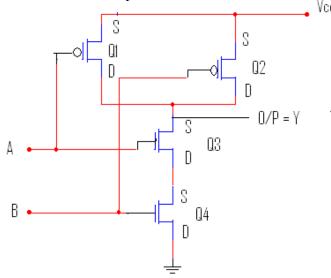
The ON resistance of any transistor i.e, CMOS transistor is low when logic output is zero when compared to the logic output high  $(Q_1 \text{ is more than } Q_2)$ 

## **CMOS NAND gate:**

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 $Q_1 \& Q_2$  are P channel MOSFETS  $\rightarrow$  pull up transistors

 $Q_3 \& Q_4$  are N channel MOSFETS  $\rightarrow$  pull down transistors



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**Figure 6.17** 

A	В	$Q_1$	$Q_2$	$Q_3$	$Q_4$	OUTPUT
0	0	ON	ON	OFF	OFF	HIGH
0	1	ON	OFF	OFF	ON	HIGH
1	0	OFF	ON	ON	OFF	HIGH
1	1	OFF	OFF	ON	ON	HIGH

When the both inputs are low the both the transistor  $Q_1,Q_2$  is in ON state &  $Q_3$  &  $Q_4$  is in OFF state then the output is pulled up to high level through the ON resistance of  $Q_1$  &  $Q_2$  in parallel. For the data inputs A = 0 & B = 1 the transistor  $Q_1,Q_4$  is in ON state &  $Q_2,Q_3$  are in OFF state then the output is pulled up to high level through the ON resistance of  $Q_1$ .

When the data output's are A = 1 & B = 0 then the transistor  $Q_2, Q_3$  is in ON state &  $Q_1, Q_4$  are in OFF state then the output is pulled up to high level through the ON resistance of  $Q_2$ .

For the data A = 1 & B = 1 the transistor  $Q_1$ ,  $Q_2$  is in OFF state &  $Q_3$ ,  $Q_4$  are in ON state. Therefore the output is directly connected to ground with the ON resistance of  $Q_3$ ,  $Q_4$  in series so output is low.