CMOS NOR gate, open drain COMOS gate & CMOS Tri State (BUFFER)

CMOS NOR GATE :

A	B	Q_1	Q_2	Q_3	Q_4	OUTPUT
0	0	ON	ON	OFF	OFF	HIGH
0	1	ON	OFF	OFF	ON	LOW
1	0	OFF	ON	ON	OFF	LOW
1	1	OFF	OFF	ON	ON	LOW

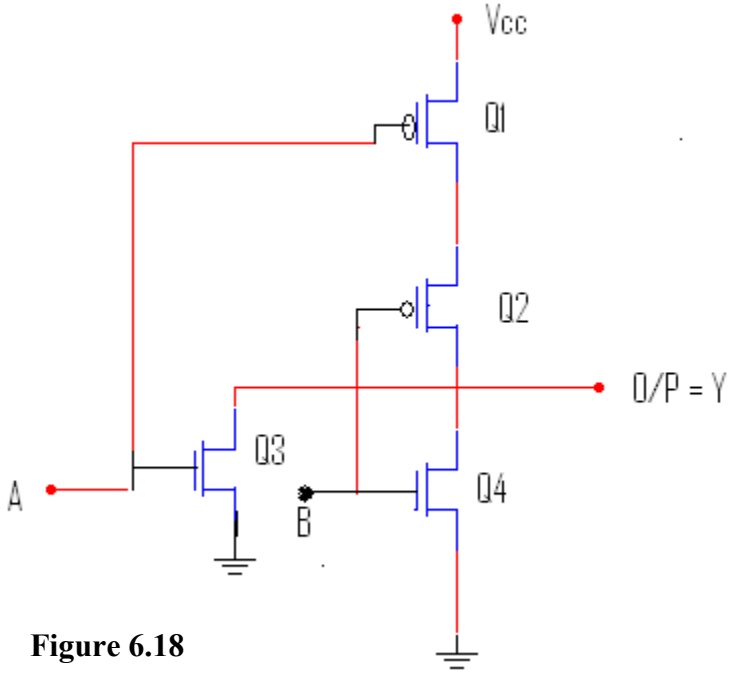


Figure 6.18

When data input's A = 0 & B = 0 then Q_1,$Q_2$is in ON state & Q_3,Q_4 are in OFF state, then the output is pulled up to high level through the ON resistance of Q_1 &Q_3 in series.

For A = 0 & B = 1 then Q_1,$Q_4$is in ON state & Q_2,Q_3 are in OFF state. Then the output is directly connected to ground with the ON resistance of Q_4. So output is low.

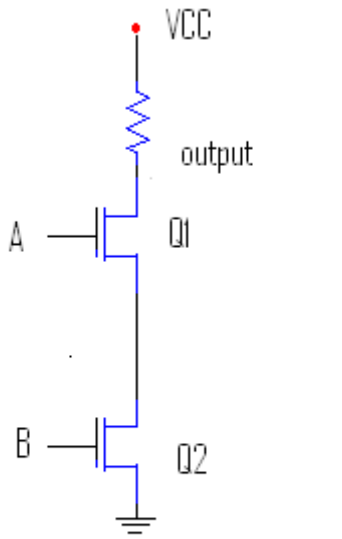
For A = 1 & B = 0 then Q_2,$Q_3$is in ON state & Q_1,Q_4 are in OFF state. Then the output is directly connected to ground with the ON resistance of Q_3. So output is low

For A = 1 & B = 1 then Q_1,$Q_2$is in OFF state & Q_3,Q_4 are in OFF state. Then the output is directly connected to ground with the ON resistance of Q_4 & Q4 in parallel.

OPEN DRAIN COMOS GATE:

A	B	Q_1	Q_2	OUTPUT
0	0	OFF	OFF	HI-Z(open)
0	1	OFF	ON	HI-Z(open)
1	0	ON	OFF	HI-Z(open)
1	1	ON	ON	LOW

Hi-Z high Impedance:



open drain cmos NAND gate

Figure 6.19

For the to pull the up the output to the high level you should connect an external resistor in B'n V_{CC} and open drain output. The choice of resistance value should be minimum for high speed switching action reduces the propagation delay during less on ON & OFF condition

However the resistance value cannot be arbitrarily small, the minimum resistance value is determined by the open drain output's maximum sink current (Ia max)

For HC,HCT IOL Max = 4 ma HC = High Speed CMOS

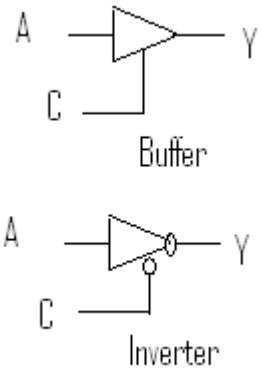
If resistance further to I_{OL} Max which may damage the transistor

Tri State CMOS:

The CMOS transistor buffer (or) Inverter outputs having two normal states low and high. Corresponding to the logic level.

However some times output have a third electrical state which is not a logic state at all called high impedance state (or) Hi-Z or floating state

Y = A when C is high



V = high impedance C is low

Y = A1 when C is low

V = high impedance C is high

Figure 6.20

An output with three possible states is called 3- state output (or) sometimes tri state output. Three state devices have an external input called control input

CMOS Tri state (Buffer):

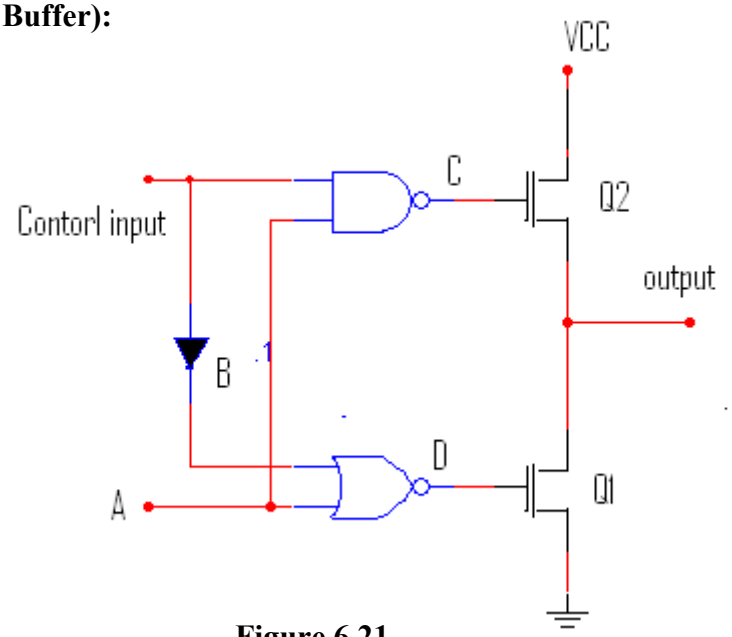


Figure 6.21

NAND gate has 4 transistor NOR gate has 4 transistor so totally to transistors actually in place of NAND & NOR gates, we have draw with transistor circuit

Control Input	A	B	C	D	Q_1	Q_2	OUTPUT
low	low	high	high	high	off	off	Hi-z
low	high	high	high	low	off	off	Hi-z
high	low	low	high	high	off	on	low
high	high	low	low	low	on	off	high

Whenever the control input is low, low is applied to NANDA for NAND any one of the input is low output is high, so C is high, Bis complement of control input so B is high. A & B are input's for NOR gate so for A = low, B = high, the NOR gate output is low i. e, D is low, and also C is high, i. e, Q_1 is off & D is low Q_2 off. In tri state condition Q1, Q2 are of then the output is Hi-z

Similarly second case whenever the control input is high→ B = low & A is low then D is high→ C is high, then Q_1 off & Q_2 on so output is low. Therefore is a path for output to ground)

Similarly when C input is high → B = low & A is high then D is low → C is low, then Q_1 on & Q_2 off then the VCC has a path for output is a path for V_{CC} . So output is high

Then it is acting as a tri state buffer with outputs low, high & high

Application of open drain CMOS:-

1. To drive the lamp and led
2. To control wired logic function
3. To construct the common Bus

Common bus is always connected to High-z output case only whenever the control input is low i. e, control input is d then CMOS tri state buffer give Hi-z output. If the two tri state output's on the same bus are enabled try to maintain opposite state, then it will produce a non logic voltage, Non logic voltage means from low voltage some voltage is provided i.e, it produces noise pulses that effects the circuit. However the leakage current in high impedance tri state output is very small so that more no. of high impendence output can be connected to form a common bus.