TTL Logic family

TTL Logic family: According to the output configuration TTL logic family is divided into three types

1. Open collector output TTL
2. Totem pole output TTL (standard TTL)
3. Tri state output TTL
4. Schotty TTL

1. Open Collector TTL:

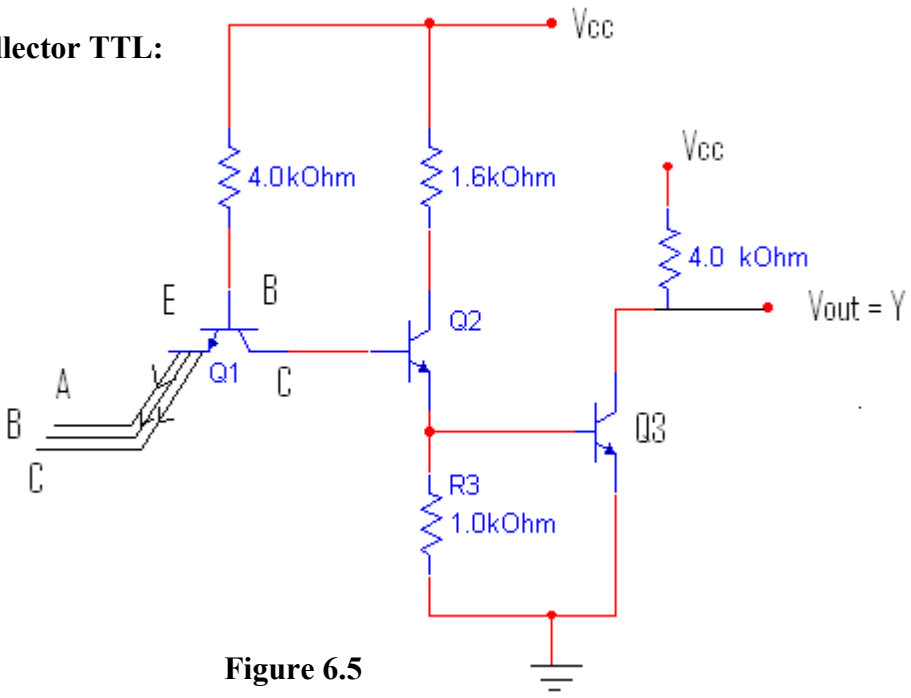


Figure 6.5

The internal construction of 3-emitter transistor

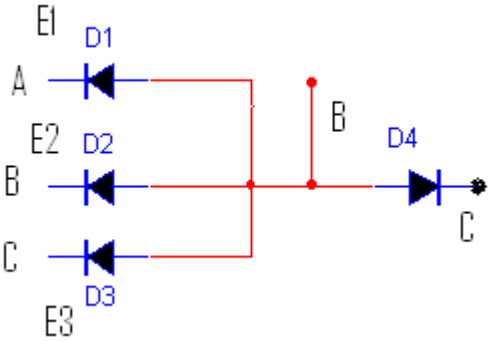


Figure 6.6

When ever the Ban voltage is more than that of emitter voltage then only transistor is in on condition or else off condition for this type of N gate, input ranges from 0 to 0. 2V logic level " 0" and for logic level "1" the input ranges from 2 . 4 to 5 V.

External resistor is also called as pull up resistor NAND gate means. If any one input is low, the output is high scale. If all the inputs are high, then the output is low state

From the fig(b) if the Base voltage is 0.7V more than that of the emitter voltage of then Base to emitter junction is forward bias, either wise it is in reverse bias.

For NAND

If any one input is low (0.2)v then base to emitter junction is forward Bias, then the voltage at the base of the transistor Q1 is 0.9 V (0. 2 V for low level input the diode drop (D_1) 0. 7 V = 0.2 + 0.7 = 0.9 V). In order to conduct the transistor Q2, Q3. The required voltages is 2.1 (one diode drop (D_4 = 0. 7) + "2" V_{BE} drops (i.e, 2(0.7) = 2.1 V).

So that the transistor Q_2 and Q_3 is off state if any external resistance (4kΩ) is B'n power supply V_{CC} and Collector of transistor Q_3, then the output is pulled to high level. The external resistor R is also called pull up Resistor it is used to pull up voltage from o0 to high level)

If all the inputs are high then base to emitter junction is reverse bias all in condition which makes Q_2 & Q_3 into saturation i. e, at the base of Q_1 sufficient voltage is presented (i. e, V_{CC} = 15) to drive the transistors Q_2 & Q_3. When Q_3 is in saturation state then the output is low level.

This confirms the operation of NAND gate

$$\left.\begin{matrix} Base\ to\ Emitter\ FB \\ Base\ to\ Collector\ RB \end{matrix}\right\} active\ \text{Re}\ gion$$

During the transition on and off condition the transistor Q_1 exhibits transistor action (active region). Results in reduction is propagation delay. If all are high the transistor Q_3 is entered into saturation level after that if any one input is brought into low level then the transistor Q_2 is in cut off region, then the transistor Q_1 acts as a active region transistor. The Collector current in the transistor Q_1 quickly removes the excess charges presented in the previous saturated state.

In this way the propagation delay is reduced by using multiple emitter type transistors.

Application: (open Collector TTL)

1. To drive the lamp
2. Perform the wired logic function
3. Construction of a Common Bus

Without using the external resistor, the output of open collector, TTL can be connected as input to the other TTL gates. The open collector output behaves like high level data input for the other TTL gates

1.To drive the lamp: When the transistor Q_3 is on (i.e in saturation state if you place the lamp on the output path of the transistor Q_3 the current has path that will turns on the lamp. If the transistor Q_3 is in cut off the current has no path to flow then it will turn of the lamp.

2. Perform the wired logic function: Fig

$Y = (AB)^1 (CD)^1 = (AB+CD)^1$

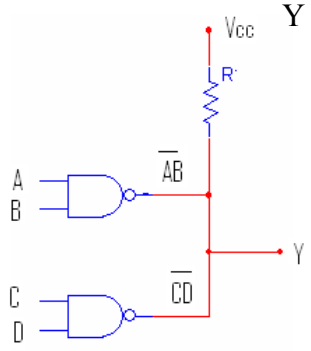


Figure 6.7

If the open collector output TTL gates are connected or tighted together then it behaves like a AND gate

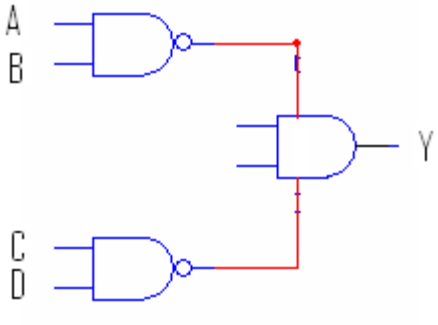
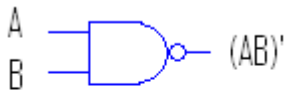


Figure 6.8

Open Collector TTL family:



Open collector NAND gate

3.Construction of a Common Bus:

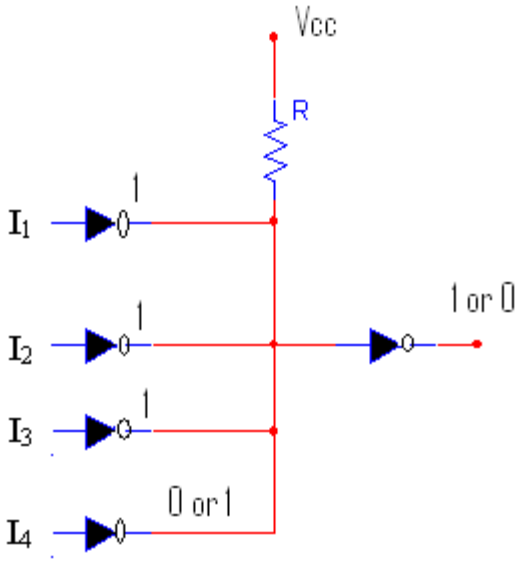


Figure 6.9

Bus is provides path for 0 or 1 transmission. The open collector output TTL'S gates can be tighted together to form a common bus. At any time all the gate outputs tight to the bus, except 1 must be maintained in their high states. The selected gates in the high or low state depending on want to transmit either 0 or 1