Performance Characteristics

Performance Characteristics:

1) Propagation delay Fan out
2) Dc supply voltage
3) Input and output logic levels
4) Power dissipation
5) Noise margin
6) Speed power product

Propagation delay:-

The time takes to propagate from input side to output side in a single logic. That time takes is called propagation delay. It is a transition delay time for the signal to propagate from input to output. If several number of gates are present then it is called total delay time.

It is the time B'n specified reference point on the input waveform and corresponding reference point on the output waveform when output waveform charges from high to low level

tp_{HL} = propagation logic from low to high level

It is the time B'n specified reference point on this input waveform and corresponding reference on the output waveform when output waveform changes from low to high level.

Logic families	Propagation delay
Standard TTL gate	11n sec
Fast TTL	3.3n Sec
HCT	7n sec
AC CMOS	5n sec
ALVC	3n sec
ECL	0.22n sec

Fan out: Fan out of a gate specifies number of standard loads that can be connected to the output of the gate without degrading in performances.

Ex:-

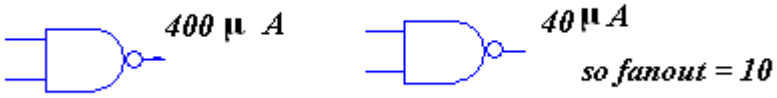

Figure 6.1

It mainly depends on the amount of current available in the output of the gate and the amount of current reached in each input of the gate

Fan out for TTL is 10

For CMOS fan out is more than 10

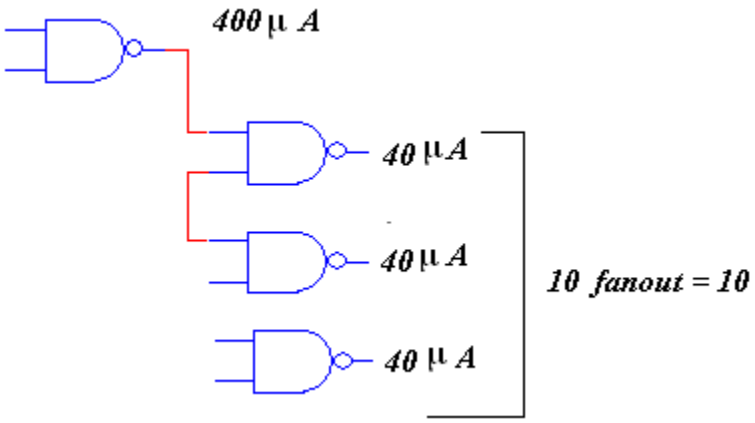

Figure 6.2

DC Supply Voltages:

A 5V CMOS → Can tolerate supply variation from 2V to 6V

A 3V CMOS → It can tolerate supply variation from 2V to 3. 6V

TTL requires 5V dc supply voltage and it can tolerate the supply variation from 4.5V to 5.5V dc supply

Power dissipation: It is the product of dc supply voltage and an average supply current. The average supply current is varies according to the output of the logic gate.

ICCL → Supply current when output is low

ICCH → Supply current when output is high

Input and output logic levels:

V_{IL}= low level input voltage

V_{IH}=High level input voltage

V_{OL}= low level output voltage

V_{OH}= low level output voltage

	Input logic level		output logic level	
	Low	**high**	**low**	**high**
5V CMOS	0 to 1.5V	3.5 to 5V	0 to 0.33v	4.4 to 5V
3VCMOS	0 to 0.8V	2 to 3.3V	0 to 0.4V	2.4 to 3.3V
TTL	0 to 0.8V	2 to 5V	0 to 0.4V	2.4 to 5V

Diagrammatic Representation

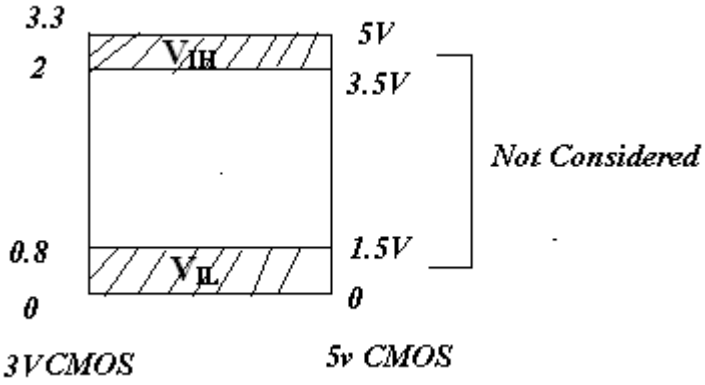

Figure 6.3

Noise Margin:

It is a unwanted voltage signal which is produced as induced in electric circuit which the output and that change the proper operation of the circuit it must be avoided. How much noise is allowed is called noise immunities and circuit. The measure of circuit Noise Immunity is called as Noise margin which is expressed is volts. In order net to be effected by the noise the logic circuit must have certain amount of Noise immunity

V_{NL}= low level Noise Margin

V_{NH}=High level Noise Margin

$$V_{NH} = (V_{NH})_{\min} - (V_{IH})_{\min}$$
$$V_{NL} = (V_{IL})_{\max} - (V_{OL})_{\max}$$

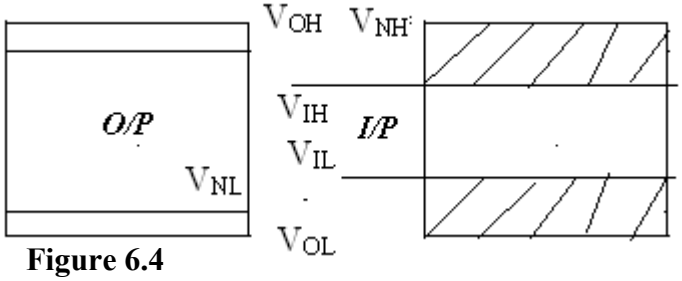

Figure 6.4

For CMOS V_{NH}= 0.9V, V_{NL}= 1.17V

For TTL V_{NH}= 0.4V, V_{NL}= 0.4V

Speed Power Product: It is the product of propagation delay time and power dissipation and is expressed in joules SPP = td.Pd