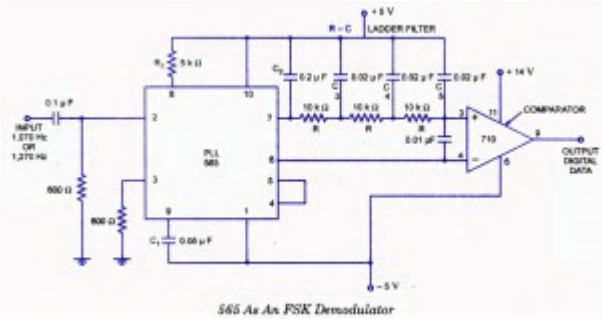
AM, FM & FSK Demodulators

A very useful application of the 565 PLL is as a FSK demodulator. In the 565 PLL the frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the logic 0 and logic 1 states of the binary data signal. The frequencies corresponding to logic 1 and logic 0 states are commonly called the *mark* and *space* frequencies. Several standards are used to set the mark and space frequencies.

An FSK signal demodulator can be built as illustrated in figure. The demodulator receives a signal at one of the two distinct carrier frequencies, 1,270 Hz or 1,070 Hz representing the RS-232 C logic levels of mark (- 5 V) or space (+ 14 V), respectively. Capacitance coupling is used at the input to remove a dc level. As the signal appears at the input of 565 PLL, the PLL locks to the input frequency and tracks it between the two possible frequencies with a corresponding dc shift at the output. Resistor R_1 and capacitor C_1 determine the free-running frequency of the VCO. Capacitor C_2 is a loop filter capacitor that establishes the dynamic characteristics of the demodulator. Capacitor C_2 is chosen smaller than usual one to eliminate overshoot on the output pulse. A three-stage RC ladder filter is employed for removing the sum frequency component from the output. The VCO frequency is adjusted with R_1 so that the dc voltage level at the output (pin 7) is the same as that at pin 6. An input at frequency 1,070 Hz drives the demodulator output voltage to a more positive voltage level, driving the digital output to the high level (space or + 14 V). An input at 1,270 Hz correspondingly drives the 565 dc output less positive with the digital output, which then drops to the low level (mark or – 5 V).



565 As An FSK Demodulator

Figure 4.11