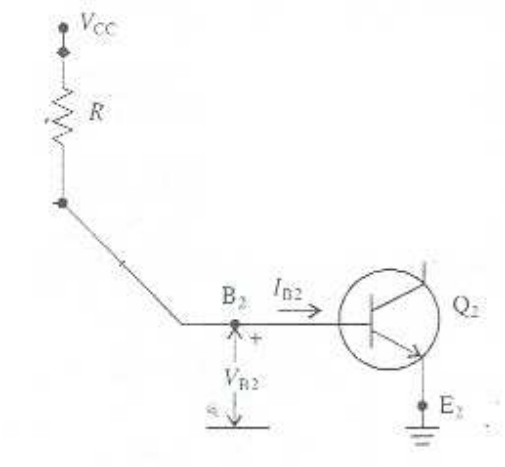
Design of Monostable Multivibrator:

Circuit diagram is shown below.

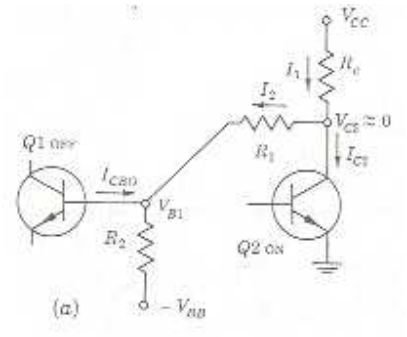
This circuit is not symmetrical . so here we need to consider both states of the device.

We know initial state of the device is

Q1 OFF & Q2 ON (Stable state)



Collector circuit of Q2 Base circuit of Q2



Since For DC analysis capacitors are replaced with an open circuit.

To keep Q1 is in OFF state , $V_{BE1} < V_{BE(cutoff)}$

From the collector circuit of Q2 , $V_{BE1} = V_{BE1}$ due to $V_{CE(sat)} + V_{BE}$ due to $-V_{BB}$

V_{BE1} due to $V_{CE(sat)} = \frac{V_{CE(sat)} R_2}{R_1 + R_2}$

V_{BE1} due to $- V_{BB} = \frac{-V_{BB} R_1}{R_1 + R_2}$

$$V_{BE1} = \frac{-V_{BB} R_1}{R_1 + R_2} + \frac{V_{CE(sat)} R_2}{R_1 + R_2}$$

So $$\frac{-V_{BB}R_1}{R_1+R_2}+\frac{V_{CE(sat)}R_2}{R_1+R_2} < V_{BE(cutoff)} \text{ ------- (1)}$$

To keep Q2 is in ON state, $I_{B2} \geq I_{B2(\min)}$

Where $$I_{B2(\min)} = \frac{I_{C2}}{h_{FE}}$$

From the collector circuit of Q2 , $I_{C2} = I_1 - I_2$

$$I_{C2} = \left(\frac{V_{CC}-V_{CE(sat)}}{R_C}\right) - \left(\frac{V_{CE(sat)}-(-V_{BB})}{R_1+R_2}\right)$$

$$I_{B2(\min)} = \frac{1}{h_{FE}}\left(\left(\frac{V_{CC}-V_{CE(sat)}}{R_C}\right) - \left(\frac{V_{CE(sat)}-(-V_{BB})}{R_1+R_2}\right)\right) \text{--------(2)}$$

From the base circuit of Q2 ,

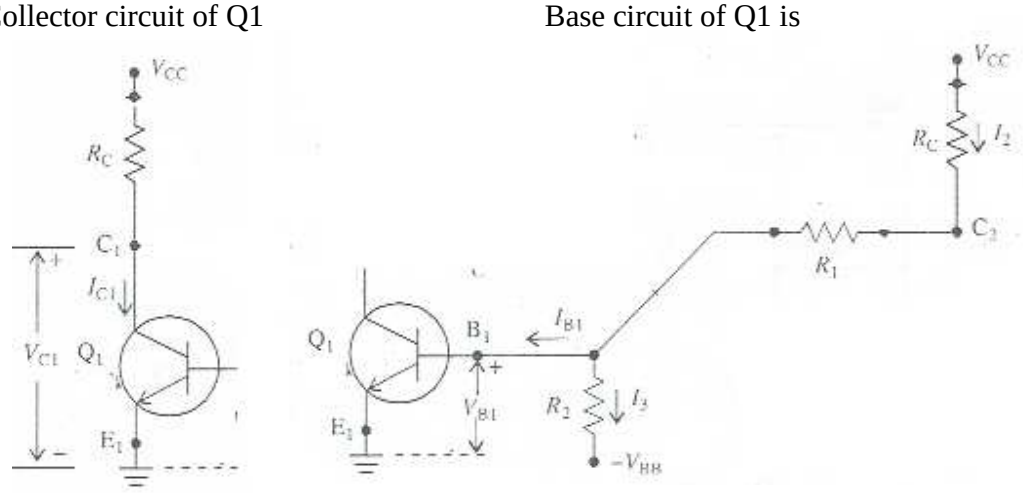
$$I_{B2} = \left(\frac{V_{CC}-V_{BE(sat)}}{R}\right)$$

Therefore, we know the necessary condition to keep the transistor in ON state is

$$\left(\frac{V_{CC}-V_{BE(sat)}}{R}\right) \geq \frac{1}{h_{FE}}\left(\left(\frac{V_{CC}-V_{CE(sat)}}{R_C}\right) - \left(\frac{V_{CE(sat)}-(-V_{BB})}{R_1+R_2}\right)\right) \text{--(3)}$$

Other state of the monostable multivibrator is Q1 ON & Q2 OFF (Quasi stable state)

Collector circuit of Q1 Base circuit of Q1 is



To keep Q1 is in ON state, $I_{B1} \geq I_{B1(\min)}$

Where $$I_{B1(\min)} = \frac{I_{C1}}{h_{FE}}$$

From the collector circuit of Q1 ,

$$I_{C1} = \left(\frac{V_{CC} - V_{CE(sat)}}{R_C} \right)$$

$$I_{B1(\min)} = \frac{1}{h_{FE}} \left(\frac{V_{CC} - V_{CE(sat)}}{R_C} \right)$$

From the base circuit of Q1 , $I_{B1} = I_2 - I_3$

$$I_{B1} = \left(\frac{V_{CC} - V_{BE(sat)}}{R_C + R_1} \right) - \left(\frac{V_{BE(sat)} - (-V_{BB})}{R_2} \right)$$

Therefore, we know the necessary condition to keep the transistor in ON state is

$$\left(\frac{V_{CC} - V_{BE(sat)}}{R_C + R_1} \right) - \left(\frac{V_{BE(sat)} - (-V_{BB})}{R_2} \right) \geq \frac{V_{CC} - V_{CE(sat)}}{R_C h_{FE}} \quad \text{----(4)}$$

Here there is no need to check the status of Q2 since voltage at base terminal of Q2 varies

From time to time(this is not a fixed value).

Capacitor value should be selected from $T = 0.693\ RC$ -----(5)

Component values should be selected to satisfy equations (1),(2),(4) & (5)