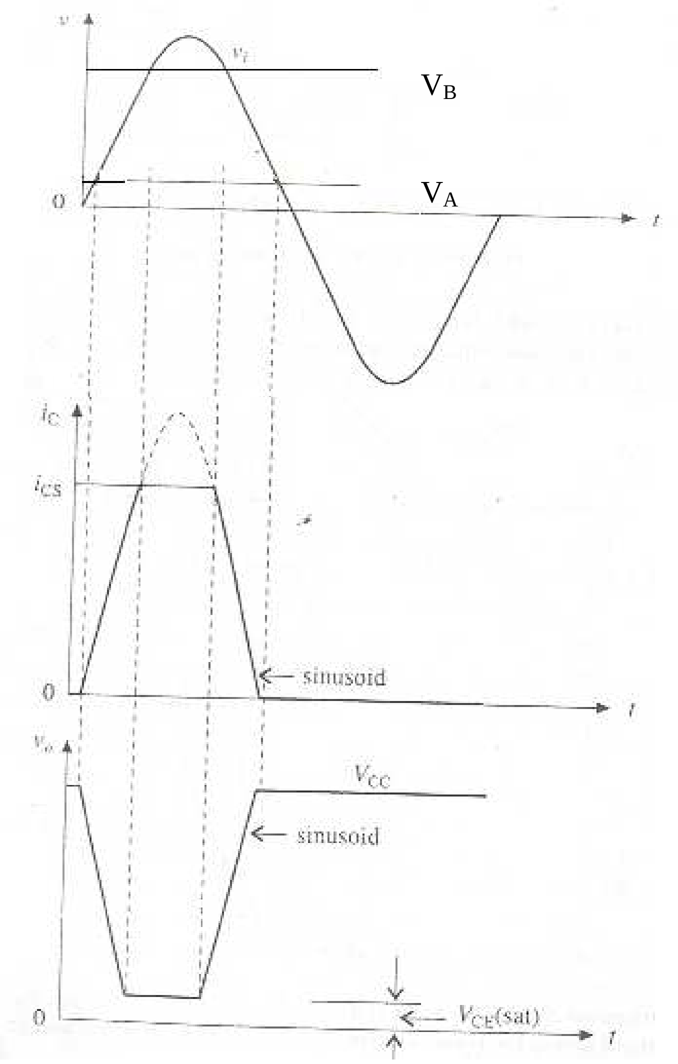
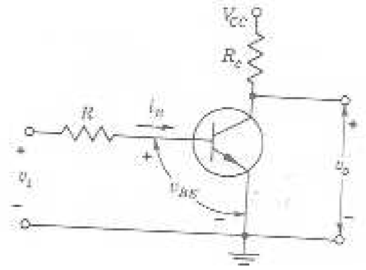
transistor clippers:

here circuit diagram is shown below,

consider input voltage is sufficient to drive the transistor from cutoff to saturation(through active region).





Assume that if $V_i < V_A$, transistor is in cutoff region

And if $V_i > V_B$, transistor is in saturation region

And also if $V_A < V_i < V_B$, transistor is in active region.

We know for the given circuit $V_o = V_{CC} - I_C R_C$

Case(i) : if $V_i < V_A$, transistor is in cutoff region.

So $I_C = 0$ mA then $V_o = V_{CC}$

Here signal below the level V_A is clipped.

Case(ii): if $V_i > V_A$, transistor is in saturation region.

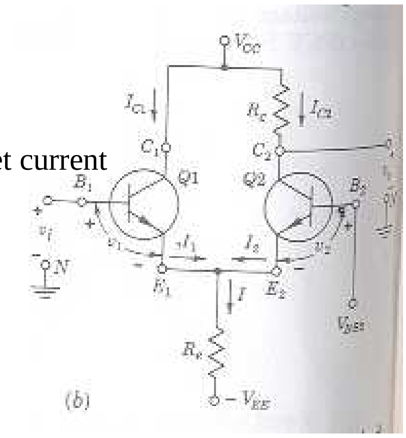
So $I_C = V_{CC} - V_{CE(sat)} / R_C$ then $V_o = V_{CE(sat)}$

Here signal above the level V_B is clipped

Case(iii) : if $V_A < V_i < V_B$, transistor is in active region
We know in active region output follows input but
With 180 degrees phase shift.

Emitter coupled clipper : to get zero phase shift between input and output voltage waveforms there is a need of emitter coupled clipper.

Circuit diagram for emitter coupled clipper is shown below,



Operation :

Assume that due to the biasing voltages(V_{CC} , V_{BB2} , $-V_{EE}$) net current flowing through the resistor Re is constant.

Means $I = I_1 + I_2$ = constant
(in the absence of input signal)

Then $V_E = I R_e - V_{EE}$ is also constant (positive).
And we know $V_o = V_{CC} - I_{C2}R_C$

Case(i) : if V_i is small(negative) , then Q1 is in

cutoff region(OFF) And Q2 is in active region(ON)

so here I_2 is maximum and I_1 is negligible. Then
I_{C2} is high so V_o is constant low voltage.

Case(ii): if V_i increases ,both transistors are in active region.
Then output follows input.

$$V_o = V_i$$

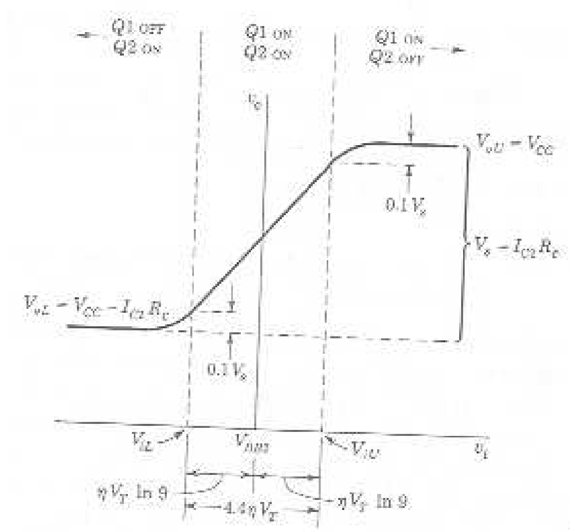
In this region , I_1 will increase and I_2 will decrease

So as V_i increases V_o is also increases.

Case(iii): if V_i is large value , Q2 is in cutoff region(OFF) And Q1 is in active region(ON)

so here I_1 is maximum and I_2 is negligible. Then I_{C2} is low so V_o is constant high voltage.

Transfer characteristics:



EXPRESSION FOR ΔV_i :

from the transfer characteristics , $\Delta V_i = V_{iu} - V_{il}$ ------------(1)

.

by applying KVL to the input and output loops of above circuit diagram,

$V_i - V_1 + V_{EE} - I\,Re = 0$ ----------(2)

$V_{BB2} - V_2 + V_{EE} - I\,Re = 0$ ----------(3) , where V_1 and V_2 are voltage across the emitter junctions of both the transistors.

From equations (2) &(3) , $V_i = V_{BB2} + V_1 - V_2$ ----------(4)

From Ebers and moll equation voltage across the emitter junction is ,

$V_E = \eta V_T \ln [1 - [(I_E + \alpha_I I_C)/ I_{EO}]]$ -----(5)

Where α_I is inverted common base current gain
I_{EO} is emitter junction reverse saturation current

Generally , I_E is approximately equals to I_C , now equation (5) will becomes (by neglecting 1, because I_E is large)

$V_E = \eta V_T \ln [- [I_E (1+ \alpha_I)/ I_{EO}]]$

Now for Q1 , $V_1 = \eta V_T \ln [- [I_1 (1+ \alpha_I)/ I_{EO}]]$

And for Q2 , $V_2 = \eta V_T \ln [- [I_2 (1+ \alpha_I)/ I_{EO}]]$

So $V_1 - V_2 = \eta V_T \ln [I_1 / I_2]$

From equation (4) , $V_i = V_{BB2} + \eta V_T \ln [I_1 / I_2]$ --------(6)

We know if $V_i = V_{iu}$, then Q1 ON and Q2 OFF . here I_1 will dominates I_2
So consider $I_1 = 0.9\ I$ and $I_2 = 0.1\ I$

From equation(6) , $V_{iu} = V_{BB2} + \eta V_T \ln [9]$

Similarly, if $V_i = V_{il}$, then Q1 OFF and Q2 ON . here I_2 will dominates I_1
So consider $I_2 = 0.9\ I$ and $I_1 = 0.1\ I$

Then $V_{il} = V_{BB2} + \eta V_T \ln [1/9]$

From equation(1) , $\Delta V_i = 4.4\ \eta V_T$