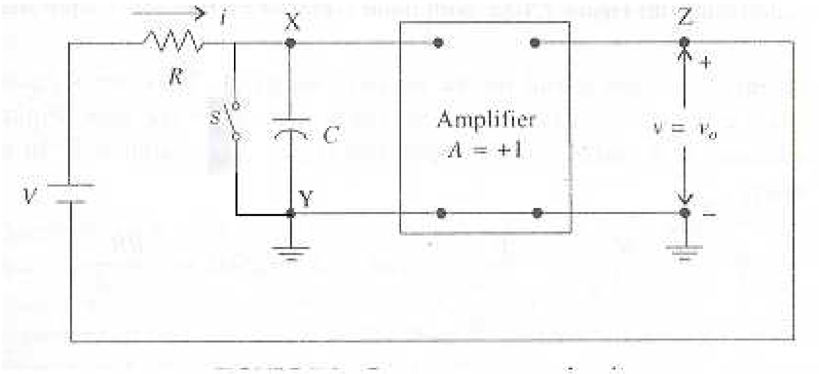
Transistor Bootstrap Time Base Generator:

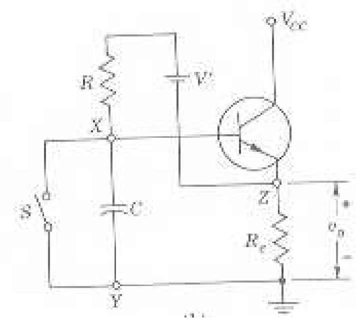
To get transistor version of bootstrap time base generator consider basic bootstrap time base generator once again.

basic bootstrap time base generator is shown below,



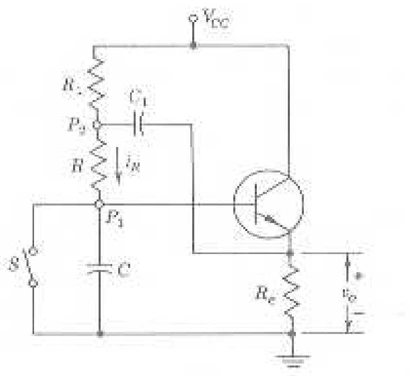
Here we need an amplifier with unity gain. We know CC amplifier offers unity gain.

Now by replacing amplifier with an emitter follower ,the circuit diagram is redrawn as shown below.



The practical disadvantage of above figure is that neither side of the supply V is grounded. This difficulty may be remedied by replacing V with a charged capacitor C_1.

This capacitor is charged through a resistor R_1, as indicated in the figure below.

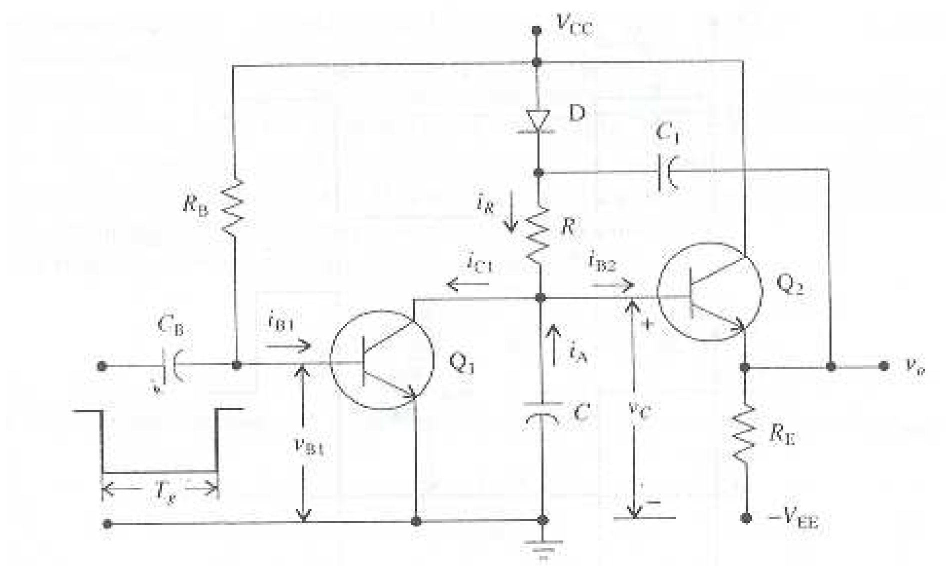


In the above we can replace switch with a transistor Q_1 as shown below.

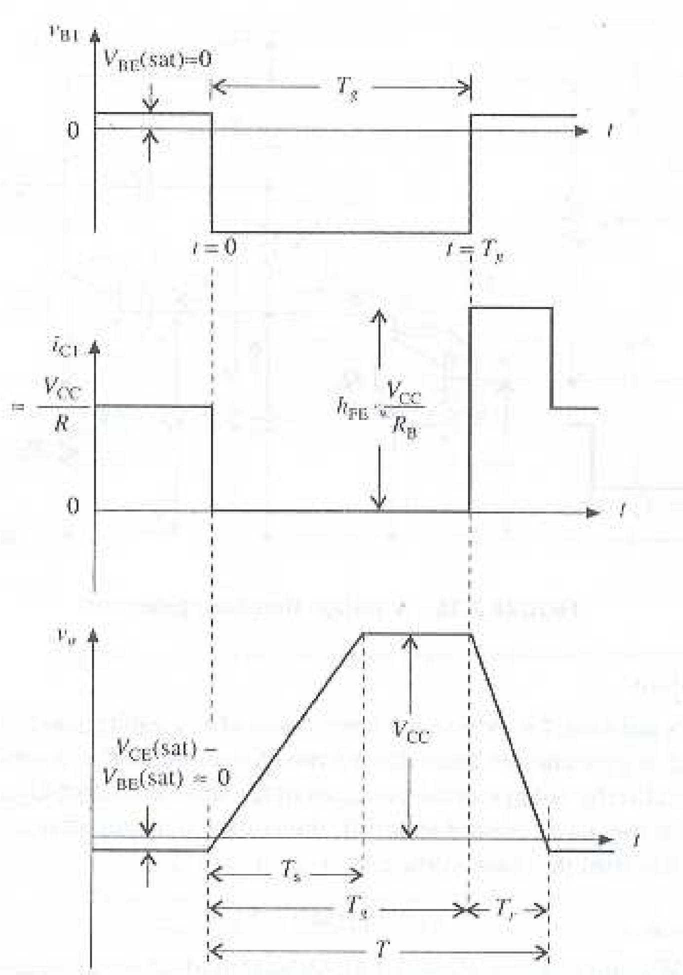
Here for satisfactory operation of a circuit there is a need to replace **R_1 with a diode D**

And R_e must be connected to **$-V_{EE}$ instead of grounding**.

Then this circuit diagram is named as Transistor Bootstrap time base generator.



Operation:



Here input waveform is a gating waveform.

It it required to operate Q1 as a switch.

Case(i): for t<0 , assume that input

Voltage is sufficient to keep Q1 in

Saturation region.

Initially diode is in ON state, sothat

Current flowing through the

Resistor R is , $i_R = \frac{V_{CC} - V_{CE(sat)}}{R}$

V_{cc} is large compared to $V_{CE(sat)}$

So $i_R \approx \frac{V_{CC}}{R}$ = constant

Here Q1 is in saturation region and

Input impedance of emitter follower is high

So that i_{B2} is negligible.

Hence $i_{C1} = i_R$ so current flowing through the capacitor is zero.

Now by applying KVL to the base circuit of Q2, $v_O = V_{CE(sat)} - V_{BE(active)} \approx 0$

Since Q2 is used as an amplifier means it must be in active region.

Necessary condition to keep Q1 in saturation:

Here Q1 is said to be in saturation when only , $i_{B1} \geq \frac{i_{C1}}{h_{FE}}$

$$\frac{V_{CC}}{R_b} \geq \frac{V_{CC}}{h_{FE} R}$$

So $R_b \le h_{FE} R$ --------(1)

Case(ii): with the application of the gating waveform at t=0 , Q1 is driven OFF.

The current i_{C1} is equals to zero and i_R now flows into C , and , assuming unity gain in the emitter follower , the Output increases linearly with time in accordance with

$$Vo(t) = \frac{V_{CC}}{RC} t \text{ -------(2)}$$

Here the maximum sweep amplitude is V_{CC}.

Assume that T_S is the time required to attain maximum sweep amplitude.

Then from equation(2) , T_S = RC -----(3)

If $T_S = T_g$, then sweep amplitude is V_{CC}.

If $T_S > T_g$, then sweep amplitude is less than V_{CC} that is $V_S = \frac{V_{CC}}{RC} T_g$

If $T_S < T_g$ here also sweep amplitude is V_{CC} but here Q2 is in saturation region

for $T_S < t < T_g$. Since from the output loop of Q2 , $V_{CC} - V_{CE2} - V_O = 0$

$$V_{CE2} = V_{CC} - V_O$$

From the above equation it is seen that as V_O approaches V_{CC} ,the collector to emitter voltage of Q2 approaches zero, and it enters the saturation region, where it no longer acts as an emitter follower.

Then as shown in above waveforms V_O remains constant at V_{CC}.

*** When the sweep starts , the diode is reverse biased . since voltage at cathode of diode D is the sum of output voltage and voltage across capacitor C1. we know initially voltage across capacitor C1 is V_{CC}.

Case(iii):At the termination of the gate(at t= Tg^+) , transistor Q1 is in active region

Since voltage between collector and emitter of Q1 is high.

Now $i_{C1} = h_{FE} i_{B1} = \dfrac{h_{FE} V_{CC}}{R_B}$

Neglecting i_{B2}, part of this current is supplied through R , and the remainder $i_A(t)$ is supplied by C. so here capacitor C will discharges with a current $i_A(t)$.

From the circuit , $i_A(t) = i_{C1} - i_R = \dfrac{h_{FE} V_{CC}}{R_B} - \dfrac{V_{CC}}{R}$ = constant

Since this current which discharges C is constant ,then voltage across C falls linearly with time. By emitter follower action the output also returns to its initial value in a linear manner, as shown in the above waveform.