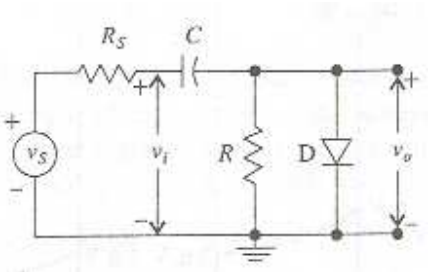
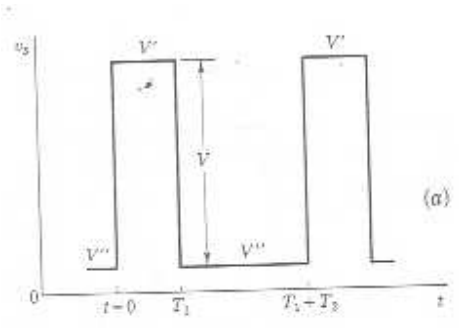
Effect of diode characteristics on clamping voltage:

Generally clamping voltage must be independent of input signal amplitude but due to the diode V-I characteristics clamping voltage will depends on amplitude of input signal.
Let us see the dependence of clamping voltage on the amplitude of input signal.

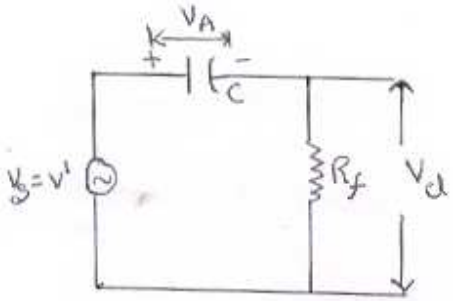
Relation between clamping voltage and input signal amplitude :

Consider practical clamping circuit and input is a square waveform as shown below . Assume that source resistance is negligible.
Also consider V_{cl} is the clamping voltage.
And V is the amplitude of input signal.





We know during the interval 0 to T_1 , diode is in
Conducting state then the equivalent circuit diagram is shown below.
Here $V_s = V'$



If diode is in conducting state output voltage
Is equals to the clamping voltage.

Current flowing through the diode if it is in ON state,

$I_{cl} = I_o (e^{Vcl / \eta V_T} - 1)$

By neglecting 1,

$I_{cl} = I_o e^{Vcl / \eta V_T}$ --------(1)

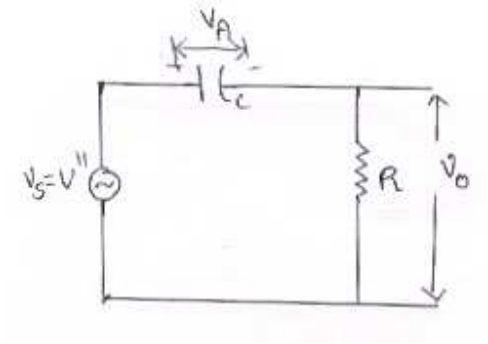
We know here capacitor will tries to charge so equation (1) represents the charging current of a capacitor.

By applying KVL to the above circuit ,

$V' - V_A - V_{cl} = 0$

So $V_A = V' - V_{cl}$ ----(2)

During the interval T_1 to $T_1 + T_2$, diode is in non conducting state and here capacitor will tries to discharge. the equivalent circuit is shown below,(here Vs = V")



Discharging current of a capacitor is $I = V_o/R$

To determine Vo , apply KVL to the given circuit,

$V_o + V_A - V'' = 0$

$V_o = V'' - V_A$

By using equation(2),

$V_o = V'' - V' + V_{cl}$

$V_o = V - V_{cl}$

By neglecting V_{cl} , $V_o = V$

So discharging current of a capacitor is I = V/R ---(3)

Under steady state conditions , net accumulation of charge by the capacitor must be zero. Hence we must set the charging current equal to the discharging current

From equations (1) & (3)

$I_o e^{Vcl/\eta V_T} = V/R$

By taking natural logarithm on both sides,

$V_{cl} = \eta V_T \ln (V / I_O R)$

By differentiating above equation with respect to V,

$d V_{cl} / dV = \eta V_T / V$

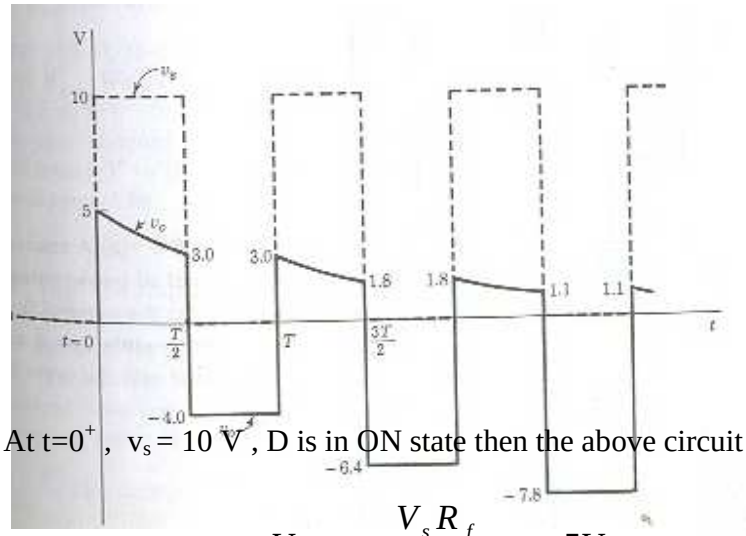
so if amplitude of input signal is large then clamping voltage is made independent of input amplitude.

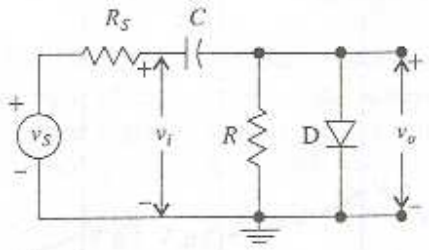
Problems on clampers :

1. In the circuit of given figure , $R_s = R_f = 100\Omega$, R = 10 KΩ, and C = 1.0 μF. at t=0 there is applied a symmetrical square wave signal of amplitude 10 V and frequency 5 KHz. As indicated below ,the signal v_s extends from 0 to 10 V.
   Draw the first several cycles of the output waveform.

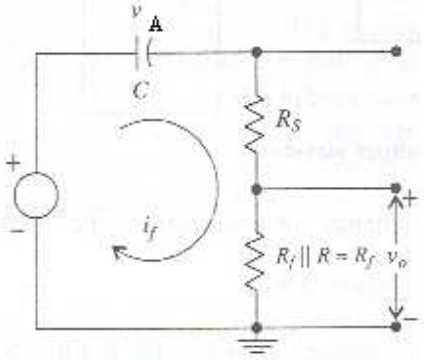
Solution:

Assume that capacitor C is initially uncharged.





At $t=0^+$, $v_s = 10$ V , D is in ON state then the above circuit will becomes



So $$V_O = \frac{V_s R_f}{(R_f + R_s)} = 5V$$

Since voltage across capacitor(V_A) is zero.

During the interval 0 to $\frac{T}{2}$, v_s is constant at 10 V so capacitor will tries to charge then output is a decaying exponential

So $$V_o(t = \frac{T}{2}) = 5e^{-(\frac{T}{2\tau})}$$

Where $\tau = (R_s + R_f)\, C = 200$ μsec

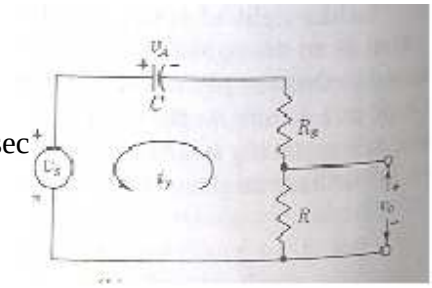
And T = 0.2 msec

So $V_o = 3$ V

At this time , since the voltage across R_s is also 3 V (since $R_s = R_f$)

$V_A = 4$ V (by applying KVL to the above circuit)

At $t = \left(\frac{T}{2}\right)^+$ input voltage suddenly changes to 0 V , here diode is in OFF state then the circuit diagram is shown below. In this circuit $V_A = 4$ V and Vs = 0 V ,so that ,neglecting Rs compared with R , Vo = - 4 V



Here output now again starts to decay toward zero.

However, the time constant now is RC = 10000 μsec
It is very much greater than T /2 .

Therefore the decay is negligible and is not
Indicated in the figure.

Since in the interval t = T/2 to t = T the voltage across the capacitor has not changed , then at t = T+ the output returns to 3 V .

Again the output decays toward zero.

By doing the above analysis we can complete the remaining cycles.