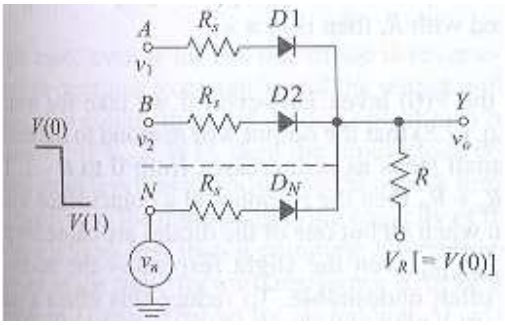
Diode OR gate for positive logic:

A diode OR for positive logic is shown in figure below . This is same as diode OR gate for negative logic except that all diodes must be reversed. Consider

The supply voltage V_R has a value equal to the voltage V(0) of the 0 state.
(for positive logic V(0) is at low potential)

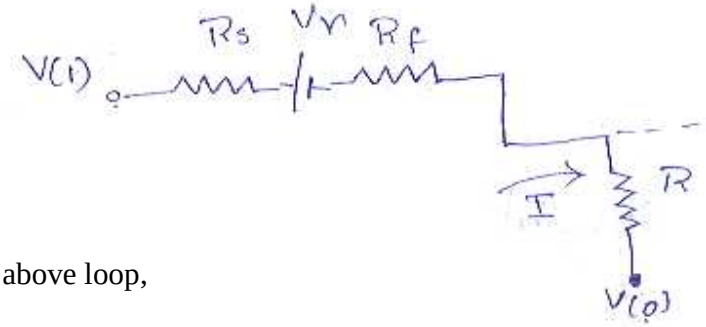


Initially equation for output voltage is $v_O = V(0) + IR$ ----(1)
Since current direction is from anode to cathode.

Case(i): If all inputs (A ,B,….N) are in the 0 state, then the voltage across each diode is $V(0) - V(0) = 0$. Since in order for a diode to conduct it must be forward-biased by Atleast the cut-in voltage V_γ, then none of the diode conducts. So current flowing Through the circuit is zero.

Hence the output voltage is $v_o = V(0)$, and Y is in the 0 state.

Case(ii): If the inputs B,….N are in 0 state and , input A is changed to the 1 state, which for positive logic is at the potential V(1), more positive than the 0 state, then D1 will conduct and remaining diodes are in non conducting state. Then the circuit diagram will Becomes as shown below. (by replacing D1 with its piece wise linear equivalent Circuit & And D2…D_N with open circuit).



By applying KVL to the above loop,

$$I = \frac{V(1) - V_\gamma - V(0)}{R_S + R_f + R}$$

Then the output becomes,

$$v_O = V(0) + \left(\frac{V(1) - V_\gamma - V(0)}{R_S + R_f + R} \right) R$$

Usually R is chosen much larger than $R_S + R_f$. Under this restriction

$$v_O = V(1) - V_\gamma$$

Hence the output voltage is smaller than the most positive value of V(1) by V_γ.

If diode is an ideal one , then $v_O = V(1)$

So OR function for positive logic is satisfied with the above circuit.

AND Gate:

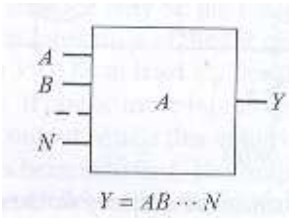
An AND gate has two or more inputs and a single output , and it operates in accordance with the following definition.

The output of an AND assumes the 1 state if and only if all the inputs assume the 1 state.

The IEEE standard symbol for the AND circuit is given in figure (a) Below together with the Boolean expression for the gate. The equation is to be read

" Y equals A and B and…..and N ". It may be verified that the two-input

Truth table of figure(b) is consistent with the above definition of the AND operation.



(a)

Input		Output
A	*B*	*Y*
0	0	0
0	1	0
1	0	0
1	1	1

(b)