Clamping circuits(clampers) : a clamping circuit is one that takes an input waveform and provides an output same as input but one edge tightly clamped to some constant reference level.

Here constant reference level is treated as clamping voltage.

Clamping circuits are used to produce AC along with DC.

Clamping circuit is also named as DC restorer , DC re inserter ,DC inserter.

Clamping circuits are of two types

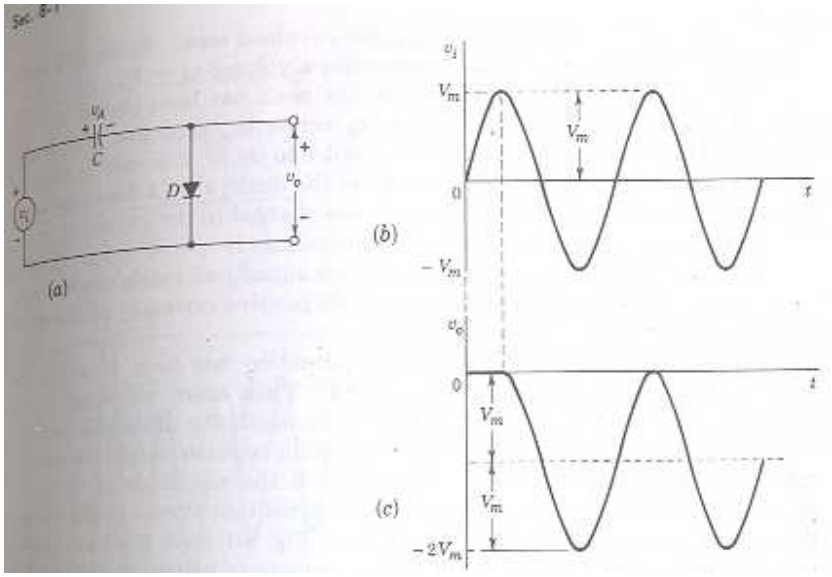
1. positive peak clamper(negative clamper)
2. negative peak clamper (positive clamper)

positive peak clamper(negative clamper) : here positive peak of input signal is clamped to some constant reference level.

Circuit diagram for positive peak clamper is shown below,

Operation :

Consider diode is an ideal one and also
Signal source resistance is zero.



Assume that V_A is voltage across the capacitor.

So now $V_o = V_i - V_A$ ---(1)

During the first quarter cycle of input waveform, D is in ON state(replaced with short circuit) so Output voltage is zero. So capacitor will be charged to input peak value(V_m).

At the end of first quarter cycle, $V_A = V_m$

Immediately after the first quarter cycle , diode is Replaced with open circuit(OFF) ,because voltage at anode is negative value. So **capacitor may never discharge**.

After the first quarter cycle, from equation(1)
If $V_i = 0$, $V_o = -V_m$

If $V_i = -V_m$, $V_o = -2V_m$

If $V_i = V_m$, $V_o = 0$

Hence positive peak of the signal is clamped to constant reference level . here clamping voltage is zero.(since diode is an ideal one)

If we consider cut in voltage of a diode , then clamping voltage is V_γ.

Negative peak clamper(positive clamper) : here negative peak of input signal is clamped to some constant reference level.

Circuit diagram for negative peak clamper is also same as positive peak clamper except that diode terminals should be reversed.

Operation of this circuit is entirely same as the above circuit diagram.

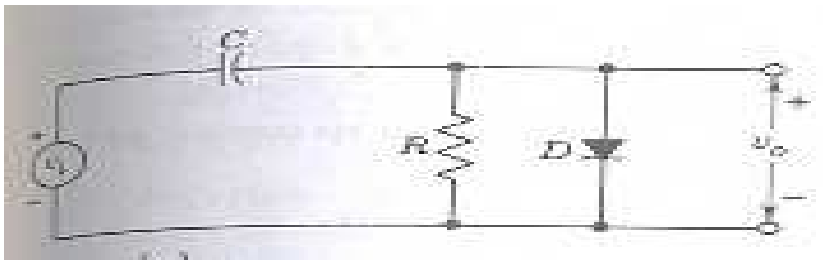
In the above circuit diagrams(positive peak clamper) , if $V_i = V_m$ then $V_A = V_m$ and clamping voltage is zero.

Case(i): now if the amplitude of the input signal is **increases** , then diode again comes into the conducting state(because voltage at anode is positive) then again capacitor will be charged to the new peak value of input signal, then again clamping voltage is zero.

So here is no problem with the above circuit diagram.

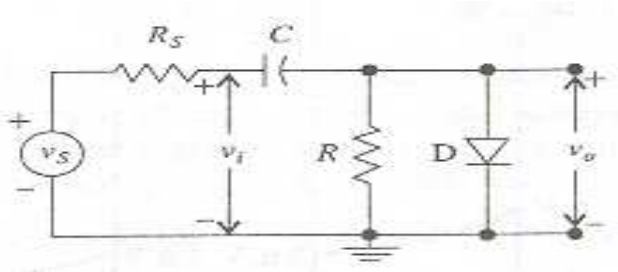
Case(ii): but if the amplitude of input signal is **decreases**, then voltage at anode of diode is some negative value, so diode is still in non conducting state(OFF).so here capacitor may never discharge. So now clamping voltage is some **negative value** .but clamping voltage must be zero here.

To attain zero clamping voltage , it it required that the voltage across the capacitor decrease. To permit a decrease in capacitor voltage it is necessary to shunt a resistor across the diode as shown in figure..



Clamping circuit taking source and diode resistances into account :
(square wave input to clamping circuit)

Consider R_f is diode forward resistance and Rs is the source resistance.



assume that $R >> R_f$.

for the applied input voltage, diode may be ON or OFF , then the above circuit diagram will behaves like a high pass RC circuit . then the input and output waveforms of the circuit diagram is shown below under steady state conditions,