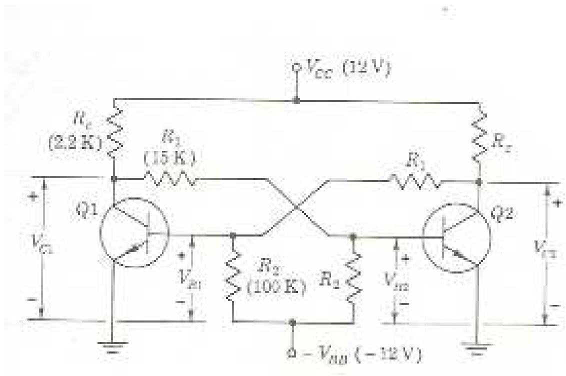
**PROBLEMS:**

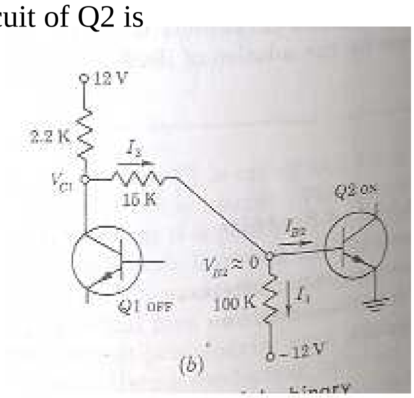
1. Calculate the stable-state currents and voltages for the circuit given below. Assume that the transistors have a minimum value of 20.



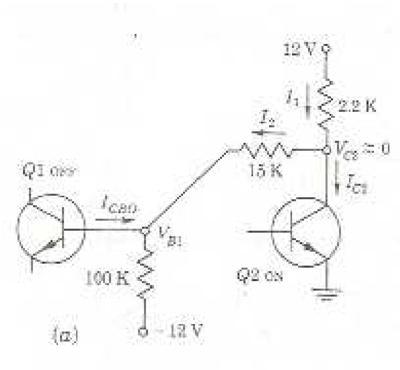

**Solution:**

Assume that Q1 is OFF & Q2 is ON

Base circuit of Q2 is




Collector circuit of Q2 is




Assume that $V_{CE(sat)} = V_{BE(sat)} = 0V$

From the above equations ,

$V_{B1}$ = -1.56 V , $V_{B2} \approx 0V$ , $V_{C2} \approx 0V$ , $V_{C1} \approx 10.5V$

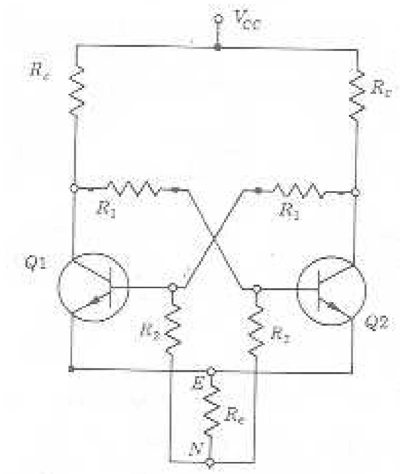
$I_{C1} = 0mA$, $I_{B1} = 0mA$, $I_{C2} = 5.35mA$ , $I_{B2} = 0.58mA$

**Self bias binary :**

The need for the negative power supply in fixed bias binary may

be eliminated by using a common emitter resistor $R_e$ to provide self bias ,

as shown in figure.



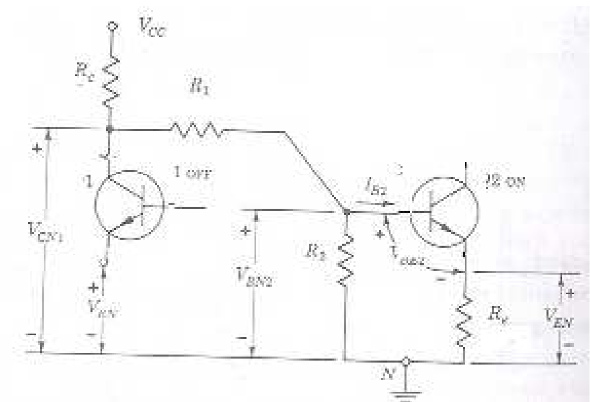

Operation of self bias binary is same as the

operation of fixed bias binary.

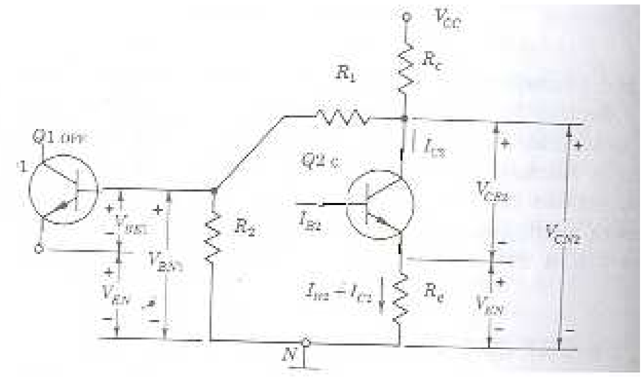
**Design of self bias binary:**

Consider stable state of binary is Q1 OFF &Q2 ON

Base circuit of Q2




Collector circuit of Q2



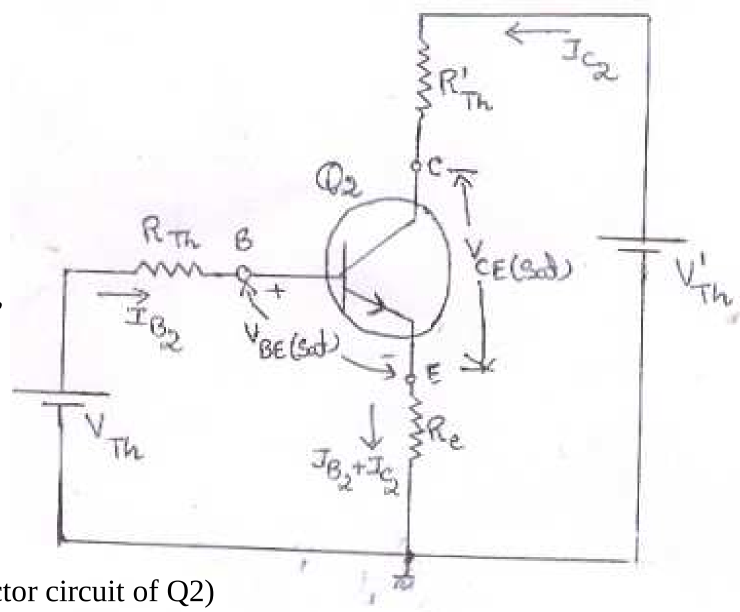

By determining Thevinan equivalent circuit at collector and base terminals of Q2 ,
Then the equivalent circuit when Q2 is in saturation is shown in figure below,

Here $V_{Th} = \dfrac{V_{CC} R_2}{R_C + R_1 + R_2}$

$$R_{Th} = \frac{R_2 (R_C + R_1)}{R_C + R_1 + R_2}$$

And also $V_{Th}{}' = \dfrac{V_{CC}(R_2+R_1)}{R_C+R_1+R_2}$

$$R_{Th}{}' = \frac{R_C(R_2+R_1)}{R_C+R_1+R_2}$$




Now by applying KVL to the above loops, determine $I_{B2}$, $I_{C2}$, $I_{E2}$ and

Also $V_{EN}$ (=$R_e$ $I_{E2}$)

We know To keep Q1 is in OFF state ,

$$V_{BE1} < V_{BE(cutoff)}$$

Here $V_{BE1} = V_{BN1} - V_{EN}$ (from collector circuit of Q2)

Where $V_{BN1} = \dfrac{V_{CN2}R_2}{R_1+R_2}$ , $V_{CN2} = V_{CE(sat)} + V_{EN}$

To keep Q2 is in ON state , $I_{B2} \geq I_{B2(\min)}$

Expression for $I_{B2}$ & $I_{C2}$ can be obtained from the above analysis.

And here $I_{B2(\min)} = \dfrac{I_{C2}}{h_{FE}}$

Hence the component values should be properly selected to satisfy the above two conditions.

**Expressions for steady state voltages and currents :**

Assume that $V_{CN1}$, $V_{BN1}$ are voltages at collector and base terminals of Q1 respectively.

And $V_{CN2}$, $V_{BN2}$ are voltages at collector and base terminals of Q2 respectively.

$V_{EN}$ is the voltage at emitter terminals of both the transistors.

And also $I_{C1}$ , $I_{C2}$, $I_{B1}$ , $I_{B2}$, $I_{E1}$,$I_{E2}$ are the collector, base and emitter currents of corresponding transistors.

Consider stable state of self bias binary is **Q1 OFF & Q2 ON**

From the above analysis,

$$V_{CN2} = V_{CE(sat)} + V_{EN}$$

$$V_{BN2} = V_{BE(sat)} + V_{EN}$$

$$V_{BN1} = \frac{V_{CN2} R_2}{R_1 + R_2}$$

From the base circuit of Q2 ,

By using super position principle ,

$V_{CN1}$ = $V_{CN1}$ due to $V_{CC}$ + $V_{CN1}$ due to $V_{BN2}$

$V_{CN1}$ due to $V_{BN2}$ = $\dfrac{V_{BN2} R_C}{R_1 + R_C}$

$V_{CN1}$ due to $V_{CC}$ = $\dfrac{V_{CC} R_1}{R_1 + R_C}$

$V_{CN1}$= $\dfrac{V_{BN2} R_C}{R_1 + R_C} + \dfrac{V_{CC} R_1}{R_1 + R_C}$

And also the currents are ,

$I_{C1} = 0mA$, $I_{B1} = 0mA$ $I_{E1} = 0mA$

$I_{C2}, I_{B2}, I_{E2}$ can be obtained by applying KVL to the equivalent circuit of Q2 when it is in saturation region .