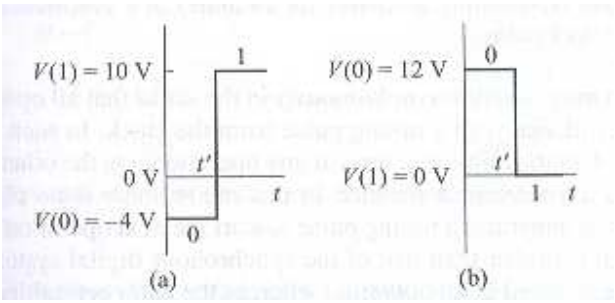
LOGIC GATES **UNIT-3**

Logic gate: an electronic circuit which produces output pulses depending on the pulses at input terminals is known as a logic gate.

Logic gates are essentially designed for use extensively in digital computers.

Binary arithmetic and mathematical manipulation of switching or logic functions are best Carried out with classification 3, which involves two symbols, a logical 0 and a logical 1.

Logic Systems: In a binary level logic system a bit is implemented as one of the two voltage levels. If as in figure (a) the more positive voltage is the 1 level and the other is the 0 level, the system is said to employ **positive logic**. On the other hand ,a **negative – logic system** , as in figure (b) is one which designates the more negative voltage state of the bit as the 1 level and the more positive as the 0 level. it should be emphasized that the absolute values of the two voltages are of no significance in these definitions. In particular, the 0 state need not represent a zero voltage level – although in some systems it might. In figure (b) we have intentionally illustrated the case where the value of the 1 state is 0 V.



In pulse logic systems a bit is recognized by the presence or absence of a pulse.

A 1 signifies the existence of a positive pulse in a pulse positive- logic system; a negative pulse denotes a 1 in a pulse negative – logic system. In either system a 0 at a particular input – or output – at a given instant of time designates that no pulse is present at that particular moment.

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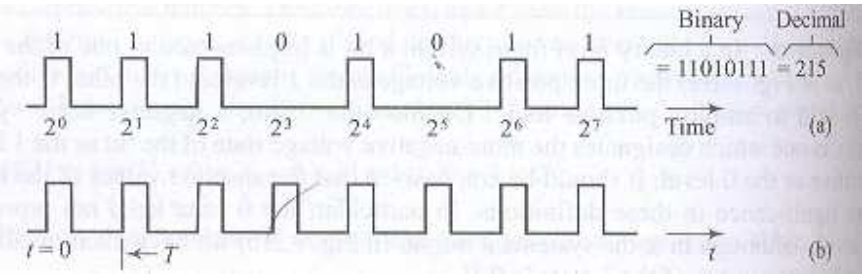
Most computers using pulses operate as a **synchronous systems** since all operations are performed during constant intervals of time. There is available in a computer , to achieve this synchronism , a continuous sequence of pulses of good wave shape , whose frequency is usually established by a crystal oscillator . this stable oscillator determines the basic rate at which the computer operates and for this reason is referred to as the master clock.

In a synchronous pulse system a number is represented in serial form by a train of pulses. A 1 is implemented by a pulse occurring at the same time as a clock pulse , where as for a 0 a signal pulse is absent at a particular clock pulse time. For example , the pulse train in Figure (a) below represents binary number 11010111- 215 in decimal number system. Note that since time increases from left to right , the least significant pulse occurs at the Extreme left – at t = 0 , whereas in representing a binary number the LSB is placed at the Extreme right. Figure (b) is a clock signal .



Different logic gates used in digital computer is

1. OR Gate
2. AND Gate
3. NOT Gate
4. NAND Gate

5. NOR Gate.

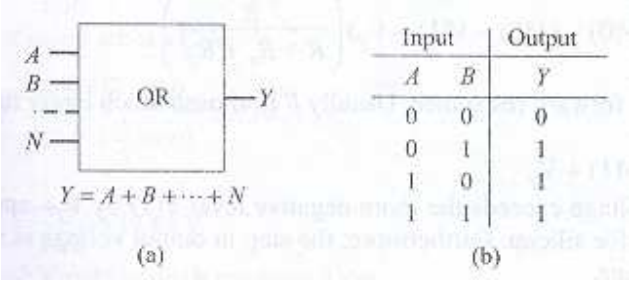
OR Gate:

An OR gate has two or more inputs and a single output , and it operates in accordance with the following definition.

The output of an OR assumes the 1 state if one or more inputs assume the 1 state.

The n inputs to a logic circuit will be designated by A,B,….N and the output by Y.

It is to be understood that each of these symbols may assume one of the two possible Values, either 0 or 1. The IEEE standard symbol for the OR circuit is given in figure (a) Below together with the Boolean expression for the gate. The equation is to be read " Y equals A or B or…..or N ". instead of defining a logical operation in words , an Alternative method is to give a truth table which contains a tabulation of all possible Input values and their corresponding outputs. It should be clear that the two-input Truth table of figure(b) is equivalent to the above definition of the OR operation.



Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

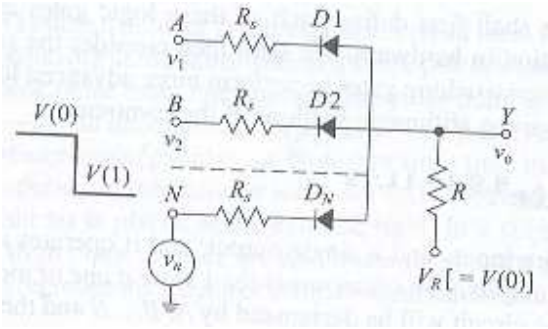
(b)

Realization of OR gate using diodes:

Diode OR gate for negative logic:

A diode OR for negative logic is shown in figure below, where the symbol D is used to Represent a semiconductor diode. The source resistance is designated by Rs. Consider

The supply voltage V_R has a value equal to the voltage V(0) of the 0 state.
(for negative logic V(0) is at high potential)

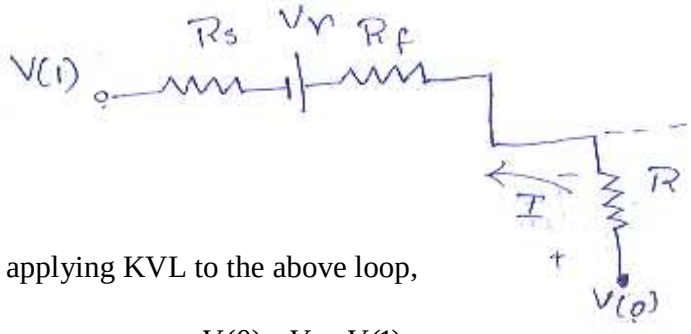


Initially equation for output voltage is $v_O = V(0) - IR$ ----(1)
Since current direction is from anode to cathode.

Case(i): If all inputs (A ,B,….N) are in the 0 state, then the voltage across each diode is $V(0) - V(0) = 0$. Since in order for a diode to conduct it must be forward-biased by Atleast the cut-in voltage V_γ, then none of the diode conducts. So current flowing Through the circuit is zero.

Hence the output voltage is $v_o = V(0)$, and Y is in the 0 state.

Case(ii): If the inputs B,….N are in 0 state and , input A is changed to the 1 state, which for negative logic is at the potential V(1), less positive than the 0 state, then D1 will conduct and remaining diodes are in non conducting state. Then the circuit diagram will Becomes as shown below. (by replacing D1 with its piece wise linear equivalent Circuit & And D2…D_N with open circuit).



By applying KVL to the above loop,

$$I = \frac{V(0) - V_\gamma - V(1)}{R_S + R_f + R}$$

Then the output becomes,

$$v_O = V(O) - \left(\frac{V(0) - V_\gamma - V(1)}{R_S + R_f + R} \right) R$$

Usually R is chosen much larger than $R_S + R_f$. Under this restriction

$$v_O = V(1) + V_\gamma$$

Hence the output voltage exceeds the more negative level V(1) by V_γ.

If diode is an ideal one , then $v_O = V(1)$

So OR function for negative logic is satisfied with the above circuit.