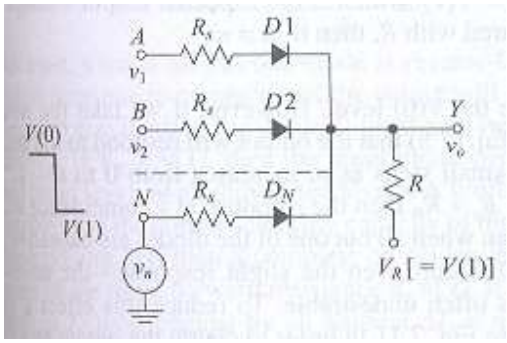
Realization of AND gate using diodes:

Diode AND gate for negative logic:

Diode AND gate for negative logic is same as diode OR gate for positive logic.

A diode AND for negative logic is shown in figure below, Consider

The supply voltage V_R has a value equal to the voltage V(1) of the 1 state.
(for negative logic V(1) is at low potential).



Initially equation for output voltage is $v_O = V(1) + IR$ ----(1)
Since current direction is from anode to cathode.

Case(i): If all inputs (A ,B,….N) are in the 1 state, then the voltage across each diode is

$V(1) - V(1) = 0$. Since in order for a diode to conduct it must be forward-biased by

Atleast the cut-in voltage V_γ, then none of the diode conducts. So current flowing

Through the circuit is zero.

Hence the output voltage is $v_o = V(1)$, and Y is in the 1 state.

Case(ii): If the inputs B,….N are in 1 state and , input A is changed to the 0 state, which

for negative logic is at the potential V(0), more positive than the 1 state, then D1 will

conduct and remaining diodes are in non conducting state. Then the circuit diagram will

Becomes as shown below. (by replacing D1 with its piece wise linear equivalent

Circuit & And D2…D_N with open circuit).

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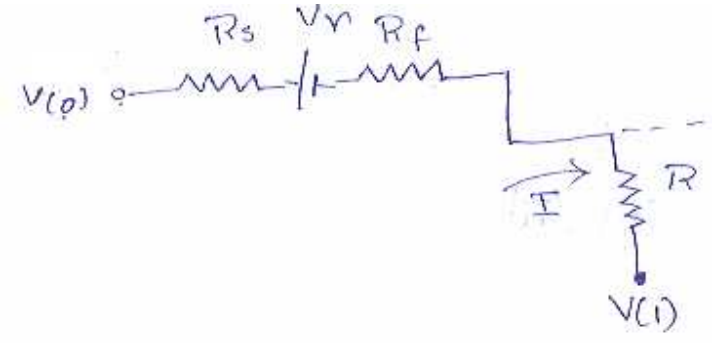


By applying KVL to the above loop,

$$I = \frac{V(0) - V_\gamma - V(1)}{R_S + R_f + R}$$

Then the output becomes,

$$v_O = V(1) + \left(\frac{V(0) - V_\gamma - V(1)}{R_S + R_f + R} \right) R$$

Usually R is chosen much larger than $R_S + R_f$. Under this restriction

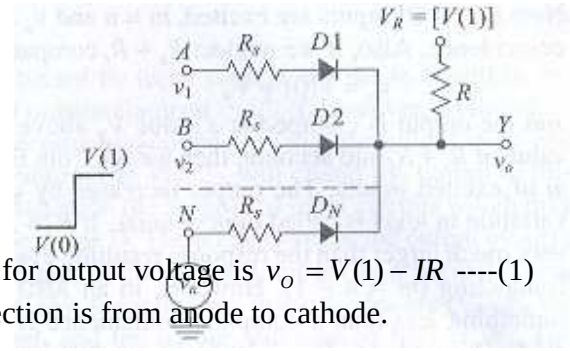
$$v_O = V(0) - V_\gamma$$

If diode is an ideal one , then $v_O = V(0)$

So AND function for negative logic is satisfied with the above circuit.

Diode AND gate for positive logic:

A diode AND for positive logic is shown in figure below . This is same as diode OR gate for negative logic. Consider The supply voltage V_R has a value equal to the voltage V(1) of the 1 state.(for positive logic V(1) is at high potential).



Initially equation for output voltage is $v_O = V(1) - IR$ ----(1)
Since current direction is from anode to cathode.

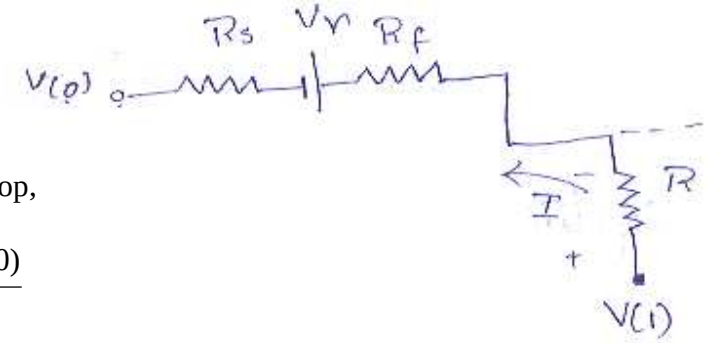
Case(i): If all inputs (A ,B,….N) are in the 1 state, then the voltage across each diode is $V(1) - V(1) = 0$. Since in order for a diode to conduct it must be forward-biased by

Atleast the cut-in voltage V_γ, then none of the diode conducts. So current flowing

Through the circuit is zero.

Hence the output voltage is $v_o = V(1)$, and Y is in the 1 state.

Case(ii): If the inputs B,….N are in 1 state and , input A is changed to the 0 state, which for positive logic is at the potential V(0), less positive than the 1 state, then D1 will conduct and remaining diodes are in non conducting state. Then the circuit diagram will Becomes as shown below. (by replacing D1 with its piece wise linear equivalent Circuit & And D2…D_N with open circuit).



By applying KVL to the above loop,

$$I = \frac{V(1) - V_\gamma - V(0)}{R_S + R_f + R}$$

Then the output becomes,

$$v_O = V(1) - \left(\frac{V(1) - V_\gamma - V(0)}{R_S + R_f + R} \right) R$$

Usually R is chosen much larger than $R_S + R_f$. Under this restriction

$$v_O = V(0) + V_\gamma$$

If diode is an ideal one , then $v_O = V(1)$

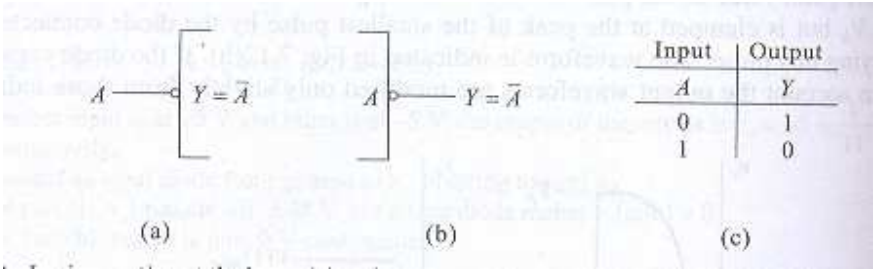
So AND function for positive logic is satisfied with the above circuit.

NOT Gate or Inverter circuit:

The NOT circuit has a single input and a single output and performs the operation of logic negation in accordance with the following definition: The output of a NOT circuit

takes on the 1 state if and only if the input does not take on the 1 state.

The IEEE standard to indicate a logic negation is a small circle drawn at the point where a signal line joins a logic symbol. Negation at the input of a logic block is indicated in figure(a) and at the output in figure(b). the truth table and the Boolean expression for negation are given in figure(c). the equation is to be read "Y equals NOT A" or " Y is the complement of A".



Input	Output
A	Y
0	1
1	0

A circuit which accomplishes a logic negation is called a NOT circuit, or, since it Inverts the sense of the output with respect to the input, it is also known as an inverter. The output of an inverter is relatively more positive if and only if the input is relatively Less positive. In a truly binary system only two levels V(0) and V(1) are recognized, and The output , as well as the input, of an inverter must operate between these two voltages. When the input is at V(0), the output must be at V(1), and viceversa. Ideally, then a NOT Circuit inverts a signal while preserving its shape and the binary levels between which the signal operates, as indicated in figure below.

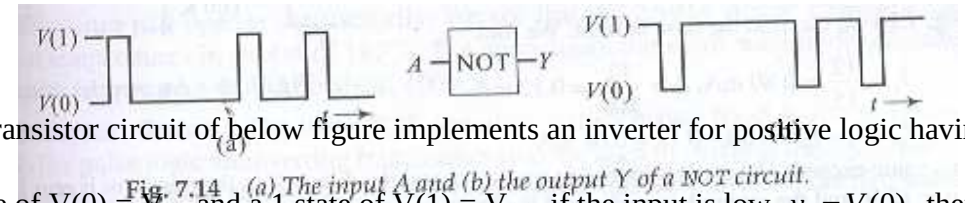


Fig. 7.14 (a) The input A and (b) the output Y of a NOT circuit.

The transistor circuit of below figure implements an inverter for positive logic having a 0 state of V(0) = V_{EE} and a 1 state of V(1) = V_{CC}. if the input is low, $v_i = V(0)$, then the Parameters are chosen so that the Q is OFF and hence $v_o = V_{CC} = V(1)$. On the otherhand, If the input is high, $v_i = V(1)$, then the circuit parameters are picked so that Q is in

Saturation and then $v_o = V_{EE} = V(0)$, if we neglect the collector-to-emitter saturation Voltage $V_{CE(sat)}$.

A similar circuit using a p-n-p transistor is used for a negative-logic NOT circuit.