Kenneth **Vallecillo G.**

Electrical Engineer

About

Kenneth
Vallecillo González.
+506-6036-7088.
San José,
Costa Rica.
kvallecillog@gmail.com
https://linkedin.com/
in/kvallecillog/

Languages

Spanish/English.

Technology Summary

Unix, Python, C/C++, Perl, Verilog, Assembly, SystemC, GIT, Excel, JMP, TPIE, TRACE, CIFT, AURA, CMTP, AQUA, Crystal Ball, Vortex, FUNMV, CLASS/SORT ATE, Microcontroller's, Oscilloscope's, Digital analyzer's.

Summary

Highly-motivated Electrical Engineer, with a strong willingness to learn. Committed to excellence and high standards. Some specific interests are aligned to computer architecture and science. Solid background in ATE's and Testing Methodologies, Unix/programming/scripting, manufacturing test principles and test program. Familiar with DFT principles and microprocessor architecture. Experience in data mining and manipulation with Excel/JMP. Always looking to grow as a professional in a challenging environment; by using, improving and getting new skills in order to deliver innovative solutions.

Professional Experience

2015-Present **Product Development Engineer at Intel** MVE DCD Array, Costa Rica

Module Owner responsible for developing test programs and test methodologies to support client and server products.

Key Accomplishments:

- Responsible of quality goals in test program releases by owning the module integration, validation and debug activities for Product Release Quality milestones.
  - A significant contributor to test hole closure activities for a major excursion by developing test flows to screen customer returns.
  - A significant contributor to achieving Cold Socket Elimination in a server Product by providing the root cause to 30% of the rejects.
- Developer of a HVM testing methodology to measure and detect voltage variability for SORT and CLASS sockets.
- Research contribution by writing and presenting the paper *Innovative HVM methodologies to screen new array defect mechanism* in Ideation Conference and GDC Innovation Conference.
- Cascade Array Oregon team support for QA debug and module validation of client products.

Honors and Awards:

- **Oral Presentation at GDC Innovation** Invited to bring an oral presentation at GDC Innovation week. Nov 2016.
- **Best Oral Presentation Intel Ideation Week** In recognition of the outstanding paper and technical talk presented at Ideation 2016. Oct 2016.
- **DCVM Q3 2016 DRA Awards** Provided TP solutions to achieve cold socket elimination for BDXML server product. Sept 2016
- **MVE DCD DNA Award (Intel)-Quality and Can-do attitude** Developed and created multiple new array algorithms, TP flows and test conditions to screen FACR units from server products. Apr 2016

Qualifications

- A methodological approach for day to day work, planning and scheduling own daily tasks with the sense of urgency.
- Fast learner, responsible of critical team activities, through proactive learning, both as the theory as well on the hands-on role.
- Excellent written and verbal communication skills either public, groups, or via electronic media.
- Capable of adapting quickly to fast-paced environments, contributing to multiple Server/Client teams and products with strong debugging and data analysis skills.
- Creative thinking, challenging the status quo and contributing to the standardization and quality efforts to module integration and validation activities. Seeking proactively to reduce manual tasks by automating and proposing new solutions.

Education and other credentials

2011–2016 **B.Sc. in Electrical Engineering** University of Costa Rica
Emphasis in computer and networks.

2015 **Startup Weekend Change Makers** Powered by Google.
Working and building a product with interdisciplinary teams.

2015 **PRIS-Workshop** By Dr. Francisco Siles, Dr. Álvaro de la Ossa and Dr. Douglas Navarro.
Street fighter open tools, parallel programming and numerical analysis.

2014 **Intel Youth Enterprise Ideation Camp** By Henrik Scheel. Intel IYE Master Trainer.
Development Entrepreneurial Culture.

2012 **Nanofabrication Workshop** By Dr. Henry I. Smith, MIT NanoStructures Laboratory.
An introduction to nanotechnology.

2005-2010 **B.Sc. Middle education** Liceo Experimental Bilingüe de Pococí
English certification in written and verbal production.

Personal Projects

2015 **Course: Embedded Systems; RTOS projects**
RTOS design and implementation with MPS432 microcontroller using C/C++.
- *Smart Lamp*, *Attitude indicator*, *Pong Game*.

2015 **Course: Graduation Project; CPU Assembler**
Design and implementation of an assembler for a RISC instruction set architecture (CPUCR), with a syntax checker developed with Python and a behavioral FSM in SystemC (C++).

2015 **Course: Digital Computers Architecture II; Pipelining CPU**
Pipelining CPU development for MIPS Verilog modeling to execute a set of instruction in the 5 pipe steps considering hazards hardware solutions.

2015 **Course: Digital Computers Architecture II; Cache Model**
C++ simulation of cache memory structures (Direct-mapped, set-associative, fully-associative) and analysis of performance parameters.

2014 **Course: Digital Circuits Laboratory; Tic Tac Toe**
Verilog hardware description of Tic Tac Toe game using FPGA's, ps2 keyboard and VGA monitor.