# **KB Verification Library and Coding Guidelines**

1/31/2018
Verification Team



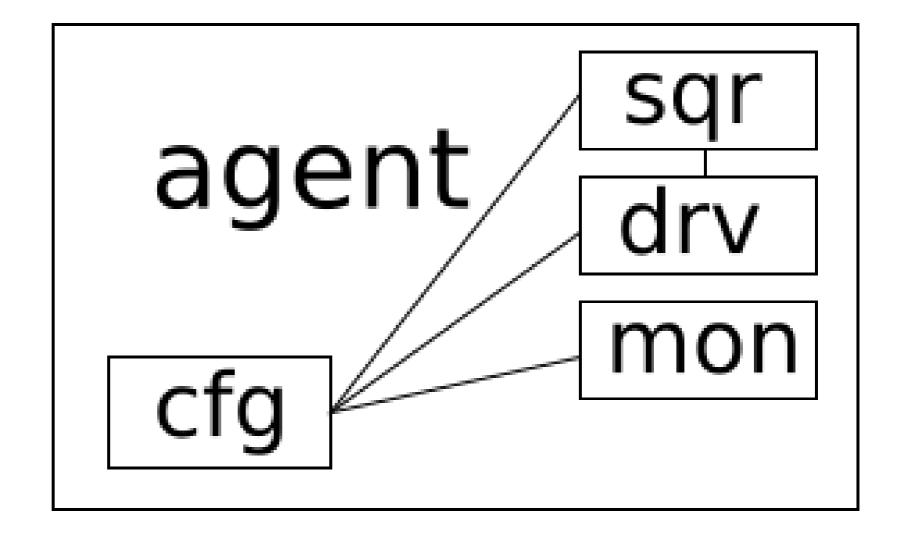
#### Outline

- Presentation of existing base classes
- How to use them
- Future developments
- Coding guidelines



#### Existing base classes: agent structure

- Kb\_agent
  - Kb\_mon
  - Kb\_drv
  - Kb\_sqr
- Kb\_agent\_cfg





#### Existing base classes: agent

- Kb\_mon functionality
  - Instantiate analysis port
  - Create transaction handle
  - Get agent config handle
  - Handle reset: TODO
- kb\_drv
  - Get agent config handle
  - Handle reset : TODO
- Kb\_agent
  - Create drv/sqr/mon type as specified in config
  - Connect/create driver and sequencer if ACTIVE
  - Get virtual interfaces and connect them to drv/mon



#### Existing base classes: agent config

- Kb\_agent\_cfg
  - Extends from uvm\_object
  - Encapsulate all the config for the agent
    - Check\_en, coverage\_en, is\_active, ...
  - Define mon/dvr/sqr types
  - Keep track of number of transactions
  - Contains generic control fields such as m\_ctrl[string]
- Having one config per agent allows great vertical/horizontal reusability



#### Existing base classes: clock agent

- Let's see use case of agent base classes with kb\_clock\_agent
  - Clock\_agent\_config contains all the information
    - o Mon\_type\_name = kb\_clock\_monitor
    - Drv\_type\_name = kb\_clock\_driver
    - Set\_active
    - Printing format code
    - Clock\_cfg
      - Defines clock names to drive and their config
        - Period
        - Duty cycle
        - Jitter
        - **–** ...
- This config is created in the env/test and then given to agent through config\_db



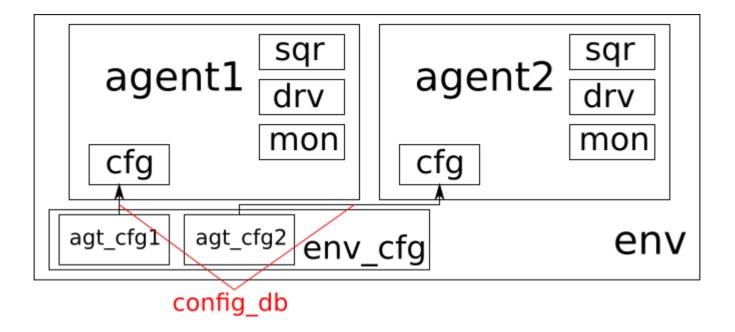
#### Existing base classes: reset agent

- reset\_agent\_config contains all the information
  - o Mon\_type\_name = kb\_reset\_monitor
  - o Drv\_type\_name = kb\_reset\_driver
  - Set\_active
  - Printing format code
  - Reset\_cfg
    - Defines clock names to drive and their config
      - Polarity
      - Pulse width
      - Init value
      - ...
- This config is created in the env/test and then given to agent through config\_db



#### How to use base classes

- In general case, we have the following architecture
  - One config at the top, that contains all the sub configs.
  - Top config is built in the base test
    - Then all sub configs are built as well
  - Then each extended test can overwrite some top/sub config parameters
  - Sub env/agents are then built and get correct updated configs
- This scenario has been tried successfully on glasswing environment





#### How to use base classes

build blka\_cfg

overwrite default values

put blka\_cfg in config\_db

build blka

get blka\_cfg

build sub blks depending on blka\_cfg

blka build\_phase

env build\_phase



#### Existing base classes: base test

- Contains generic UVCs
  - Custom report server
  - Report catcher for handling report errors
  - Watchdog for timeout handling
  - Assert monitor for checking assertions/cover/assume are covered for specific tests
- Handles end-of-test mechanism
- Add debug mechanisms : print factory, field override
- Hooks for config object program
  - Used for overwriting default values of config objects before the objects that use these config are built



#### Common macros

- Factory registration
  - For parameterized object/classes
    - Kb\_param\_object/component\_registry
- For reporting : use get\_type\_name() for ID field and string formatting
  - `kb\_info((Tests %d, 1), UVM\_NONE)
- For dynamic upcast
  - `kb\_dcast(dest, src)
- For assertion definitions
  - Automatic property/assertion naming
- For config\_db get/set
  - Automatic fatal report if get fails



#### Existing base classes: RAL

- Kb\_reg\_block
  - Define shared init method
    - Configure, build, set\_base\_addr, lock\_model and reset
- Kb\_reg\_model\_cfg
  - Contains configuration of the reg model
    - Register mode : EXPLICIT/IMPLICIT
    - Adapter\_type\_name
    - Register coverage enable
    - o Reg block name
  - It is provided to the reg model and predictor
- Kb\_reg\_model
  - Build adapter
  - Provides method for connecting adapter
- Kb\_reg\_predictor
  - TODO: provide mechanism for automatic connection to bus agent



#### How to use base classes

#### Build phase

- RAL objects are built in base test: TBC
  - Fields can be set/randomized in test and then there is automatic update of the RAL in the configure phase of the running sequence.
- Reg block is first built with specified base address
- Reg model config is built and programmed
  - Set adapter type name, reg mode, ...
- Set reg model config in config db
- Build reg model and predictor
- Connect phase
  - Connect bus agent with reg model method
  - Connect bus agent with predictor



#### Future developments

- Automatic generations of UVCs
  - Use templates for agents/mon/drv ... that extends base classes
- Develop methodology/base classes for sequences in order to ease vertical/horizontal reuse : sequence\_cfg ?
- Complete features for clock, reset agents
- Use Doxygen for base classes documentation
- Coverage base class encapsulating covergroups
- Wavedrom json timing diagram for interface
- Develop common header
- Add example for base classes
- Add description in header of each test/sequence



#### Common coding Guidelines

- Common indentation level = 2
- No TABs
- Use one file per module/class/interface except for specific cases
- Identifiers should use lower\_case\_with\_underscores except for parameters, enum literals, constants and `defines which use UPPER\_CASE\_WITH\_UNDERSCORE
- Macros may use lower\_case\_with\_underscore if they provide procedural code
- Add label for endclass delimeters, begin end blocks
- All base classes should start with prefix kb\_
- All base macros should start with prefix kb\_macro\_
- Use prefix m\_ before the name of user-defined class members (properties).
   Exception for ports/exports and vif
- Use prefix \_ ? for private members
- Use prefix h\_ when you get handles from config\_db or when you upcast components/objects
  - These guidelines are consistent with UVM base class library

#### Common coding Guidelines

- Use suffixes \_env, \_agent, \_test, \_drv, \_mon, \_sqr, \_vsqr, \_seq, \_vseq, \_sb, \_trans for corresponding classes except base classes
- Use suffix \_cfg for user-defined configuration classes
- When configuration objects are referenced from config\_db, field name should be "cfg"
- Use suffix \_port / \_export for corresponding port/export instance. They do not need m\_ prefix since they are always class member variables.
- Use suffix \_vif for virtual interfaces
- Use suffix \_t for user-defined typedef
- Use suffix \_e for enumerated types
- Use suffix \_cb for clocking blocks
- Use suffix \_mp for modports
- Use suffix \_cg for covergroups
- Use suffix \_ctr for constraints
- Use suffix \_pkg for user-defined packages
- Do not use UVM deprecated features
- Do not use internal features of UVM that are not documented
  - Use conditional guards to avoid compiling the same include file more than once

#### Common coding Guidelines

- Primary focus should be reusability, we should avoid introducing dependencies that would prevent subsequent reuse
- Each class should be defined within a package
- Do not use wildcard import at compilation unit scope (outside module/package declaration)
- Env should be written so that they can be integrated in another top env
- All class should be registered in the factory with corresponding macros
- Always create objects/components through the factory
- Handle name should match string instance name of factory
- Use new constructor for covergroup and port/exports creations only
- Use build\_phase for building other elements



#### Coding Guideline file structure

- File structure
- Common header
- Include guards
- Possible include files
- Class declaration
- All class should be registered in the factory with corresponding macros
- Covergroup definition
- Declare ports, exports, and virtual interfaces
- Declare any member variables
- Constraints declaration
- After any member variables, define constructor/ covergroup creation
- If class implements multiple phase methods, keep their order in the file. First declare build\_phase, connect, ...
- Other functions use extern if many lines of code
- Enclass
  - `endif

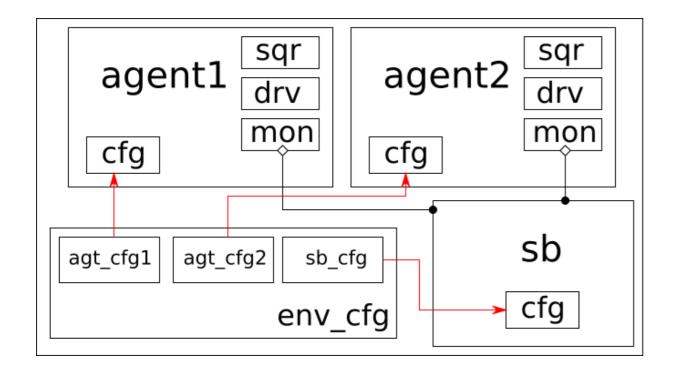


#### Coding Guidelines: env

- Inside env we can find following structure
  - Agents
  - Scoreboards
  - Configs
  - Exports/Port forwarding
  - Subscribers
- Each env may be reused at higher level so only put components that can be reused: no virtual sequencer, no bus agent.
- Scoreboard and their connections are placed inside the env.
- Env has also its own config containing sub configs for the agents and scoreboards



## Coding Guidelines: env





#### Coding Guidelines: agent

- For agent base classes use following naming style
  - Kb\_VIP\_monitor
  - Kb\_VIP\_driver
  - Kb\_VIP\_sequencer



### Coding Guidelines: packages

• Group includes for typedef, sequences, components in svh files



#### Coding Guidelines: uvm\_sequence

- For any common code use pre/post\_start instead of pre/post\_body because you are not sure if the latter method will actually be called
- Use macro declare\_p\_sequencer only when the sequence needs to access members of the sequencer on which it is running



# Backup



# KANDOU reinventing the BUS

