

# Verification Environments Overview

08<sup>th</sup> June 2018

# Types of Verification

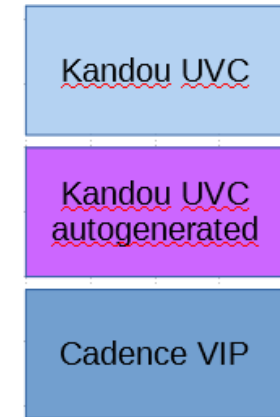
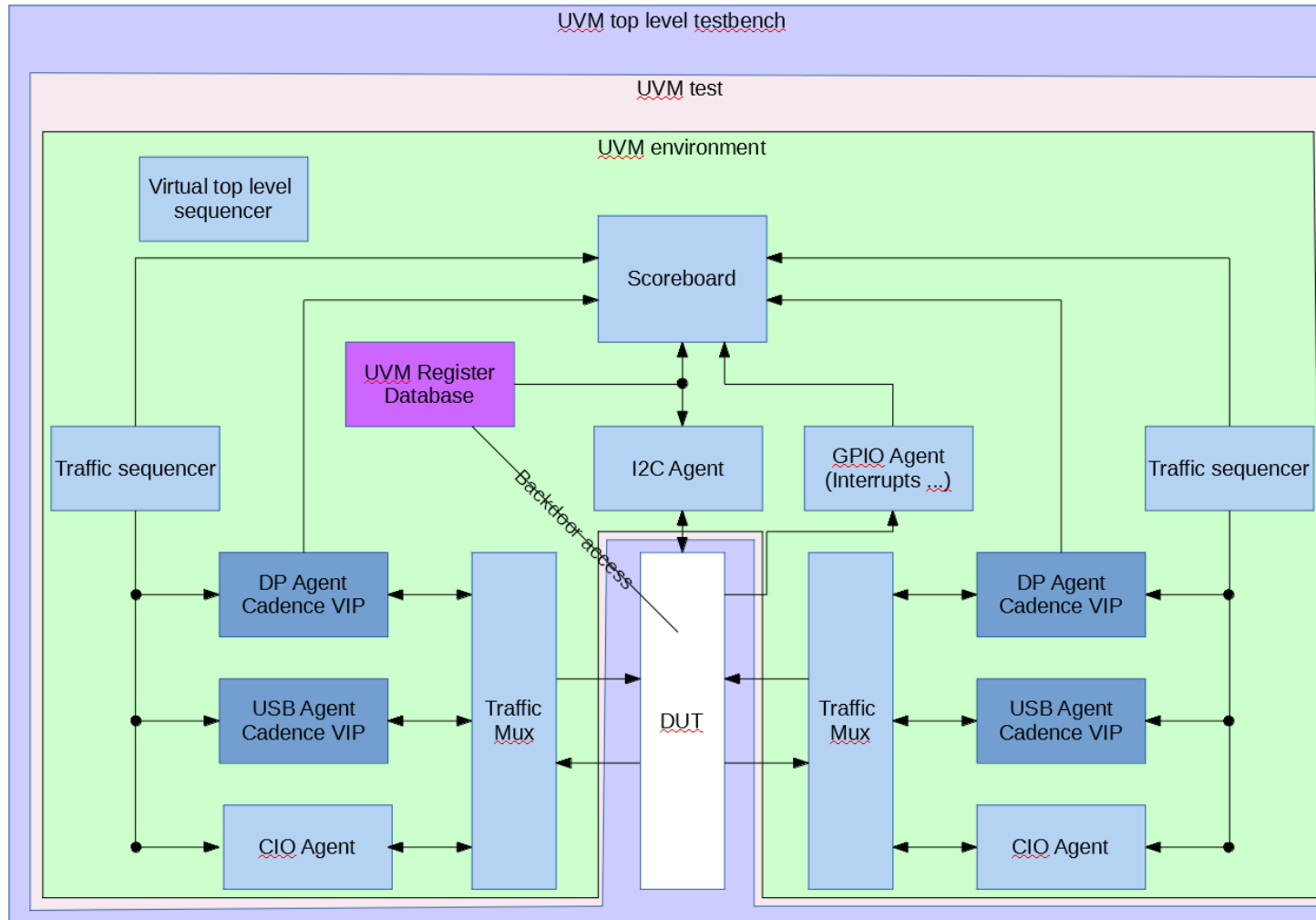
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- Similar setups for both IP and chip level
- UVM based simulation envs
  - RAL (uvm Reg)
  - VIPs integrated as part of the same environment.
- Formal
- Co-simulations
  - Both AoT (AMS) and DoT (DMS)
- FPGA prototyping

# Chip Level Testbench Architecture

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# Single DUT



# Serdes IP Testbench Architecture

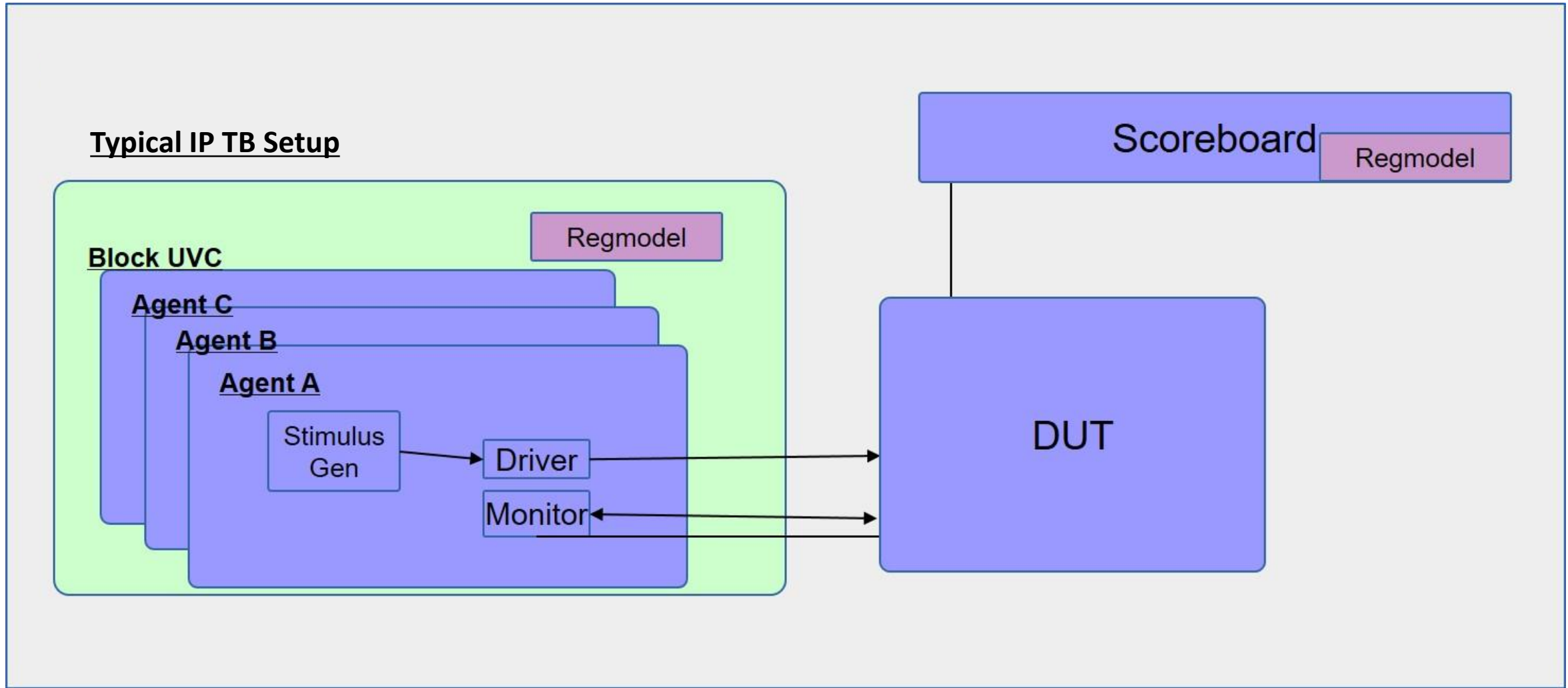
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# SerdesTestbench Architecture

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- Main simulation environment is UVM based.
- Analog modelled using Verilog.
  - Models are done at lower level as possible to preserve full hierarchy.
  - Some blocks can be swapped with wreals or AMS if required
- Using the same environment for DMS
- Also have a separate AMS environment driven from ADEXL (mainly for co-simulation of tightly coupled loops)

# SerdesTestbench Architecture



# Other verification environments

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# Formal strategy

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- Apps
  - Unreachable Coverage Elimination (with assumptions)
  - Connectivity
  - Control Register Verification
  - CDC / Reset checks
  - Formal property verification (FPV)
- Jasper is our formal verification tool.
- Assumptions (constraints) are reviewed and cross checked in simulation.

# Analog/Digital Co-simulations

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- Mainly for IP level to check loops between analog and digital.
  - Leverage existing UVM envs by using DMS based flow.
  - Assertions added for self checking
  - Powerup/down / reset
  - Co-simulation can be done using
    - VerilogA/AMS
    - Schematic
    - Extracted

# Regression Management

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## Regression management

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- In-house regression script
- Vmanager now also in use on one of the projects.
- Jenkins as CI tool

# Tools Summary

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# Tools

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- Simulation
  - Xcelium/Incisive
- AMS
  - Spectre/Ultrsim/Xcelium
  - DMS2.0
- Formal
  - Jasper Gold
- Test-planning
  - In-house spreadsheet based flow
  - Vmanager
- Coverage Analysis
  - IMC / Vmanager
- Continuous Integration and Regression Scheduler
  - Jenkins

# Thank You

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# Backup

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# KANDOU reinventing the BUS

