BEACON TECHNOLOGY FOR SAFE MOVEMENT OF DISABLED PEOPLE

A PROJECT REPORT

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in partial fulfillment for the award of the degree

of

BACHELOR OF ENGINEERING

IN

ELECTRONICS AND COMMUNICATION ENGINEERING
(NBA Accredited)

GOVERNMENT COLLEGE OF ENGINEERING, SALEM-636 011.
(An Autonomous Institution affiliated to Anna University, Chennai, Accredited by NAAC.)

MAY 2023

GOVERNMENT COLLEGE OF ENGINEERING,

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BONAFIDE CERTIFICATE

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ACKNOWLEDGEMENT

At this delightful moment of having successfully completed our project, we convey our sincere thanks and gratitude to our beloved Principal **Dr.R.MALAYALAMURTHI,** for providing us the great opportunity with all facilities required for the successful completion of our project work.

We wish to express our gratitude and profound thanks to our Head of the Department, **Dr.A.M.KALPANA**, Department of Electronics and Communication Engineering, Government College of Engineering, Salem, for forwarding us to do our project and offering adequate duration and constant encouragement in completing project work.

We wish to record my deep sense of gratitude and profound thanks to our Project Supervisor **D.MANIBHARATHI,** Assistant Professor, Department of Electronics and Communication Engineering, Government College of Engineering, Salem, who has induced to innovate this project with technological intents, inspiring guidance, keen interest and constant encouragement throughout the course of project work, to bring this report into fruition.

We would like to thank the Project Review Committee Members for their comments which help to improve the overall quality of the project work. We also convey our sincere thanks to all the Teaching faculty and non-teaching staff members of our department, for their kind help and valuable support which facilitate us to complete the project work successfully. Finally, we wish to express our heartfelt thanks to our beloved parents and all our friends for the kindly help rendered by them.

ABSTRACT

This proposed beacon technology for safe movement of disabled people is to improve the efficiency and effectiveness of people navigation in indoors. The visually impaired people faces extreme difficulties while travelling to new places. While GPS can provide a reliable mode of navigation in outdoors, it becomes a hard task to navigate indoors without reliable location data. In this project we have proposed a solution to tackle this problem using a Zigbee technology called beacons. This technology helps to navigate within a room without sight or others help. This technology is a advanced feature for the disabled people by indicating all the obstacles in the way and it guide the person with the audio control under a roof of certain circumference. This technology in addition saves the times for navigation and gives the confidents to them to travel and manages themselves alone. The project has the potential to significantly improve the mobility and independence of individuals with disabilities, while also promoting greater inclusivity and accessibility in public spaces.

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CHAPTER - 1
INTRODUCTION

INTRODUCTION

Individuals with disabilities face a range of challenges in their daily lives, particularly when it comes to mobility and independent living. Navigating public spaces can be particularly difficult, with hazards such as crowded areas, and traffic making it hard for individuals with disabilities to move around safely. This beacon technology has the potential to address some of these challenges, promoting safer and more accessible environments for individuals with disabilities. This project aims to leverage beacon technology to develop a system that promotes safe movement for visually disabled people. Beacons are small wireless devices that transmit signals over short distances, typically using Zigbee technology. By placing beacon devices in designated areas, such as sidewalks, crossings, and other points of interest, the system can provide audio signals and tactile feedback to visually disabled people as they navigate their environment. The goal is to enabling them to navigate public spaces more safely and confidently.

1.1 OVERVIEW PROPOSED SYSTEM

- The proposed system for the Beacon Technology Safe Movement of Disable People project will consist of a network of beacon devices. The beacons will transmit signals through audio commands via ZigBee technology, which will alert users to potential hazards and guide them through their environment.
- It will include a feature like voice commands to accommodate users with visual impairments. The data collected from the beacon devices will be analyzed to identify patterns and trends in user behavior and environment, which can be used to optimize the system's performance over time.
- The system will be designed to be scalable, allowing for additional beacon devices to be added as needed to expand the network's coverage.

CHAPTER – 2
LITERATURE SURVEY

LITERATURE SURVEY

"A Review on Beacon-Based Technologies for Smart Tourism Destinations" by J. Yoon et al.: This paper provides an overview of how beacon technology can be used in the tourism industry to enhance visitor experiences. The authors discuss various applications of beacon technology, such as providing location-based information and personalized recommendations to tourists.

"A Comprehensive Study on the Role of Beacon Technology in the Internet of Things" by S. K. Jayapal and S. K. Jayapal: This paper provides a comprehensive review of beacon technology and its applications in the Internet of Things (IoT). The authors discuss how beacon technology can be used for asset tracking, indoor navigation, and location-based services.

"Beacon Technology in Healthcare: A Review" by D. M. Babu et al.: This paper provides a review of how beacon technology can be used in the healthcare industry. The authors discuss various applications of beacon technology, such as tracking patient movements within hospitals and providing location-based information to medical staff.

"Beacon-based System for Smart Traffic Management" by P. S. Khajone et al.: This paper presents a system that uses beacons to manage traffic flow in urban areas. The system includes a mobile application that communicates with the beacons and provides real-time traffic information to drivers.

"Beacon-Based Indoor Positioning Systems: A Survey" by K. Wu et al.: This paper provides a survey of the state-of-the-art in beacon-based indoor positioning systems. The authors discuss various beacon-based positioning technologies and their strengths and weaknesses.

"Beacons in the Wild: A Survey of Augmented Reality Experiences Using Bluetooth Low Energy Beacons" by J. C. Lee et al.: This paper provides a survey of augmented reality experiences that use Bluetooth Low Energy (BLE) beacons. The authors discuss various applications of beacon-based augmented reality, such as navigation and gaming.

"A Survey of Beacon Technology and Its Applications in Location-Based Services" by L. Sun et al.: This paper provides a survey of beacon technology and its applications in location-based services. The authors discuss various beacon-based technologies, such as iBeacon and Eddystone, and their potential use cases.

"Beacon Technology: A Survey and Future Directions" by S. Garg and M. Kumar: This paper provides a survey of beacon technology and its applications. The authors discuss various beacon-based technologies, such as iBeacon and Eddystone, and their strengths and weaknesses.

CHAPTER – 3
BLOCK DIAGRAM AND CIRCUIT DIAGRAM

BLOCK DIAGRAM AND CIRCUIT DIAGRAM

3.1 BLOCKDIAGRAM

In this project, the components that are used for making an easy and wearable device are connected as per the block diagram drawn below. These sensors are working and processing data from one place to another with the help of power supply which is also used for this project.

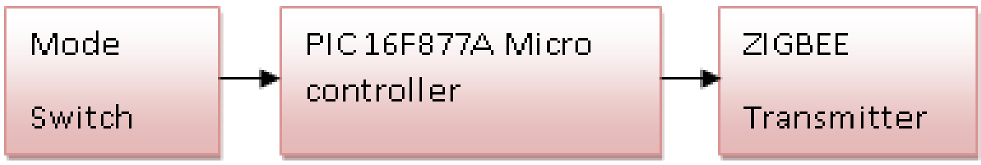

Fig.3.1 Block Diagram of Transmitter

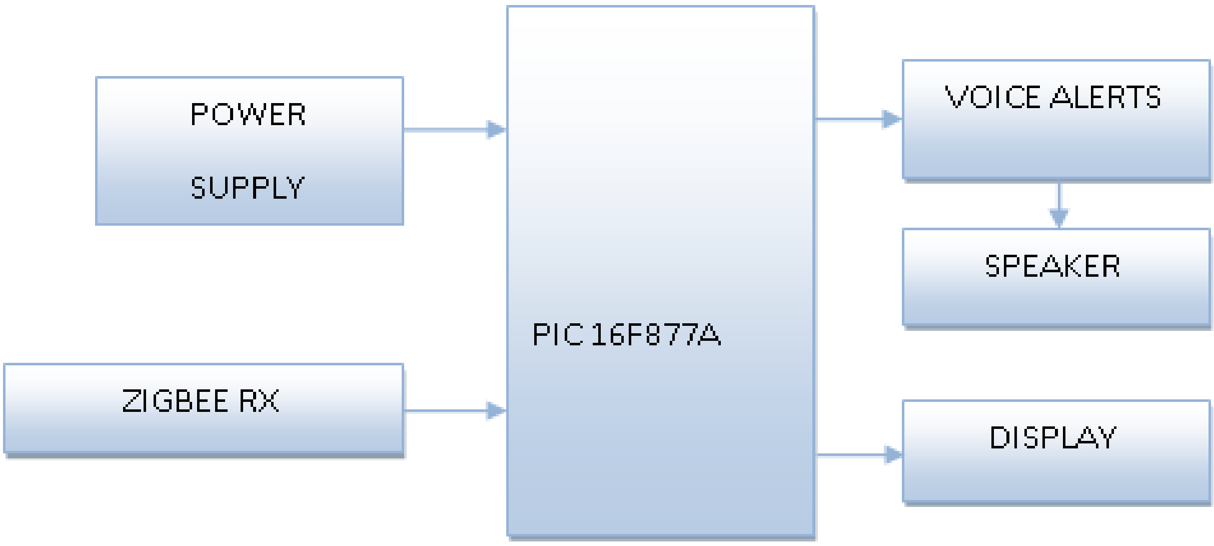

Fig.3.2 Block Diagram of Receiver

3.1.1 HARDWARE REQUIREMENTS:

- PIC16F877A Microcontroller
- Zigbee Module
- LCD Display unit
- Power Supply
- Switch
- Speaker
- Voice Playback chip

3.1.2 SOFTWARE REQUIREMENTS:

- MP LAB IDE 8.46
- HITECH ‘C’
- PIC KIT 3

3.2 CIRCUIT DIAGRAM

In this project, Zigbee transmitter and receivers are placed to stay connected. Voice playback chip is used to control the audio. Speaker is placed to deliver a voice output.

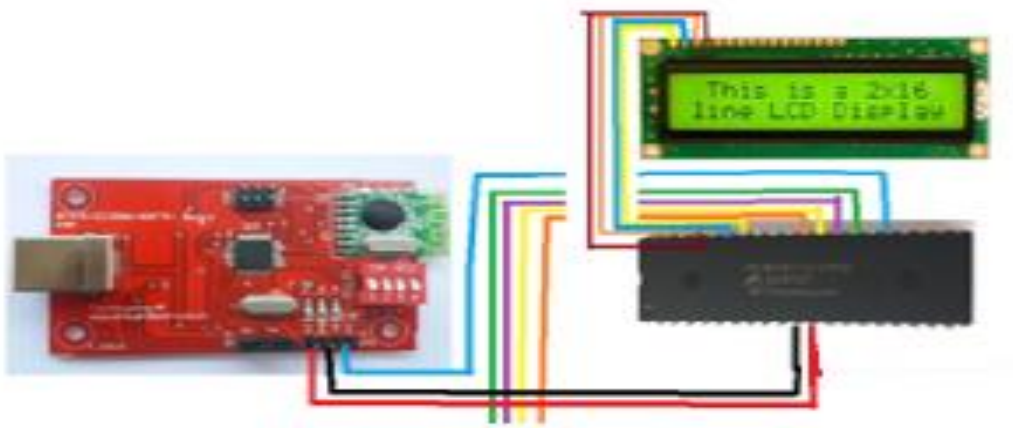

Fig.3.3 Circuit Diagram of Transmitter

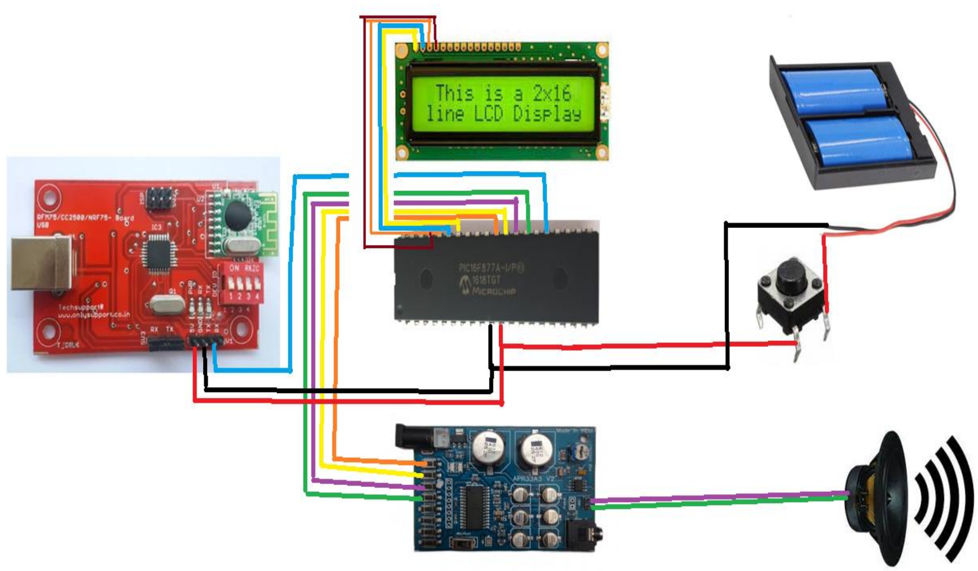

Fig.3.4 Circuit Diagram of Receiver

3.2.1 COMPONENTS USED IN THIS PROJECT:

The Components that are used for making our proposed system are,

1. PIC16F877A MICROCONTROLLER
2. ZIGBEE MODULE
3. LCD DISPLAY UNIT
4. POWER SUPPLY
5. SWITCH
6. SPEAKER
7. VOICE PLAYBACK CHIP

CHAPTER - 4
MODULE DESCRIPTION

MODULE DESCRIPTION

4.1.POWER SUPPLY

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in fig 19.1. The ac voltage, typically 120 V rms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

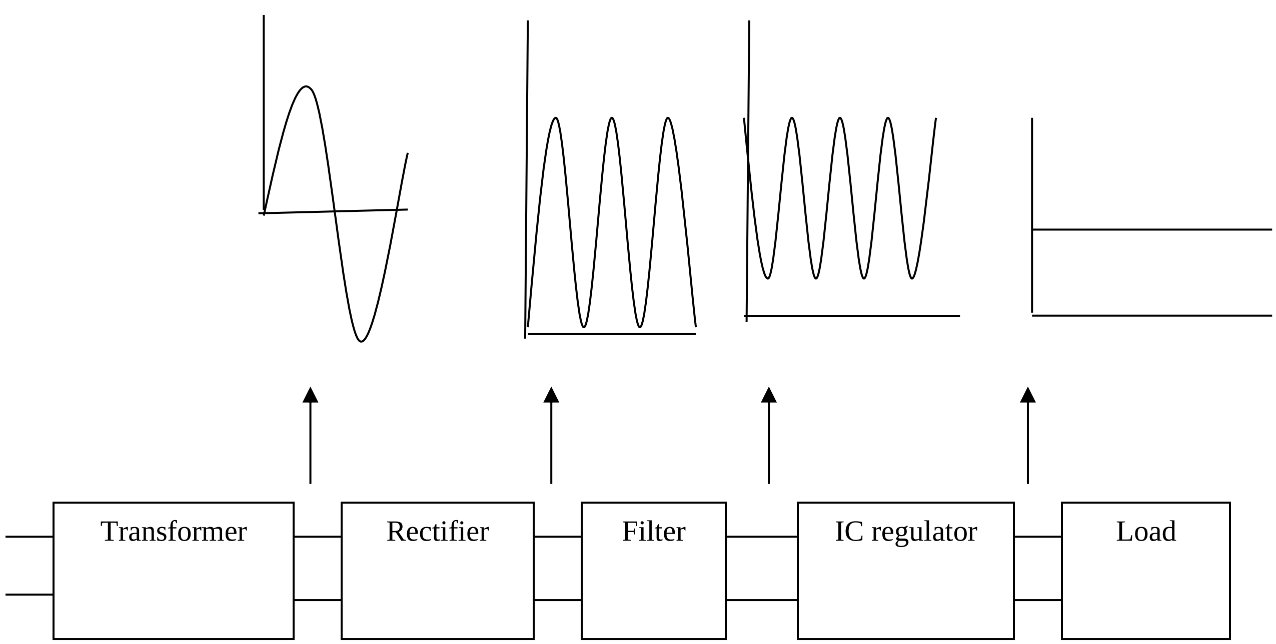

Fig.4.1 Block Diagram of Power Supply

4.2 PIC MICROCONTROLLER

PIC16F877A Microcontroller

- A family of Harvard architecture microcontrollers made by Microchip Technology
- PIC16F877A belongs to a class of 8bit microcontrollers of RISC architecture.
- The integrated circuits(IC) contained both processor and peripherals (Timers, ADC, USART,EEPROM,I2C,SSP,PSP) are inbuilt is called PIC microcontroller

4.2.1 PIC Microcontroller Overview/ Core Features:

- High performance RISC CPU
- Operating speed: DC (4 – 20) MHz clock input
- Only 35 single word instructions to learn
- Up to 8K x 14 words of FLASH Program Memory.
- Up to 368 x 8 bytes of Data Memory (RAM).
- Up to 256 x 8 bytes of EEPROM Data Memory
- Wide operating voltage range: 2.0V to 5.5V
- Interrupt capability (up to 14 sources)
- Eight level deep hardware stack
- Direct, indirect and relative addressing modes
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options

- All single cycle instructions except for program branches which are two cycles
- Low-power consumption:
  < 0.6 mA typical @ 3V, 4 MHz
  20 µA typical @ 3V, 32 kHz
  < 1µA typical standby current

Special Microcontroller Features

- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Low power, high speed CMOS FLASH/EEPROM technology
- Fully static design
- In-Circuit Serial Programming (ICSP) via two pins
- Single 5V In-Circuit Serial Programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- High Sink/Source Current: 25mA
- Commercial, Industrial and Extended temperature ranges

Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler,can be incremented during SLEEP via external crystal/clock

- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and post scaler
- Two Capture, Compare, PWM modules-Capture is 16-bit, max. resolution is 12.5 ns-Compare is 16-bit, max. resolution is 200 ns-PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI (Master mode) and I2C
- (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

4.2.2 Pin Description:

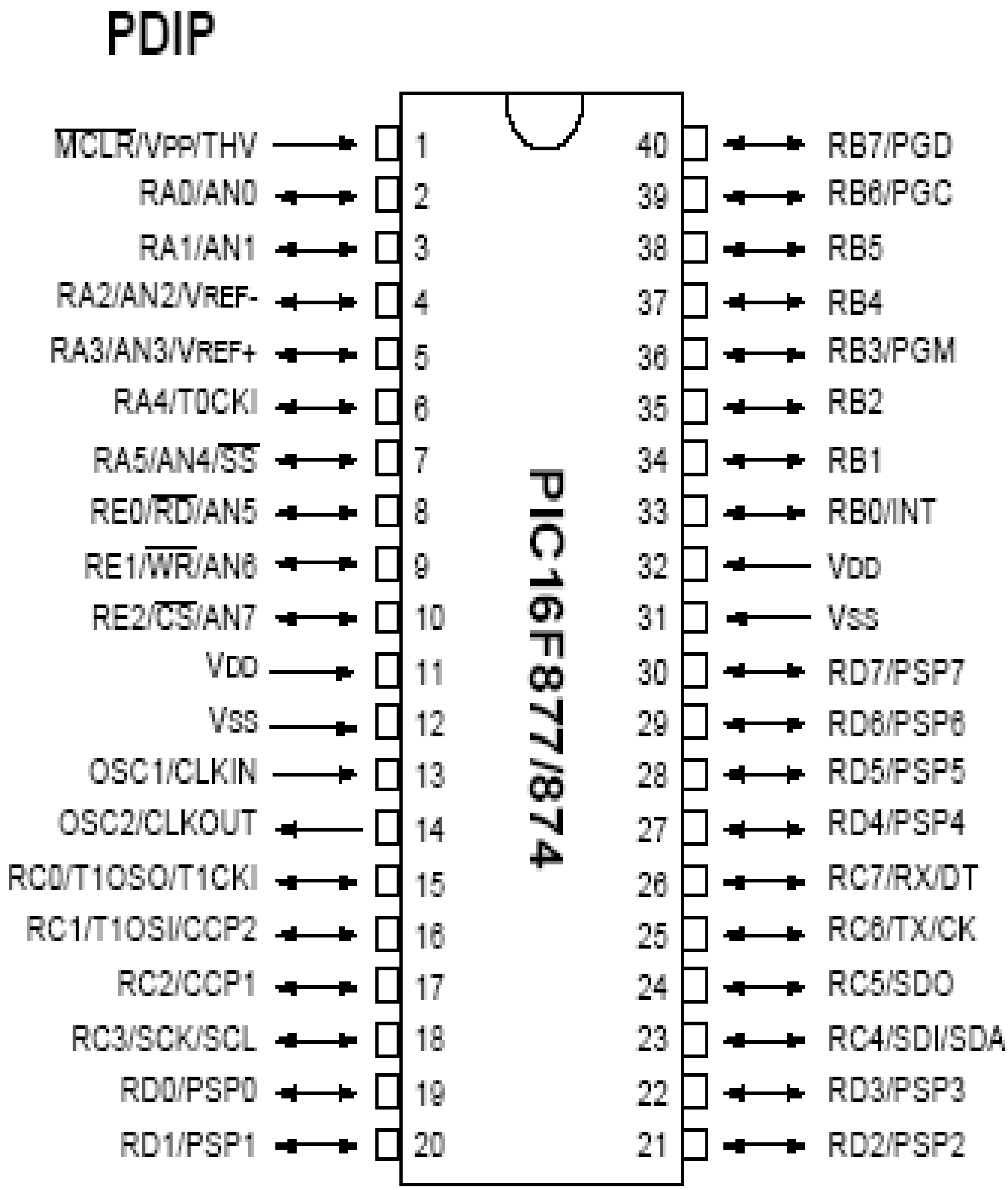

Fig.4.2 Pin Diagram of PIC Microcontroller

Pin Configuration:

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS(4)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{\text{MCLR}}$/VPP/THV	1	2	18	I/P	ST	Master clear (reset) input or programming voltage input or high voltage test mode control. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19	I/O	TTL	RA0 can also be analog input0
RA1/AN1	3	4	20	I/O	TTL	RA1 can also be analog input1
RA2/AN2/VREF-	4	5	21	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage
RA3/AN3/VREF+	5	6	22	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage
RA4/T0CKI	6	7	23	I/O	ST	RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type.
RA5/$\overline{\text{SS}}$/AN4	7	8	24	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(1)	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3/PGM	36	39	11	I/O	TTL	RB3 can also be the low voltage programming input
RB4	37	41	14	I/O	TTL	Interrupt on change pin.
RB5	38	42	15	I/O	TTL	Interrupt on change pin.
RB6/PGC	39	43	16	I/O	TTL/ST(2)	Interrupt on change pin or In-Circuit Debugger pin. Serial programming clock.
RB7/PGD	40	44	17	I/O	TTL/ST(2)	Interrupt on change pin or In-Circuit Debugger pin. Serial programming data.

Table 4.1 Pin Configuration

Block diagram:

Device	Program Flash	Data Memory	Data EEPROM
PIC16F874	4K	192 Bytes	128 Bytes
PIC16F877	8K	368 Bytes	256 Bytes

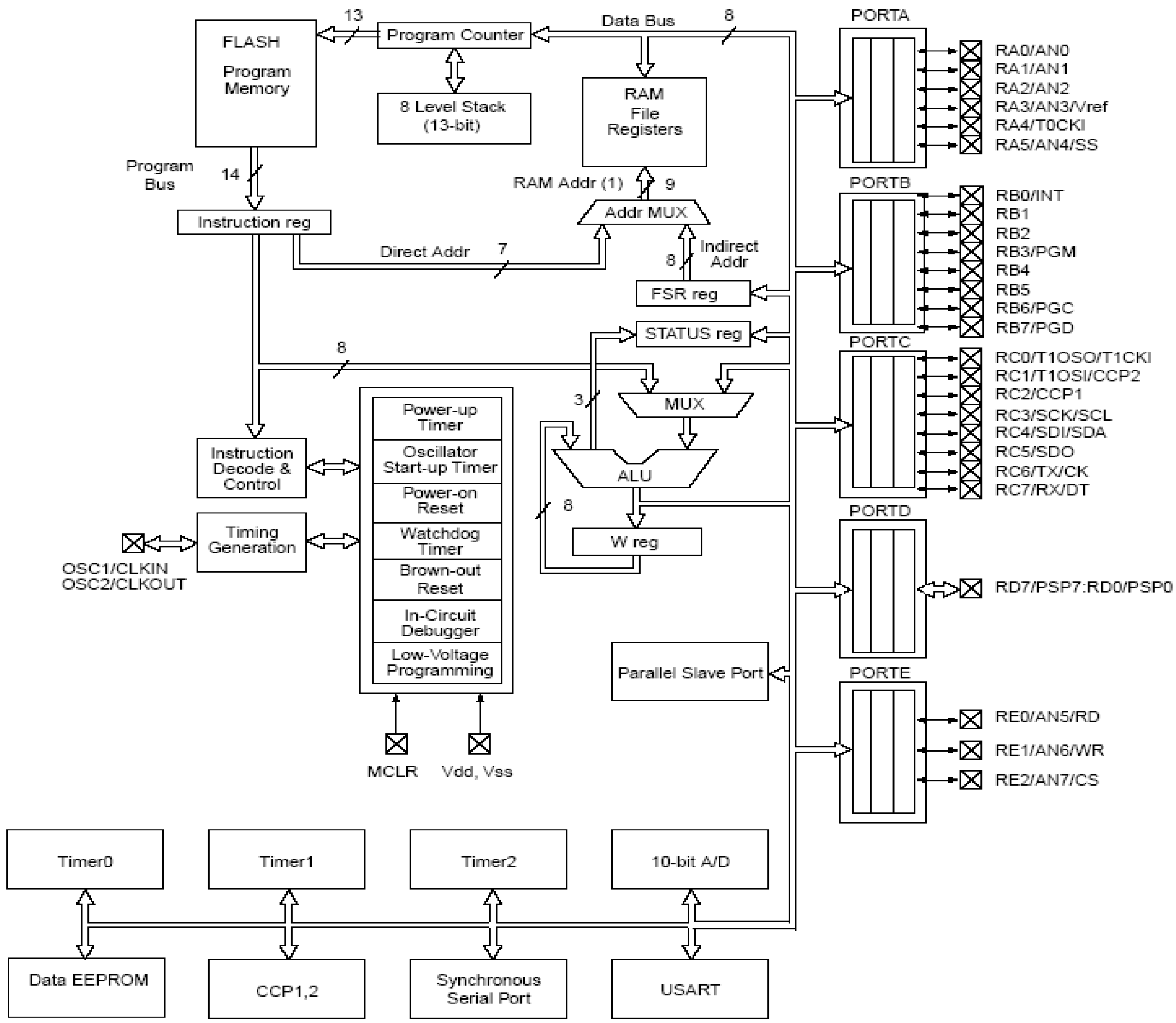

Fig.4.3 Block Diagram of Microcontroller

I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

PORT A and TRIS A Register:

PORTA is a 6-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input, i.e., put the corresponding output driver in a Hi-impedance mode. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output, i.e., put the contents of the output latch on the selected pin.

Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read; this value is modified, and then written to the port data latch. Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. Other PORTA pins are multiplexed with analog inputs and analog VREF input. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input
RA1/AN1	bit1	TTL	Input/output or analog input
RA2/AN2	bit2	TTL	Input/output or analog input
RA3/AN3/VREF	bit3	TTL	Input/output or analog input or VREF
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0 Output is open drain type
RA5/$\overline{SS}$/AN4	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input

Table.4.2 PORT A Function

PORT B and TRIS B Register

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input, i.e., put the corresponding output driver in a hi-impedance mode.

Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output, i.e., put the contents of the output latch on the selected pin. Three pins of PORTB are multiplexed with the Low Voltage Programming function; RB3/PGM, RB6/PGC and RB7/PGD. The alternate functions of these pins are described in the Special Features Section. Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR 'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>). This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.

b) Clear flag bit RBIF. A mismatch condition will continue to set flag bit RBIF. The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature. This interrupt on mismatch feature, together with software configurable pull-ups on these four pins, allow easy interface to a keypad and make it possible for wake-up on key depression

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM	bit3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6/PGC	bit6	TTL/ST(2)	Input/output pin (with interrupt on change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit7	TTL/ST(2)	Input/output pin (with interrupt on change) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming data.

Table.4.3 PORT B Function

PORT C and TRIS C Register

PORT C is an 8-bit wide bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (=1) will make the corresponding PORTC pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISC bit (=0) will make the corresponding PORTC pin an output, i.e., put the contents of the output latch on the selected pin. PORTC is multiplexed with several peripheral functions.PORTC pins have Schmitt Trigger input buffers.

When the I2C module is enabled, the PORTC (3:4) pins can be configured with normal I2C levels or with SMBUS levels by using the CKE bit (SSPSTAT <6>). When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit.

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/ Compare2 output/PWM2 output
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I^2C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data output
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit or Synchronous Clock
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive or Synchronous Data

Table.4.4 PORT C Function

PORT D and TRIS D Registers

This section is not applicable to the 28-pin devices. PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor Port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL(1)	Input/output port pin or parallel slave port bit0
RD1/PSP1	bit1	ST/TTL(1)	Input/output port pin or parallel slave port bit1
RD2/PSP2	bit2	ST/TTL(1)	Input/output port pin or parallel slave port bit2
RD3/PSP3	bit3	ST/TTL(1)	Input/output port pin or parallel slave port bit3
RD4/PSP4	bit4	ST/TTL(1)	Input/output port pin or parallel slave port bit4
RD5/PSP5	bit5	ST/TTL(1)	Input/output port pin or parallel slave port bit5
RD6/PSP6	bit6	ST/TTL(1)	Input/output port pin or parallel slave port bit6
RD7/PSP7	bit7	ST/TTL(1)	Input/output port pin or parallel slave port bit7

Table.4.5 PORT D Function

PORT E and TRIS E Register

PORTE has three pins RE0/RD/AN5, RE1/WR/AN6 and RE2/CS/AN7, which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers.

The PORTE pins become control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs). Ensure ADCON1 is configured for digital I/O. In this mode the input buffers are TTL.

PORTE pins are multiplexed with analog inputs. When selected as an analog input, these pins will read as '0's. TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Name	Bit#	Buffer Type	Function
RE0/$\overline{RD}$/AN5	bit0	ST/TTL(1)	Input/output port pin or read control input in parallel slave port mode or analog input: $\overline{RD}$ 1 = Not a read operation 0 = Read operation. Reads PORTD register (if chip selected)
RE1/$\overline{WR}$/AN6	bit1	ST/TTL(1)	Input/output port pin or write control input in parallel slave port mode or analog input: $\overline{WR}$ 1 =Not a write operation 0 =Write operation. Writes PORTD register (if chip selected)
RE2/$\overline{CS}$/AN7	bit2	ST/TTL(1)	Input/output port pin or chip select control input in parallel slave port mode or analog input: $\overline{CS}$ 1 = Device is not selected 0 = Device is selected

Table.4.6 PORT E Function

Memory Organization

There are three memory blocks in each of the PIC16f877 MUCs. The program memory and Data Memory have separate buses so that concurrent access can occur.

Program Memory Organization

The PIC16f877 devices have a 13-bit program counter capable of addressing

8K *14 words of FLASH program memory. Accessing a location above the physically implemented address will cause a wraparound.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

Data Memory Organization

The data memory is partitioned into multiple banks which contain the General-Purpose Registers and the special functions Registers. Bits RP1 (STATUS<6) and RP0 (STATYUS<5>) are the bank selected bits.

Each bank extends up to 7Fh (1238 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain special function registers. Some frequently used special function registers from one bank may be mirrored in another bank for code reduction and quicker access.

4.3 LCD DISPLAY:

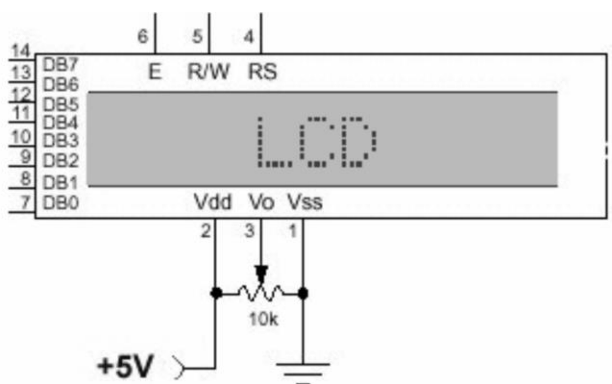

Fig.4.4 Pin Configuration of LCD

Liquid crystal displays (LCDs) have materials which combine the properties of both liquids and crystals. Rather than having a melting point, they have a temperature range within which the molecules are almost as mobile as they would be in a liquid, but are grouped together in an ordered form similar to a crystal.

An LCD consists of two glass panels, with the liquid crystal material sand witched in between them. The inner surface of the glass plates is coated with transparent electrodes which define the character, symbols or patterns to be displayed polymeric layers are present in between the electrodes and the liquid crystal, which makes the liquid crystal molecules to maintain a defined orientation angle.

One each polarizer is pasted outside the two glass panels. These polarizers would rotate the light rays passing through them to a definite angle, in a particular direction. When the LCD is in the off state, light rays are rotated by the two polarizers and the liquid crystal, such that the light rays come out of the LCD without any orientation, and hence the LCD appears transparent.

When sufficient voltage is applied to the electrodes, the liquid crystal molecules would be aligned in a specific direction. The light rays passing through the LCD would be rotated by the polarizers, which would result in activating / highlighting the desired characters. The LCDs are lightweight with only a few millimeters thickness. Since the LCD's consume less power, they are compatible with low power electronic circuits, and can be powered for long durations.

Fig.4.5 Liquid Crystal Display

4.4 ZIGBEE MODULE

ZigBee is an established set of specifications for wireless personal area networking (WPAN), i.e., digital radio connections between computers and related devices.

WPAN Low Rate or ZigBee provides specifications for devices that have low data rates, consume very low power and are thus characterized by long battery life. ZigBee makes possible completely networked homes where all devices are able to communicate and be controlled by a single unit.

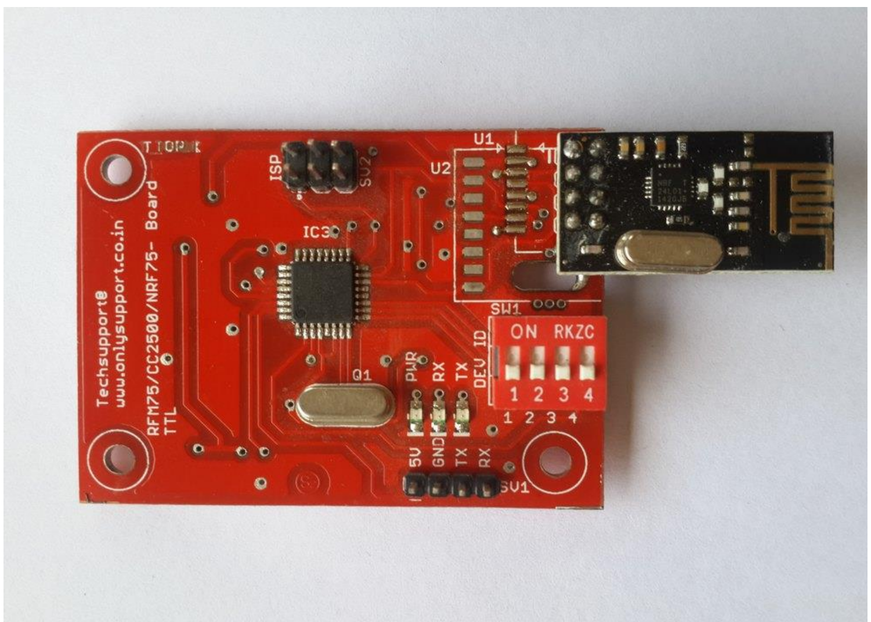

Fig.4.6 Zigbee Module

When you hold the TV remote and wish to use it you have to necessarily point your control at the device. This one-way, line-of-sight, short-range communication uses infrared (IR) sensors to enable communication and control and it is possible to operate the TV remotely only with its control unit.

Add other home theatre modules, an air- conditioner and remotely enabled fans and lights to your room, and you become a juggler who has to handle not only these remotes, but also more numbers that will accompany other home appliances you are likely to use.

Some remotes do serve to control more than one device after ‘memorizing' access codes, but this interoperability is restricted to LOS, that too only for a set of related equipment, like the different units of a home entertainment system Now picture a home with entertainment units, security systems including fire alarm, smoke detector and burglar alarm, air-conditioners and kitchen appliances all within whispering distance from each other and imagine a single unit that talks *with* all the devices, no longer depending on line-of-sight, and traffic no longer being one-way.

This means that the devices and the control unit would all need a common standard to enable intelligible communication. **ZigBee** is such a standard for embedded application software and has been ratified in late 2004 under IEEE 802.15.4 Wireless Networking Standards.

ZigBee is an established set of specifications for wireless personal area networking (WPAN), i.e., digital radio connections between computers and related devices. This kind of network eliminates use of physical data buses like USB and Ethernet cables. The devices could include telephones, hand-held digital assistants, sensors and controls located within a few meters of each other.

ZigBee is one of the global standards of communication protocol formulated by the relevant task force under the IEEE 802.15 working group. The fourth in the series, WPAN Low Rate/ZigBee is the newest and provides specifications for devices that have low data rates, consume very low power and are thus characterized by long battery life. Other standards like Bluetooth and IrDA address high data rate applications such as voice, video and LAN communications.

The ZigBee Alliance has been set up as “an association of companies working together to enable reliable, cost-effective, low-power, wirelessly networked, monitoring and control products based on an open global standard”.

Once a manufacturer enrols in this Alliance for a fee, he can have access to the standard and implement it in his products in the form of ZigBee chipsets that would be built into the end devices. Philips, Motorola, Intel, HP are all members of the Alliance The goal is “to provide the consumer with ultimate flexibility, mobility, and ease of use by building wireless intelligence and capabilities into every day devices. ZigBee technology will be embedded in a wide range of products and applications across consumer, commercial, industrial and government markets worldwide. For the first time, companies will have a standards-based wireless platform optimized for the unique needs of remote monitoring and control applications, including simplicity, reliability, low-cost and low-power”.

The target networks encompass a wide range of devices with low data rates in the Industrial, Scientific and Medical (ISM) radio bands, with building-automation controls like intruder/fire alarms, thermostats and remote (wireless) switches, video/audio remote controls likely to be the most popular applications. So far sensor and control devices have been marketed as proprietary items for want of a standard. With acceptance and implementation of ZigBee, interoperability will be enabled in multi-purpose, self-organizing mesh networks

4.4.1Architecture

Though WPAN implies a reach of only a few meters, 30 feet in the case of ZigBee, the network will have several layers, so designed as to enable intrapersonal communication within the network, connection to a network of higher level and ultimately an uplink to the Web.

The ZigBee Standard has evolved standardized sets of solutions, called ‘layers. These layers facilitate the features that make ZigBee very attractive: low cost, easy implementation, reliable data transfer, short-range operations, very low power consumption and adequate security features.

1. Network and Application Support layer : The network layer permits growth of network sans high power transmitters. This layer can handle huge numbers of nodes. This level in the ZigBee architecture includes the ZigBee Device Object (ZDO), user-defined application profile(s) and the Application Support (APS) sub-layer.

The APS sub-layer's responsibilities include maintenance of tables that enable matching between two devices and communication among them, and also discovery, the aspect that identifies other devices that operate in the operating space of any device.

The responsibility of determining the nature of the device (Coordinator / FFD or RFD) in the network, commencing and replying to binding requests and ensuring a secure relationship between devices rests with the ZDO (Zigbee Define Object). The user-defined application refers to the end device that conforms to the ZigBee Standard.

2. Physical (PHY) layer : The IEEE802.15.4 PHY physical layer accommodates high levels of integration by using direct sequence to permit simplicity in the analog circuitry and enable cheaper implementations.

3. Media access control (MAC) layer : The IEEE802.15.4 MAC media access control layer permits use of several topologies without introducing complexity and is meant to work with large numbers of devices.

Device Types

There are three different ZigBee device types that operate on these layers in any self-organizing application network.

These devices have 64-bit IEEE addresses, with option to enable shorter addresses to reduce packet size, and work in either of two addressing modes – star and peer-to-peer.

1. The ZigBee coordinator node : There is one, and only one, ZigBee coordinator in each network to act as the router to other networks, and can be likened to the root of a (network) tree. It is designed to store information about the network.

2. The full function device FFD : The FFD is an intermediary router transmitting data from other devices. It needs lesser memory than the ZigBee coordinator node, and entails lesser manufacturing costs. It can operate in all topologies and can act as a coordinator.

3. The reduced function device RFD : This device is just capable of talking in the network; it cannot relay data from other devices. Requiring even less memory, (no flash, very little ROM and RAM), an RFD will thus be cheaper than an FFD. This device talks only to a network coordinator and can be implemented very simply in star topology.

ZigBee Characteristics

The focus of network applications under the IEEE 802.15.4 / ZigBee standard includes the features of low power consumption, needed for only two major modes (Tx/Rx or Sleep), high density of nodes per network, low costs and simple implementation.

These features are enabled by the following characteristics (technical data)

- *2.4GHz and 868/915 MHz dual PHY modes*. This represents three license-free bands: 2.4-2.4835 GHz, 868-870 MHz and 902-928 MHz. The number of channels allotted to each frequency band is fixed at sixteen (numbered 11-26), one (numbered 0) and ten (numbered 1-10) respectively. The higher frequency band is applicable worldwide, and the lower band in the areas of North America, Europe, Australia and New Zealand .

- Low power consumption, with battery life ranging from months to years. Considering the number of devices with remotes in use at present, it is easy to see that more numbers of batteries need to be provisioned every so often, entailing regular (as well as timely), recurring expenditure. In the ZigBee standard, longer battery life is achievable by either of two means: continuous network connection and slow but sure battery drain, or intermittent connection and even slower battery drain.

- Maximum data rates allowed for each of these frequency bands are fixed as 250 kbps @2.4 GHz, 40 kbps @ 915 MHz, and 20 kbps @868 MHz

- High throughput and low latency for low duty-cycle applications (<0.1%)

• Channel access using Carrier Sense Multiple Access with Collision Avoidance (CSMA - CA)

• Addressing space of up to 64-bit IEEE address devices, 65,535 networks

• 50m typical range

• Fully reliable “hand-Shaked” data transfer protocol.

• Different topologies as illustrated below: star, peer-to-peer, mesh

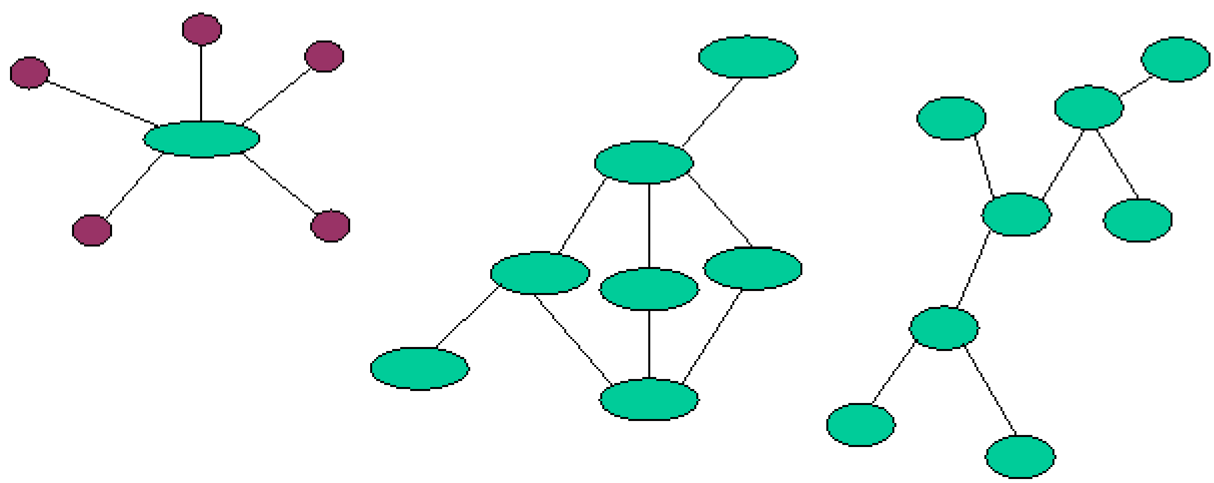

Fig.4.7 Zigbee Topology

Traffic Types

ZigBee/IEEE 802.15.4 addresses three typical traffic types. IEEE 802.15.4 MAC can accommodate all the types.

1. Data is *periodic*. The application dictates the rate, and the sensor activates, checks for data and deactivates.

2. Data is *intermittent*. The application, or other stimulus, determines the rate, as in the case of say smoke detectors. The device needs to connect to the network only when communication is necessitated. This type enables optimum saving on energy.

3. Data is *repetitive*, and the rate is fixed a priori. Depending on allotted time slots, called GTS (guaranteed time slot), devices operate for fixed durations.

ZigBee employs either of two modes, beacon or non-beacon to enable the to-and-fro data traffic. Beacon mode is used when the coordinator runs on batteries and thus offers maximum power savings, whereas the non-beacon mode finds favour when the coordinator is mains-powered.

In the beacon mode, a device watches out for the coordinator's beacon that gets transmitted at periodically, locks on and looks for messages addressed to it. If message transmission is complete, the coordinator dictates a schedule for the next beacon so that the device ‘goes to sleep'; in fact, the coordinator itself switches to sleep mode.

While using the beacon mode, all the devices in a mesh network know when to communicate with each other. In this mode, necessarily, the timing circuits have to be quite accurate, or wake up sooner to be sure not to miss the beacon. This in turn means an increase in power consumption by the coordinator's receiver, entailing an optimal increase in costs.

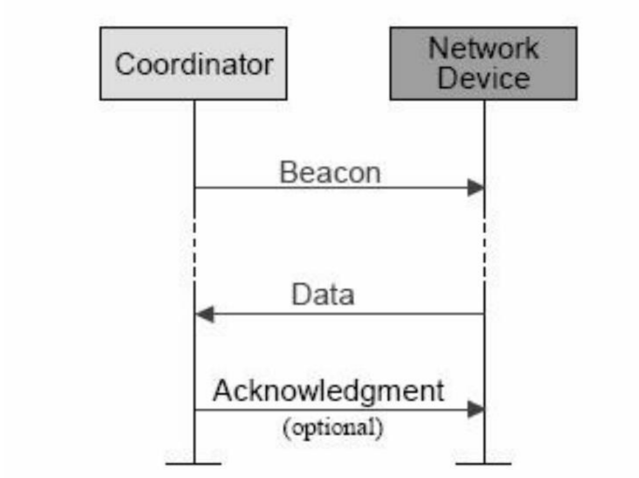

Fig.4.8 ***Beacon Network Communication***

The non-beacon mode will be included in a system where devices are ‘asleep' nearly always, as in smoke detectors and burglar alarms. The devices wake up and confirm their continued presence in the network at random intervals.

On detection of activity, the sensors ‘spring to attention', as it were, and transmit to the ever-waiting coordinator's receiver (since it is mains-powered). However, there is the remotest of chances that a sensor finds the channel busy, in which case the receiver unfortunately would ‘miss a call'.

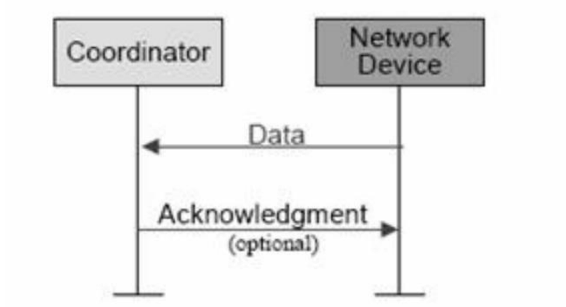

Fig.4.9 Non-*Beacon Network Communication*

Network Model

The functions of the coordinator, which usually remains in the receptive mode, encompass network set-up, beacon transmission, node management, storage of node information and message routing between nodes.

The network node, however, is meant to save energy (and so 'sleeps' for long periods) and its functions include searching for network availability, data transfer, checks for pending data and queries for data from the coordinator.

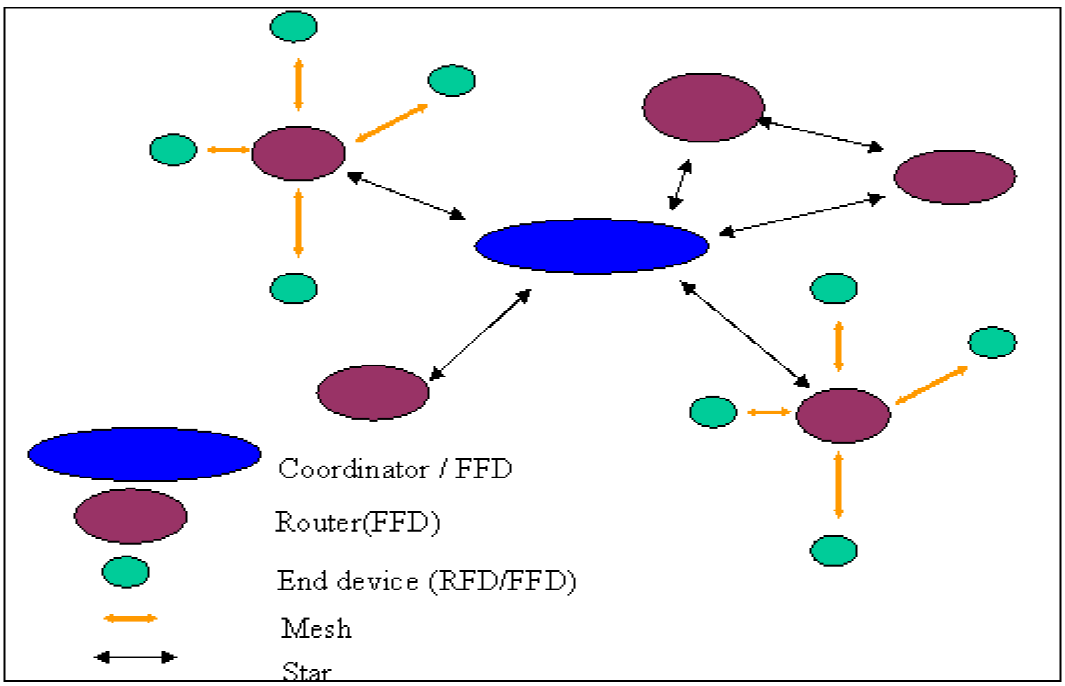

Fig.4.10 ***ZigBee Network Model***

For the sake of simplicity without jeopardising robustness, this particular IEEE standard defines a quartet frame structure and a super-frame structure used optionally only by the coordinator.

The four frame structures are

- Beacon frame for transmission of beacons
- Data frame for all data transfers
- Acknowledgement frame for successful frame receipt confirmations
- MAC command frame

These frame structures and the coordinator's super-frame structure play critical roles in security of data and integrity in transmission.

All protocol layers contribute headers and footers to the frame structure, such that the total overheads for each data packet range are from 15 octets (for short addresses) to 31 octets (for 64-bit addresses).

The coordinator lays down the format for the super-frame for sending beacons after every 15.38 Ms or/and multiples thereof, up to 252s. This interval is determined a priori and the coordinator thus enables sixteen time slots of identical width between beacons so that channel access is contention-less. Within each time slot, access is contention-based. Nonetheless, the coordinator provides as many as seven GTS (guaranteed time slots) for every beacon interval to ensure better quality.

IEEE 802.11b

With 802.11b WLANs, mobile users can get Ethernet levels of performance, throughput, and availability.

The basic architecture, features, and services of 802.11b are defined by the original 802.11 standard. The 802.11b specification affects only the physical layer, adding higher data rates and more robust connectivity.

The key contribution of the 802.11b addition to the wireless LAN standard was to standardize the physical layer support of two new speeds,5.5 Mbps and 11 Mbps.

To accomplish this, DSSS had to be selected as the sole physical layer technique for the standard since, as frequency hopping cannot support the higher speeds without violating current FCC regulations. The implication is that 802.11b systems will interoperate with 1 Mbps and 2 Mbps 802.11 DSSS systems, but will not work with 1 Mbps and 2 Mbps 802.11 FHSS systems.

The original 802.11 DSSS standard specifies an 11-bit chipping? Called a Barker sequence? To encode all data sent over the air. Each 11-chip sequence represents a single data bit (1 or 0), and is converted to a waveform, called a symbol, that can be sent over the air.

These symbols are transmitted at a 1 MPs (1 million symbols per second) symbol rate using technique called Binary Phase Shift Keying BPSK). In the case of 2 Mbps, a more sophisticated implementation called Quadrature Phase Shift Keying (QPSK) is used; it doubles the data rate available in BPSK, via improved efficiency in the use of the radio bandwidth. To increase the data rate in the 802.11b standard, advanced coding techniques are employed.

Rather than the two 11-bit Barker sequences, 802.11b specifies Complementary Code Keying (CCK), which consists of a set of 64 8-bit code words. As a set, these code words have unique mathematical properties that allow them to be correctly distinguished from one another by a receiver even in the presence of substantial noise and multipath interference (e.g., interference caused by receiving multiple radio reflections within a building).

The 5.5 Mbps rate uses CCK to encode 4 bits per carrier, while the 11 Mbps rate encodes 8 bits per carrier. Both speeds use QPSK as the modulation technique and signal at 1.375 MPs. This is how the higher data rates are obtained. To support very noisy environments as well as extended range, 802.11b WLANs use dynamic rate shifting, allowing data rates to be automatically adjusted to compensate for the changing nature of the radio channel. Ideally, users connect at the full 11 Mbps rate.

However, when devices move beyond the optimal range for 11 Mbps operation, or if substantial interference is present, 802.11b devices will transmit at lower speeds, falling back to 5.5, 2, and 1 Mbps. Likewise, if the device moves back within the range of a higher-speed transmission, the connection will automatically speed up again. Rate shifting is a physical layer mechanism transparent to the user and the upper layers of the protocol stack.

One of the more significant disadvantages of 802.11b is that the frequency band is crowded, and subject to interference from other networking technologies, microwave ovens, 2.4GHz cordless phones (a huge market), and Bluetooth [Wireless Standards Up in the Air]. There are drawbacks to 802.11b, including lack of interoperability with voice devices, and no QoS provisions for multimedia content. Interference and other limitations aside, 802.11b is the clear leader in business and institutional wireless networking and is gaining share for home applications as well.

IEEE 802.11a

802.11a, is much faster than 802.11b, with a 54Mbps maximum data rate operates in the 5GHz frequency range and allows eight simultaneous channels [Emerging Technology: Wireless Lan Standards].

802.11a uses Orthogonal Frequency Division Multiplexing (OFDM), a new encoding scheme that offers benefits over spread spectrum in channel availability and data rate.

Channel availability is significant because the more independent channels that are available, the more scalable the wireless network becomes. 802.11a uses OFDM to define a total of 8 non-overlapping 20 MHz channels across the 2 lower bands. By comparison, 802.11b uses 3 non-overlapping channels.

All wireless LANs use unlicensed spectrum; therefore, they're prone to interference and transmission errors. To reduce errors, both types of 802.11 automatically reduce the Physical layer data rate. IEEE 802.11b has three lower data rates (5.5, 2, and 1Mbit/sec), and 802.11a has seven (48, 36, 24, 18, 12, 9, and 6Mbits/sec). Higher (and more) data rates aren't 802.11a's only advantage. It also uses a higher frequency band, 5GHz, which is both wider and less crowded than the 2.4GHz band that 802.11b shares with cordless phones, microwave ovens, and Bluetooth devices.

The wider band means that more radio channels can coexist without interference. Each radio channel corresponds to a separate network, or a switched segment on the same network. One big disadvantage is that it is not directly compatible with 802.11b, and requires new bridging products that can support both types of networks. Other clear disadvantages are that 802.11a is only available in half the bandwidth in Japan (for a maximum of four channels), and it isn't approved for use in Europe, where HiperLAN2 is the standard.

4.5 VOICE PLAYBACK CHIP

The APR33A series are powerful audio processor along with high performance audio analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The APR33A series are a fully integrated solution offering high performance and unparalleled integration with analog input, digital processing and analog output functionality. The aPR33A incorporates all the functionality required to perform demanding audio/voice applications. High quality audio/voice systems with lower bill-of-material costs can be implemented with the APR33A series because of its integrated analog data converters and full suite of quality-enhancing features such as sample-rate convertor. The APR33A series E2.1 is specially designed for simple key trigger, user can record & play the message averagely for 1, 2, 4 or 8 voice message(s) by switch and be adjusted the sample rate by using different values of resistors to meet your requirement. It is suitable in simple interface or need to limit the length of single message, e.g. toys, leave messages system, answering machine etc. Meanwhile, this mode provides the power-management system. Users can let the chip enter power-down mode when unused. It can effectively reduce electric current consuming to 15uA and increase the using time in any projects powered by batteries.

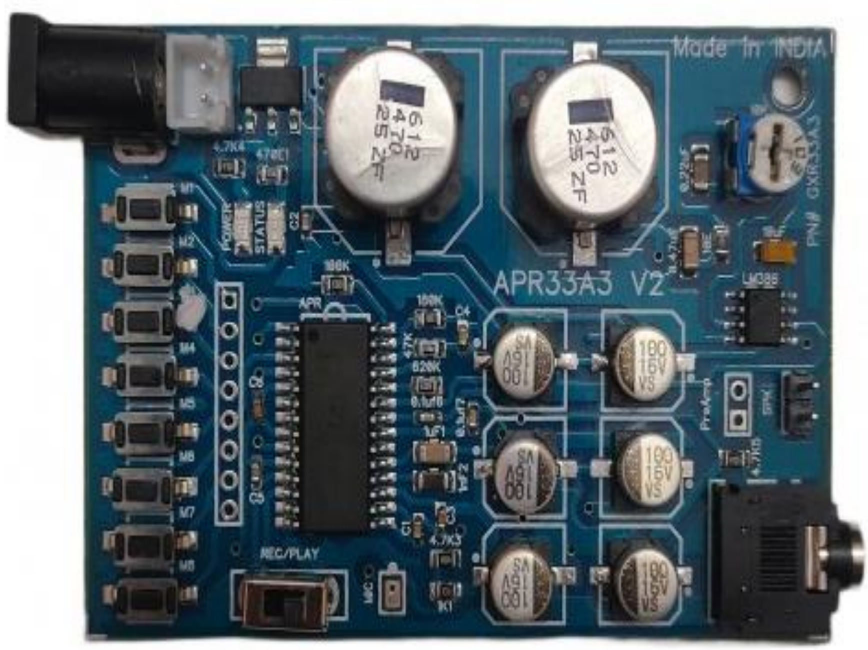

Fig.4.11 Voice Playback Chip

Features:

• Operating Voltage Range: 3V ~ 6.5V

• Single Chip, High Quality Audio/Voice Recording & Playback Solution

- User Friendly, Easy to Use Operation
- 340-680 sec duration. Voice Recording Length in APR33A3
- Powerful 16-Bits Digital Audio Processor
- Nonvolatile Flash Memory Technology
- External Reset pin
- Powerful Power Management Unit
- Built-in Audio-Recording Microphone Amplifier
- Configurable analog interface
- High Quality Analog to Digital, DAC and PWM module
- Simple And Direct User Interface
- Averagely 1,2,4 or 8 voice messages record & playback.

Symbol	Parameters	Min	Type	Max	Units
VDD	Operating Voltage	3		6.5	V
ISB	Standby Current			1	µA
IPDN	Power-Down Current		15	20	µA
IOP(IDLE)	Operating Current (Idle)		20		mA
IOP(REC)	Operating Current (Record)		35		mA
IOP(PLAY)	Operating Current (Playback)		25		mA
VIH	"H" Input Voltage	2.5			V
VIL	"L" Input Voltage			0.6	V
IVOUT	VOUT Current		185		mA

Table 4.7 Specification of Voice Playback Chip

CHAPTER - 5

SOFTWARE USED

SOFTWARE USED

In this project, we used software called **"MPLAB IDE"** which is used to feed the input to Zigbee Transmitter by writing a program in this software. Let's see about this software in detail.

5.1 MP LAB IDE

An Overview of Embedded Systems

MPLAB IDE is a Windows Operating System (OS) software program that runs on a PC to develop applications for Microchip microcontrollers. It is called an Integrated Development Environment, or IDE, because it provides a single integrated "environment" to develop code for embedded microcontrollers. Experienced embedded systems designers may want to skip ahead to <u>Components of MPLAB IDE</u>.

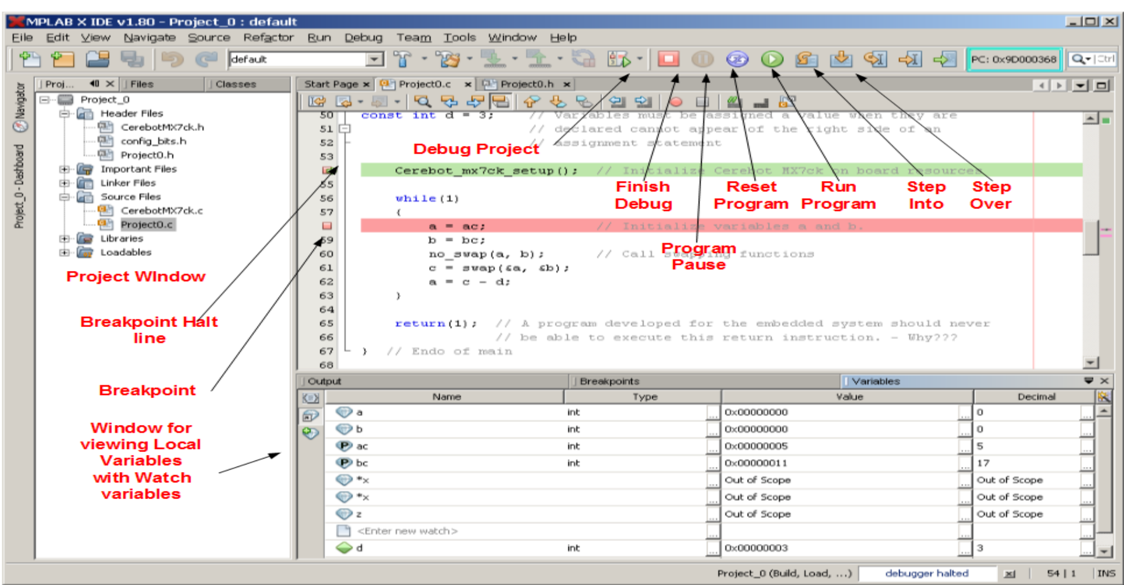

Fig.5.1 Overview of MPLAB

Implementing an Embedded System Design with MPLAB IDE

A development system for embedded controllers is a system of programs running on a desktop PC to help write, edit, debug and program code - the intelligence of embedded systems applications - into a microcontroller. MPLAB IDE runs on a PC and contains all the components needed to design and deploy embedded systems applications.

The typical tasks for developing an embedded controller application are:

1. Create the high-level design. From the features and performance desired, decide which PIC MCU or dsPIC DSC device is best suited to the application, then design the associated hardware circuitry. After determining which peripherals and pins control the hardware, write the firmware - the software that will control the hardware aspects of the embedded application. A language tool such as an assembler, which is directly translatable into machine code, or a compiler that allows a more natural language for creating programs, should be used to write and edit code. Assemblers and compilers help make the code understandable, allowing function labels to identify code routines with variables that have names associated with their use, and with constructs that help organize the code in a maintainable structure.

2. Compile, assemble and link the software using the assembler and/or compiler and linker to convert your code into "ones and zeroes" - machine code for the PIC MCUs. This machine code will eventually become the firmware (the code programmed into the microcontroller).
3. Test your code. Usually, a complex program does not work exactly the way imagined, and "bugs" need to be removed from the design to get proper

results. The debugger allows you to see the "ones and zeroes" execute, related to the source code you wrote, with the symbols and function names from your program. Debugging allows you to experiment with your code to see the value of variables at various points in the program, and to do "what if" checks, changing variable values and stepping through routines.

4. "Burn" the code into a microcontroller and verify that it executes correctly in the finished application.

Of course, each of these steps can be quite complex. The important thing is to concentrate on the details of your own design, while relying upon MPLAB IDE and its components to get through each step without continuously encountering new learning curves.

Step 1 is driven by the designer, although MPLAB IDE can help in modeling circuits and code so that crucial design decisions can be made.

MPLAB IDE really helps with steps 2 through 4. Its Programmer's Editor helps write correct code with the language tools of choice. The editor is aware of the assembler and compiler programming constructs and automatically "color-keys" the source code to help ensure it is syntactically correct. The Project Manager enables you to organize the various files used in your application: source files, processor description header files and library files. When the code is built, you can control how rigorously code will be optimized for size or speed by the compiler and where individual variables and program data will be programmed into the device. You can also specify a "memory model" in order to make the best use of the microcontroller's memory for your application. If the language tools run into errors when building the application, the offending line is shown and can be "double clicked" to go to the corresponding source file for immediate editing. After editing, press the "build" button to try again. Often this write-compile-fix loop is done many times for complex code as the sub-sections are written and tested. MPLAB IDE goes through this loop with maximum speed, allowing you to get on to the next step.

Once the code builds with no errors, it needs to be tested. MPLAB IDE has components called "debuggers" and free software simulators for all PIC MCU and PIC DSC devices to help test the code. Even if the hardware is not yet finished, you can begin testing the code with the simulator, a software program that simulates the execution of the microcontroller. The simulator can accept a simulated input (stimulus), in order to model how the firmware responds to external signals. The simulator can measure code execution time, single step through code to watch variables and peripherals, and trace the code to generate a detailed record of how the program ran.

Once the hardware is in a prototype stage, a hardware debugger, such as an in-circuit emulator or an in-circuit debugger, can be used. These debug tools run the code in real time on your actual application by using special circuitry built into many devices with Flash program memory. They can "see into" the target microcontrollers program and data memory, and stop and start program execution, allowing you to test the code with the microcontroller in place on the application.

After the application is running correctly, you can program a microcontroller with one of Microchip's device or development programmers. These programmers verify that the finished code will run as designed. MPLAB IDE supports most PIC MCUs and all PIC DSCs.

5.2 HI-TECH Software

HI-TECH Software is an Australian-based company that provides ANSI

C compilers and development tools. Founded in 1984, the company is best known for its HI-TECH C PRO compilers with whole-program compilation technology, or Omniscient Code Generation (OCG).[1] HI-TECH Software was bought by Microchip on 20 February 2009,[2] whereupon it refocused its development effort exclusively on supporting Microchip products. Microchip PIC10, PIC12, PIC14, PIC16, PIC18, PIC24, PIC32 and dsPIC

HI-TECH Software has also provided compilers for the following manufacturers and architectures, but none of them are advertised since the Microchip acquisition:

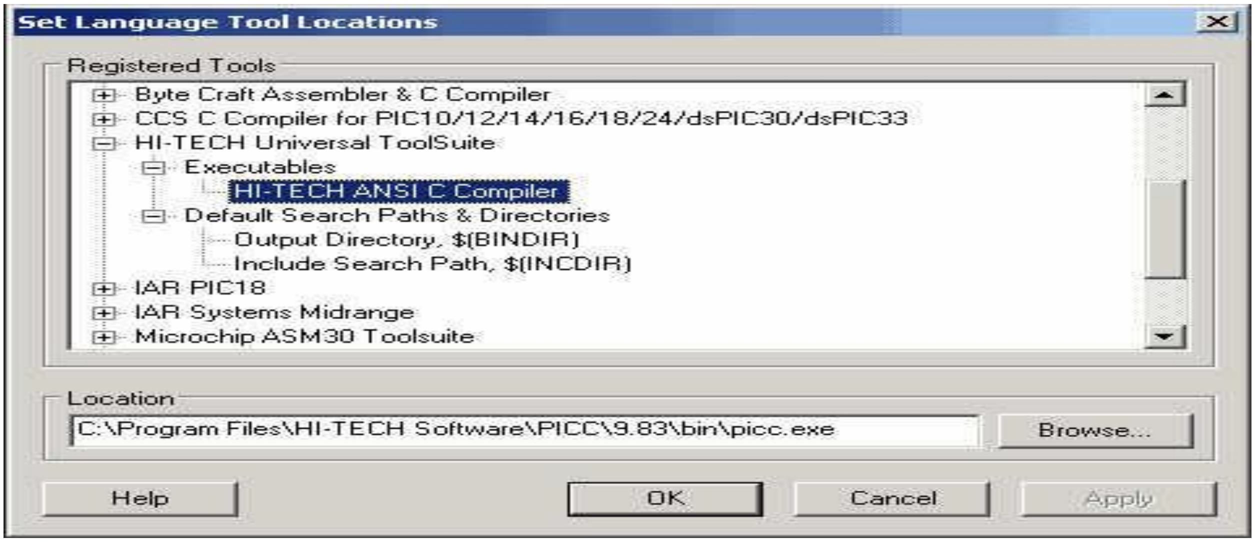

Fig5.2 HITECH Location

5.3 PIC Simulator IDE

PIC Simulator IDE is powerful application that supplies PIC developers with user-friendly graphical development environment for Windows with integrated simulator (emulator), Basic compiler, assembler, disassembler and debugger. PIC Simulator IDE currently supports the following microcontrollers from the Microchip Pismire 12F and 16F product lines: 12F629, 12F635, 12F675, 12F683, 16F627, 16F627A, 16F628, 16F628A, 16F630, 16F631, 16F636, 16F639, 16F648A, 16F676, 16F677, 16F684, 16F685, 16F687, 16F688, 16F689, 16F690, 16F72, 16F73, 16F74, 16F76, 16F77, 16F737, 16F747, 16F767, 16F777, 16F83, 16F84, 16F84A, 16F87, 16F88, 16F818, 16F819, 16F870, 16F871, 16F872, 16F873, 16F873A, 16F874, 16F874A, 16F876, 16F876A, 16F877, 16F877A, 16F882, 16F883, 16F884, 16F886, 16F887, 16F913, 16F914, 16F916, 16F917, 16F946. Additional PIC models sharing the same architecture will be supported in the new releases.

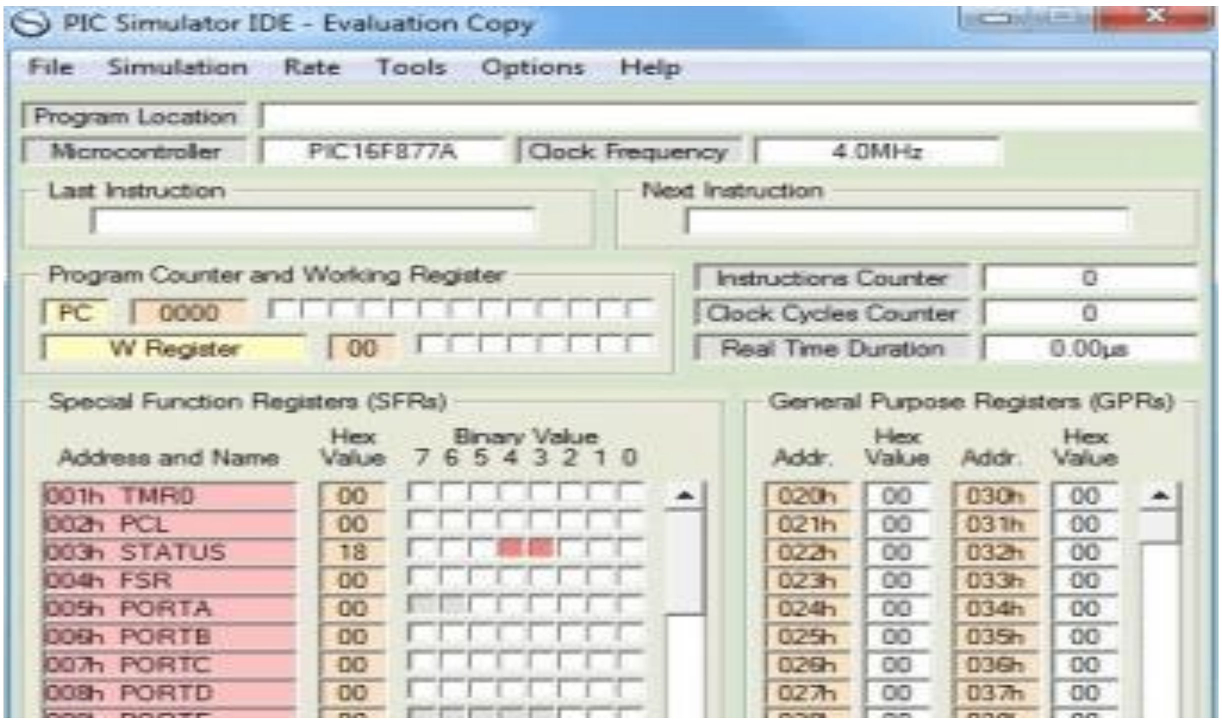

Fig5.3 PIC Simulator IDE

PIC Simulator IDE main features:

Main simulation interface showing internal microcontroller architecture, FLASH program memory editor, EEPROM data memory editor, hardware stack viewer, Microcontroller pinout interface for simulation of digital I/O and analog inputs, Breakpoints manager for code debugging with breakpoints support, PIC assembler, interactive assembler editor for beginners, PIC disassembler, Powerful PIC Basic compiler with smart Basic source editor, PIC Basic compiler features: three basic integer data types (1-bit, 1-byte, 2-byte), optional 4-

byte (32-bit) long integer data type with 32-bit arithmetic's, optional 4-byte (32-bit) single precision floating point data type with single precision math functions, arrays, all standard PIC Basic language elements, optional support for structured language (procedures and functions), high level language support for using internal EEPROM memory, using internal A/D converter module, using interrupts, serial communication using internal hardware UART, software UART implementation, I2C communication with external I2C devices, Serial Peripheral Interface (SPI) communication, interfacing character LCDs, interfacing graphical LCDs with 128x64 dot matrix, R/C servos, stepper motor control, 1-Wire devices, PC's serial port terminal for communication with real devices connected to serial port, LCD module simulation interface for character LCD modules, Graphical LCD module simulation interface for 128x64 graphical LCD modules, Stepper motor phase simulation interface for stepper motor driving visualization, Simulation module for external I2C EEPROMs from 24C family, Software UART simulation interface for software implemented UART routines, Oscilloscope (with Zoom feature) and signal generator simulation tools, Extensive program options, color themes ,There are eleven examples bundled with PIC Simulator IDE. They are located in application folder. This is short step by step guide for the beginners that will help them to test these examples and, in that way, explore the most important features of PIC Simulator IDE.

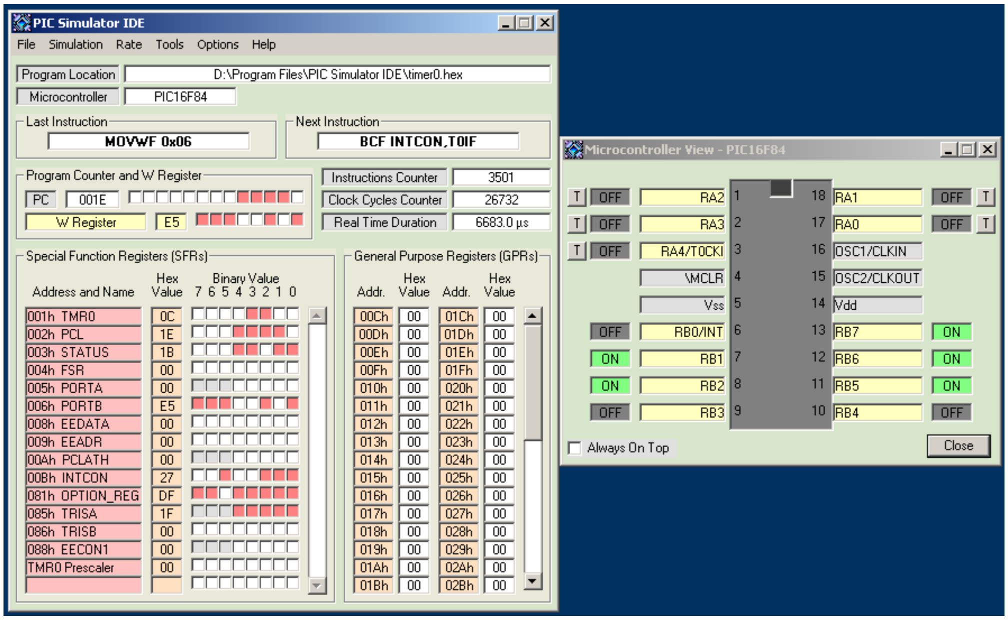

Fig5.4 PIC Microcontroller view

CHAPTER – 6

RESULTS AND DISCUSSIONS

RESULTS AND DISCUSSIONS

The beacon is calibrated so that the zigbee signal is detected by the mobile device within a proximity radius of 10m. When the signal is detected by receiver, it sends out a voice command indicating the name of the locality and also nearest location.

Two locations are programmed in transmitter.

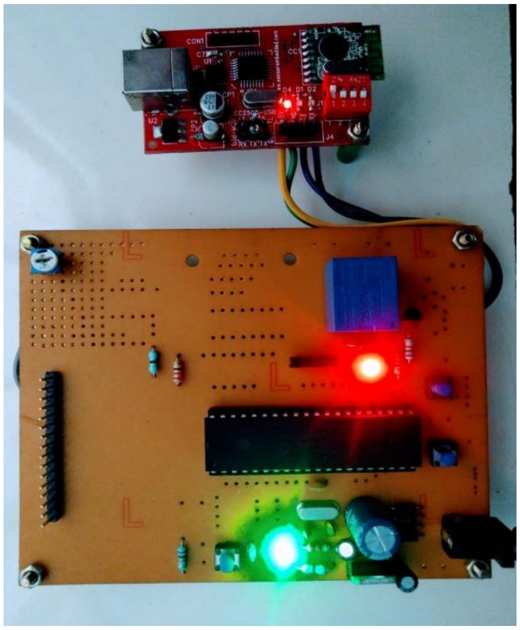

Fig.6.1 Beacon transmitter

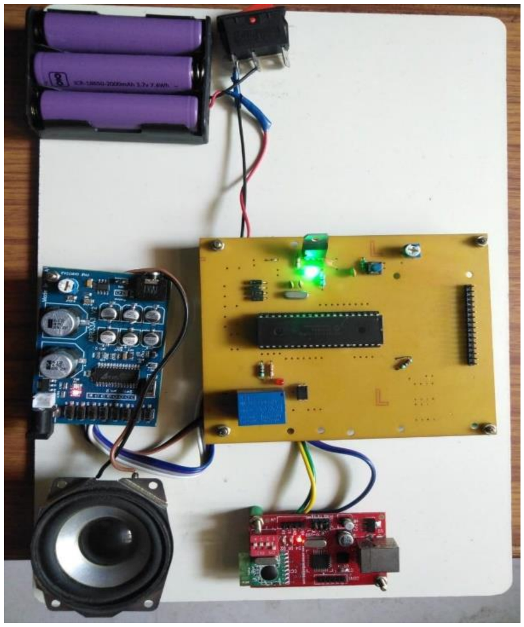

Fig6.2 Beacon receiver

CHAPTER - 7

CONCLUSION

CONCLUSION

The proposed system aims to develop a Beacon technology for Safe Movement of Disabled People. This project suggests that beacon technology can have a significant impact on the mobility and safety of disabled individuals. By providing location-based information and assistance, beacons can help individuals navigate unfamiliar environments with greater ease and confidence. Additionally, beacons can be used to trigger alerts and notifications that can provide timely assistance.

Overall, the project suggest that beacon technology offers promising opportunities for improving the safety and mobility of disabled individuals, but it should be approached as one tool among many in larger effort to promote accessibility and inclusion. Further research and development are needed to optimize the use of beacon technology for the needs of visually disabled people.

CHAPTER - 8

APPENDIX

APPENDIX

PROGRAM:

Transmitter:

```
#include<dlcd.h>
void serial_trans1(unsigned char);
unsigned char serial_recev1(void);
void serial_line_trans1(unsigned char const*);

unsigned char R,i,j;
unsigned char k0,k1,k2,k3;
void main()
{
TRISB=0x00;
TRISD=0x00;
TRISC=0X85;

lcd_init();
delay(1000);
print_line(" TRANSMITTER ",0X80);


while(1)
{
if(RC0==1)
```

```
{
while(RC0==1);
j++;
j=j%4;
}
if(RC2==1)
{
while(RC2==1);
j--;
j=j%4;
}

if(j==0)
{
print_line("MODE 1 ",0XC0);
serial_line_trans1("MODE1");
}
if(j==1)
{
print_line("MODE 2 ",0XC0);
serial_line_trans1("MODE2");
}
if(j==2)
{
print_line("MODE 3 ",0XC0);
serial_line_trans1("MODE3");
}
```

```
}
}
void serial_line_trans1(unsigned char const*line_dat)
{
        while(*line_dat)
        {
                serial_trans1(*line_dat);
                line_dat++;
                delay(200);
        }
}
```

Receiver:

```
#include<pic.h>

#include<dlcd.h>

unsigned char i,c,f,j,k1,k2,k3,k4,x;

unsigned char d[10];

void main()

            {

            TRISB=0X00;

            TRISC=0X80;

            TRISD=0X00;

            PORTB=0X00;
```

```
        RC5=0;

        lcd_init();

        delay(1000);

        print_line("Receiver",0x80);

        delay(6500);

        delay(65000);

        RD4=RD5=RD6=RD7=1;

while(1){

        CREN=1;

        //lcd_command(0xc0);

        if((d[0]=='M' && d[1]=='O' && d[2]=='D' && d[3]=='E' && d[4]=='1')

          && k1<1 )

          {

          d[0]=d[1]=d[2]=d[3]=0x00;

          k1++;

          k2=k3=k4=0;

          print_line("Mode 1",0xc0);

          RD4=0;

          i=20;

          while(i--)
```

```
{
delay(65000);
}
RD4=1;
}
if((d[0]=='M' && d[1]=='O' && d[2]=='D' && d[3]=='E' &&
d[4]=='2') && k2<1 )
{
d[0]=d[1]=d[2]=d[3]=0x00;
k2++;
k4=k3=k1=0;

print_line("Mode 2",0xc0);
RD5=0;
i=20;
while(i--)
{
delay(65000);
}
RD5=1;
```

```
}
if((d[0]=='M' && d[1]=='O' && d[2]=='D' && d[3]=='E' &&
d[4]=='3') && k3<1 )
{
d[0]=d[1]=d[2]=d[3]=0x00;
k3++;
k2=k4=k1=0;
print_line("Mode 3",0xc0);
RD6=0;
i=20;
while(i--)
{
delay(65000);
}
RD6=1;
}
if((d[0]=='M' && d[1]=='O' && d[2]=='D' && d[3]=='E' &&
d[4]=='4')&& k4<1 )
{
d[0]=d[1]=d[2]=d[3]=0x00;
```

```
            k4++;
            k2=k3=k1=0;
            print_line("Mode 4",0xc0);
            RD7=0;
                i=20;
            while(i--)
            {
            delay(65000);
            }
            RD7=1;
            }
}}
void interrupt isr(void)
        {
                if(RCIF==1)
                {
                        RCIF=0;
                        d[x]=RCREG;
                        x++;
                        x=x%5;
```

```
    //CREN=0;
        RCREG=0;
    }
}
```

CHAPTER - 9

REFERENCES

REFERENCES

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CHAPTER – 10

PERSONAL DETAILS

PERSONAL DETAILS

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