CprE 488 – Embedded Systems Design
MP-1: Quad UAV Interfacing

Group: C2
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In your writeup, describe your experiences in practicing controlling the quad.

Flying the quad showed us how sensitive the controller is to the motion of the quad. We understood what various controls in the quad controller and how they affected the quad. We understand the importance of maintaining the thrust while flying the quad to ensure the quad is in the air.

In your writeup, describe the PPM signals. What do each of the channels correspond to, and what are their minimum and maximum ranges? What is the total length of the individual PPM frames, and what is the minimum length of the idle pulse?

The PPM signal is a repeating frame that contains different channel lengths based on what changes are being made on the controller. It has an output for every channel segregated by a constant gap of 400 microseconds and an idle state for every PPM frame.

In the PPM signal frame, a fixed-length pulse indicates the start of every channel (also the end of the last channel). While transmitting/generating a signal position of the pulse is varied depending on the length of a channel. While receiving or capturing, the beginning of a channel (and the end of the last channel) is determined when a fixed-length pulse is detected.

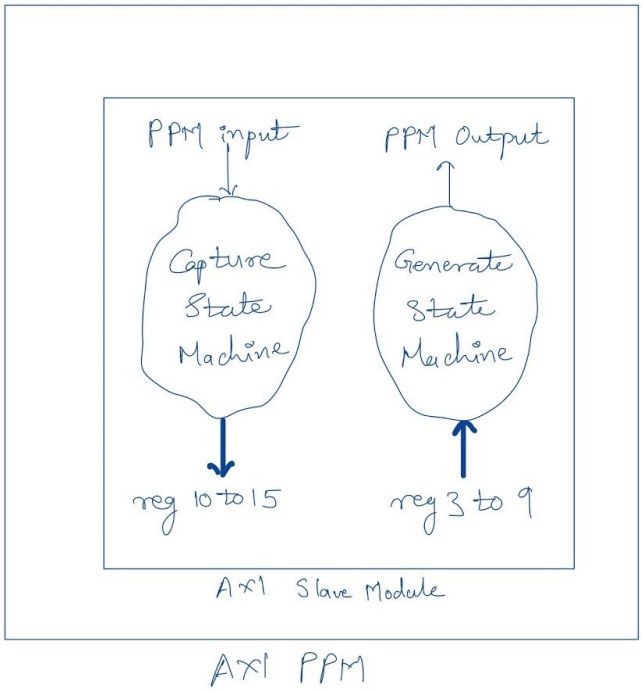
The spreadsheet below contains minimum and maximum values and which channels correspond to which controls:

Time durations (in ms)					
Period of PPM Frame	20				
Minimum length of Idle Pulse	7.837				
		Channel	Min	Max	Trim range
Left Stick	Left,Right	4	0.686	1.561	0.14
	Up-Down	3	0.604	1.588	0.16
Left dial		6	0.6	1.62	-
Left Switch		3	0.6	1.2	-
		Channel	Min	Max	Trim range
Right Stick	Left,Right	1	0.665	1.558	0.14
	Up-Down	2	0.682	1.508	0.16
Right dial		5	0.6	1.62	-
Right Switch		1	1.04	1.08	-
		2	1	1.06	-

Based on the ZedBoard documentation and your oscilloscope measurement of the trainer port, what concerns do you have about making this connection?

The controller output is sending a 5 V signal, but the Zedboard uses a max of 3.3 V signal, so we would need a voltage level shifter.

1) In your write up, provide a structural diagram of the axi_ppm design, from the top-level AMBA AXI interface down to where your user logic will reside.



2) How does an address on the AMBA bus generate a read or write enable signal for the slave registers in your design?

The writing or reading of slave registers is controlled by the slv_reg_wren signal in the axi ppm module. This signal is determined by the axi_wready, s_axi_wvalid, axi_awready and s_axi_awvalid bits. These bits are used to determine when there is valid address and data available and the slave is ready to accept these values.

3) How will your PPM state machine get access to the IP core's Memory Mapped registers?

Our state machines reside as components within the AXI_PPM slave that resides in the larger AXI_PPM module. These components are ported in VHDL to their parent components. We port the output/input ports from our state machine to the slave registers in the AXI PPM module.