SWITCHING THEORY & LOGIC DESIGN

(Common to CSE and IT)

Course Code:22EC11D1

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Course Outcomes: At the end of the course the student will be able to
CO1: discuss the significance of number systems, conversions, binary codes (L2)
CO2: apply different simplification methods for minimizing boolean functions (L3)
CO3: analyze the design concepts of various combinational circuits (L4)
CO4: analyze the concept of sequential logic design (L4)
CO5: categorize Mealy & Moore models and Simplify & Design Sequential machines (L4)

UNIT-I **10 Lectures**

Number Systems and Codes: Introduction to number systems, representation of negative numbers, binary arithmetic, binary codes, Error detecting and correcting codes.

Learning outcomes: At the end of this unit, the student will be able to

1. understand the advantages of using different number systems. (L2)
2. describe the usefulness of different binary codes. (L2)
3. summarize the error detection and correction concepts. (L2)

UNIT-II **10 Lectures**

Boolean Algebra And Switching Function

Fundamental postulates of Boolean algebra, De-Morgan theorems, switching functions, Simplification of Boolean equations, Digital logic gates, properties of XOR gates, universal gates, NAND/NOR realizations. K-map method, Prime implicants, don't care combinations, Minimal SOP and POS forms, Tabular Method, Prime –Implicant chart, simplification rules.

Learning outcomes: At the end of this unit, the student will be able to

1. apply basic laws and De Morgan's theorems to simplify Boolean expressions. (L3)
2. understand concepts of sum-of-products and product-of-sums representations. (L2)
3. describe K- Map & Tabular methods of minimizing logic functions. (L2)

UNIT-III **10 Lectures**

Combinational Logic Design

Adders, Subtractors, Multiplexer, De-Multiplexer, MUX Realization of switching functions, Encoder, Decoder, Parity bit generator, Code converters, Basic PLD's: ROM, PROM, PLA, PAL Realizations.

Learning outcomes: At the end of this unit, the student will be able to

1. apply Boolean algebra for describing combinational digital circuits (L3)
2. describe standard combinational circuits such as adders, subtractors, comparators etc. (L2)
3. analyze the digital circuit design using PLDs (L4)

UNIT-IV **10 Lectures**

Sequential Circuits

Latches, SR Flip-flops, JK Flip-flops, D Flip-flop, T-Flip-flop, Race around condition, Master-Slave Flip-flop, Shift Registers, Asynchronous and Synchronous Counters, Ring Counter, Jhonson Counter.

Learning outcomes: At the end of this unit, the student will be able to

1. understand the principle of Flip-Flops and Latches (L2)
2. summarize the concepts of Shift Registers (L2)
3. analyze the design of Counters. (L4)

UNIT-V **10 Lectures**

Finite State Machines

Analysis and Design of Synchronous Sequential Circuits: Moore and Mealy machine models, State Equations, State Table, State diagram, State reduction & assignment, Synthesis of synchronous sequential circuits- serial binary adder, sequence detector and binary counter, Partition technique for completely specified sequential machines.

Learning outcomes:At the end of this unit, the student will be able to

1. understand Moore and Mealy machine models (L2)
2. discuss the concepts of State assignment & Reduction (L2)
3. analyze the design and synthesis of synchronous sequential circuits (L4)

Text Books:

1. M. Morris Mano and Michael D. Ciletti, *Digital Design*, 4th Edition, Pearson Education, 2013.

Reference Books:

1. A. Anand Kumar, Switching Theory and Logic Design. PHI, 2014.
2. Z. Kohavi, Switching and Finite Automata Theory, Tata McGraw Hill,2009
3. Charles H Roth (Jr), Larry L. Kinney, Fundamentals of Logic Design, 5th Edition,Cengage Learning India Edition, 2010.
4. John.M Yarbrough, Digital Logic Applications and Design, Thomson Learning, 2006.