IIITB COMET FOUNDATION

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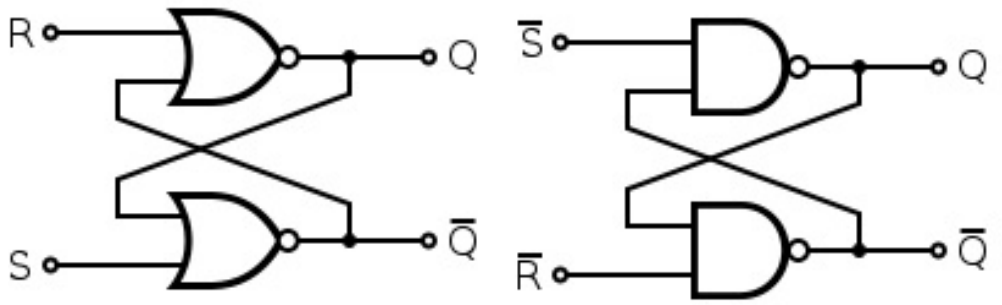
Q.38 Refer to the NAND and NOR latches shown in the figure. The inputs (P_1, P_2) for both the latches are first made (0,1) and then, after a few seconds, made (1,1). The corresponding stable outputs (Q_1, Q_2) are:



(A) NAND: first (0,1) then (0,1) NOR: first (1,0) then (0,0)

(B) NAND: first (1,0) then (1,0) NOR: first (1,0) then (1,0)

(C) NAND: first (1,0) then (1,0) NOR: first (1,0) then (0,0)

(D) NAND: first (1,0) then (1,1) NOR: first (0,1) then (0,1)

Solution:

NAND Latch (Active-Low SR Latch)

Inputs: $P_1 = S'$, $P_2 = R'$
Output: Q_1, Q_2 (complementary)

Truth Table:

S'	R'	Q_1	Q_2	Description
1	1	No change	No change	Hold state
0	1	1	0	Set
1	0	0	1	Reset
0	0	1	1	Invalid

Step 1: Input $(0, 1)$ (Set condition): $Q_1 = 1$, $Q_2 = 0$
Step 2: Input $(1, 1)$ (Hold): Output remains $Q_1 = 1$, $Q_2 = 0$

Final NAND output: $(1, 0)$

NOR Latch (Active-High SR Latch)

Inputs: $P_1 = S$, $P_2 = R$
Output: Q_1, Q_2 (complementary)

Truth Table:

S	R	Q_1	Q_2	Description
0	0	No change	No change	Hold state
1	0	1	0	Set
0	1	0	1	Reset
1	1	0	0	Invalid

Step 1: Input $(0, 1)$ (Reset): $Q_1 = 0$, $Q_2 = 1$
Step 2: Input $(1, 1)$ (Invalid): Output becomes $Q_1 = 0$, $Q_2 = 0$

Final NOR output: $(0, 0)$

Answer: **(C) NAND: first (1,0) then (1,0); NOR: first (1,0) then (0,0)**