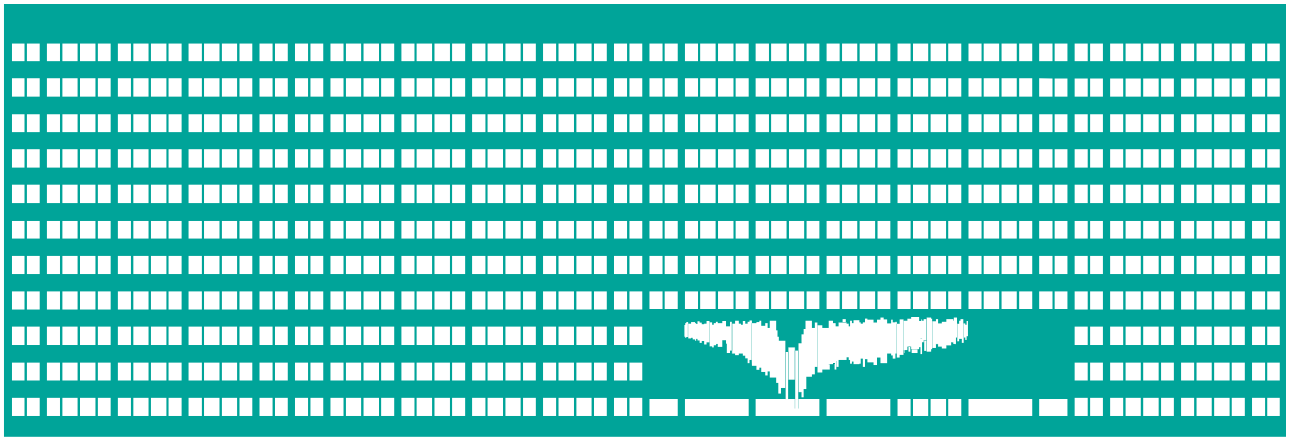
VSB TECHNICAL UNIVERSITY OF OSTRAVA | FACULTY OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE | DEPARTMENT OF COMPUTER SCIENCE

Power management on mobile devices



MS (Mobile Computing)
Lecture 11

Mobile devices & power consumption

- Portable systems, such as laptop computers, smartphones and PDAs draw power from batteries → reducing power consumption extends their operating times. Problems:
  - Limited capacity of battery
  - Ever increasing requirements for *AOAC* (*Always On Always Connected*) computing.
  - Multimedia playback, faster CPUs in mobile devices, power-consuming applications such as games, full-featured browser (including Adobe Flash support), …

Rechargeable power sources

The power source for a wireless device should have good capacity, low weight, may have to supply wide ranges of currents (the power must be sufficient) and survive many charging cycles without adverse effects.

- Some devices have a built-in battery: may not be replaced

Type	Energy density (Wh/kg)	Power (W/ kg)	Charg. Eff. (%)	Discharge (%/month)	Cycles (#)	Lifetime (years)
Alkaline	85	50	99.9%	<0.3	100-1000	<5
NiCd	40-60	150	70%-90%	20,00%	1500	
NiMH	30-80	250-1000	66,00%	30,00%	500-1000	
Li-Ion	150-250	1800	80-90%	5%-10%	1200	2-3
Li polymer	130-200	3000			500-1000	2-3
LiFePO4	80-120	1400			2000	

Power management – why?

- PM is desired for many reasons, especially to:
  - *Prolong battery life on portable & embedded systems*
  - *Reduce cooling requirements*
  - *Reduce overall energy consumption*
  - Reduce noise
  - Reduce operating costs for energy and cooling
- Lower power consumption → lower heat dissipation → increase in system stability & lower energy consumption → "greener" & cheaper in long-term use.

CPU-based PM mechanisms

- Well known from desktop/laptop computers – the techniques evolved over the time:
  - Issuing halt instruction when CPU is idle
  - CPU throttling
    - Halting the CPU core XY% of time
    - Dynamic frequency scaling
  - Voltage scaling (lower voltage → lower heat)
  - Deep sleep states in APM (suspend-to-RAM, hibernation, combined approach, ...)
  - Selective power-off of unused circuity
  - Thinner die size (lower channel resistance)
  - Turning off whole cores of multi-core CPU

Dynamic voltage & frequency scaling

- Dynamic power consumption in a chip is given by the equation: $\mathbf{P_d = k * C * V^2 * f}$, where P_d is dynamic power (2/3 of chip power in current chips), k is the number of changes, C is the capacitance being switched per clock cycle, V is voltage, and *f* is the processor frequency (cycles per second).
- Lower frequency → less power, lower voltage → power reduction is squared
- DFS – changing basic frequency (clock rate may be not feasible) → changes in clock multiplier instead.
- Balancing between power & battery life (OS governor)

Current chip PM techniques

- Dynamic
  - Clock gating – turns off clock signal for parts of circuity: no dynamic changes, only leakage current. Design must include conditions when CG occurs
  - Power gating – turns off V_{DD} for a circuit block. Takes longer time to enter & leave than CG.
  - Data gating
  - DVS & DFS, Variable device threshold
- Structural
  - Voltage islands – parts of chip have different voltages
  - Multi-oxide devices, Multi-threshold devices (for PG)
  - Capacitance reduction, …

Power reduction in HW design

- Integration techniques:
  - System in package (SiP) – all main parts of a electric system are packaged together, usually stacked vertically
  - System-on-a-chip (SoC) – all components of a computer or other electronic system are integrated into a single integrated circuit (on a single die)
  - Package-on-package (PoP) – integrated circuit packaging technique allowing to vertically combine discrete logic and memory ball grid array packages.

Dynamic power management

Set of policies defining how to compromise between computational power and battery life by defining state transitions.

- Basic states: ON ↔ IDLE ↔ STANDBY ↔ ON
- DFS Types:
  - Timeout DFS – changes state after pre-defined inactivity
    - too short – performance degradation × too long – wasting pwr
    - Energy break-even time – calculates transitions based on state powers, energy & time required to exit & return to state
  - Predictive DFS – predicts future activities (no waiting) based on current information & attenuation factor
  - Stochastic DFS – Markov models (chains), non-deterministic, may make consecutive mistakes, may be computationally expensive

System component power consumption

Studies in 1990s identified main power-intensive system components:

1. Display → turning off backlight & then display in inactive periods, LED backlight, OLED displays, dynamic luminance scaling, backlight autoregulation, …
2. CPU & memory → reducing voltage, already discussed improvements.
3. Hard drive → turning off during inactive periods, replacement by flash (typically NAND) memory in PDAs, smartphones, tablets, …
4. Network/Wireless communication → lower-power chips, power-saving modes, bandwidth scaling, turn off radio during inactive periods, selecting best base station, …

OS directed PM in ACPI

ACPI defines power, processor and power states

- Power states: G0 (S0) – working, G1 – sleep mode:
  - S1 – CPU caches flushed, execution suspended, CPU, memory and must-stay-on devices powered
  - S2 – CPU powered down
  - S3 – sleep/suspend to RAM mode – RAM powered and refreshed, some devices may wake the computer
  - S4 – hibernation/suspend to disk – identical to S5, but RAM contents are stored to non-volatile ram (e.g. HD)

  G2 (S5) – soft off (Wake-on-LAN, modem, …), G3 – mechanical off (only RTC is running)
- Processor states: C0 – running, C1 – halt no execution, C2 – CPU clock stopped, C3 – CPU cache is not kept, keeps internal state intact, …

Suspend vs. stand-by mode

Sleep modes implemented by most modern devices

- *Stand-by* mode – CPU power is reduced (throttling, DFVS, …), HDD and display are turned off, the rest of the device is operational, but at lowest possible rate. Device is almost immediately operational upon resumption when turned back on.
- *Suspend* mode (suspend-to-RAM)– coresponds to S3 mode in ACPI – operation suspended, CPU powered down and its state copied to RAM, most devices powered down. Slower wake-up.

Examples of system-level PM techniques

- Freescale XEC
- ARM intelligent energy manager – OS events & IEM policies
- National semiconductors – Power Wise™ technology
- (Enhanced) Intel SpeedStep™ - P states, DFVS, …
- AMD PowerNOW (or Cool'n'Quiet)
- Transmeta LongRun & LongRun2
- Mobile industry processor interface
- …

Application-level PM

- Suboptimal algorithms may cost much power → reducing power consumption by optimization (studies suggest, that the power can be often reduced to ¼)
- On-demand connectivity, optimization of connectivity time, turning off wireless circuity when off-line
- Offloading computation-intensive tasks to specialized chip/GPU/processor (e.g. MP3, video decompression).
- Power-aware APIs that can be used by the application programmer when deploying the application:
  - Active Mode Power Management (AM/PM)

AM/PM examples

- E-mail client – off-line when not downloading E-mail, turning off the wireless HW
  - Fine-tuning the message download interval
- Web browser – during reading the page, when no objects are requested, the wireless HW is turned off
  - Problems with current technologies – AJAX, active content (HTML5, Flash, …)
- Audio playback, recording – dim/turn off backlight, full backlight on input event.
- …