

NAME: BINEY KWAKU EGYIR

INDEX NUMBER: 9312617

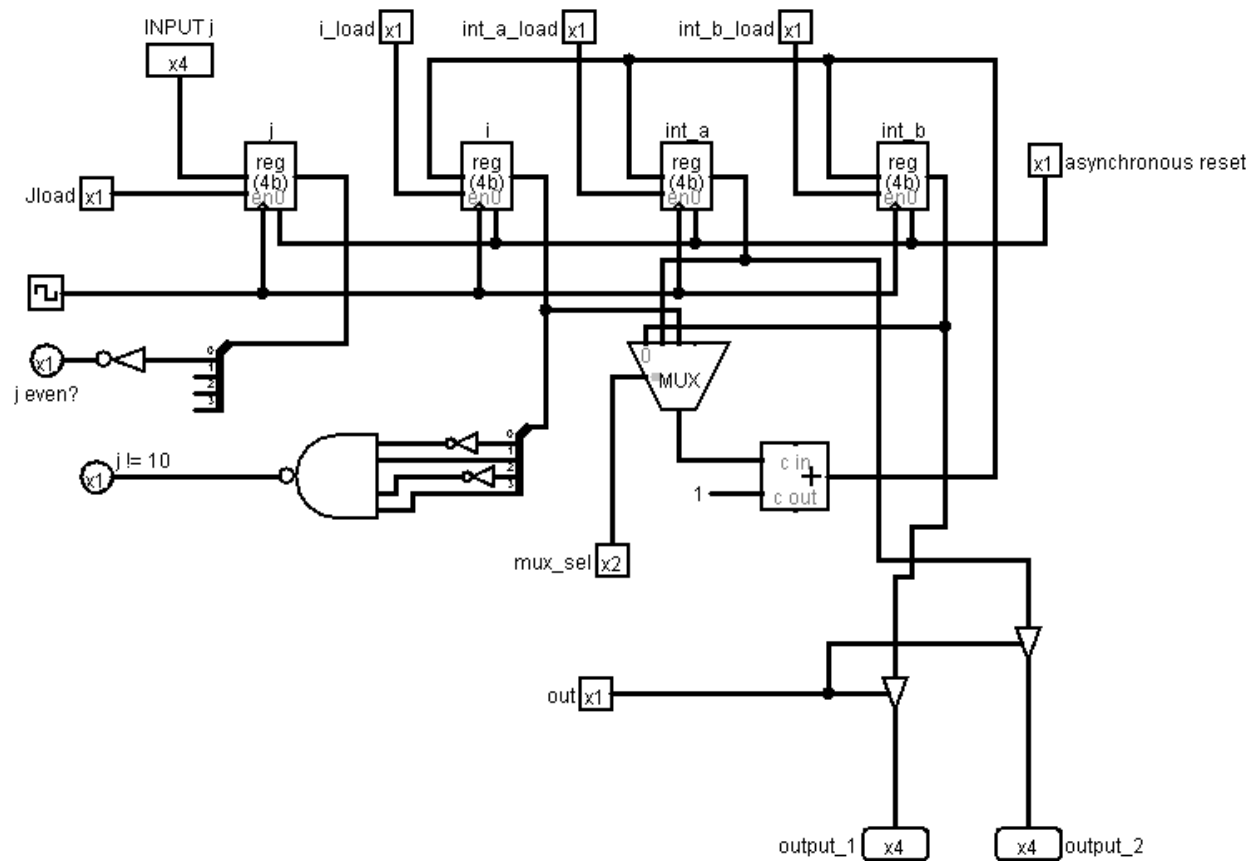
ELECTRICAL ENGINEERING: YEAR 3

ASSIGNMENT 2

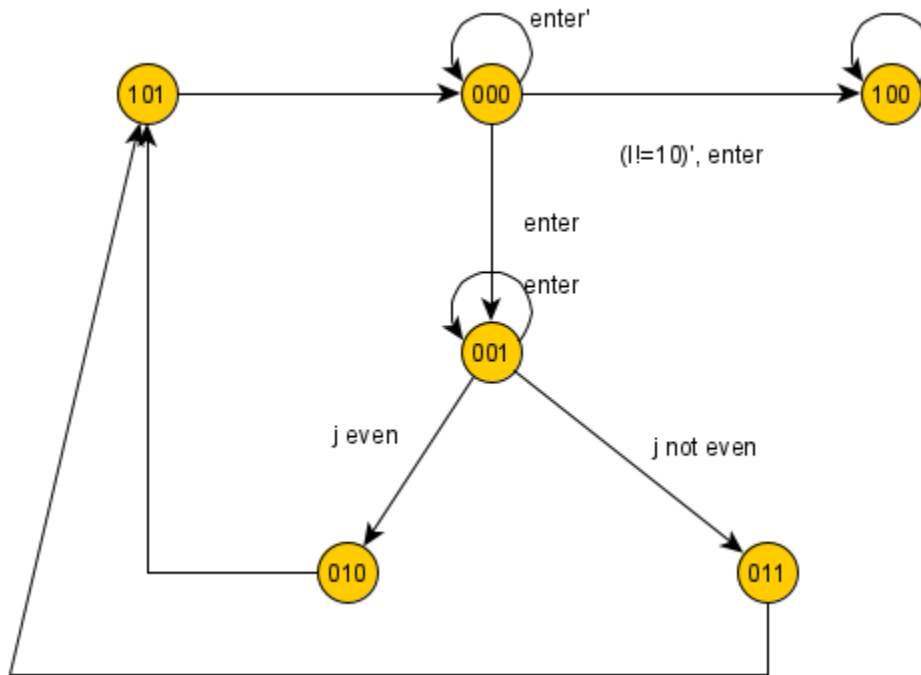
ALGORITHM

```
main()
{ int j; int in_a = 0;
  int in_b = 0;
  for (a = 0, a != 10, a++)
  { scanf("Enter value: %d", &j );
    if (j % 2 == 0) in_a++;
    else in_b++; }
  printf("You entered %d even numbers", in_a);
  printf("You entered %d odd numbers", in_b);
}
```

DATAPATH



STATE DIAGRAM



OUTPUT TABLE

Q ₂ Q ₁ Q ₀	instruction	jload	iload	IntA_load	IntB_load	Mux_sel (10)	OUT
000	input J	1	0	0	0	XX	0
001	WAIT	0	0	0	0	XX	0
010	Int_a ++	0	0	1	0	01	0
011	Int_b ++	0	0	0	1	00	0
100	output	0	0	0	0	XX	1
101	l++	0	1	0	0	10	0

NEXT STATE TABLE

Current state $Q_3Q_2Q_1$	Next state (Implementation) $Q_{2next}Q_{1next}Q_{0next} (D_3D_2D_1)$							
	Enter , $l \neq 10, j \text{ even}$							
	000	001	010	011	100	101	110	111
000	000	000	000	000	100	100	001	001
001	011	010	011	010	001	001	001	001
010	101	101	101	101	101	101	101	101
011	101	101	101	101	101	101	101	101
100	100	100	100	100	100	100	100	100
101	000	000	000	000	000	000	000	000

Using Quinn McCluskey, the following expressions were derived from the next state table,

$$D_3 = Q_3'Q_2 + Q_3Q_2'Q_1' + Q_3'Q_1'(\text{enter})(l \neq 10)'$$

$$D_2 = Q_3'Q_2'Q_1(\text{enter}')$$

$$D_1 = Q_3'(\text{enter})(l \neq 10) + Q_3'Q_1j_{\text{even}}' + Q_3'Q_1\text{enter} + Q_3'Q_2$$

Using the Karnaugh Map method, the following expressions were derived from the output table,

$$J_{\text{load}} = Q_3'Q_2'Q_1'$$

$$I_{\text{load}} = Q_3Q_2'Q_1$$

$$\text{Mux_sel}_{(1)} = Q_2'$$

$$\text{Mux_sel}_{(0)} = Q_1'Q_3'$$

$$\text{Int_a_load} = Q_3'Q_2Q_1'$$

$$\text{Int_b_load} = Q_3'Q_2Q_1$$

$$\text{Out} = Q_3Q_2'Q_1'$$

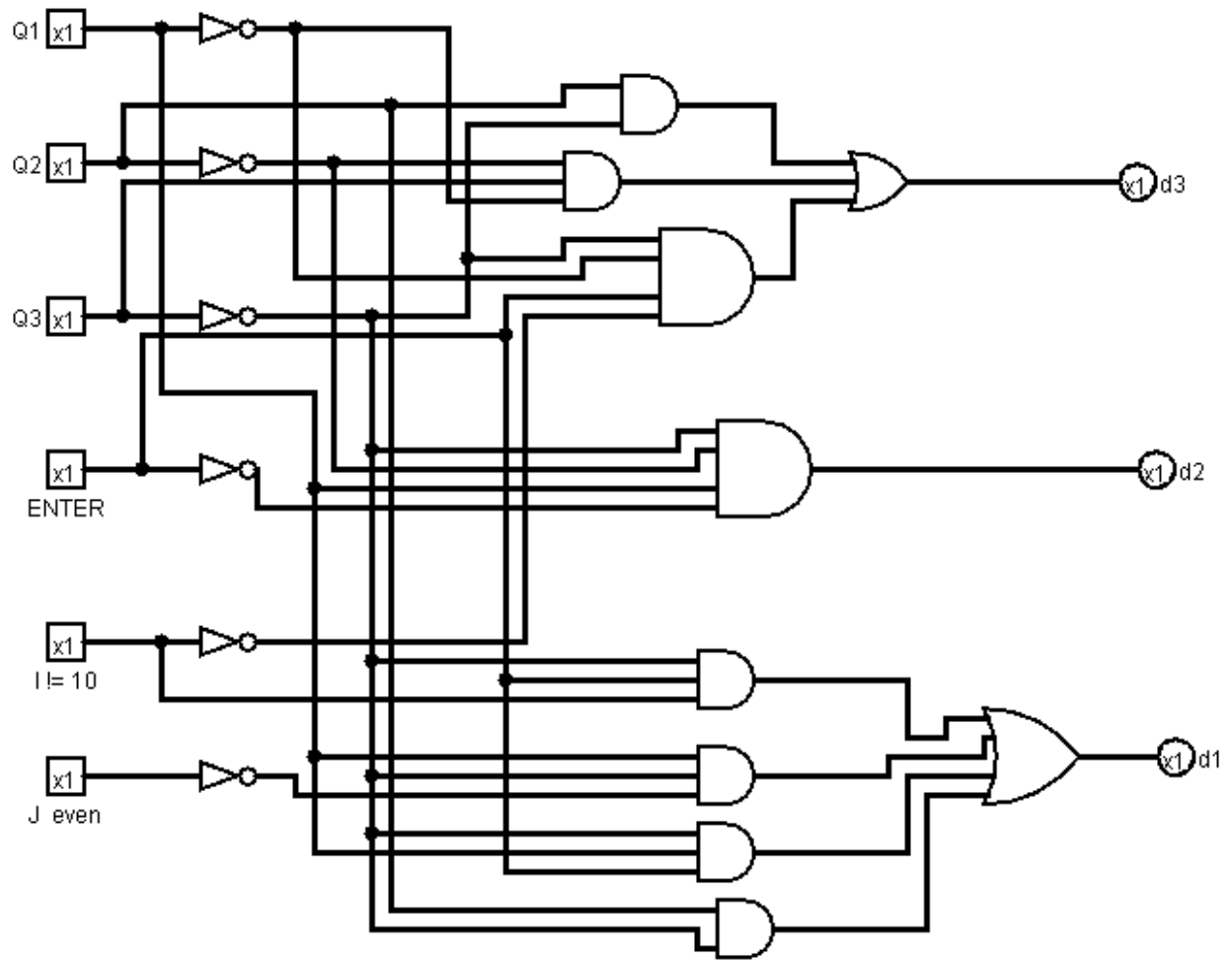


Figure 1, next state logic

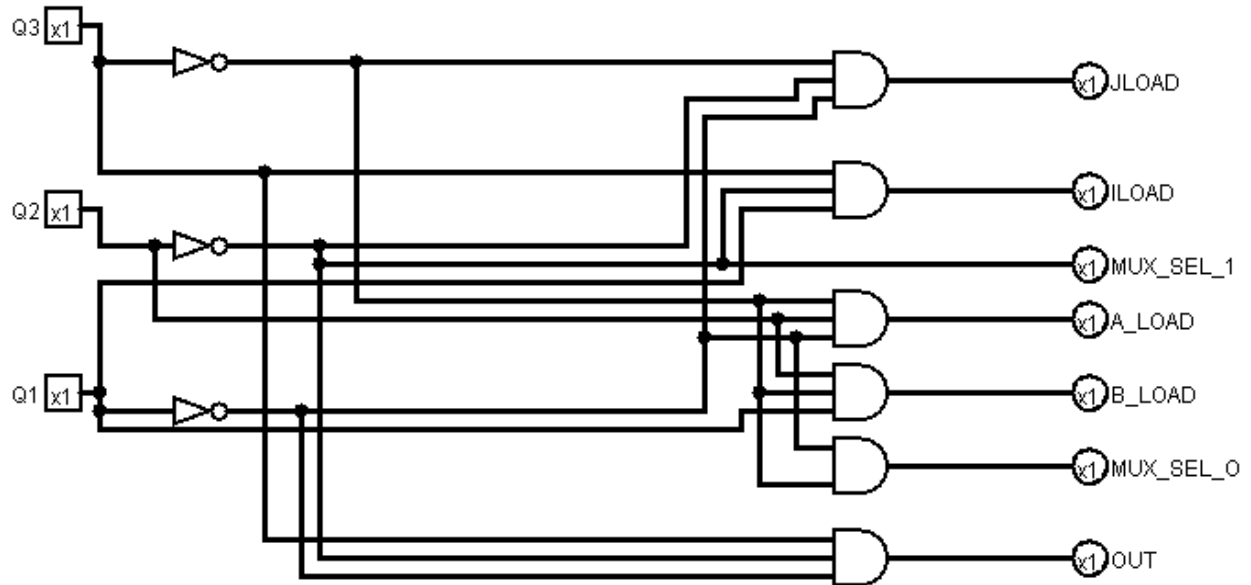


Figure 2(output logic)

ASSIGNMENT 2

- 1) Choose suitable frequency (64Hz)
- 2) Restart the system, input your numbers using the InputJ input when the wait LED is on
- 3) Hit enter after every number has been entered, and an extra enter after the tenth input
- 4) Output will be displayed afterwards

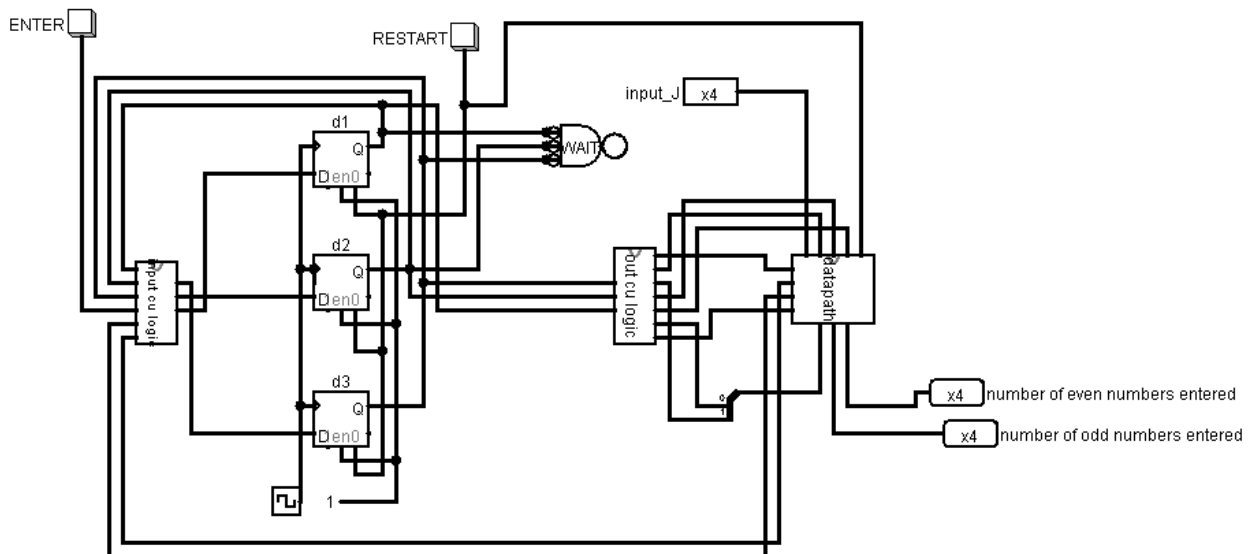


Figure 3(Abstraced circuits to form final circuit)