# STA-FX Datasheet 128-Channel CMOS Analog Switch IC

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#### **GENERAL DESCRIPTION**

The STA IC is a monolithic CMOS device containing 64 independently selectable switches. These switches are fabricated with an advanced submicron CMOS process that provides low power dissipation, low on resistance, low leakage currents, and high signal bandwidth. The STA IC is designed to operate in 3.3V for digital circuits and 5V for analog switches. Each switch can operate with a wide input and output voltage range. The off-leakage current is only 30nA at room temperature of 25°C.

All digital inputs have 0.8-V to 2.4-V input noise margin to ensure TTL/CMOS-logic compatibility when using a 3.3-V power supply.

#### **FEATURE**

3.3V logic-compatible input ( $V_{IH}$ =2.4V,  $V_{IL}$ =0.8V) Dual supply operation: 3.3V for digital, 5V for analog. Analog signal frequency: DC-to-1MHz Low on-resistance: 1 $\Omega$  (@typ) Wide range analog input from 0V to 5V Chip-ID programmable with OTP memory Multi-channel switch control Switching control using CMOS IF command 360-pin FBGA package

#### **APPLICATIONS**

Data-acquisition systems Mechanical reed-relay replacement Communication systems

#### **FUNCTIONAL DIAGRAM**

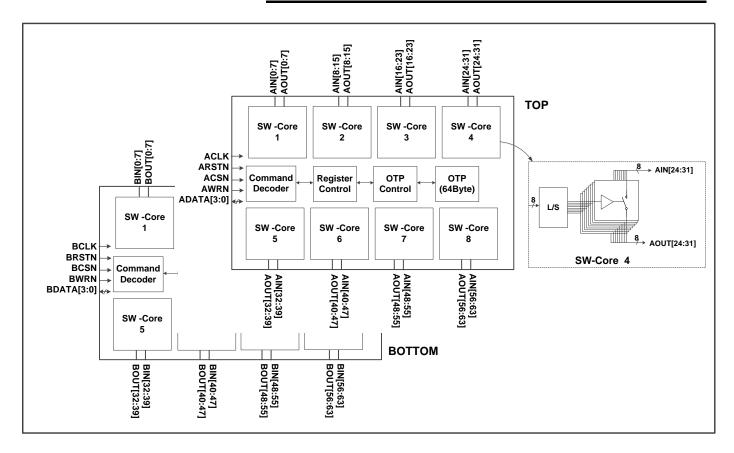


Figure 1. Functional Diagram



# ABSOLUTE MAXIMUM RATINGS\_\_\_\_\_

#### (All Voltages Referenced to GND, Unless Otherwise Noted.)

AVDD (for Analog Switch)	0.3V to +6V
DVDD (for Digital Control)	0.3V to +4.5V
Voltage at any digital pin	0.3V to +4.5V
Voltage at any analog pin	0.3V to +6V
Continuous current into any terminal	50mA
Peak current into analog switch I/O	100mA
(current pulse with 1ms and 10% duty of	cycle)

Operating temperature range	40°C to +85°C
Storage temperature range	65°C to +125°C
Junction temperature	+150°C
ESD protection on all pins (HBM, MI	M)≥2kV, 200V

Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at those or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS\_\_\_\_\_

AAVDD=5.0V, AAVSS=0V, ADVDD=3.3V, ADVSS=0V, and TA = +25°C, unless otherwise noted. BAVDD=5.0V, BAVSS=0V, BDVDD=3.3V, BDVSS=0V, and TA = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION		UNIT			
PARAMETER	STWIBOL	CONDITION	MIN	TYP	MAX	JINIT	
POWER SUPPLIES							
Angle of Cumply Velters	AAVDD		4.5	5	5.5	V	
Analog Supply Voltage	BAVDD		4.5	5	5.5	V	
Digital Complex Valtage	ADVDD		3.0	3.3	3.6	V	
Digital Supply Voltage	BDVDD		3.0	3.3	3.6	V	
Analog Cround Voltage	AAVSS		-	0	-	V	
Analog Ground Voltage	BAVSS		-	0	-	V	
Digital Cround Voltage	ADVSS		-	0	-	V	
Digital Ground Voltage	BDVSS		-	0	-	V	

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# **ELECTRICAL CHARACTERISTICS (Continued)**

AAVDD=5.0V, AAVSS=0V, ADVDD=3.3V, ADVSS=0V, and TA = +25°C, unless otherwise noted. BAVDD=5.0V, BAVSS=0V, BDVDD=3.3V, BDVSS=0V, and TA = +25°C, unless otherwise noted.

PARAMETER		CVMDOL	CONDITION		VALU	VALUE	
		SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
ANALOG S	WITCH			•			
Top	Input Range	V <sub>AIN</sub>		0		AAVDD	V
Signal Range	Output Range	V <sub>AOUT</sub>		0		AAVDD	V
Bottom	Input Range	V <sub>BIN</sub>		0		BAVDD	V
Signal Range	Output Range	V <sub>BOUT</sub>		0		BAVDD	V
Top Channe	el On Current	I <sub>ACH_ON</sub>	AAVDD=5V, V <sub>AIN</sub> =0V or 5V			50	mA
Bottom Channel On Current		I <sub>BCH_ON</sub>	BAVDD=5V, V <sub>BIN</sub> =0V or 5V			50	mA
Top Switch On-resistance		R <sub>AON</sub>	V <sub>AIN</sub> =0V to AAVDD , I <sub>ACH_ON</sub> =-1mA		1	3	Ω
Bottom Swit	ch On-resistance	R <sub>BON</sub>	V <sub>BIN</sub> =0V to BAVDD , I <sub>BCH_ON</sub> =-1mA		1	3	Ω
_	Source Off Leakage Current	I <sub>AS_OFF</sub>	AAVDD=5V, V <sub>AIN</sub> =5, V <sub>AOUT</sub> =0V		0.05	1	uA
Top Leakage Current	Drain Off Leakage Current	I <sub>AD_OFF</sub>	AAVDD=5V, V <sub>AIN</sub> =0V, V <sub>AOUT</sub> =5V		0.05	1	uA
	Channel On Leakage Current	I <sub>ACH_OFF</sub>	AAVDD=5V, V <sub>AIN</sub> =0V or 5V		0.05	1	uA
Dettern	Source Off Leakage Current	I <sub>BS_OFF</sub>	BAVDD=5V, V <sub>BIN</sub> =5, V <sub>BOUT</sub> =0V		0.05	1	uA
Bottom Leakage Current	Drain Off Leakage Current	I <sub>BD_OFF</sub>	BAVDD=5V, V <sub>BIN</sub> =0V, V <sub>BOUT</sub> =5V		0.05	1	uA
	Channel On Leakage Current	I <sub>BCH_OFF</sub>	BAVDD=5V, V <sub>BIN</sub> =0V or 5V		0.05	1	uA

# **ELECTRICAL CHARACTERISTICS (Continued)**

AAVDD=5.0V, AAVSS=0V, ADVDD=3.3V, ADVSS=0V, and TA = +25°C, unless otherwise noted. BAVDD=5.0V, BAVSS=0V, BDVDD=3.3V, BDVSS=0V, and TA = +25°C, unless otherwise noted.

DADA	METER	SYMBOL	CONDITION		UNIT		
FANA	IMIETEK	STINDOL GONDITION		MIN	TYP	MAX	UNIT
DIGITAL I/O						,	
Top Logic Input	Input High	V <sub>AIH</sub>		0.7* ADVDD			V
Voltage	Input Low	V <sub>AIL</sub>				0.3* ADVDD	V
Bottom Logic Input	Input High	V <sub>BIH</sub>		0.7* BDVDD			V
Voltage	Input Low	V <sub>BIL</sub>				0.3* BDVDD	V
Top Logic Input	Input High	I <sub>AIH</sub>		-1		1	uA
Current	Input Low	I <sub>AIL</sub>		-1		1	uA
Bottom Logic Input	Input High	I <sub>BIH</sub>		-1		1	uA
Current	Input Low	I <sub>BIL</sub>		-1		1	uA
SWITCH DYN	AMIC CHARACT	ERISTICS					
Switching	Turn ON Time	t <sub>ON</sub>	Clock base (calculate for special condition)		175		ns
Time	Turn OFF Time	t <sub>OFF</sub>			235		ns
	Input Off- Capacitance	C <sub>AIN_OFF</sub>			150		pF
Top Capacitance	Output Off- Capacitance	C <sub>AOUT_OFF</sub>			150		pF
	Output On- Capacitance	C <sub>AOUT_ON</sub>			300		pF
	Input Off- Capacitance	C <sub>BIN_OFF</sub>			150		pF
Bottom Capacitance	Output Off- Capacitance	C <sub>BOUT_OFF</sub>			150		pF
	Output On- Capacitance	C <sub>BOUT_ON</sub>			300		pF
Off-Isolation			No Load, f <sub>SW</sub> =1MHz	-16			dB
Channel-to-Ch	annel Crosstalk		No Load, f <sub>SW</sub> =1MHz	-41			dB



# ELECTRICAL CHARACTERISTICS (Continued)\_\_\_\_\_

AAVDD=5.0V, AAVSS=0V, ADVDD=3.3V, ADVSS=0V, and TA = +25°C, unless otherwise noted. BAVDD=5.0V, BAVSS=0V, BDVDD=3.3V, BDVSS=0V, and TA = +25°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION			UNIT	
FANA	PARAMETER		STWIBOL CONDITION		TYP	MAX	UNIT
POWER CONS	SUMPTION						
Тор	Static	I <sub>AAVDD_ST</sub>	AAVDD=5V			1	uA
Analog Operating Current (AAVDD)	Dynamic	I <sub>AAVDD_DYN</sub>	AAVDD=5V, f <sub>SW</sub> =1.25MHz (Note1), All switch On/Off operating simultaneously			50	mA
Bottom	Static	I <sub>BAVDD_ST</sub>	BAVDD=5V			1	uA
Analog Operating Current (AAVDD)	Dynamic	I <sub>BAVDD_DYN</sub>	BAVDD=5V, f <sub>SW</sub> =1.25MHz (Note1), All switch On/Off operating simultaneously			50	mA
Тор	Static	I <sub>ADVDD_ST</sub>	ADVDD=3.3V			1	uA
Digital Operating Current (ADVDD)	Dynamic	I <sub>ADVDD_DYN</sub>	ADVDD=3.3V, f <sub>CLK</sub> =10MHz (Note1), Combined operation of Reset, Group-On and DUT- Reject			400	uA
Bottom	Static	I <sub>BDVDD_ST</sub>	BADVDD=3.3V			1	uA
Digital Operating Current (ADVDD)	Dynamic	I <sub>BDVDD_DYN</sub>	BADVDD=3.3V, f <sub>CLK</sub> =10MHz (Note1), Combined operation of Reset, Group-On and DUT- Reject			400	uA

**Note1**: The  $f_{CLK}$  is the frequency of digital signal CLK. When the  $f_{CLK}$  is 10MHz, the maximum switching frequency ( $f_{SW}$ ) is 1.25MHZ (1-clock command).

**Note2**: The maximum of total analog operating current is 100 mA calculated by adding together Top and Bottom. The maximum of total digital operating current is 800 uA calculated by adding together Top and Bottom.

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## TIMING CHARACTERISTICS\_

AAVDD=5.0V, AAVSS=0V, ADVDD=3.3V, ADVSS=0V, and TA = +25°C, unless otherwise noted. BAVDD=5.0V, BAVSS=0V, BDVDD=3.3V, BDVSS=0V, and TA = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT	
PARAMETER	STWIBOL	CONDITION	MIN	TYP	MAX	0.111	
DIGITAL I/O SIGNALS							
CLK Period	tperiod				20	ns	
DATA to CLK Setup Time	t <sub>DS</sub>		10			ns	
DATA to CLK Hold Time	t <sub>DH</sub>		5			ns	
CSN to CLK Setup Time	tcs		10			ns	
CSN to CLK Hold Time	tch		5			ns	
WRN to CLK Setup Time	t <sub>WS</sub>		10			ns	
WRN to CLK Hold Time	t <sub>WH</sub>		5			ns	
POWER AND RESET SEQUENC	E						
Power-up Period	t <sub>PU</sub>		500			us	
Power-down Period	t <sub>PD</sub>		500			us	
Power-on Reset Time	t <sub>RST</sub>		2			us	
Chip-ID Read Routine Time	t <sub>IDRD</sub>		2			us	
SWITCH ON/OFF TIMING DIAGE	RAM						
Switch Control Enable Time	tswen		1			us	
1-Clock Command Control Time	tsw1				3	cycle	
2-Clock Command Control Time	t SW2				6	cycle	

Note3: The AC parameters of 'DIGITAL I/O SIGNALS', 'POWER AND RESET SEQUENCE' and 'SWITCH ON/OFF TIMING DIAGRAM' of Top and Bottom are the same each other.

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#### Timing Diagram of Digital I/O Signals

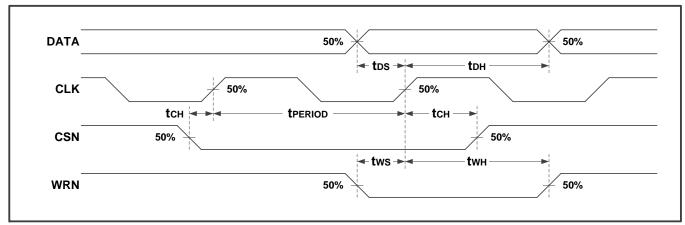


Figure 2. Timing Diagram of Digital Signals

#### Power and Reset sequence

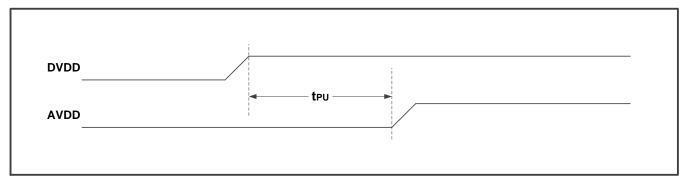


Figure 3. Power-up Sequence

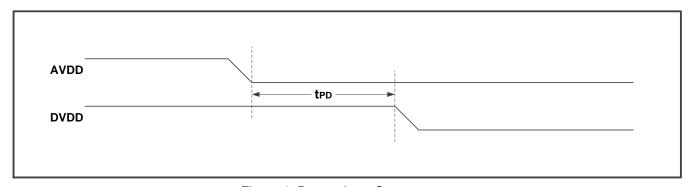


Figure 4. Power-down Sequence

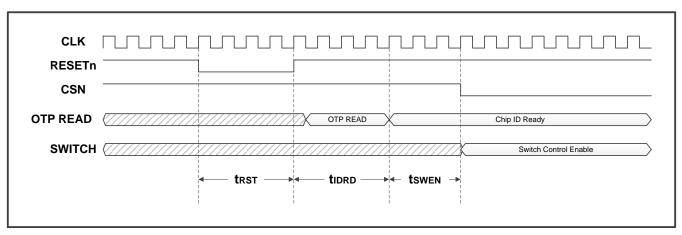


Figure 5. Reset and Stand-by Sequence

#### Switch On/Off Timing Diagram

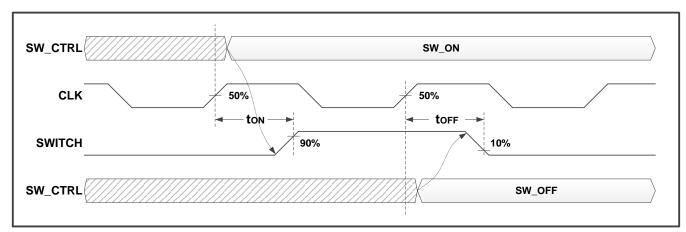


Figure 6. Switch On/Off Timing Diagram

# PIN MAPPING TABLE\_\_\_\_\_

AC	AB	B	4	W	<	_	-	70	70	z	=	_	_	ے	I	G	П	ш	0	C		A	
AAVSS	AOUT[15]	AOUT[14]	АОП[13]	AOUT[12]	AOUT[11]	AOUT[10]	AOUT[9]	AOUT[8]	AAVSS	ΑΟυΤ[7]	AOUT[6]	AOUT[5]	AOUT[4]	АОП[3]	AOUT[2]	ΑΟυΤ[1]	AOUT[0]	AAVSS	ADATA[3]	ADATA[1	ADVSS	ACLK	_
AAVDD	] AIN[15]	] AIN[14]	] AIN[13]	] AIN[12]	] AIN[11]	] AIN[10]	AIN[9]	AIN[8]	AAVDD	AIN[7]	AIN[6]	AIN[5]	AIN[4]	AIN[3]	AIN[2]	AIN[1]	AIN[0]	AAVDD	] ADATA[2]	ADATA[1] ADATA[0]	ADVDD	ADVSS	2
BAVSS	воипиз	воип[14]	воипиз	воип[12]	воипп	воит[10]	воитр	воит[8]	BAVSS	воитгл	воит[6]	BOUT[5]	воит[4]	воит[з]	воит[2]	воити	воит[0]	BAVSS	ADVDD	ADVSS	ATEST_IN	APAGE_UP	w
BAVDD	BIN[15]	BIN[14]	BIN[13]	BIN[12]	BIN[11]	BIN[10]	BIN[9]	BIN[8]	BAVDD	BIN[7]	BIN[6]	BIN[5]	BIN[4]	BIN[3]	BIN[2]	BIN[1]	BIN[0]	BAVDD	AVPP	ARSTN	ACSN	AWRN	4
AOUT[16	AIN[16]	воипле	BIN[16]																BAVDD	BAVSS	AAVDD	AAVSS	5
AOUT[17	AIN[17]	воит[16] воит[17]	BIN[17]																BIN[63]	воит[63]	AIN[63]	АОП[63]	6
] AOUT[18	AIN[18]	Boullus	BIN[18]																BIN[62]	] воит[62]	AIN[62]	AOUT[62]	7
אסטון16] אסטון17] אסטון18] אסטון18] אסטון20]	AIN[19]	BOUT[18] BOUT[19] BOUT[20]	BIN[19]				AAVSS	AAVSS	AAVSS	AAVSS	BDVSS	BDATA[3	BDATA[1]	BDVSS	BCLK				BIN[61]	BOUT[61	AIN[61]	AOUT[61	
AOUT[20]	AIN[20]	BOUT[20]	BIN[20]				AAVSS	BAVSS	BAVSS	BAVSS	BDVDD	BDATA[3] BDATA[2]	BDATA[0]	BDVDD	BDVSS				BIN[60]	воит[61] воит[60]	AIN[60]	AOUT[61] AOUT[60]	9
AOUT[21]	AIN[21]	BOUT[21]	BIN[21]				AAVSS	BAVSS						BTEST_IN	BPAGE_UP				BIN[59]	] воит[59]	AIN[59]	AOUT[59]	<b>5</b>
	AIN[22]	воит[22]	BIN[22]				AAVSS	BAVSS						BCSN	P BWRN				BIN[58]	воит[58]	AIN[58]	AOUT[58]	<b>±</b>
AOUT[23] AOUT[24] AOUT[25] AOUT[26]	AIN[23]		BIN[23]				AAVSS	BAVSS		(10b view)	STAFX	360 EBGA		BVPP	BRSTN				BIN[57]	BOUT[57	AIN[57]		12
AOUT[24	AIN[24]	BOUT[24	BIN[24]				AAVSS	BAVSS		3		-		BAVSS	AAVSS				BIN[56]	воит[57] воит[56]	AIN[56]	AOUT[57] AOUT[56]	ಚ
AOUT[25]	AIN[25]	воит[23] воит[24] воит[25]	BIN[25]				AAVSS	BAVSS						BAVSS	AAVSS				BAVDD	BAVSS	AAVDD	AAVSS	14
AOUT[26]	AIN[26]	воип[26]	BIN[26]				AAVSS	BAVSS	BAVSS	BAVSS	BAVSS	BAVSS	BAVSS	BAVSS	AAVSS				BIN[55]	воит[55]	AIN[55]	АОП[55]	5
AOUT[27]	AIN[27]		BIN[27]				AAVSS	AAVSS	AAVSS	AAVSS	AAVSS	AAVSS	AAVSS	BAVSS	AAVSS				BIN[54]		AIN[54]	A	ŧ6
AOUT[28]	AIN[28]	воит[28]	BIN[28]												•				BIN[53]	воит[53]	AIN[53]	оит[54] АОИТ[53] АОИТ[52]	17
AOUT[29]	AIN[29]	воипгэј	BIN[29]																BIN[52]	воит[52]	AIN[52]	AOUT[52]	<b>1</b> 50
АОП[30]	AIN[30]	воитвој	BIN[30]																BIN[51]	воит[51]	AIN[51]	AOUT[51]	19
אסטון	AIN[31]	BOUT[27] BOUT[28] BOUT[29] BOUT[30] BOUT[31] BIN[33]	BIN[31]	BIN[34]	BIN[35]	BIN[36]	BIN[37]	BIN[38]	BIN[39]	BAVDD	BIN[40]	BIN[41]	BIN[42]	BIN[43]	BIN[44]	BIN[45]	BIN[46]	BIN[47]	BIN[50]	воит[50]	AIN[50]	AOUT[50]	20
BIN[32]	воит[32]	BIN[33]	воит[33]	воит[34]	воипзы	воипзеј	воит[37]	воит[38]	воит[39]	BAVSS	ВОUТ[40]	воит[41]	воит[42]	воит[43]	воит[44]	BOUT[45]	воит[46]	BOUT[47] AIN[47]	BIN[49]	BOUT[54] BOUT[53] BOUT[51] BOUT[51] BOUT[50] BOUT[48]	AIN[49]	ΑΟυΤ[51] ΑΟυΤ[50] ΑΟυΤ[49] ΑΟυΤ[48]	21
AAVDD	AAVSS	BAVDD	BAVSS	AIN[34]	AIN[35]	AIN[36]	AIN[37]	AIN[38]	AIN[39]	AAVDD	AIN[40]	AIN[41]	AIN[42]	AIN[43]	AIN[44]	AIN[45]	AIN[46]		BIN[48]	BOUT[48]	AIN[48]	AOUT[48]	22
AIN[32]	АОПТ[32]	AIN[33]	АОП[33]	АОП[34]	АОП[35]	АОП[36]	АОП[37]	АОП[38]	АОП[39]	AAVSS	ΑΟυΤ[40]	AOUT[41]	ΑΟυτ[42]	АОП[43]	AOUT[44]	ΑΟυΤ[45]	ΑΟυτ[46]	AOUT[47]	BAVDD	BAVSS	AAVDD	AAVSS	23

# PIN DESCRIPTIONS\_

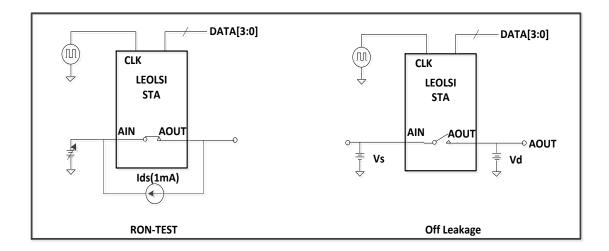
PIN NAME	I/O	Descriptions
ACLK	DI	System clock (TOP)
ARSTN	DI	System reset. Active Low (TOP)
ACSN	DI	Chip select. Active Low (TOP)
AWRN	DI	Data write enable. Active Low (TOP)
ADATA[3:0]	DIO	Data bus (TOP)
ATEST_IN	DI	Tied to GND in Normal mode (TOP)
APAGE_UP	DI	Tied to GND in Normal mode (TOP)
AVPP	PWR	Tied to GND in Normal mode (TOP)
AIN[63:0]	Al	Analog switch input (TOP)
AOUT[63:0]	AO	Analog switch output (TOP)
AAVDD	PWR	Analog Power (TOP)
AAVSS	GND	Analog Ground (TOP)
ADVDD	PWR	Digital Power (TOP)
ADVSS	GND	Digital Ground (TOP)
BCLK	DI	System clock (BOTTOM)
BRSTN	DI	System reset. Active Low (BOTTOM)
BCSN	DI	Chip select. Active Low (BOTTOM)
BWRN	DI	Data write enable. Active Low (BOTTOM)
BDATA[3:0]	DIO	Data bus (BOTTOM)
BTEST_IN	DI	Tied to GND in Normal mode (BOTTOM)
BPAGE_UP	DI	Tied to GND in Normal mode (BOTTOM)
BVPP	PWR	Tied to GND in Normal mode (BOTTOM)
BIN[63:0]	Al	Analog switch input (BOTTOM)
BOUT[63:0]	AO	Analog switch output (BOTTOM)
BAVDD	PWR	Analog Power (BOTTOM)
BAVSS	GND	Analog Ground (BOTTOM)
BDVDD	PWR	Digital Power (BOTTOM)
BDVSS	GND	Digital Ground (BOTTOM)

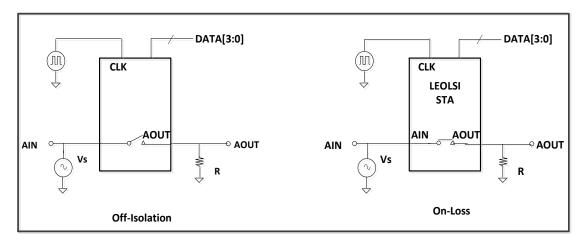
Al: analog input Dl: digital Input PWR: power AO: analog output DIO: digital Input / Output

**GND**: ground

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## TEST CIRCUITS





Off isolation=20log(V<sub>AOUT</sub>/V<sub>AIN</sub>), On Loss=20log(V<sub>AOUT</sub>/V<sub>AIN</sub>)

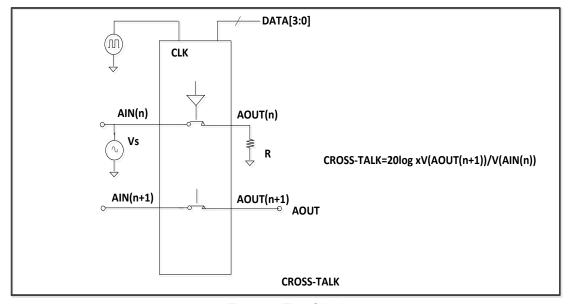
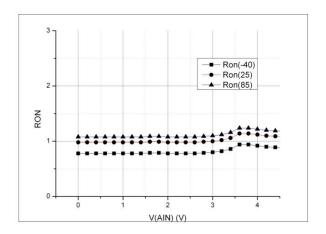


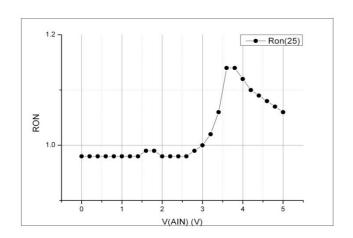
Figure 7. Test Circuits

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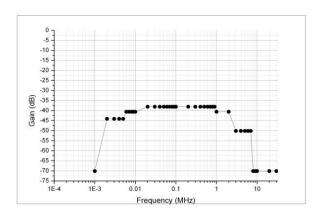
## TEST RESULTS



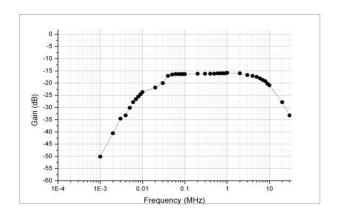
On-resistance vs. vain



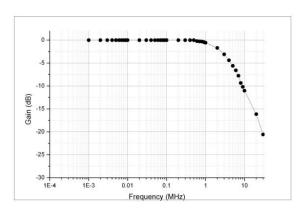
On-resistance(room temp) vs. vain



Cross talk vs. Frequency



Isolation vs. Frequency



On Loss vs. Frequency

Figure 8. Test Results

#### **DETAIL DESCRIPTIONS\_**

#### **Definitions**

The STA-FX IC consists of 16 cores which consist of 8 switches, hence it has 128 switches. The device provides two Chip-IDs for Top and Bottom and they can be programmed in internal OTP memory inside Top and Bottom individually. On the other hand, the eight Core-IDs of Top and Bottom are fixed in the device. The internal switch structure is shown in Figure 9. The Channel-ID is implicated in user defined commands interpreted in Digital Interface section.

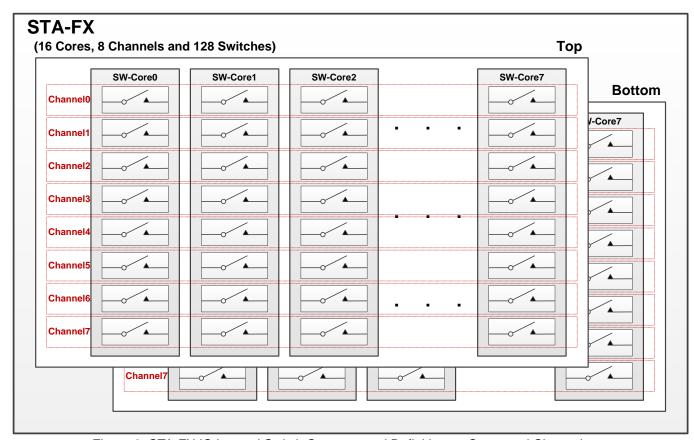


Figure 9. STA-FX IC Internal Switch Structure and Definitions – Cores and Channels

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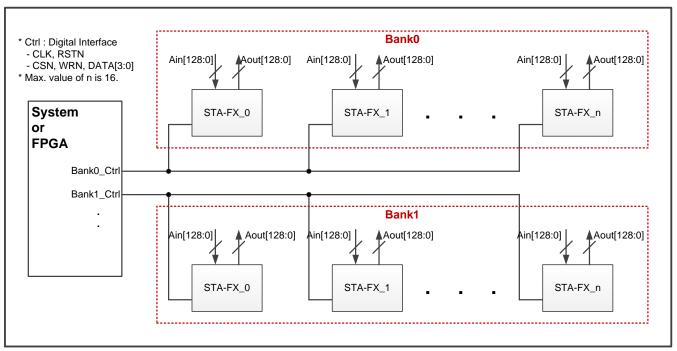


Figure 10. STA-FX IC Application Structure and Definitions - Banks and Controls

In system application, two or more STA-FX ICs can be controlled by the same digital interface - control and data signals such as CLK, RESETN, CSN, WRN and DATA[3:0] shown in Figure 10 and these STA-FX IC network can be called as 'bank'. Because the Chip-ID is assigned in 5-bit address and two Chip-IDs can be used in one STA-FX IC, the maximum number of STA-FX IC in one bank is 16. The 3-bit address is used to assign Core-ID in Top and Bottom of STA-FX IC individually. The user can not apply the Chip-ID and the Core-ID to 1-clock command but to 2-clock command. Refer to Figure 12 and 13.

#### - Bank

The bank means STA network connected by the same digital interface - control and data signals such as CLK, RESETN, CSN, WRN and DATA[3:0]. Refer to the Figure 10.

#### - Reject

The individual switch control logic can be rejected from all commands. After entering reject state in which the switch is off, no command alters on/off state of rejected switch except the command 'INITIAL\_ALL', 'CANCEL\_REJECT' and external RSTN.

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#### Digital Interface

#### - 1-Clock Command

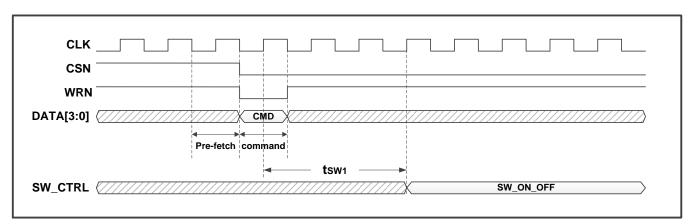


Figure 11. 1-Clock Command Control Timing Diagram

The 1-clock command is applied to all cores and all switches. Furthermore, this command is applied to all STA ICs in the same bank. The 'CMD' in Figure 11 means command which defines following modes:

Command	Value	Function
NORMAL	0x0	Returns to normal mode from Load mode (release all chip selection)
LOAD_ALL	0x1	Selects all chips to load(apply) the same commands
VIRTUAL	0x2	Programming mode for test
CLEAR_ALL	0x3	Makes all switches off
ENABLE_ALL	0x4	Makes all switches on
INITIAL_ALL	0x5	Initializes all switches releasing reject condition and making them on

#### - 2-Clock Command

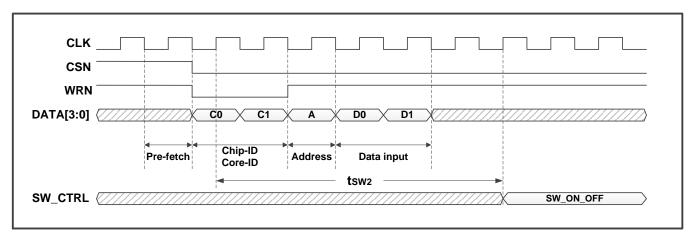


Figure 12. 2-Clock Command Control Timing Diagram

The '2-clock command' can control 8 Cores individually as well as simultaneously. Especially, the case of simultaneous 8 Core control can explain Channel-level switch control and it means that the users do not access Channel-ID directly.

In 2-clock command protocol, the signal DATA[3:0] can represent several items 'C0', 'C1', 'A', 'D0' and 'D1' shown in Figure 12 and these can be interpreted like as Figure 13.

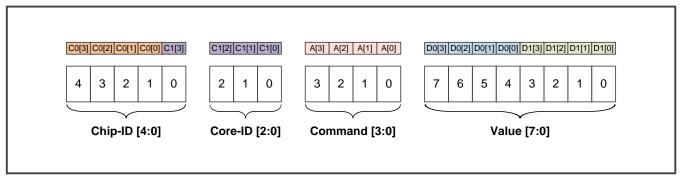


Figure 13. Interpretation of DATA[3:0] Signals in 2-Clock Command

The 'C0' and 'C1' are Chip-ID and Core-ID items and the address 'A' defines switch control Command. The Data 'D0' and 'D1' means the next state Value of 8 individual switches.

The 2-Clock command has three types of control.

- CHL(Chip-level) : applied to all chips in the same bank (both Chip-ID and Core-ID are ignored)
- CRL(Core-level) : applied to all cores of selected chip (Chip-ID is referred but Core-ID is ignored)
- SWL(Switch-level): applied to selected switches of selected core (both Chip-ID and Core-ID are referred)

When the MSB of Command[3:0] is low, the Value[7:0] is applied to all Cores. Otherwise, the MSB of Command[3:0] is high, the Value[7:0] is applied to one Core selected by Core-ID[2:0].

The detail 2-Clock commands are given below.

Command	Value	Function	Remark
AND_CRL	0x0	Next switch status are produced by bitwise AND operation between current switch status and Data[7:0]. Applied to all cores of the selected chip.	CRL
OR_CRL	0x1	Next switch status are produced by bitwise OR operation between current switch status and Data[7:0] ].  Applied to all cores of the selected chip.	CRL
DIRECT_CRL	0x2	Next switch status are produced by Data[7:0] directly.  Applied to all cores of the selected chip.	CRL
DIRECT_CHL	0x3	Next switch status are produced by Data[7:0] directly. Applied to all cores of all chips in the same bank.	CHL
REJECT_CRL	0x4	Reject all switches of selected core by bitwise AND operation between current core reject status and Data[7:0].	CRL
-	0x5	Reserved	-
-	0x6	Reserved	-
-	0x7	Reserved	
AND_SWL	0x8	Next switch status are produced by bitwise AND operation between current switch status and Data[7:0]. Applied to the selected core.	SWL
OR_SWL	0x9	Next switch status are produced by bitwise OR operation between current switch status and Data[7:0].  Applied to the selected core.	SWL
DIRECT_SWL	0xa	Next switch status are produced by Data[7:0] directly. Applied to the selected core.	SWL
-	0xb	Reserved	-
REJECT_CRL	0xc	Reject selected switch by bitwise AND operation between current switch reject status and Data[7:0]	SWL
CANCEL_RJT	0xd	Cancel all switch-reject of selected core	-
-	0xe	Reserved	-
-	0xf	Reserved	-

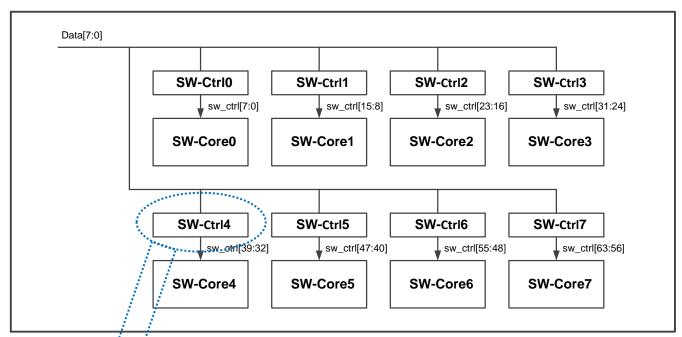


Figure 14. Switch Control Structure for 2-Clock Command

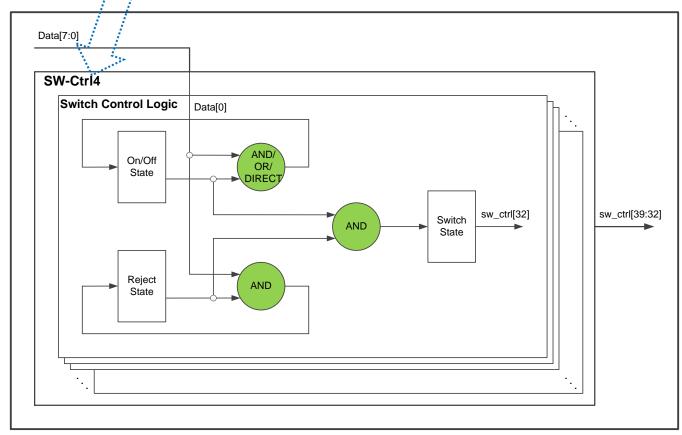


Figure 15. Basic Concept of 2-Clock Command Switch Control

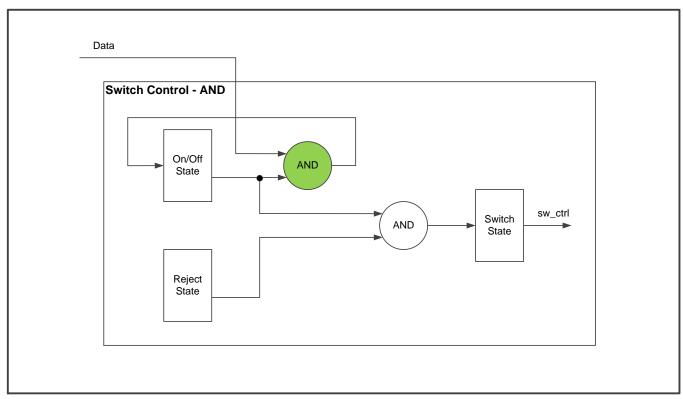


Figure 16. 2-Clock Command Switch Control - AND

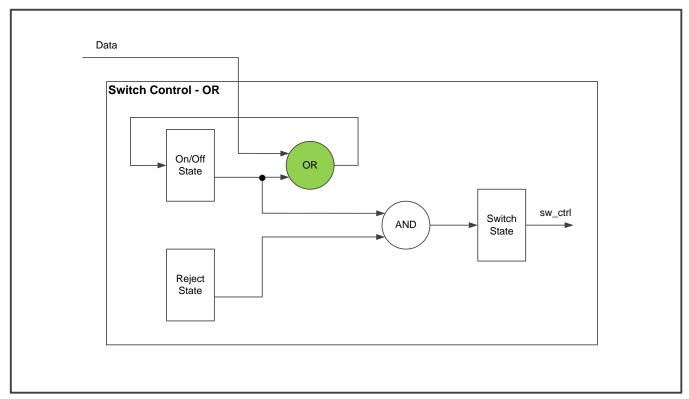


Figure 17. 2-Clock Command Switch Control - OR

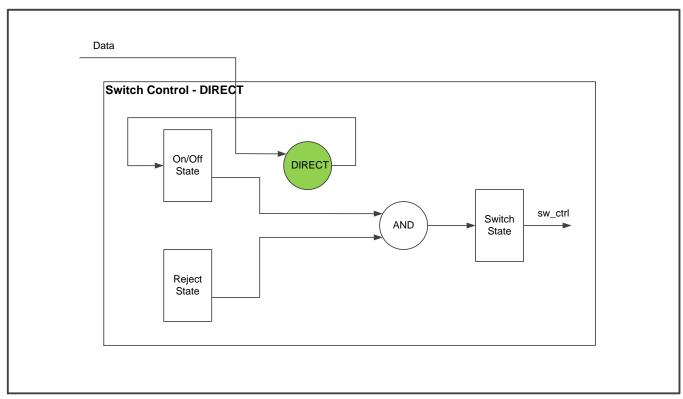


Figure 18. 2-Clock Command Switch Control - DIRECT

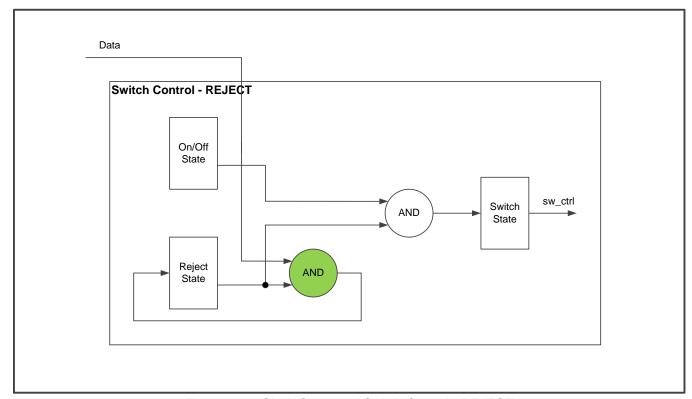


Figure 19. 2-Clock Command Switch Control - REJECT

## **APPLICATION EXAMPLE**

The STA IC receives serial input data synchronized with a clock signal.

Most of all, to achieve maximum control speed in PCB, simulation using IBIS model should be carried out.

- 1. TEST\_IN, PAGE\_UP and VPP pins should be connected to ground through 20-k $\Omega$  (pull-down) resistor.
- 2. CSN pin should be connected to digital power through 20-k $\Omega$  (pull-up) resistor.
- 3. To guarantee the control speed, any resistor or capacitor should not be connected to CLK and DATA pins.

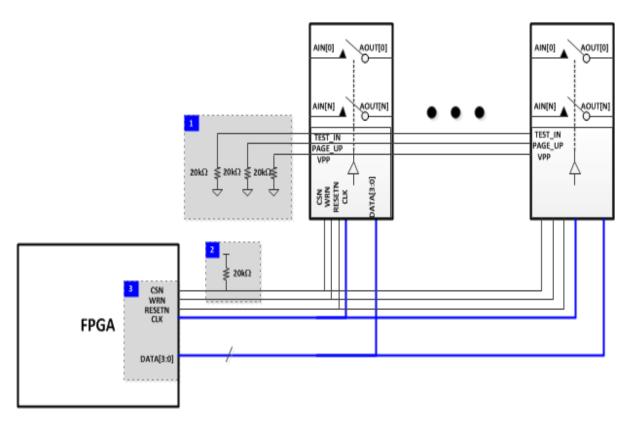
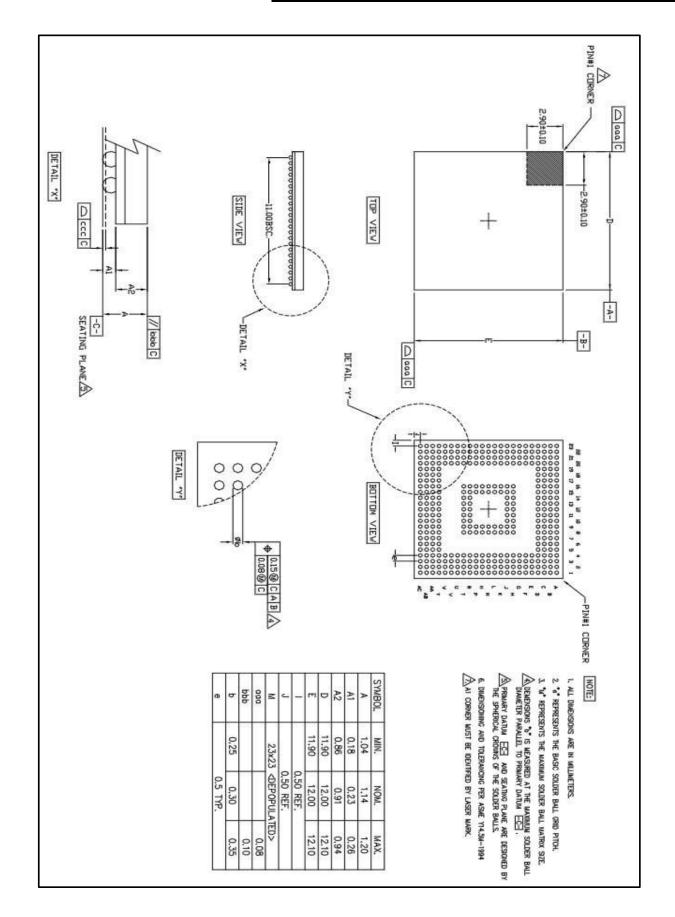


Figure 20. Application Example of PCB design

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## PACKAGE INFORMATION



## **REVISION HISTORY\_**

Revision	Date	Description					
0.0	2012-06	Initial draft					
1.0	2013-11	Revised format					

## DOCUMENT INFORMATION

File name: STA-FX Datasheet

Product code: STA-FX

Product description: Analog Switch IC

Document revision: 1.0 Revision date: 2013-11



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