SP2003 Datasheet

2-in/6-out CMOS PMIC

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The world is driven by analog

GENERAL DESCRIPTION

The SP2003 is a PMIC with four LDOs and two current limit switches for supplying power during four DUT test. The LDOs are controllable output voltage with wide range and high resolution. Each LDO has Current Limit function. In addition, the thermal shutdown function will automatically turn off All channel temperature exceeds 170°C.

All digital input pins adopt the Schmitt trigger I/O, which has 0.5-V to 1.3-V input noise margin to ensure TTL/CMOS-logic compatibility when using a 1.8-V power supply.

And these feature output active discharge function.

Finally The SP2003 can configure up to 16 Daisy chains.

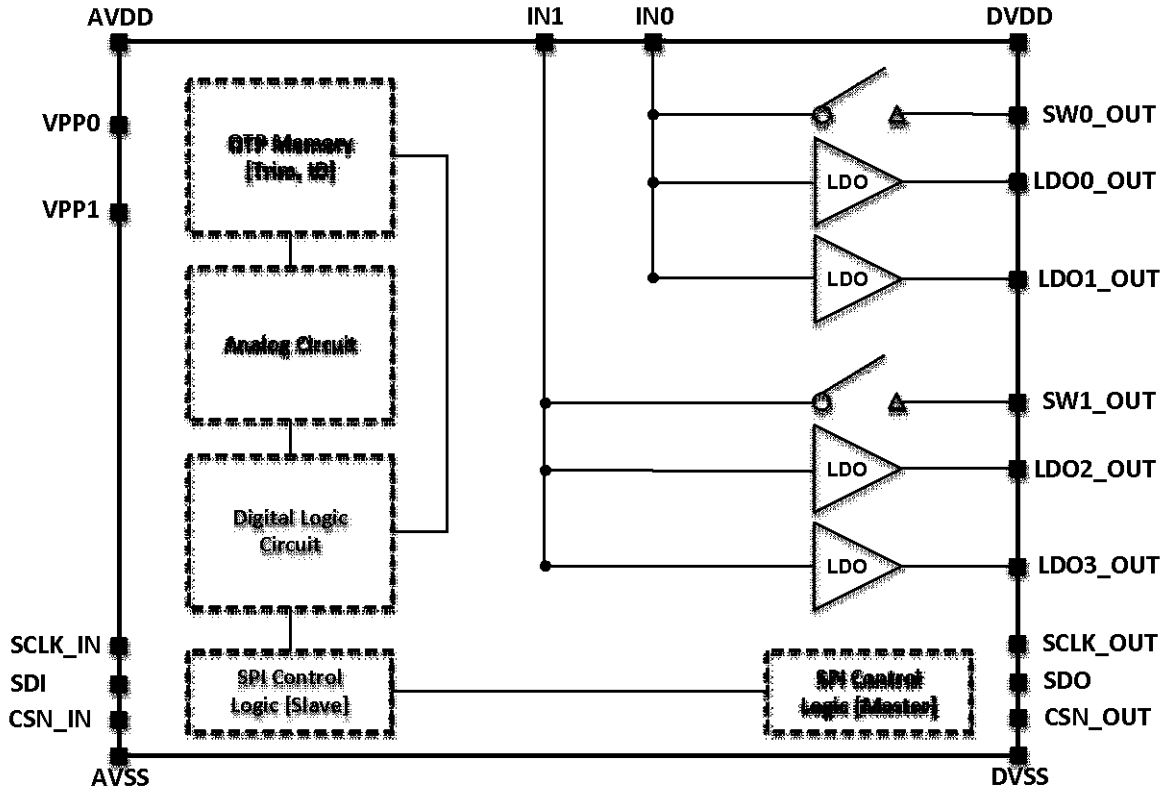
APPLICATIONS

Power distribution system
Industrial equipment
Memory test
Probe Card

FEATURE

SPI protocol interface
1.8V logic-compatible input (V_{IH}=1.3V, V_{IL}=0.5V)
Dual supply operation: 1.8V for digital, 5V for analog
Analog signal frequency: DC-to-10KHz
LDO maximum load current: 200mA
Wide range analog input from 1.65V to 4.8V
Wide range LDO output from 0.4V to 3.35V
High resolution LDO output step: 10mV
Low on leakage current LDO: 400nA (@125˚C)
LDO Output accuracy: < ±1.5%
Low on-resistance: 0.3Ω (@typ)
Thermal shutdown temperature:
170°C All Channel Off(CLS no Operating)
150°C Corresponding Channel Off(CLS Operating)
Current Limit Level : 220mA
Fold-back Current Limit Level : 110mA
Reverse Current Block
Active Discharge
24-pin SiP package
Daisy chain

FUNCTIONAL BLOCK DIAGRAM



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PIN MAPPING TABLE

	1	2	3	4	5	6	
A	LDO2	SCLK_OUT	VPP1(DVDD)	VPP0(DVDD)	SCLK_IN	LDO0	A
B	SW1	CSN_OUT	SDO	SDI	CSN_IN	SW0	B
C	AIN1	TEST1	NC1	NC0	TEST0	AIN0	C
D	LDO3	AVSS	AVDD	DVSS	DVDD	LDO1	D
	1	2	3	4	5	6	

PIN DESCRIPTIONS

D: Digital, A: Analog

O: Output, I: Input, P: Power, G: Ground

Power

Name	I/O	Description
AVDD	P	Analog Power.
DVDD	P	Digital Power.
AVSS	G	Analog Ground
DVSS	G	Digital Ground
VPP[1:0]	P	Digital Power.

SPI Interface (6 pins)

Name	I/O	Description
SCLK_IN	I	SPI Clock In
SDI	I	SPI Data In
CSN_IN	I	Chip Select In
SCLK_OUT	O	SPI Clock Out
SDI	O	SPI Data Out
CSN_IN	O	Chip Select Out

Analog

Name	I/O	Description
AIN[1:0]	I	Analog Switch/LDO Input
SW OUT[1:0]	O	Analog Switch Output
LDO OUT[3:0]	O	Analog LDO Output

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. The functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Input Voltage	Vin		-0.3 to 6.0	V
Control Voltage	VCT		-0.3 to 6.0	V
Output Voltage	VOUT		-0.3 to 6.0	V
Output Current	IOUT		Internally limited	-
Power Dissipation	PD		TBD	mW
Operating Temperature Range	Topr		-40 to 125	°C
Junction Temperature	Tj		175	°C
Storage Temperature	Tstg		-55 to 150	°C

NOTE: The device is not guaranteed to operate properly above those listed in “Absolute Maximum Ratings”.

ELECTRICAL CHARACTERISTICS(TA = +25°C)

VDD=5.0V, VSS=0V, DVDD=1.8V, DVSS=0V and TA = +25°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
POWER SUPPLIES							
Analog Supply Voltage		AVDD		4.5	5	5.5	V
Digital Supply Voltage		DVDD		1.62	1.8	1.98	V
Analog Ground Voltage		AVSS			0		V
Digital Ground Voltage		DVSS			0		V
ANALOG SWITCH							
Input Voltage Range		V_{AIN}	VDD=5V	1.65V		4.8V	V
Output Voltage Range		V_{SWOUT}	VDD=5V	1.65V		4.8V	V
Switch On-resistance		R_{ON}	I_{CH_ON}=10mA		0.3	0.4	Ω
Switch Leakage Current	Channel ON Leakage Current	I_{CH_ON}	V_{AIN}=3.3V			10	nA
	Channel OFF Leakage Current Input	I_{CH_OFFI}	V_{AIN}=3.3V, V_{SWOUT}=0V			10	nA
	Channel OFF Leakage Current Output	I_{CH_OFFO}	V_{AIN}=3.3V, V_{SWOUT}=0V			10	nA

Current Limit Level		I_{CL}	Fold-back Off	187	220	253	mA
Fold-back Current Limit Level		I_{FCL}	Fold-back On	93	110	127	mA
Fold-back Time		T_F		100		200	us
Reverse Current Block		I_{RC}	V_{AIN}=1.65V, V_{SWOUT}=3.0V		-10		nA
Switch On / OFF Time	Switch On Time	T_{ON_CLN}	V_{AIN}=4.8V, Current Limit Function ON, Load R=500Ω, Load C=100nF	7.9	10.7	14.3	us
		T_{ON_CLF}	V_{AIN}=4.8V, Current Limit Function OFF, Load R=500Ω, Load C=100nF	3.96	4.82	5.82	us
	Switch Off Time	T_{OFF_CLN}	V_{AIN}=4.8V, Current Limit Function ON, Load R=500Ω, Load C=100nF	3.53	3.72	3.88	us
		T_{OFF_CLF}	V_{AIN}=4.8V, Current Limit Function OFF, Load R=500Ω, Load C=100nF	21.9	24.2	26.6	us
Capacitance	Input Off-Capacitance	C_{AIN_OFF}	*Guaranteed by design. Cannot be guaranteed by testing			500	pF
	Output Off-Capacitance	$C_{SWOUT\ OFF}$				500	pF
	Output On-Capacitance	$C_{SWOUT\ ON}$				1000	pF
LOW DROP OUTPUT							
Input Voltage Range		V_{AIN}	VDD=5V	1.65		4.8	V
Output Voltage Range		V_{LDOOUT}	VDD=5V	0.4		3.35	V
Output Control Step Voltage		V_{STEP}			10		mV
Maximum Load Current		I_{MAX}			200		mA
Current Limit Level		I_{CL}	Fold-back Off	187	220	253	mA
Fold-back Current Limit Level		I_{FCL}	Fold-back On	93	110	127	mA
Fold-back Time		T_F		100		200	us
Drop Out Voltage		V_{DO}	V_{LDOOUT} =1.8V, Load = 200mA	183	207	221	mV
			V_{LDOOUT} =1.2V, Load = 200mA	453	470	505	mV
Load Regulation			V_{AIN} =3.3V, V_{LDOOUT} =1.8V Load = 1uA ~ 200mA	0.4	0.5	0.6	%
			V_{AIN} =3.3V, V_{LDOOUT} =1.2V Load = 1uA ~ 200mA	0.6	0.7	0.8	%
Line Regulation			V_{AIN} =1.65V ~ 4.8V, V_{LDOOUT} =1.2V, Load = 10mA	0.7	0.8	0.9	%
Reverse Current Block		I_{RC}	V_{AIN}=1.65V, $V_{LDOOUTT}$=3.0V		10		nA
LDO Leakage Current	Channel ON Leakage Current	I_{CH_ON}	V_{AIN}=3.3V, V_{LDOOUT}=1.2V			310	nA
	Channel OFF Leakage Current Input	I_{CH_OFFI}	V_{AIN}=3.3V, V_{LDOOUT}=0V			10	nA

	Channel OFF Leakage Current Output	I_{CH_OFFO}	V_{AIN}=3.3V, V_{LDOOUT}=0V			10	nA
LDO On / OFF Time	LDO On Time	T_{ON_CLN}	V_{AIN}=4.8V, Current Limit Function ON, Load R=500Ω, Load C=100nF	18.8	23.8	30.1	us
		T_{ON_CLF}	V_{AIN} =4.8V, V_{LDOOUT} =1.2V Current Limit Function OFF, Load R=500Ω, Load C=100nF	14.6	18.8	23.6	us
	LDO Off Time	T_{OFF_CLN}	V_{AIN} =4.8V, V_{LDOOUT} =1.2V Current Limit Function ON, Load R=500Ω, Load C=100nF	3.34	3.53	3.71	us
		T_{OFF_CLF}	V_{AIN} =4.8V, V_{LDOOUT} =1.2V Current Limit Function OFF, Load R=500Ω, Load C=100nF	3.34	3.53	3.71	us
Capacitance	Input Off-Capacitance	$C_{AIN\ OFF}$	*Guaranteed by design. Cannot be guaranteed by testing			500	pF
	Output Off-Capacitance	$C_{LDOOUT\ OFF}$				500	pF
	Output On-Capacitance	C_{LDOOUT_ON}				1000	pF
TSD / Active Discharge							
Thermal Shutdown Temperature		T_{ST_CLN}	Guaranteed by design. Cannot be guaranteed by testing.		+170		°C
		T_{ST_CLF}			+150		C
Thermal Shutdown Hysteresis		T_{SH}			15		°C
Output Discharge Resistance		R_{DS}			1		kΩ
Leakage(Switch + LDO[1:0])							
Leakage Current		I_{CH_OFF}	V_{AIN}=3.3V, V_{SWOUT}=0V, V_{LDOOUT} =1.2V	-10		30	nA
		I_{CH_ON}	V_{AIN}=3.3V, V_{LDOOUT} =1.2V			700	nA
Reverse Current Block		I_{RC}	V_{AIN}=1.65V, V_{SWOUT}=3.0V, $V_{LDOOUTT}$=3.0V	-10		30	nA
Power CONSUMPTION							
Analog Operating Current (AVDD)	Static	I_{AVDD_ST}	Load R=3Ω, Load C=100nF (ALL CLS Operating)		1.3		mA
			Load R=500Ω, Load C=100nF (ALL CLS No Operating)		0.8		mA
			Load R=500Ω, Load C=100nF (ALL OFF)		0.5		mA
	Dynamic	I_{AVDD_DYN}	AVDD=5V, f_{CLK}=25MHz, f_{SW}=10kHz		0.8		mA
Digital Operating	Static	I_{DVDD_ST}	DVDD=1.8V				mA

Current (DVDD)	Dynamic	I_{DVDD_DYN}	DVDD=1.8V, f_{CLK}=25MHz, f_{SW}=10kHz Cp* = 50pF Cp* : Parasitic Capacitance				mA

ELECTRICAL CHARACTERISTICS(TA = +125°C)

VDD=5.0V, VSS=0V, DVDD=1.8V, DVSS=0V and TA = +125°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
POWER SUPPLIES							
Analog Supply Voltage		AVDD		4.5	5	5.5	V
Digital Supply Voltage		DVDD		1.62	1.8	1.98	V
Analog Ground Voltage		AVSS			0		V
Digital Ground Voltage		DVSS			0		V
ANALOG SWITCH							
Input Voltage Range		V_{AIN}	VDD=5V	1.65V		4.8V	V
Output Voltage Range		V_{SWOUT}	VDD=5V	1.65V		4.8V	V
Switch On-resistance		R_{ON}	I_{CH_ON}=10mA		0.4	0.5	Ω
Switch Leakage Current	Channel ON Leakage Current	I_{CH_ON}	V_{AIN}=3.3V			20	nA
	Channel OFF Leakage Current Input	I_{CH_OFFI}	V_{AIN}=3.3V, V_{SWOUT}=0V			20	nA
	Channel OFF Leakage Current Output	I_{CH_OFFO}	V_{AIN}=3.3V, V_{SWOUT}=0V			20	nA
Current Limit Level		I_{CL}	Fold-back Off	187	220	253	mA
Fold-back Current Limit Level		I_{FCL}	Fold-back On	93	110	127	mA
Fold-back Time		T_F		100		200	us
Reverse Current Block		I_{RC}	V_{AIN}=1.65V, V_{SWOUT}=3.0V		-20		nA
Switch On / OFF Time	Switch On Time	T_{ON_CLN}	V_{AIN}=4.8V, Current Limit Function ON, Load R=500Ω, Load C=100nF	5.2	7.3	17	us
		T_{ON_CLF}	V_{AIN}=4.8V, Current Limit Function OFF, Load R=500Ω, Load C=100nF	3.6	4.4	6.1	us

	Switch Off Time	T_{OFF_CLN}	V_{AIN}=4.8V, Current Limit Function ON, Load R=500Ω, Load C=100nF	3.5	3.8	3.9	us
		T_{OFF_CLF}	V_{AIN}=4.8V, Current Limit Function OFF, Load R=500Ω, Load C=100nF	22	24	27	us
Capacitance	Input Off-Capacitance	C_{AIN_OFF}	*Guaranteed by design. Cannot be guaranteed by testing			500	pF
	Output Off-Capacitance	$C_{SWOUT\ OFF}$				500	pF
	Output On-Capacitance	$C_{SWOUT\ ON}$				1000	pF
LOW DROP OUTPUT							
Input Voltage Range		V_{AIN}	VDD=5V	1.65		4.8	V
Output Voltage Range		V_{LDOOUT}	VDD=5V	0.4		3.35	V
Output Control Step Voltage		V_{STEP}			10		mV
Maximum Load Current		I_{MAX}			200		mA
Current Limit Level		I_{CL}	Fold-back Off	187	220	253	mA
Fold-back Current Limit Level		I_{FCL}	Fold-back On	93	110	127	mA
Fold-back Time		T_F		100		200	us
Drop Out Voltage		V_{DO}	V_{LDOOUT} =1.8V, Load = 200mA	170	210	230	mV
			V_{LDOOUT} =1.2V, Load = 200mA	460	480	510	mV
Load Regulation			V_{AIN} =3.3V, V_{LDOOUT} =1.8V Load = 1uA ~ 200mA	0.5	0.6	0.7	%
			V_{AIN} =3.3V, V_{LDOOUT} =1.2V Load = 1uA ~ 200mA	0.7	0.8	1.0	%
Line Regulation			V_{AIN} =1.65V ~ 4.8V, V_{LDOOUT} =1.2V, Load = 10mA	0.8	0.9	1.0	%
Reverse Current Block		I_{RC}	V_{AIN}=1.65V, $V_{LDOOUTT}$=3.0V		20		nA
LDO Leakage Current	Channel ON Leakage Current	I_{CH_ON}	V_{AIN}=3.3V, V_{LDOOUT}=1.2V			350	nA
	Channel OFF Leakage Current Input	I_{CH_OFFI}	V_{AIN}=3.3V, V_{LDOOUT}=0V			20	nA
	Channel OFF Leakage Current Output	I_{CH_OFFO}	V_{AIN}=3.3V, V_{LDOOUT}=0V			20	nA
LDO On / OFF Time	LDO On Time	T_{ON_CLN}	V_{AIN}=4.8V, Current Limit Function ON, Load R=500Ω, Load C=100nF	18	23	37	us
		T_{ON_CLF}	V_{AIN} =4.8V, V_{LDOOUT} =1.2V Current Limit Function OFF, Load R=500Ω, Load C=100nF	13	17	25	us
	LDO Off Time	T_{OFF_CLN}	V_{AIN} =4.8V, V_{LDOOUT} =1.2V Current Limit Function ON, Load R=500Ω, Load C=100nF	3.0	3.4	3.7	us
		T_{OFF_CLF}	V_{AIN} =4.8V, V_{LDOOUT} =1.2V Current Limit Function OFF, Load R=500Ω, Load C=100nF	3.0	3.4	3.7	us

Capacitance	Input Off-Capacitance	$C_{AIN\ OFF}$	*Guaranteed by design. Cannot be guaranteed by testing			500	pF
	Output Off-Capacitance	$C_{LDOOUT\ OFF}$				500	pF
	Output On-Capacitance	C_{LDOOUT_ON}				1000	pF
TSD / Active Discharge							
Thermal Shutdown Temperature		T_{ST_CLN}	Guaranteed by design. Cannot be guaranteed by testing.		+170		°C
		T_{ST_CLF}			+150		C
Thermal Shutdown Hysteresis		T_{SH}			15		°C
Output Discharge Resistance		R_{DS}			1		kΩ
Leakage(Switch + LDO[1:0])							
Leakage Current		I_{CH_OFF}	V_{AIN}=3.3V, V_{SWOUT}=0V, V_{LDOOUT} =1.2V	-10		60	nA
		I_{CH_ON}	V_{AIN}=3.3V, V_{LDOOUT} =1.2V			750	nA
Reverse Current Block		I_{RC}	V_{AIN}=1.65V, V_{SWOUT}=3.0V, $V_{LDOOUTT}$=3.0V	-10		60	nA
Power CONSUMPTION							
Analog Operating Current (AVDD)	Static	I_{AVDD_ST}	Load R=3Ω, Load C=100nF (ALL CLS Operating)		1.6	1.9	mA
			Load R=500Ω, Load C=100nF (ALL CLS No Operating)		0.9	1.1	mA
			Load R=500Ω, Load C=100nF (ALL OFF)		0.5	0.6	mA
	Dynamic	I_{AVDD_DYN}	AVDD=5V, f_{CLK}=25MHz, f_{SW}=10kHz		1.0		mA
Digital Operating Current (DVDD)	Static	I_{DVDD_ST}	DVDD=1.8V				mA
	Dynamic	I_{DVDD_DYN}	DVDD=1.8V, f_{CLK}=25MHz, f_{SW}=10kHz Cp* = 50pF Cp* : Parasitic Capacitance				mA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
DIGITAL I/O							
Logic Input Voltage	Input High	V_{IH}		0.9			V
	Input Low	V_{IL}				0.4	V
Logic Input Current	Input High	I_{IH}		-1		1	μA
	Input Low	I_{IL}		-1		1	μA
SCLK_IN Period		t_{PERIOD}			40		ns
SDI to SCLK_IN Setup Time		t_{SS}		2.5		5	ns
SDI to SCLK_IN Hold Time		t_{SH}		2.5		5	ns
CSN to SCLK_IN Setup Time		t_{CS}		2.5		5	ns
CSN to SCLK_IN Hold Time		t_{CH}		2.5		5	ns

TIMING CHARACTERISTICS

Timing Diagram of Digital SPI I/O Signals

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
SCLK_IN Period	t_{PERIOD}	SPI Clock Speed 25MHz				ns
SDI Setup Time	t_{SS}					ns
SDI Hold Time	t_{SH}					ns
CSN Setup Time	t_{CS}					ns
CSN Hold Time	t_{CH}					ns
SCLK_OUT Setup Time	t_{SOS}					ns
SCLK_IN High Pulse	t_{PH}	ratio of SCLK_IN				%
SCLK_IN Low Pulse	t_{PL}	ratio of SCLK_IN				%

Write Timing

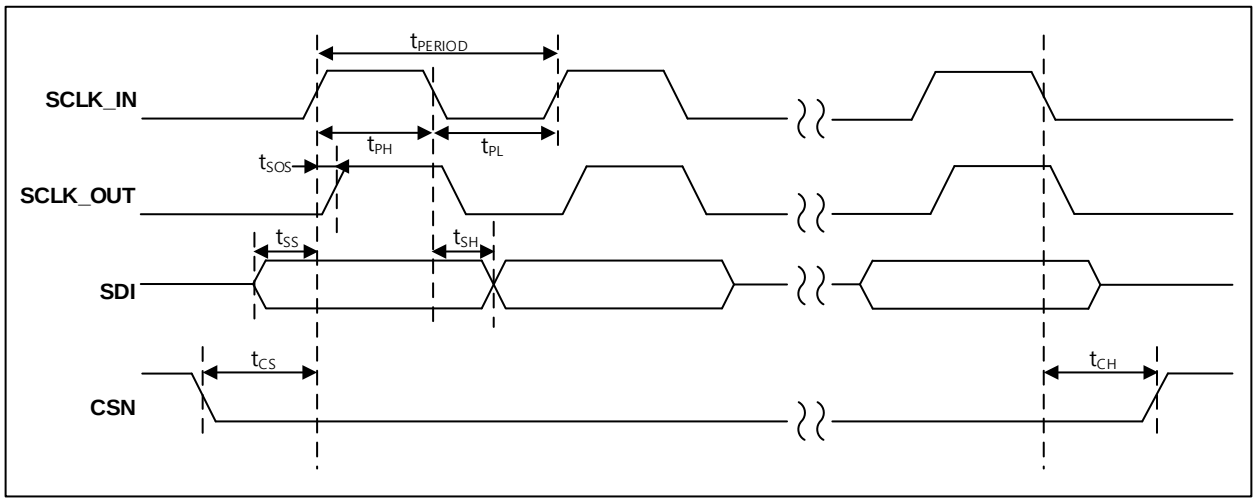


Figure 1. Timing Diagram of Digital Signals.

Power up and down Sequence

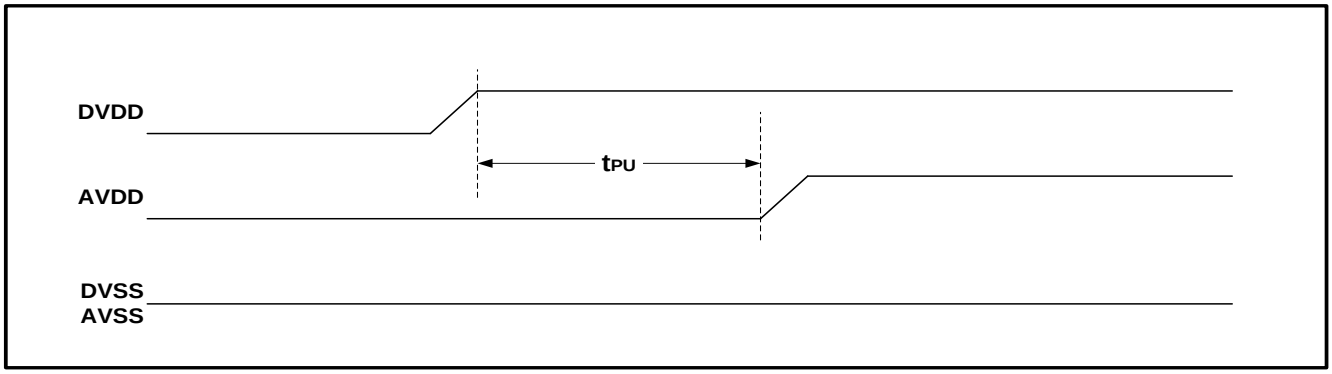


Figure 2. Power-up Sequence.

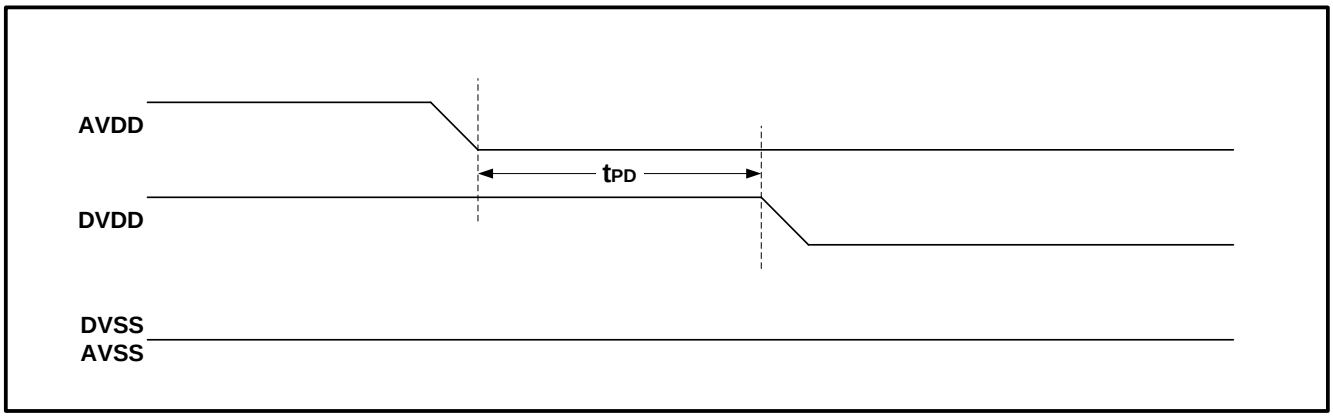


Figure 3. Power-down Sequence.

Power up Operation Sequence

The Power-up Operation Sequence of SP2003 Shall Be Wait for OSC Stable time(250ns * 15).

The SP2003 does not have a EXTERNAL RESET PIN, it has to wait for the operation of the internal DIGITAL POR.

Figure 4. SP2003 Power UP Operation Diagram shows the Power-up sequence of SP2003.

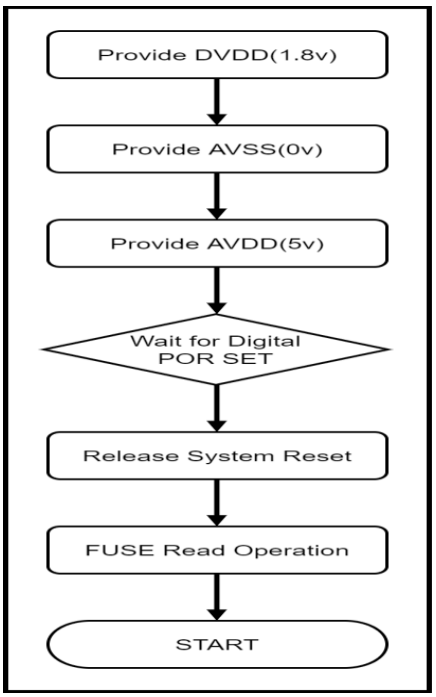


Figure 4. Power-UP Operation Diagram.

SW On/Off Timing Diagram

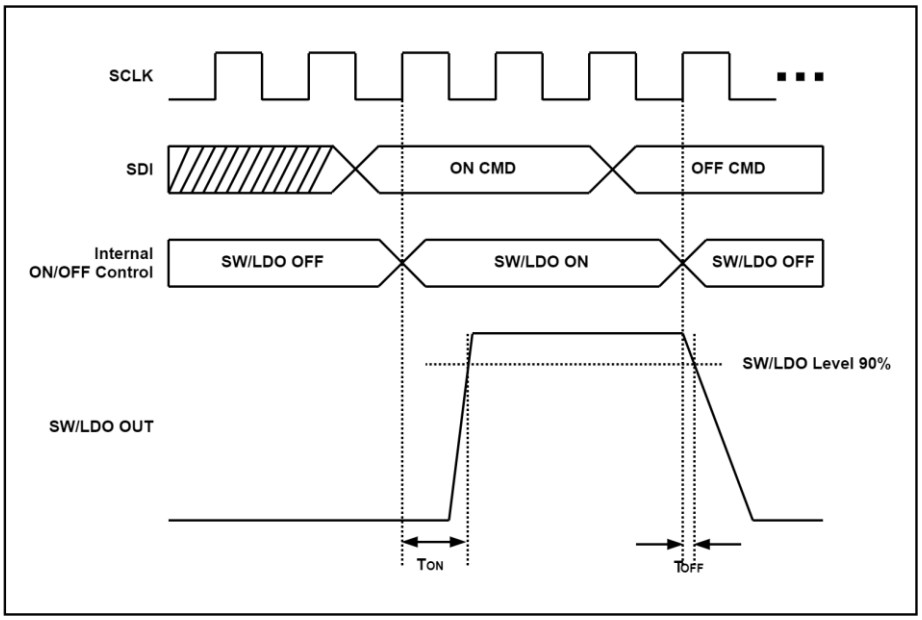


Figure 5. SW ON/OFF Timing Diagram

Current Limit Operating Timing Diagram

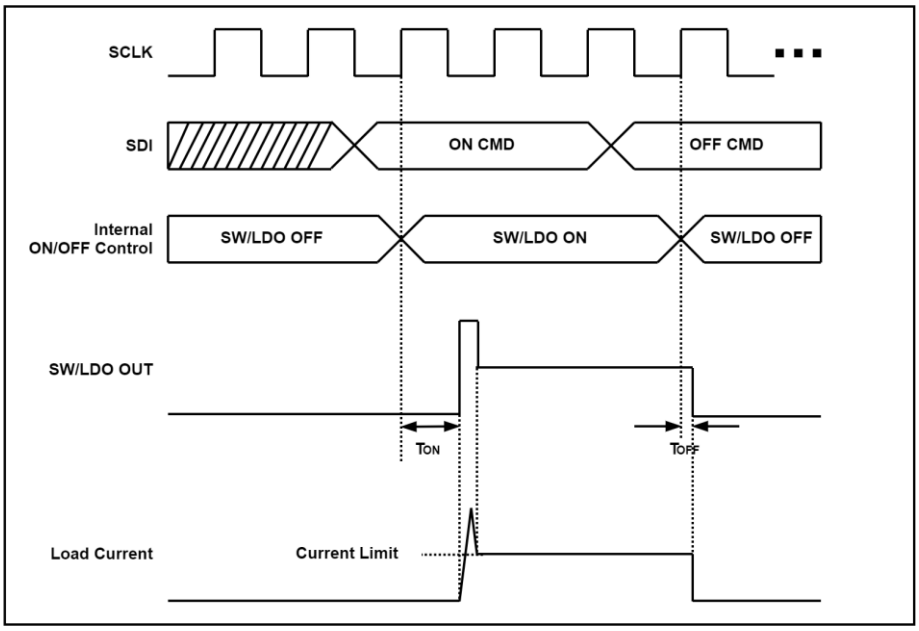


Figure 6. Current Limit Operating Timing Diagram.

Current Limit Foldback Operating Timing Diagram

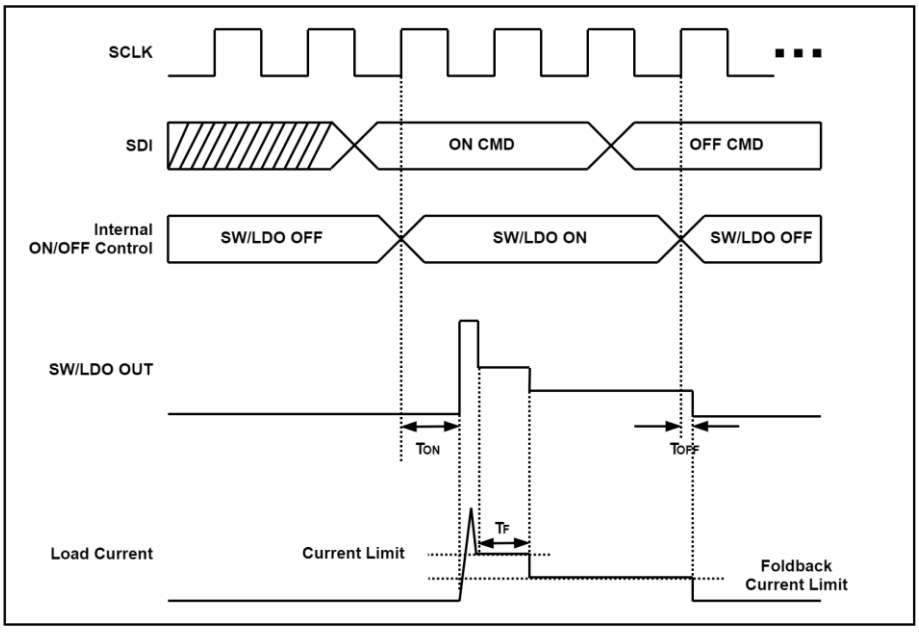


Figure 7. Current Limit Foldback Operating Timing Diagram.

Thermal Shutdown Operating Diagram

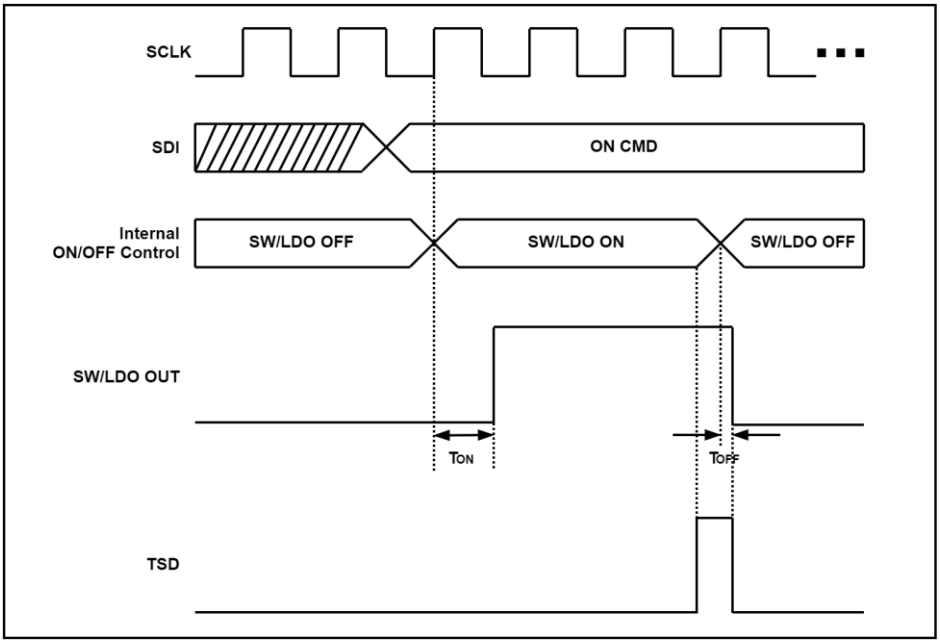


Figure 8. Thermal Shutdown Operating Diagram.

TEST CIRCUITS

TBD

TEST RESULTS

LDO 추가

TBD

On-resistance vs. Vain

TBD

ALL ON Leakage vs. Vain

TBD

ALL OFF Leakage vs. Vain

TBD

Current limit vs. Vain

TBD

Current limit vs. Time

TBD

Fold-back Current limit vs. Vain

TBD

Fold-back Current limit vs. Time

TBD

LDOOUT vs. Load Current

TBD

LDOOUT vs. Vain

LDO TABLE

Descriptions

- Selects LDO output Voltage. Minimum Voltage step is 10mV in case of voltage range 0.35V ~ 3.5V

CODE	V_{LDOOUT}	CODE	V_{LDOOUT}	CODE	V_{LDOOUT}	CODE	V_{LDOOUT}
0d035	0.35V	0d078	0.78V	0d121	1.21V	0d164	1.64V
0d036	0.36V	0d079	0.79V	0d122	1.22V	0d165	1.65V
0d037	0.37V	0d080	0.80V	0d123	1.23V	0d166	1.66V
0d038	0.38V	0d081	0.81V	0d124	1.24V	0d167	1.67V
0d039	0.39V	0d082	0.82V	0d125	1.25V	0d168	1.68V
0d040	0.40V	0d083	0.83V	0d126	1.26V	0d169	1.69V
0d041	0.41V	0d084	0.84V	0d127	1.27V	0d170	1.70V
0d042	0.42V	0d085	0.85V	0d128	1.28V	0d171	1.71V
0d043	0.43V	0d086	0.86V	0d129	1.29V	0d172	1.72V
0d044	0.44V	0d087	0.87V	0d130	1.30V	0d173	1.73V
0d045	0.45V	0d088	0.88V	0d131	1.31V	0d174	1.74V
0d046	0.46V	0d089	0.89V	0d132	1.32V	0d175	1.75V
0d047	0.47V	0d090	0.90V	0d133	1.33V	0d176	1.76V
0d048	0.48V	0d091	0.91V	0d134	1.34V	0d177	1.77V
0d049	0.49V	0d092	0.92V	0d135	1.35V	0d178	1.78V
0d050	0.50V	0d093	0.93V	0d136	1.36V	0d179	1.79V
0d051	0.51V	0d094	0.94V	0d137	1.37V	0d180	1.80V
0d052	0.52V	0d095	0.95V	0d138	1.38V	0d181	1.81V
0d053	0.53V	0d096	0.96V	0d139	1.39V	0d182	1.82V
0d054	0.54V	0d097	0.97V	0d140	1.40V	0d183	1.83V
0d055	0.55V	0d098	0.98V	0d141	1.41V	0d184	1.84V
0d056	0.56V	0d099	0.99V	0d142	1.42V	0d185	1.85V
0d057	0.57V	0d100	1.00V	0d143	1.43V	0d186	1.86V
0d058	0.58V	0d101	1.01V	0d144	1.44V	0d187	1.87V
0d059	0.59V	0d102	1.02V	0d145	1.45V	0d188	1.88V
0d060	0.60V	0d103	1.03V	0d146	1.46V	0d189	1.89V
0d061	0.61V	0d104	1.04V	0d147	1.47V	0d190	1.90V
0d062	0.62V	0d105	1.05V	0d148	1.48V	0d191	1.91V
0d063	0.63V	0d106	1.06V	0d149	1.49V	0d192	1.92V
0d064	0.64V	0d107	1.07V	0d150	1.50V	0d193	1.93V
0d065	0.65V	0d108	1.08V	0d151	1.51V	0d194	1.94V
0d066	0.66V	0d109	1.09V	0d152	1.52V	0d195	1.95V
0d067	0.67V	0d110	1.10V	0d153	1.53V	0d196	1.96V
0d068	0.68V	0d111	1.11V	0d154	1.54V	0d197	1.97V
0d069	0.69V	0d112	1.12V	0d155	1.55V	0d198	1.98V
0d070	0.70V	0d113	1.13V	0d156	1.56V	0d199	1.99V
0d071	0.71V	0d114	1.14V	0d157	1.57V	0d200	2.00V
0d072	0.72V	0d115	1.15V	0d158	1.58V	0d201	2.01V
0d073	0.73V	0d116	1.16V	0d159	1.59V	0d202	2.02V
0d074	0.74V	0d117	1.17V	0d160	1.60V	0d203	2.03V
0d075	0.75V	0d118	1.18V	0d161	1.61V	0d204	2.04V
0d076	0.76V	0d119	1.19V	0d162	1.62V	0d205	2.05V
0d077	0.77V	0d120	1.20V	0d163	1.63V	0d206	2.06V

CODE	V_{LDOOUT}	CODE	V_{LDOOUT}	CODE	V_{LDOOUT}	CODE	V_{LDOOUT}
0d207	2.07V	0d250	2.50V	0d293	2.93V	0d336	3.36V
0d208	2.08V	0d251	2.51V	0d294	2.94V	0d337	3.37V
0d209	2.09V	0d252	2.52V	0d295	2.95V	0d338	3.38V
0d210	2.10V	0d253	2.53V	0d296	2.96V	0d339	3.39V
0d211	2.11V	0d254	2.54V	0d297	2.97V	0d340	3.40V
0d212	2.12V	0d255	2.55V	0d298	2.98V	0d341	3.41V
0d213	2.13V	0d256	2.56V	0d299	2.99V	0d342	3.42V
0d214	2.14V	0d257	2.57V	0d300	3.00V	0d343	3.43V
0d215	2.15V	0d258	2.58V	0d301	3.01V	0d344	3.44V
0d216	2.16V	0d259	2.59V	0d302	3.02V	0d345	3.45V
0d217	2.17V	0d260	2.60V	0d303	3.03V	0d346	3.46V
0d218	2.18V	0d261	2.61V	0d304	3.04V	0d347	3.47V
0d219	2.19V	0d262	2.62V	0d305	3.05V	0d348	3.48V
0d220	2.20V	0d263	2.63V	0d306	3.06V	0d349	3.49V
0d221	2.21V	0d264	2.64V	0d307	3.07V	0d350	3.50V
0d222	2.22V	0d265	2.65V	0d308	3.08V		
0d223	2.23V	0d266	2.66V	0d309	3.09V		
0d224	2.24V	0d267	2.67V	0d310	3.10V		
0d225	2.25V	0d268	2.68V	0d311	3.11V		
0d226	2.26V	0d269	2.69V	0d312	3.12V		
0d227	2.27V	0d270	2.70V	0d313	3.13V		
0d228	2.28V	0d271	2.71V	0d314	3.14V		
0d229	2.29V	0d272	2.72V	0d315	3.15V		
0d230	2.30V	0d273	2.73V	0d316	3.16V		
0d231	2.31V	0d274	2.74V	0d317	3.17V		
0d232	2.32V	0d275	2.75V	0d318	3.18V		
0d233	2.33V	0d276	2.76V	0d319	3.19V		
0d234	2.34V	0d277	2.77V	0d320	3.20V		
0d235	2.35V	0d278	2.78V	0d321	3.21V		
0d236	2.36V	0d279	2.79V	0d322	3.22V		
0d237	2.37V	0d280	2.80V	0d323	3.23V		
0d238	2.38V	0d281	2.81V	0d324	3.24V		
0d239	2.39V	0d282	2.82V	0d325	3.25V		
0d240	2.40V	0d283	2.83V	0d326	3.26V		
0d241	2.41V	0d284	2.84V	0d327	3.27V		
0d242	2.42V	0d285	2.85V	0d328	3.28V		
0d243	2.43V	0d286	2.86V	0d329	3.29V		
0d244	2.44V	0d287	2.87V	0d330	3.30V		
0d245	2.45V	0d288	2.88V	0d331	3.31V		
0d246	2.46V	0d289	2.89V	0d332	3.32V		
0d247	2.47V	0d290	2.90V	0d333	3.33V		
0d248	2.48V	0d291	2.91V	0d334	3.34V		
0d249	2.49V	0d292	2.92V	0d335	3.35V		

FUNCTIONAL DESCRIPTION

- ***Internal Structure***

The SP2003 consists of 2Channel CMOS Analog Switch and 4Channel LDO.

The SP2003 Command structure consists of two types: Initial Command and Control Command.

The Initial Command must be used during the Power-Up sequence.
The Initial Command has a 2-Type data frame, 1st Command for used Chip ID Set. 2nd Command for used temperature Select.

- ***SPI Interface***

The SP2003 uses the serial peripheral interface and consists of four pins: SCLK, SDI, SDO, and CSN.
The structure without Internal/External clocks operates the system using SCLK and Internal OSC CLOCK.

The SP2003 Max operating Speed at 25Mhz. Network configuration is connected by broadcasting method and up to 16 ICs can be connected.

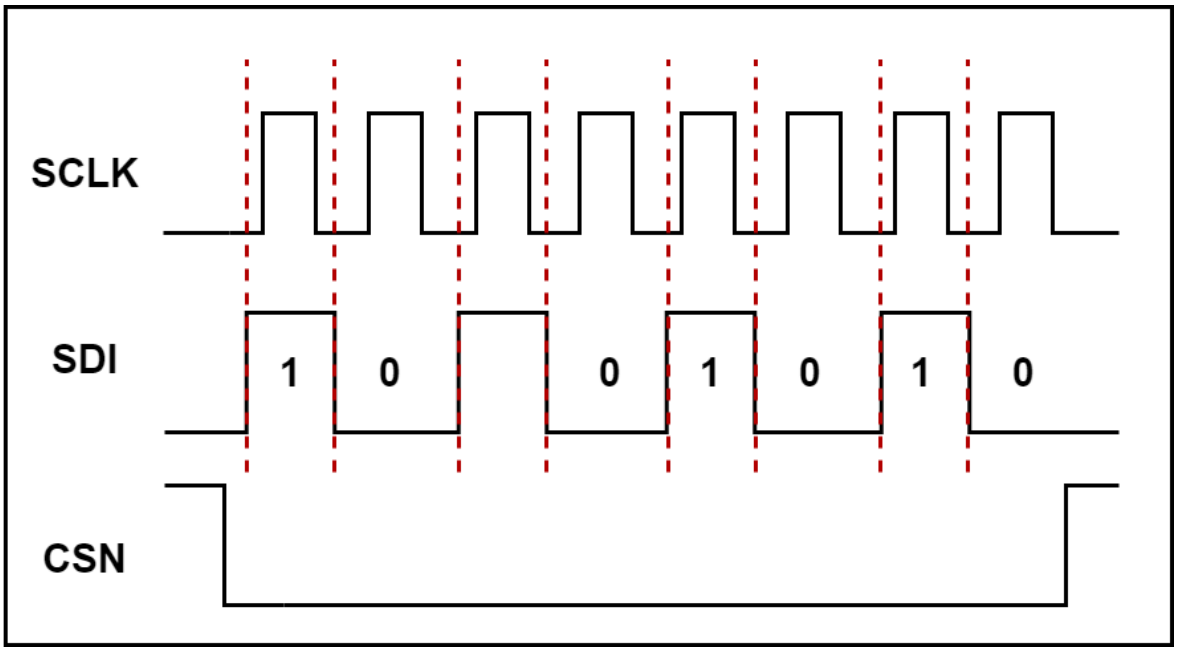


Figure 8. Example for SPI Interface (1Byte) Timing Diagram.

- ***SPI Daisy Chain Pin Sharing***

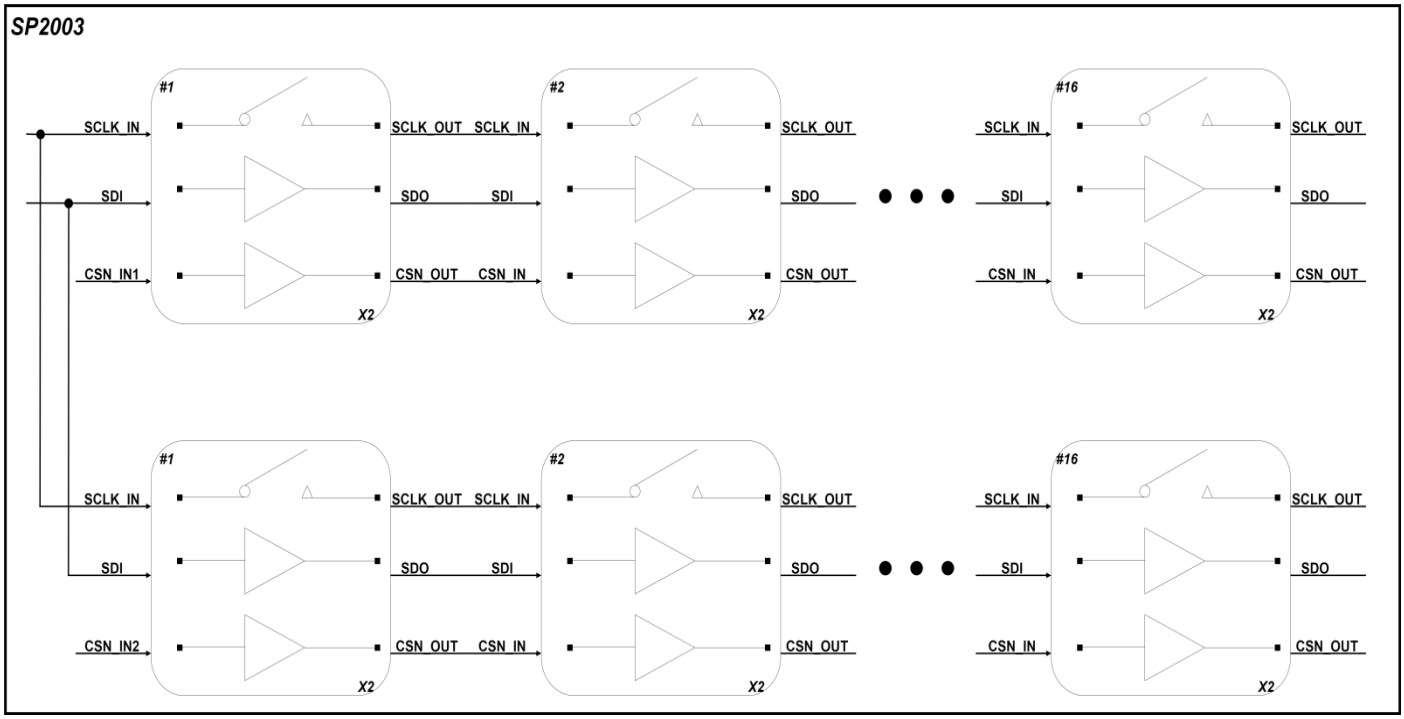


Figure 8. Example for SPI Interface (1Byte) Timing Diagram.

The SP2003 has 2 AIN, Switch, 4 LDO out Pin, and has Analog/Digital input voltage and ground as a pair. It also has a total of 24 pins including SCLK_IN, SCLK_OUT, SDI, CSN_IN, CSN_OUT, SDO, and VPP0,1 for SP2003 control.

- ***SP2003 Initial CMD***

The SP2003 has 2-Type Initial CMD. In Sp2003, after the Power-UP Sequence(after System Reset), the ID of the IC must be set using initial CMD, and the Temperature Type must be determined.(Default High Temp Select).

- ***Initial Chip ID Set***

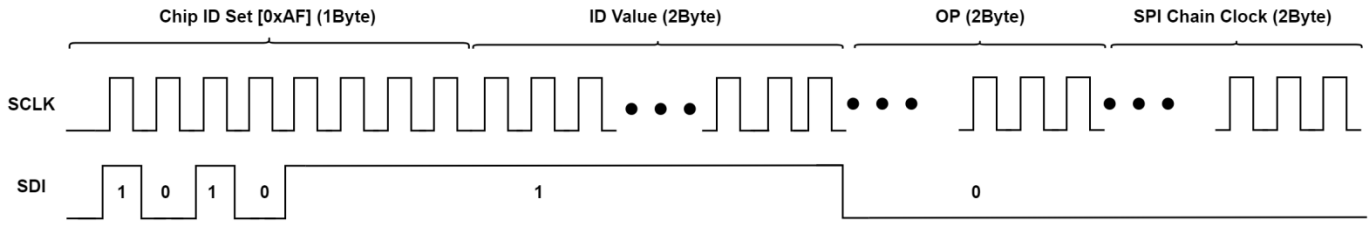


Figure 9. Example for SP2003 Chip Assign CMD Timing Diagram.

As SP2003 has an SPI Daisy Chain structure, IDs must be set as many as the ICs connected to the chain (Max 16ea).

When master (FPGA) transmits [0xAF], [0xFF], [0xFF], [0x00], [0x00], [0x00], [0x00] data through SPI Interface, the ID of SP2003 connected to the chain is set.

- ***Initial Temperature Type Select.***

The SP2003 can select the Temperature Type according to the usage environment.

By default, High Temp is selected, and you can select and use Low Temp according to the usage environment.

If data of [0xAE], [0x1B], [0x00], [0x00], [0x00], [0x00] is transmitted from Master (FPGA) through SPI Interface, it is possible to change from High Temp to Low Temp.

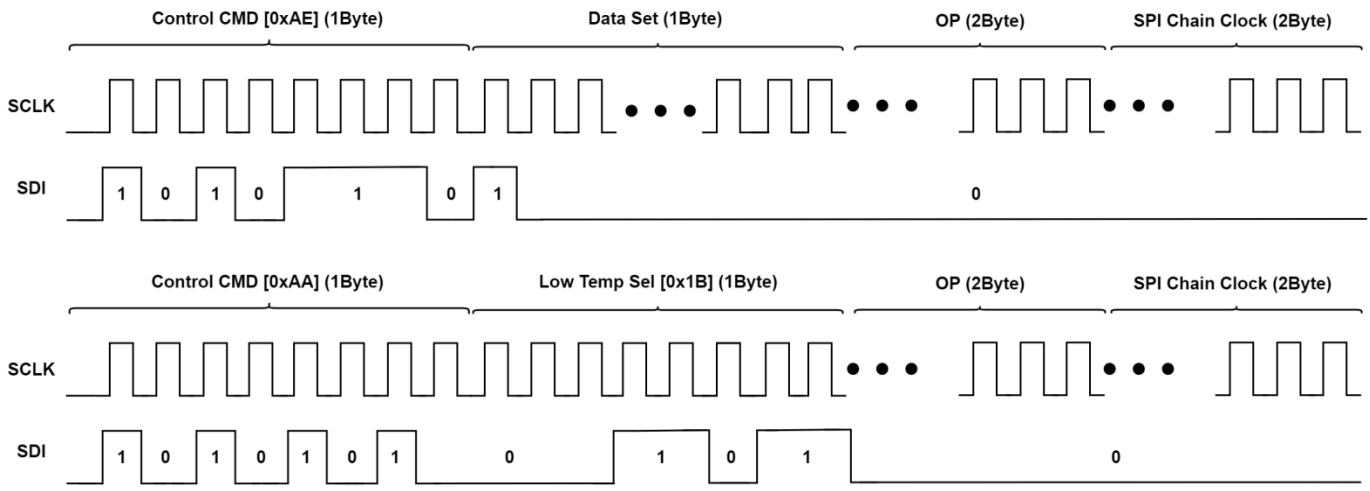


Figure 10. Example for SP2003 Low Temp Select Timing Diagram.

To change from Low Temp state to High Temp, if data of [0xAE], [0x1C], [0x00], [0x00], [0x00], [0x00] is transmitted from Master(FPGA) through SPI Interface, or System Reset.

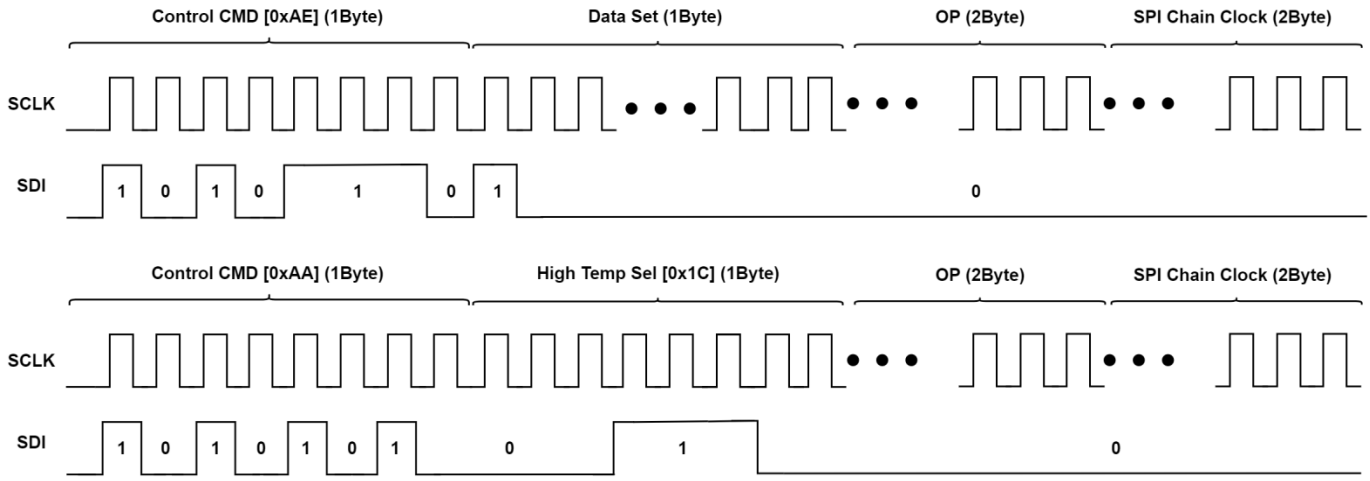


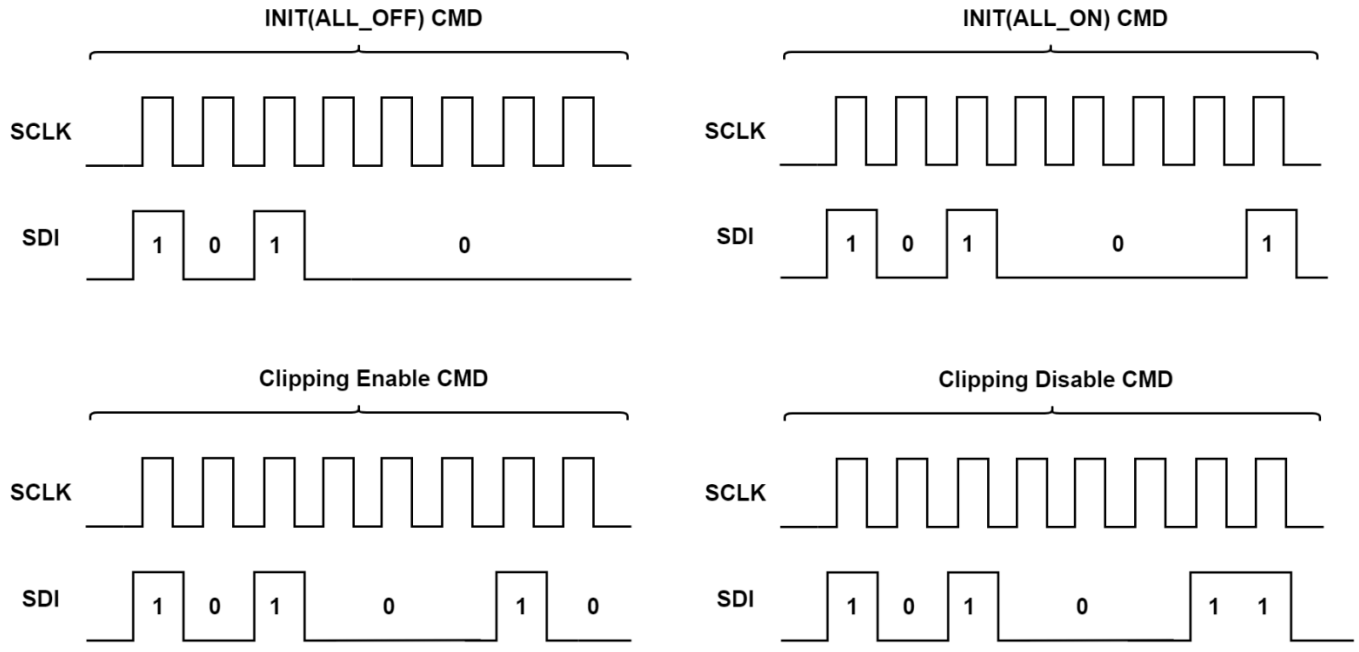
Figure 11. Example for SP2003 High Temp Select Timing Diagram.

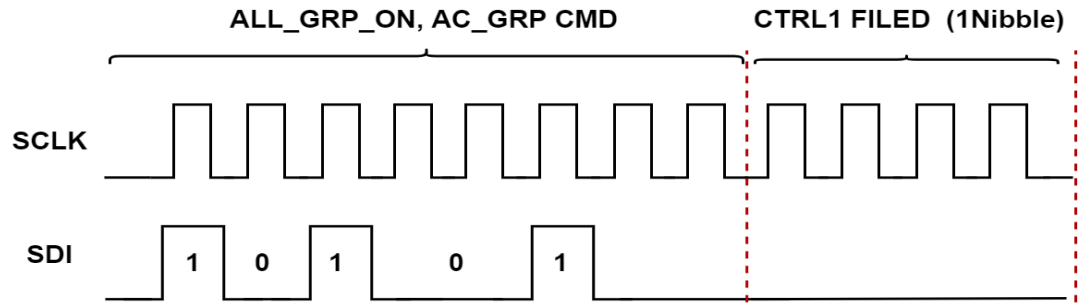
- ***Switch & LDO Control Command List***

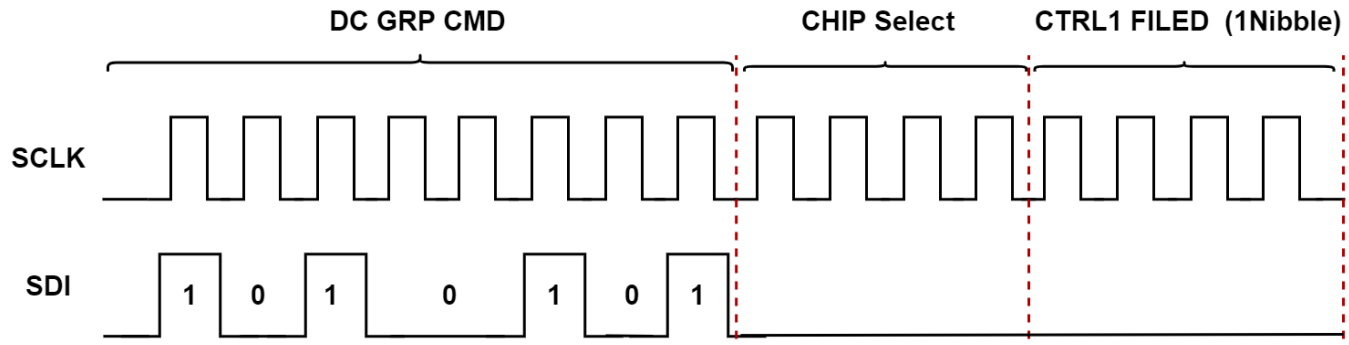
Name	CMD Value	Description
INIT(ALL OFF)	0x0	All Chip Switch, LDO Off, Reject Clear
INIT(ALL ON)	0x1	All Chip Switch, LDO On, Reject Clear
Clipping Enable	0x2	All Chip CLS Function Enable.
Clipping Disable	0x3	All Chip CLS Function Disable.
All GRP ON, AC GRP	0x4	All Chip SW, LDO Same Control.
DC GRP	0x5	The same control of SW and LDO of a specific chip.
ICC/ICCQ	0x6	The individually control SW0/1, LDO0/1/2/3 of a specific chip
ALL CMD 1D REJ	0x7	The reject control of SW0/1, LDO0/1/2/3 of a specific chip individually.
Half CMD	0x8	The same Control for SW0/1, LDO0/1/2/3 of the selected chip.
Data Set	0x9	All Chip LDO Level Set.

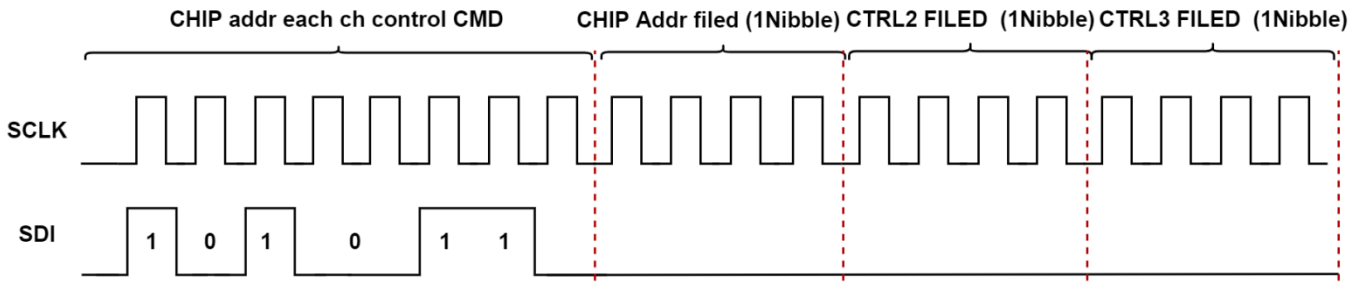
Name	Description			
	Bit[3]	Bit[2]	Bit[1]	Bit[0]
CTRL-1	-	Switch(0,1) ON / OFF	LDO(0,2) ON / OFF	LDO(1,3) ON / OFF
CTRL-2	-	Switch(0) ON / OFF	LDO(0) ON/OFF	LDO(1) ON / OFF
CTRL-3	-	Switch(1) ON / OFF	LDO(2) ON/OFF	LDO(3) ON / OFF
CTRL-4	1DUT / 2DUT Select	Switch(0,1) Reject	LDO(0,2) Reject	LDO(1,3) Reject

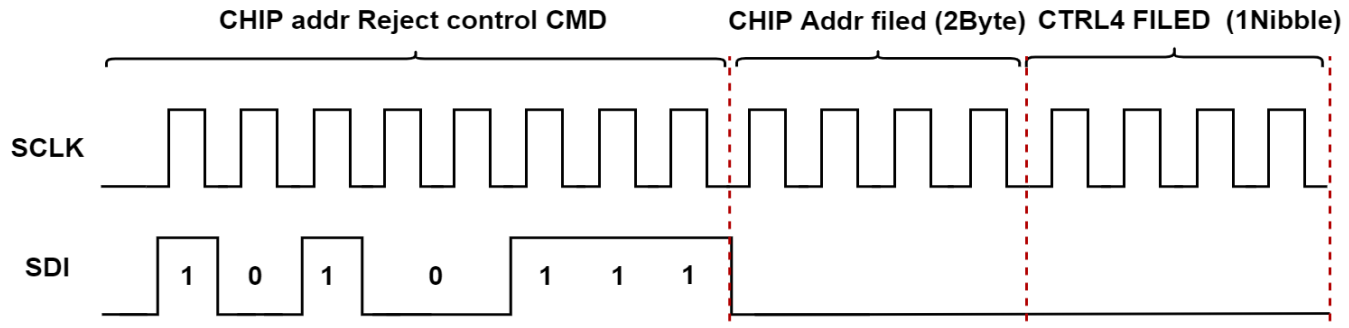
- ***Switch & LDO Control Command Overview***

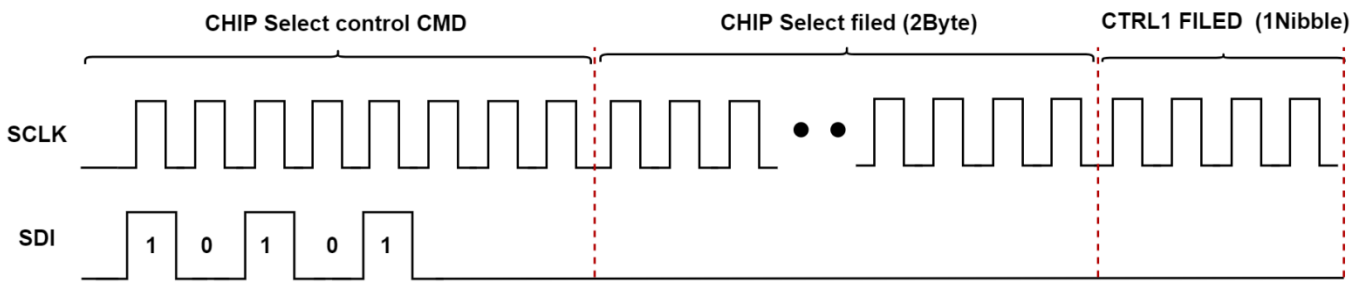



ALL_GRP_ON, AC_GRP CMD
CTRL1 FILED (1Nibble)
SCLK
SDI
1 0 1 0 1


DC GRP CMD
CHIP Select
CTRL1 FILED (1Nibble)
SCLK
SDI
1 0 1 0 1 0 1


CHIP addr each ch control CMD
CHIP Addr filed (1Nibble)
CTRL2 FILED (1Nibble)
CTRL3 FILED (1Nibble)
SCLK
SDI
1 0 1 0 1 1


CHIP addr Reject control CMD
CHIP Addr filed (2Byte)
CTRL4 FILED (1Nibble)
SCLK
SDI
1 0 1 0 1 1 1


CHIP Select control CMD
CHIP Select filed (2Byte)
CTRL1 FILED (1Nibble)
SCLK
SDI
1 0 1 0 1

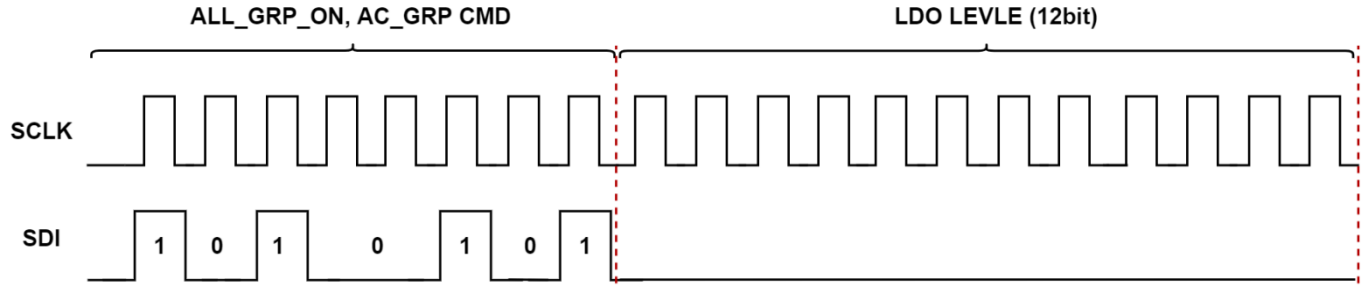


Figure 12. SP2003 Command Timing Diagram.

- ***INIT(ALL_OFF) CMD Example***

INIT(ALL_OFF) CMD turns OFF all switches / LDOs of all SP2003 ICs connected in the SPI Chain. Also, it performs the operation to remove the set REJECT FLAG.

When Master (FPGA) transmits [0xA0], [0x00], [0x00], [0x00], [0x00], all switches / LDOs are OFF.

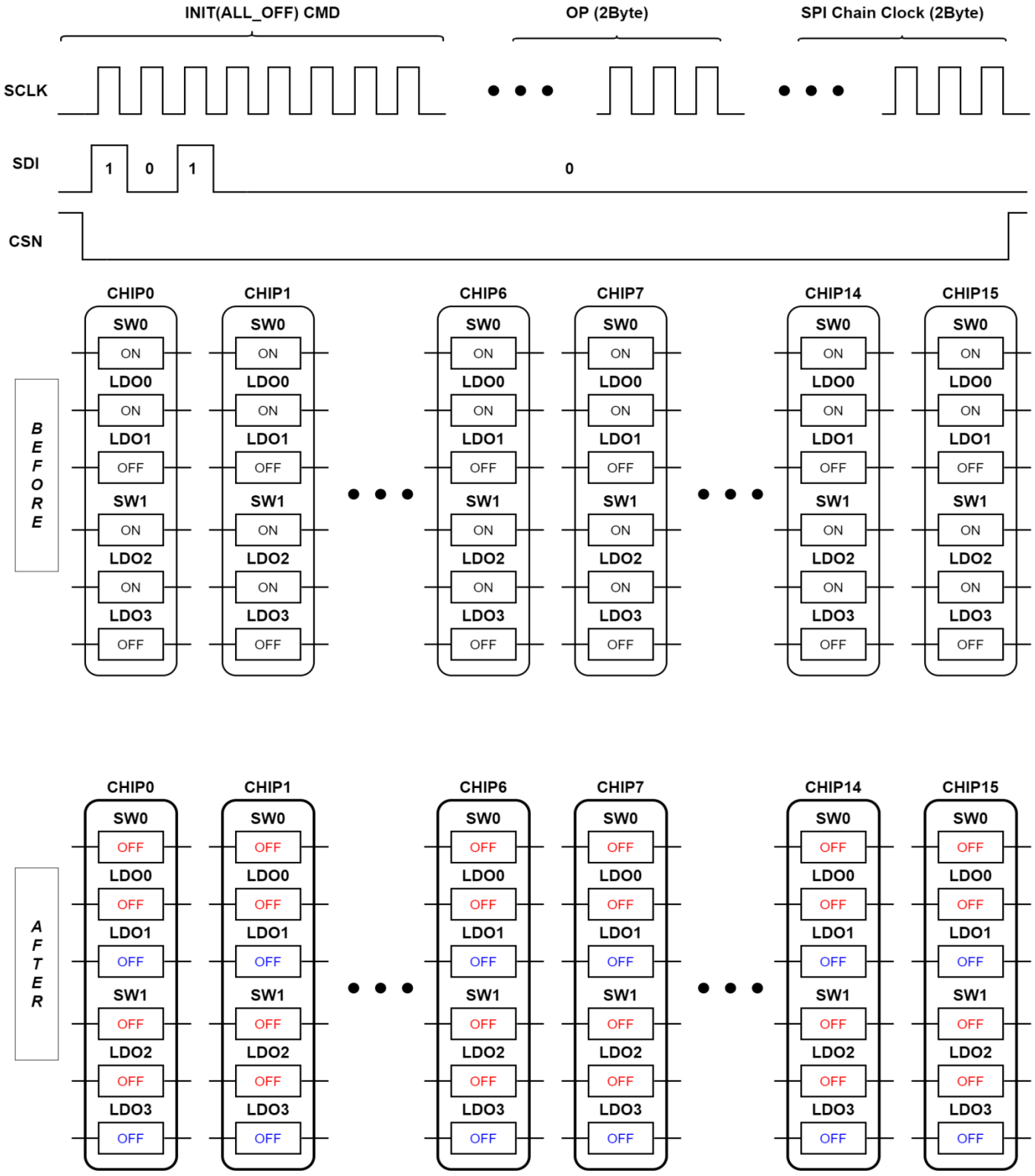


Figure 13. Example for INIT(ALL_OFF) Timing Diagram.

- ***INIT(ALL_ON) CMD***

INIT(ALL_ON) CMD turns ON all switches / LDOs of all SP2003 ICs connected in the SPI Chain. Also, it performs the operation to remove the set REJECT FLAG.

When Master (FPGA) transmits [0xA1], [0x00], [0x00], [0x00], [0x00], all switches / LDOs are ON.

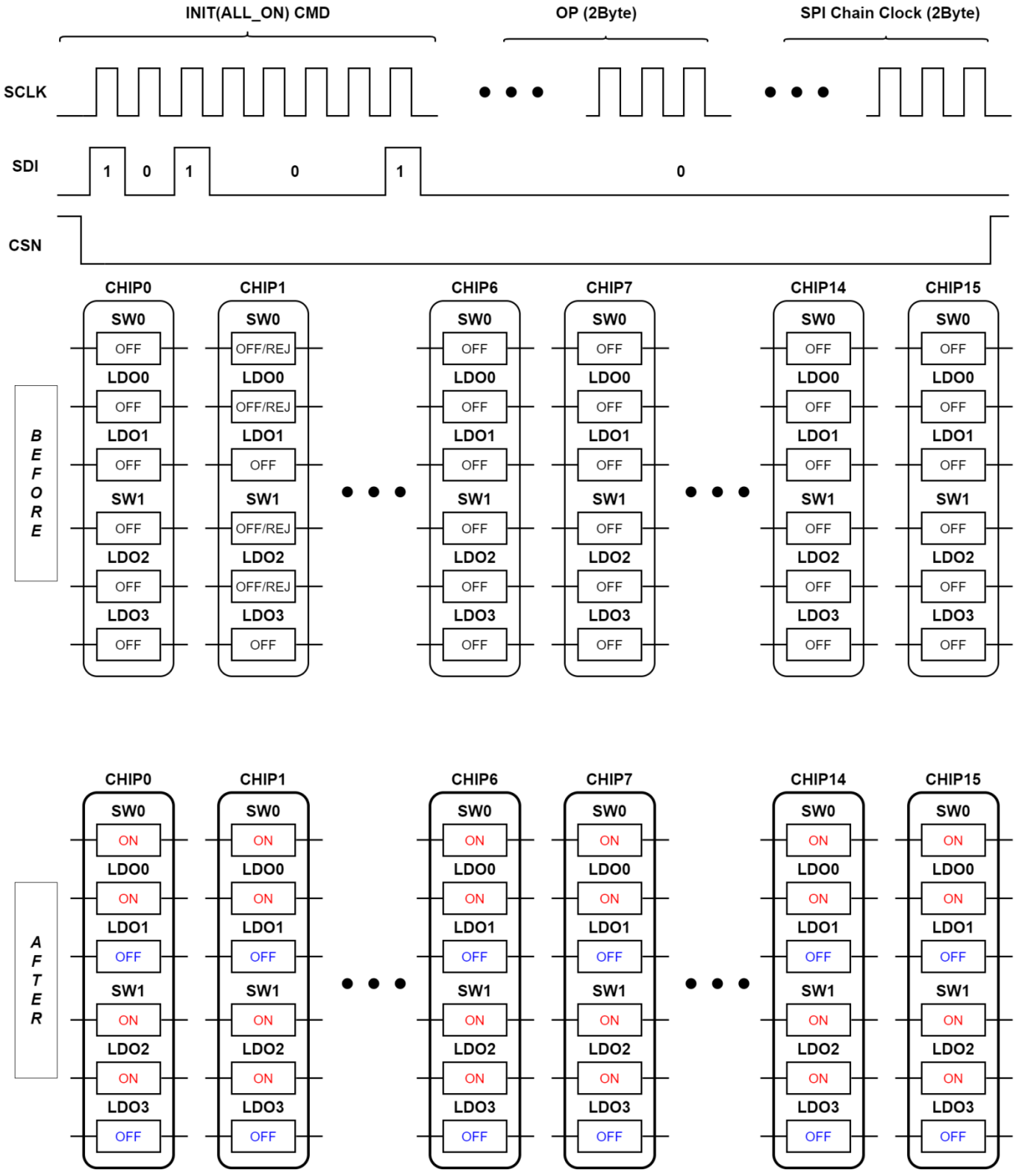


Figure 14. Example for INIT(ALL_ON) Timing Diagram.

- ***Clipping Circuit Enable(CLS_ON) CMD***

The Clipping Circuit Enable (CLS_ON) CMD is enables (ON) the CLS (Current Limiting) function of all SP2003 ICs connected in the SPI Chain.

The operation of Switch / LDO of all Channels is not changed.

When Master (FPGA) transmits [0xA2],[0x00], [0x00], [0x00], [0x00], all SP2003 CLS Function are ON.

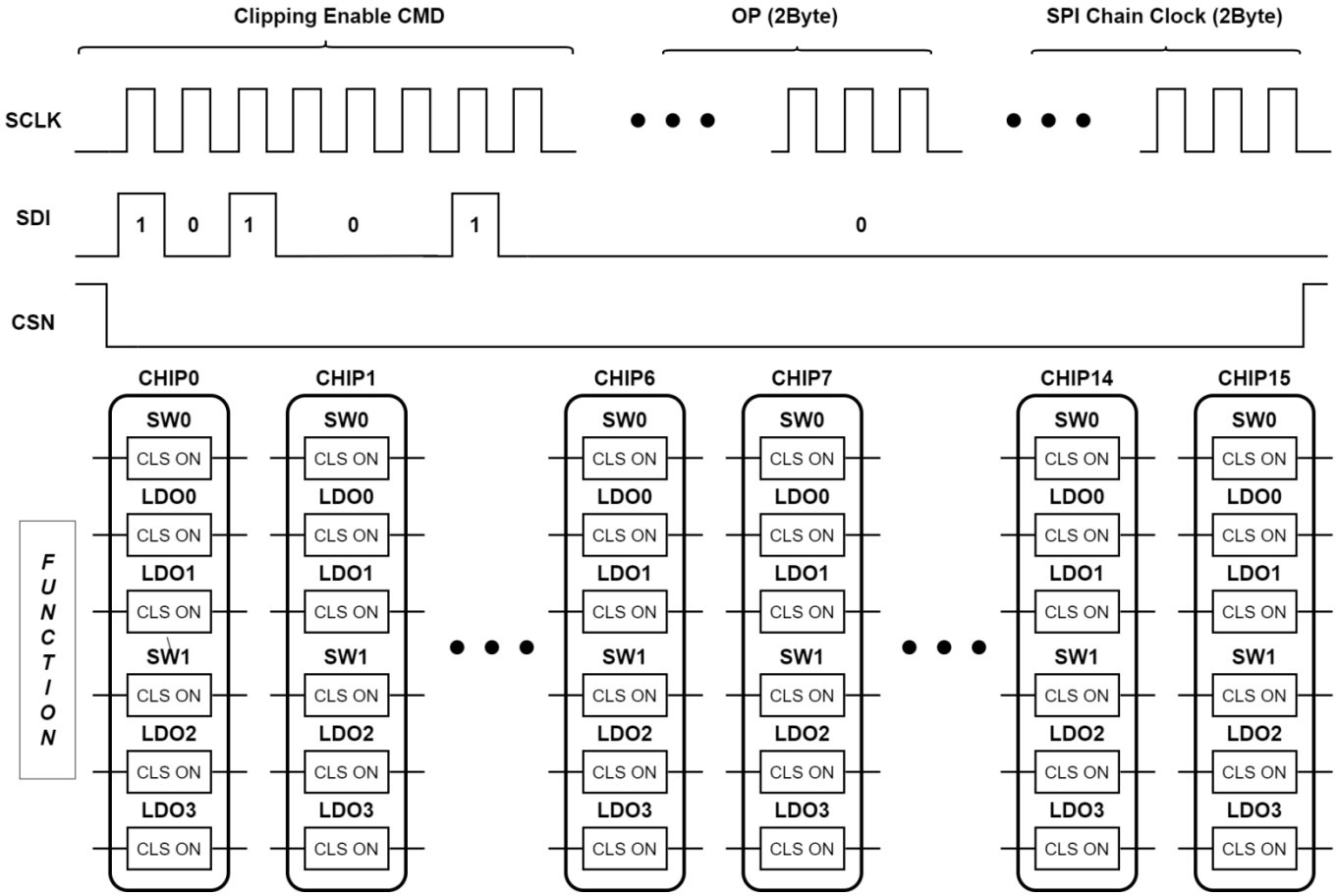


Figure 15. Example for Clipping Circuit(CLS_ON) Timing Diagram.

- ***Clipping Circuit Disable (CLS_OFF) CMD***

The Clipping Circuit Disable (CLS_OFF) CMD is disable (OFF) the CLS (Current Limiting) function of all SP2003 ICs connected in the SPI Chain.

The operation of Switch / LDO of all Channels is not changed.

When Master (FPGA) transmits [0xA3],[0x00], [0x00], [0x00], [0x00], all SP2003 CLS Function are OFF.

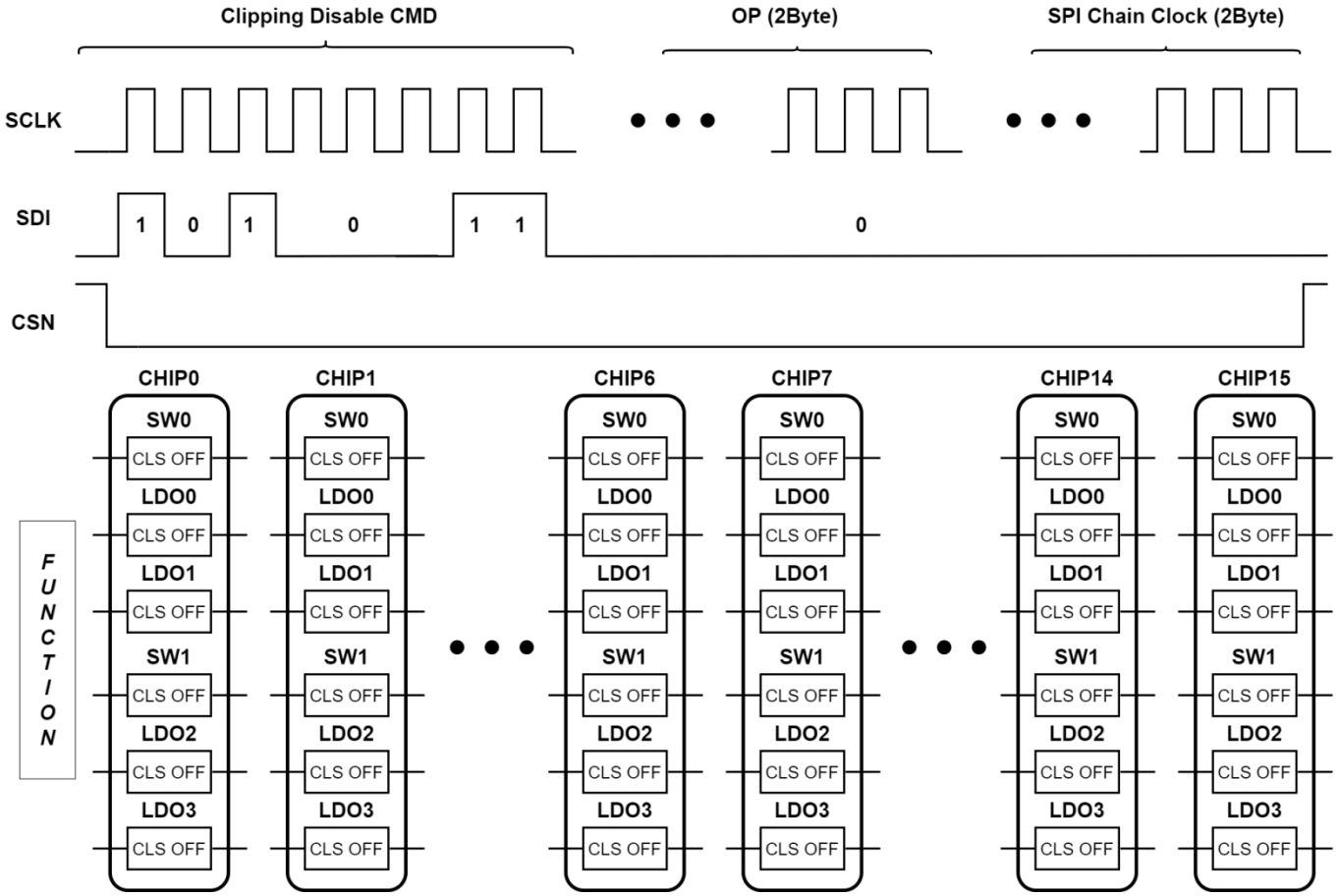


Figure 16. Example for Clipping Circuit(CLS_OFF) Timing Diagram.

- ***ALL / AC_GRP CMD***

The ALL_GRP / AC_GRP CMD control the switch and LDO operation of all ICs of SP2003 in the SPI Chain in the same way.

Depending on the CTRL-1 Filed, Switch 0/1, LDO0/2/, and LDO1/3 can be controlled respectively.

CTRL-1	Description
0x0	All Chips Switch0/1, LDO0/1/2/3 OFF.
0x1	All Chips Switch 0/1 and LDO0/2 OFF, LDO1/3 ON.
0x2	All Chips Switch 0/1 and LDO0/2 OFF, LDO1/3 ON.
0x3	All Chips Switch 0/1 OFF, LDO0/1/2/3 ON.
…	…
0x7	All Chips Switch 0/1 and LDO0/1/2/3 ON.

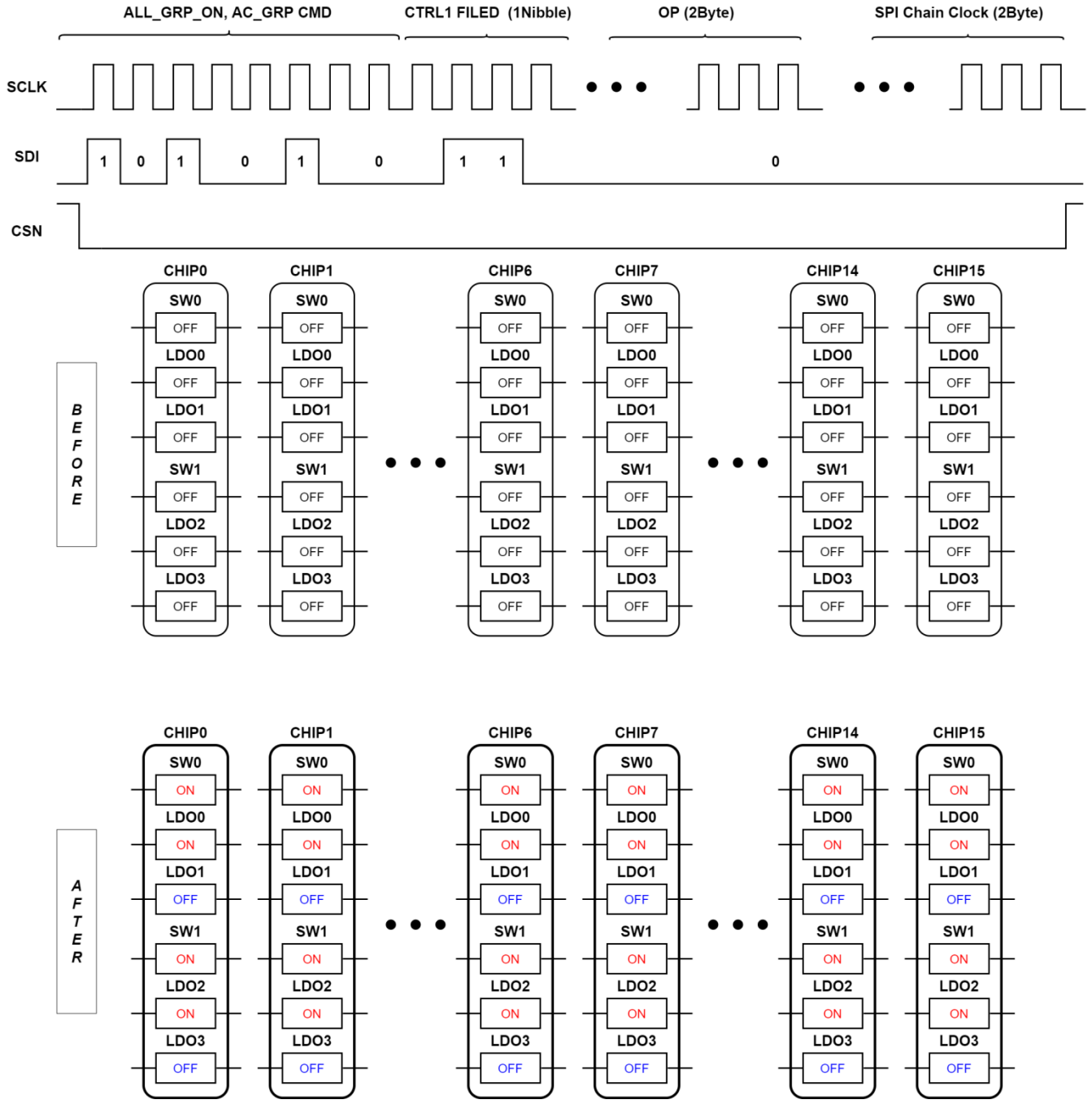


Figure 17. Example for All/ AC_GRP Command Timing Diagram.

- ***DC_GRP CMD***

The DC_GRP CMD controls the switch and LDO of the selected IC of SP2003 in the SPI Chain in the same way.

Depending on the CTRL-1 Filed, Switch 0/1, LDO0/2/, and LDO1/3 can be controlled respectively.

Chip Num	CTRL-1	Description
0x1	0x0	CHIP ID(1) Switch 0/1 and LDO0/1/2/3 is OFF.
	0x1	CHIP ID(1) Switch 0/1 and LDO0/2 is OFF, LDO1/3 is ON.
0x7	0x2	CHIP ID(7) Switch 0/1, and LDO1/3 is OFF, LDO0/2 is ON.
	0x3	CHIP ID(7) Switch 0/1 is OFF, LDO0/1/2/3 is ON.
…	…	…
0xF	0x7	CHIP ID(15) Switch 0/1 and LDO0/1/2/3 is ON
	0x6	CHIP ID(15) Switch 0/1 and LOD0/2 is ON, LDO1/3 is OFF
	0x5	CHIP ID(15) Switch 0/1 and LDO1/3 is ON, LDO0/2 is OFF
…	…	…
0x0	0x7	CHIP ID(0) Switch 0/1 and LDO0/1/2/3 is ON.

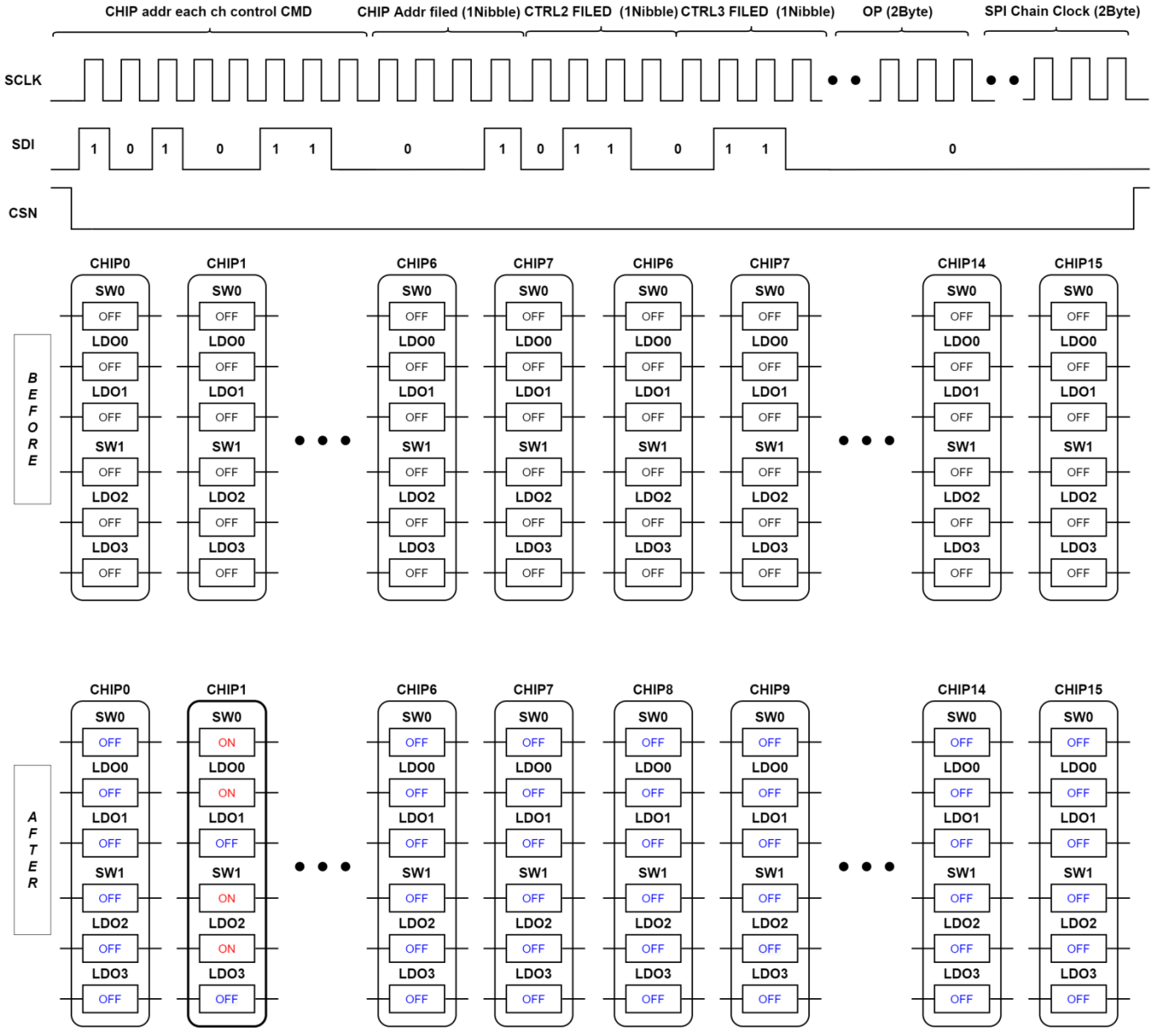


Figure 18. Example for DC_GRP Command Timing Diagram.

- ***ICC/ICCQ CMD***

The ICC / ICCQ CMD individually control Switch and LDO for the selected chip in the SPI Chain.

Depending on the CTRL-1 Filed, Switch 0/1, LDO0/2/, and LDO1/3 can be controlled respectively.

Chip Num	CTRL-2	CTRL-3	Description
0x1	0x7	0x0	Chip ID(1) DUT1(Switch0,LDO0/1) ON, DUT2(Switch1, LDO2/3) OFF.
	0x6	0x1	Chip ID(1) DUT1(Switch0 and LDO0 ON, LDO1 OFF), DUT2 (Switch1 and LDO2 OFF, LDO3 ON).
0x7	0x1	0x4	Chip ID(7) DUT1(Switch0 and LDO0 OFF, LDO1 ON), DUT2 (Switch1 ON LDO2/3 OFF).
	0x4	0x1	Chip ID(7) DUT1(Switch0 ON, LDO0/1 OFF), DUT2 (Switch1 and LDO2 ON, LDO3 OFF).
…	…	…	…
0x5	0x0	0x0	Chip ID(5) DUT1(Switch0and LDO0/1 OFF), DUT2 (Switch1 and LDO2/3 OFF).

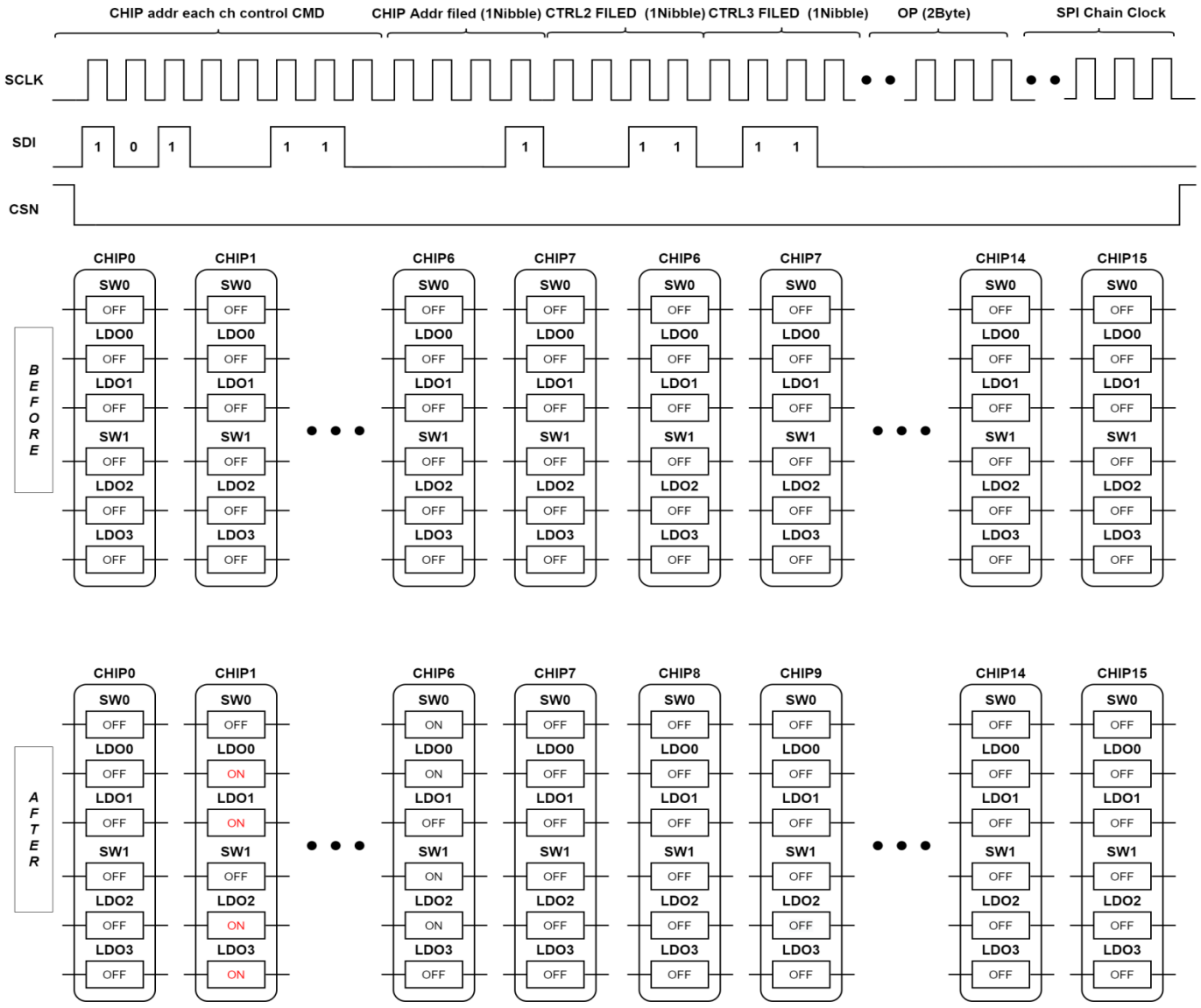


Figure 19. Example for ICC/ICCQ Command Timing Diagram.

- ***ALL / 1DUT REJ(CMD)***

The ALL / 1DUT_REJ CMD controls the same switch and LDO of the selected IC of SP2003 in the SPI Chain.

Depending on the CTRL-4 Filed, Switch 0/1, LDO0/2/, and LDO1/3 can be controlled respectively

Chip Num	CTRL-4	Description
0x1	0x7	Chip ID(1) Switch 0 and LDO0/1 Reject.
	0xE	Chip ID(1) Switch 1 and LDO2 Reject. LDO3 OFF.
0x7	0x6	Chip ID(7) Switch 0 and LDO0 Reject. LDO1 OFF.
	0x1	Chip ID(7) Switch 0 and LDO0 OFF, LDO1 Reject.
…	…	…
0x5	0x8	Chip ID(5) Switch 1 and LDO2/3 OFF.

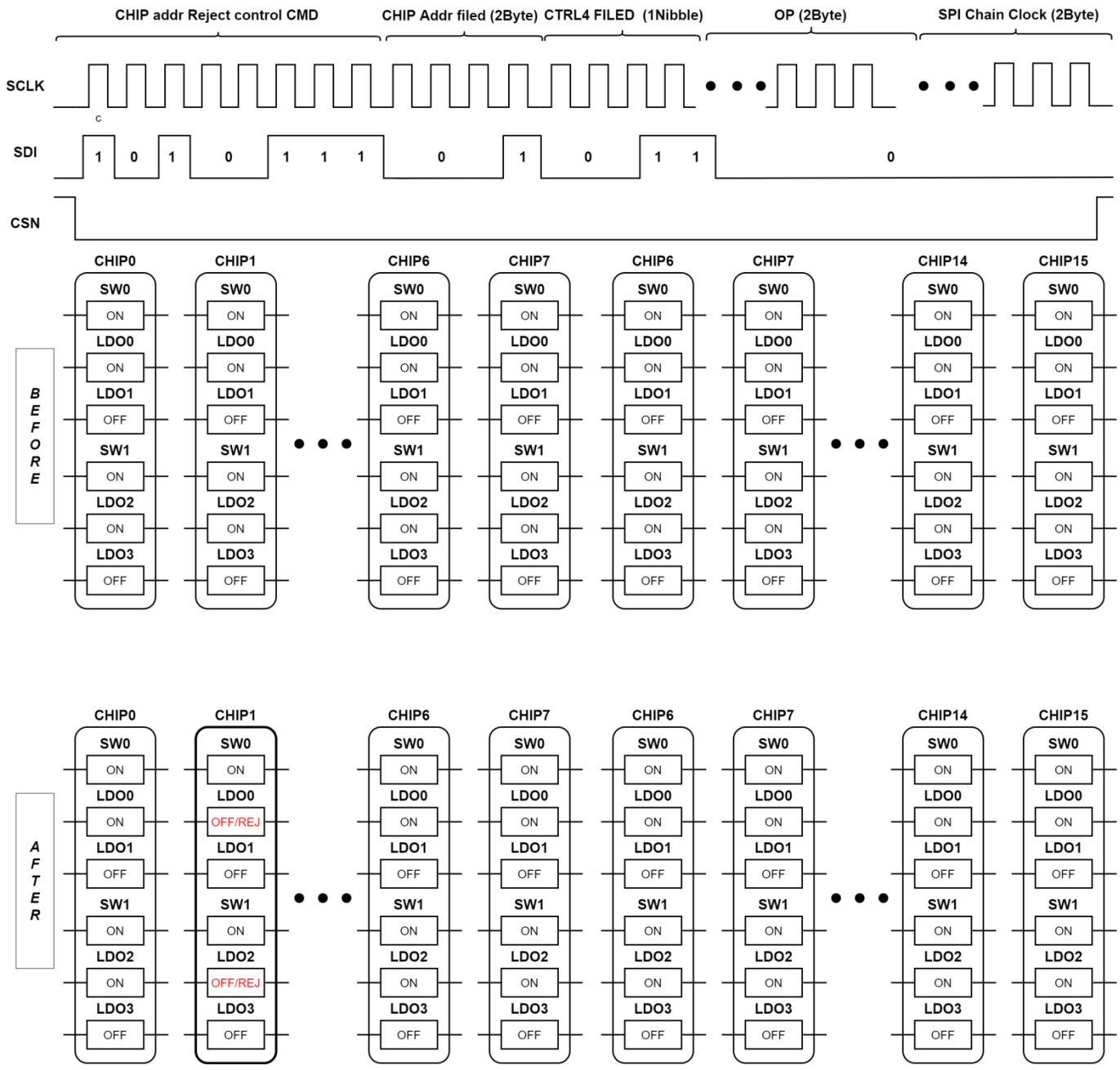


Figure 20. Example for ALL/1DUT REJ Command Timing Diagram.

- ***Half (Chip Select) CMD***

The Half (Chip Select) CMD controls Switch and LDO by selecting multiple ICs of SP2003 in SPI Chain.

Depending on the CTRL-1 Filed, Switch 0/1, LDO0/2/, and LDO1/3 can be controlled respectively.

Chip Num	CTRL-1	Description
0x001F	0x7	Chip ID (0),(1),(2),(3),(4) Switch0/1 and LDO0/1/2/3 is ON.
	0x6	Chip ID (0),(1),(2),(3),(4) Switch0/1 and LDO0/2 is ON. LDO1/3 is OFF.
0x03E0	0x6	Chip ID (5),(6),(7),(8),(9) Switch0/1 and LDO0/2 is ON. LDO1/3 is OFF.
	0x1	Chip ID (5),(6),(7),(8),(9) Switch0/1 and LDO0/2 is OFF. LDO1/3 is ON.
…	…	…
0x0333	0x6	Chip ID (0),(1), (4), (5), (8), (9) Switch 0/1 and LDO0/2 is ON, LDO1/3 is OFF.

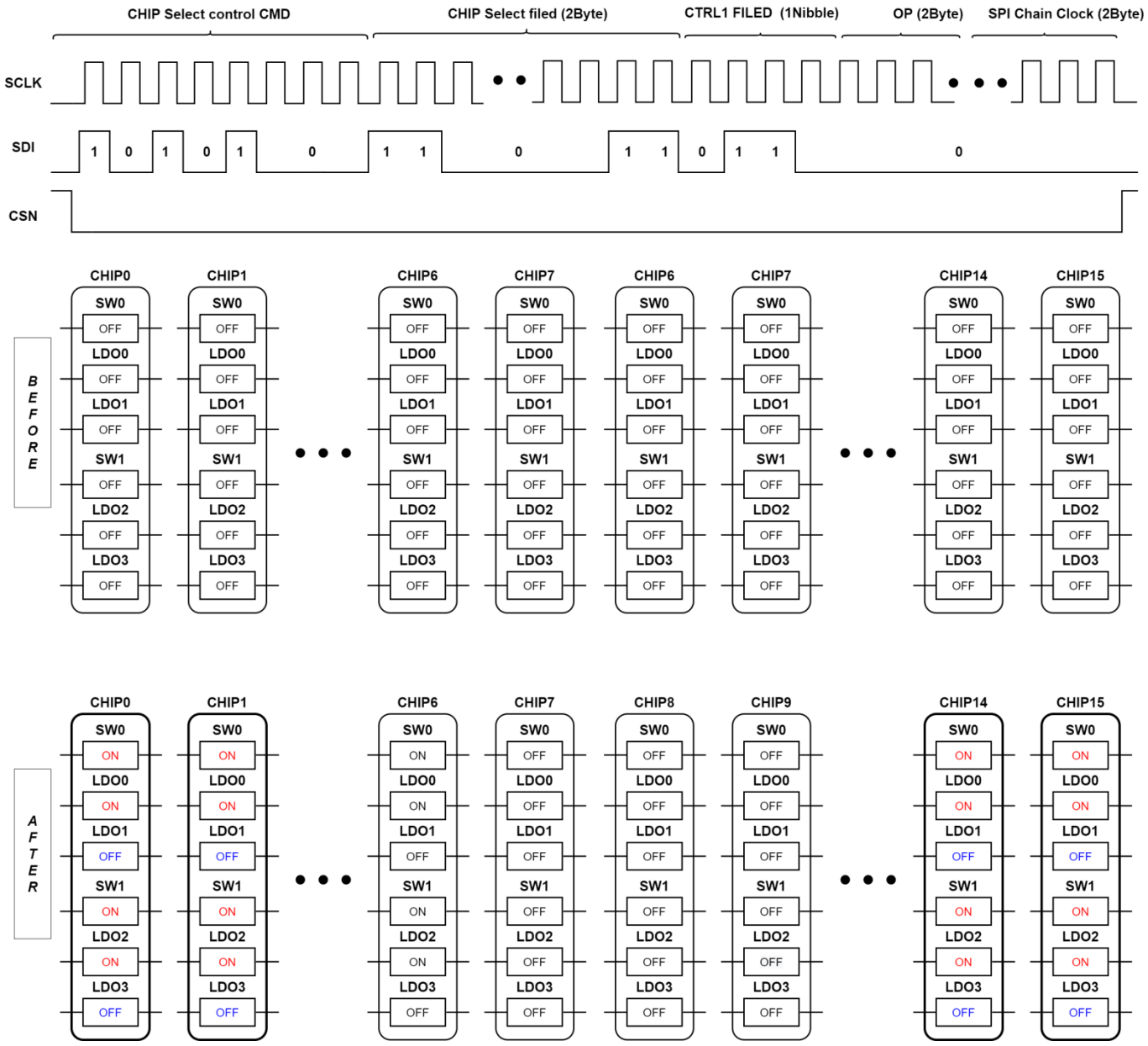


Figure 21. Example for Half (Chip Select) Command Timing Diagram.

- ***PMIC DATA SET (LDO LEVEL SET) CMD***

The PMIC DATA SET CMD sets the same LDO Level of all SP2003 in the SPI Chain.

When Master (FPGA) transmits data of [0xA9], [0x0B], [0x40], [0x00], [0x00], [0x00], [0x00], all LDOs of SP2003 connected to the chain have the same Level.

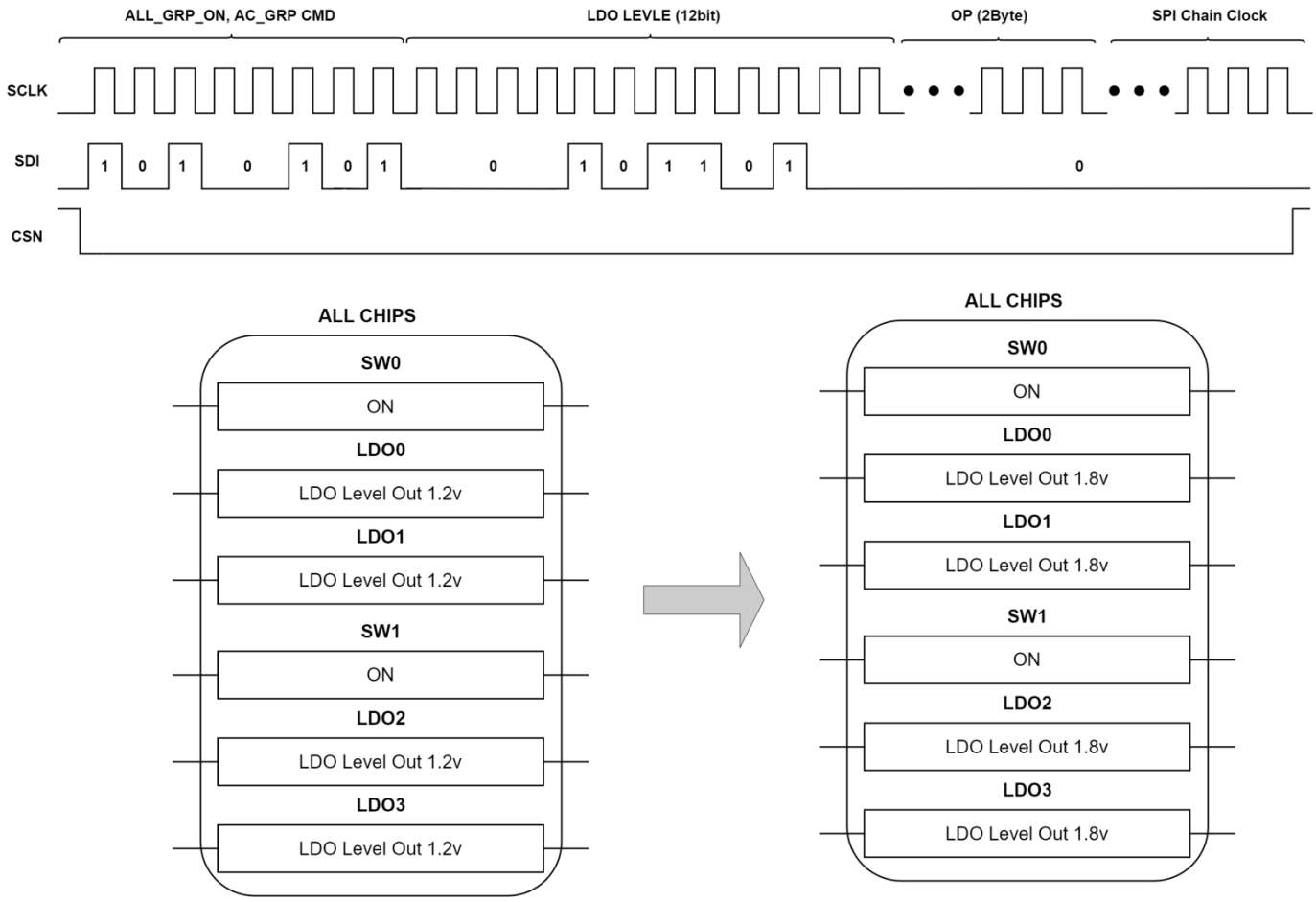


Figure 22. Example for PMIC DATA SET(LDO LEVEL SET) Command Timing Diagram.

- ***Current Limiting***

SP2003 supports Current Limiting to protect itself from excessive high current. If current more than the threshold flows through a switch, the switch automatically increases the turn-on resistance by an internal protection circuit.
The current limit is continuous type and is automatically released when the load current decreases.

- ***Fold-back Current Limiting***

SP2003 supports Current Limiting to protect itself from excessive high current. If current more than the threshold (Current Limit Level) flows through a switch, the switch automatically increases the turn-on resistance by an internal protection circuit.
When enable Fold-back function, the turn-on resistance increases reducing the current until Fold-back Current Limit Level. Due to this, the current limit value becomes smaller, which is advantageous for heat generation reduce heat to slow or reduce the probability of TSD operation

The current limit is continuous type and is automatically released when the load current decreases

- ***Thermal Shutdown***

SP2003 supports thermal shutdown to protect itself from excessive high temperature. If the temperature of a switch goes above the threshold (170°C), All channel automatically turn off by internal thermal shutdown circuit.
When Current Limit function operating, the thermal shutdown function automatically turn off only channel exceeding temperature 150°C. The threshold is set from internal Thermal Shutdown Circuit. Thermal Shutdown is the secondary protection scheme for the case that Current Limiting does not work for some reasons even though excessive high current flows. The channel turns on again after the device temperature drops by approximately 15°C.

- ***Active Discharge***

This device has an active discharge circuit. When the switch is turned off, this function is automatically activated and the out pin is shorted to GND with 1kΩ. When switched on, this function is automatically turned off.

- ***Reverse Current Blocking***

This device has built-in reverse current blocking circuit (RCB) to block reverse current from VOUT to VIN. When switch ON condition, it works if the VOUT voltage is higher than VIN.

PACKAGE INFORMATION

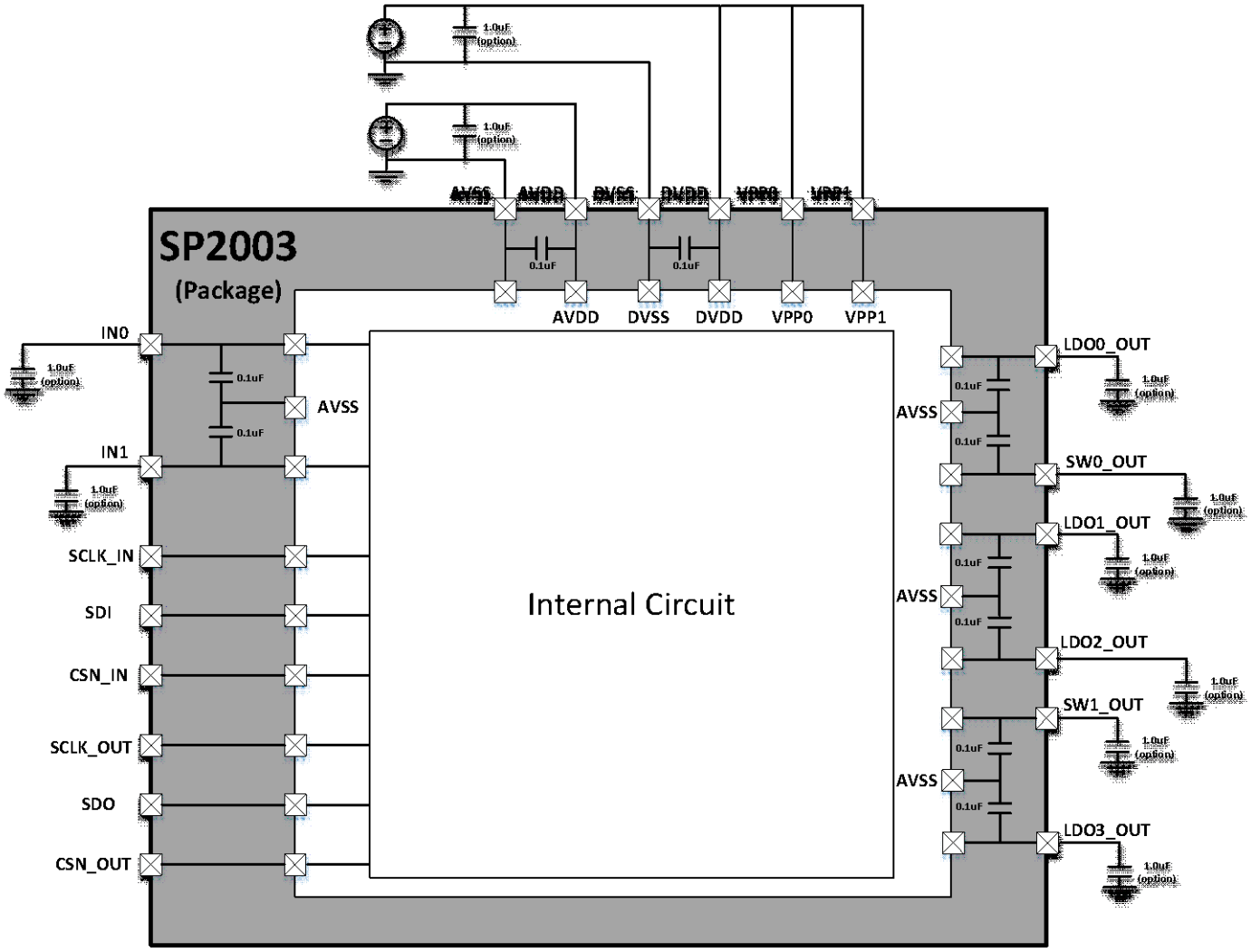
Figure 9. Package Information.

APPLICATION EXAMPLE

Table.XX is the command used in FPGA shows the command for the same operation when using SP2003.

ATE CMD	SP2003 CMD
INIT(ALL OFF)	1st : Send to “0xA9” CMD -> Default LDO Level Set. 2nd : Send to “0xA1”CMD -> Switch 0/1 ON , LDO 0/2 ON, LDO1/3 OFF. *Reject Flag Clear.
INIT(ALL ON)	1st : Send to “0xA9” CMD -> Default LDO Level Set. 2nd : Send to “0xA0”CMD -> All Channel OFF(Switch 0/1, LDO 01/2/3) *Reject Flag Clear.
Clipping Enable	Send To “0xA3” -> All Chips CLS Function Enable.
Clipping Disable	Send To “0xA2” -> All Chips CLS Function Disable.
All GRP ON,	1st : Send to “0xA9” CMD -> Default LDO Level Set. 2nd : Send to “0xA0”CMD -> All Channel OFF(Switch 0/1, LDO 01/2/3)
AC GRP	1st : Send to “0xA9” CMD -> LDO Level Set. 2nd : Send to “0xA4”CMD -> All Chip Sw0/SW1/LDO0/LDO2 ON, LDO1/LDO3 OFF
DC GRP	Send to “0xA5” -> Select Chip SW0/1, LDO0/2 ON, Etc All Chips All Channels OFF. OR Send to “0xA8” -> Select Chip SW0/1, LDO0/2 ON, Etc All Chips All Channels OFF.
ICC/ICCQ	Send to “0xA6” -> Select Chip Switch, LDO ON/OFF Control.
ALL CMD 1D REJ	Send to “0xA7”-> Select 1 DUT All Channel Reject.
1D RJT(PWR ON)	1st : Send to “0xA7” CMD -> Select DUT LDO1 or LDO3 Reject, 2nd : Send to “0xA4”CMD -> SW0/LDO0/SW1/LDO2 ON, LDO1/LDO3 OFF.
Incoming Bypass Grp	Send to “0xA5” -> Select Chip SW0/1 ON, LDO All Channel OFF. Non Select Chips All Channels OFF.
Incoming LDO Grp	Send to “0xA5” -> Select Chip LDO0/2 ON, SW0/1, LDO1/3 Channel OFF. Non Select Chips All Channels OFF.

The figure below shows the recommended configuration.



1. 0.1uF decoupling capacitors connected to between AVDD and AVSS, and the same capacitors to between DVDD and DVSS in Package.
2. IN pins or OUT pins capacitors connected to OUT and AVSS in Package.
3. If connecting capacitors at IN pins or OUT pins or AVDD or DVDD are optional. It should be placed as close to the chip as possible. If connecting capacitors at IN pins, output capacitors are optional.

REVISION HISTORY

Revision	Date	Description
0.0	2021-12	Initial draft

DOCUMENT INFORMATION

File name: SP2003 Datasheet
Product code: SP2003
Product description: Power Switch & LDO IC
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