STA-FX2 Datasheet

128-Channel CMOS Analog Switch IC

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Preliminary

The world is driven by analog

GENERAL DESCRIPTION

The STA IC is a monolithic CMOS device containing 128 independently-selectable switches. These switches are fabricated with an advanced submicron CMOS process that provides low power dissipation, low on resistance, low leakage currents, and high signal bandwidth. The STA IC is designed to operate in 3.3V for digital circuits and 5V for analog switches. Each switch can operate with a wide input and output voltage range. The off-leakage current is only 30nA at room temperature of 25°C.

All digital inputs have 0.8-V to 2.4-V input noise margin to ensure TTL/CMOS-logic compatibility when using a 3.3-V power supply.

FEATURE

3.3V logic-compatible input (V_{IH}=2.4V, V_{IL}=0.8V)
Dual supply operation: 3.3V for digital, 5V for analog.
Analog signal frequency: DC-to-1MHz
Low on-resistance: 1Ω (@typ)
Wide range analog input from 0V to 5V
Chip-ID programmable with OTP memory
Multi-channel switch control
Switching control using CMOS IF command
360-pin FBGA package

APPLICATIONS

Data-acquisition systems
Mechanical reed-relay replacement
Communication systems

FUNCTIONAL DIAGRAM

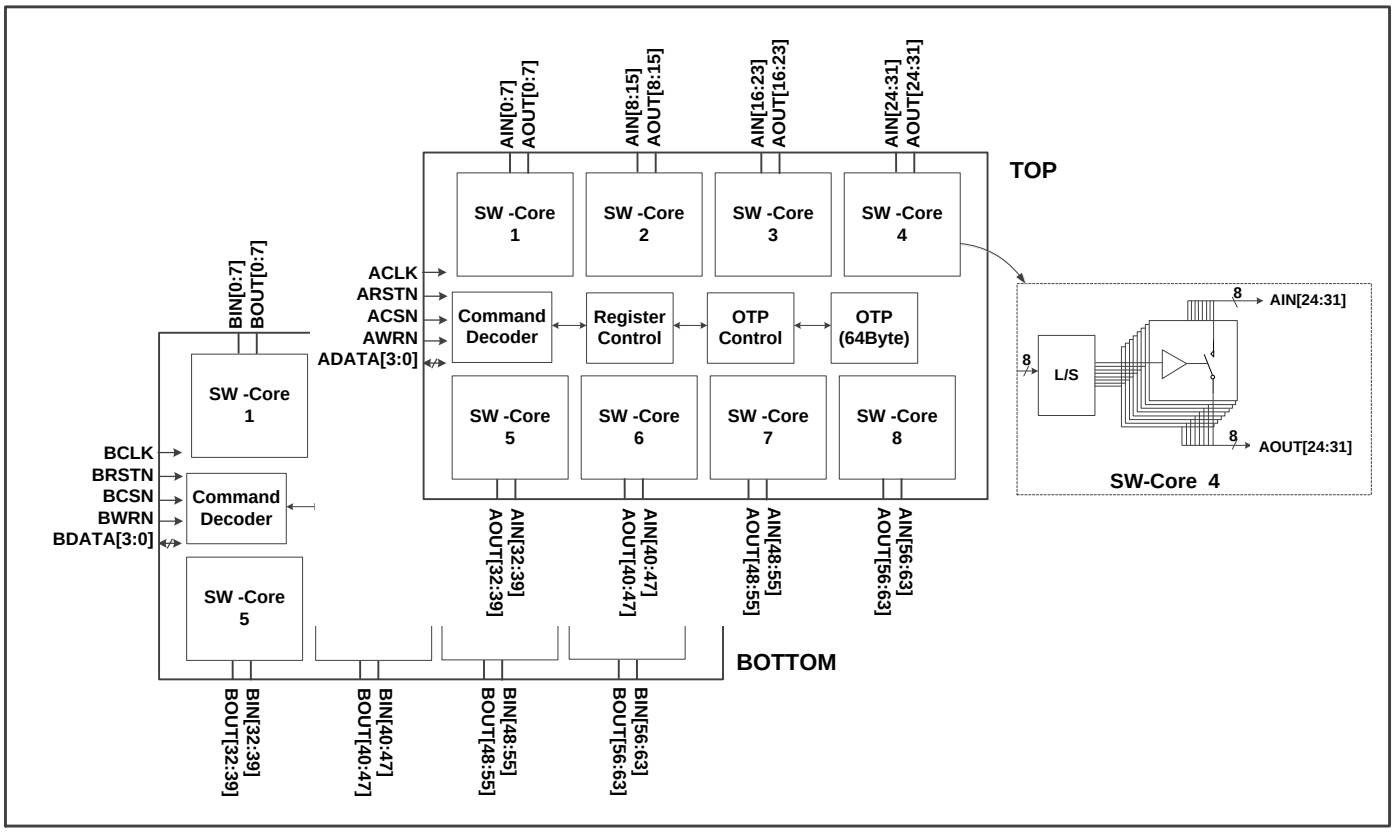


Figure 1. Functional Diagram

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND, Unless Otherwise Noted.)

AVDD (for Analog Switch).....-0.3V to +6V
DVDD (for Digital Control).....-0.3V to +4.5V
Voltage at any digital pin .....-0.3V to +4.5V
Voltage at any analog pin ……..…- 0.3V to +6V
Continuous current into any terminal 50mA
Peak current into analog switch I/O…….....100mA
(current pulse with 1ms and 10% duty cycle)

Operating temperature range .....-40°C to +85°C
Storage temperature range .....-65°C to +125°C
Junction temperature.....+150°C
ESD protection on all pins (HBM, MM)……≥2kV, 200V

Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at those or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

AVDD=5.0V, AVSS=0V, DVDD=3.3V, DVSS=0V and TA = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
POWER SUPPLIES						
Analog Supply Voltage	AVDD	AVSS=0V	4.5	5	5.5	V
		AVSS=-2.5V	2.0	2.5	3.0	V
Digital Supply Voltage	DVDD		3.0	3.3	3.6	V
Analog Ground Voltage	AVSS		-	AVDD-5	0	V
Digital Ground Voltage	DVSS		-	0	-	V

ELECTRICAL CHARACTERISTICS (Continued)

AVDD=5.0V, AVSS=0V, DVDD=3.3V, DVSS=0V and TA = +25°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
ANALOG SWITCH							
Top Signal Range	Input Range	V_{AIN}		0		AVDD	V
	Output Range	V_{AOUT}		0		AVDD	V
Bottom Signal Range	Input Range	V_{BIN}		0		AVDD	V
	Output Range	V_{BOUT}		0		AVDD	V
Top Channel On Current		I_{ACH_ON}	AVDD=5V, V_{AIN}=0V or 5V			50	mA
Bottom Channel On Current		I_{BCH_ON}	AVDD=5V, V_{BIN}=0V or 5V			50	mA
Top Switch On-resistance		R_{AON}	V_{AIN}=0V to AVDD , I_{ACH_ON}=-1mA		1	3	Ω
Bottom Switch On-resistance		R_{BON}	V_{BIN}=0V to AVDD , I_{BCH_ON}=-1mA		1	3	Ω
Top Leakage Current	Source Off Leakage Current	I_{AS_OFF}	AVDD=5V, V_{AIN} =5, V_{AOUT}=0V		0.05	1	uA
	Drain Off Leakage Current	I_{AD_OFF}	AVDD=5V, V_{AIN}=0V, V_{AOUT}=5V		0.05	1	uA
	Channel On Leakage Current	I_{ACH_OFF}	AVDD=5V, V_{AIN}=0V or 5V		0.05	1	uA
Bottom Leakage Current	Source Off Leakage Current	I_{BS_OFF}	AVDD=5V, V_{BIN} =5, V_{BOUT}=0V		0.05	1	uA
	Drain Off Leakage Current	I_{BD_OFF}	AVDD=5V, V_{BIN}=0V, V_{BOUT}=5V		0.05	1	uA
	Channel On Leakage Current	I_{BCH_OFF}	AVDD=5V, V_{BIN}=0V or 5V		0.05	1	uA

ELECTRICAL CHARACTERISTICS (Continued)

AVDD=5.0V, AVSS=0V, DVDD=3.3V, DVSS=0V and TA = +25°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
DIGITAL I/O							
Top Logic Input Voltage	Input High	V_{AIH}		0.7* DVDD			V
	Input Low	V_{AIL}				0.3* DVDD	V
Bottom Logic Input Voltage	Input High	V_{BIH}		0.7* DVDD			V
	Input Low	V_{BIL}				0.3* DVDD	V
Top Logic Input Current	Input High	I_{AIH}		-1		1	uA
	Input Low	I_{AIL}		-1		1	uA
Bottom Logic Input Current	Input High	I_{BIH}		-1		1	uA
	Input Low	I_{BIL}		-1		1	uA
SWITCH DYNAMIC CHARACTERISTICS							
Switching Time	Turn ON Time	t_{ON}	Clock base (calculate for special condition)		175		ns
	Turn OFF Time	t_{OFF}			235		ns
Top Capacitance	Input Off-Capacitance	C_{AIN_OFF}			150		pF
	Output Off-Capacitance	C_{AOUT_OFF}			150		pF
	Output On-Capacitance	C_{AOUT_ON}			300		pF
Bottom Capacitance	Input Off-Capacitance	C_{BIN_OFF}			150		pF
	Output Off-Capacitance	C_{BOUT_OFF}			150		pF
	Output On-Capacitance	C_{BOUT_ON}			300		pF
Off-Isolation			No Load, f_{SW}=1MHz	-16			dB
Channel-to-Channel Crosstalk			No Load, f_{SW}=1MHz	-41			dB

ELECTRICAL CHARACTERISTICS (Continued)

AVDD=5.0V, AVSS=0V, DVDD=3.3V, DVSS=0V and TA = +25°C, unless otherwise noted

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
POWER CONSUMPTION							
Top Analog Operating Current (AVDD)	Static	I_{AVDD_ST}	AVDD=5V			1	uA
	Dynamic	I_{AVDD_DYN}	AVDD=5V, f_{SW}=1.25MHz (Note1), All switch On/Off operating simultaneously			50	mA
Bottom Analog Operating Current (AVDD)	Static	I_{AVDD_ST}	AVDD=5V			1	uA
	Dynamic	I_{AVDD_DYN}	AVDD=5V, f_{SW}=1.25MHz (Note1), All switch On/Off operating simultaneously			50	mA
Top Digital Operating Current (DVDD)	Static	I_{DVDD_ST}	DVDD=3.3V			1	uA
	Dynamic	I_{DVDD_DYN}	DVDD=3.3V, f_{CLK}=10MHz (Note1), Combined operation of Reset, Group-On and DUT-Reject			400	uA
Bottom Digital Operating Current (DVDD)	Static	I_{DVDD_ST}	DVDD=3.3V			1	uA
	Dynamic	I_{DVDD_DYN}	DVDD=3.3V, f_{CLK}=10MHz (Note1), Combined operation of Reset, Group-On and DUT-Reject			400	uA

Note1 : The f_{CLK} is the frequency of digital signal CLK.
When the f_{CLK} is 10MHz, the maximum switching frequency (f_{SW}) is 1.25MHZ (1-clock command).

Note2 : The maximum of total analog operating current is 100 mA calculated by adding together Top and Bottom.
The maximum of total digital operating current is 800 uA calculated by adding together Top and Bottom.

TIMING CHARACTERISTICS

AVDD=5.0V, AVSS=0V, DVDD=3.3V, DVSS=0V and TA = +25°C, unless otherwise noted

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
DIGITAL I/O SIGNALS						
CLK Period	t_{PERIOD}				20	ns
DATA to CLK Setup Time	t_{DS}		10			ns
DATA to CLK Hold Time	t_{DH}		5			ns
CSN to CLK Setup Time	t_{CS}		10			ns
CSN to CLK Hold Time	t_{CH}		5			ns
WRN to CLK Setup Time	t_{WS}		10			ns
WRN to CLK Hold Time	t_{WH}		5			ns
POWER AND RESET SEQUENCE						
Power-up Period	t_{PU}		500			us
Power-down Period	t_{PD}		500			us
Power-on Reset Time	t_{RST}		2			us
Chip-ID Read Routine Time	t_{IDRD}		2			us
SWITCH ON/OFF TIMING DIAGRAM						
Switch Control Enable Time	t_{SWEN}		1			us
1-Clock Command Control Time	t_{SW1}				3	cycle
2-Clock Command Control Time	t_{SW2}				6	cycle

Note3 : The AC parameters of '**DIGITAL I/O SIGNALS**', '**POWER AND RESET SEQUENCE**' and '**SWITCH ON/OFF TIMING DIAGRAM**' of Top and Bottom are the same each other.

Timing Diagram of Digital I/O Signals

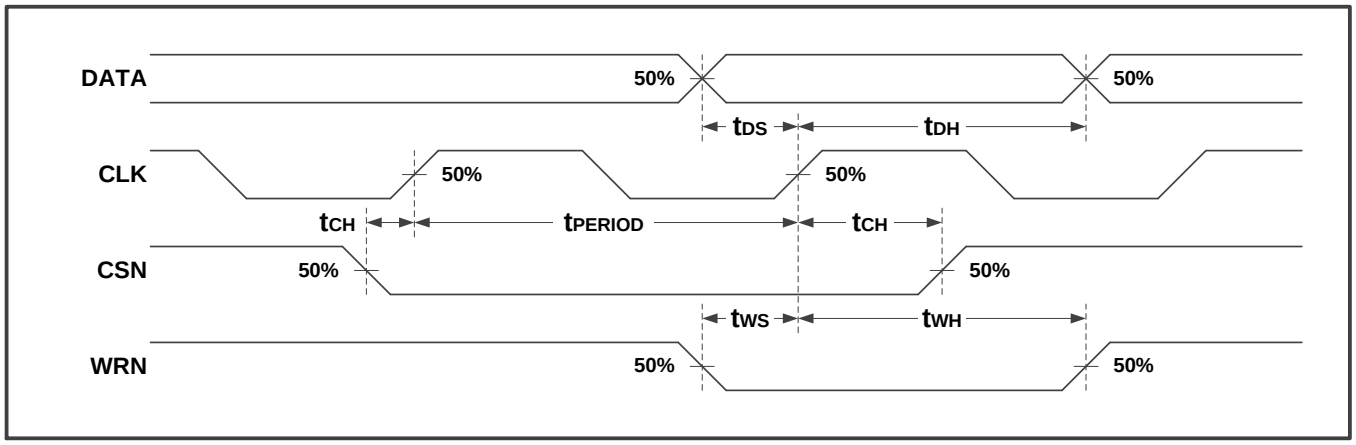
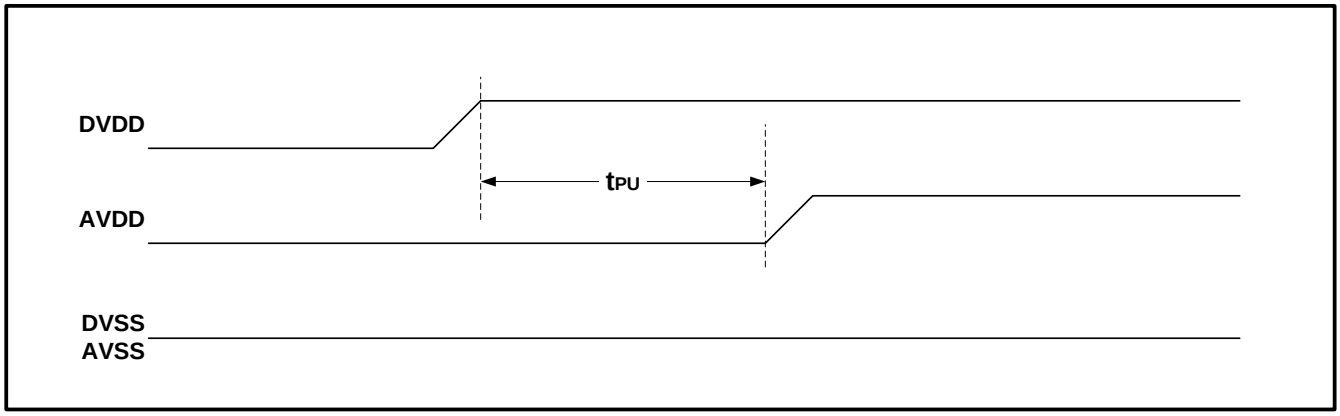
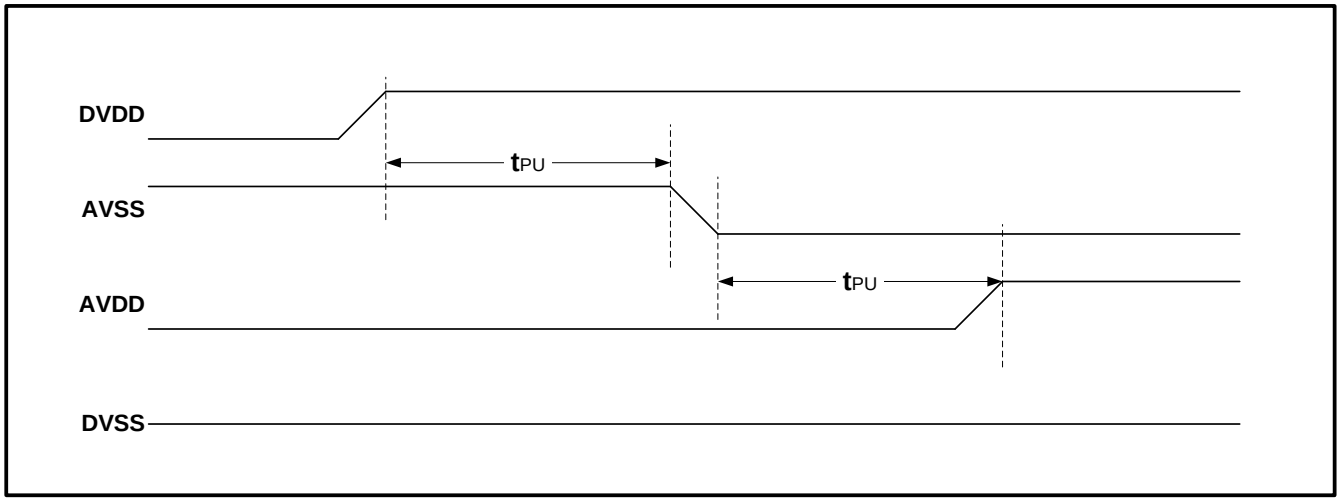


Figure 2. Timing Diagram of Digital Signals

Power and Reset sequence

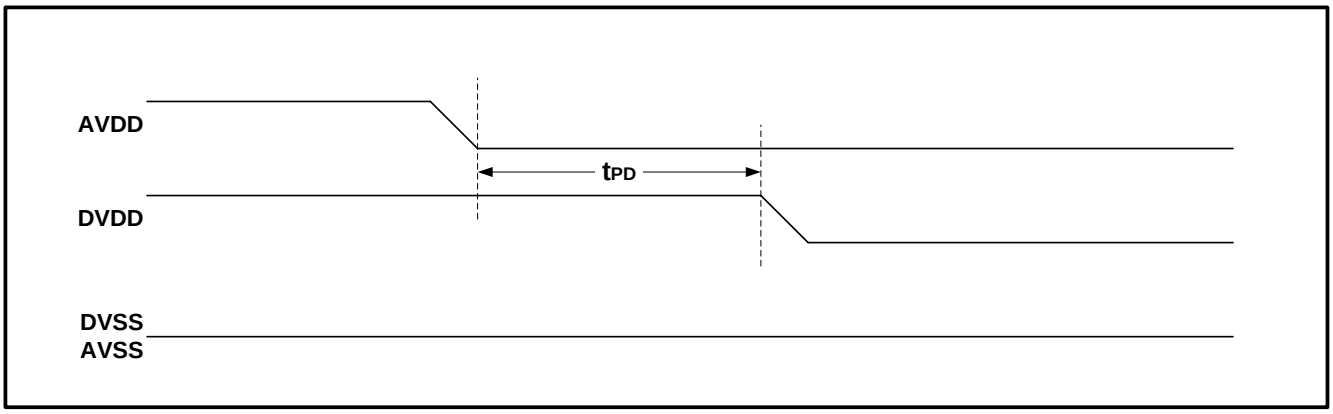


a. When AVSS = 0 V

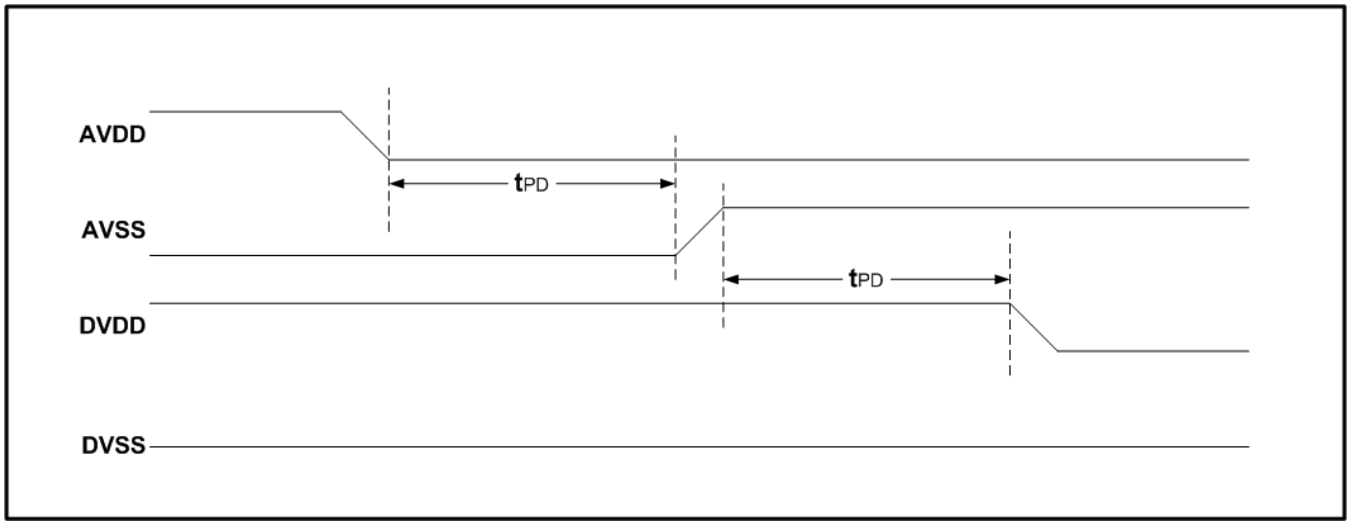


b. When AVSS < 0 V

Figure 3. Power-up Sequence



a. When AVSS = 0 V



b. When AVSS < 0 V

Figure 4. Power-down Sequence

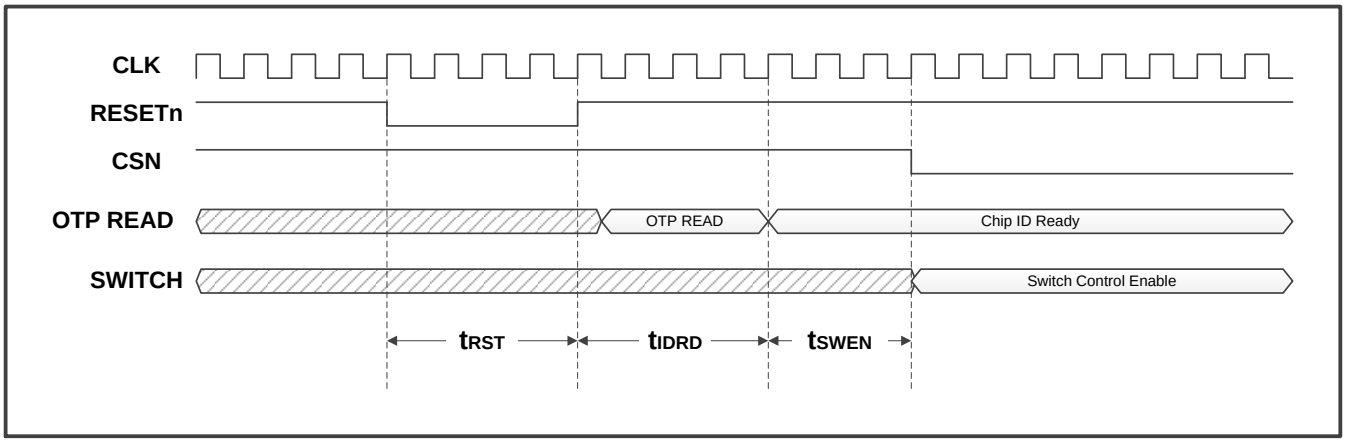


Figure 5. Reset and Stand-by Sequence

Switch On/Off Timing Diagram

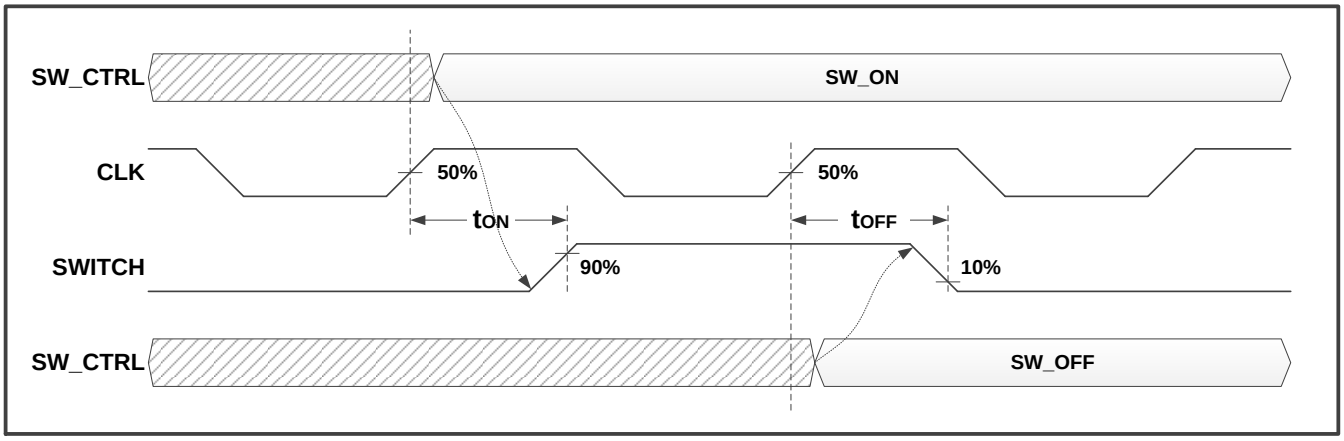


Figure 6. Switch On/Off Timing Diagram

PIN MAPPING TABLE

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	A_CLK	A_PAGE_UP	A_WRN	VPP	AIN63	AOUT62	AIN61	AOUT60	AIN59	AOUT58	AIN57	AOUT55	AIN54	AOUT52	AIN51	AOUT50	AIN49
B	A_TEST_IN	A_CSN	A_RSTN	BIN62	AOUT63	AIN62	AOUT61	AIN60	AOUT59	AIN58	AOUT57	AIN55	AOUT54	AIN52	AOUT51	AIN50	AOUT49
C	A_DATA1	A_DATA0	BIN0	BOUT62	BIN61	BOUT59	BIN58	BOUT56	BIN55	BOUT54	BIN51	AOUT56	AIN56	AOUT53	AIN53	AOUT48	AIN48
D	A_DATA3	A_DATA2	BOUT0	BIN63	BOUT61	BIN59	BOUT58	BIN56	BOUT55	BIN54	BOUT51	BIN50	BOUT49	BIN48	BOUT47	AIN47	AOUT47
E	AIN0	AOUT0	BIN1	BOUT63	AVDD	BOUT60	BIN60	BOUT57	BIN57	BOUT52	BIN52	BOUT50	BIN49	BOUT48	BIN47	AOUT46	AIN46
F	AOUT1	AIN1	BOUT1	BIN2	BOUT2	AVDD	DVDD	AVSS	AVSS	AVSS	BOUT53	BIN53	BOUT46	BIN45	BOUT44	AIN45	AOUT45
G	AIN2	AOUT2	AIN3	BOUT3	BIN4	AVDD	DVDD	DVSS	B_PAGE_UP	AVSS	BIN42	BOUT41	BIN46	BOUT45	BIN44	AOUT44	AIN44
H	AOUT4	AIN4	AOUT3	BIN3	BOUT4	AVDD	B_TEST_IN	DVSS	B_CSN	B_WRN	BOUT42	BIN41	BOUT40	BIN39	BOUT43	AIN43	AOUT43
J	AIN5	AOUT5	AIN6	BOUT5	BIN6	BOUT17	B_DATA1	B_DATA0	B_CLK	BOUT24	BIN27	BOUT37	BIN40	BOUT39	BIN43	AOUT42	AIN42
K	AOUT7	AIN7	AOUT6	BIN5	BOUT6	BIN17	B_DATA3	B_DATA2	B_RSTN	BIN24	BOUT27	BIN37	BOUT36	BIN35	BOUT38	AIN41	AOUT41
L	AIN8	AOUT8	AIN9	BOUT7	BIN8	BOUT16	BIN19	BOUT19	BIN23	BOUT23	BIN26	BOUT28	BIN36	BOUT35	BIN38	AOUT40	AIN40
M	AOUT10	AIN10	AOUT9	BIN7	BOUT8	BIN16	BOUT18	BIN20	BOUT21	BIN22	BOUT26	BIN28	BOUT30	BIN32	BOUT34	AIN39	AOUT39
N	AIN11	AOUT11	BIN9	BOUT10	BIN11	AOUT18	BIN18	BOUT20	BIN21	BOUT22	BIN25	BOUT25	BIN30	BOUT32	BIN34	AOUT38	AIN38
P	AOUT12	AIN12	BOUT9	BIN10	BOUT11	AIN18	AOUT20	AIN22	AOUT24	AIN26	AOUT28	AIN30	BOUT29	BIN31	BOUT33	AIN37	AOUT37
R	AIN13	AOUT13	BIN12	BOUT13	BIN14	AOUT17	AIN20	AOUT22	AIN24	AOUT26	AIN28	AOUT30	BIN29	BOUT31	BIN33	AOUT36	AIN36
T	AOUT14	AIN14	BOUT12	BIN13	BOUT14	AIN17	AOUT19	AIN21	AOUT23	AIN25	AOUT27	AIN29	AOUT31	AIN32	AOUT33	AIN35	AOUT35
U	AIN15	AOUT15	BIN15	BOUT15	AIN16	AOUT16	AIN19	AOUT21	AIN23	AOUT25	AIN27	AOUT29	AIN31	AOUT32	AIN33	AOUT34	AIN34

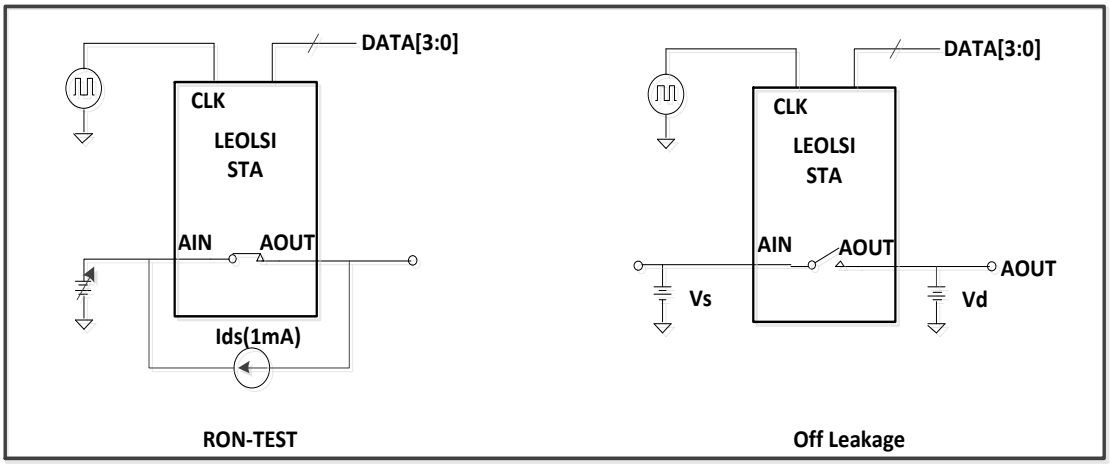
(TOP View)

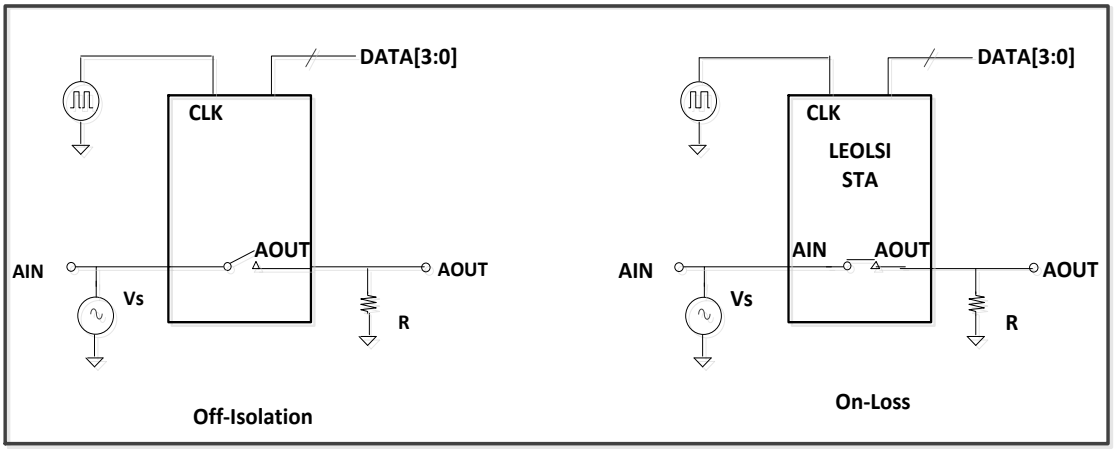
PIN DESCRIPTIONS

PIN NAME	I/O	Descriptions
A_CLK	DI	System clock (TOP)
A_RSTN	DI	System reset. Active Low (TOP)
A_CSN	DI	Chip select. Active Low (TOP)
A_WRN	DI	Data write enable. Active Low (TOP)
A_DATA[3:0]	DIO	Data bus (TOP)
A_TEST_IN	DI	Tied to GND in Normal mode (TOP)
A_PAGE_UP	DI	Tied to GND in Normal mode (TOP)
VPP	PWR	Tied to GND in Normal mode (TOP, BOTTOM)
AIN[63:0]	AI	Analog switch input (TOP)
AOUT[63:0]	AO	Analog switch output (TOP)
AVDD	PWR	Analog Power (TOP, BOTTOM)
AVSS	GND	Analog Ground (TOP, BOTTOM)
DVDD	PWR	Digital Power (TOP, BOTTOM)
DVSS	GND	Digital Ground (TOP, BOTTOM)
B_CLK	DI	System clock (BOTTOM)
B_RSTN	DI	System reset. Active Low (BOTTOM)
B_CSN	DI	Chip select. Active Low (BOTTOM)
B_WRN	DI	Data write enable. Active Low (BOTTOM)
B_DATA[3:0]	DIO	Data bus (BOTTOM)
B_TEST_IN	DI	Tied to GND in Normal mode (BOTTOM)
B_PAGE_UP	DI	Tied to GND in Normal mode (BOTTOM)
BIN[63:0]	AI	Analog switch input (BOTTOM)
BOUT[63:0]	AO	Analog switch output (BOTTOM)

AI: analog input **AO: analog output**
DI: digital Input **DIO: digital Input / Output**
PWR: power **GND: ground**

TEST CIRCUITS





Off isolation=20log(V_{AOUT}/V_{AIN}), On Loss=20log(V_{AOUT}/V_{AIN})

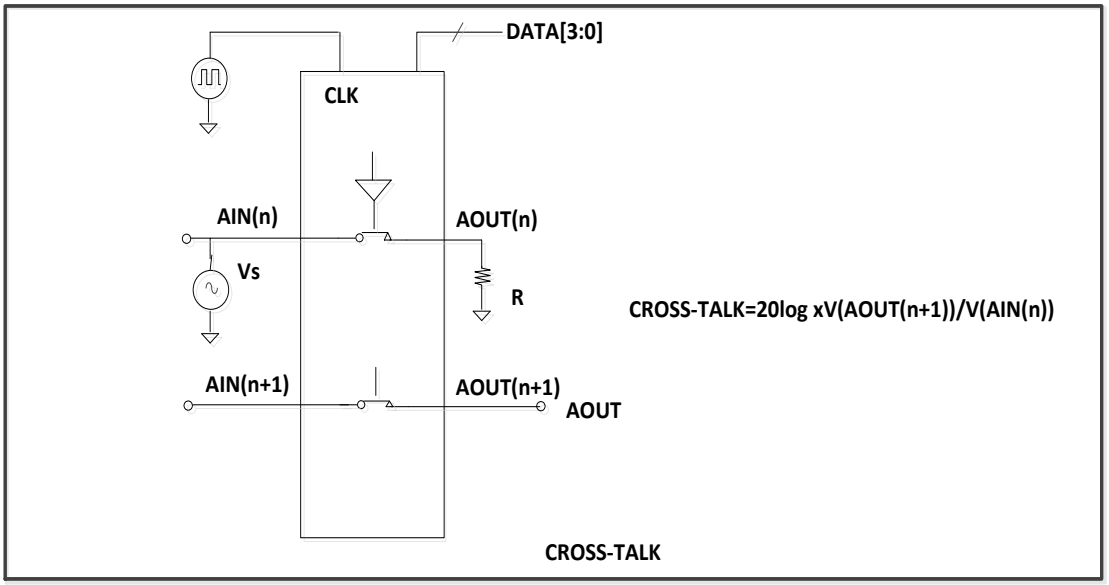
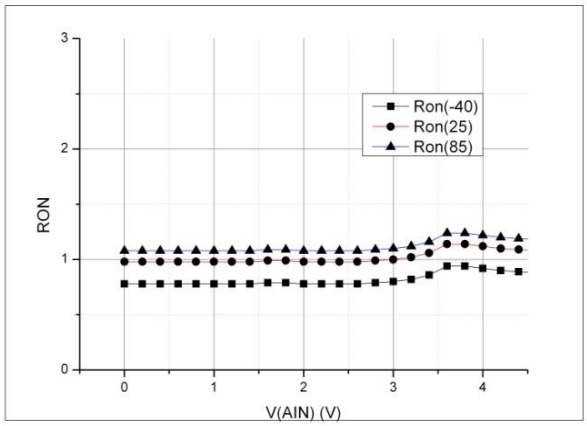
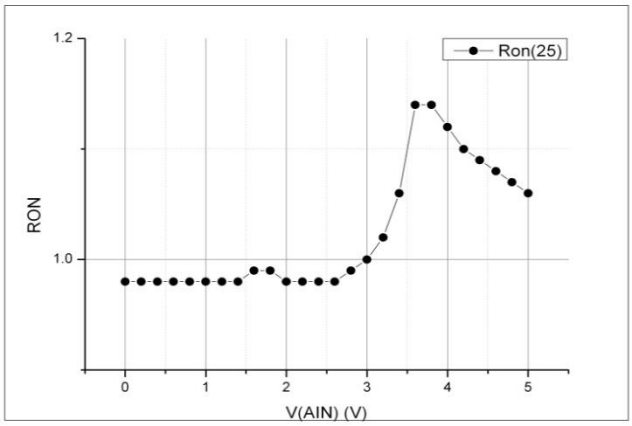


Figure 7. Test Circuits

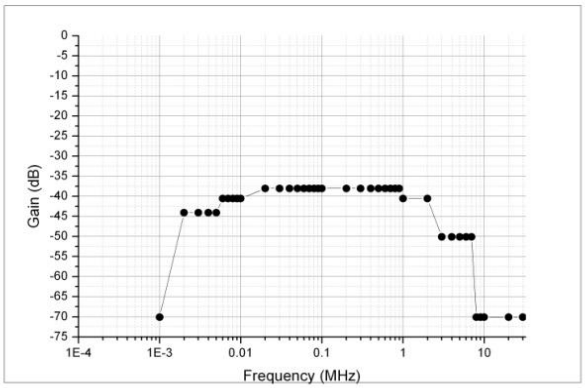
TEST RESULTS



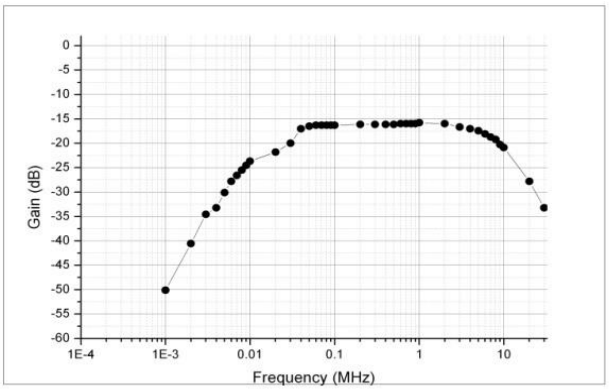
On-resistance vs. vain



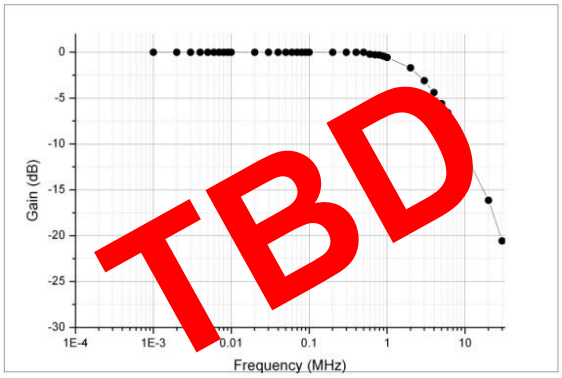
On-resistance(room temp) vs. vain



Cross talk vs. Frequency



Isolation vs. Frequency



On Loss vs. Frequency

Figure 8. Test Results

DETAIL DESCRIPTIONS

Definitions

The STA-FX2 IC consists of 16 cores which consist of 8 switches, hence it has 128 switches. The device provides two Chip-IDs for Top and Bottom and they can be programmed in internal OTP memory inside Top and Bottom individually. On the other hand, the eight Core-IDs of Top and Bottom are fixed in the device. The internal switch structure is shown in Figure 9. The Channel-ID is implicated in user defined commands interpreted in Digital Interface section.

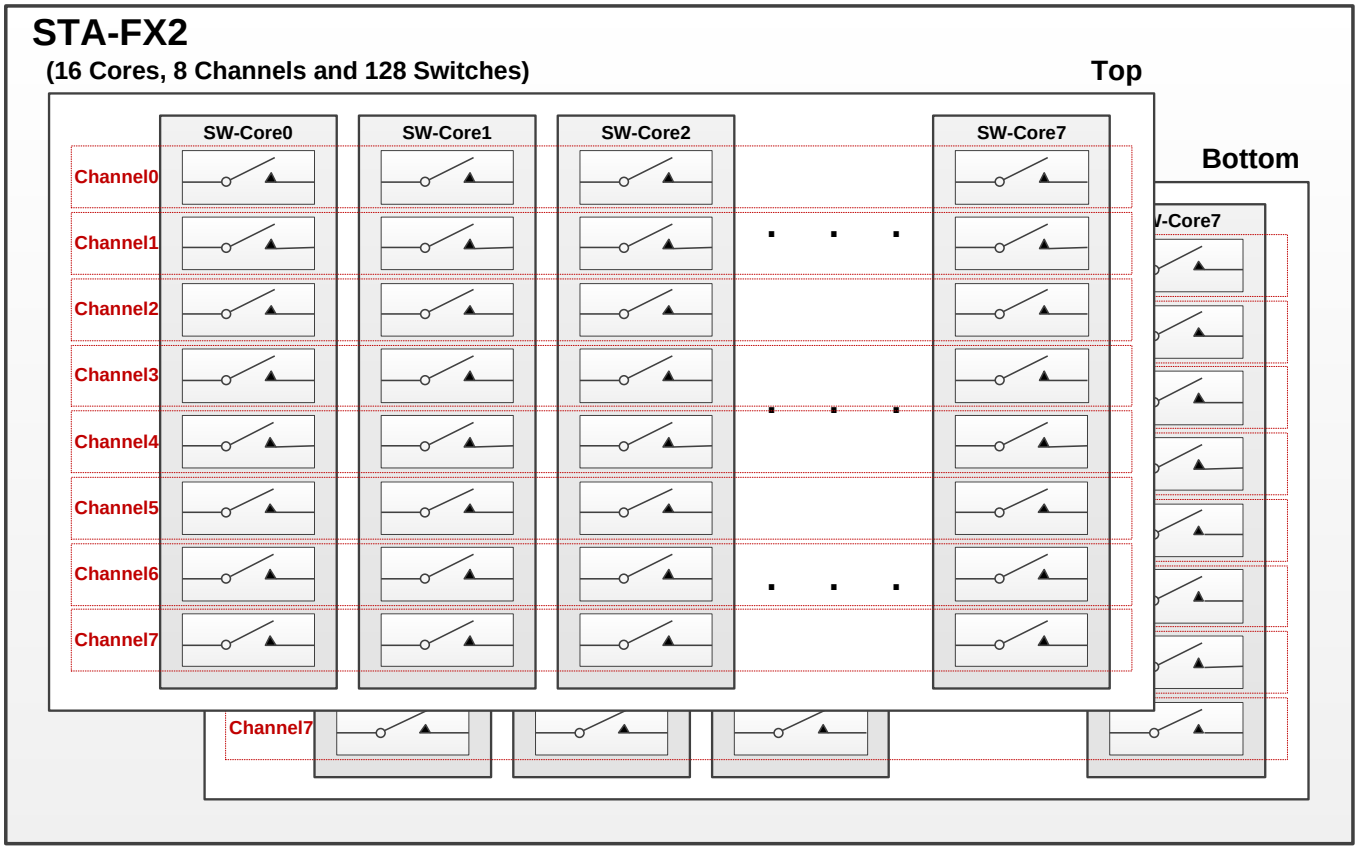


Figure 9. STA-FX2 IC Internal Switch Structure and Definitions – Cores and Channels

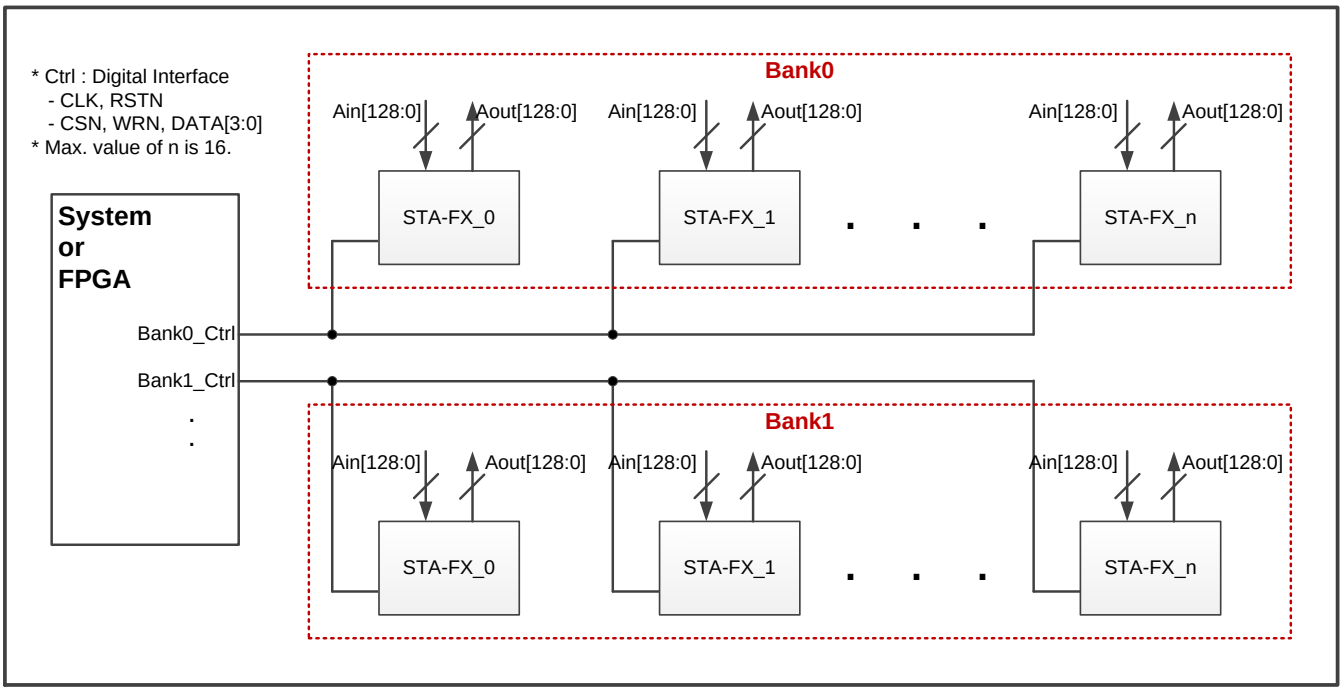


Figure 10. STA-FX2 IC Application Structure and Definitions – Banks and Controls

In system application, two or more STA-FX2 ICs can be controlled by the same digital interface - control and data signals such as CLK, RESETN, CSN, WRN and DATA[3:0] shown in Figure 10 and these STA-FX2 IC network can be called as 'bank'. Because the Chip-ID is assigned in 5-bit address and two Chip-IDs can be used in one STA-FX2 IC, the maximum number of STA-FX2 IC in one bank is 16. The 3-bit address is used to assign Core-ID in Top and Bottom of STA-FX2 IC individually. The user can not apply the Chip-ID and the Core-ID to 1-clock command but to 2-clock command. Refer to Figure 12 and 13.

- ***Bank***

The bank means STA network connected by the same digital interface - control and data signals such as CLK, RESETN, CSN, WRN and DATA[3:0]. Refer to the Figure 10.

- ***Reject***

The individual switch control logic can be rejected from all commands. After entering reject state in which the switch is off, no command alters on/off state of rejected switch except the command 'INITIAL_ALL', 'CANCEL_REJECT' and external RSTN.

Digital Interface

- *1-Clock Command*

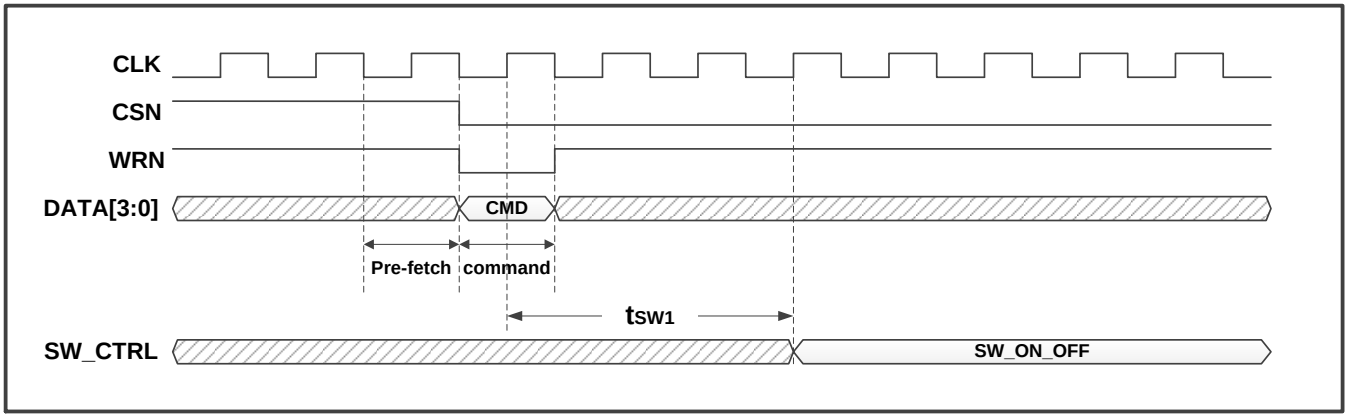


Figure 11. 1-Clock Command Control Timing Diagram

The 1-clock command is applied to all cores and all switches. Furthermore, this command is applied to all STA ICs in the same bank. The ‘CMD’ in Figure 11 means command which defines following modes:

Command	Value	Function
NORMAL	0x0	Returns to normal mode from Load mode (release all chip selection)
LOAD_ALL	0x1	Selects all chips to load(apply) the same commands
VIRTUAL	0x2	Programming mode for test
CLEAR_ALL	0x3	Makes all switches off
ENABLE_ALL	0x4	Makes all switches on
INITIAL_ALL	0x5	Initializes all switches releasing reject condition and making them on

- ***2-Clock Command***

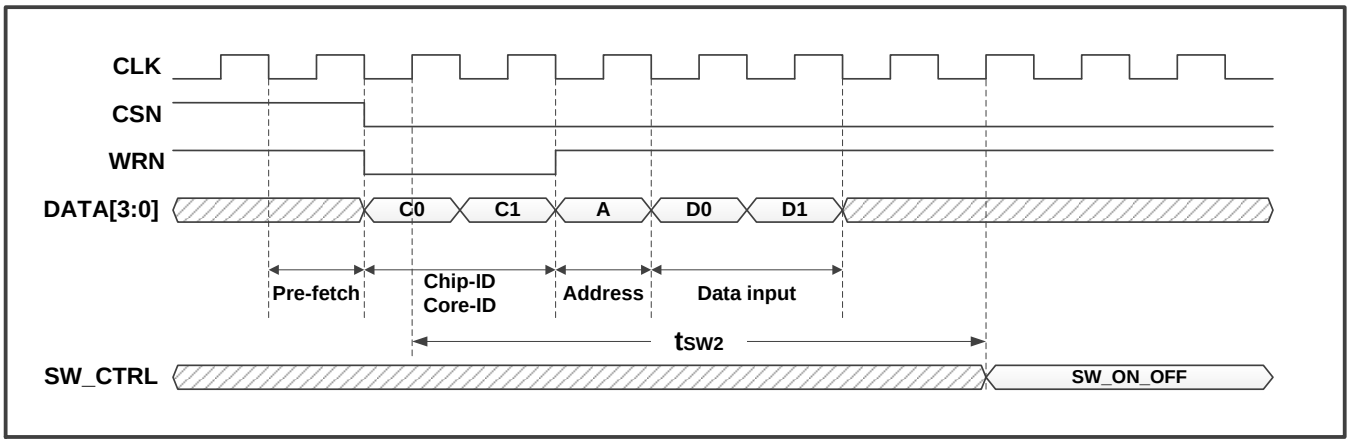


Figure 12. 2-Clock Command Control Timing Diagram

The '2-clock command' can control 8 Cores individually as well as simultaneously. Especially, the case of simultaneous 8 Core control can explain Channel-level switch control and it means that the users do not access Channel-ID directly.

In 2-clock command protocol, the signal DATA[3:0] can represent several items 'C0', 'C1', 'A', 'D0' and 'D1' shown in Figure 12 and these can be interpreted like as Figure 13.

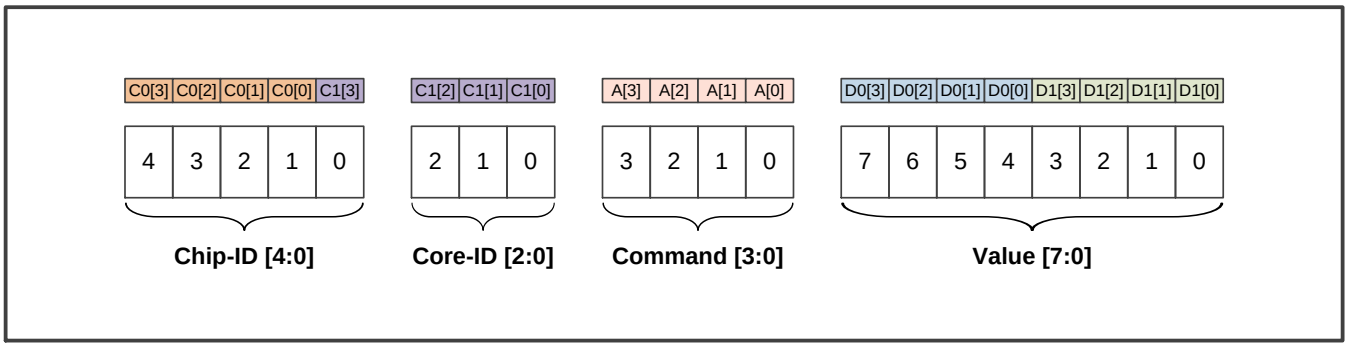


Figure 13. Interpretation of DATA[3:0] Signals in 2-Clock Command

The 'C0' and 'C1' are Chip-ID and Core-ID items and the address 'A' defines switch control Command. The Data 'D0' and 'D1' means the next state Value of 8 individual switches.

The 2-Clock command has three types of control.

- CHL(Chip-level) : applied to all chips in the same bank (both Chip-ID and Core-ID are ignored)
- CRL(Core-level) : applied to all cores of selected chip (Chip-ID is referred but Core-ID is ignored)
- SWL(Switch-level) : applied to selected switches of selected core (both Chip-ID and Core-ID are referred)

When the MSB of Command[3:0] is low, the Value[7:0] is applied to all Cores. Otherwise, the MSB of Command[3:0] is high, the Value[7:0] is applied to one Core selected by Core-ID[2:0].

The detail 2-Clock commands are given below.

Command	Value	Function	Remark
AND_CRL	0x0	Next switch status are produced by bitwise AND operation between current switch status and Data[7:0]. Applied to all cores of the selected chip.	CRL
OR_CRL	0x1	Next switch status are produced by bitwise OR operation between current switch status and Data[7:0]]. Applied to all cores of the selected chip.	CRL
DIRECT_CRL	0x2	Next switch status are produced by Data[7:0] directly. Applied to all cores of the selected chip.	CRL
DIRECT_CHL	0x3	Next switch status are produced by Data[7:0] directly. Applied to all cores of all chips in the same bank.	CHL
REJECT_CRL	0x4	Reject all switches of selected core by bitwise AND operation between current core reject status and Data[7:0].	CRL
-	0x5	Reserved	-
-	0x6	Reserved	-
-	0x7	Reserved	
AND_SWL	0x8	Next switch status are produced by bitwise AND operation between current switch status and Data[7:0]. Applied to the selected core.	SWL
OR_SWL	0x9	Next switch status are produced by bitwise OR operation between current switch status and Data[7:0] . Applied to the selected core.	SWL
DIRECT _SWL	0xa	Next switch status are produced by Data[7:0] directly. Applied to the selected core.	SWL
-	0xb	Reserved	-
REJECT _SWL	0xc	Reject selected switch by bitwise AND operation between current switch reject status and Data[7:0]	SWL
CANCEL_RJT	0xd	Cancel all switch-reject of selected core	-
-	0xe	Reserved	-
-	0xf	Reserved	-

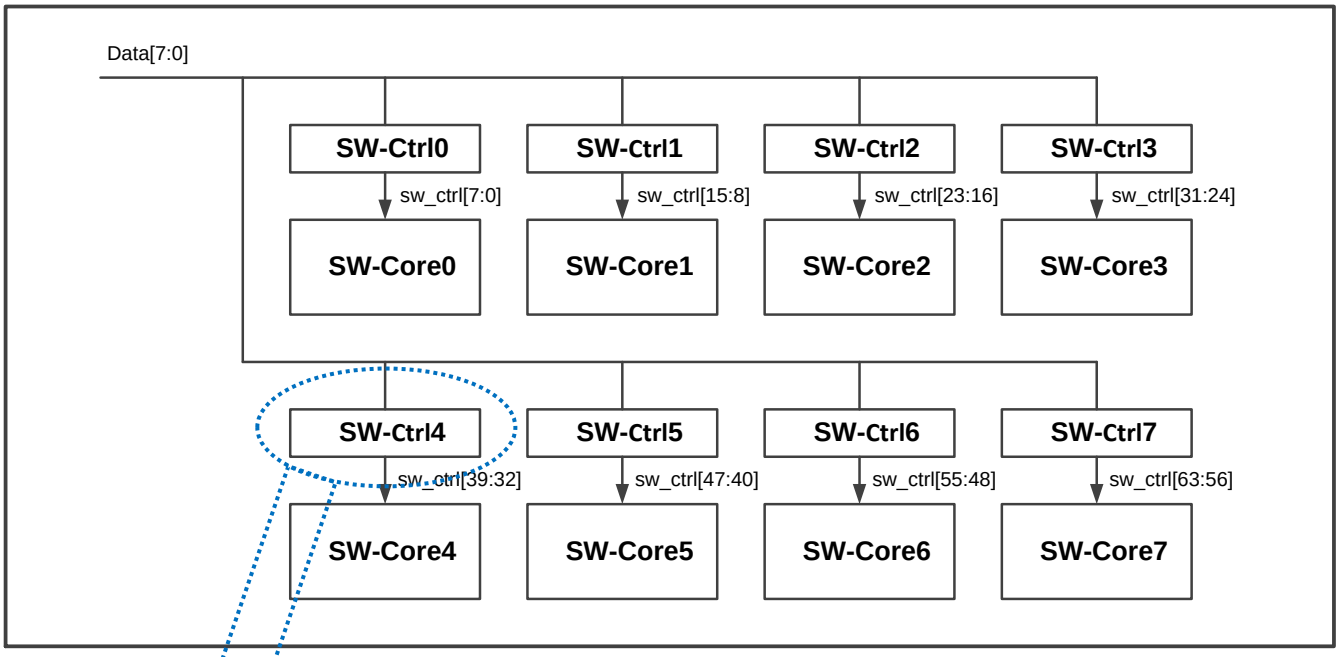


Figure 14. Switch Control Structure for 2-Clock Command

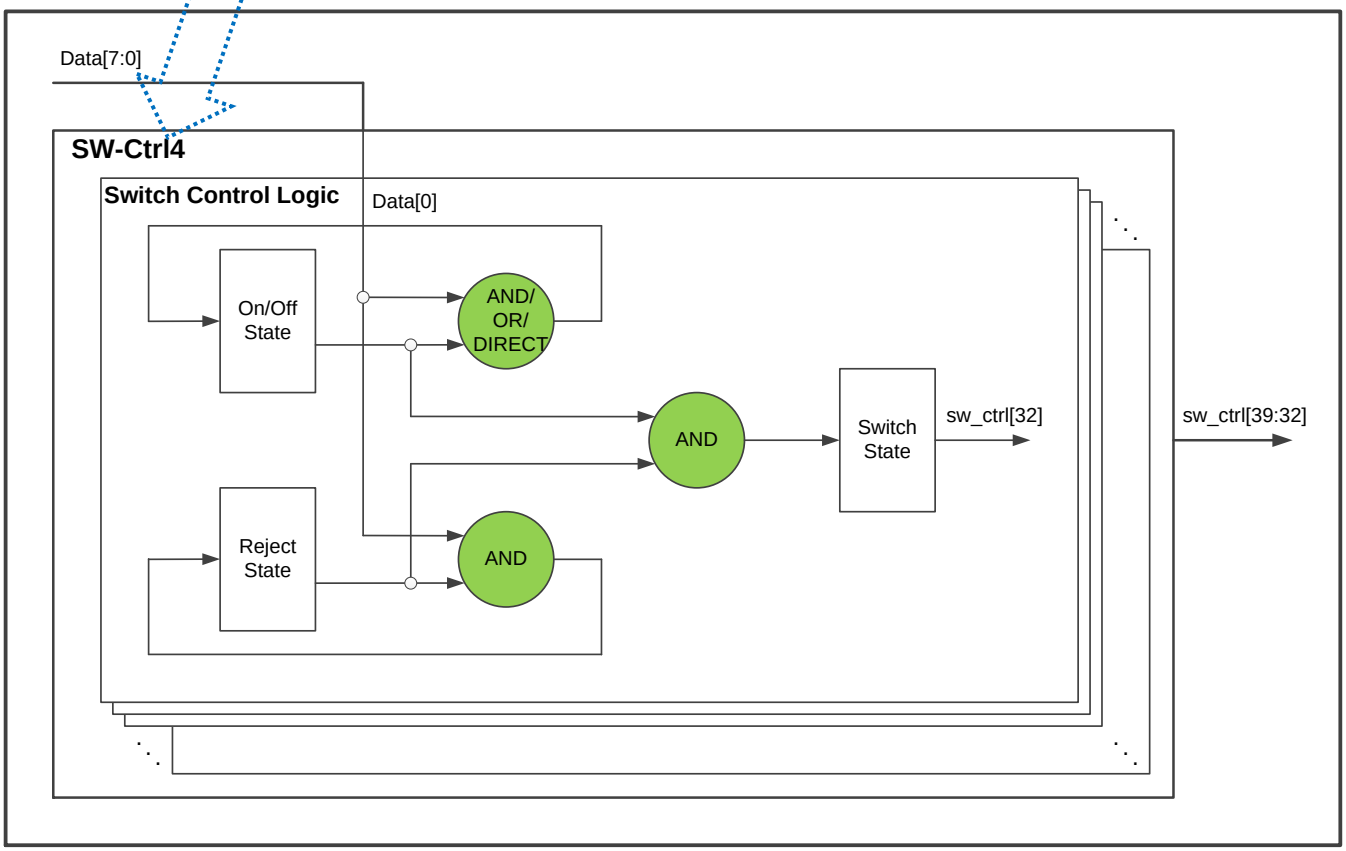


Figure 15. Basic Concept of 2-Clock Command Switch Control

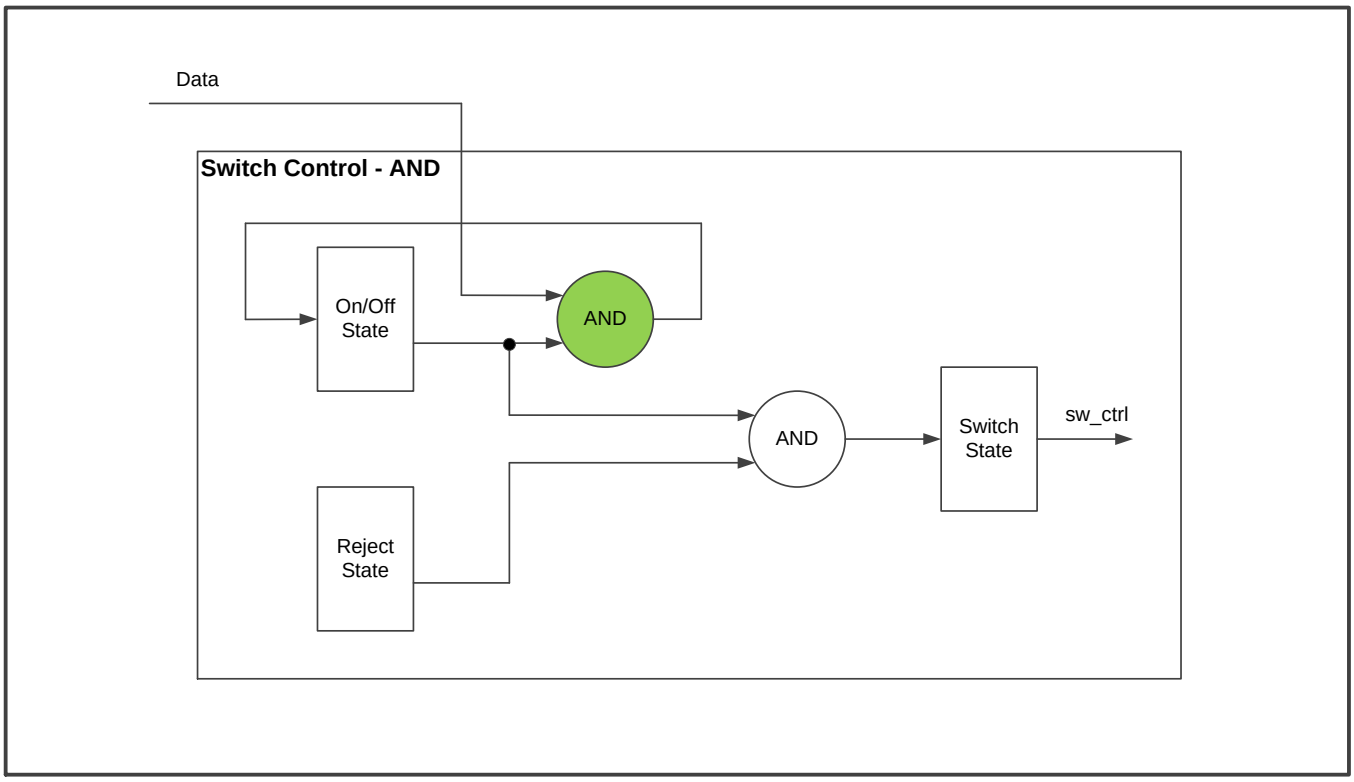


Figure 16. 2-Clock Command Switch Control - AND

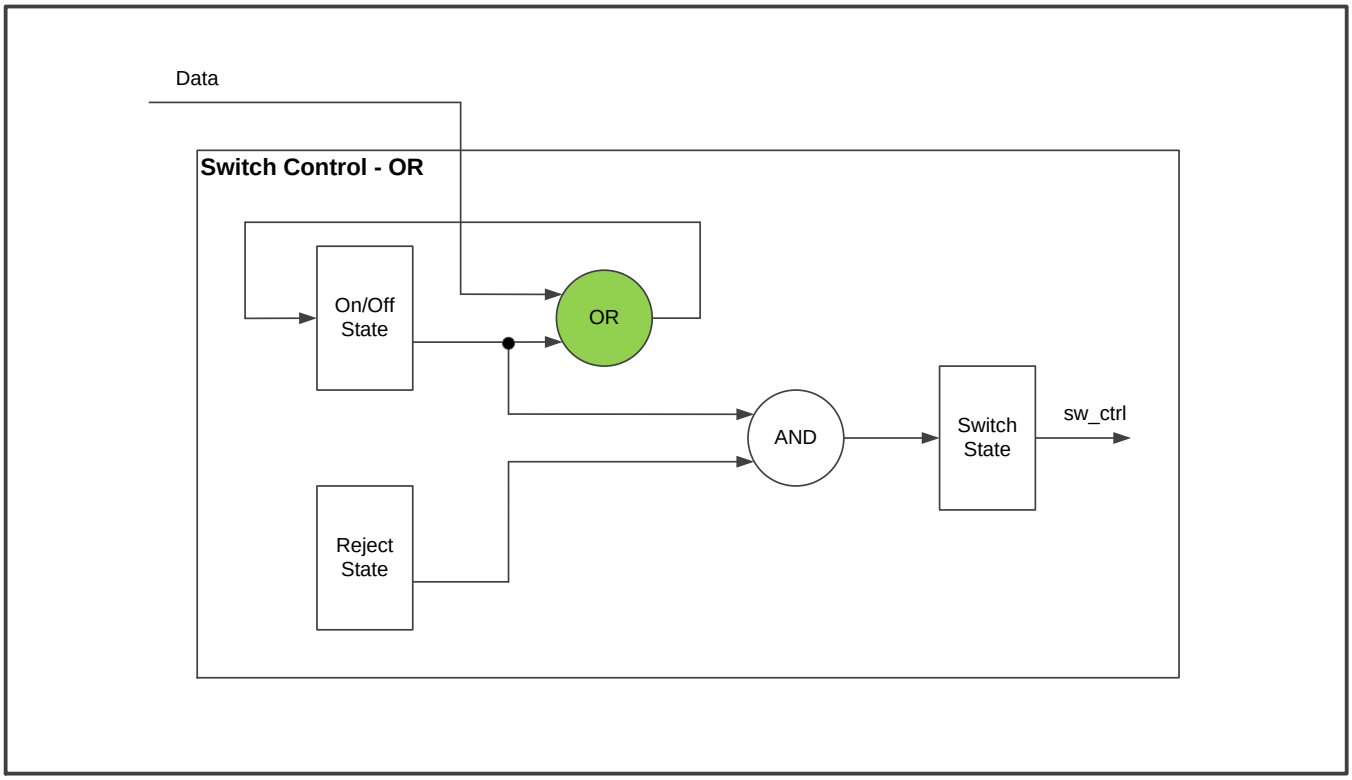


Figure 17. 2-Clock Command Switch Control - OR

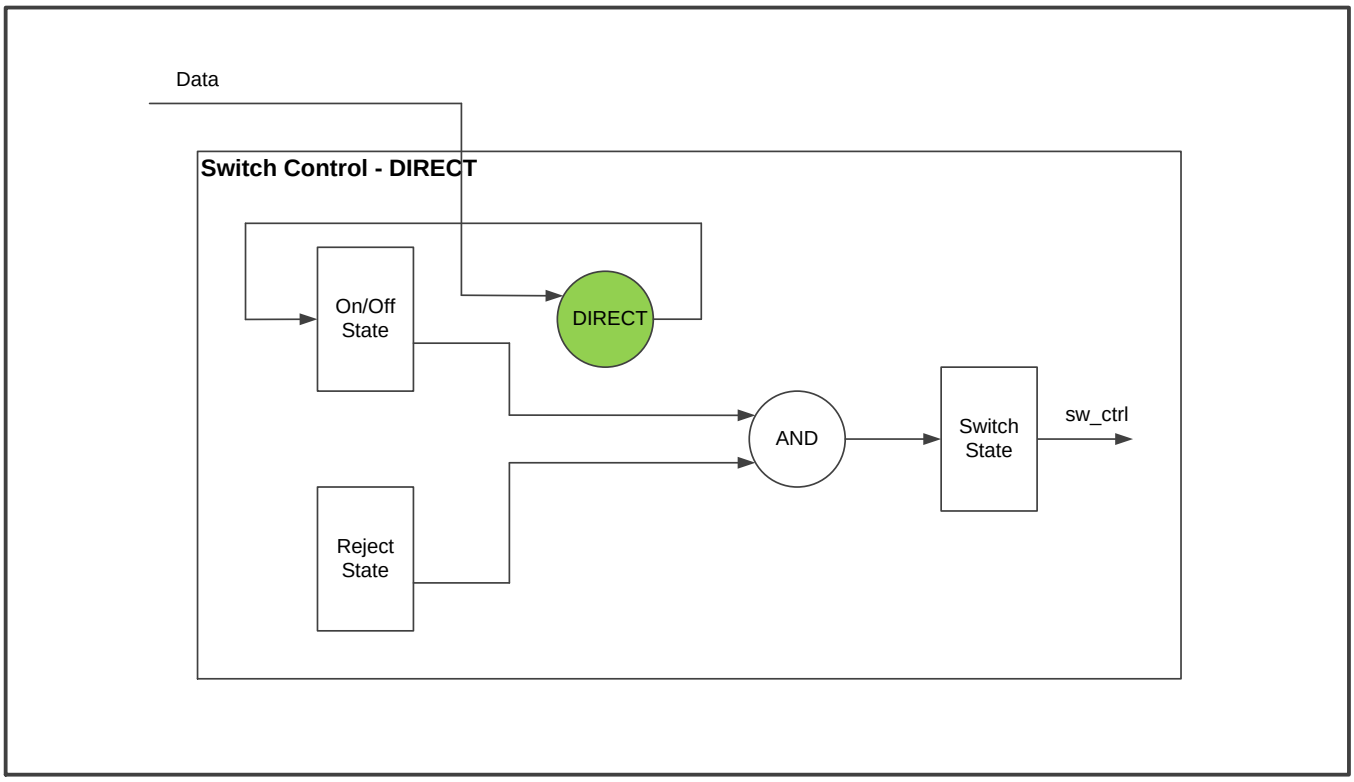


Figure 18. 2-Clock Command Switch Control - DIRECT

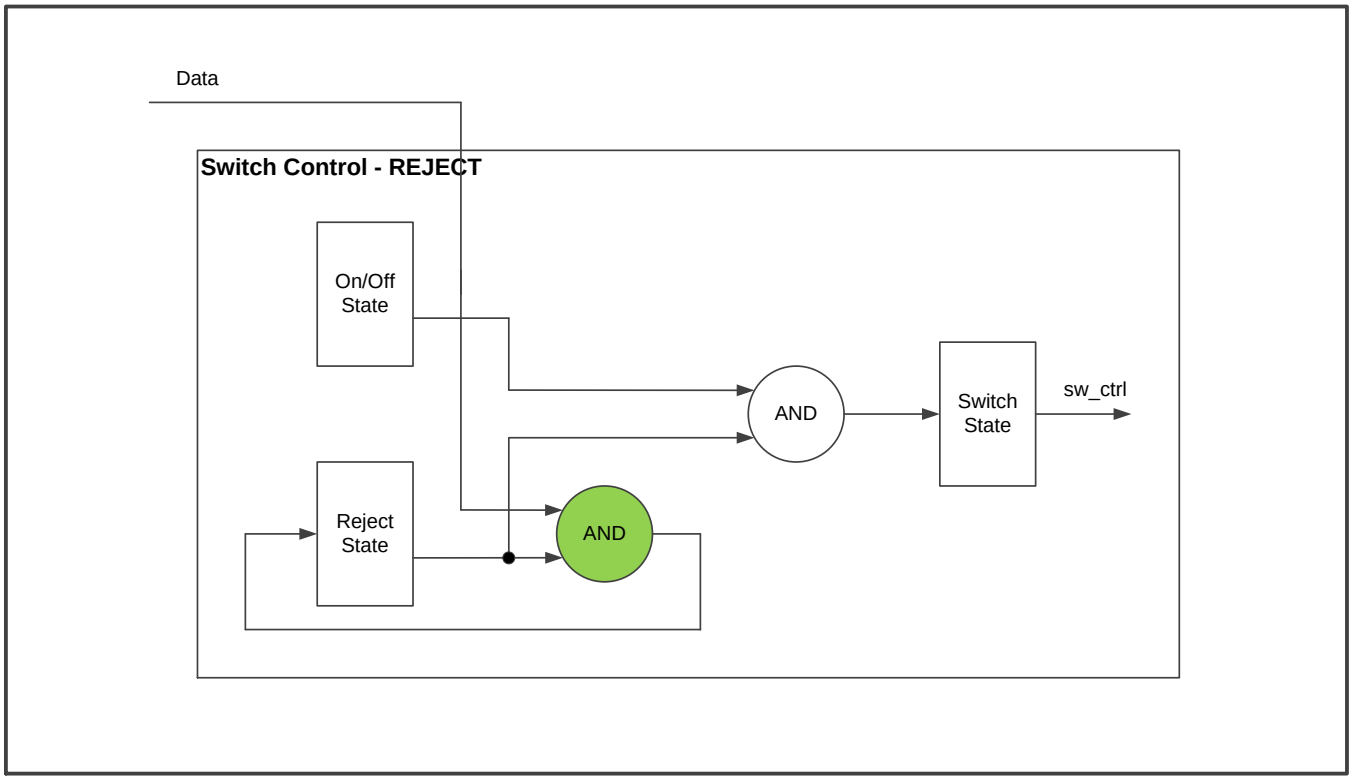


Figure 19. 2-Clock Command Switch Control - REJECT

APPLICATION EXAMPLE

The STA IC receives serial input data synchronized with a clock signal.
Most of all, to achieve maximum control speed in PCB, simulation using IBIS model should be carried out.

1. TEST_IN, PAGE_UP and VPP pins should be connected to ground through 20-kΩ (pull-down) resistor.
2. CSN pin should be connected to digital power through 20-kΩ (pull-up) resistor.
3. To guarantee the control speed, any resistor or capacitor should not be connected to CLK and DATA pins.
4. 10uF and 0.1uF decoupling capacitors should be connected to between AVDD and AVSS, and the same capacitors to between DVSS and DVSS.

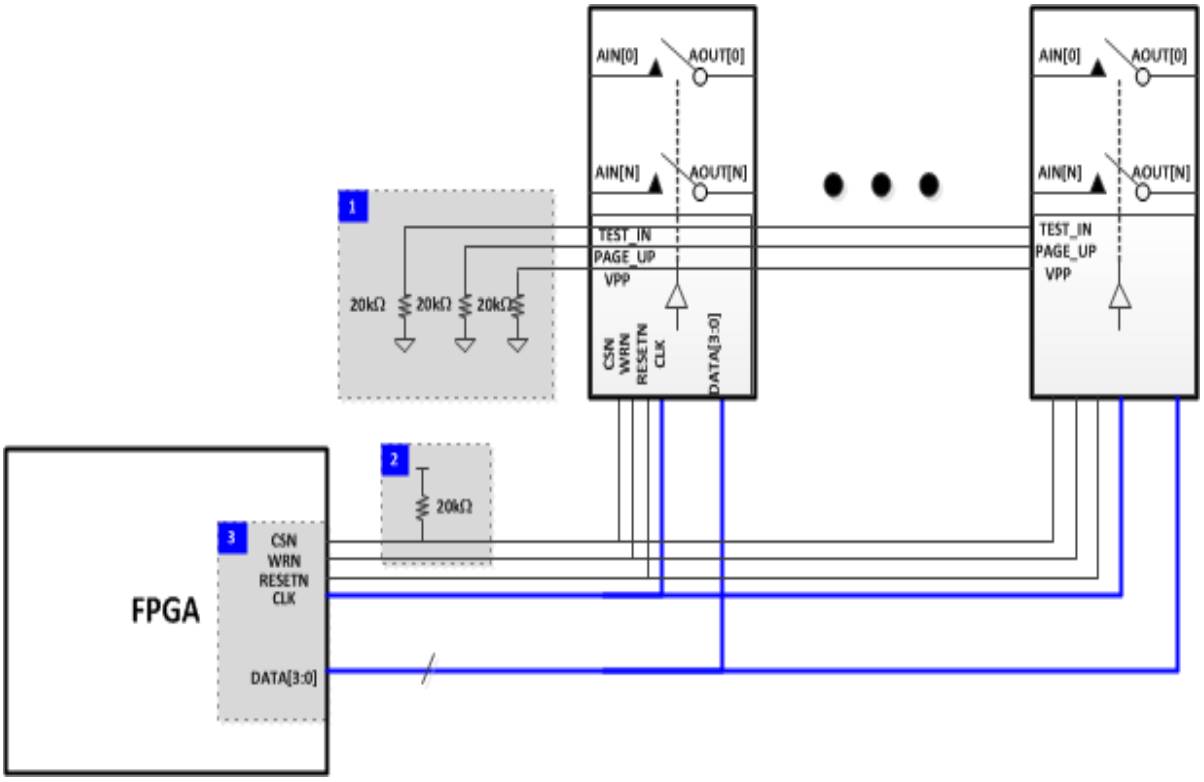
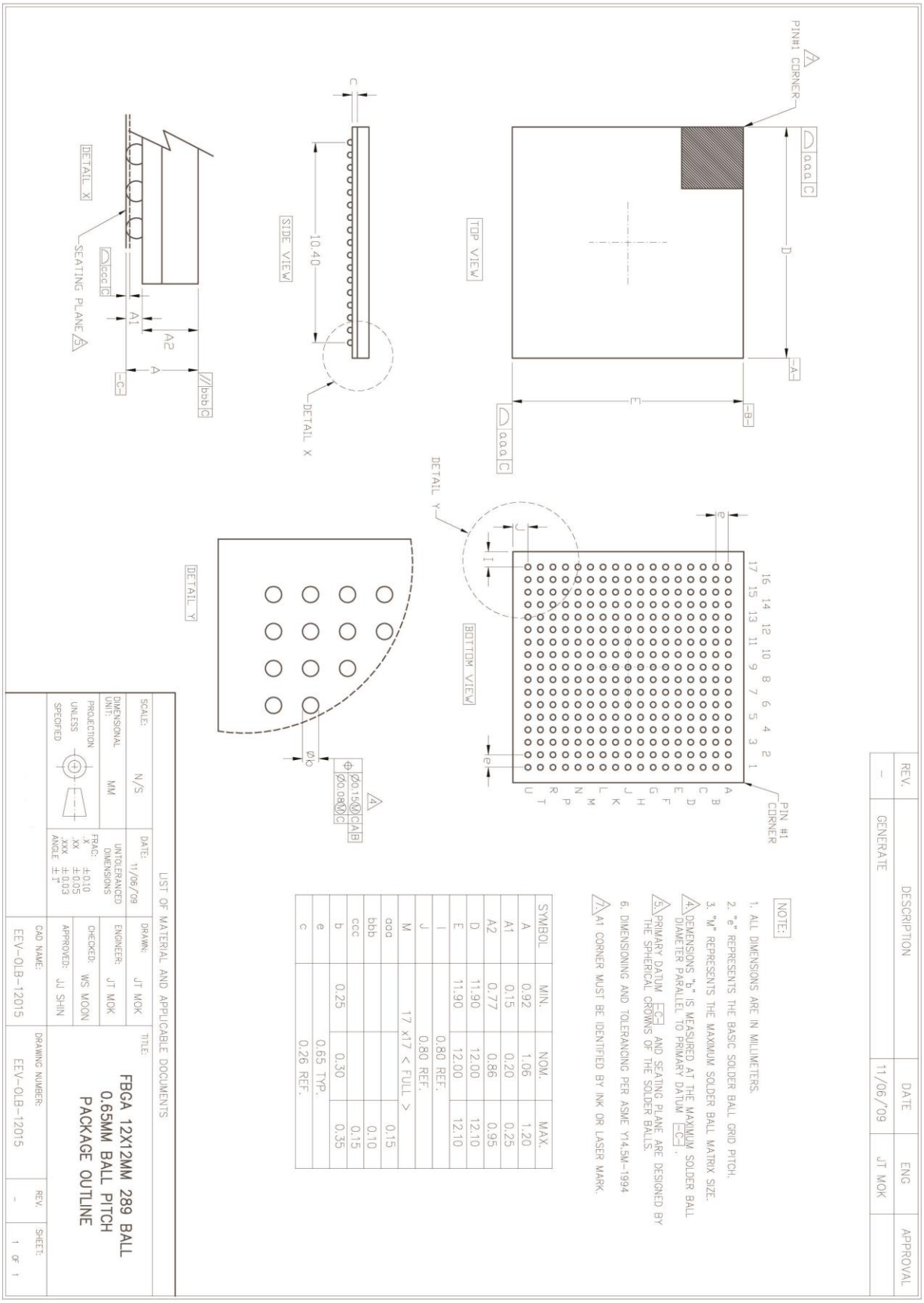


Figure 20. Application Example of PCB design

PACKAGE INFORMATION



REVISION HISTORY

Revision	Date	Description
1.0	2015-03	Revised format

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The world is driven by analog

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