STAx
Commands Descriptions

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Preliminary

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SCOPE OF THIS DOCUMENT

This document is intended to provide users with supplementary information about the commands of STAx series. This document describes only the commands of STAx ICs. For more information about each STAx series, refer to the corresponding data sheet.

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STAx Commands Descriptions

Interface Protocol & Types of Commands

Controlling STAx is performed through commands from the host. The host sends commands through two control signals (CSN and WRN) and 4-bit wide data pins. CSN signal is used to select the target Bank, and WRN signal decides the type of the command. The protocol for each command is decided by the type of the command – 1/2 clock commands.

- *1-Clock Commands (Writing Commands Only)*

1-clock commands are the commands for which WRN signal goes LOW for single cycle. Figure 1 shows the timing diagram for 1-clock commands.

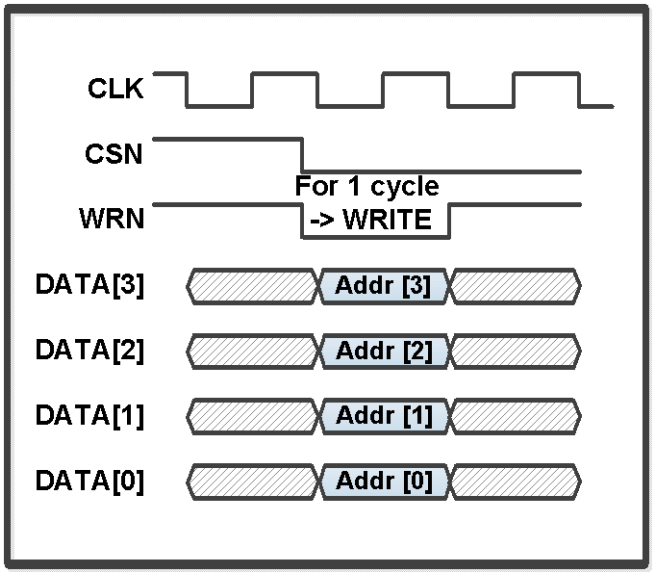

Figure 1. Timing Diagram for 1-Clock Commands.

The 1-clock commands consist of the commands which are applied to all switches of all STAx ICs in the bank. Since the target for the 1-clock command is all switches in all Cores of all STAx ICs, they require neither Chip ID nor Core ID.

- *2-Clock commands (Writing Commands Only)*

2-clock commands are the commands for which WRN signal goes LOW for two clocks. Each command includes Chip-ID, Core-ID, Command, and Parameters, and it is mainly used to control the switches. Figure 2 shows the timing diagram for 2-clock commands.

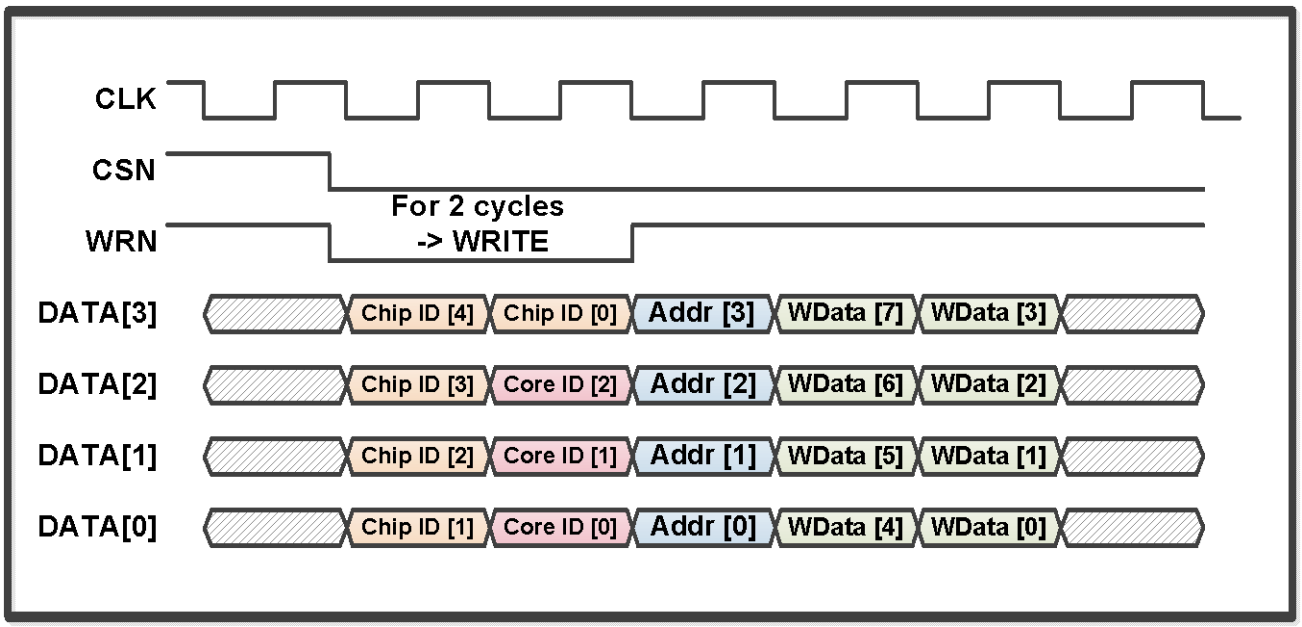

Figure 2. Timing Diagram for 2-Clock commands.

As shown in Figure 2, IDs and commands are received through DATA[3:0] pins. Chip-ID specifies the target STAx IC in the bank, and Core-ID specifies the target Core / Channel of the target chip. Addr[3:0] is the actual command, and WData[7:0] is a parameter to control the states of the 8 switches specified by Chip-ID and Core-ID. All of the 2-clock commands are for writing WData[7:0] to target registers.

Controlling Switches

- *States of Switches*

The main usage of STAx is to control AIN – AOUT connection by changing the states of its switches. Each switch can be in one of two states – ON, OFF.

In **ON** state, the switch is turned-on, and the AIN signal is CONNECTED to the corresponding AOUT signal.

In **OFF** state, the switch is turned-off, and the AIN signal is DISCONNECTED from the corresponding AOUT signal.

Besides ON/OFF states, each switch has an additional flag named **REJECTn**. If REJECTn flag is '0' for a switch, the switch changes to OFF state automatically, and further commands to turn on the switch are ignored. Only special 1-clock commands or external reset (RSTN) can set the REJECTn flag to '1'.

- *Initialization of Switches*

The initialization of the switches can be done through initialization commands. There are three initialization commands. They are,

- 1-clock command 0x3: CLEAR_ALL
- 1-clock command 0x4: ENABLE_ALL
- 1-clock command 0x5: INITIAL_ALL

Since all of these commands are 1-clock commands, they are executed by all STAx ICs in the selected bank by CSN signal. The states of all switches in the bank are simultaneously changed by these commands, and it helps set the initial states of all switches with less commands. For the detailed information about each command, refer to *Commands Descriptions*.

- *Changing States of Switches*

To change the states of switches, following 2-clock commands are used.

- 2-clock command 0x0: AND_CRL
- 2-clock command 0x1: OR_CRL
- 2-clock command 0x2: DIRECT_CRL
- 2-clock command 0x3: DIRECT_CHL
- 2-clock command 0x8: AND_SWL
- 2-clock command 0x9: OR_SWL
- 2-clock command 0xA: DIRECT_SWL

DIRECT_XXX commands directly specify the ON-OFF states of the target switches. The target switches are specified using Chip-ID and Core-ID in the transmitted command, combined with the suffix of the command. The intended ON-OFF states for the target switches are transmitted through WData[7:0]. To turn on the switch, corresponding bit of WData should be '1', and to turn off, it should be '0'.

AND_XXX / OR_XXX commands updates the ON-OFF states of the target switches by AND/OR-ing the target switches' current ON-OFF states with the transmitted data through WData[7:0]. The target switches are specified using Chip-ID and Core-ID in the transmitted command, combined with the suffix of the command. As for AND/OR-ing operation, ON is represented as '1', and OFF is represented as '0'.

For the detailed information about each command, refer to *Commands Descriptions*.

- *Controlling REJECTn Flags*

A REJECTn flag is used to let the switch ignore further ON-OFF related commands. It is useful when we want some switches to stay OFF while we control many switches simultaneously with commands such as DIRECT_CHL. REJECTn flags can be controlled by REJECT_XXX / CANCEL_RJT commands. There are three commands to set REJECTn flags.

- 2-clock command 0x4: REJECT_CRL
- 2-clock command 0xC: REJECT_SWL
- 2-clock command 0xD: CANCEL_RJT

REJECTn flags are set to '0' according to the transmitted WData[7:0] of REJECT_XXX commands. If a bit of WData is '0', corresponding REJECTn flag(s) is set to '0'. Otherwise, corresponding REJECTn flag(s) does not change. The target switches are specified by Chip-ID and Core-ID of the transmitted command.

CANCEL_RJT command is used to set the REJECTn flag to '1'. It clears the REJECTn flags of the specified Core of the specified STAx IC regardless of WDATA[7:0] value. The target Chip and Core are specified by Chip-ID and Core-ID of the transmitted command.

For the detailed information about REJECT_XXX / CANCEL_RJT commands, refer to *Commands Descriptions*.

Commands Descriptions

- Suffixes of the Commands

Most of STAx's commands are to control the states of the switches. Basically, each command can control switches in Core unit. However, to reduce the number of commands for setting the states of the switches, several variations of commands are supported, and they can address target switches in different ways from basic command (i.e. in Core unit). To represent this easily, commands have suffixes which represent the range of the target switches. The suffixes are,

- *_ALL
- *_CHL
- *_CRL
- *_SWL

_ALL suffix is for 1-clock commands. It represents that the target switches for this command is ALL SWITCHES IN THE BANK.

_CHL suffix is for 2-clock commands. It represents that the target switches for this command are ALL SWITCHES IN THE BANK. The transmitted WData for _CHL commands are applied to eight switches in every Core. Since WData is applied to all Cores in all STAx ICs in the Bank, Chip-ID / Core-ID are ignored.

_CRL suffix is for 2-clock commands. It represents that the target switches for this command are ALL SWITCHES IN THE SPECIFIED CHIP. The transmitted WData for _CHL commands are applied to eight switches in every Core. Since WData is applied to all Cores in the specified STAx IC, Core-ID is ignored.

_SWL suffix is for 2-clock commands. It represents that the target switches for this command are SWITCHES OF THE SPECIFIED CORE IN THE SPECIFIED CHIP. The transmitted WData for _SWL commands are applied to eight switches of the specified Core. Since WData is applied to single Core in the specified STAx IC, both Chip-ID / Core-ID are used.

- ***1-Clock Commands***

Table 1 shows the list of the 1-clock commands.

Table 1. 1-Clock Commands List.

Addr	Command	Description
0x0	NORMAL	NOT SUPPORTED (Returns to NORMAL mode).
0x1	LOAD_ALL	NOT SUPPORTED (Enters LOAD mode).
0x2	VIRTUAL	NOT SUPPORTED (Enters VIRTUAL mode).
0x3	CLEAR_ALL	Turns-off all switches of all chips in the Bank (i.e. OFF state). REJECTn flags are NOT affected.
0x4	ENABLE_ALL	Turns-on all switches of all chips in the Bank (i.e. ON state). Switches with REJECTn flags remain in OFF state.
0x5	INITIAL_ALL	Turns-on all switches of all chips in the Bank (i.e. ON state). REJECTn flags are set to '1' (i.e. NO REJECT). Switches with REJECTn flags being '0' are also changed to ON state.
0x6 ~ 0xF	RSVD	Reserved

- ***CLEAR_ALL (0x3) / ENABLE_ALL (0x4) / INITIAL_ALL (0x5)***

CLEAR_ALL / ENABLE_ALL / INITIAL_ALL commands are mainly used for initialization of switches in the selected Bank. These commands are applied to all switches of all STAx ICs in the Bank simultaneously.

CLEAR_ALL command turns off (i.e. change to OFF state) all switches of all STAx ICs in the Bank. Note that REJECTn flags are NOT affected by CLEAR_ALL command.

INITIAL_ALL / ENABLE_ALL commands turn on (i.e. change to ON state) all switches of all STAx ICs in the Bank. The difference between these two commands is that while INITIAL_ALL command also sets REJECTn flags of all switches to '1', ENABLE_ALL command does not affect REJECTn flags.

Table 2 shows the operation of the four initialization commands.

Table 2. Operation of Initialization Commands.

Command	ON-OFF States	REJECTn Flags
CLEAR_ALL	OFF	NOT AFFECTED
INITIAL_ALL	ON	SET TO '1'
ENABLE_ALL	ON	NOT AFFECTED

- ***2-Clock commands***

Table 3 shows the list of 2-clock commands.

Table 3. 2-Clock commands List.

Addr	Command	Function
0x0	AND_CRL	Updates all Cores' ON-OFF states of the target STAx IC. Performs logical AND operation on all Cores of the specified STAx IC with the transmitted eight bit data through WDATA[3:0]. The ON-OFF states of each Core of the specified STAx IC are replaced with the corresponding logical AND operation result. Switches whose REJECTn flags are '0' remain in OFF state. For the logical operation, ON is regarded as 1, and OFF is regarded as 0. Chip-ID specifies the target STAx IC. Core-ID is ignored. WData represents the operand for logical AND operation.
0x1	OR_CRL	Updates all Cores' ON-OFF states of the target STAx IC. Performs logical OR operation on all Cores of the specified STAx IC with the transmitted eight bit data through WDATA[3:0]. The ON-OFF states of each Core of the specified STAx IC are replaced with the corresponding logical OR operation result. Switches whose REJECTn flags are '0' remain in OFF state. For the logical operation, ON is regarded as 1, and OFF is regarded as 0. Chip-ID specifies the target STAx IC. Core-ID is ignored. WData represents the operand for logical OR operation.
0x2	DIRECT_CRL	Changes ON-OFF states of all switches in the specified STAx IC. Updates all Cores' ON-OFF states of the target STAx IC. Switches whose REJECTn flags are '0' remain in OFF state. Chip-ID specifies the target STAx IC. Core-ID is ignored. WData represents the update value for ON-OFF states of all Cores in the target STAx IC. 0: OFF, 1: ON
0x3	DIRECT_CHL	Changes ON-OFF states of all switches of all STAx ICs in the selected Bank. Updates all Cores' ON-OFF states of all STAx ICs in the selected Bank. Switches whose REJECTn flags are '0' remain in OFF state. Chip-ID is ignored. Core-ID is ignored. WData represents the update value for ON-OFF states of all Cores in the target STAx IC. 0: OFF, 1: ON

(Continued)

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0x4	REJECT_CRL	Changes the REJECTn flags of the specified STAx IC. Eight REJECTn flags of each Core are changed identically. ON-OFF states are updated according to REJECTn flags' values. Chip-ID specifies the target STAx IC. Core-ID is ignored. WData[0] represents the update value for REJECTn flags of Core0. WData[1] represents the update value for REJECTn flags of Core1. WData[2] represents the update value for REJECTn flags of Core2. WData[3] represents the update value for REJECTn flags of Core3. WData[4] represents the update value for REJECTn flags of Core4. WData[5] represents the update value for REJECTn flags of Core5. WData[6] represents the update value for REJECTn flags of Core6. WData[7] represents the update value for REJECTn flags of Core7. 0: Changes to REJECT state (i.e. REJECTn = 0). 1: No Change.
0x5 ~ 0x7	RSVD	Reserved
0x8	AND_SWL	Updates specified Core's ON-OFF states of the target STAx IC. Performs logical AND operation on the specified Core of the specified STAx IC with the transmitted eight bit data through WDATA[3:0]. The ON-OFF states of the specified Core of the specified STAx IC are replaced with the corresponding logical AND operation result. Switches whose REJECTn flags are '0' remain in OFF state. For the logical operation, ON is regarded as 1, and OFF is regarded as 0. Chip-ID specifies the target STAx IC. Core-ID specifies the target Core. WData represents the operand for logical AND operation.
0x9	OR_SWL	Updates specified Core's ON-OFF states of the target STAx IC. Performs logical OR operation on the specified Core of the specified STAx IC with the transmitted eight bit data through WDATA[3:0]. The ON-OFF states of the specified Core of the specified STAx IC are replaced with the corresponding logical OR operation result. Switches whose REJECTn flags are '0' remain in OFF state. For the logical operation, ON is regarded as 1, and OFF is regarded as 0. Chip-ID specifies the target STAx IC. Core-ID specifies the target Core. WData represents the operand for logical OR operation.
0xA	DIRECT_SWL	Changes ON-OFF states of the specified Core in the specified STAx IC. Switches whose REJECTn flags are '0' remain in OFF state. Chip-ID specifies the target STAx IC. Core-ID specifies the target Core. WData represents the update value for ON-OFF states of the target Core in the target STAx IC. 0: OFF, 1: ON
0xB	RSVD	Reserved

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0xC	REJECT_SWL	Changes the REJECTn flags of the specified Core of the specified STAx IC. ON-OFF states are updated according to REJECTn flags' values. Chip-ID specifies the target STAx IC. Core-ID specifies the target Core. WData represents the update value for REJECTn flags of the specified Core. 0: Changes to REJECT state (i.e. REJECTn = 0). 1: No Change.
0xD	CANCEL_RJT	Sets the REJECTn flags of the specified Core of the specified STAx IC to '1' (i.e. back to NORMAL state from REJECT state). Eight REJECTn flags of the specified Core of the specified STAx IC are set to '1'. Chip-ID specifies the target STAx IC. Core-ID specifies the target Core. WData is ignored.
0xE ~ 0xF	RSVD	Reserved

- ***AND_CRL (0x0)***

AND_CRL command updates all of the ON-OFF states in the target STAx IC. Logical AND operation is performed on every Core with the input eight bit data, and each Core's ON-OFF state is updated with the logical operation result. The target STAx IC is specified by Chip-ID. Figure 3 shows an example for AND_CRL command.

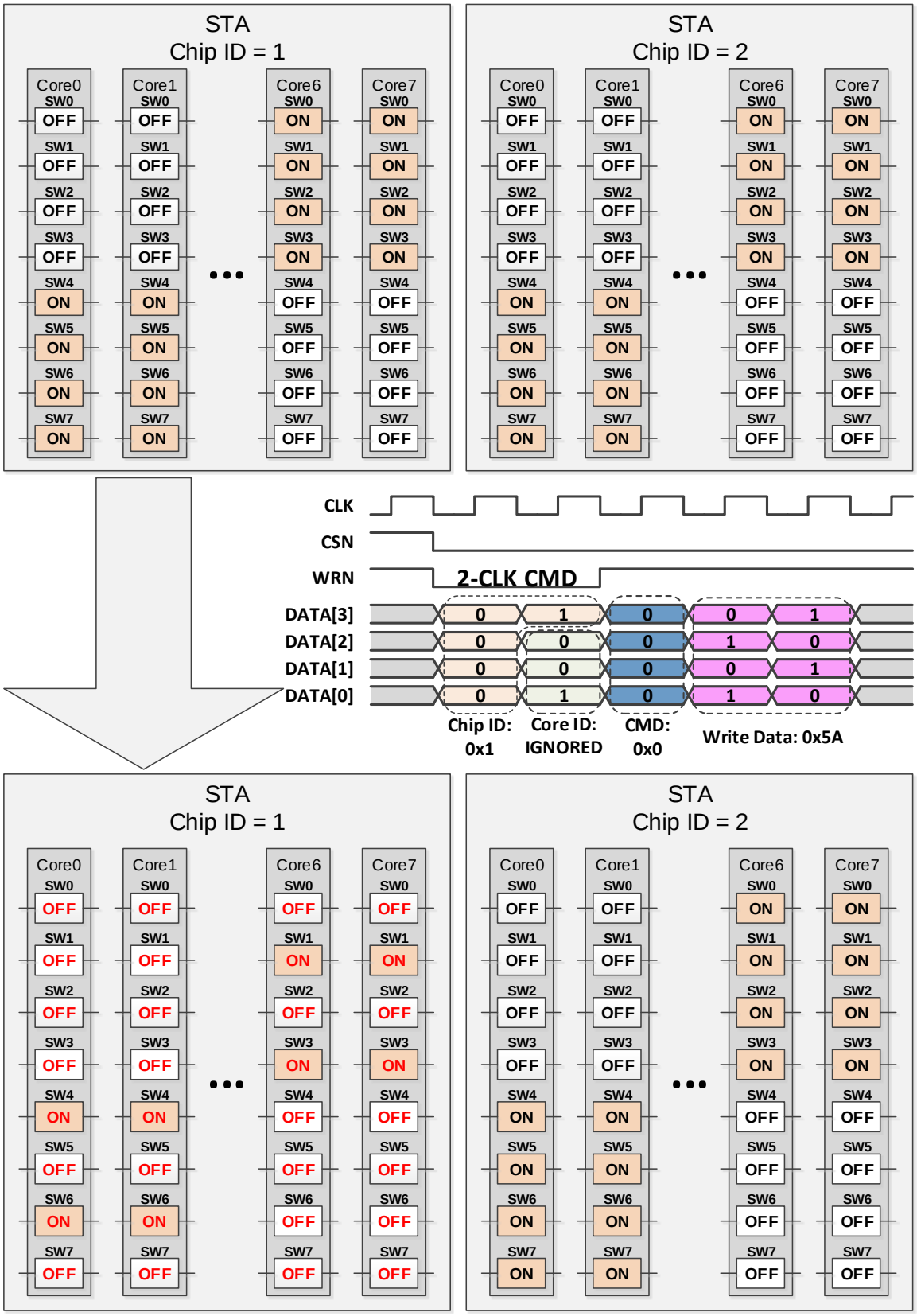

Figure 3. Example for AND_CRL Command.

In Figure 3, the input Chip-ID from the command is 0x1. Logical AND operation is performed with every Core of the STAx IC whose Chip-ID is 0x1, and the ON-OFF state is updated with the result of the logical operation. For the logical operation, ON is regarded as ‘1’, and OFF is as ‘0’. The Core-ID included in the command is ignored. Note that the switches whose REJECTn flags are set to ‘0’ are not updated, and remain in OFF state.

- ***OR_CRL (0x1)***

OR_CRL command updates all of the ON-OFF states in the target STAx IC. Logical OR operation is performed on every Core with the input eight bit data, and each Core's ON-OFF state is updated with the logical operation result. The target STAx IC is specified by Chip-ID. Figure 4 shows an example for OR_CRL command.

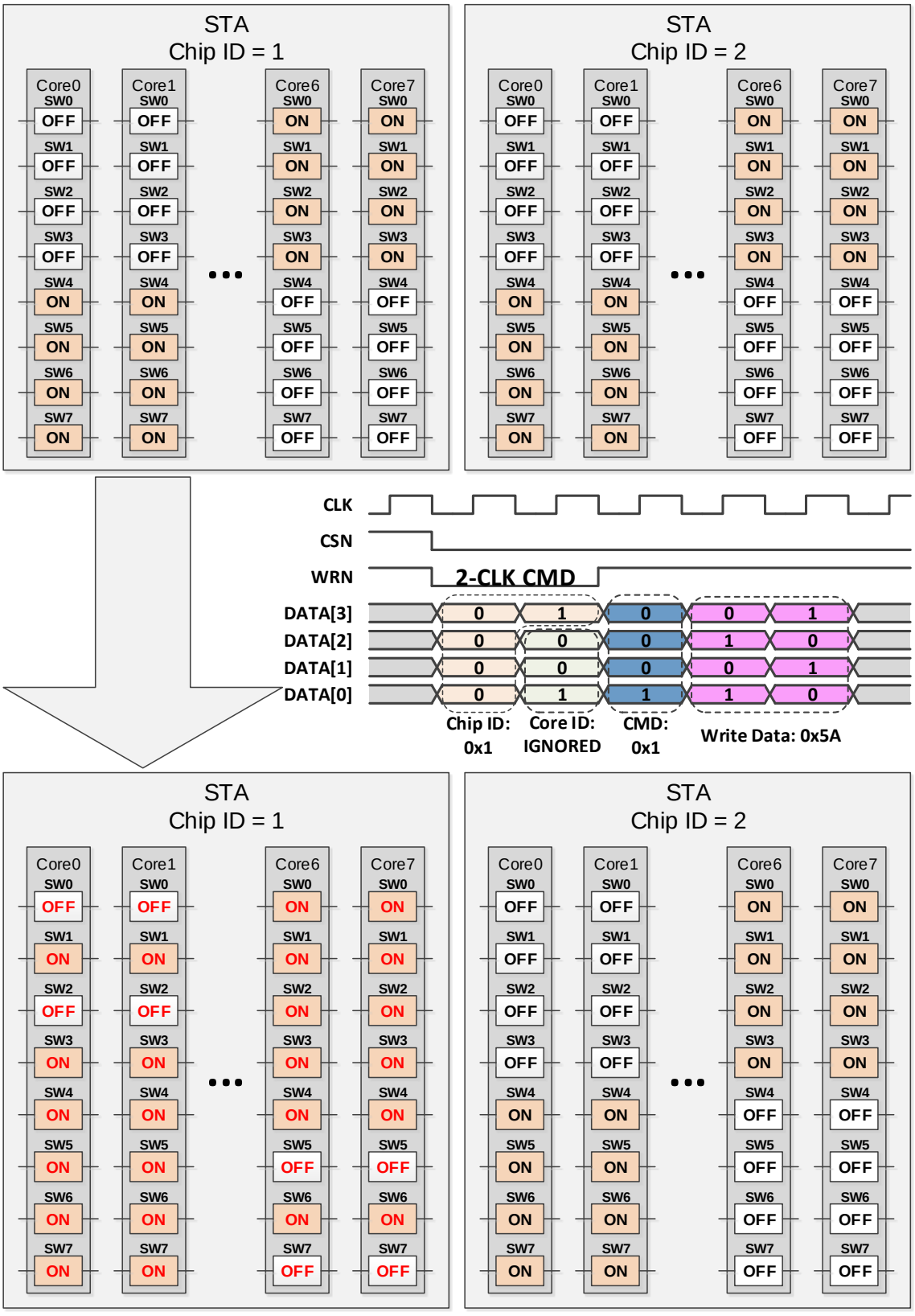

Figure 4. Example for OR_CRL Command.

In Figure 4, the input Chip-ID from the command is 0x1. Logical OR operation is performed with every Core of the STAx IC whose Chip-ID is 0x1, and the ON-OFF state is updated with the result of the logical operation. For the logical operation, ON is regarded as ‘1’, and OFF is as ‘0’. The Core-ID included in the command is ignored. Note that the switches whose REJECTn flags are set to ‘0’ are not updated, and remain in OFF state.

- ***DIRECT_CRL (0x2)***

DIRECT_CRL command changes all of the ON-OFF states in the target STAx IC. The input WData value is written to all Cores of the specified STAx IC. The target STAx IC is specified by Chip-ID. Figure 5 shows an example for DIRECT_CRL command.

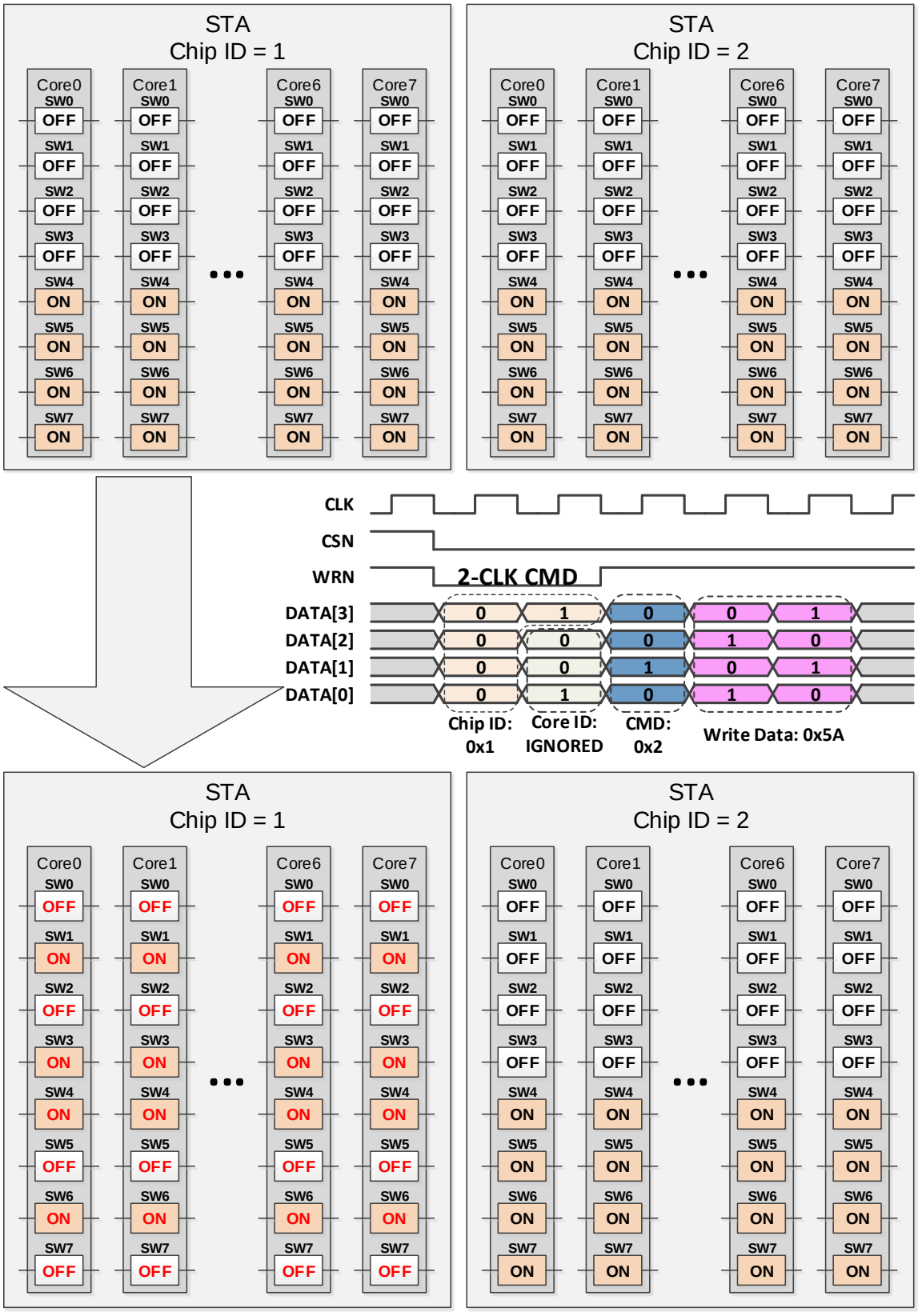

Figure 5. Example for DIRECT_CRL Command.

In Figure 5, the input Chip-ID from the command is 0x1. All Cores of the STAx IC whose Chip-ID is 0x1, is updated with the value of WData[7:0] (= 0xA5). The Core-ID included in the command is ignored. Note that the switches whose REJECTn flags are set to '0' are not updated, and remain in OFF state.

- ***DIRECT_CHL (0x3)***

DIRECT_CHL command changes all of the ON-OFF states in STAx ICs in the selected Bank. The input WData value is written to all Cores of the STAx ICs. Figure 6 shows an example for DIRECT_CHL command.

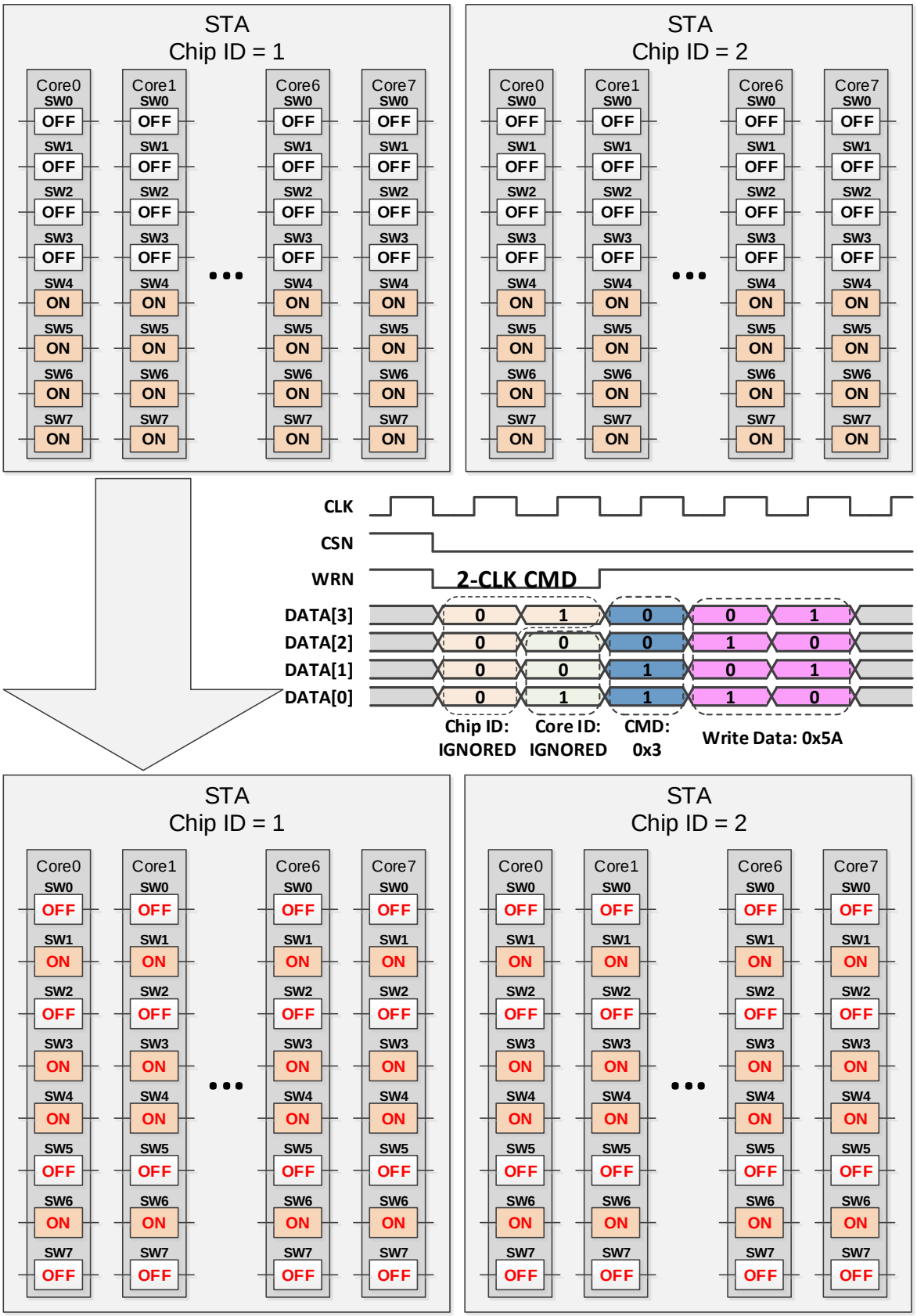

Figure 6. Example for DIRECT_CHL Command.

In Figure 6, WData[7:0] is written to all Cores of all STAx ICs in the Bank. Chip-ID and Core-ID are ignored. Note that the switches whose REJECTn flags are set to ‘0’ are not updated, and remain in OFF state.

- ***REJECT_CRL (0x4)***

REJECT_CRL command controls REJECTn flags of the specified STAx IC in Core unit. According to each bit's value of WData[7:0], it sets REJECTn flags of each Core's eight switches. Figure 7 shows an example for REJECT_CRL command.

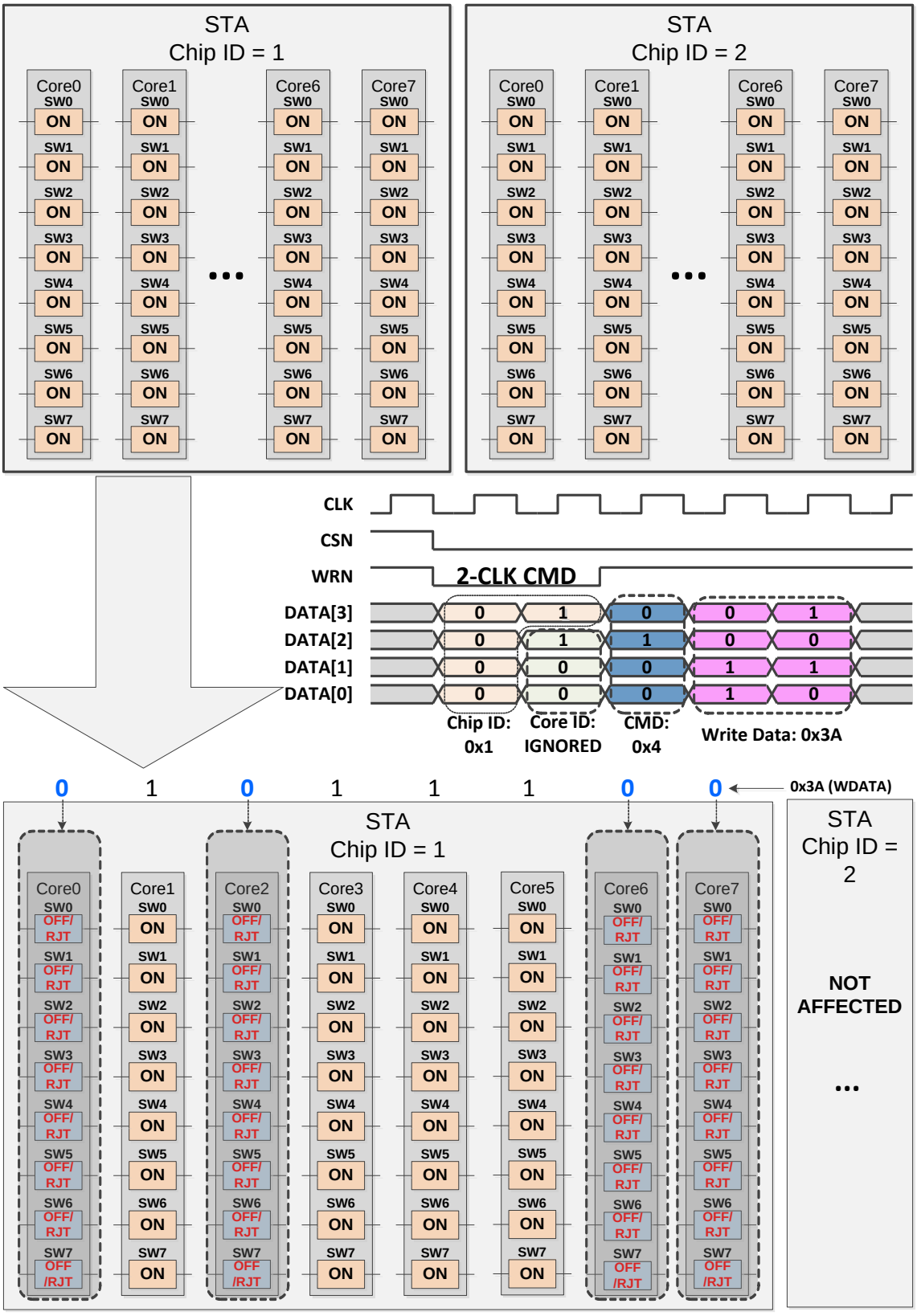

Figure 7. Example for REJECT_CRL Command.

In Figure 7, target STAx IC is selected by the Chip-ID (= the one with Chip-ID is 0x1). Each bit of WData decides REJECTn flags of each Core. From bit0 to bit7 of WData[7:0] corresponds to Core0 to Core7. Since bit0, bit2, bit6, and bit7 are '0's, REJECTn flags of Core0, Core2, Core6, Core7 are set to '0'.

Note that WData bit's value '1' does not mean 'Clear REJECT flag', but 'No Change'. Once REJECTn flags are set, they can be cleared only by INITIAL_ALL command or CANCEL_RJT command.

■ *AND_SWL (0x8)*

AND_SWL command updates the ON-OFF states of a Core in the target STAx IC. Logical OR operation is performed on a Core with the input eight bit data, and the target Core's ON-OFF state is updated with the logical operation result. The target STAx IC is specified by Chip-ID, and the target Core by Core-ID. Figure 8 shows an example for AND_SWL command.

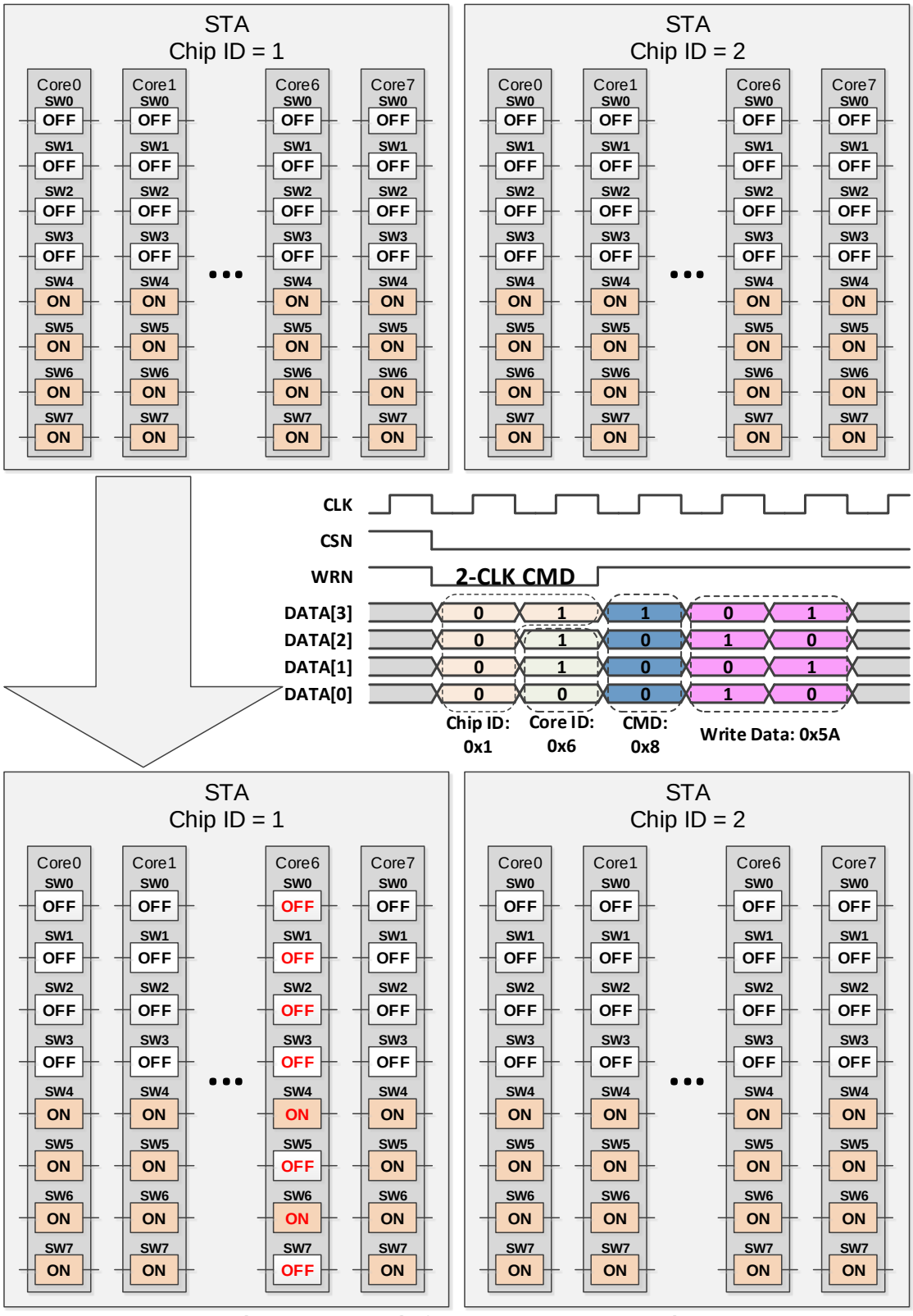

Figure 8. Example for AND_SWL Command.

In Figure 8, the input Chip-ID from the command is 0x1, and Core-ID is 0x6. According to the input Chip-ID and Core-ID, Core6 of the STAx IC whose Chip-ID is 0x1, is updated with the result of logical AND operation value. For the logical operation, ON is regarded as ‘1’, and OFF is as ‘0’. Note that the switches whose REJECTn flags are set to ‘0’ are not updated, and remain in OFF state.

- ***OR_SWL (0x9)***

OR_SWL command updates the ON-OFF states of a Core in the target STAx IC. Logical OR operation is performed on a Core with the input eight bit data, and the target Core's ON-OFF state is updated with the logical operation result. The target STAx IC is specified by Chip-ID, and the target Core by Core-ID. Figure 9 shows an example for OR_SWL command.

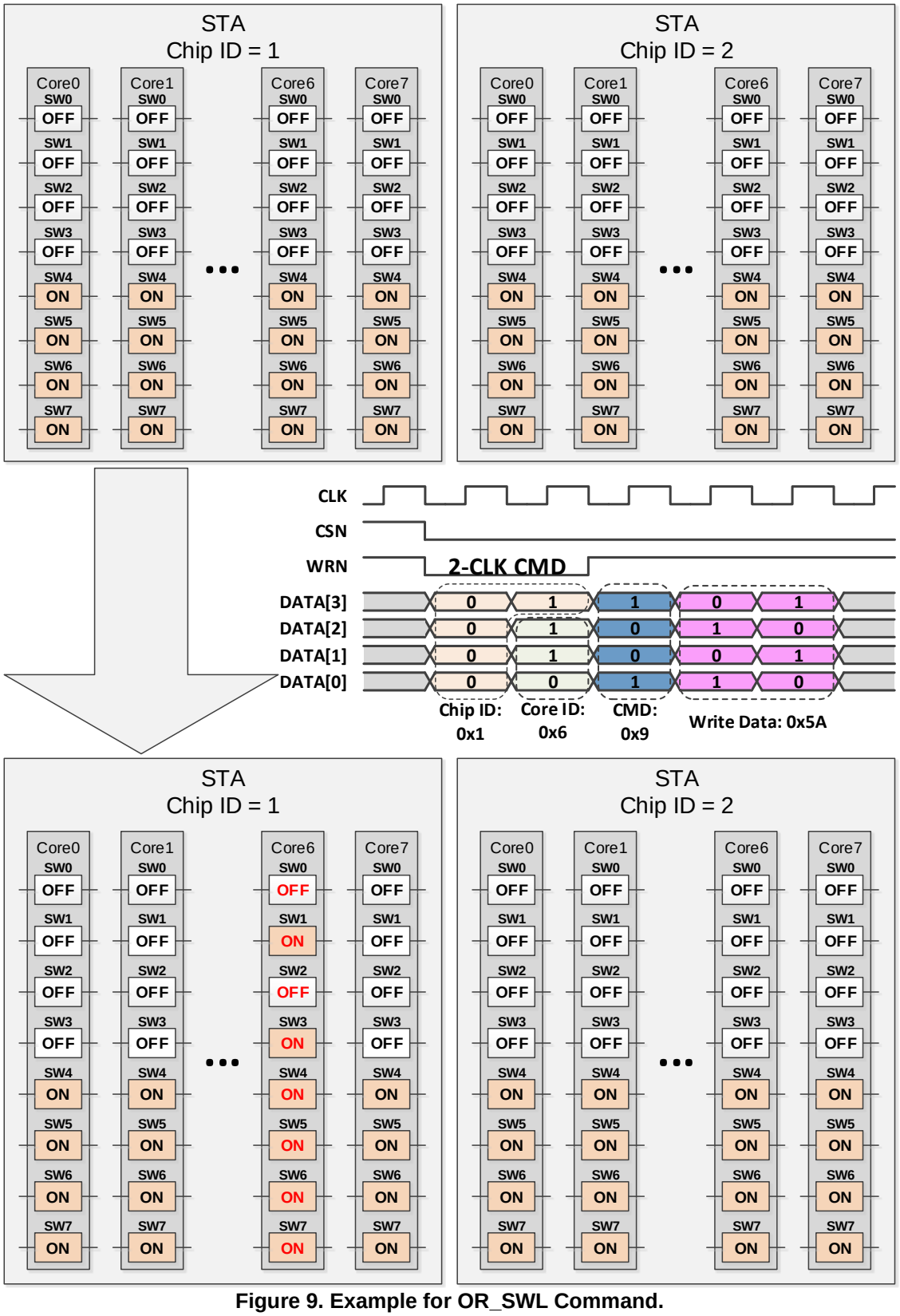

Figure 9. Example for OR_SWL Command.

In Figure 9, the input Chip-ID from the command is 0x1, and Core-ID is 0x6. According to the input Chip-ID and Core-ID, Core6 of the STAx IC whose Chip-ID is 0x1, is updated with the result of logical OR operation value. For the logical operation, ON is regarded as '1', and OFF is as '0'. Note that the switches whose REJECTn flags are set to '0' are not updated, and remain in OFF state.

- ***DIRECT_SWL (0xA)***

DIRECT_SWL command changes the ON-OFF states of a Core in the target STAx IC. The input WData value is written to the target Core of the specified STAx IC. The target STAx IC is specified by Chip-ID, and the target Core by Core-ID. Figure 10 shows an example for DIRECT_SWL command.

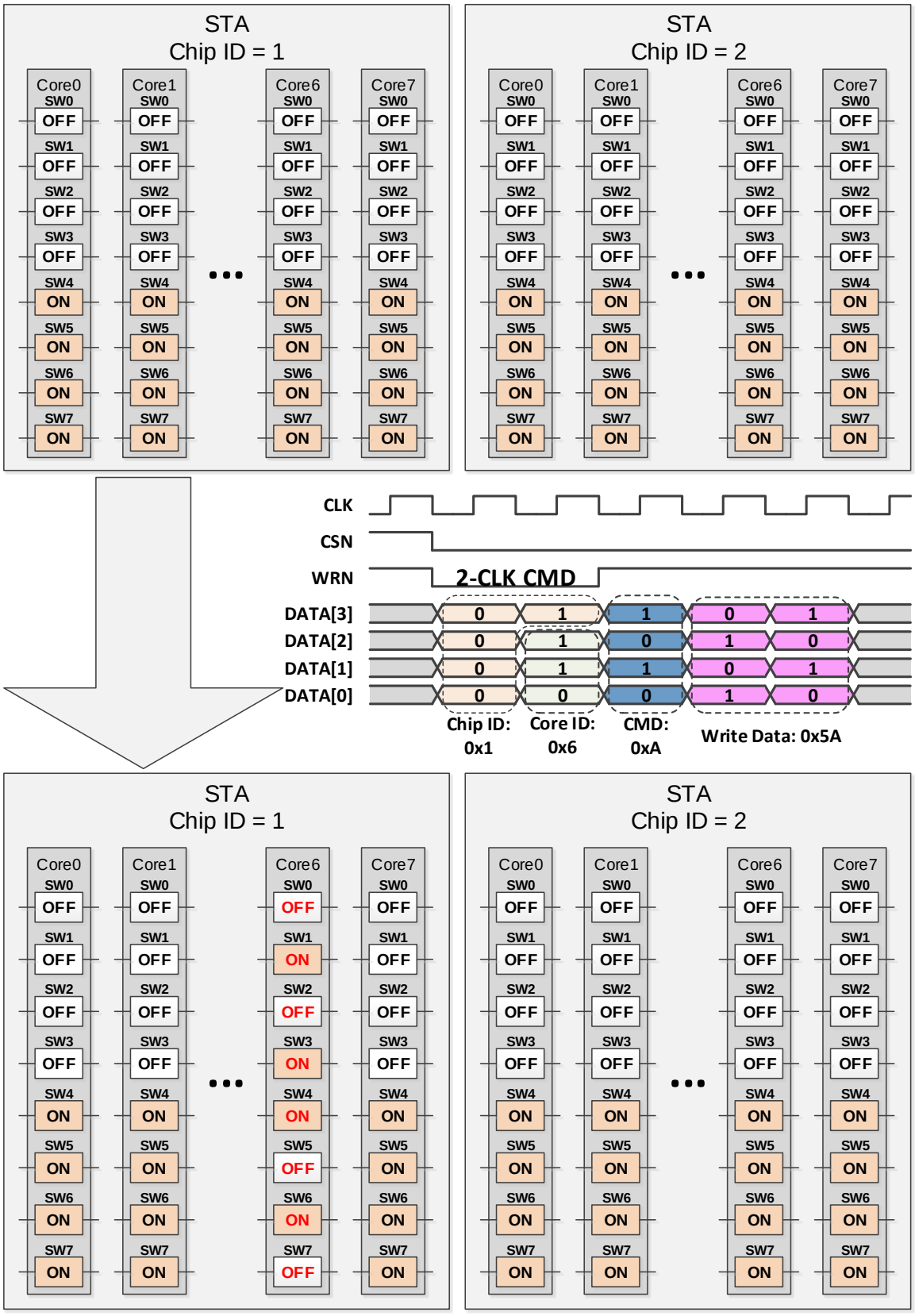

Figure 10. Example for DIRECT_SWL Command.

In Figure 10, the input Chip-ID from the command is 0x1, and Core-ID is 0x6. According to the input Chip-ID and Core-ID, Core6 of the STAx IC whose Chip-ID is 0x1, is updated with the value of WData[7:0] (= 0xA5). Note that the switches whose REJECTn flags are set to '0' are not updated, and remain in OFF state.

- ***REJECT_SWL (0xC)***

REJECT_SWL command updates REJECTn flags of the specified Core. It receives Chip-ID and Core-ID, and uses them to specify the target Channel in the target STAx IC. According to each bit's value of WData[7:0], it sets REJECTn flags of each switch of the selected Core. Figure 11 shows an example for REJECT_SWL command.

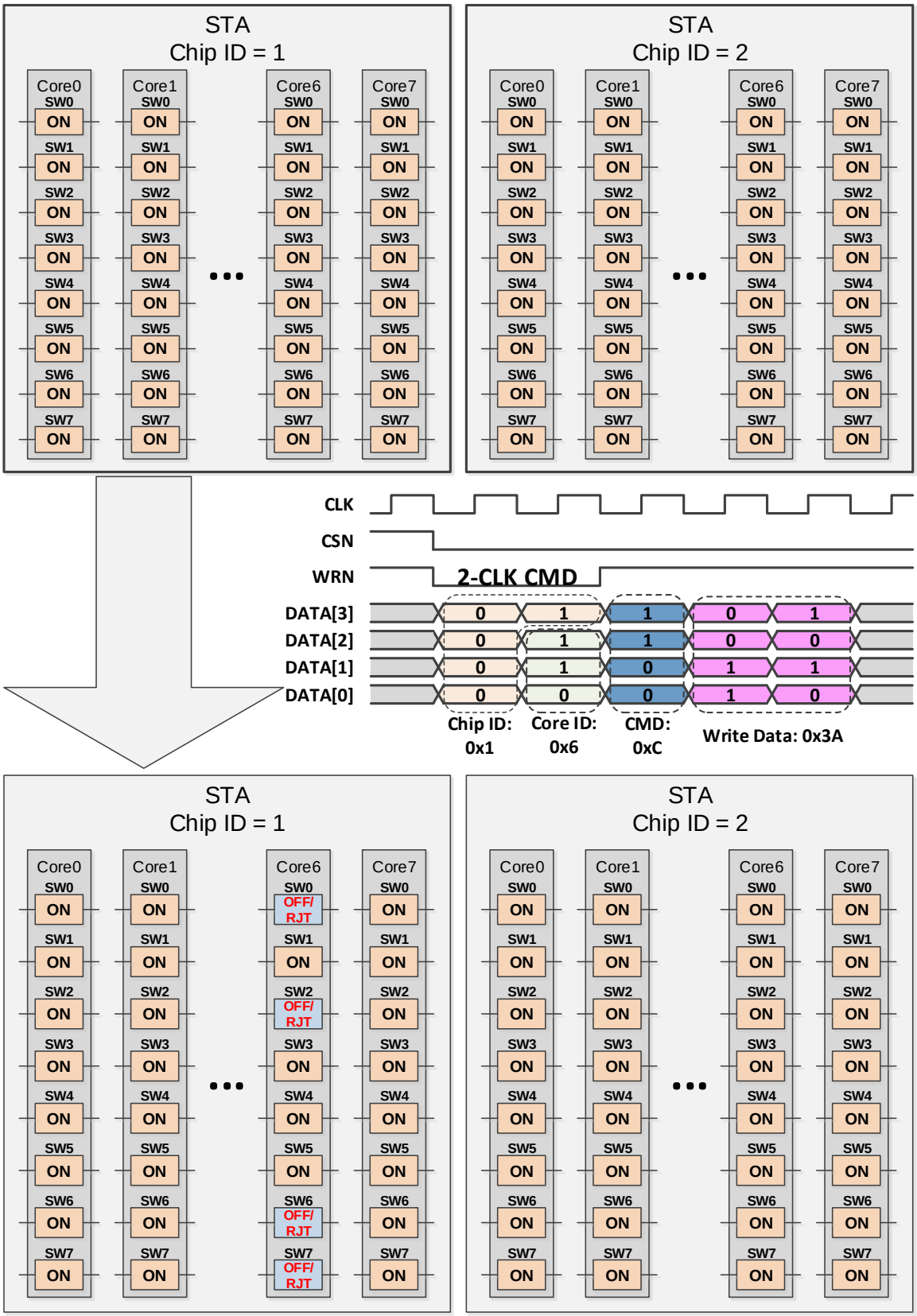

Figure 11. Example for REJECT_SWL Command.

In Figure 11, since Chip-ID is 0x1, the one with Chip-ID is 0x1 is selected as the target (i.e. the one with Chip-ID = 0x2 is not affected). Core-ID (= 0x6) specifies the target Core as Core6.

WData[7:0] contains the actual update value of REJECTn flags. If a bit of WData is '0', it indicates that the corresponding switch's REJECTn flag should be set to '0'. In Figure 11, WData is 0x3A, and bit7, bit6, bit2, bit0 of WData are ZERO. Since even numbered bits control two switches including odd numbered switches, it results in that REJECTn flags of switch7, switch6, switch3, switch2, switch1, and switch0 are set to '0'. ON-OFF states of those switches are also set to OFF.

Note that WData bit's value '1' does not mean 'Clear REJECT flag', but 'No Change'. Once REJECT flags are set, they can be cleared only by INITIAL_ALL command or CANCEL_RJT command.

■ *CANCEL_RJT (0xD)*

CANCEL_RJT command sets REJECTn flags of a Core of the specified STAx IC to '1', which recovers the ON-OFF states of the switches to the previous states. Figure 12 shows an example for CANCEL_RJT command.

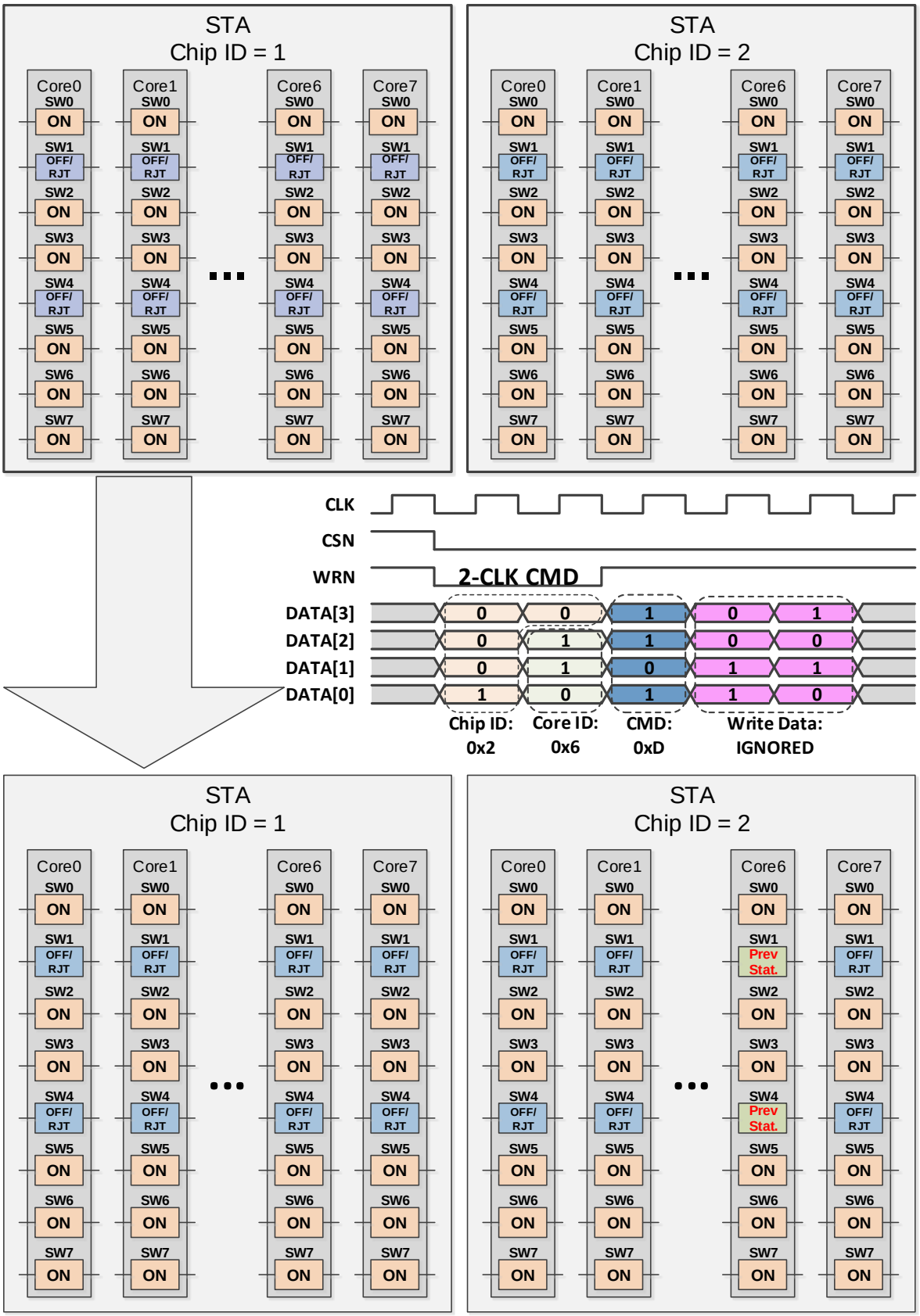

Figure 12. Example for CANCEL_RJT Command.

The ON-OFF states of the switches are internally preserved even though REJECT_CRL / REJECT_SWL commands are executed. However, REJECTn flag of each switch masks out the ON-OFF states, and it is seen as OFF outside if corresponding REJECTn flag is set to ‘0’. By executing CANCEL_RJT command, the REJECTn flag is set to ‘1’, and the ON-OFF states are seen as they are outside.

In Figure 12, the target STAx IC and target Core are specified by Chip-ID (= 0x2) and Core-ID (= 0x6). Core6 of the STAx IC whose Chip-ID is 0x6 is selected as the target, and its REJECTn flags are set to ‘1’ by CANCEL_RJT command. By setting REJECTn flags to ‘1’, the ON-OFF states are changed to the PREVIOUS STATES. If the switch was ON before setting its REJECTn flag to ‘0’, its ON-OFF state is changed to ON. If it was OFF, the state still remains in OFF. Note that WData is ignored, and all REJECTn flags in the target Core are set to ‘1’.

REVISION HISTORY

Revision	Date	Description
0.0	2015-10	Initial draft

DOCUMEN INFORMATION

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The world is driven by analog

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