PS2064 Datasheet

64-Channel CMOS Analog Switch IC

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Preliminary

The world is driven by analog

GENERAL DESCRIPTION

The PS2064 is a monolithic CMOS device containing 64 independently selectable switches. These switches are fabricated with an advanced submicron CMOS process that provides low power dissipation, low on resistance, low leakage currents, and high signal bandwidth. The PS2064 is designed to operate in 3.3V for digital circuits and 5V for analog switches. Each switch can operate with a wide input and output voltage range. In addition, the thermal shutdown function will automatically turn off the channel temperature exceeds 150°C. The off-leakage current is no more than 50nA at room temperature of 25°C.

All digital input pins adopt the Schmitt trigger I/O, which has 1.0-V to 2.3-V input noise margin to ensure TTL/CMOS-logic compatibility when using a 3.3-V power supply.

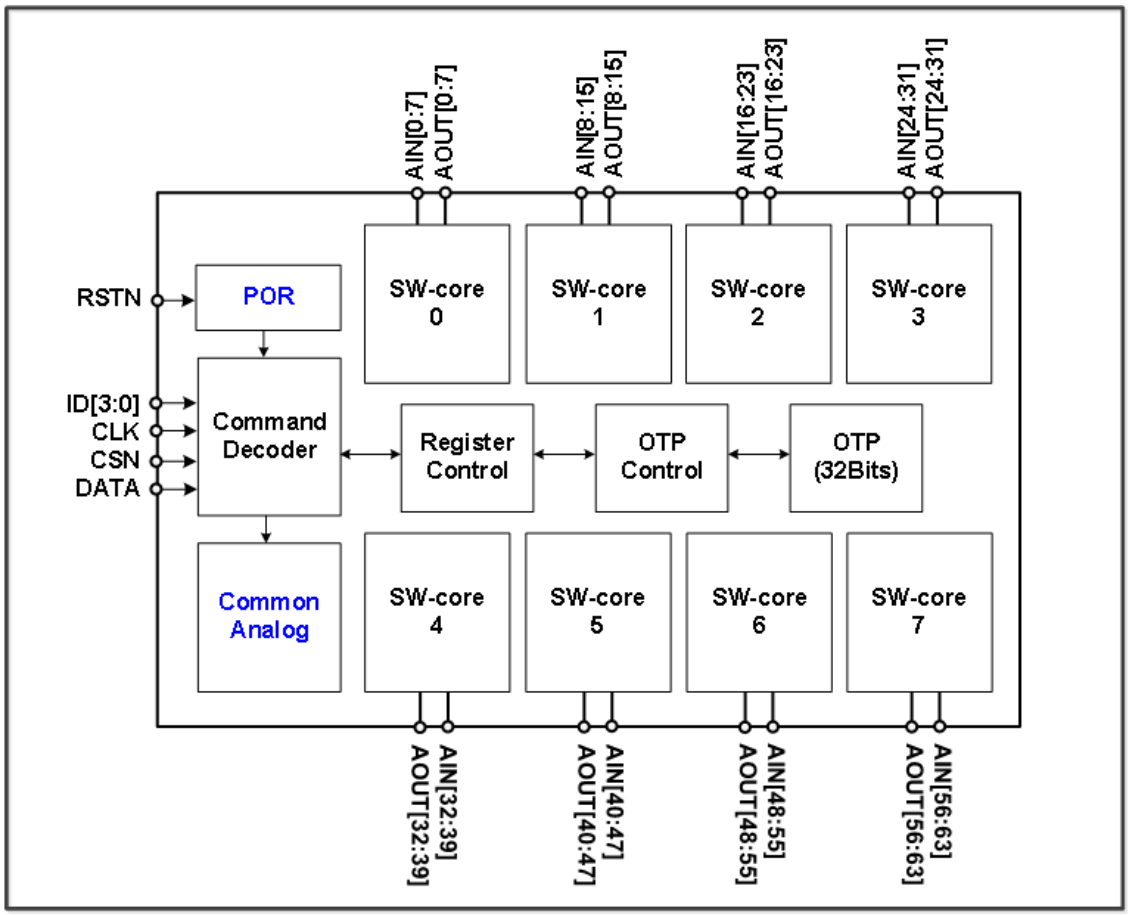
FEATURE

3.3V logic-compatible input (V_{IH}=2.3V, V_{IL}=1.0V)
Dual supply operation: 3.3V for digital, 5V for analog.
Analog signal frequency: DC-to-1MHz
Low on-resistance: 1Ω (@typ)
Wide range analog input from -1.5V to 7V (@max)
Multi-channel switch control
Switching control using CMOS interface command
117-pin FC-FBGA package

APPLICATIONS

Data-acquisition systems
Mechanical reed-relay replacement
Communication systems

FUNCTIONAL BLOCK DIAGRAM



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PIN MAPPING TABLE

PS2064(Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	DVDD	AOUT0	AOUT1	AOUT2	DATA	CLK	CSN	RSTN	AOUT61	AOUT60	AOUT56	AOUT55	AVDD	A
B	DVDD	AOUT6	AOUT7	AOUT3	AIN2	AIN3	AOUT63	AOUT62	AOUT59	AOUT58	AOUT57	AOUT54	AOUT53	B
C	AOUT4	AOUT5	AIN0	AIN1	AIN4	AIN6	AIN60	AIN56	AIN54	AIN52	AOUT51	AOUT50	AOUT52	C
D	AOUT8	AOUT10	AIN8	AIN9	AIN10	AIN11	AIN62	AIN58	AIN50	AIN48	AOUT47	AOUT49	AOUT48	D
E	AOUT9	AOUT11	AOUT18	AIN12	AIN14	AIN26	AIN43	AIN42	AIN46	AIN44	AOUT46	AOUT45	AOUT44	E
F	AOUT12	AOUT14	AOUT19	AIN18	AIN22	AIN30	AIN32	AIN33	AIN41	AIN40	AOUT43	AOUT41	AOUT40	F
G	AOUT13	AOUT15	AOUT23	AIN16	AIN20	AIN24	AIN28	AIN34	AIN35	AIN38	AOUT42	AOUT37	AOUT36	G
H	AOUT16	AOUT17	AOUT22	AOUT25	AOUT26	AOUT27	AOUT29	AOUT30	AOUT31	AIN36	AOUT39	AOUT38	AOUT35	H
J	DVSS	AOUT20	AOUT21	AOUT24	ID[0]	ID[1]	ID[2]	ID[3]	AOUT28	AOUT32	AOUT33	AOUT34	AVSS	J
	1	2	3	4	5	6	7	8	9	10	11	12	13	

PIN DESCRIPTIONS

PIN NAME	I/O	Descriptions
CLK	DI	System clock
RSTN	DI	System reset. Active Low
CSN	DI	Chip select. Active Low
DATA	DI	Data
ID[3:0]	DI	ID assign pin(PID)
AIN	AI	40 analog switch inputs
AOUT	AO	64 analog switch outputs
AVDD	PWR	Analog Power
AVSS	GND	Analog Ground
DVDD	PWR	Digital Power
DVSS	GND	Digital Ground

AI: analog input **AO: analog output**
DI: digital Input
PWR: power **GND: ground**

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND, Unless Otherwise Noted.)

AVDD (for Analog Switch).....-0.3V to +6V
DVDD (for Digital Control).....-0.3V to +4.5V
Voltage at any digital pin .....-0.3V to +4.5V
Voltage at any analog pin ……- 0.3V to +6V
Continuous current into any terminal 100mA
Peak current into analog switch I/O…….....150mA
(Current pulse with 1ms and 10% duty cycle)

Operating temperature range .....-40°C to +125°C
Storage temperature range .....-55°C to +150°C
Junction temperature.....+150°C
ESD protection on all pins (HBM, MM)……≥2kV, 200V

Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at those or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

AVDD=5.0V, AVSS=-1.5V, DVDD=3.3V, DVSS=0V, and TA = +25°C/+125°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
POWER SUPPLIES							
Analog Supply Voltage		AVDD		4.5	5	5.5	V
Digital Supply Voltage		DVDD		3.0	3.3	3.6	V
Analog Ground Voltage		AVSS		-2	-1.5	0	V
Digital Ground Voltage		DVSS		-	0	-	V
ANALOG SWITCH							
Input Signal Range		V_{AIN}	AVSS= -1.5V, AVDD= 5V	-1.5		7	V
Channel On Current		I_{CH_ON}	AVDD=5V			100	mA
Switch On-resistance		R_{ON}	I_{CH_ON}=10mA		1	2	Ω
Leakage Current	Source Off Leakage Current	I_{S_OFF}	AVDD= 5V, AVSS= −1.5V V_{AIN}= 5, V_{AOUT}= 0V		15	20	nA
	Drain Off Leakage Current	I_{D_OFF}	AVDD= 5V, AVSS= −1.5V V_{AIN}= 0V, V_{AOUT}= 5V		15	20	nA
	Channel On Leakage Current	I_{CH_ON}	AVDD= 5V, AVSS= −1.5V V_{AIN}= 0V or 5V		10	20	nA

ELECTRICAL CHARACTERISTICS (Continued)

AVDD=5.0V, AVSS=-1.5V, DVDD=3.3V, DVSS=0V, and TA = +25°C/+125°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
DIGITAL I/O							
Logic Input Voltage	Input High	V_{IH}		0.7* DVDD			V
	Input Low	V_{IL}				0.3* DVDD	V
Logic Input Current	Input High	I_{IH}		-1		1	uA
	Input Low	I_{IL}		-1		1	uA
SWITCH DYNAMIC CHARACTERISTICS							
Switching Time	Turn ON Time	t_{ON}	Clock base (calculate for special condition)		175		ns
	Turn OFF Time	t_{OFF}			235		ns
Capacitance	Input Off-Capacitance	C_{AIN_OFF}			150		pF
	Output Off-Capacitance	C_{AOUT_OFF}			150		pF
	Output On-Capacitance	C_{AOUT_ON}			300		pF
Switching Frequency		f_{SW}				1.25	MHz

POWER CONSUMPTION							
Analog Operating Current (AVDD)	Static	I_{AVDD_ST}	AVDD= 5V, AVSS= -1.5V		4	6	mA
	Dynamic	I_{AVDD_DYN}	AVDD= 5V, AVSS= -1.5V, f_{SW}= 10KHz,		5	6	mA
Analog Operating Current (AVSS)	Static	I_{AVSS_ST}	AVDD= 5V, AVSS= -1.5V		4	6	mA
	Dynamic	I_{AVSS_DYN}	AVDD= 5V, AVSS= -1.5V, f_{SW}= 10KHz,		5	6	mA
Digital Operating Current (DVDD)	Static	I_{DVDD_ST}	DVDD= 3.3V		4	5	mA
	Dynamic	I_{DVDD_DYN}	DVDD= 3.3V, f_{CLK}= 10MHz, Combined operation of Reset, and DUT-Reject		5	6	mA
	Dynamic	I_{DVDD_DYN}	DVDD= 3.3V, f_{CLK}= 25MHz, Combined operation of Reset, and DUT-Reject		6	7	mA

TIMING CHARACTERISTICS

AVDD=5.0V, AVSS=-1.5V, DVDD=3.3V, DVSS=0V, and TA = +25°C/+125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
DIGITAL I/O SIGNALS						
CLK Period	t_{PERIOD}		40			ns
CLK Frequency	f_{CLK}			10	25	MHz
DATA to CLK Setup Time	t_{DS}		10			ns
DATA to CLK Hold Time	t_{DH}		5			ns
CSN to CLK Setup Time	t_{CS}		10			ns
CSN to CLK Hold Time	t_{CH}		5			ns
POWER AND RESET SEQUENCE						
Power-up Period	t_{PU}		500			us
Power-down Period	t_{PD}		500			us
Power-on Reset Time	t_{RST}		500			us
OTP(ID number) Read Time	t_{ORD}	CLK freq. >= 10MHz	200			us
		CLK freq. < 10MHz	2000			cycle
SWITCH ON/OFF TIMING DIAGRAM						
Command Control Time	t_{SW1}				32	cycle

Timing Diagram of Digital I/O Signals

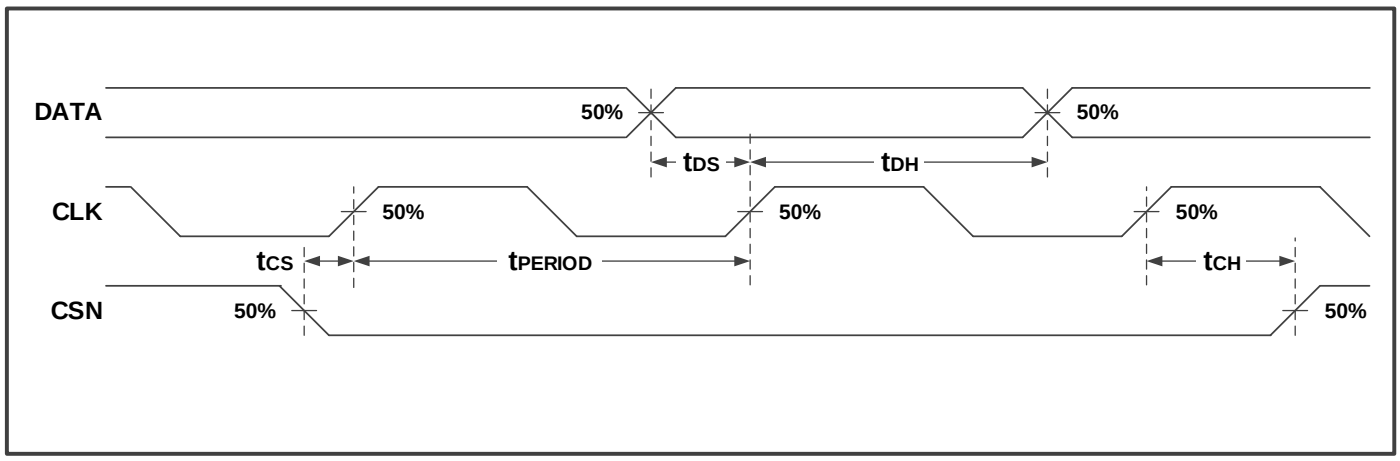


Figure 1. Timing Diagram of Digital Signals.

Power and Reset sequence

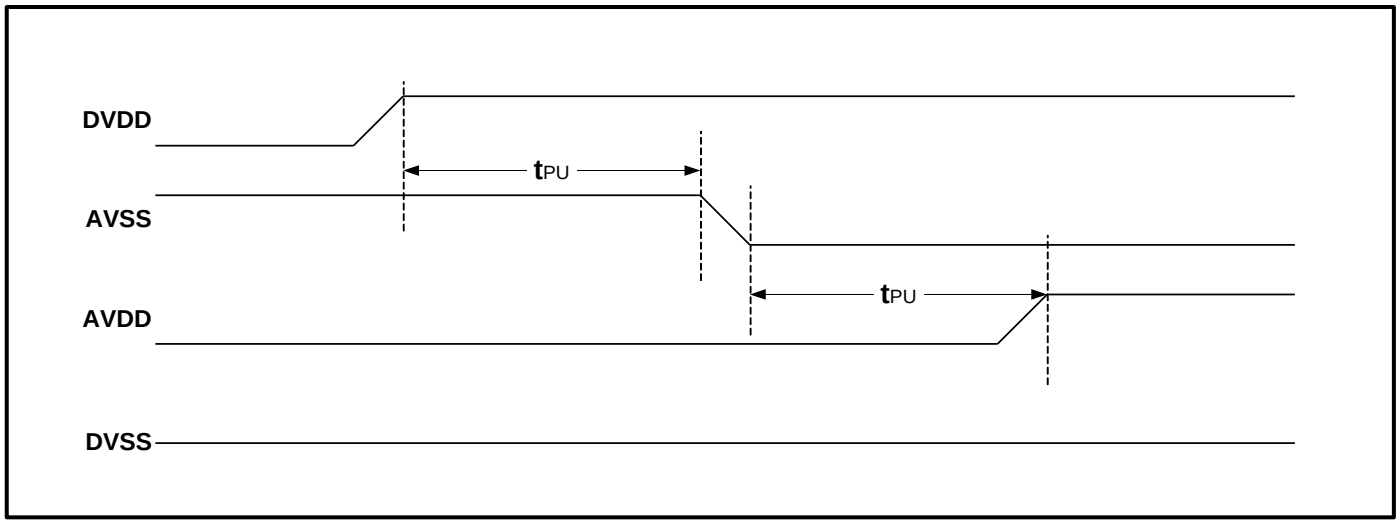


Figure 2. Power-up Sequence.

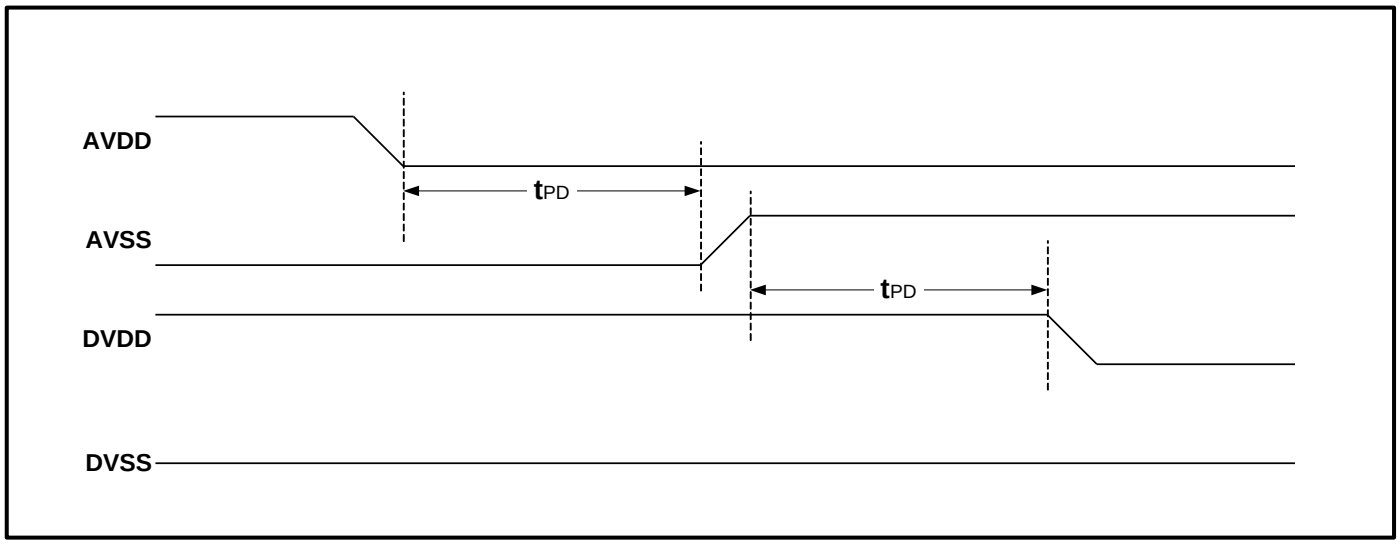
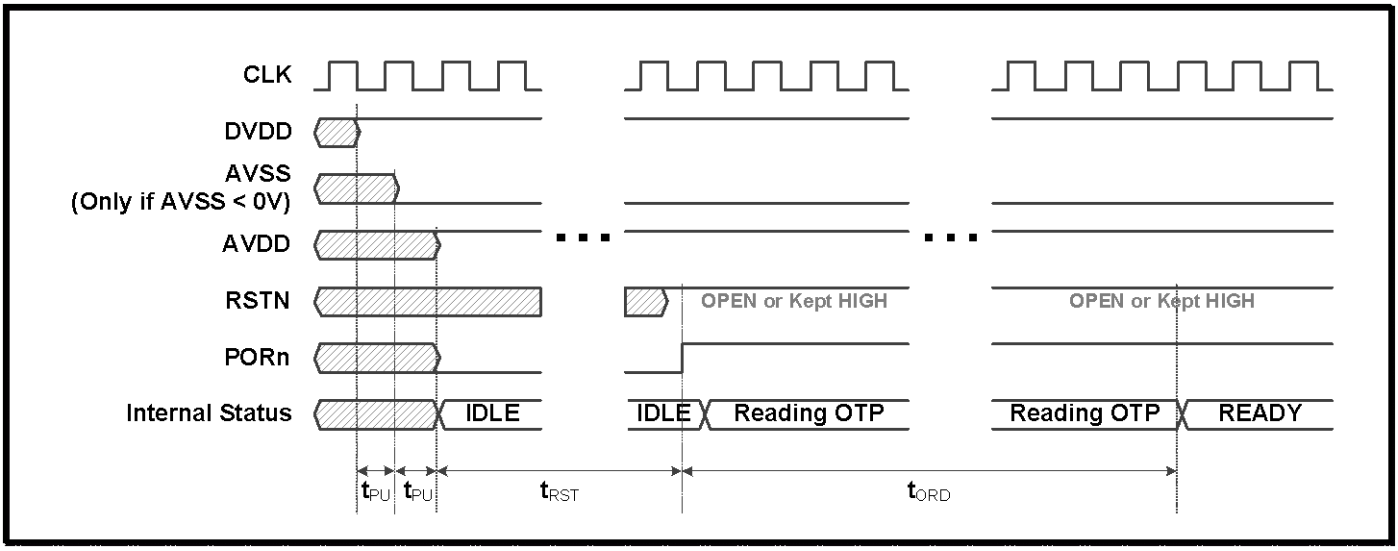
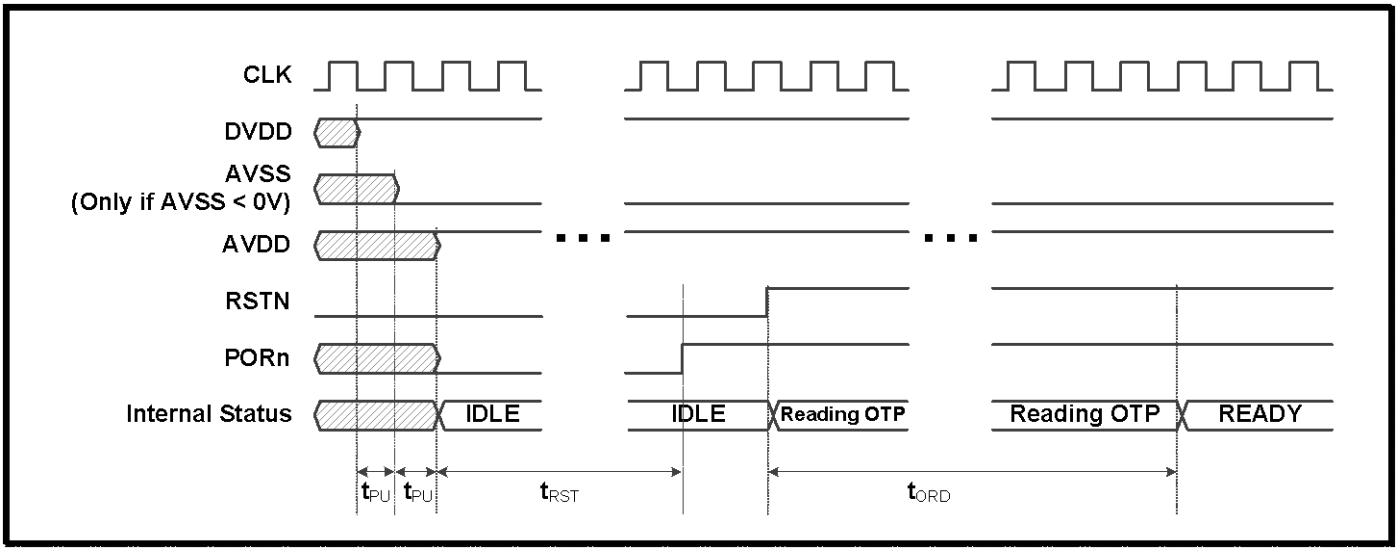


Figure 3. Power-down Sequence.



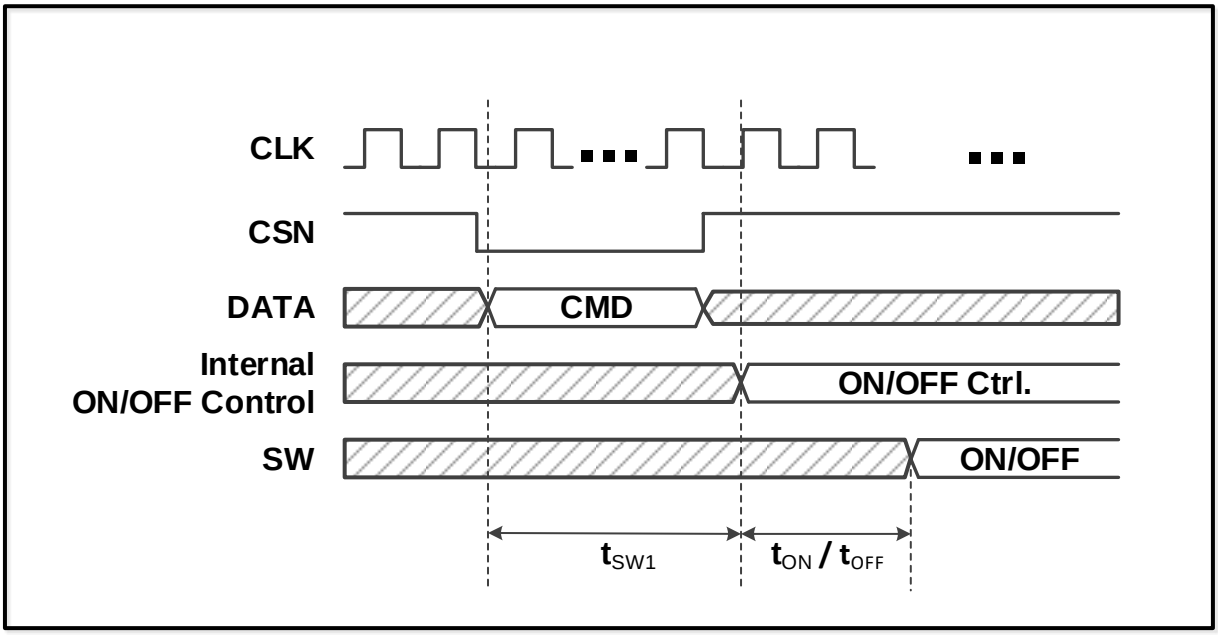
(a) In case RSTN is OPEN or kept HIGH before (t_{PU} + t_{PU} + t_{RST}).



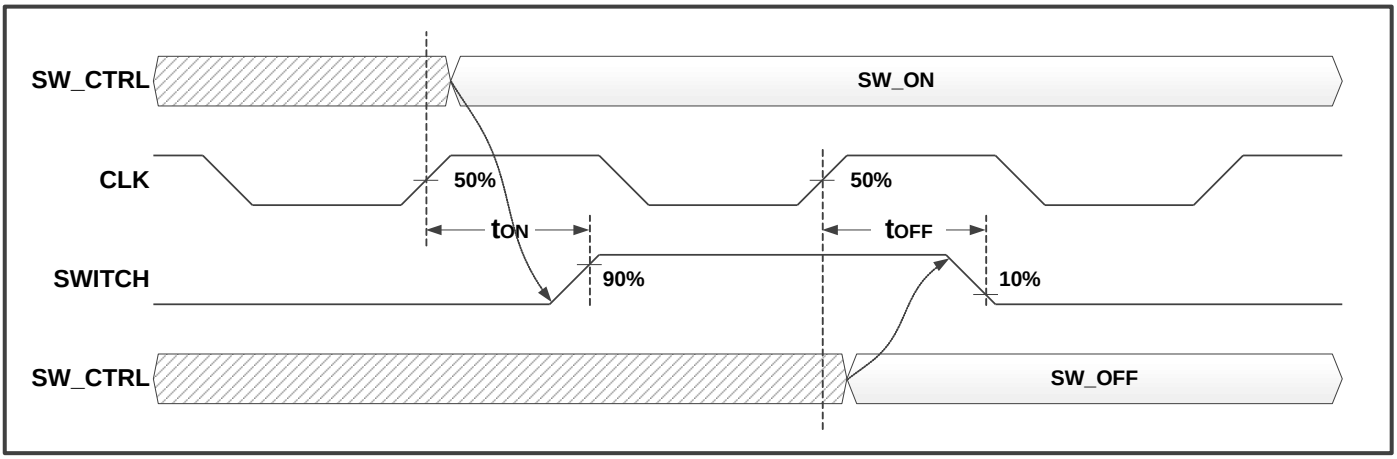
(b) In case RSTN changes from LOW to HIGH after (t_{PU} + t_{PU} + t_{RST}).

Figure 4. Reset and Stand-by Sequence.

Switch On/Off Timing Diagram



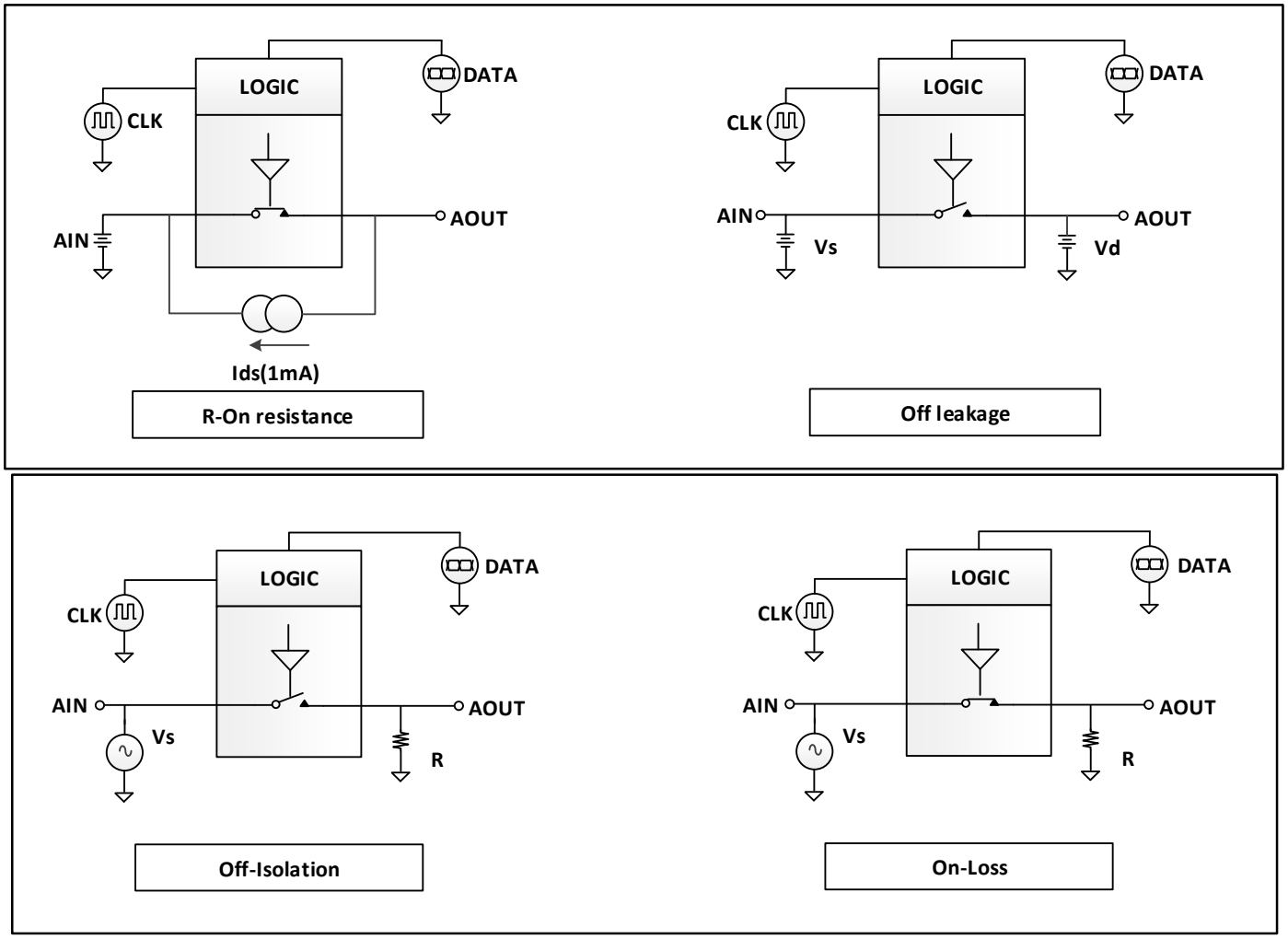
(a) command switch on/off timing diagram.



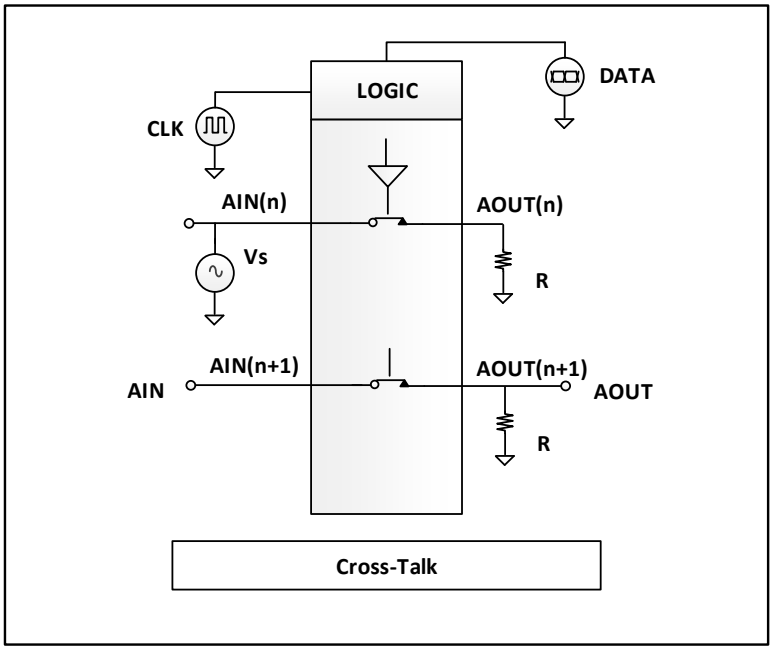
(b) Detail t_{ON} / t_{OFF} timing diagram.

Figure 5. Switch On/Off Timing Diagram.

TEST CIRCUITS



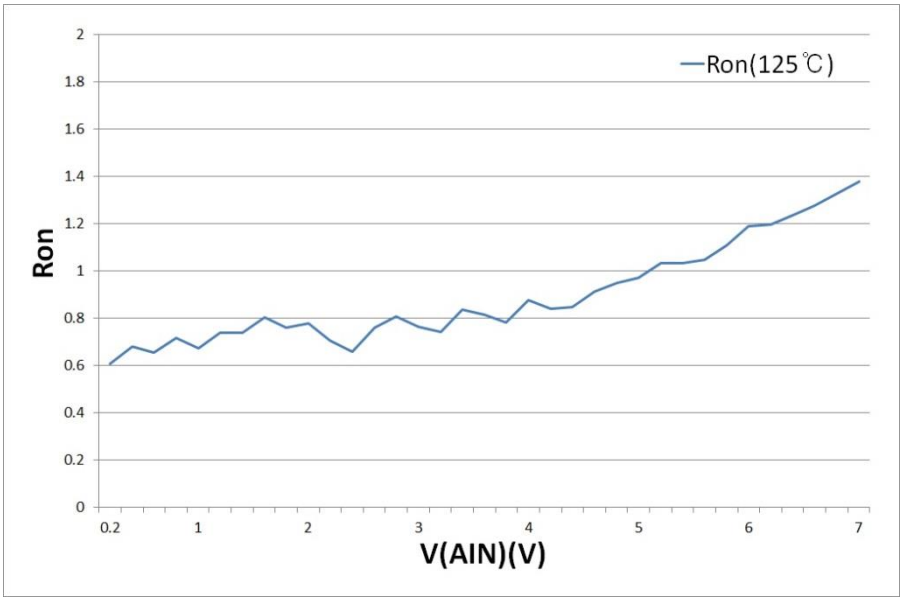
Off isolation=20log(V_{AOUT}/V_{AIN}), On Loss=20log(V_{AOUT}/V_{AIN})



Cross-Talk=20log*V($AOUT_{(n+1)}$)/V($AIN_{(n)}$)

Figure 6. Test Circuits.

TEST RESULTS



On-resistance(125℃) vs. vain

Figure 7. Test Results.

FUNCTIONAL DESCRIPTION

Internal Structure

PS2064 is analog switches with control logic. It consists of 8 switching Cores and control logics. Since each switching Core has 8 switches, a PS2064 contains 64 switches. Each switch has an ID from 0 to 7.

The switches in PS2064 can also be grouped into Channels. A Channel indicates the switches of the same ID in all cores. For example, Channel1 indicates Switch1s in Core0, Core1, Core2, …, and Core7. The host can control the switches either by Cores or Channels. Figure 8 shows the internal structure of Cores, Channels, and Switches.

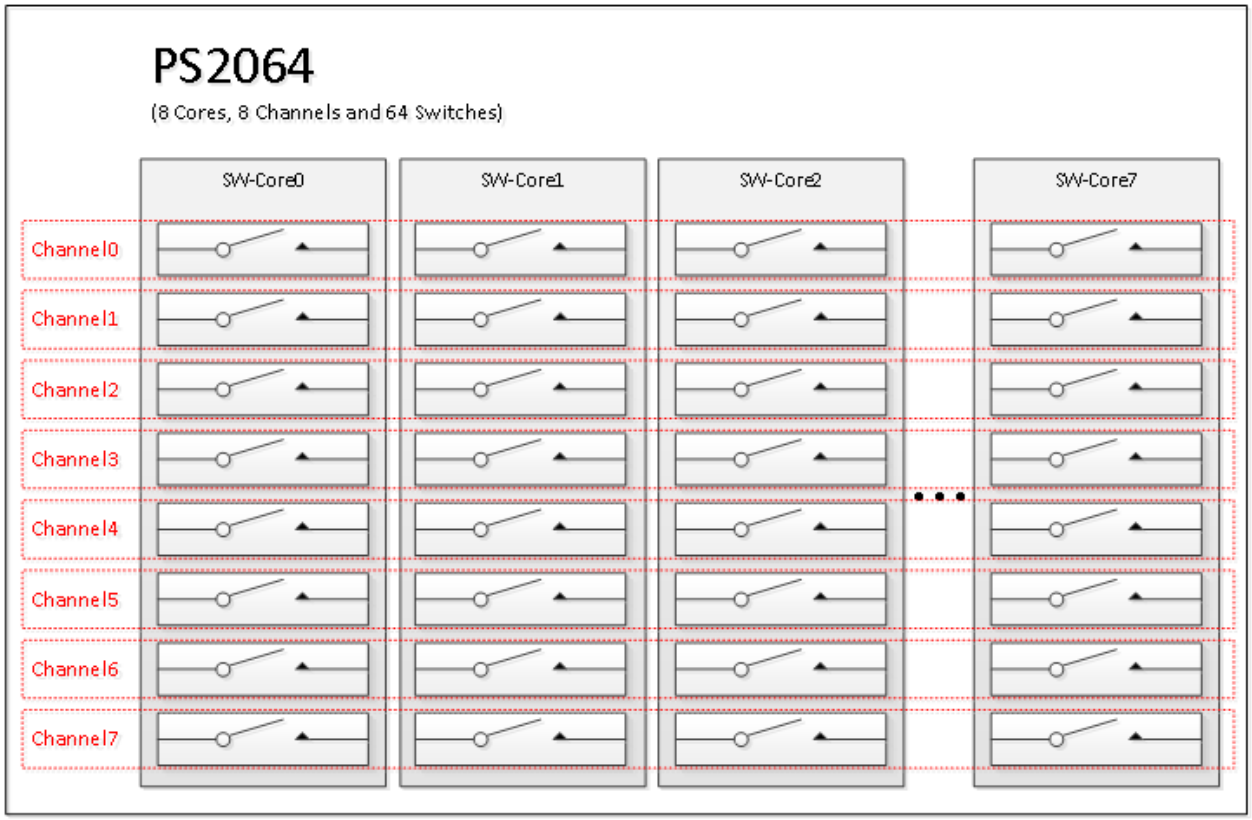


Figure 8. Internal Structure of PS2064.

The input pins of switches in each Core are connected all together to achieve 40-in 64-out operation. Figure 9 shows how the AIN / AOUT pins are connected to each switches.

As depicted in Figure 9, switches share the input pin, AIN.

Core0, Core1, Core4, Core5 has 4 unshared and 2 shared input signals.
Core2, Core3, Core6, Core7 has 4 shared input signals.

For example, in SW-Core0, each AIN0 and AIN1 is for single output signal. AIN0 connected to AOUT0 and AIN1 connected to AOUT1.
But AIN4 and AIN6 shares 2 outputs. AIN4 connected to AOUT4/AOUT5 and AIN6 connected to AIN6/AIN7.
SW-Core2 is AIN16, AIN18, AIN20, AIN22 shares 2 outputs. AIN16 connected to AOUT16/AOUT17 and AIN18 connected to AOUT18/AOUT19.

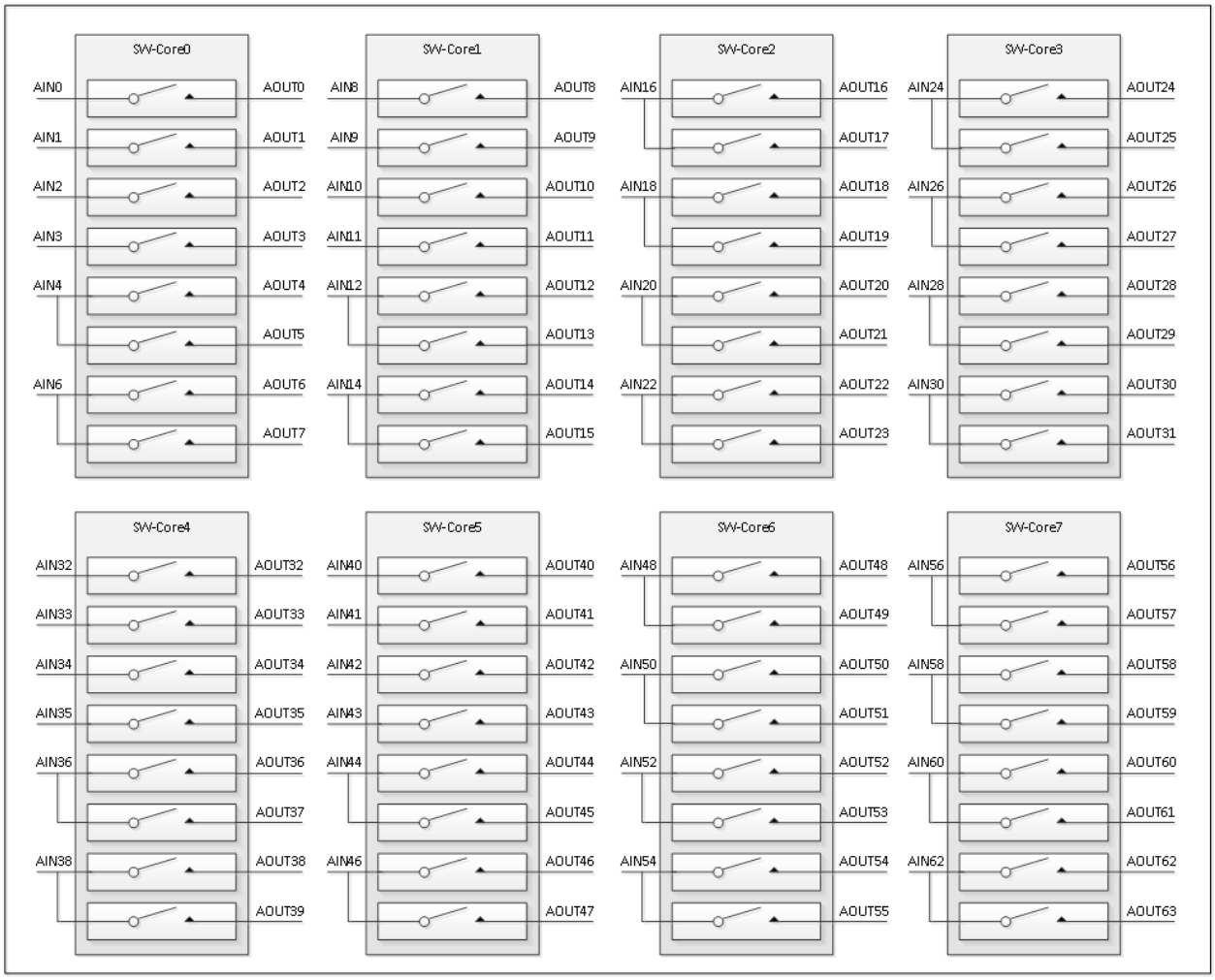


Figure 9.PS2064 Pin Sharing Block Diagram.

Connection

In system application, control signals can be shared among multiple PS2064s. Figure shows an example for the connection of multiple PS2064s.

PS2064s with the same control signals are called Bank. Since there are multiple PS2064s in a Bank, there should be a way to specify the target chip for the control commands. To support this, Pin-ID is used.

ID is a 4-bit number decided either from the external Pin-ID[3:0]. Each PS2064 acquires its Pin-ID on bootstrap, and user can specify the target chip of the control commands by sending target Pin-ID with them. Since Pin-ID is a 4-bit number, the maximum number of PS2064s in one bank is 16.

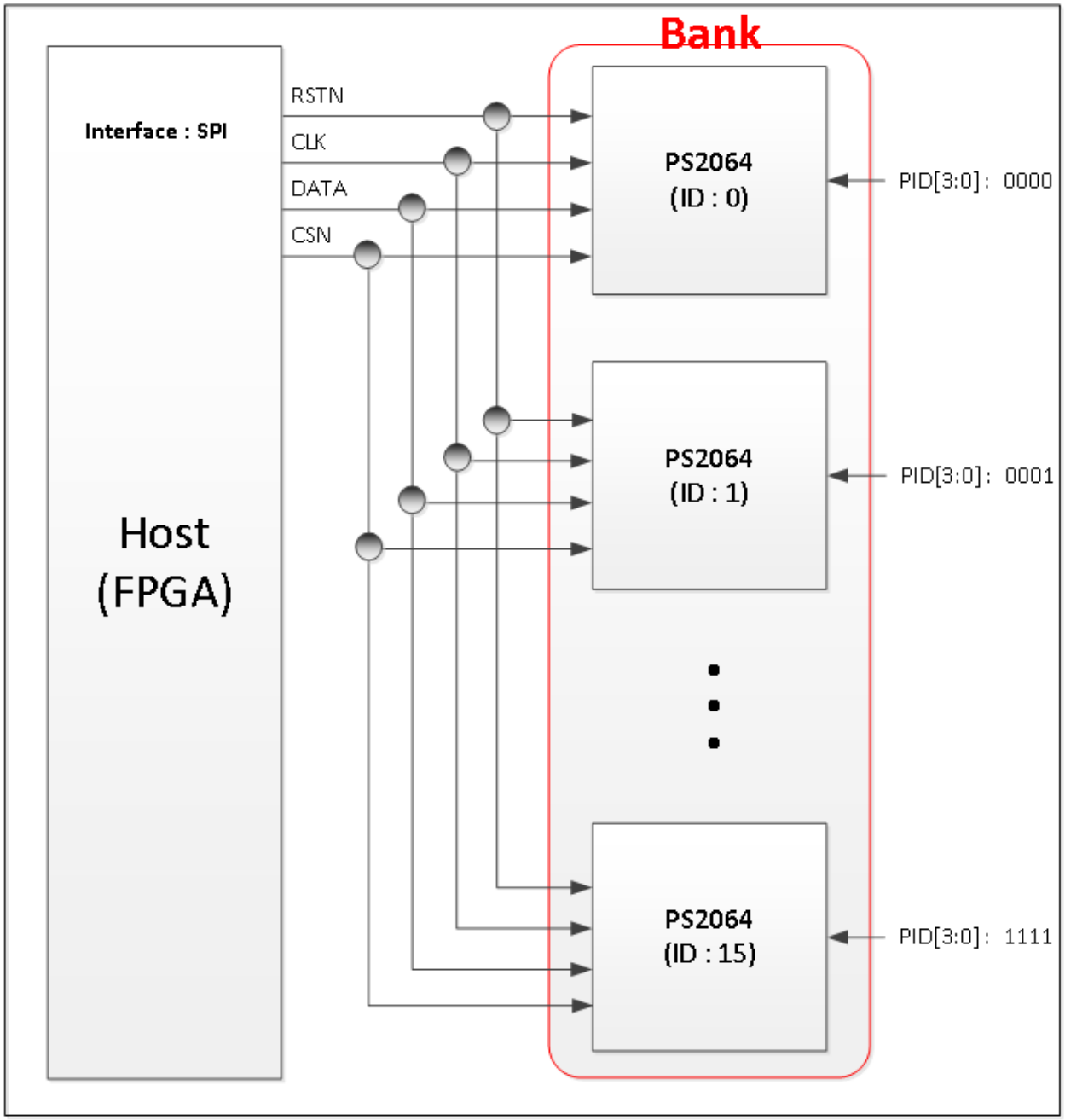


Figure 10. Example for connecting PS2064s.

Power-up Sequence

PS2064 requires two kinds of Power/Ground pairs – AVDD/AVSS and DVDD/DVSS. As the names imply, AVDD/AVSS pair is for Analog circuits, and DVDD/DVSS pair is for Digital logic. To ensure reliable operation on power-up, it is required that each Power and Ground should be provided in proper order. Figure 91 shows the Power-up sequence of PS2061.

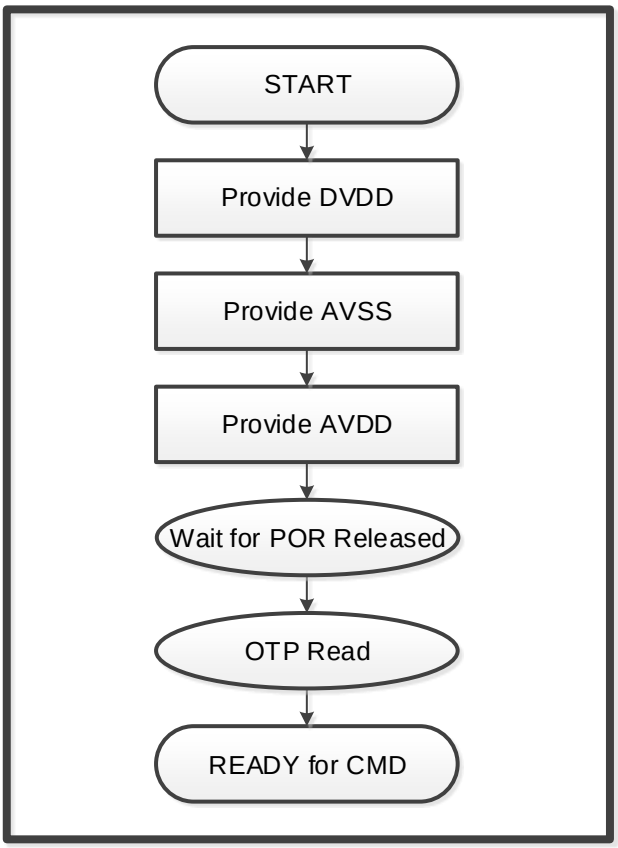


Figure 91. Power-up Sequence.

As depicted in Figure 91, the logic power, DVDD, should be provided first. If AVDD is provided prior to DVDD, the switch control logic's state is undefined until DVDD is supplied, which may unintentionally turn on the switches before DVDD is supplied. Note that for negative AVSS, AVSS also should be provided after DVDD, because negative AVSS means a certain voltage (AVDD – AVSS) is applied to the analog circuit.

If PS2064 is supplied with DVDD and AVDD, the internal POR of PS2064 generates RESET signal internally, and PS2064 changes to RESET state until the RESET signal from POR is released. RESET from POR is released after t_{RST}, and PS2064 starts reading its own internal OTP memory. To read the OTP Memory, an external clock is necessary. Don't forget that a minimum of 2000 clocks is always required after reset or power on.

External RESET is also supported through a pin named RSTN, and actual RESET signal is generated from both POR and RSTN signals. This leads to that on power-up, if RSTN is released before POR is released (i.e. RSTN changes from LOW to HIGH before $t_{PU} + t_{PU} + t_{RST}$ is elapsed), actual RESET signal is still active (i.e. RESET is being issued) until RESET from POR is released. On the other hand, if RSTN is kept LOW though POR is released, actual RESET signal is still active until RSTN is released.

However, since RSTN pin is internally pulled-up, user may leave RSTN pin OPEN in most of the cases. For the detailed timing of power-up sequence, refer to *Figure 2. Power-up Sequence.*

Interface Protocol & Types of Commands

Controlling PS2064s is performed through commands from the host. The host sends commands through two control signals (CSN) and 1-bit wide data pins. CSN signal is used to select the target Bank.

- ***Data frame(SPI)***

PS2064 interface is structured with a data frame as depicted in the following Figure 102.

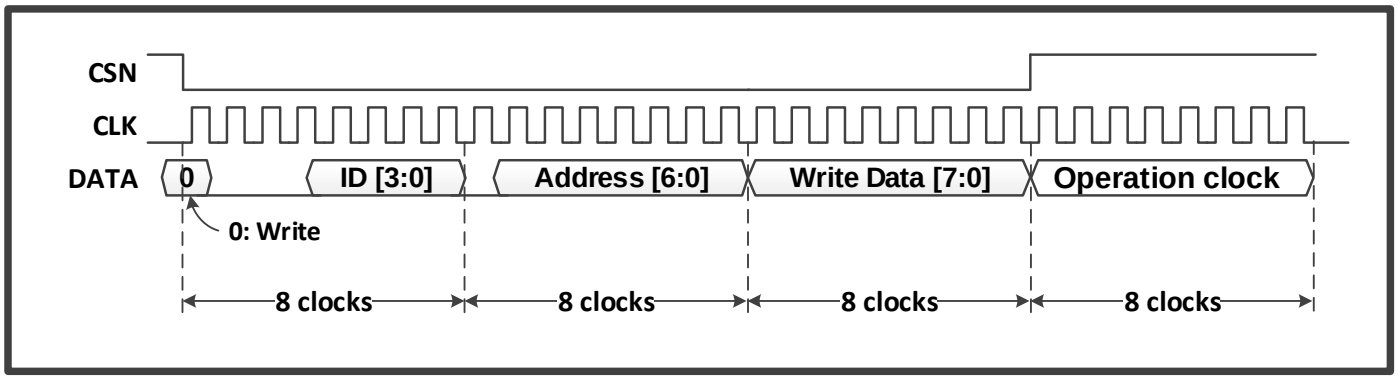


Figure 102. Timing Diagram for SPI.

PS2064 Interface initiates when CSN transitions from high to low, consisting of a 3-byte data frame, along with a 1-byte operation byte.

Controlling Switches

- *States of Switches*

The main usage of PS2064 is to control AIN – AOUT connection by changing the states of its switches. Each switch can be in one of two states – ON, OFF.

In **ON** state, the switch is turned-on, and the AIN signal is CONNECTED to the corresponding AOUT signal.

In **OFF** state, the switch is turned-off, and the AIN signal is DISCONNECTED from the corresponding AOUT signal.

Besides ON/OFF states, each switch has an additional flag named **REJECT**. If REJECT flag is set for a switch, the switch changes to OFF state automatically, and further commands to turn on the switch are ignored. Only special commands or external reset (RSTN) can clear the REJECT flag.

- *Initialization of Switches*

The initialization of the switches can be done through initialization commands. There are two initialization commands. They are,

> 0x1C: RST_BNK
> 0x1D: INIT_BNK

The states of all switches in the bank are simultaneously changed by these commands, and it helps set the initial states of all switches with less commands. For the detailed information about each command, refer to *Commands Descriptions*.

- *Changing States of Switches*

To change the states of switches, ONOFF_XXX commands are used.

> 0x20: ONOFF_CHP_CR0
> 0x21: ONOFF_CHP_CR1
> 0x22: ONOFF_CHP_CR2
> 0x23: ONOFF_CHP_CR3
> 0x24: ONOFF_CHP_CR4
> 0x25: ONOFF_CHP_CR5
> 0x26: ONOFF_CHP_CR6
> 0x27: ONOFF_CHP_CR7

- 0x28: ONOFF_CHP_CH0
- 0x29: ONOFF_CHP_CH1
- 0x2A: ONOFF_CHP_CH2
- 0x2B: ONOFF_CHP_CH3
- 0x2C: ONOFF_CHP_CH4
- 0x2D: ONOFF_CHP_CH5
- 0x2E: ONOFF_CHP_CH6
- 0x2F: ONOFF_CHP_CH7
- 0x30: ONOFF_CHP_ACR
- 0x31: ONOFF_CHP_ACH
- 0x38: ONOFF_BNK_ACR
- 0x39: ONOFF_BNK_ACH
- 0x3A: ONOFF_BNK_SCR
- 0x3B: ONOFF_BNK_SCH

ONOFF_XXX commands directly specify the ON-OFF states of the target switches. The target switches are specified using Chip-ID and Core-ID in the transmitted command, combined with the suffix of the command. The intended ON-OFF states for the target switches are transmitted through Write Data[7:0]. To turn on the switch, corresponding bit of Write Data should be '1', and to turn off, it should be '0'. For the detailed information about each ONOFF_XXX commands, refer to *Commands Descriptions*.

- *Setting REJECT Flags*

A REJECT flag is used to let the switch ignore further ON-OFF related commands. It is useful when we want some switches to stay OFF while we control many switches simultaneously with commands such as ONOFF_BNK_ACR. REJECT flags can be controlled by RJT_XXX commands. The command to set the REJECT flag is as follows.

- 0x40: RJT_CHP_CR0
- 0x41: RJT_CHP_CR1
- 0x42: RJT_CHP_CR2
- 0x43: RJT_CHP_CR3
- 0x44: RJT_CHP_CR4
- 0x45: RJT_CHP_CR5
- 0x46: RJT_CHP_CR6
- 0x47: RJT_CHP_CR7
- 0x48: RJT_CHP_CH0
- 0x49: RJT_CHP_CH1
- 0x4A: RJT_CHP_CH2
- 0x4B: RJT_CHP_CH3
- 0x4C: RJT_CHP_CH4
- 0x4D: RJT_CHP_CH5
- 0x4E: RJT_CHP_CH6
- 0x4F: RJT_CHP_CH7
- 0x50: RJT_CHP_ACR
- 0x51: RJT_CHP_ACH
- 0x58: RJT_BNK_ACR
- 0x59: RJT_BNK_ACH
- 0x5A: RJT_BNK_SCR
- 0x5B: RJT_BNK_SCH

REJECT flags are set to ‘1’ according to the transmitted Write Data[7:0] of RJT_XXX commands. If a bit of Write Data is ‘0’, corresponding REJECT flag(s) is set to ‘1’. Otherwise, corresponding REJECT flag(s) does not change. The target switches are specified by Chip-ID and Core-ID of the transmitted command. For the detailed information about RJT_XXX commands, refer to *Commands Descriptions*.

Protection functions

- ***Active discharge (Default: Disable)***

PS2064 supports the Active discharging to prevent EOS in the DUT. When the switch is turned OFF, AOUT is automatically pull-down, discharging the current stored in AOUT.

Active discharging feature is enabled by TSTCON bit (bit 1) of Test Control Register(i.e. enabled if AD_EN = 1). For more information about AD_EN bit, refer to TST_CON(0x6) of Commands Descriptions.

Commands Descriptions

- Suffixes of the Commands

Most of PS2064's commands are to control the states of the switches. Basically, each command can control switches in Core unit. However, to reduce the number of commands for setting the states of the switches, several variations of commands are supported, and they can address target switches in different ways from basic command (i.e. in Core unit). To represent this easily, commands have suffixes which represent the range of the target switches. The suffixes are,

> *_BNK
> *_CHP_CRX / *_CHP_CHX
> *_CHP_ACR / *_CHP_ACH
> *_BNK_ACR / *_BNK_ACH
> *_BNK_SCR / *_BNK_SCH

_BNK suffix signifies BANK. BANK represents a group with the same control signals.

_CHP_CRX suffix means CHIP CORE X. It signifies the Xth CORE within one CHIP in the BANK.
_CHP_CHX suffix means CHIP CH X. It signifies the Xth CH within one CHIP in the BANK.

_CHP_ACR suffix means CHIP ALL CORE. It signifies all COREs within one CHIP in the BANK.
_CHP_ACH suffix means CHIP ALL CH. It signifies all CHs within one CHIP in the BANK.

_BNK_ACR suffix means BANK ALL CORE. It represents all CHIPs and all COREs within the BANK. ID is not necessary.
_BNK_ACH suffix means BANK ALL CH. It represents all CHIPs and all CHs within the BANK. ID is not necessary.

_BNK_SCR suffix means BANK SINGLE CORE. It represents the CORE-ID within the BANK. ID serves as the CORE-ID.
_BNK_SCH suffix means BANK SINGLE CH. It represents the CH-ID within the BANK. ID serves as the CH-ID.

- ***Switch On/Off commands***

Table 1 shows the list of the switch on/off commands.

Table 1. On/Off Commands List.

Addr	Command	Description	ID is used as
0x1C	RST_BNK	Disables all switches in the bank. REJECT states are CLEARED.	IGNORE
0x1D	INIT_BNK	Enables all switches in the bank. Including those in REJECT state. REJECT states are CLEARED.	IGNORE
0x20	ONOFF_CHP_CR0	ONOFF states of the eight switches of CORE0 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x21	ONOFF_CHP_CR1	ONOFF states of the eight switches of CORE1 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x22	ONOFF_CHP_CR2	ONOFF states of the eight switches of CORE2 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x23	ONOFF_CHP_CR3	ONOFF states of the eight switches of CORE3 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x24	ONOFF_CHP_CR4	ONOFF states of the eight switches of CORE4 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x25	ONOFF_CHP_CR5	ONOFF states of the eight switches of CORE5 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x26	ONOFF_CHP_CR6	ONOFF states of the eight switches of CORE6 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x27	ONOFF_CHP_CR7	ONOFF states of the eight switches of CORE7 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x28	ONOFF_CHP_CH0	ONOFF states of the eight switches of Channel0 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x29	ONOFF_CHP_CH1	ONOFF states of the eight switches of Channel1 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x2A	ONOFF_CHP_CH2	ONOFF states of the eight switches of Channel2 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x2B	ONOFF_CHP_CH3	ONOFF states of the eight switches of Channel3 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID

0x2C	ONOFF_CHP_CH4	ONOFF states of the eight switches of Channel4 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x2D	ONOFF_CHP_CH5	ONOFF states of the eight switches of Channel5 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x2E	ONOFF_CHP_CH6	ONOFF states of the eight switches of Channel6 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x2F	ONOFF_CHP_CH7	ONOFF states of the eight switches of Channel7 of the specified chip. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x30	ONOFF_CHP_ACR	Changes the states of all switches in the specified chip. Eight bit data is written to all Cores identically. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x31	ONOFF_CHP_ACH	Changes the states of all switches in all Channels of the specified chip. Eight bit data is written to all Channels identically. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHIP-ID
0x38	ONOFF_BNK_ACR	Changes the states of all switches of all chips in the bank. Eight bit data is written to all Cores identically. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	IGNORE
0x39	ONOFF_BNK_ACH	Changes the states of all switches of all chips in the bank. Eight bit data is written to all Channels identically. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	IGNORE
0x3A	ONOFF_BNK_SCR	Changes the states of the specified core of all chips in the bank. Eight bit data is written to the specified Core for all chips in the bank. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CORE-ID
0x3B	ONOFF_BNK_SCH	Changes the states of the specified channel of all chips in the bank. Eight bit data is written to the specified Channel for all chips in the bank. 0: OFF, 1: ON Note) Switches in REJECT states are NOT affected.	CHANNEL-ID

- ***RST_BNK (0x1C) / INIT_BNK (0x1D)***

RST_BNK / INIT_BNK commands are mainly used for initialization of switches in the selected Bank. These commands are applied to all switches of all PS2064s in the Bank simultaneously.

RST_BNK commands turn off (i.e. change to OFF state) all switches of all PS2064s in the Bank. The RST_BNK command clears all REJECT flags.

INIT_BNK commands turn on (i.e. change to ON state) all switches of all PS2064s in the Bank. The INIT_BNK command clears the REJECT flags for all switches.

Table 2 shows the operation of the four initialization commands.

Table 2. Operation of Initialization Commands.

Command	ON-OFF States	REJECT Flags
RST_BNK	OFF	CLEARED
INIT_BNK	ON	CLEARED

- ***Reject commands***

Table 3 shows the list of reject commands.

Table 3. Reject Commands List.

Addr	Command	Description	ID is used as
0x40	RJT_CHP_CR0	REJECT states of the eight switches of CORE0 of the specified chip. 0: No change, 1: REJECT & OFF	CHIP-ID
0x41	RJT_CHP_CR1	REJECT states of the eight switches of CORE1 of the specified chip. 0: No change, 1: REJECT & OFF	CHIP-ID
0x42	RJT_CHP_CR2	REJECT states of the eight switches of CORE2 of the specified chip. 0: No change, 1: REJECT & OFF	CHIP-ID
0x43	RJT_CHP_CR3	REJECT states of the eight switches of CORE3 of the specified chip. 0: No change, 1: REJECT & OFF	CHIP-ID
0x44	RJT_CHP_CR4	REJECT states of the eight switches of CORE4 of the specified chip. 0: No change, 1: REJECT & OFF	CHIP-ID
0x45	RJT_CHP_CR5	REJECT states of the eight switches of CORE5 of the specified chip. 0: No change, 1: REJECT & OFF	CHIP-ID
0x46	RJT_CHP_CR6	REJECT states of the eight switches of CORE6 of the specified chip. 0: No change, 1: REJECT & OFF	CHIP-ID
0x47	RJT_CHP_CR7	REJECT states of the eight switches of CORE7 of the specified chip. 0: No change, 1: REJECT & OFF	CHIP-ID
0x48	RJT_CHP_CH0	REJECT states of the eight switches of Channel0 of the specified chip. 0: No change, 1: REJECT & 0FF.	CHIP-ID
0x49	RJT_CHP_CH1	REJECT states of the eight switches of Channel1 of the specified chip. 0: No change, 1: REJECT & 0FF.	CHIP-ID
0x4A	RJT_CHP_CH2	REJECT states of the eight switches of Channel2 of the specified chip. 0: No change, 1: REJECT & 0FF.	CHIP-ID
0x4B	RJT_CHP_CH3	REJECT states of the eight switches of Channel3 of the specified chip. 0: No change, 1: REJECT & 0FF.	CHIP-ID
0x4C	RJT_CHP_CH4	REJECT states of the eight switches of Channel4 of the specified chip. 0: No change, 1: REJECT & 0FF.	CHIP-ID
0x4D	RJT_CHP_CH5	REJECT states of the eight switches of Channel5 of the specified chip. 0: No change, 1: REJECT & 0FF.	CHIP-ID
0x4E	RJT_CHP_CH6	REJECT states of the eight switches of Channel6 of the specified chip. 0: No change, 1: REJECT & 0FF.	CHIP-ID
0x4F	RJT_CHP_CH7	REJECT states of the eight switches of Channel7 of the specified chip. Write) 0: No change, 1: REJECT & OFF	CHIP-ID
0x50	RJT_CHP_ACR	Changes the states of all switches in the specified chip to REJECT. Eight bit data is applied to all Cores identically. 0: No change, 1: REJECT & OFF	CHIP-ID

0x51	RJT_CHP_ACH	Changes the states of all switches in all Channels of the specified chip to REJECT. Eight bit data is applied to all Channels identically. 0: No change, 1: REJECT & OFF	CHIP-ID
0x58	RJT_BNK_ACR	Changes the states of all switches of all chips in the bank to REJECT. Eight bit data is applied to all Cores identically. 0: No change, 1: REJECT & OFF	IGNORED
0x59	RJT_BNK_ACH	Changes the states of all switches of all chips in the bank to REJECT. Eight bit data is applied to all Channels identically. 0: No change, 1: REJECT & OFF	IGNORED
0x5A	RJT_BNK_SCR	Changes the states of the specified core of all chips in the bank to REJECT. Each bit is applied to the specified Core of all chips in the bank. 0: No change, 1: REJECT & OFF	CORE-ID
0x5B	RJT_BNK_SCH	Changes the states of the specified channel of all chips in the bank to REJECT. Each bit is applied to the specified Channel of all chips in the bank. 0: No change, 1: REJECT & OFF	CHANNEL-ID

- ***Function commands***

Table 34 shows the list of function commands.

Table 4. Function Commands List.

Addr	Command	Description	ID is used as
0x06	TSTCON	Test Control Register.	CHIP-ID

■ ***TSTCON (0x6)***

TSTCON command is used to update Test Control Register. **오류! 참조 원본을 찾을 수 없습니다.** shows the contents of Test Control Register.

Table 6. Test Control Register.

Bit Name	Bits	Descriptions	Reset	Remarks
RSVD	[7:5]	Reserved	-	-
AD_WEN	4	AD_EN write enable. AD_EN is updated. only if the written value of AD_WEN is '1'	-	-
AD_EN	3	Output active discharge enable	0	Initialized from OTP
RSVD	[2:0]	Reserved	-	-

Though the default values for AD_EN registers are loaded from internal OTP memory on bootstrap, their values can be changed by TSTCON command.

■ ***ONOFF_CHP_CR0 (0x20) ~ ONOFF_CHP_CR7 (0x27)***

ONOFF_CHP_CR0 command changes CORE0 of the ON-OFF states in the target PS2064. The input Write Data value is written to CORE0 of the specified PS2064. The target PS2064 is specified by ID. Figure 113 shows an example for ONOFF_CHP_CR0 command.

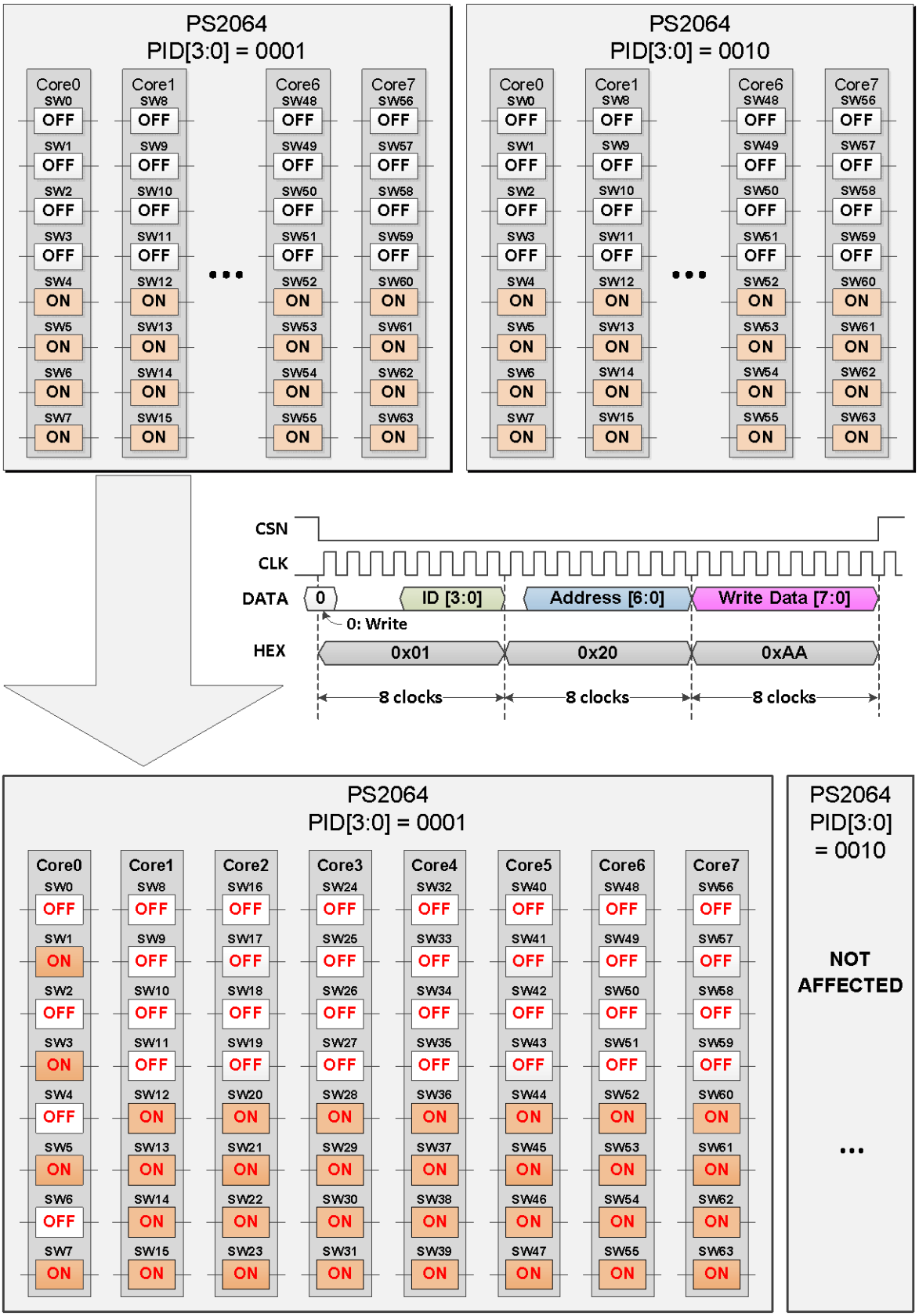


Figure 113. Example for ONOFF_CHP_CR0 Command.

In Figure 113, the input ID from the command is 0x1. CORE0 of the PS2064 whose ID is 0x1, is updated with the value of Write Data[7:0] (= 0xAA).
Note that the switches whose REJECT flags are set to ‘1’ are not updated, and remain in OFF state.
From ONOFF_CHP_CR0 to ONOFF_CHP_CR7, the operation remains the same, with only the target Core changing.

■ ***ONOFF_CHP_CH0 (0x28) ~ ONOFF_CHP_CH7 (0x2F)***

ONOFF_CHP_CH0 command changes Channel0 of the ON-OFF states in the target PS2064. The input Write Data value is written to Channel0 of the specified PS2064. The target PS2064 is specified by ID. Figure 13 shows an example for ONOFF_CHP_CH0 command.

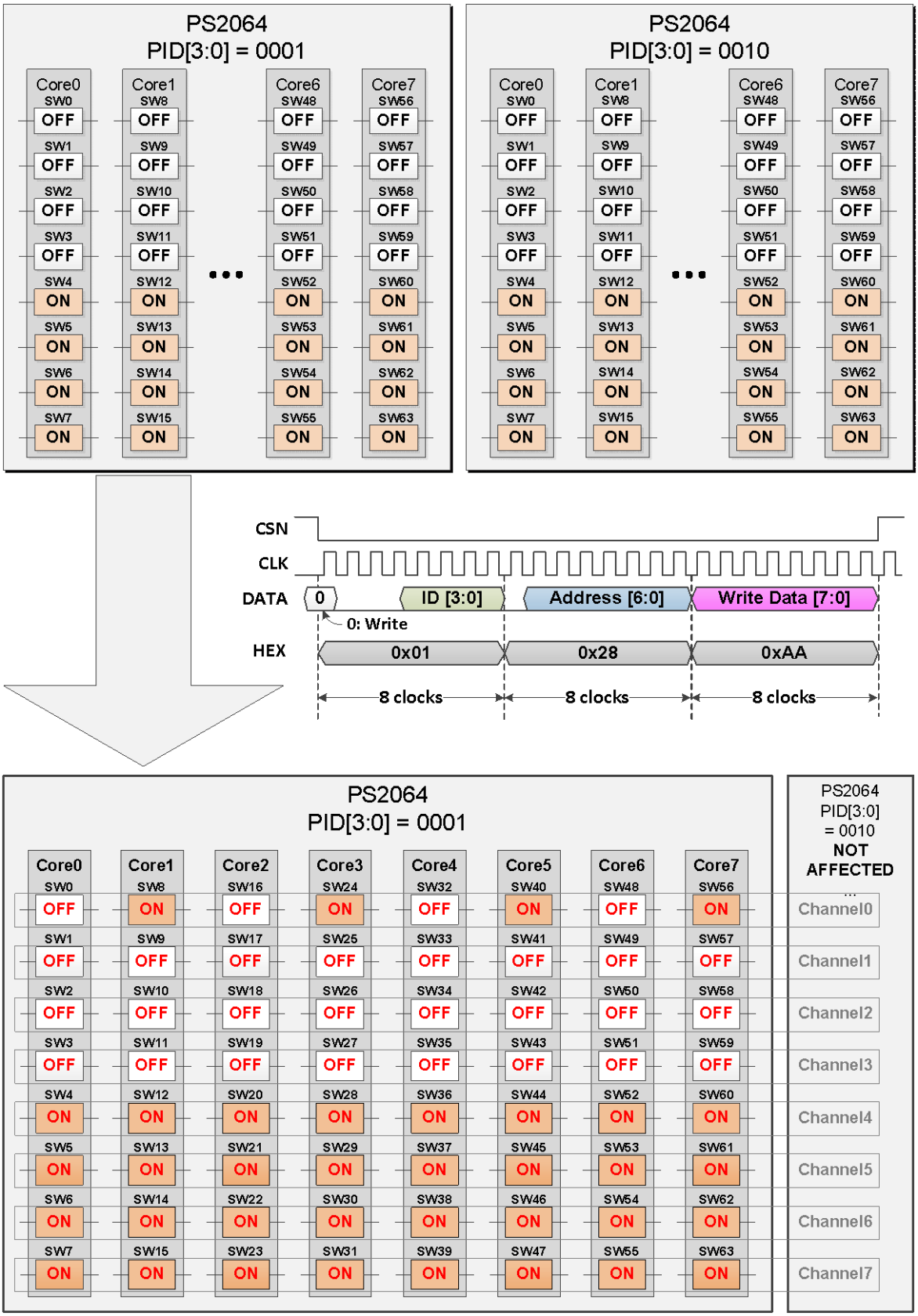


Figure 12. Example for ONOFF_CHP_CH0 Command.

In Figure 13, the input ID from the command is 0x1. Channel0 of the PS2064 whose ID is 0x1, is updated with the value of Write Data[7:0](=0xAA).
Note that the switches whose REJECT flags are set to ‘1’ are not updated, and remain in OFF state.
From ONOFF_CHP_CH0 to ONOFF_CHP_CH7, the operation remains the same, with only the target Core changing.

■ ***ONOFF_CHP_ACR (0x30)***

ONOFF_CHP_ACR command changes all Cores of the ON-OFF states in the target PS2064. The input Write Data value is written to all Cores of the specified PS2064. The target PS2064 is specified by ID. Figure 135 shows an example for ONOFF_CHP_ACR command.

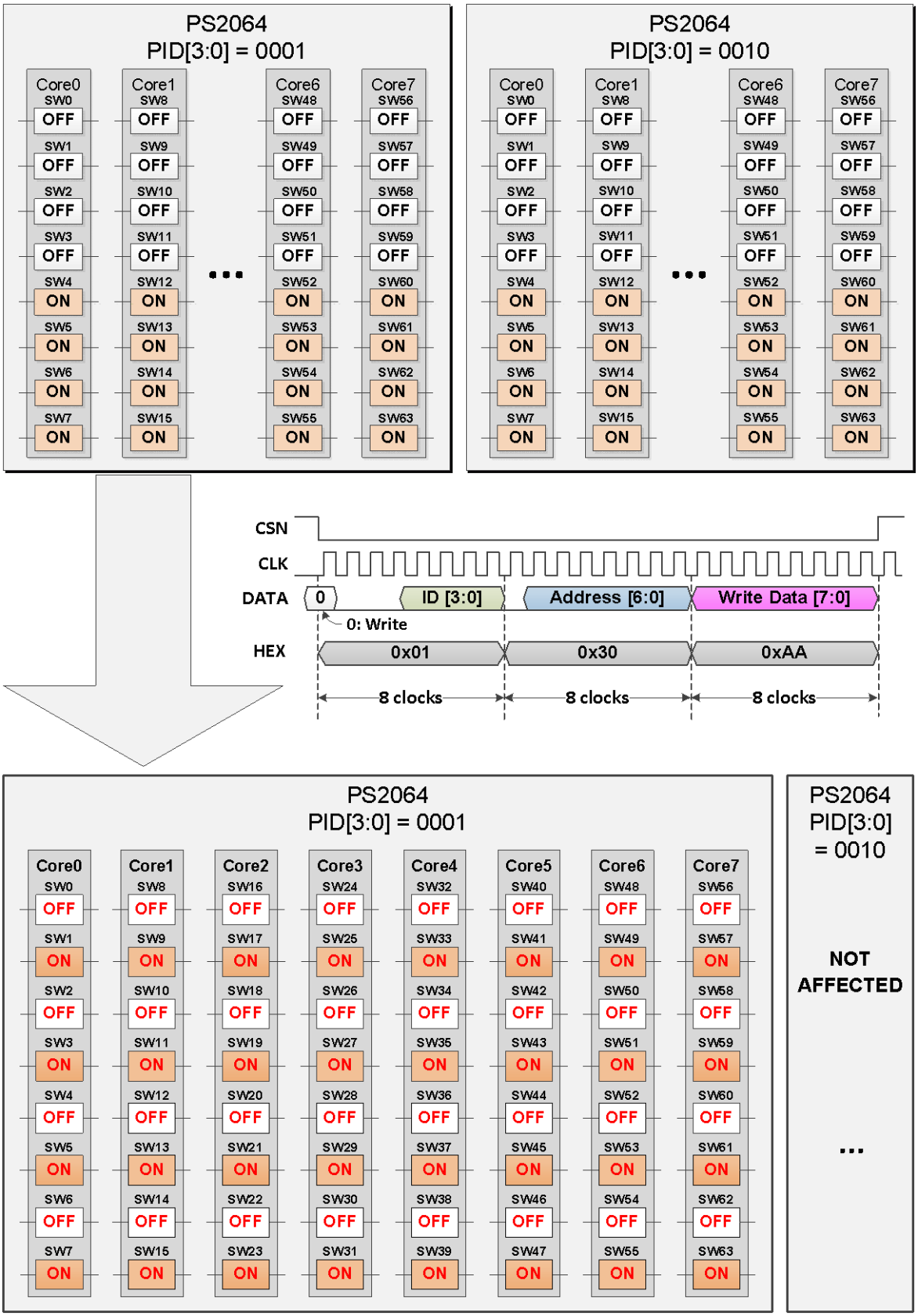


Figure 135. Example for ONOFF_CHP_ACR Command.

In Figure 135, the input ID from the command is 0x1. All Cores of the PS2064 whose ID is 0x1, is updated with the value of Write Data[7:0](=0xAA).
Note that the switches whose REJECT flags are set to ‘1’ are not updated, and remain in OFF state.

- ***ONOFF_CHP_ACH (0x31)***

ONOFF_CHP_ACH command changes all Channels of the ON-OFF states in the target PS2064. The input Write Data value is written to all Channels of the specified PS2064. The target PS2064 is specified by ID. Figure 136 shows an example for ONOFF_CHP_ACH command.

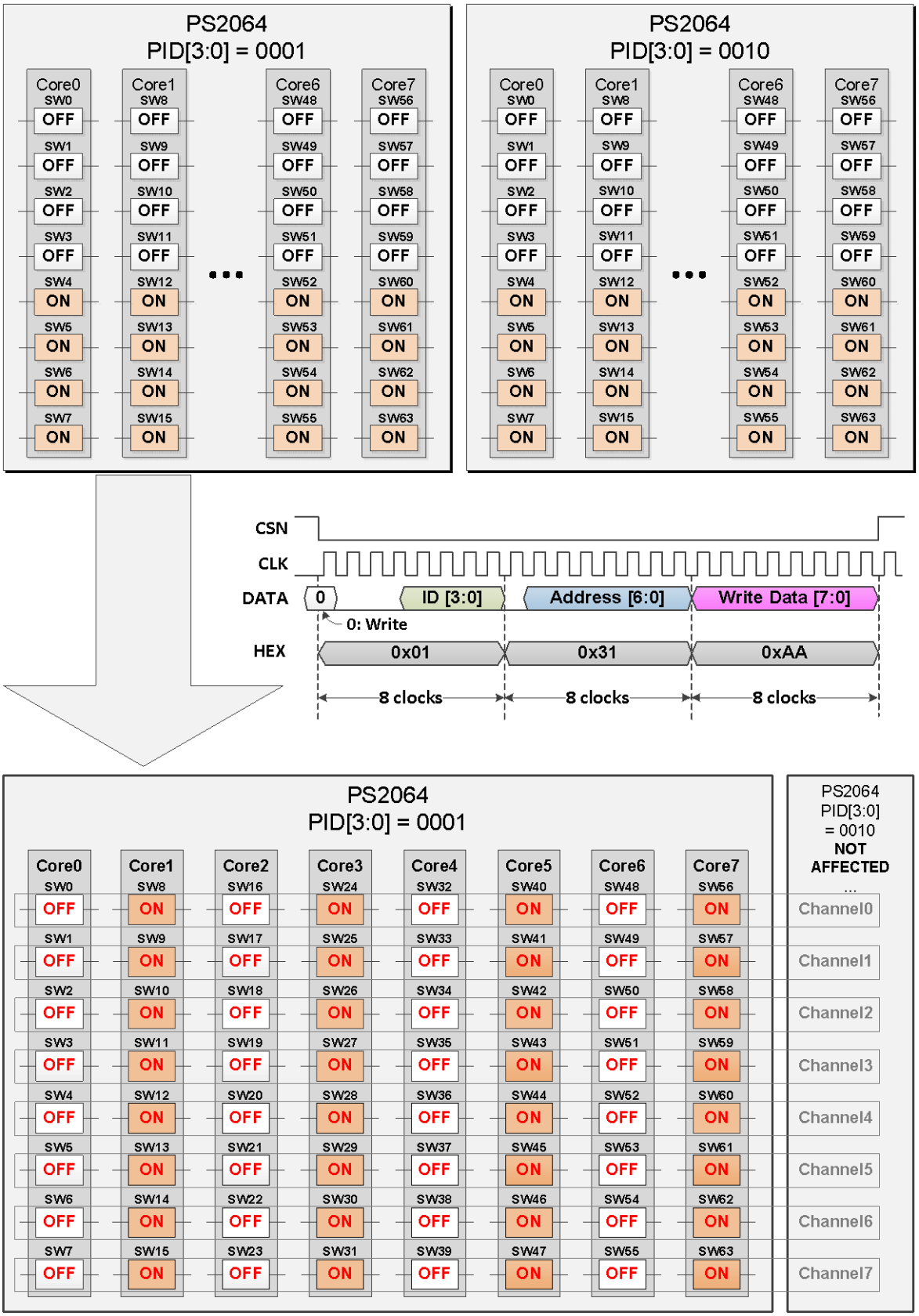


Figure 14. Example for ONOFF_CHP_ACH Command.

In Figure 13, the input ID from the command is 0x1. All Channels of the PS2064 whose ID is 0x1, is updated with the value of Write Data[7:0](=0xAA).
Note that the switches whose REJECT flags are set to ‘1’ are not updated, and remain in OFF state.

- ***ONOFF_BNK_ACR (0x38)***

ONOFF_BNK_ACR command changes all of the ON-OFF states in PS2064 in the selected BANK. The input Write Data value is written to all Cores of the PS2064. Figure 13 shows an example for ONOFF_BNK_ACR command.

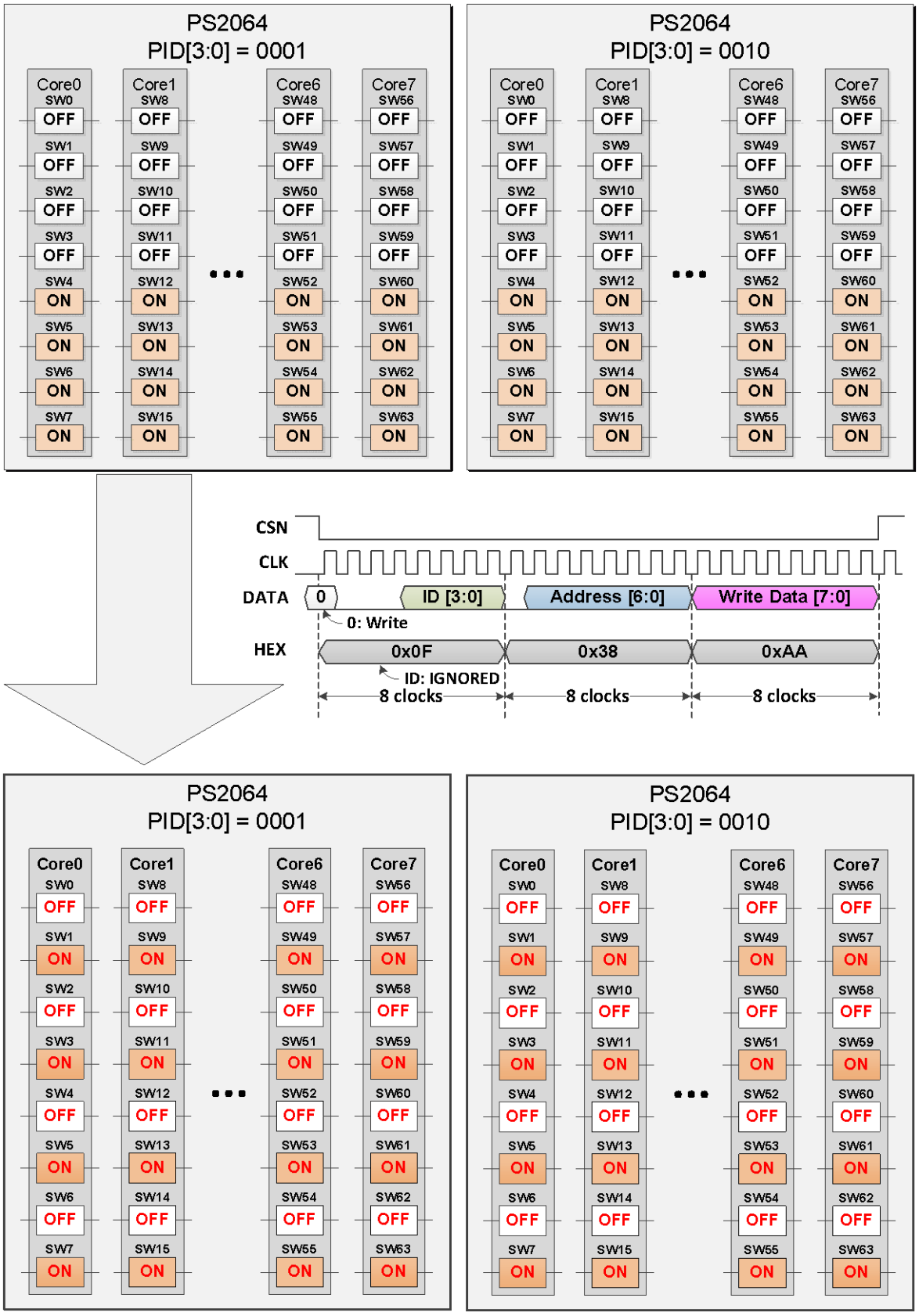


Figure 15. Example for ONOFF_BNK_ACR Command.

In Figure 13, Write Data[7:0] is written to all Cores of all PS2064s in the BANK. Since all Cores of all PS2064s are the target of ONOFF_BNK_ACR command, ID are ignored.
Note that the switches whose REJECT flags are set to ‘1’ are not updated, and remain in OFF state.

- ***ONOFF_BNK_ACH (0x39)***

ONOFF_BNK_ACH command changes all of the ON-OFF states in PS2064s in the selected BANK. The input Write Data[7:0] value is written to all Channels of the PS2064s. Figure 13 shows an example for ONOFF_BNK_ACH command.

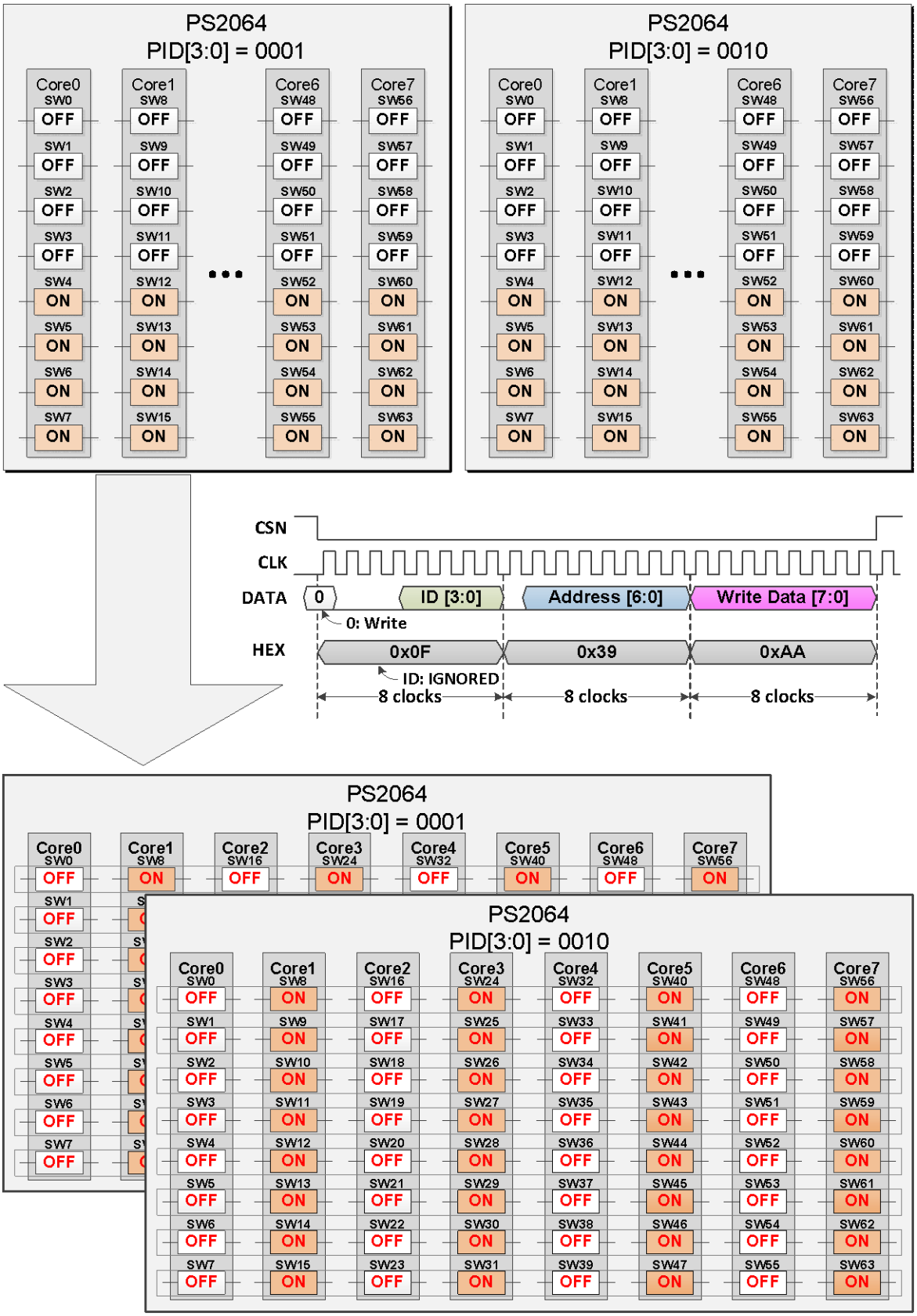


Figure 16. Example for ONOFF_BNK_ACH Command.

In Figure 13, Write Data[7:0] is written to all Channels of all PS2064s in the BANK. Since all Channels of all PS2064s are the target of ONOFF_BNK_ACH command, ID are ignored.
Note that the switches whose REJECT flags are set to ‘1’ are not updated, and remain in OFF state.

■ ***ONOFF_BNK_SCR (0x3A)***

ONOFF_BNK_SCR command changes the ON-OFF state of one Core of the PS2064 in the selected BANK. The input Write Data[7:0] value is written to one Core of the PS2064. The target Core is specified by ID. Figure 13 shows an example for ONOFF_BNK_SCR command.

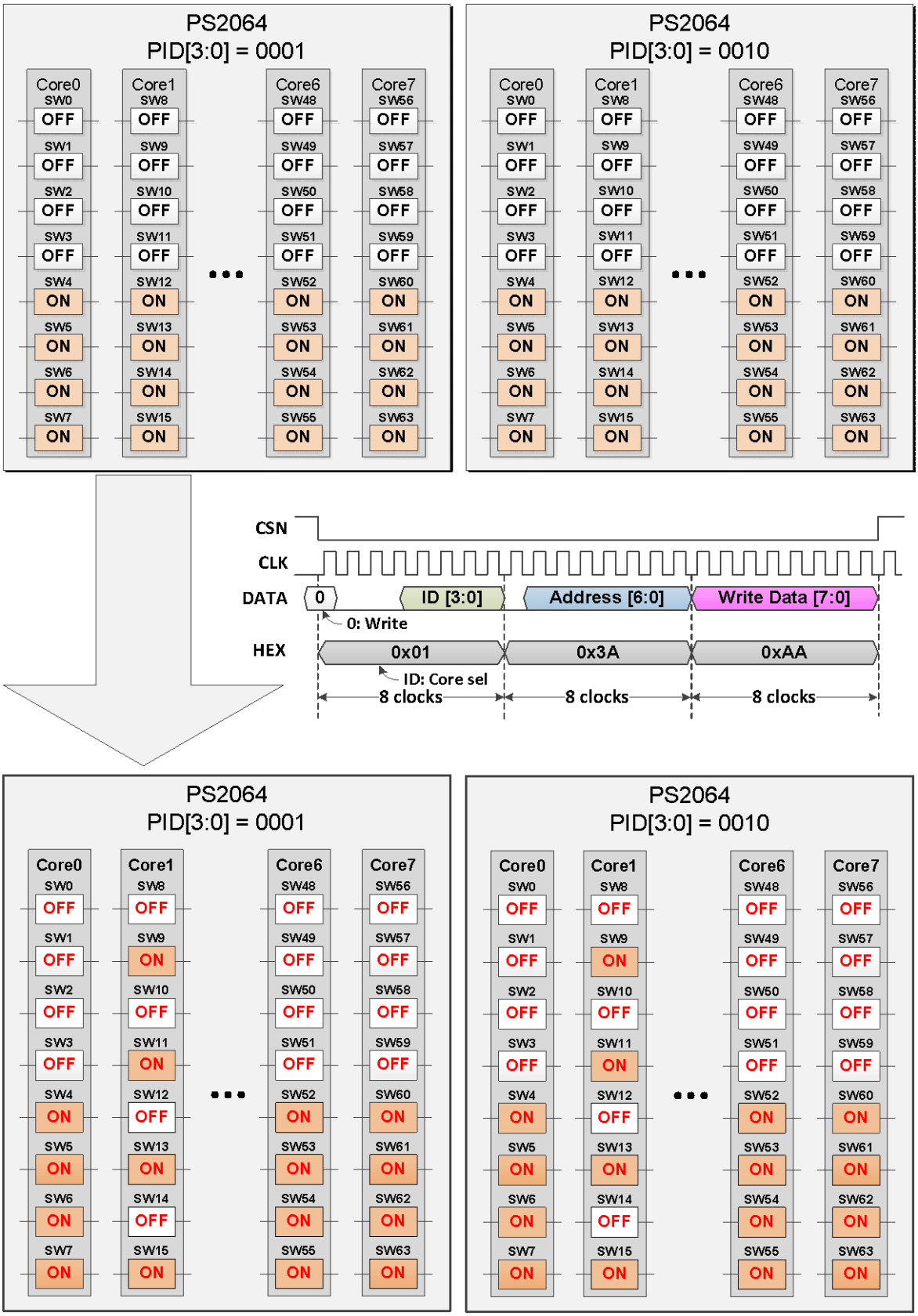


Figure 17. Example for ONOFF_BNK_SCR Command.

In Figure 13, Write Data[7:0] is written to one Core of all PS2064s in the BANK. Since one Core of all PS2064s are the target of ONOFF_BNK_SCR command, ID are selects the Core.
Note that the switches whose REJECT flags are set to ‘1’ are not updated, and remain in OFF state.

- ***ONOFF_BNK_SCH (0x3B)***

ONOFF_BNK_SCH command changes the ON-OFF state of one Channel of the PS2064 in the selected BANK. The input Write Data[7:0] value is written to one Channel of the PS2064. The target Channel is specified by ID. Figure 13 shows an example for ONOFF_BNK_SCH command.

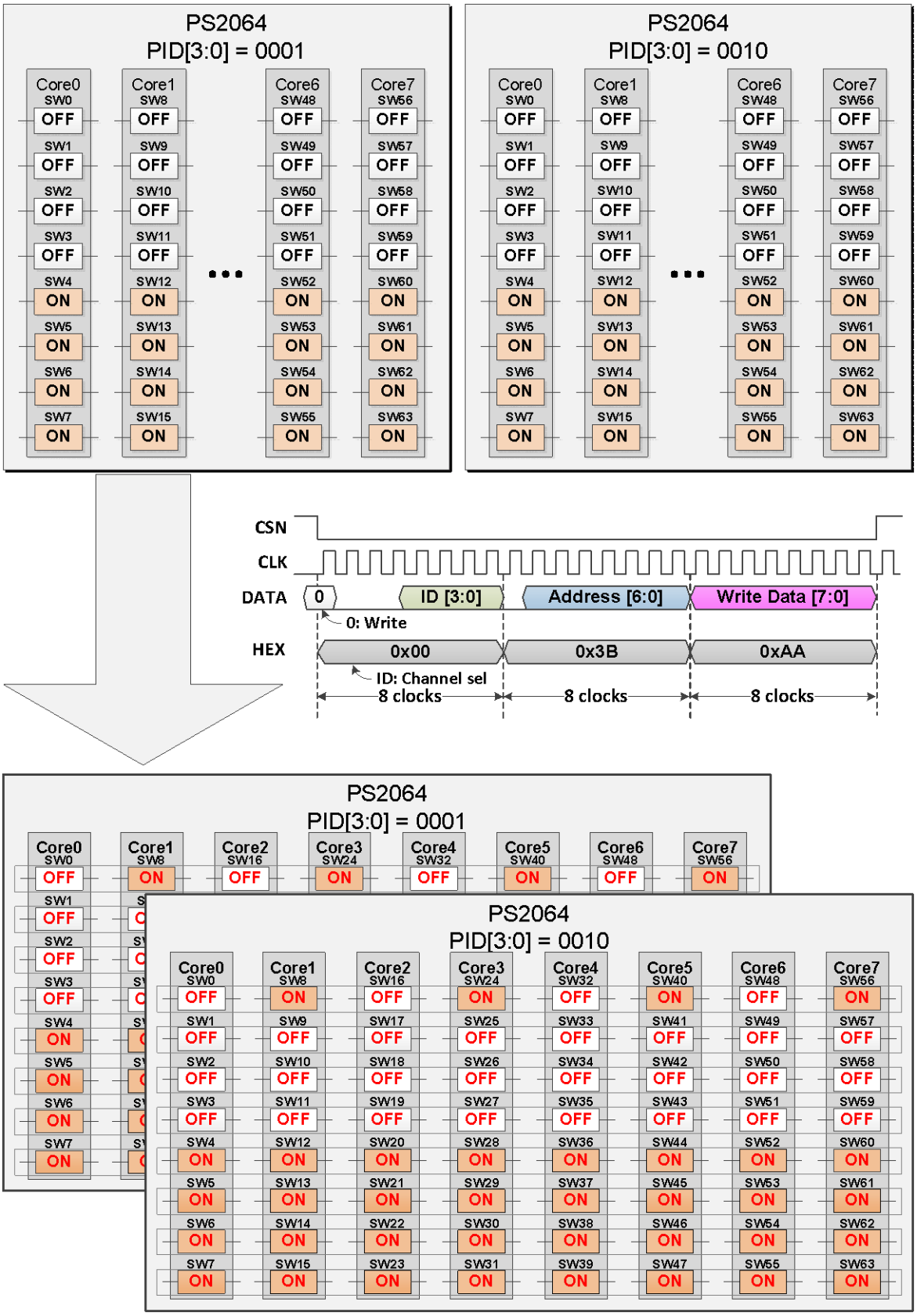


Figure 180. Example for ONOFF_BNK_SCH Command.

In Figure 13, Write Data[7:0] is written to one Channel of all PS2064s in the BANK. Since one Channel of all PS2064s are the target of ONOFF_BNK_SCH command, ID are selects the Channel.
Note that the switches whose REJECT flags are set to ‘1’ are not updated, and remain in OFF state.

- ***RJT_CHP_CR0 (0x40) ~ RJT_CHP_CR7 (0x47)***

RJT_CHP_CR0 command updates REJECT flags of the Core0. It receives ID and uses them to specify the target Switches in the target PS2064. According to each bit's value of Write Data[7:0], it sets REJECT flags of each switch of the Core0. Figure 11 shows an example for RJT_CHP_CR0 command.

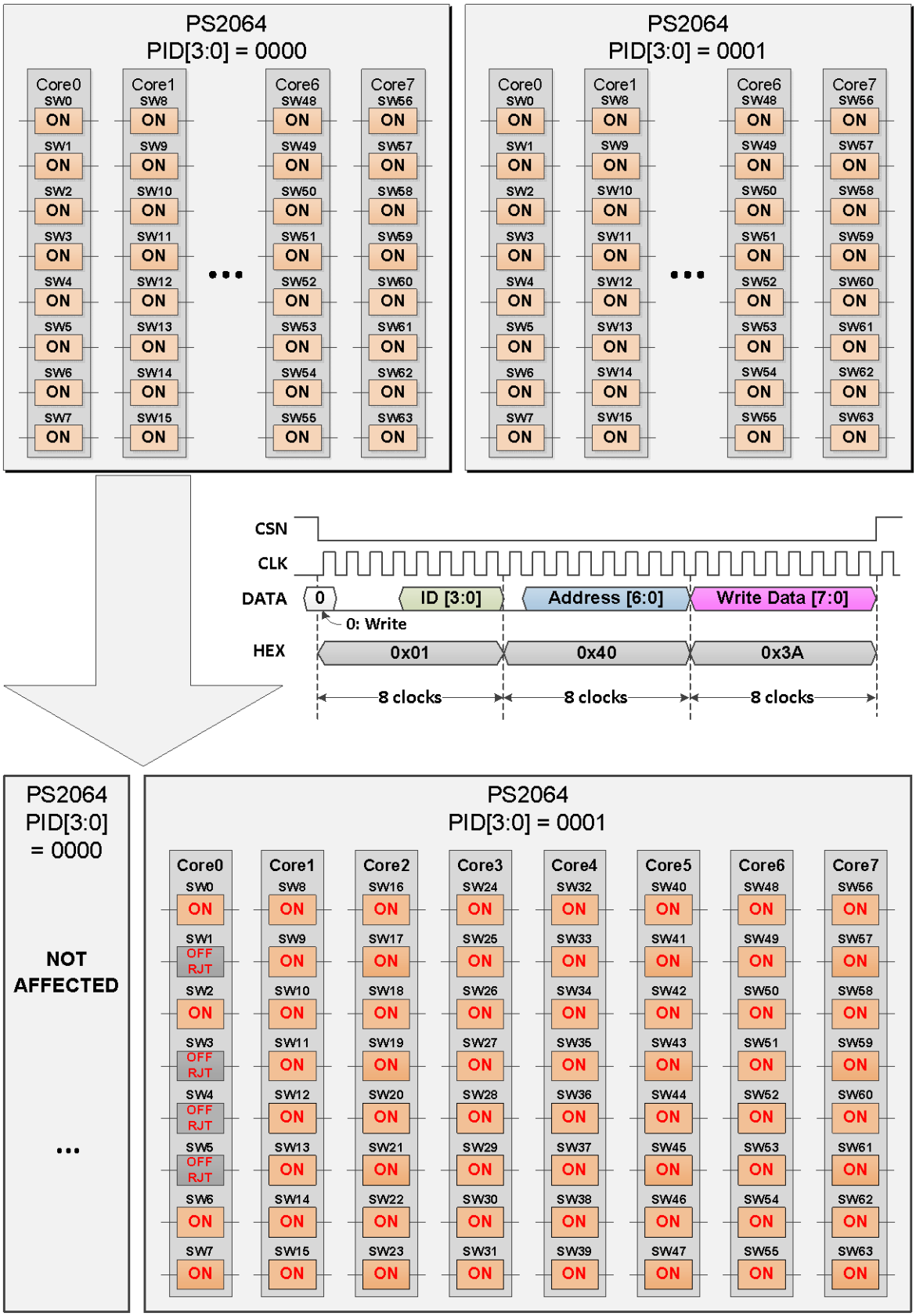


Figure 19. Example for RJT_CHP_CR0 Command.

In Figure 11, since ID is 0x1, the one with PID is 0x1 is selected as the target(i.e. the one with PID= 0x0 is not affected). Address(= 0x40) specifies the target Core as Core0.

Write Data[7:0] contains the actual update value of REJECT flags. If a bit of Write Data is '1', it indicates that corresponding switch's REJECT flag should be set to '1'. In Figure 11, since Write Data is 0x3A, bit5, bit4, bit3, bit1 of Write Data are '1'. This results in that REJECT flags of SW5, SW4, SW3, SW1 are set to '1'. ON-OFF states of those switches are also set to OFF.

Note that Write Data bit's value '1' does not mean 'Clear REJECT flag', but 'Set REJECT flag'. Once REJECT flags are set, they can be cleared only by RST_BNK or INIT_BNK commands. From RJT_CHP_CR0 to RJT_CHP_CR7, the operation remains the same, with only the target Core changing.

- ***RJT_CHP_CH0 (0x48) ~ RJT_CHP_CH7 (0x4F)***

RJT_CHP_CH0 command updates REJECT flags of the Channel0. It receives ID and uses them to specify the target Switches in the target PS2064. According to each bit's value of Write Data[7:0], it sets REJECT flags of each switch of the Channel0. Figure 11 shows an example for RJT_CHP_CH0 command.

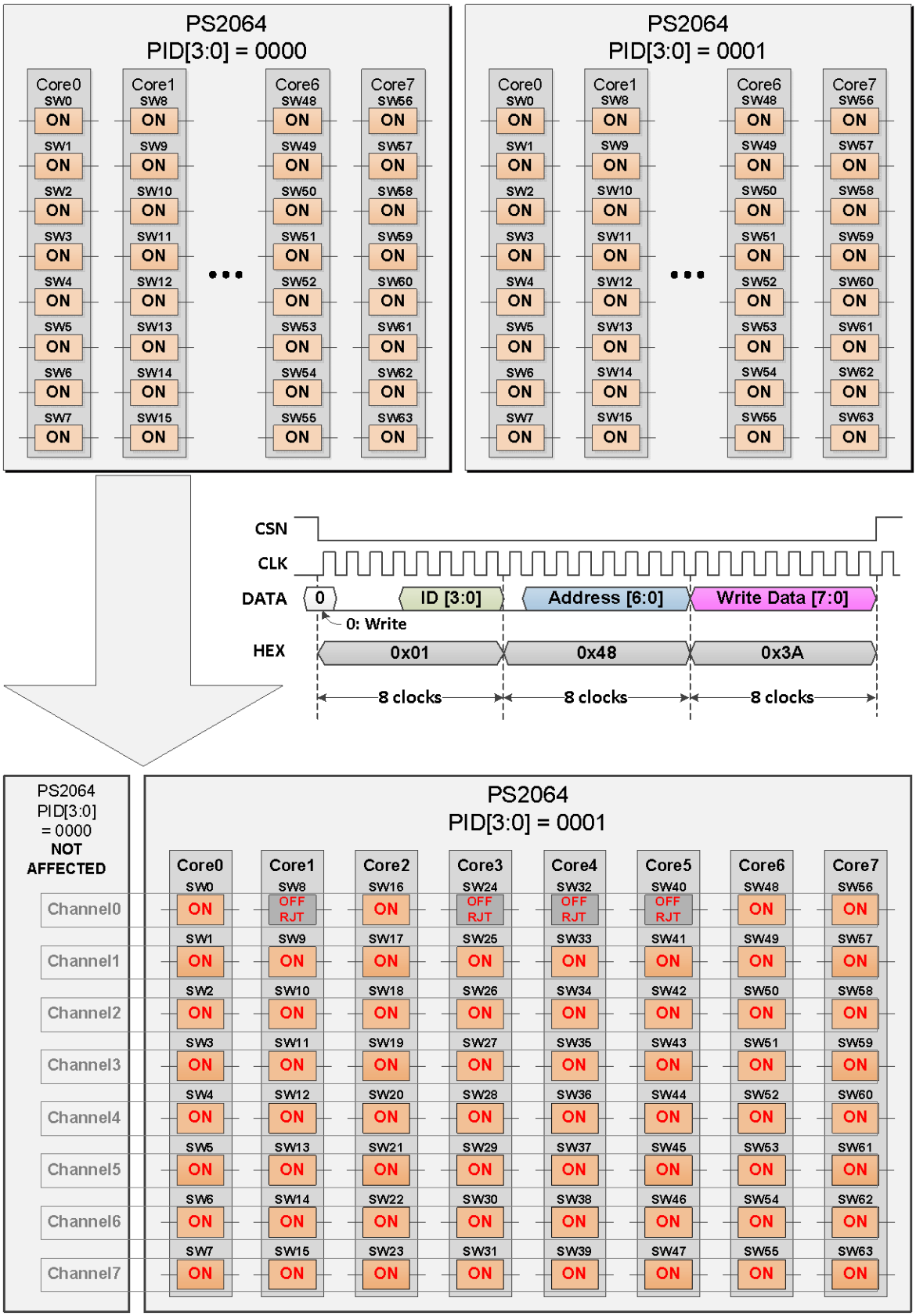


Figure 20. Example for RJT_CHP_CH0 Command.

In Figure 11, since ID is 0x1, the one with PID is 0x1 is selected as the target(i.e. the one with PID= 0x0 is not affected). Address(= 0x48) specifies the target Channel as Channel0.

Write Data[7:0] contains the actual update value of REJECT flags. If a bit of Write Data is '1', it indicates that corresponding switch's REJECT flag should be set to '1'. In Figure 11, since Write Data is 0x3A, bit5, bit4, bit3, bit1 of Write Data are '1'. This results in that REJECT flags of SW40, SW32, SW24, SW8 are set to '1'. ON-OFF states of those switches are also set to OFF.

Note that Write Data bit's value '1' does not mean 'Clear REJECT flag', but 'Set REJECT flag'. Once REJECT flags are set, they can be cleared only by RST_BNK or INIT_BNK commands. From RJT_CHP_CH0 to RJT_CHP_CH7, the operation remains the same, with only the target Channel changing.

- ***RJT_CHP_ACR (0x50)***

RJT_CHP_ACR command controls the REJECT flags in all Cores of the specified PS2064. According to each bit's value of Write Data[7:0], it sets REJECT flags for the eight switches of all Cores. Figure 13 shows an example for RJT_CHP_ACR command.

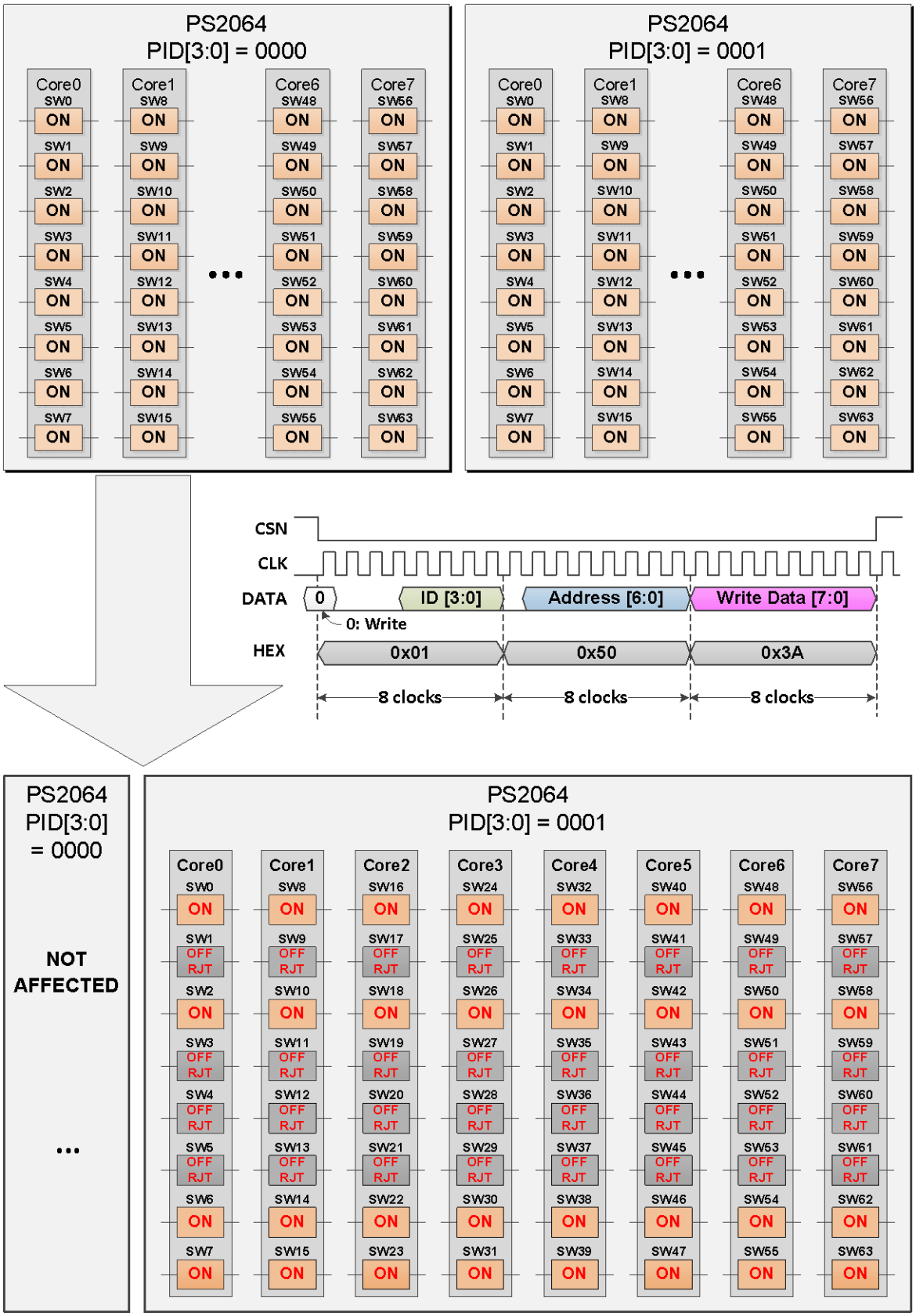


Figure 21. Example for RJT_CHP_ACR Command.

In Figure 13, target PS2064 is selected by the ID (= the one with PID is 0x1). Each bit of Write Data decides REJECT flags of all Cores. From bit0 to bit7 of Write Data[7:0] corresponds to SW0 to SW7 of each Core. In Core0, since bit1, bit3, bit4, and bit5 are '1's, REJECT flags of SW1, SW3, SW4, SW5 are set to '1'. When the REJECT flag is set to '1', the switch is status 'OFF'.

Note that Write Data bit's value '1' does not mean 'Clear REJECT flag', but 'Set REJECT flag'. Once REJECT flags are set, they can be cleared only RST_BNK or INIT_BNK commands.

- ***RJT_CHP_ACH (0x51)***

RJT_CHP_ACH command controls the REJECT flags in all Channels of the specified PS2064. According to each bit's value of Write Data[7:0], it sets REJECT flags for the eight switches of all Channels. Figure 13 shows an example for RJT_CHP_ACH command.

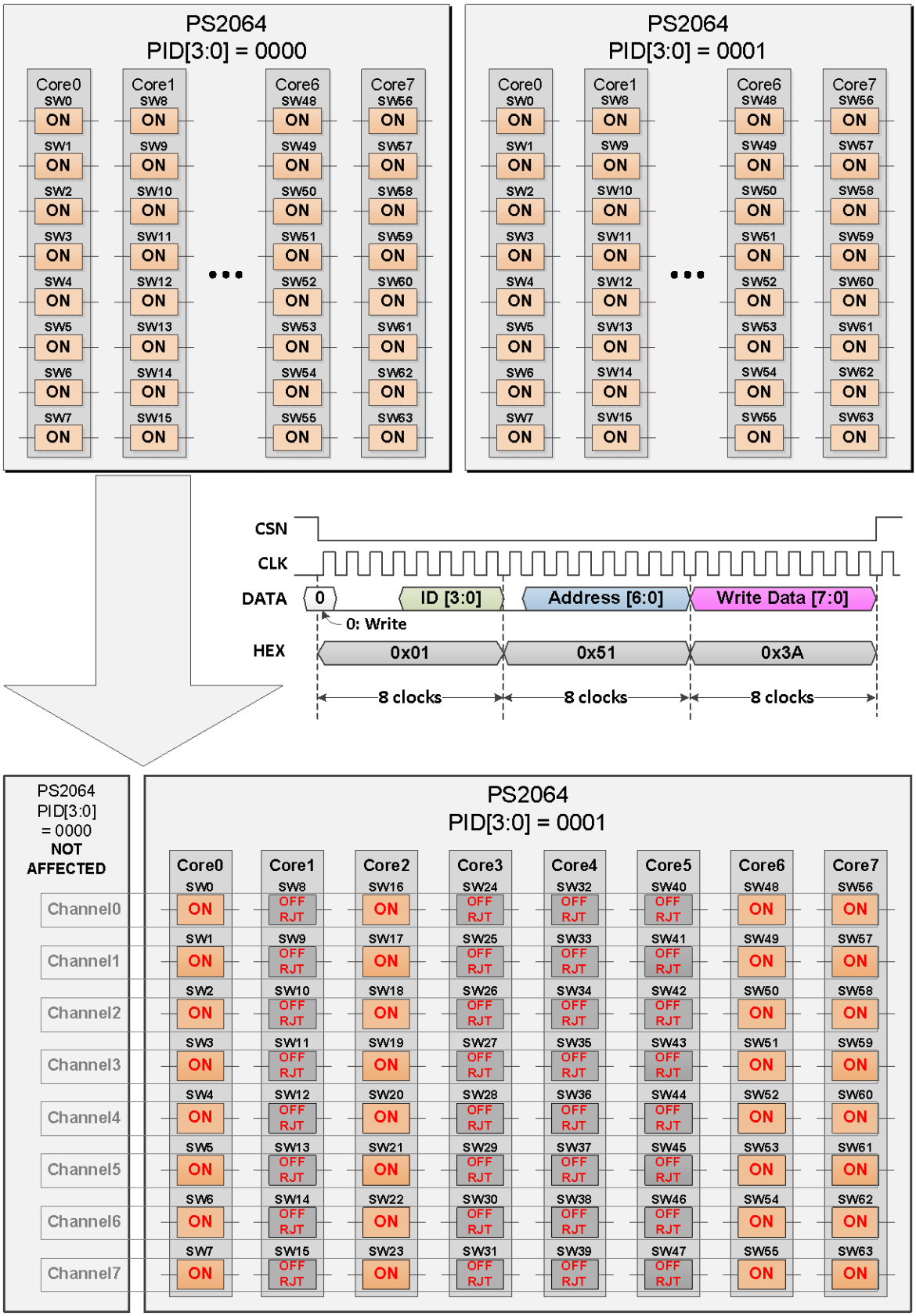


Figure 22. Example for RJT_CHP_ACH Command.

In Figure 13, target PS2064 is selected by the ID (= the one with PID is 0x1). Each bit of Write Data decides REJECT flags of all Channels. From bit0 to bit7 of Write Data[7:0] corresponds to Switch0 to Switch7 of each Channel. In Channel0, since bit1, bit3, bit4, and bit5 are '1's, REJECT flags of SW8, SW24, SW32, SW40 are set to '1'. When the REJECT flag is set to '1', the switch is status 'OFF'.

Note that Write Data bit's value '1' does not mean 'Clear REJECT flag', but 'Set REJECT flag'. Once REJECT flags are set, they can be cleared only RST_BNK or INIT_BNK commands.

- ***RJT_BNK_ACR (0x58)***

RJT_BNK_ACR command controls the REJECT flags of all Cores of the PS2064 in the selected BANK. According to each bit's value of Write Data[7:0], it sets REJECT flags of all Cores eight switches. Figure 13 shows an example for RJT_BNK_ACR command.

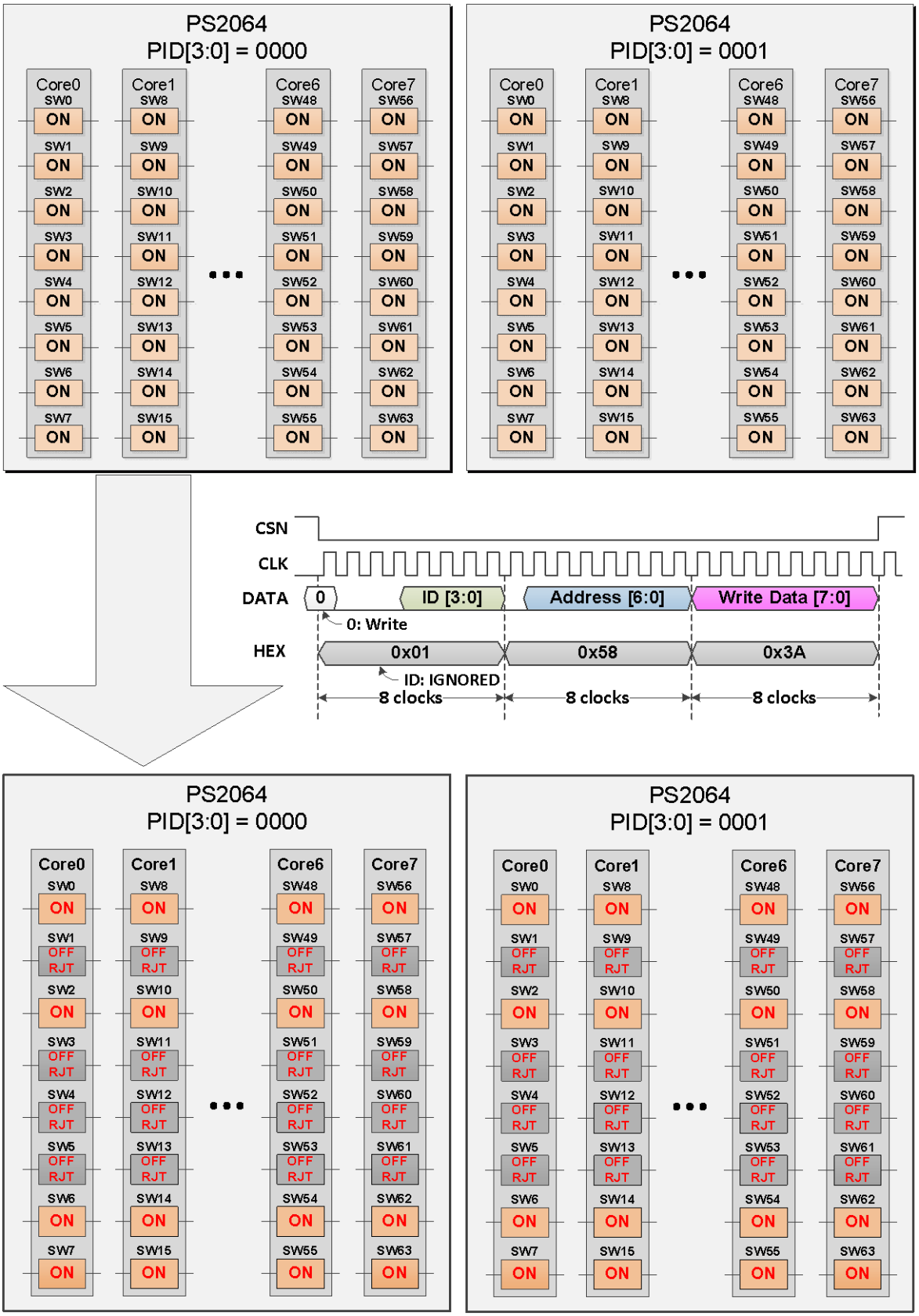


Figure 23. Example for RJT_BNK_ACR Command.

In Figure 13, all PS2064 devices within the BANK are targets. Therefore, the ID is ignored. Each bit of Write Data decides REJECT flags of all Cores. From bit0 to bit7 of Write Data[7:0] corresponds to SW0 to SW7 of each Core. In Core0, since bit1, bit3, bit4 and bit5 are '1's, REJECT flags of SW1, SW3, SW4, SW5 are set to '1'. When the REJECT flag is set to '1', the switch is status 'OFF'.

Note that Write Data bit's value '1' does not mean 'Clear REJECT flag', but 'Set REJECT flag'. Once REJECT flags are set, they can be cleared only RST_BNK or INIT_BNK commands.

- ***RJT_BNK_ACH (0x59)***

RJT_BNK_ACH command controls the REJECT flags of all Channels of the PS2064 in the selected BANK. According to each bit's value of Write Data[7:0], it sets REJECT flags for the eight switches of all Channels. Figure 13 shows an example for RJT_BNK_ACH command.

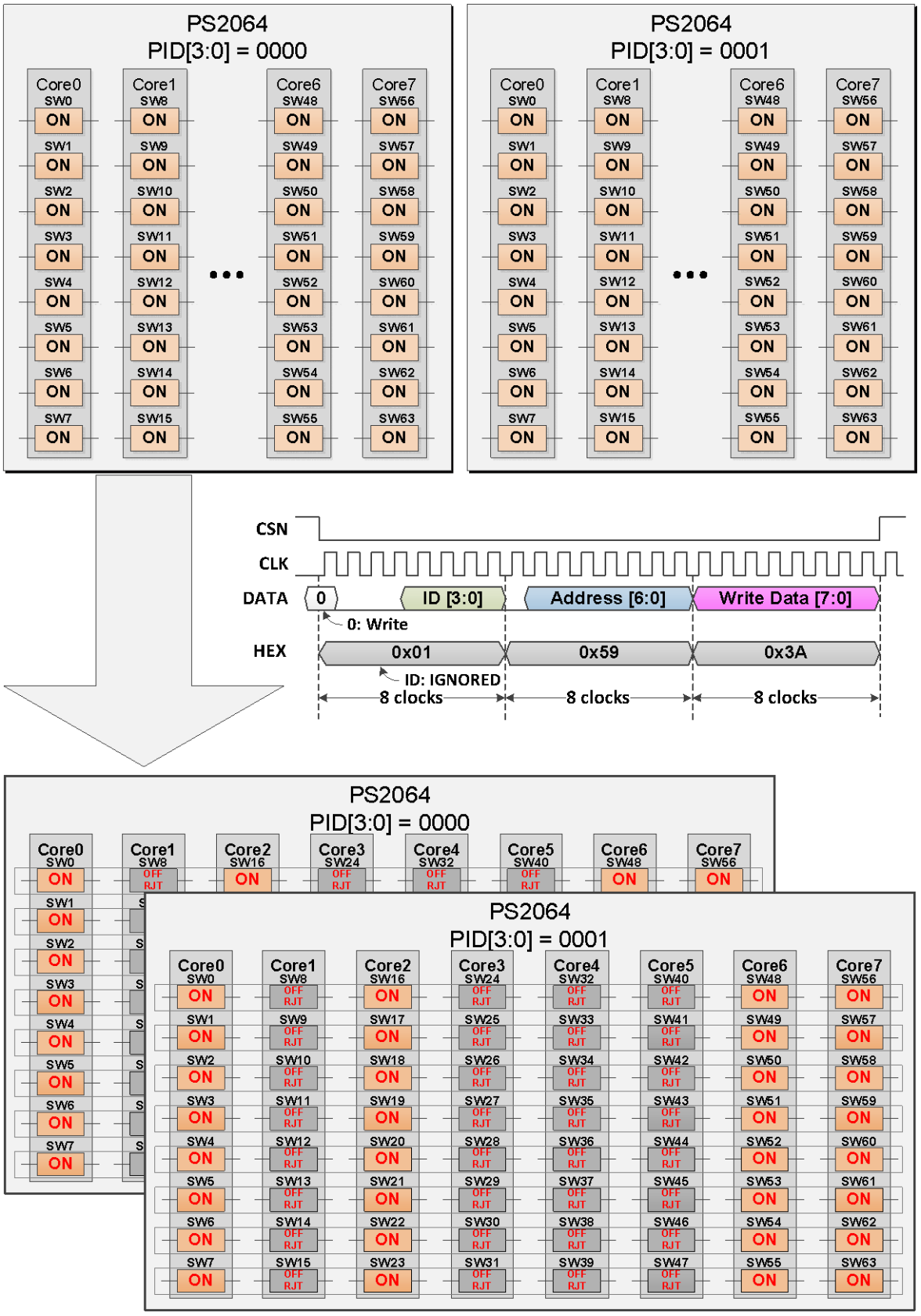


Figure 24. Example for RJT_BNK_ACH Command.

In Figure 13, all PS2064 devices within the BANK are targets. Therefore, the ID is ignored. Each bit of Write Data decides REJECT flags of all Channels. From bit0 to bit7 of Write Data[7:0] corresponds to Switch0 to Switch7 of each Channel. In Channel0, since bit1, bit3, bit4 and bit5 are '1's, REJECT flags of SW8, SW24, SW32, SW40 are set to '1'. When the REJECT flag is set to '1', the switch is status 'OFF'.

Note that Write Data bit's value '1' does not mean 'Clear REJECT flag', but 'Set REJECT flag'. Once REJECT flags are set, they can be cleared only RST_BNK or INIT_BNK commands.

- ***RJT_BNK_SCR (0x5A)***

RJT_BNK_SCR command controls the REJECT flags of one Core of the PS2064 in the selected BANK. According to each bit's value of Write Data[7:0], it sets REJECT flags for the eight switches of one Core. The target Channel is specified by ID. Figure 13 shows an example for RJT_BNK_SCR command.

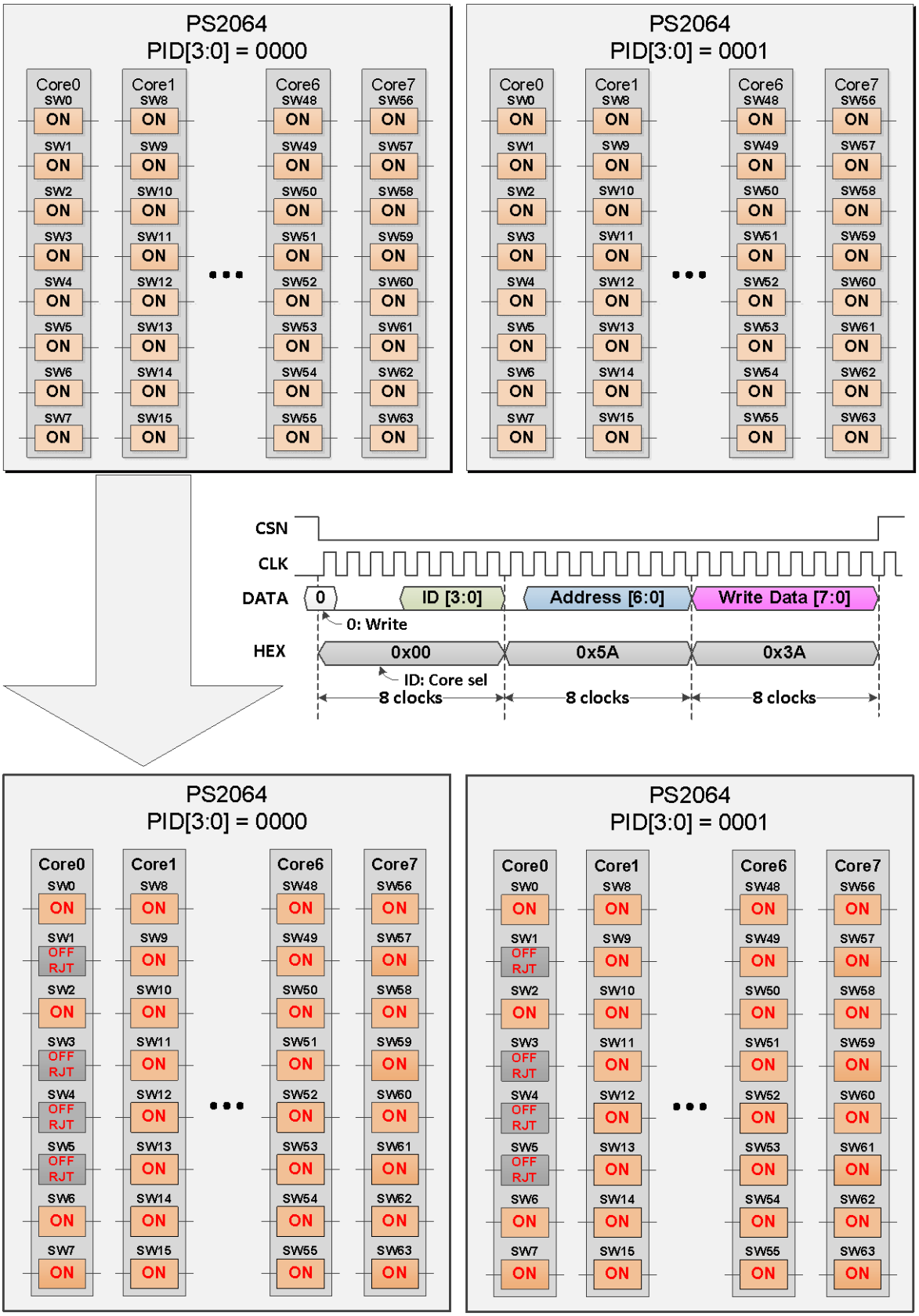


Figure 25. Example for RJT_BNK_SCR Command.

In Figure 13, one Core of all PS2064 devices within the BANK is the target. Here, the ID selects the Core0. Each bit of Write Data[7:0] corresponds to SW0 to SW7 of each Core. In Core0, since bit1, bit3, bit4 and bit5 are ‘1’s, REJECT flags of SW1, SW3, SW4, SW5 are set to ‘1’. When the REJECT flag is set to ‘1’, the switch is status ‘OFF’.

Note that Write Data bit’s value ‘1’ does not mean ‘Clear REJECT flag’, but ‘Set REJECT flag’. Once REJECT flags are set, they can be cleared only RST_BNK or INIT_BNK commands.

- ***RJT_BNK_SCH (0x5B)***

RJT_BNK_SCH command controls the REJECT flags of one Channel of the PS2064 in the selected BANK. According to each bit's value of Write Data[7:0], it sets REJECT flags for the eight switches of one Channel. The target Channel is specified by ID. Figure 13 shows an example for RJT_BNK_SCH command.

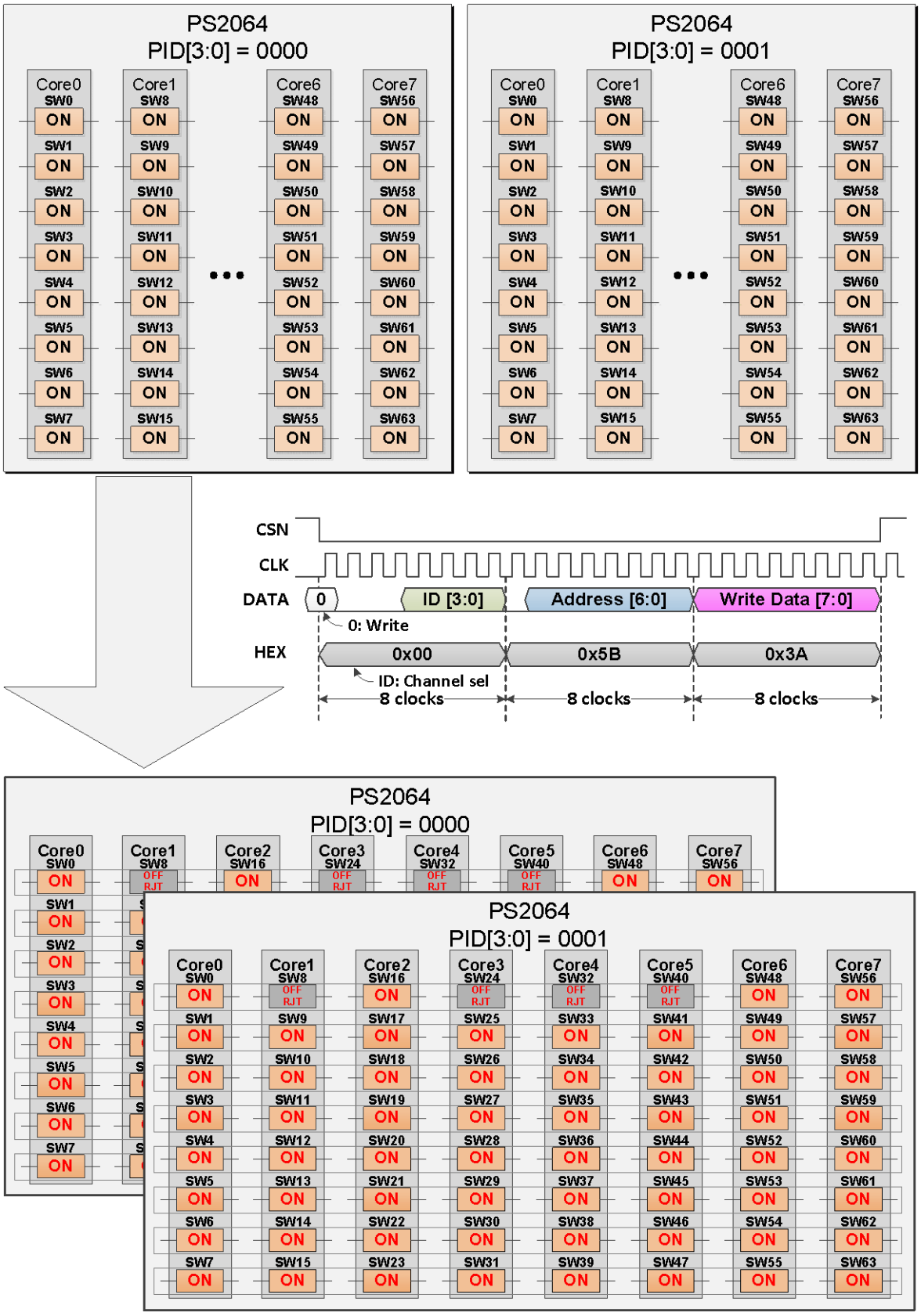
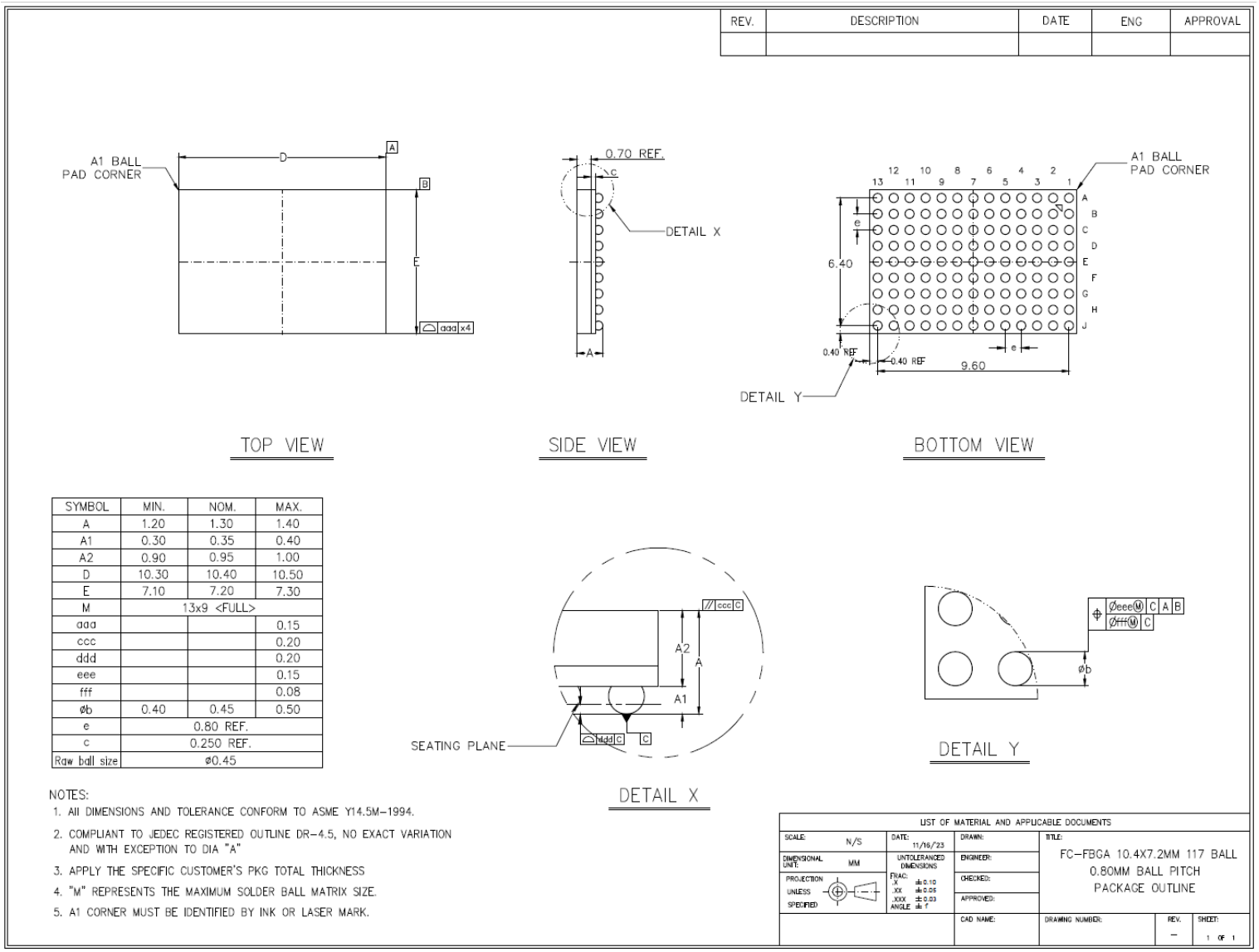


Figure 26. Example for RJT_BNK_SCH Command.

In Figure 13, one Channel of all PS2064 devices within the BANK is the target. Here, the ID selects the Channel0. Each bit of Write Data[7:0] corresponds to SW0 to SW7 of each Channel. In Channel0, since bit1, bit3, bit4 and bit5 are ‘1’s, REJECT flags of SW8, SW24, SW32, SW40 are set to ‘1’. When the REJECT flag is set to ‘1’, the switch is status ‘OFF’.

Note that Write Data bit’s value ‘1’ does not mean ‘Clear REJECT flag’, but ‘Set REJECT flag’. Once REJECT flags are set, they can be cleared only RST_BNK or INIT_BNK commands.

PACKAGE INFORMATION



SYMBOL	MIN.	NOM.	MAX.
A	1.20	1.30	1.40
A1	0.30	0.35	0.40
A2	0.90	0.95	1.00
D	10.30	10.40	10.50
E	7.10	7.20	7.30
M	13x9 <FULL>		
aaa			0.15
ccc			0.20
ddd			0.20
eee			0.15
fff			0.08
øb	0.40	0.45	0.50
e	0.80 REF.		
c	0.250 REF.		
Raw ball size	ø0.45		

Figure 27. Package Information.

APPLICATION EXAMPLE

IC and Package Information

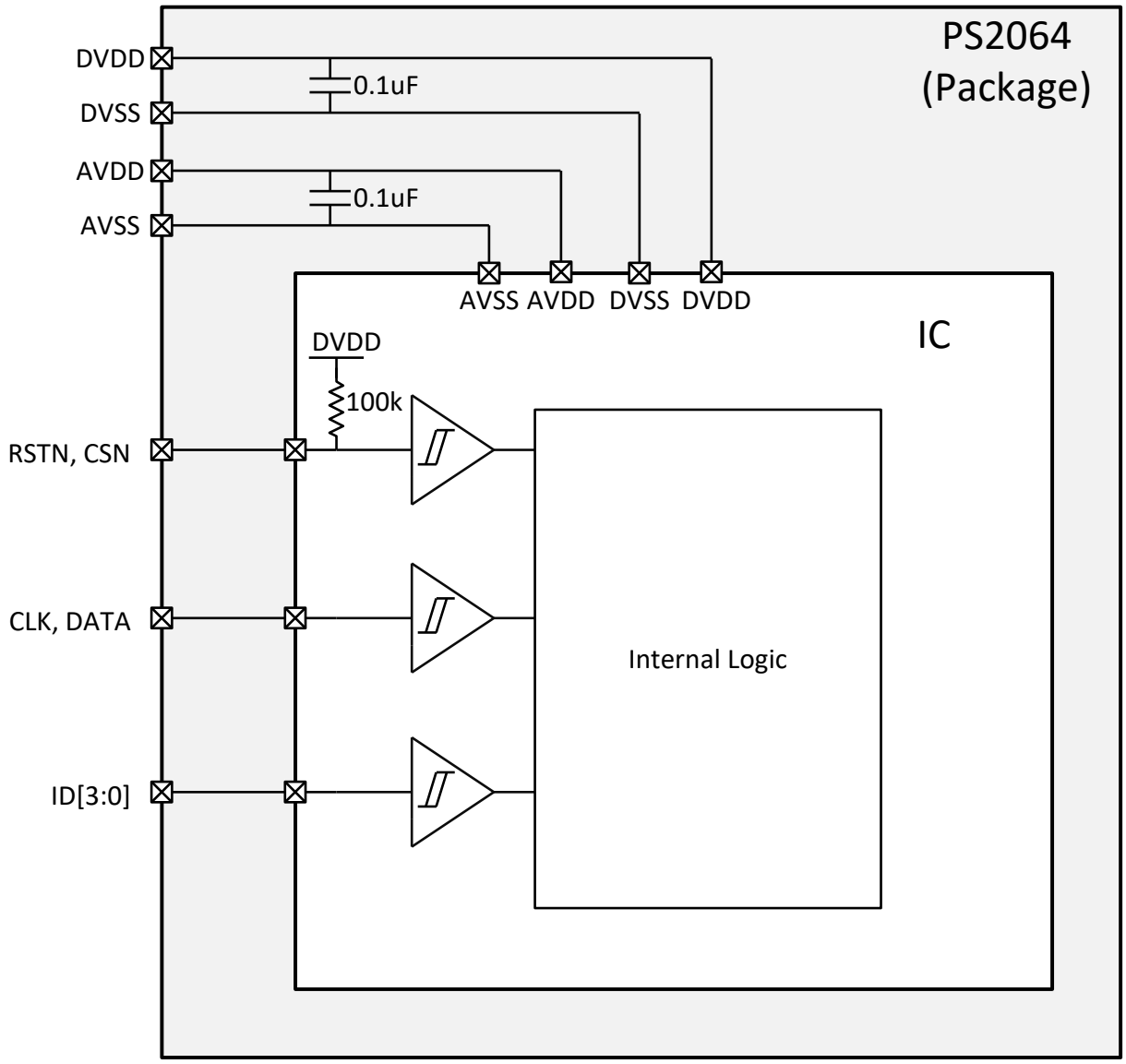
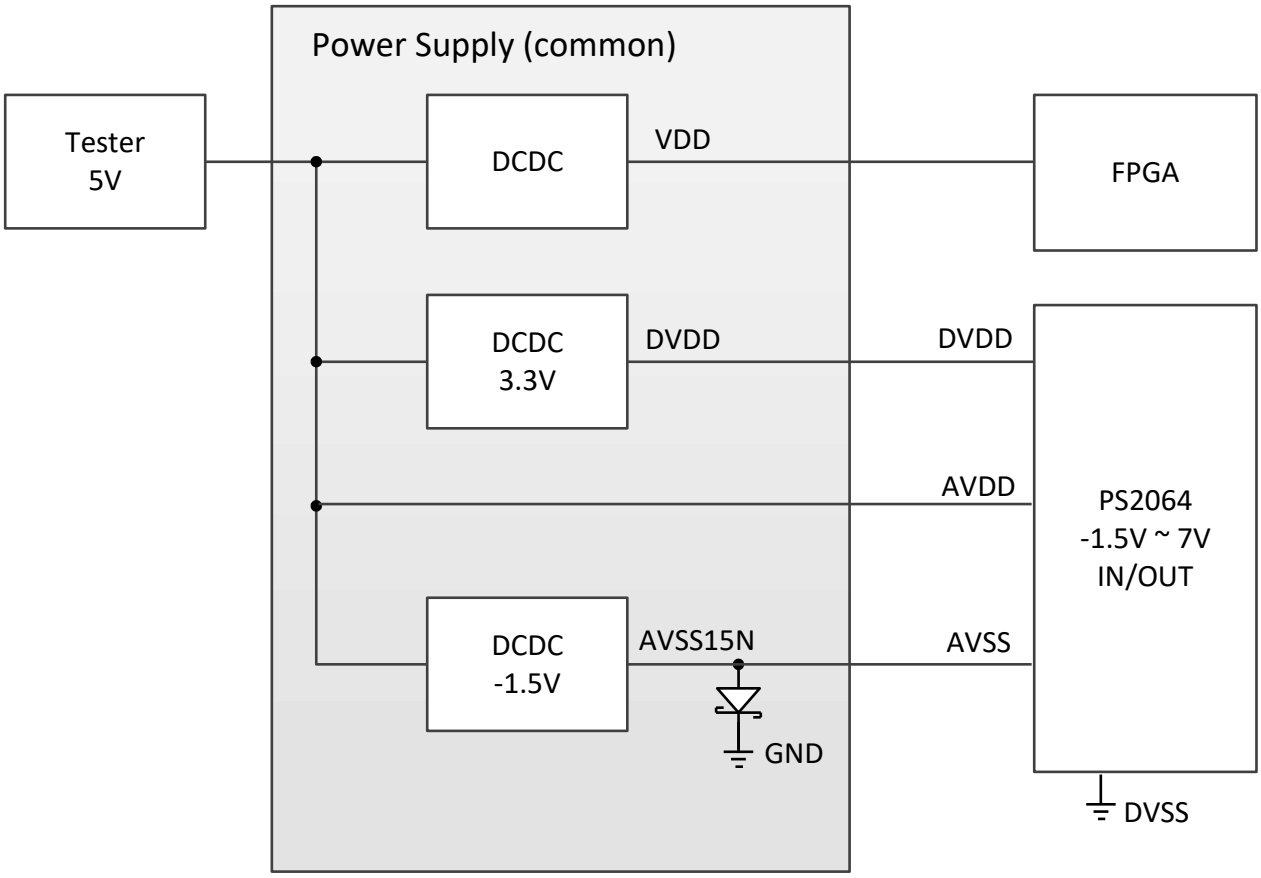


Figure 28. IC and package information

PS2064 includes all the passive components required for more stable operation. All the bypass capacitors, between AVDD and AVSS and between DVDD and DVSS, are embedded in the package. All the pull-up and pull-down resistors are included in the I/O block of the IC.

Power Supply Configuration



(a) In case of using 5V power supply directly for AVDD

Figure 29. Application Example

PS2064 IC can support bipolar configuration that negative voltage less than ground level can be applied to AVSS. When AVDD is 5.0V, AVSS can be lowered to -1.5V. When using the negative voltage to AVSS, to prevent latch-up phenomenon of PS2064 IC, a Schottky barrier diode should be attached between AVSS (anode) and DVSS (cathode). Without this protection diode, permanent malfunction of PS2064 IC may occur occasionally.

Control I/O Pin Connection

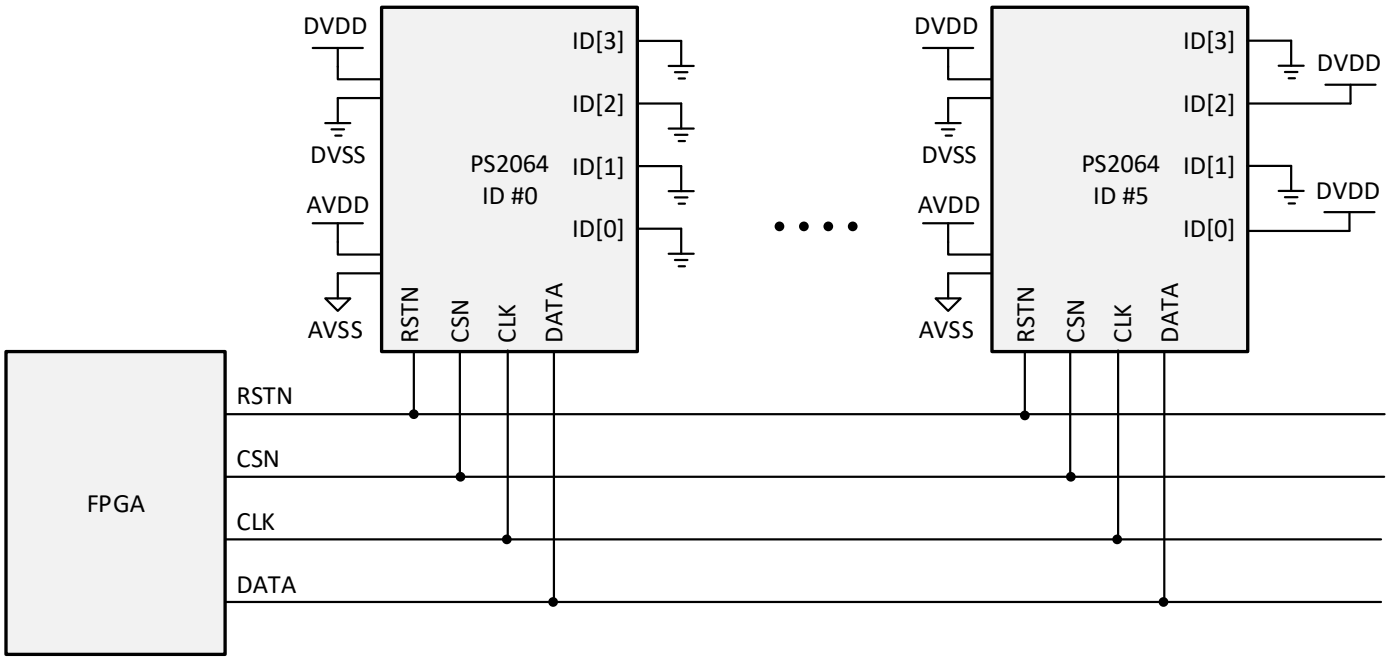


Figure 30. Recommended I/O connection

PS2064 ICs can share their control pins such as CSN, RSTN, CLK and DATA. Figure 32 shows the I/O pin configuration in case of using the signal from FPGA. To assign the ID, connect the ID[3:0] pin to DVDD or GND as shown in Figure 32. Any pull-up/down resistor or bypass capacitor is not required to be attached.

REVISION HISTORY

Revision	Date	Description
0.0	2024-02	Initial draft

DOCUMENT INFORMATION

Document name: PS2064 Datasheet
Product code: PS2064
Product description: Analog Switch IC
Document revision: 0.0
Revision date:

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