

# MCC16 Datasheet

## 16-Channel Current Limit Switch IC

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**Preliminary**



The world is driven by analog

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## GENERAL DESCRIPTION

The MCC16 IC is programmable current limit Switch IC for power management. This switch IC limits the current to prevent damage due to excessive load. Switch fabricated with an advanced submicron CMOS process that provides low power dissipation, low on resistance, and low leakage currents. The current limit level of the switch IC is 190mA to 240mA. They also got a thermal shutdown function will automatically turn off the channel temperature exceeds 150°C. The off-leakage current is under 20nA at hot temperature.

All digital inputs have 0.8-V to 2.5-V input noise margin to ensure TTL/CMOS-logic compatibility when using a 3.3-V power supply.

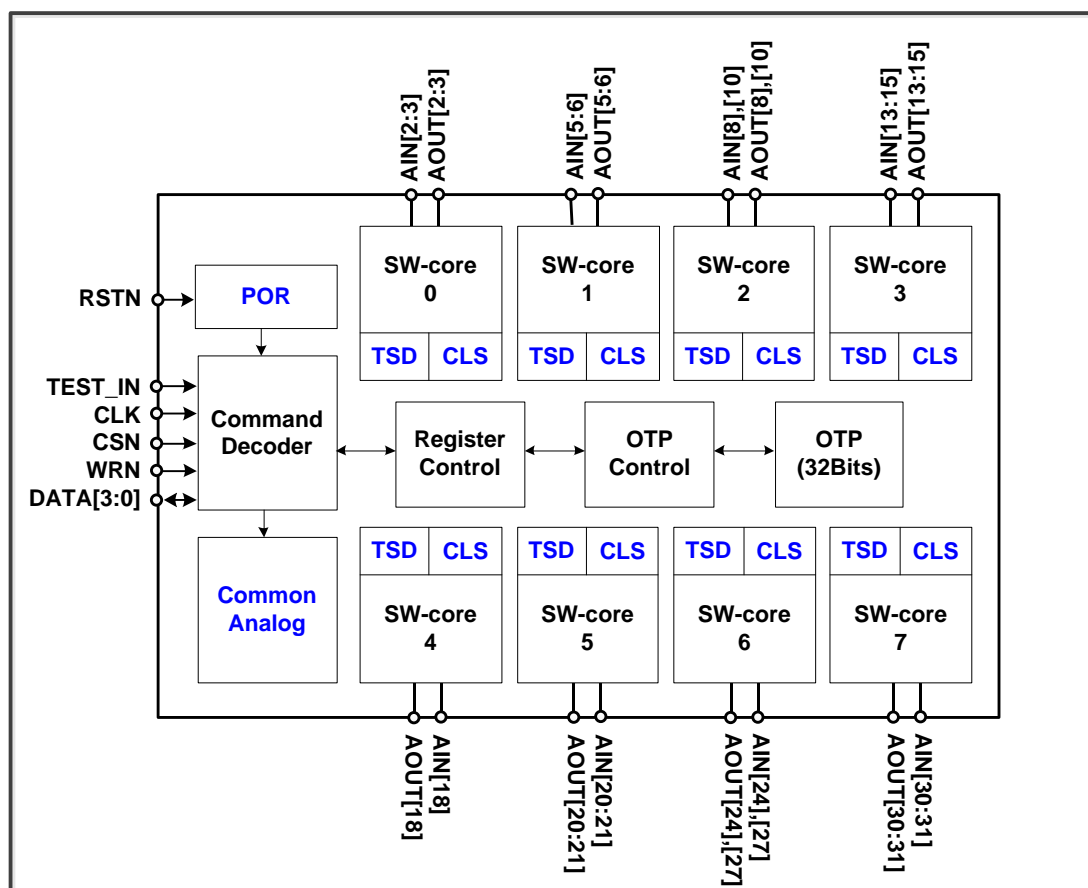
## FEATURE

3.3V logic-compatible input ( $V_{IH}=2.5V$ ,  $V_{IL}=0.8V$ )  
 Dual supply operation: 3.3V for digital, 5V for analog.  
 Analog signal frequency: DC-to-10kHz  
 Low on-resistance: 0.25Ω (@typ)  
 Analog input range from 1.5V to 5.0V (@max)  
 Limit current on analog input: 190mA~240mA  
 Thermal shutdown temperature: 150°C  
 Chip-ID programmable with OTP memory  
 Multi-channel switch control  
 Switching control using CMOS interface command  
 49-pin WL-CSP package

## APPLICATIONS

Power distribution system  
 Industrial equipment  
 Memory test

## FUNCTIONAL BLOCK DIAGRAM



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# **MCC16 Specification      16-Channel Current Limit Switch IC**

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## PIN MAPPING TABLE

	1	2	3	4	5	6	7	
A	AVSS	CN	CP	RSTN	AOUT30	AIN30	VCP	A
B	DVDD	AVDD	DVSS	TEST_IN	AOUT27	AOUT24	AIN24	B
C	AOUT31	AIN31	AOUT2	AIN2	CSN	AIN27	AOUT20	C
D	AOUT3	AIN3	DATA[0]	WRN	AOUT21	AIN21	AIN20	D
E	DATA[2]	DATA[3]	CLK	DATA[1]	DVDD	AIN18	AOUT18	E
F	AIN5	AOUT5	AIN6	AOUT6	AIN14	AOUT14	AOUT15	F
G	AIN8	AOUT8	AIN10	AOUT10	AIN13	AOUT13	AIN15	G
	1	2	3	4	5	6	7	

## PIN DESCRIPTIONS

PIN NAME	I/O	Descriptions
CLK	DI	System clock
RSTN	DI	System reset. Active Low
CSN	DI	Chip select. Active Low
WRN	DI	Data write enable. Active Low
DATA[3:0]	DIO	Data bus
TEST_IN	DI	Tied to GND in Normal mode
AIN[*]	AI	Analog switch input
AOUT[*]	AO	Analog switch output
CN	AIO	Pumping cap. negative
CP	AIO	Pumping cap. positive
VCP	PWR	Charge pump output
AVDD	PWR	Analog Power
AVSS	GND	Analog Ground
DVDD	PWR	Digital Power
DVSS	GND	Digital Ground

AI: analog input  
DI: digital Input  
PWR: power

AO: analog output  
DIO: digital Input / Output  
GND: ground

## ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND, Unless Otherwise Noted.)

AVDD (for Analog Switch).....	-0.3V to +6.0V	Operating temperature range .....	-40°C to +125°C
DVDD (for Digital Control).....	-0.3V to +4.5V	Storage temperature range .....	-55°C to +125°C
Voltage at any digital pin .....	-0.3V to +4.5V	Junction temperature.....	+150°C
Voltage at any analog pin .....	-0.3V to +6.0V	ESD protection on all pins (HBM, MM).....	≥2kV, 200V
Continuous current into any terminal .....	450mA		
Peak current into analog switch I/O.....	800mA		
(current pulse with 1ms and 10% duty cycle)			

Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at those or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

AVDD=5.0V, AVSS=-2.5V, DVDD=3.3V, DVSS=0V, and TA = +25°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
POWER SUPPLIES							
Analog Supply Voltage		AVDD	AVSS=-2.5V	4.5	5	5.5	V
Digital Supply Voltage		DVDD		3.0	3.3	3.6	V
Analog Ground Voltage		AVSS		-3	-2.5	-1.5	V
Digital Ground Voltage		DVSS		-	0	-	V
ANALOG SWITCH							
Signal Range	Current Limited	V <sub>AIN1</sub>	AVSS=-2.5V, AVDD=5V	1.5		5	V
Channel On Limit Current		I <sub>ON_CL</sub>	AVDD=5V, V <sub>AIN</sub> =1.5V~5V	190		240	mA
Switch On-resistance		R <sub>ON</sub>	I <sub>CH_ON</sub> =10mA		0.2	0.4	Ω
Leakage Current	Input Pin	I <sub>S_OFF</sub>	AVDD=5V, AVSS=-2.5V, Channel off, V <sub>AIN</sub> =5V, V <sub>AOUT</sub> =Floating		0.005	0.01	uA
	Output Pin	I <sub>D_OFF</sub>	AVDD=5V, AVSS=-2.5V, Channel off, V <sub>AIN</sub> =Floating, V <sub>AOUT</sub> =5V		0.005	0.01	uA
	Channel On	I <sub>CH_ON</sub>	AVDD=5V, AVSS=-2.5V, Channel on, V <sub>AIN</sub> =5V, V <sub>AOUT</sub> =Floating		0.005	0.01	uA
	Channel Off	I <sub>CH_OFF</sub>	AVDD=5V, AVSS=-2.5V, Channel off, V <sub>AIN</sub> =5V, V <sub>AOUT</sub> =0V		0.005	0.01	uA
THERMAL SHUTDOWN							
Thermal shutdown temperature		T <sub>ST</sub>			+150		°C
Thermal shutdown hysteresis		T <sub>SH</sub>			20		°C



DIGITAL I/O							
Logic Input Voltage	Input High	$V_{IH}$		0.75* DVDD			V
	Input Low	$V_{IL}$				0.25* DVDD	V
Logic Input Current	Input High	$I_{IH}$		-1		1	uA
	Input Low	$I_{IL}$		-1		1	uA
SWITCH DYNAMIC CHARACTERISTICS							
Switching Time	Turn ON Time	$t_{ON}$	Clock base (calculate for special condition)		60		us
	Turn OFF Time	$t_{OFF}$	Clock base (calculate for special condition)		50		us
Current Limit Reaction Time		$t_{CLRT}$			9		us
Capacitance	Input Off-Capacitance	$C_{AIN\_OFF}$			300		pF
	Output Off-Capacitance	$C_{AOUT\_OFF}$			300		pF
	Output On-Capacitance	$C_{AOUT\_ON}$			600		pF
Switching Frequency						10	KHz
POWER CONSUMPTION							
Analog Operating Current (AVDD)	Static 1	$I_{AVDD\_ST1}$	AVDD=5V, AVSS= -2.5V		14	25	mA
	Dynamic 1	$I_{AVDD\_DYN}$	AVDD=5V, AVSS= -2.5V, $f_{CLK}=10MHz$ , $f_{SW}=10KHz$		15	25	mA
Analog Operating Current (AVSS)	Static 1	$I_{AVSS\_ST1}$	AVDD=5V, AVSS= -2.5V		14	25	mA
	Dynamic 1	$I_{AVSS\_DYN}$	AVDD=5V, AVSS= -2.5V, $f_{CLK}=10MHz$ , $f_{SW}=10KHz$ ,		15	25	mA
Digital Operating Current (DVDD)	Static 1	$I_{DVDD\_ST}$	DVDD=3.3V		2	5	mA
	Dynamic 1	$I_{DVDD\_DYN}$	DVDD=3.3V, $f_{CLK}=10MHz$ (Note2), Combined operation of Reset, and DUT-Reject		3	7	mA

**Note2. All switch On/Off operating simultaneously**

## ELECTRICAL CHARACTERISTICS

AVDD=5.0V, AVSS=-2.5V, DVDD=3.3V, DVSS=0V, and TA = +125°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
POWER SUPPLIES							
Analog Supply Voltage		AVDD	AVSS=-2.5V	4.5	5	5.5	V
Digital Supply Voltage		DVDD		3.0	3.3	3.6	V
Analog Ground Voltage		AVSS		-3	-2.5	-1.5	V
Digital Ground Voltage		DVSS		-	0	-	V
ANALOG SWITCH							
Signal Range	Current Limited	V <sub>AIN1</sub>	AVSS=-2.5V, AVDD=5V	1.5		5	V
Channel On Limit Current*		I <sub>ON_CL</sub>	AVDD=5V, V <sub>AIN</sub> =1.5V~5V	190		240	mA
Switch On-resistance		R <sub>ON</sub>	I <sub>CH_ON</sub> =10mA		0.25	0.5	Ω
Leakage Current	Input Pin	I <sub>S_OFF</sub>	AVDD=5V, AVSS=-2.5V, Channel off, V <sub>AIN</sub> =5V, V <sub>AOUT</sub> =Floating		0.015	0.02	uA
	Output Pin	I <sub>D_OFF</sub>	AVDD=5V, AVSS=-2.5V, Channel off, V <sub>AIN</sub> =Floating, V <sub>AOUT</sub> =5V		0.015	0.02	uA
	Channel On	I <sub>CH_ON</sub>	AVDD=5V, AVSS=-2.5V, Channel on, V <sub>AIN</sub> =5V, V <sub>AOUT</sub> =Floating		0.015	0.02	uA
	Channel Off	I <sub>CH_OFF</sub>	AVDD=5V, AVSS=-2.5V, Channel off V <sub>AIN</sub> =5V, V <sub>AOUT</sub> =0V		0.015	0.02	uA
THERMAL SHUTDOWN							
Thermal shutdown temperature		T <sub>ST</sub>			+150		°C
Thermal shutdown hysteresis		T <sub>SH</sub>			20		°C
DIGITAL I/O							
Logic Input Voltage	Input High	V <sub>IH</sub>		0.75* DVDD			V
	Input Low	V <sub>IL</sub>				0.25* DVDD	V
Logic Input Current	Input High	I <sub>IH</sub>		-1		1	uA
	Input Low	I <sub>IL</sub>		-1		1	uA
SWITCH DYNAMIC CHARACTERISTICS							
Switching Time	Turn ON Time	t <sub>ON</sub>	Clock base (calculate for special condition)		60		us
	Turn OFF Time	t <sub>OFF</sub>	Clock base (calculate for special condition)		50		us

Current Limit Reaction Time		tCLRT			14		us
Capacitance	Input Off-Capacitance	C <sub>AIN_OFF</sub>			300		pF
	Output Off-Capacitance	C <sub>AOUT_OFF</sub>			300		pF
	Output On-Capacitance	C <sub>AOUT_ON</sub>			600		pF
Switching Frequency						10	KHz
<b>POWER CONSUMPTION</b>							
Analog Operating Current (AVDD)	Static 1	I <sub>AVDD_ST1</sub>	AVDD=5V, AVSS= -2.5V		15	25	mA
	Dynamic 1	I <sub>AVDD_DYN</sub>	AVDD=5V, AVSS= -2.5V, f <sub>CLK</sub> =10MHz, f <sub>SW</sub> =10KHz,		17	25	mA
Analog Operating Current (AVSS)	Static 1	I <sub>AVSS_ST1</sub>	AVDD=5V, AVSS= -2.5V		15	25	mA
	Dynamic 1	I <sub>AVDD_DYN</sub>	AVDD=5V, AVSS= -2.5V, f <sub>CLK</sub> =10MHz, f <sub>SW</sub> =10KHz,		17	25	mA
Digital Operating Current (DVDD)	Static 1	I <sub>DVDD_ST</sub>	DVDD=3.3V		2	5	mA
	Dynamic 1	I <sub>DVDD_DYN</sub>	DVDD=3.3V, f <sub>CLK</sub> =10MHz(Note3), Combined operation of Reset, and DUT-Reject		3	7	mA

**Note3. All switch On/Off operating simultaneously**

## TIMING CHARACTERISTICS

AVDD=5.0V, AVSS=-2.5V, DVDD=3.3V, DVSS=0V, and TA = +25°C ~ +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
DIGITAL I/O SIGNALS						
CLK Period	t <sub>PERIOD</sub>		20			ns
CLK Frequency	f <sub>CLK</sub>				50	MHz
DATA to CLK Setup Time	t <sub>DS</sub>		10			ns
DATA to CLK Hold Time	t <sub>DH</sub>		5			ns
CSN to CLK Setup Time	t <sub>CS</sub>		10			ns
CSN to CLK Hold Time	t <sub>CH</sub>		5			ns
WRN to CLK Setup Time	t <sub>WS</sub>		10			ns
WRN to CLK Hold Time	t <sub>WH</sub>		5			ns
POWER AND RESET SEQUENCE						
Power-up Period	t <sub>PU</sub>		500			us
Power-down Period	t <sub>PD</sub>		500			us
Power-on Reset Time	t <sub>RST</sub>		500			us
OTP Read Time	t <sub>ORD</sub>	CLK freq. >= 10MHz	200			us
		CLK freq. < 10MHz	2000			cycle
SWITCH ON/OFF TIMING DIAGRAM						
1-Clock Command Control Time	t <sub>SW1</sub>				3	cycle
2-Clock Command Control Time	t <sub>SW2</sub>				6	cycle

## Timing Diagram of Digital I/O Signals

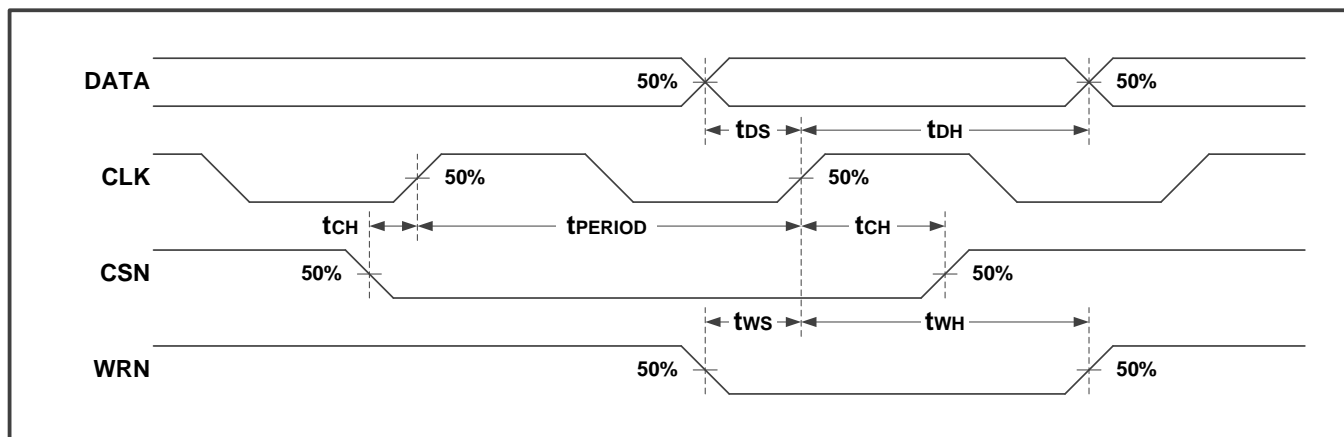
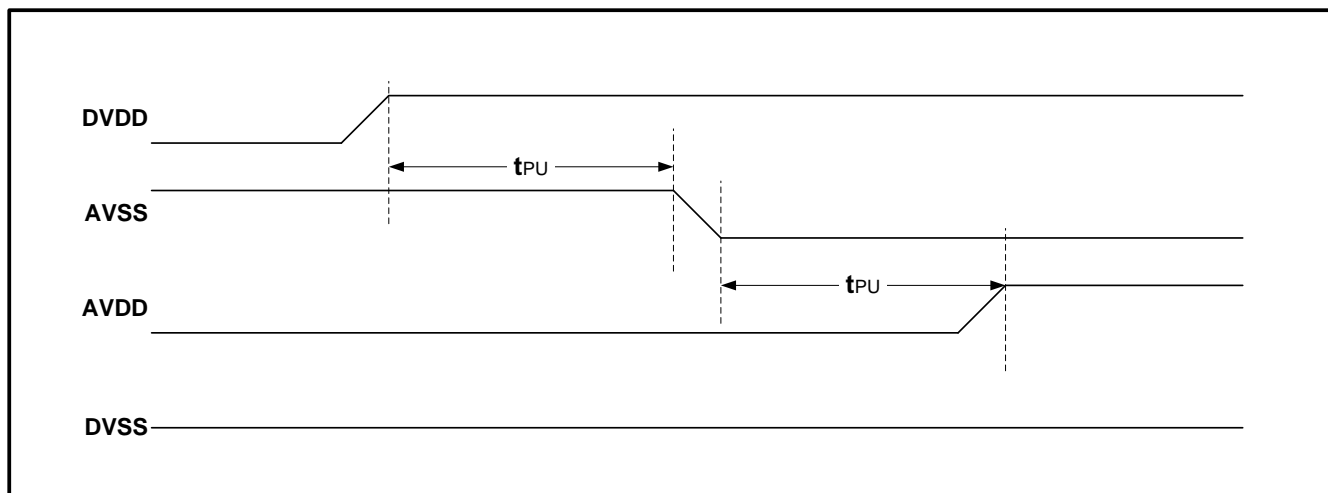


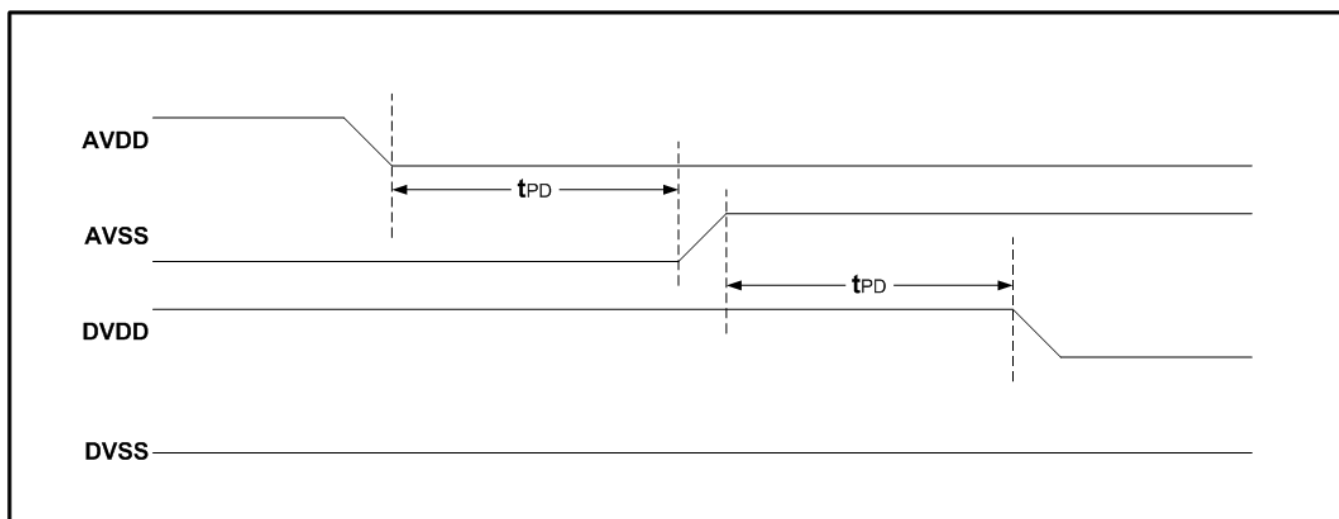
Figure 1. Timing Diagram of Digital Signals.

## Power and Reset sequence



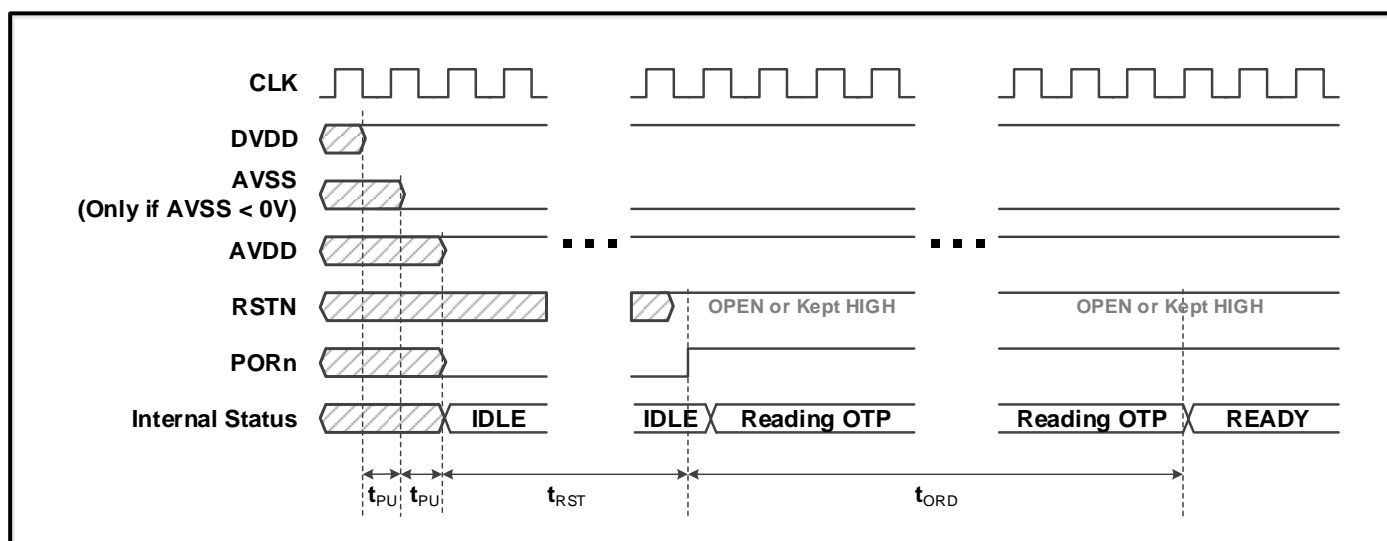
In case AVSS &lt; 0 V

Figure 2. Power-up Sequence.

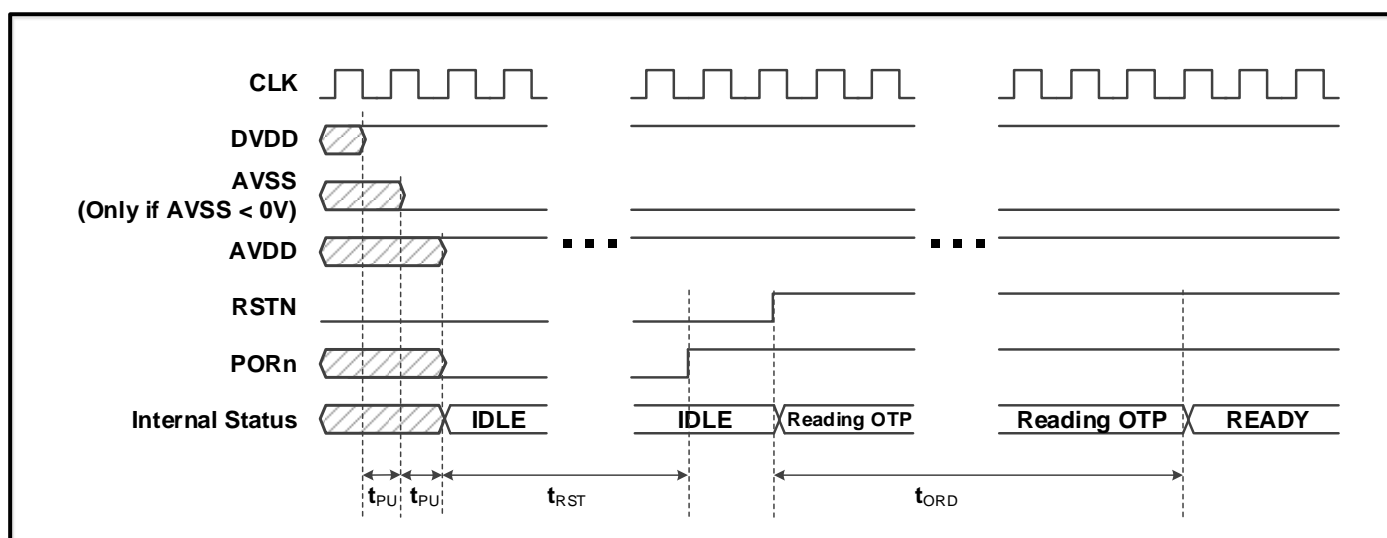


In case AVSS &lt; 0 V

Figure 3. Power-down Sequence.



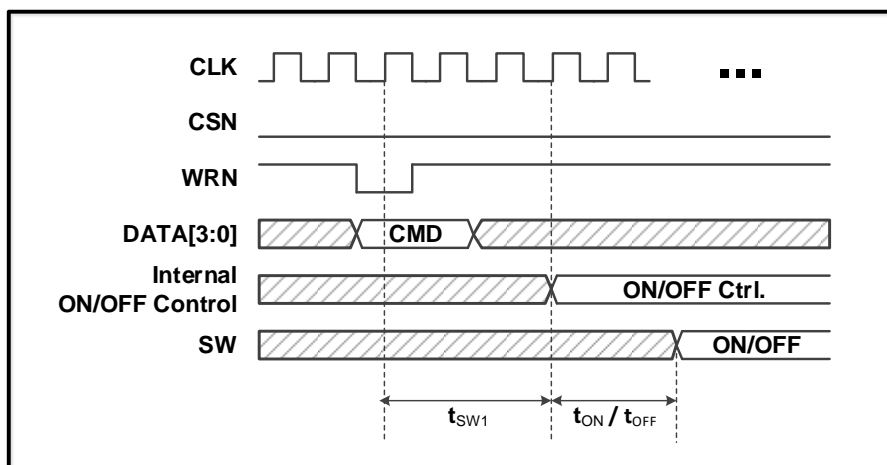
(a) In case RSTN is OPEN or kept HIGH before  $(t_{PU} + t_{PU} + t_{RST})$ .



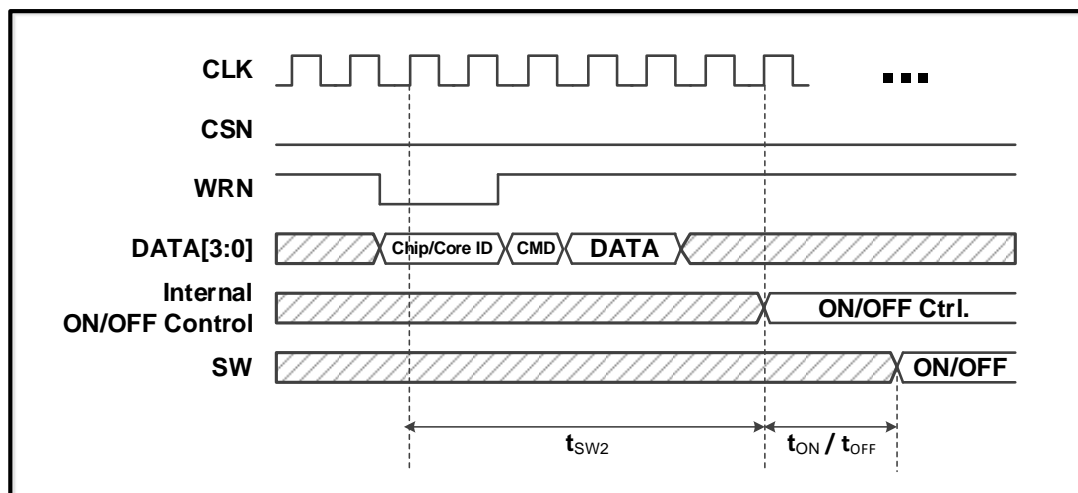
(b) In case RSTN changes from LOW to HIGH after  $(t_{PU} + t_{PU} + t_{RST})$ .

**Figure 4. Reset and Stand-by Sequence.**

## Switch On/Off Timing Diagram



(a) 1-clock command switch on/off timing diagram.



(b) 2-clock command switch on/off timing diagram.

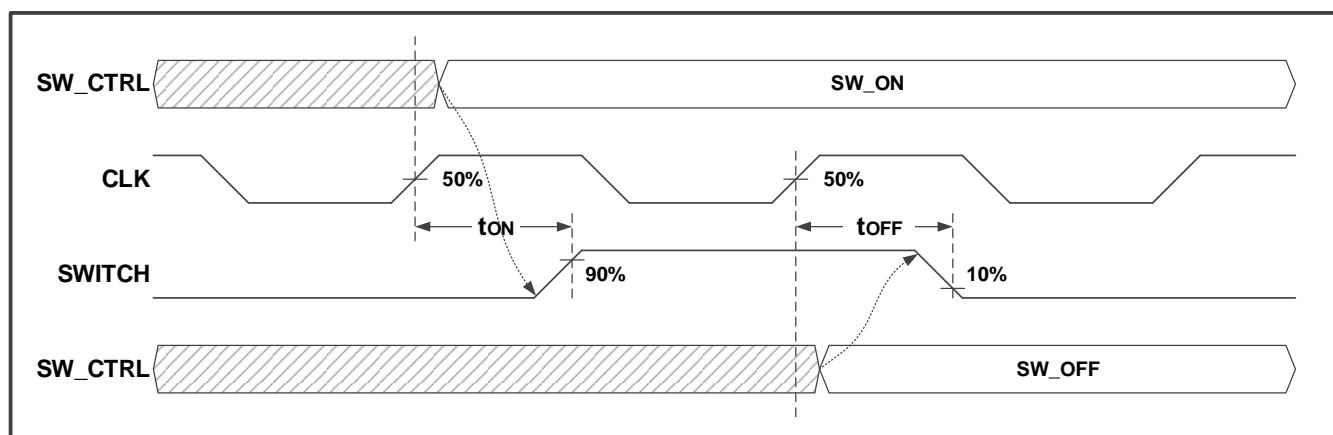
(c) Detail  $t_{ON} / t_{OFF}$  timing diagram.

Figure 5. Switch On/Off Timing Diagram.



## FUNCTIONAL DESCRIPTION

### Internal Structure

MCC16 is analog switches with control logic. It consists of 8 switching Cores and control logics. Since each switching Core has 1, 2 or 3 switches, a MCC16 contains 16 switches.

The switches in MCC16 can also be grouped into Channels. A Channel indicates the switches of the same ID in all cores. For example, Channel1 indicates Switch1s in Core0, Core1, Core2,..., and Core7. The host can control the switches either by Cores or Channels.

Note that the control of the switches is also based on even numbered switches. Only control registers for even numbered switches are used for actual control of the switches. For example, to turn on / off the AIN[2] – AOUT[2] current path, Core0 SW4's control register should be set to proper value. On the other hand, changing the values of switch control registers for Core0 SW6 has no effect on AIN[2] – AOUT[2] current path.

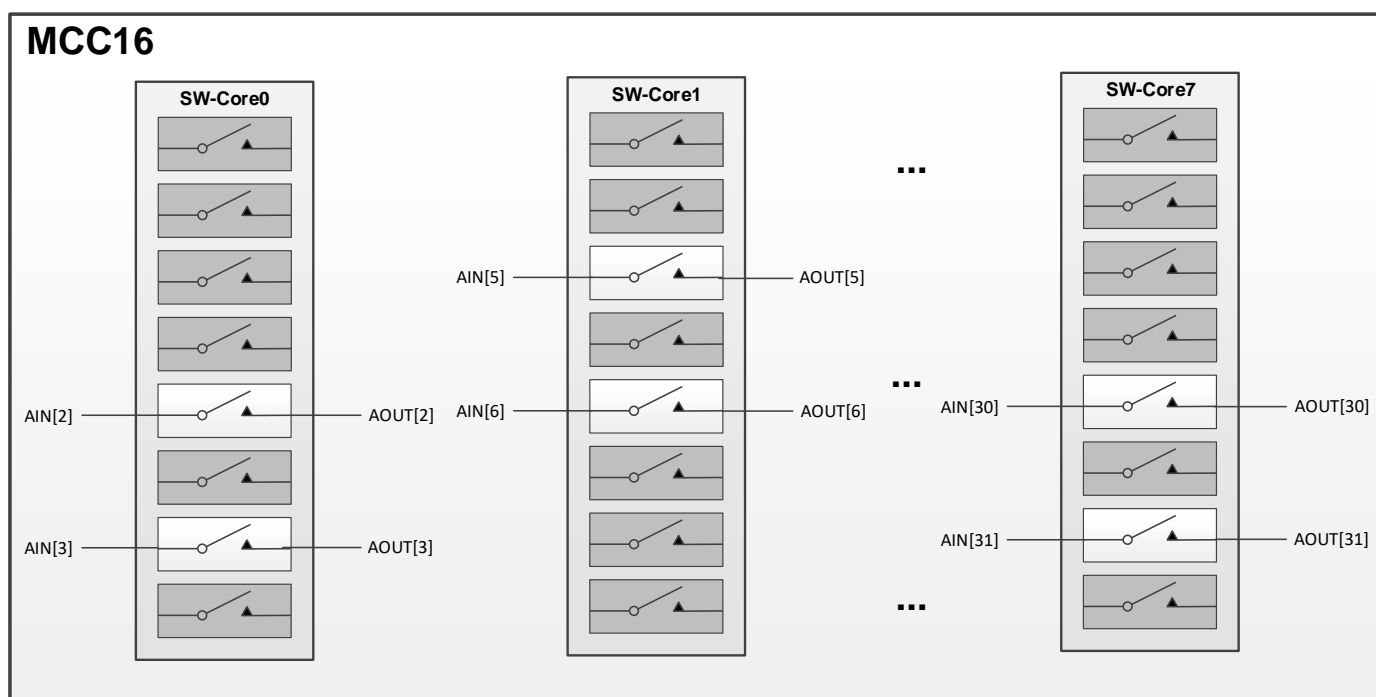


Figure 6. Internal Structure of MCC16.

Each CORE has a different number of AIN-AOUT paths (One, two, or three). For example, AIN[2]-AOUT[2], AIN[3]-AOUT[3] in CORE0, AIN[13]-AOUT[13], AIN[14]-AOUT[14], AIN[15]-AOUT[15] in CORE3 and AIN[18]-AOUT[18] in CORE4. Paths belonging to those COREs are shown in Figure 7 below.

Core #0		Core #1		Core #2		Core #3	
Input	Output	Input	Output	Input	Output	Input	Output
				AIN8	AOUT8		
		AIN5	AOUT5			AIN13	AOUT13
AIN2	AOUT2	AIN6	AOUT6	AIN10	AOUT10	AIN14	AOUT14
AIN3	AOUT3					AIN15	AOUT15

Core #4		Core #5		Core #6		Core #7	
Input	Output	Input	Output	Input	Output	Input	Output
		AIN20	AOUT20	AIN24	AOUT24		
		AIN21	AOUT21				
AIN18	AOUT18					AIN30	AOUT30
				AIN27	AOUT27	AIN31	AOUT31

Figure 7. MCC16 AIN-AOUT Paths.

### Connection

In system application, control signals can be shared among multiple MCC16s. Figure 8 shows an example for the connection of multiple MCC16s.

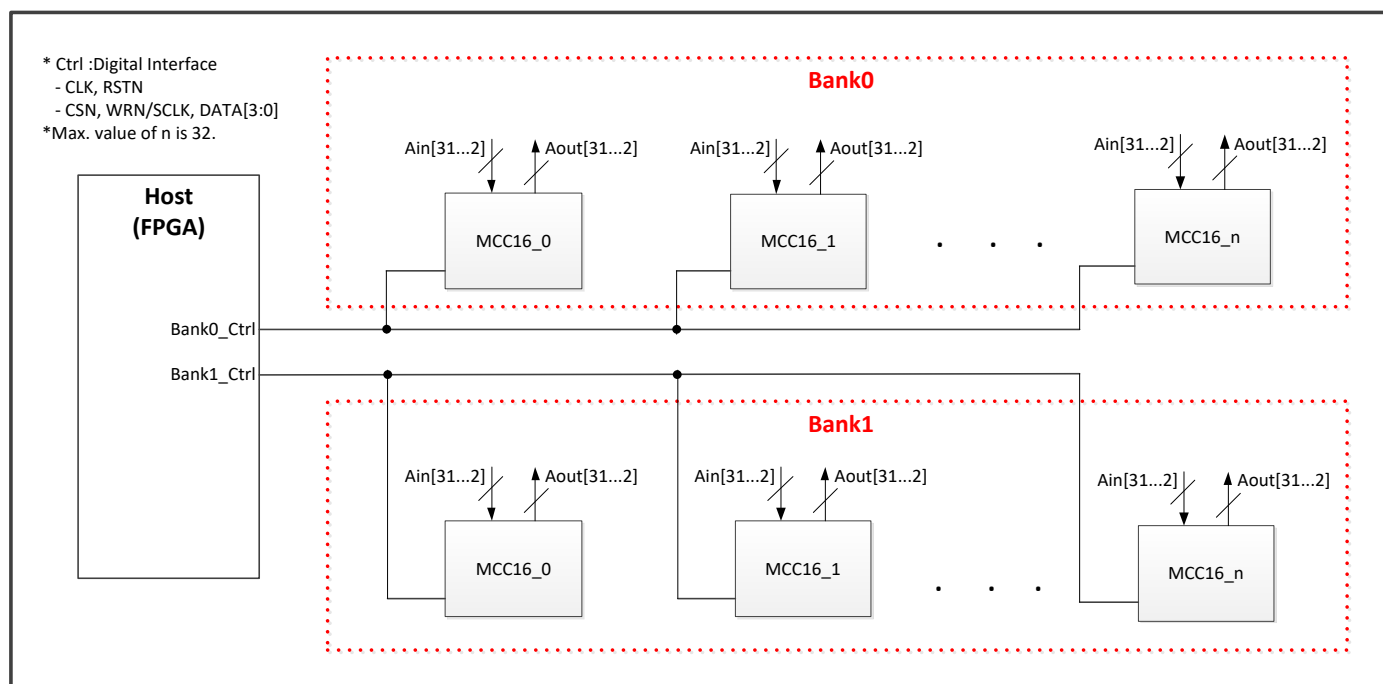


Figure 8. Example for connecting MCC16s.

MCC16s with the same control signals are called Bank. Since there are multiple MCC16s in a Bank, there should be a way to specify the target chip for the control commands. To support this, Chip-ID is used.

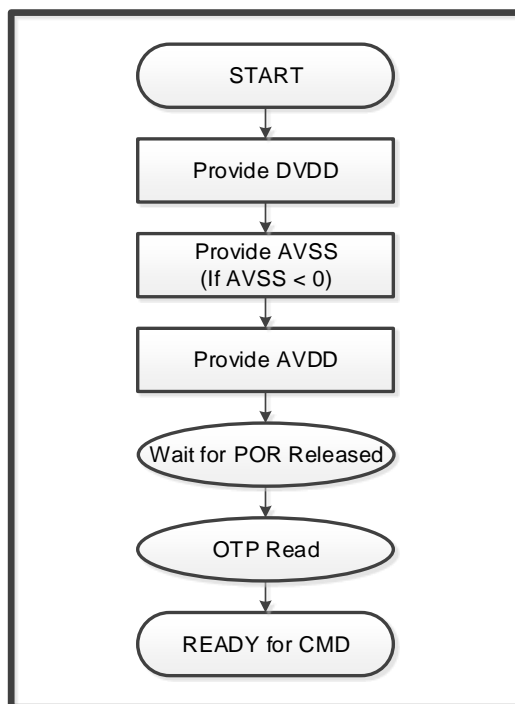
Chip-ID is a 5-bit number decided either from the internal OTP memory. Each MCC16 acquires its Chip-ID on bootstrap, and user can specify the target chip of the control commands by sending target Chip-ID with them. Since Chip-ID is a 5-bit number, the maximum number of MCC16s in one bank is 32.

### Power-up Sequence

MCC16 requires two kinds of Power/Ground pairs – AVDD/AVSS and DVDD/DVSS. As the names imply, AVDD/AVSS pair is for Analog circuits, and DVDD/DVSS pair is for Digital logic. To ensure reliable operation on power-up, it is required that each Power and Ground should be provided in proper order.

**Figure 9. Power-up Sequence**

Figure 9 shows the Power-up sequence of MCC16.



**Figure 9. Power-up Sequence**

As depicted in Figure 9, the logic power, DVDD, should be provided first. If AVDD is provided prior to DVDD, the switch control logic's state is undefined until DVDD is supplied, which may unintentionally turn on the switches before DVDD is supplied. Note that for negative AVSS, AVSS also should be provided after DVDD, because negative AVSS means a certain voltage ( $AVDD - AVSS$ ) is applied to the analog circuit.

If MCC16 is supplied with DVDD and AVDD, the internal POR of MCC16 generates RESET signal internally, and MCC16 changes to RESET state until the RESET signal from POR is released. RESET from POR is released after  $t_{RST}$ , and MCC16 starts reading its own internal OTP memory.

External RESET is also supported through a pin named RSTN, and actual RESET signal is generated from both POR and RSTN signals. This leads to that on power-up, if RSTN is released before POR is released (i.e. RSTN changes from LOW to HIGH before  $t_{PU} + t_{PU} + t_{RST}$  is elapsed), actual RESET signal is still active (i.e. RESET is being issued) until RESET from POR is released. On the other hand, if RSTN is kept LOW though POR is released, actual RESET signal is still active until RSTN is released.

However, since RSTN pin is internally pulled-up, user may leave RSTN pin OPEN in most of the cases. For the detailed timing of power-up sequence, refer to *Figure 2. Power-up Sequence*.

### Interface Protocol & Types of Commands

Controlling MCC16s is performed through commands from the host. The host sends commands through two control signals (CSN and WRN) and 4-bit wide data pins. CSN signal is used to select the target Bank, and WRN signal decides the type of the command. The protocol for each command is decided by the type of the command – 1/2 clock commands.

### - 1-Clock Commands (Writing Commands Only)

1-clock commands are the commands for which WRN signal goes LOW for single cycle. Figure 10 shows the timing diagram for 1-clock commands.

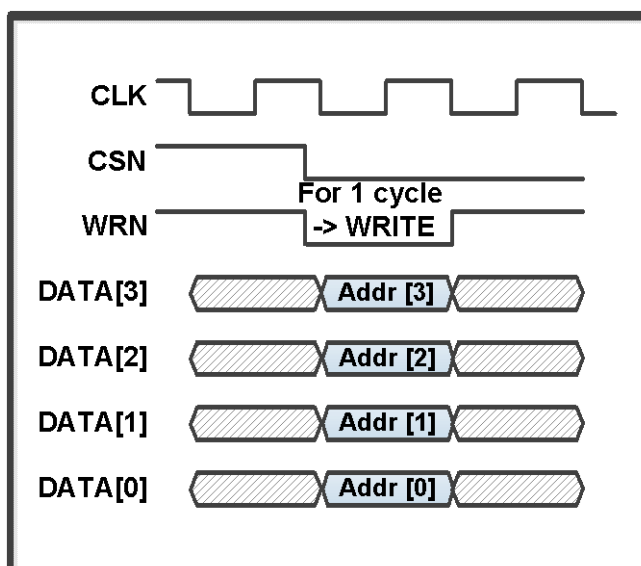


Figure 10. Timing Diagram for 1-Clock Commands.

The 1-clock commands consist of the commands which are applied to all switches of all MCC16s in the bank. Since the target for the 1-clock command is all switches in all Cores of all MCC16s, they require neither Chip ID nor Core ID.

### - 2-Clock commands (Writing Commands Only)

2-clock commands are the commands for which WRN signal goes LOW for two clocks. Each command includes Chip-ID, Core-ID, Command, and Parameters, and it is mainly used to control the switches. Figure 11 shows the timing diagram for 2-clock commands.

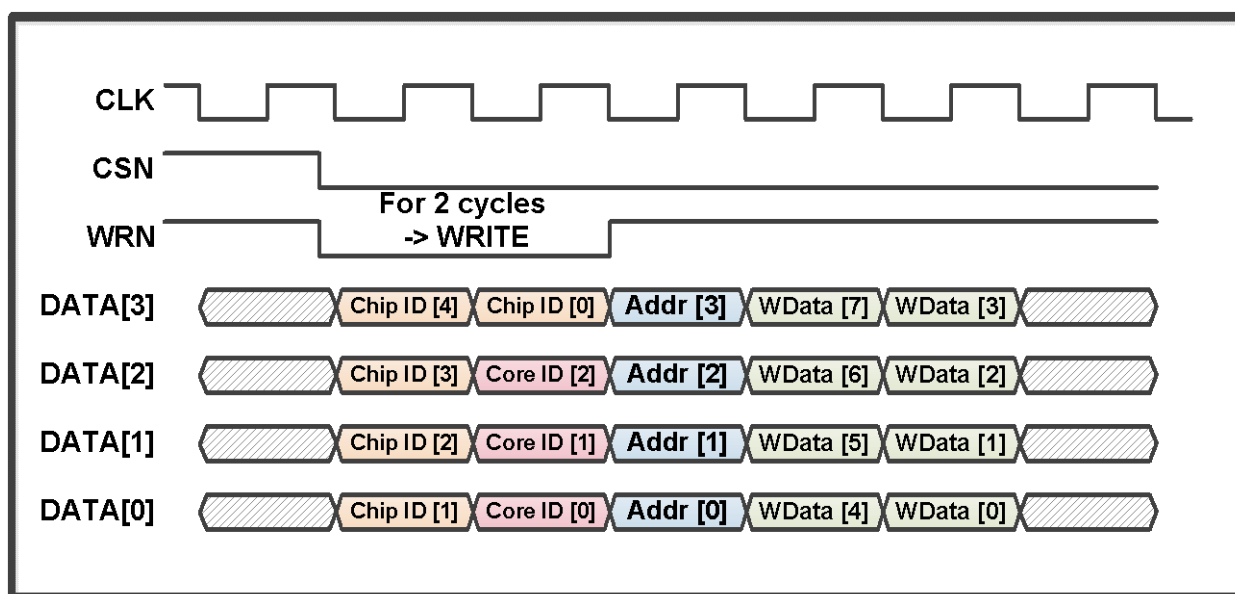


Figure 11. Timing Diagram for 2-Clock commands.

As shown in Figure 11, IDs and commands are received through DATA[3:0] pins. Chip-ID specifies the target MCC16

in the bank, and Core-ID specifies the target Core / Channel of the target chip. Addr[3:0] is the actual command, and WData[7:0] is a parameter to control the states of the 8 switches specified by Chip-ID and Core-ID. All of the 2-clock commands are for writing WData[7:0] to target registers.

## Controlling Switches

### - States of Switches

The main usage of MCC16 is to control AIN – AOUT connection by changing the states of its switches. Each switch can be in one of two states – ON, OFF.

In **ON** state, the switch is turned-on, and the AIN signal is CONNECTED to the corresponding AOUT signal.

In **OFF** state, the switch is turned-off, and the AIN signal is DISCONNECTED from the corresponding AOUT signal.

Besides ON/OFF states, each switch has an additional flag named **REJECT**. If REJECT flag is set for a switch, the switch changes to OFF state automatically, and further commands to turn on the switch are ignored. Only special 1-clock commands or external reset (RSTN) can clear the REJECT flag.

### - Initialization of Switches

The initialization of the switches can be done through initialization commands. There are four initialization commands. They are,

- > 1-clock command 0x2: RESET\_ALL
- > 1-clock command 0x3: CLEAR\_ALL
- > 1-clock command 0x4: ENABLE\_ALL
- > 1-clock command 0x5: INITIAL\_ALL

Since all of these commands are 1-clock commands, they are executed by all MCC16s in the selected bank by CSN signal. The states of all switches in the bank are simultaneously changed by these commands, and it helps set the initial states of all switches with less commands. For the detailed information about each command, refer to *Commands Descriptions*.

### - Changing States of Switches

To change the states of switches, DIRECT\_XXX commands are used.

- > 2-clock command 0x2: DIRECT\_CHP\_COR
- > 2-clock command 0x3: DIRECT\_BNK\_COR
- > 2-clock command 0x5: DIRECT\_CHP\_CHN
- > 2-clock command 0x6: DIRECT\_BNK\_CHN
- > 2-clock command 0xA: DIRECT\_COR\_SW
- > 2-clock command 0xB: DIRECT\_CHN\_SW

DIRECT\_XXX commands directly specify the ON-OFF states of the target switches. The target switches are specified using Chip-ID and Core-ID in the transmitted command, combined with the suffix of the command. The intended ON-OFF states for the target switches are transmitted through WData[7:0]. To turn on the switch, corresponding bit of WData should be '1', and to turn off, it should be '0'. For the detailed information about each DIRECT\_XXX commands, refer to *Commands Descriptions*.

### - Setting REJECT Flags

A REJECT flag is used to let the switch ignore further ON-OFF related commands. It is useful when we want some switches to stay OFF while we control many switches simultaneously with commands such as DIRECT\_BNK\_COR.

REJECT flags can be controlled by REJECT\_XXX commands. There are four commands to set REJECT flags.

- > 2-clock command 0x4: REJECT\_CHP\_COR
- > 2-clock command 0x7: REJECT\_CHP\_CHN
- > 2-clock command 0xC: REJECT\_COR\_SW
- > 2-clock command 0xD: REJECT\_CHN\_SW

REJECT flags are set to '1' according to the transmitted WData[7:0] of REJECT\_XXX commands. If a bit of WData is '0', corresponding REJECT flag(s) is set to '1'. Otherwise, corresponding REJECT flag(s) does not change. The target switches are specified by Chip-ID and Core-ID of the transmitted command. For the detailed information about REJECT\_XXX commands, refer to *Commands Descriptions*.

### **Protection from Excessive Current**

#### **- Current Limiting**

MCC16 supports Current Limiting to protect itself from excessive high current. If current more than the threshold flows through a switch, the switch is automatically raises turn-on resistance by internal protection circuit.

The current limit is continuous type and is automatically released when the load current decreases.

Current Limiting feature is enabled by CL\_EN bit (bit 1) of General Control Register (i.e. enabled if CL\_EN = 1). For more information about CL\_EN bit, refer to *WR\_GCON (0x1)* of *Commands Descriptions*.

#### **- Thermal Shutdown**

MCC16 supports thermal shutdown to protect itself from excessive high current. If the temperature of a switch goes above the threshold (+150°C, typ.), the switch is automatically DISCONNECTED by internal thermal shutdown circuit. The threshold is loaded from internal OTP memory programmed during manufacturing. Thermal Shutdown is the secondary protection scheme for the case that Current Limiting does not work for some reasons even though excessive high current flows. The switch turns on again after the device temperature drops by approximately 20°C (typ.).

Once the switch is disconnected by Thermal Shutdown, the switch does not work until the temperature goes below the threshold.

Thermal Shutdown feature is enabled by TS\_EN bit (bit 0) of General Control Register (i.e. enabled if TS\_EN = 1). For more information about TS\_EN bit, refer to *WR\_GCON* of *Commands Descriptions*.

## Commands Descriptions

### - Suffixes of the Commands

Most of MCC16's commands are to control the states of the switches. Basically, each command can control switches in Core unit. However, to reduce the number of commands for setting the states of the switches, several variations of commands are supported, and they can address target switches in different ways from basic command (i.e. in Core unit). To represent this easily, commands have suffixes which represent the range of the target switches. The suffixes are,

- > \*\_ALL
- > \*\_BNK\_COR / \*\_BNK\_CHN
- > \*\_CHP\_COR / \*\_CHP\_CHN
- > \*\_COR\_SW / \*\_CHN\_SW

\_ALL suffix is for 1-clock commands. It represents that the target switches for this command is ALL SWITCHES IN THE BANK.

\_BNK\_COR / \_BNK\_CHN suffixes are for 2-clock commands. They represent that the target switches for this command are ALL SWITCHES IN THE BANK. While WData for \_BNK\_COR commands are in Core unit, WData for \_BNK\_CHN commands are in Channel unit. Since WData is applied to all Cores / Channels in all MCC16s in the Bank, Chip-ID / Core-ID are ignored.

\_CHP\_COR / \_CHP\_CHN suffixes are for 2-clock commands. They represent that the target switches for this command are ALL SWITCHES IN THE SPECIFIED CHIP. While WData for \_CHP\_COR commands are in Core unit, WData for \_CHP\_CHN commands are in Channel unit. Since WData is applied to all Cores / Channels in the specified MCC16, Core-ID is ignored.

\_COR\_SW / \_CHN\_SW suffixes are for 2-clock commands. They represent that the target switches for this command are SWITCHES OF THE SPECIFIED CORE / CHANNEL IN THE SPECIFIED CHIP. While WData for \_COR\_SW commands are in Core unit, WData for \_CHN\_SW commands are in Channel unit. Since WData is applied to single Core / Channel in the specified MCC16, both Chip-ID / Core-ID are used.

### - 1-Clock Commands

Table 1 shows the list of the 1-clock commands.

**Table 1. 1-Clock Commands List.**

Addr	Command	Description
0x0	RSVD	Reserved
0x1	RSVD	Reserved
0x2	RESET_ALL	Turns-off all switches of all chips in the Bank (i.e. OFF state). REJECT flags are cleared.
0x3	CLEAR_ALL	Turns-off all switches of all chips in the Bank (i.e. OFF state). REJECT flags are NOT affected.
0x4	ENABLE_ALL	Turns-on all switches of all chips in the Bank (i.e. ON state). Switches with REJECT flags remain in OFF state.
0x5	INITIAL_ALL	Turns-on all switches of all chips in the Bank (i.e. ON state). REJECT flags are cleared. Switches with REJECT flags are also changed to ON state.
0x6 ~ 0xA	RSVD	Reserved
0xB	EN1_WCON	First sequence to enable writing to control register. Should be followed by EN2_WCON command to enable writing. Otherwise, both EN1_WCON and EN2_WCON commands are canceled.
0xC	EN2_WCON	Enables writing to control registers. Should be preceded by EN1_WCON. If not preceded by EN1_WCON, EN2_WCON is ignored.  Note) To enable writing to control registers, EN1_WCON -> EN2_WCON commands should be issued in order. Otherwise, both EN1_WCON and EN2_WCON commands are canceled.
0xD	DIS_WCON	Disables writing to control register.
0xE	RSVD	Reserved
0xF	RSVD	Reserved



**■ RESET\_ALL (0x2) / CLEAR\_ALL (0x3) / ENABLE\_ALL (0x4) / INITIAL\_ALL (0x5)**

RESET\_ALL / CLEAR\_ALL / ENABLE\_ALL / INITIAL\_ALL commands are mainly used for initialization of switches in the selected Bank. These commands are applied to all switches of all MCC16s in the Bank simultaneously.

RESET\_ALL / CLEAR\_ALL commands turn off (i.e. change to OFF state) all switches of all MCC16s in the Bank. The difference between these two commands is that while RESET\_ALL command also clears REJECT flags altogether, CLEAR\_ALL command does not affect REJECT flags.

INITIAL\_ALL / ENABLE\_ALL commands turn on (i.e. change to ON state) all switches of all MCC16s in the Bank. The difference between these two commands is that while INITIAL\_ALL command also clears REJECT flags of all switches, ENABLE\_ALL command does not affect REJECT flags.

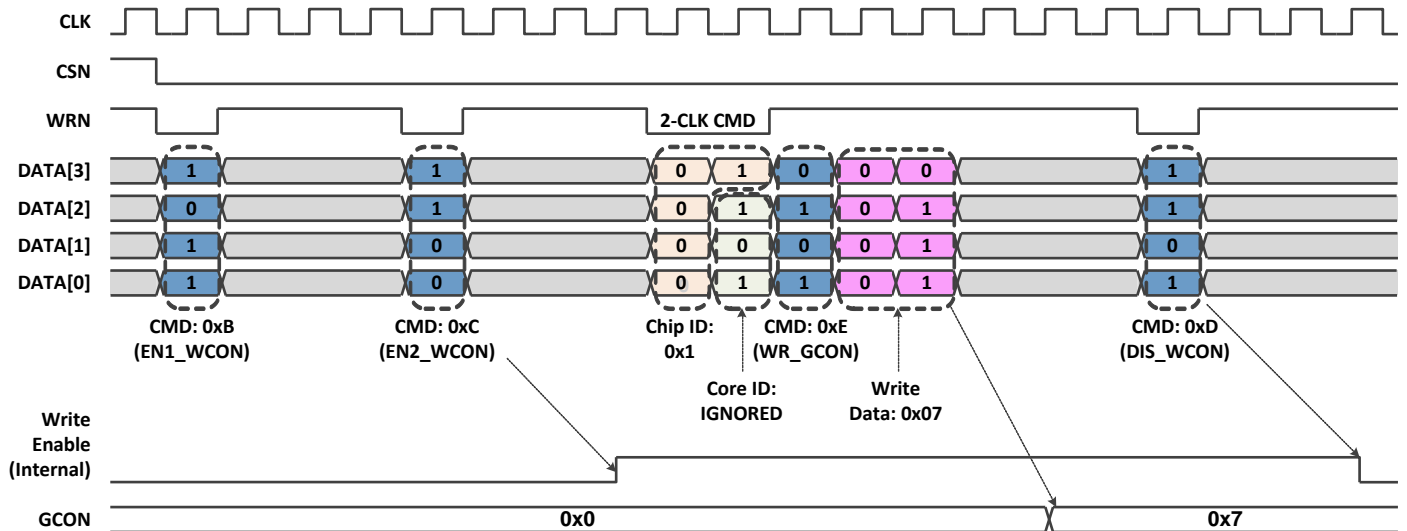
Table 2 shows the operation of the four initialization commands.

**Table 2. Operation of Initialization Commands.**

Command	ON-OFF States	REJECT Flags
RESET_ALL	OFF	CLEARED
CLEAR_ALL	OFF	NOT AFFECTED
INITIAL_ALL	ON	CLEARED
ENABLE_ALL	ON	NOT AFFECTED

■ **EN1\_WCON (0xB) / EN2\_WCON (0xC) / DIS\_WCON (0xD)**

By default, writing to control registers is disabled to prevent unintentional corruption of them. Therefore, it is needed to enable writing to control registers before updating control registers. By issuing EN1\_WCON and EN2\_WCON commands in order, writing to control register is internally enabled, and control registers can be updated by following 2-clock commands. Figure 12 shows an example for writing to GCON register.



### Figure 12. Example for Writing to Control Registers.

As shown in Figure 12, writing to control register is internally enabled by issuing EN1\_WCON and EN2\_WCON commands in order, and control registers are updated by WR\_GCON command, a 2-clock command.

After updating the control register, DIS\_WCON command is issued to disable writing to control register again.

- 2-Clock commands

Table 3 shows the list of 2-clock commands.

**Table 3. 2-Clock commands List.**

Addr	Command	Function
0x0	RSVD	Reserved
0x1	WR_GCON	Writes to General Control Register. Chip-ID specifies the target MCC16. Core-ID is ignored. WData is the written value to GCON register.
0x2	DIRECT_CHP_COR	Changes ON-OFF states of all switches in the specified MCC16. Updates all Cores' ON-OFF states of the target MCC16. Switches whose REJECT flags are '1' remain in OFF state.  Chip-ID specifies the target MCC16. Core-ID is ignored. WData represents the update value for ON-OFF states of all Cores in the target MCC16.  0: OFF, 1: ON
0x3	DIRECT_BNK_COR	Changes ON-OFF states of all switches of all MCC16s in the selected Bank. Updates all Cores' ON-OFF states of all MCC16s in the selected Bank. Switches whose REJECT flags are '1' remain in OFF state.  Chip-ID is ignored. Core-ID is ignored. WData represents the update value for ON-OFF states of all Cores in the target MCC16.  0: OFF, 1: ON
0x4	REJECT_CHP_COR	Changes the REJECT flags of the specified MCC16. ON-OFF states are updated according to REJECT flags' values.  Chip-ID specifies the target MCC16. Core-ID is ignored. WData[0] represents the update value for REJECT flags of Core0. WData[1] represents the update value for REJECT flags of Core1. WData[2] represents the update value for REJECT flags of Core2. WData[3] represents the update value for REJECT flags of Core3. WData[4] represents the update value for REJECT flags of Core4. WData[5] represents the update value for REJECT flags of Core5. WData[6] represents the update value for REJECT flags of Core6. WData[7] represents the update value for REJECT flags of Core7.  0: REJECT, 1: No Change.
0x5	DIRECT_CHP_CHN	Changes ON-OFF states of all switches in the specified MCC16. Updates all Channels' ON-OFF states of the target MCC16. Switches whose REJECT flags are '1' remain in OFF state.  Chip-ID specifies the target MCC16. Core-ID is ignored. WData represents the update value for ON-OFF states of all Channels in the target MCC16.  0: OFF, 1: ON

(Continued)

(Continued)

0x6	DIRECT_BNK_CHN	<p>Changes ON-OFF states of all switches of all MCC16s in the selected Bank. Updates all Channels' ON-OFF states of all MCC16s in the selected Bank. Switches whose REJECT flags are '1' remain in OFF state.</p> <p>Chip-ID is ignored. Core-ID is ignored. WData represents the update value for ON-OFF states of all Channels in the target MCC16.</p> <p>0: OFF, 1: ON</p>
0x7	REJECT_CHP_CHN	<p>Changes the REJECT flags of the specified MCC16. ON-OFF states are updated according to REJECT flags' values.</p> <p>Chip-ID specifies the target MCC16. Core-ID is ignored. WData[0] represents the update value for REJECT flags of Channel0/1. WData[1] is not used. WData[2] represents the update value for REJECT flags of Channel2/3. WData[3] is not used. WData[4] represents the update value for REJECT flags of Channel4/5. WData[5] is not used. WData[6] represents the update value for REJECT flags of Channel6/7. WData[7] is not used.</p> <p>0: REJECT, 1: No Change.</p>
0x8	WR_CLCON	<p>Writes to Current Limiting Control Register.</p> <p>Chip-ID specifies the target MCC16. Core-ID is ignored. WData is the written value to CLCON register.</p>
0x9	WR_TSDCON	<p>Writes to Thermal Shutdown Control Register.</p> <p>Chip-ID specifies the target MCC16. Core-ID is ignored. WData is the written value to TSDCON register.</p>
0xA	DIRECT_COR_SW	<p>Changes ON-OFF states of the specified Core in the specified MCC16. Switches whose REJECT flags are '1' remain in OFF state.</p> <p>Chip-ID specifies the target MCC16. Core-ID specifies the target Core. WData represents the update value for ON-OFF states of the target Core in the target MCC16.</p> <p>0: OFF, 1: ON</p>
0xB	DIRECT_CHN_SW	<p>Changes ON-OFF states of the specified Channel in the specified MCC16. Switches whose REJECT flags are '1' remain in OFF state.</p> <p>Chip-ID specifies the target MCC16. Core-ID specifies the target Channel. WData represents the update value for ON-OFF states of the target Channel in the target MCC16.</p> <p>0: OFF, 1: ON</p>

(Continued)

(Continued)

0xC	REJECT_COR_SW	<p>Changes the REJECT flags of the specified Core of the specified MCC16. ON-OFF states are updated according to REJECT flags' values.</p> <p>Chip-ID specifies the target MCC16. Core-ID specifies the target Core. WData represents the update value for REJECT flags of the specified Core.</p> <p>0: REJECT, 1: No Change.</p>
0xD	REJECT_CHN_SW	<p>Changes the REJECT flags of the specified Channel of the specified MCC16. ON-OFF states are updated according to REJECT flags' values.</p> <p>Chip-ID specifies the target MCC16. Core-ID specifies the target Channel. WData represents the update value for REJECT flags of the specified Channel.</p> <p>0: REJECT, 1: No Change.</p>
0xE ~ 0xF	RSVD	Reserved

■ **WR\_GCON (0x1)**

WR\_GCON command is used to update General Control Register. Table 4 shows the contents of General Control Register.

**Table 4. General Control Register.**

Bit Name	Bits	Descriptions	Reset	Remarks
RSVD	[7:2]	Reserved	-	-
CL_EN	1	Current Limiting Enable. 0: Disable, 1: Enable.	0	Initialized from OTP
TS_EN	0	Thermal Shutdown Enable. 0: Disable, 1: Enable.	0	Initialized from OTP

Though the default values for CL\_EN / TS\_EN registers are loaded from internal OTP memory on bootstrap, their values can be changed by WR\_GCON command.

Note that writing to General Control Register is prohibited by default. To write to General Control Register, EN1\_WCON / EN2\_WCON commands should be preceded. For more information about EN1\_WCON / EN2\_WCON commands, refer to *EN1\_WCON / EN2\_WCON / DIS\_WCON* of *Commands Descriptions*.

### ■ DIRECT\_CHP\_COR (0x2)

DIRECT\_CHP\_COR command changes all of the ON-OFF states in the target MCC16. The input WData value is written to all Cores of the specified MCC16. The target MCC16 is specified by Chip-ID. Figure 13 shows an example for DIRECT\_CHP\_COR command.

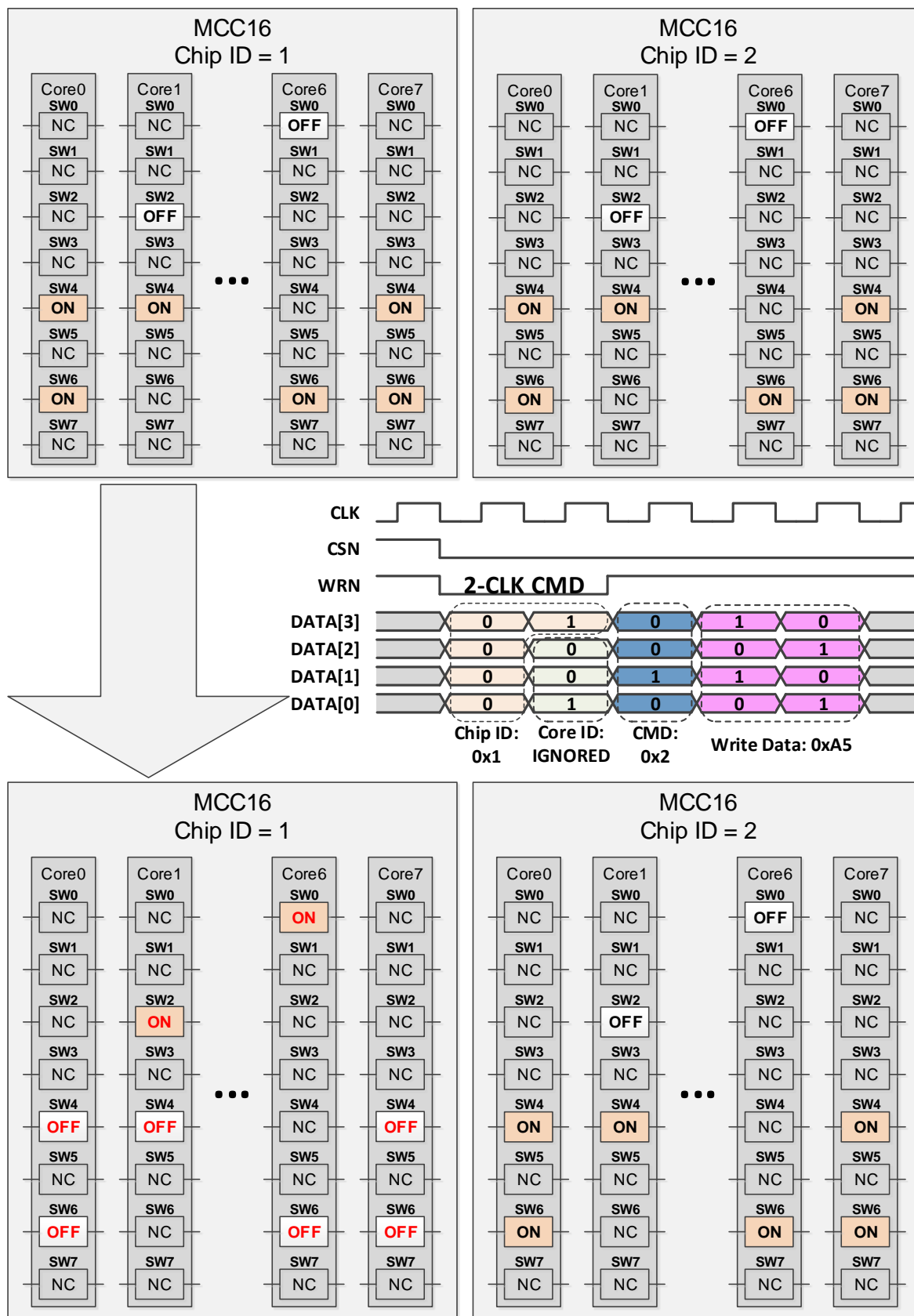


Figure 13. Example for DIRECT\_CHP\_COR Command.

In Figure 13, the input Chip-ID from the command is 0x1. All Cores of the MCC16 whose Chip-ID is 0x1, is updated with the value of WData[7:0] (= 0xA5). The Core-ID included in the command is ignored. Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.

For more information about the connection between control bits and switches, refer to *Figure 6. Internal Structure of MCC16*.



### ■ DIRECT\_BNK\_COR (0x3)

DIRECT\_BNK\_COR command changes all of the ON-OFF states in MCC16s in the selected Bank. The input WData value is written to all Cores of the MCC16s. Figure 14 shows an example for DIRECT\_BNK\_COR command.

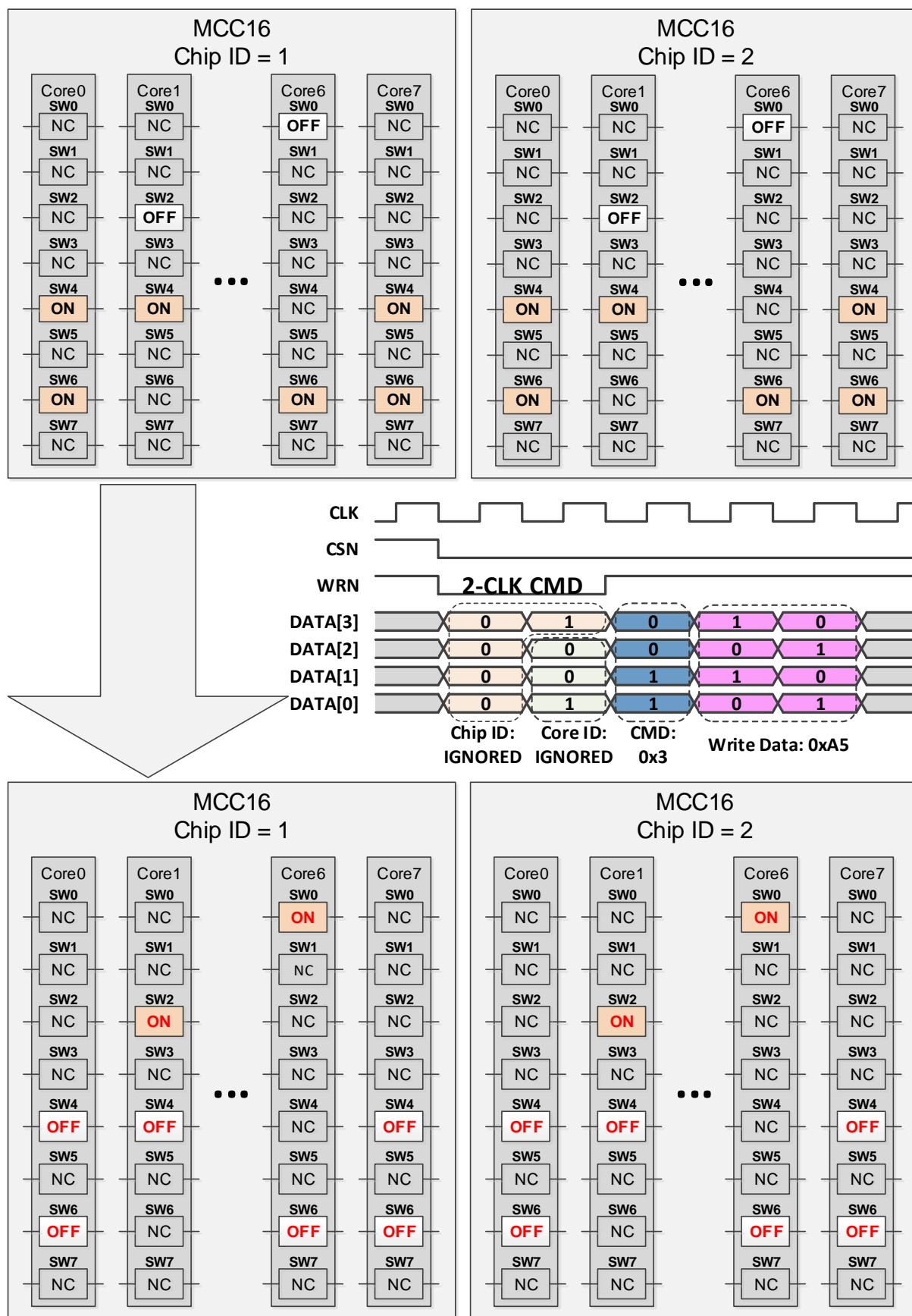


Figure 14. Example for DIRECT\_BNK\_COR Command.

In Figure 14, WData[7:0] is written to all Cores of all MCC16s in the Bank. Chip-ID and Core-ID are ignored. Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.

For more information about the connection between control bits and switches, refer to *Figure 6. Internal Structure of MCC16*.

### ■ REJECT\_CHP\_COR (0x4)

REJECT\_CHP\_COR command controls REJECT flags of the specified MCC16 in Core unit. According to each bit's value of WData[7:0], it sets REJECT flags of each Core's eight switches. Figure 15 shows an example for REJECT\_CHP\_COR command.

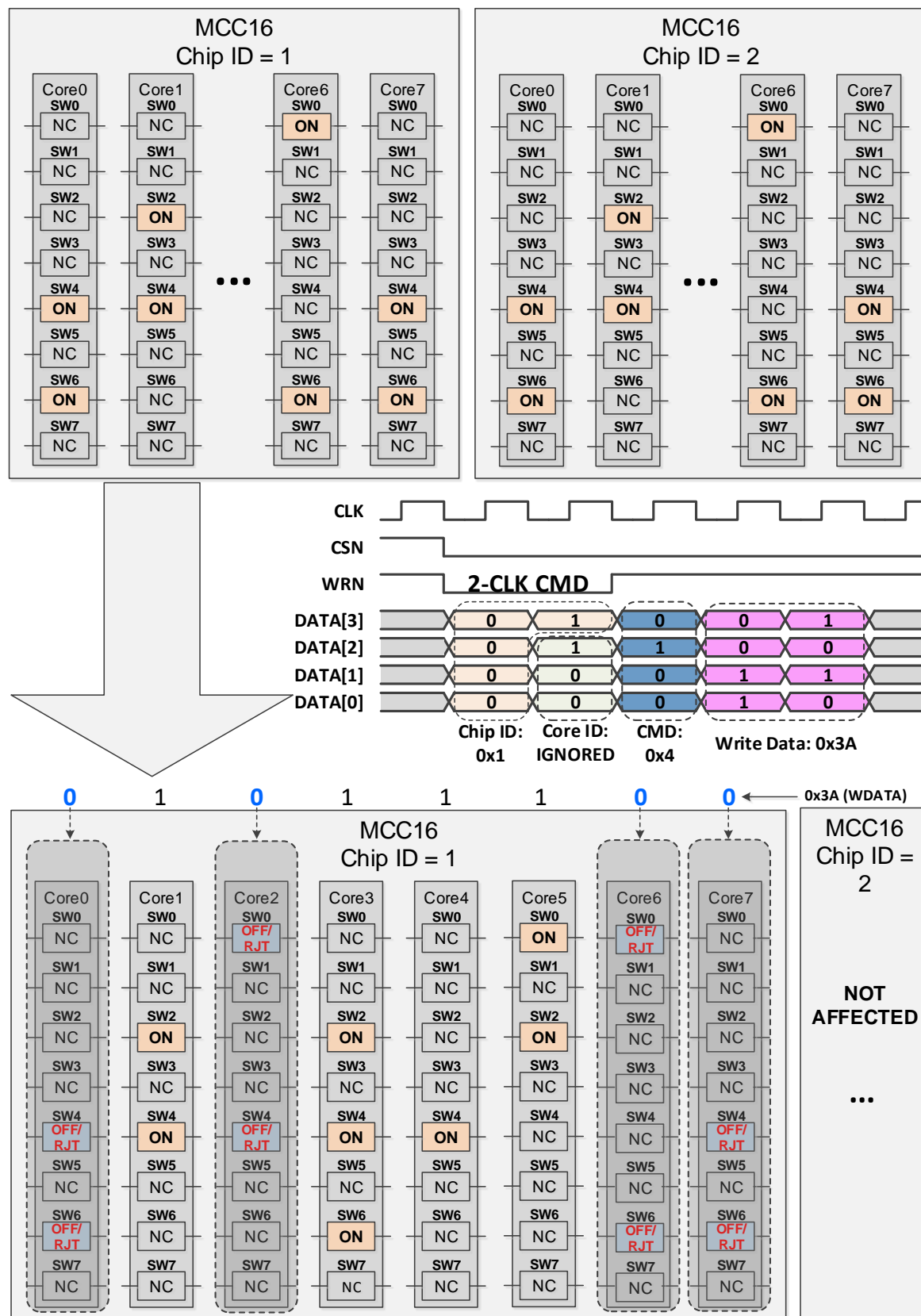


Figure 15. Example for REJECT\_CHP\_COR Command.

In Figure 15, target MCC16 is selected by the Chip-ID (= the one with Chip-ID is 0x1). Each bit of WData decides REJECT flags of each Core. From bit0 to bit7 of WData[7:0] corresponds to Core0 to Core7. Since bit0, bit2, bit6, and bit7 are '0's, REJECT flags of Core0, Core2, Core6, Core7 are set to '1'.

Note that WData bit's value '1' does not mean 'Clear REJECT flag', but 'No Change'. Once REJECT flags are set, they can be cleared only by 1-clock commands.

### ■ DIRECT\_CHP\_CHN (0x5)

DIRECT\_CHP\_CHN command changes all of the ON-OFF states in the target MCC16. The input WData value is written to all Channels of the specified MCC16. The target MCC16 is specified by Chip-ID. Figure 16 shows an example for DIRECT\_CHP\_CHN command.

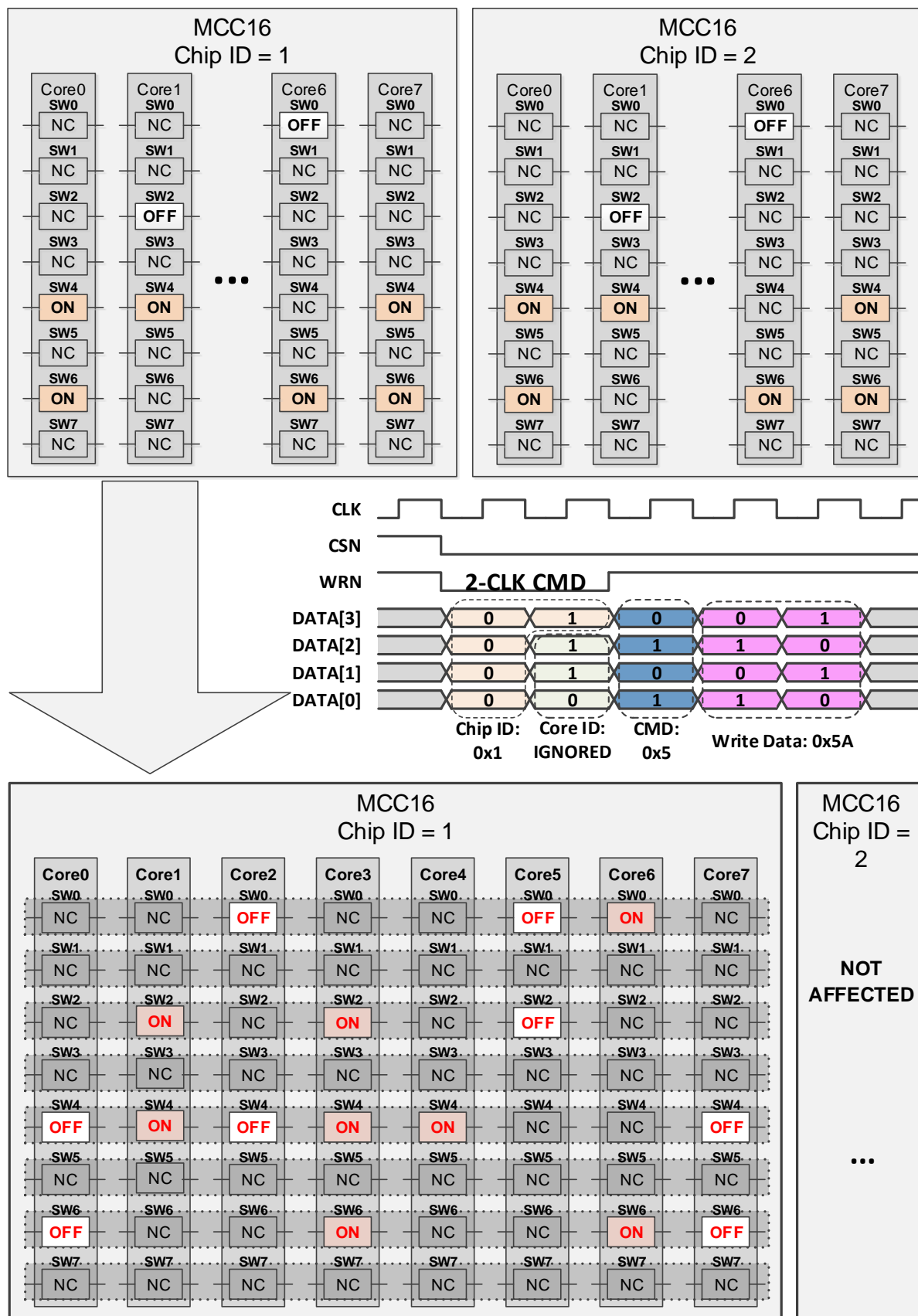


Figure 16. Example for DIRECT\_CHP\_CHN Command.

In Figure 16, the input Chip-ID from the command is 0x1. All Channels of the MCC16 whose Chip-ID is 0x1, is updated with the value of WData[7:0] (= 0x5A). Since all Channels are updated, the Core-ID included in the command is ignored. Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.

## ■ DIRECT\_BNK\_CHN (0x6)

DIRECT\_BNK\_CHN command changes all of the ON-OFF states in MCC16s in the selected Bank. The input WData value is written to all Channels of the MCC16s. Figure 17 shows an example for DIRECT\_BNK\_CHN command.

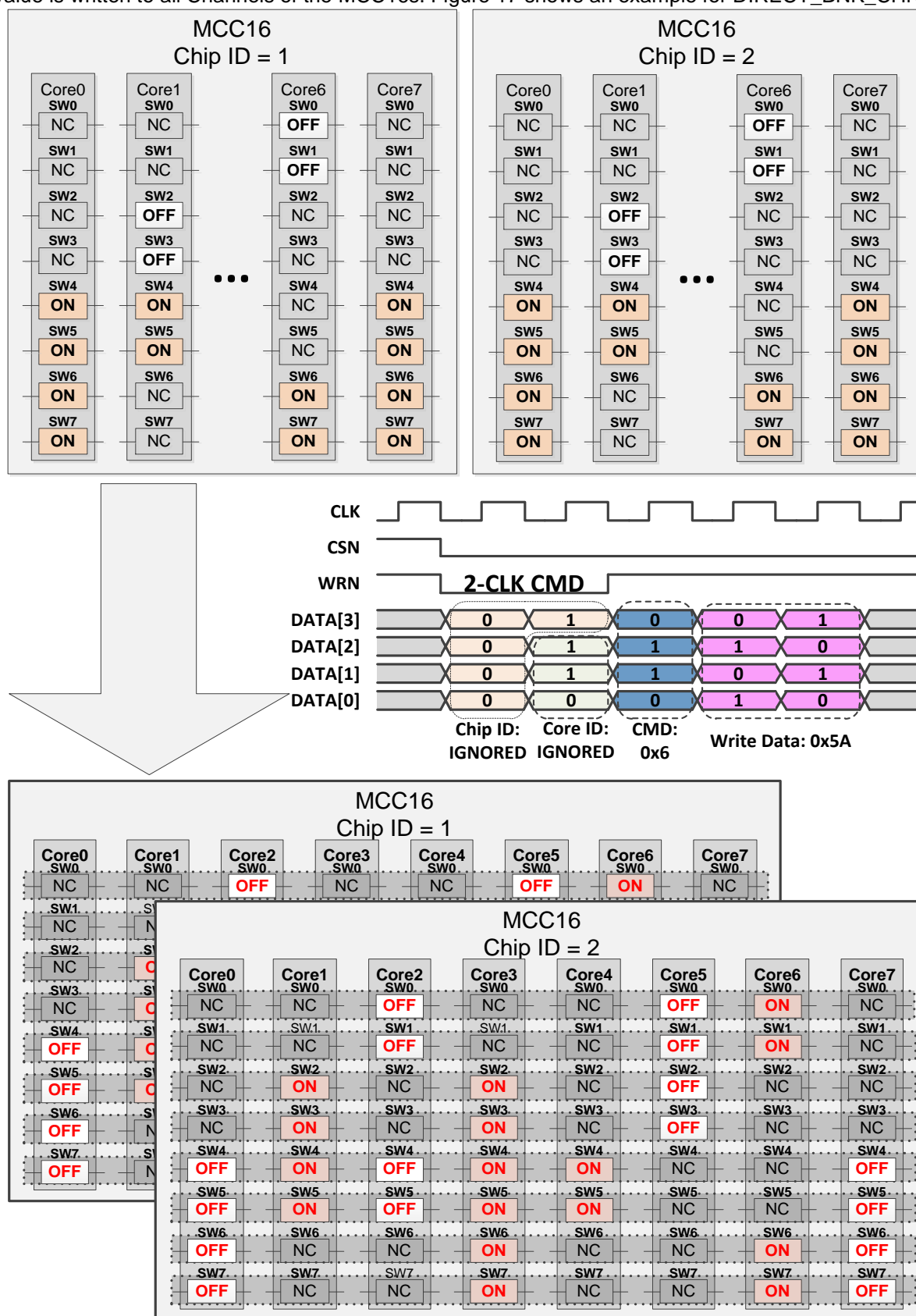


Figure 17. Example for DIRECT\_BNK\_CHN Command.

In Figure 17, WData[7:0] is written to all Channels of all MCC16s in the Bank. Since all Channels of all MCC16s are the target of DIRECT\_BNK\_CHN command, Chip-ID and Core-ID are ignored. Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.



## REJECT\_CHP\_CHN (0x7)

REJECT\_CHP\_CHN command controls REJECT flags of the specified MCC16 in Channel unit. According to each bit's value of WData[7:0], it sets REJECT flags of each Channel's eight switches. Figure 18 shows an example for REJECT\_CHP\_CHN command.

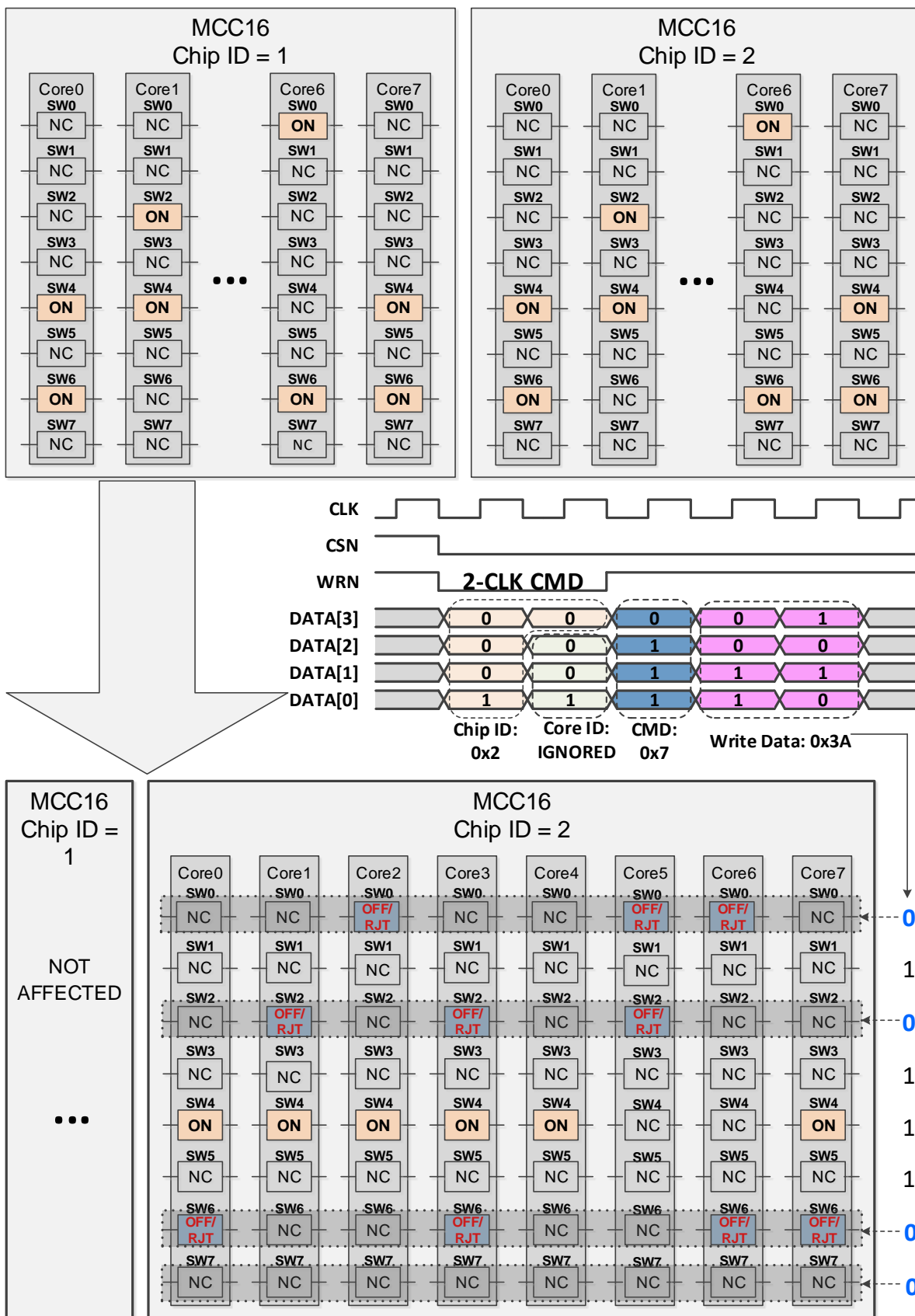


Figure 18. Example for REJECT\_CHP\_CHN Command.

In Figure 18, target MCC16 is selected by the Chip-ID (= the one with Chip-ID is 0x2). Each even numbered bit of WData decides REJECT flags. Bit0, bit2, bit4, bit6 of WData[7:0] correspond to Channel0, Channel2, Channel4, Channel6. Since bit0, bit2, and bit6 are '0's, REJECT flags of Channel0, Channel2, Channel4 are set to '1'.

Note that WData bit's value '1' does not mean 'Clear REJECT flag', but 'No Change'. Once REJECT flags are set, they can be cleared only by 1-clock commands.

For more information about the connection between control bits and switches, refer to *Figure 6. Internal Structure of MCC16*.

■ **WR\_CLCON (0x8)**

WR\_CLCON command is used to update Current Limiting Control Register. Table 5 shows the contents of Current Limiting Control Register.

**Table 5. Current Limiting Control Register.**

Bit Name	Bits	Descriptions	Reset	Remarks
TV_WEN	7	TRM_VAL write enable. TRM_VAL is updated only if the written value of TV_WEN is '1'.	-	-
TRM_VAL	[6:4]	Current limit trimming (8step). Specifies the trimming value for Current Limiting target limit current. Used for the trimming of target limit current.  Note) UPDATED ONLY IF TV_WEN == '1'.	000	Initialized from OTP

TRM\_VAL register is the trimming value for target limit current. However, actual temperature which triggers Current Limiting can be different from the target limiting current. Current Limiting circuit is trimmed with TRM\_VAL register to minimize this difference.

Though the default values for TRM\_VAL registers are loaded from internal OTP memory on bootstrap, their values can be changed by WR\_CLCON command. To make it possible to update TRM\_VAL registers respectively, TV\_WEN bits are supported. To update TRM\_VAL register, TV\_WEN should be HIGH.

### ■ WR\_TSDCON (0x9)

WR\_TSDCON command is used to update Thermal Shutdown Control Register. Table 6 shows the contents of Thermal Shutdown Control Register.

**Table 6. Thermal Shutdown Control Register.**

Bit Name	Bits	Descriptions	Reset	Remarks
TT_WEN	7	TSD_TRIM write enable. TSD_TRIM is updated only if the written value of TT_WEN is '1'.	-	-
TSD_TRIM	[6:4]	Thermal shutdown temp. trim (8step). Specifies the trimming value for Thermal Shutdown target temperature. Used for the trimming of target temperature of Thermal Shutdown.  Note) UPDATED ONLY IF TT_WEN == '1'.	000	Initialized from OTP
RSVD	[3:2]	Reserved	-	-
TS_WEN	1	TSS write enable. TSS is updated only if the written value of TS_WEN is '1'.	-	-
TSS	0	Thermal shutdown hysteresis select.  0: Selects Hysteresis A (about 20°C) 1: Selects Hysteresis B (about 10°C)  NOTE) UPDATED ONLY IF TS_WEN == '1'.	0	Initialized from OTP

TSD\_TRIM register is the trimming value for Thermal Shutdown target temperature. The target temperature of LSW9X00 Thermal Shutdown circuit is 150°C. However, actual temperature which triggers Thermal Shutdown can be different from the target temperature (i.e. 150°C). Thermal Shutdown circuit is trimmed with TSD\_TRIM register to minimize this difference.

TSS register selects Thermal Shutdown Hysteresis. If a switch is turned off by Thermal Shutdown, the switch can be turned on after the temperature goes below (150 – Thermal Shutdown Hysteresis) °C.

Though the default values for TSD\_TRIM / TSS registers are loaded from internal OTP memory on bootstrap, their values can be changed by WR\_TSDCON command. To make it possible to update TSD\_TRIM / TSS registers respectively, TT\_WEN / TS\_WEN bits are supported. To update TSD\_TRIM register, TT\_WEN should be HIGH. To update TSS register, TS\_WEN should be HIGH. The write-enable feature helps update either TSD\_TRIM or TSS register keeping the other register's value not changed.

Note that writing to Thermal Shutdown Control Register is prohibited by default. To write to Thermal Shutdown Control Register, EN1\_WCON / EN2\_WCON commands should be preceded. For more information about EN1\_WCON / EN2\_WCON commands, refer to *EN1\_WCON / EN2\_WCON / DIS\_WCON* of *Commands Descriptions*.

## ■ DIRECT\_COR\_SW (0xA)

DIRECT\_COR\_SW command changes the ON-OFF states of a Core in the target MCC16. The input WData value is written to the target Core of the specified MCC16. The target MCC16 is specified by Chip-ID, and the target Core by Core-ID. Figure 19 shows an example for DIRECT\_COR\_SW command.

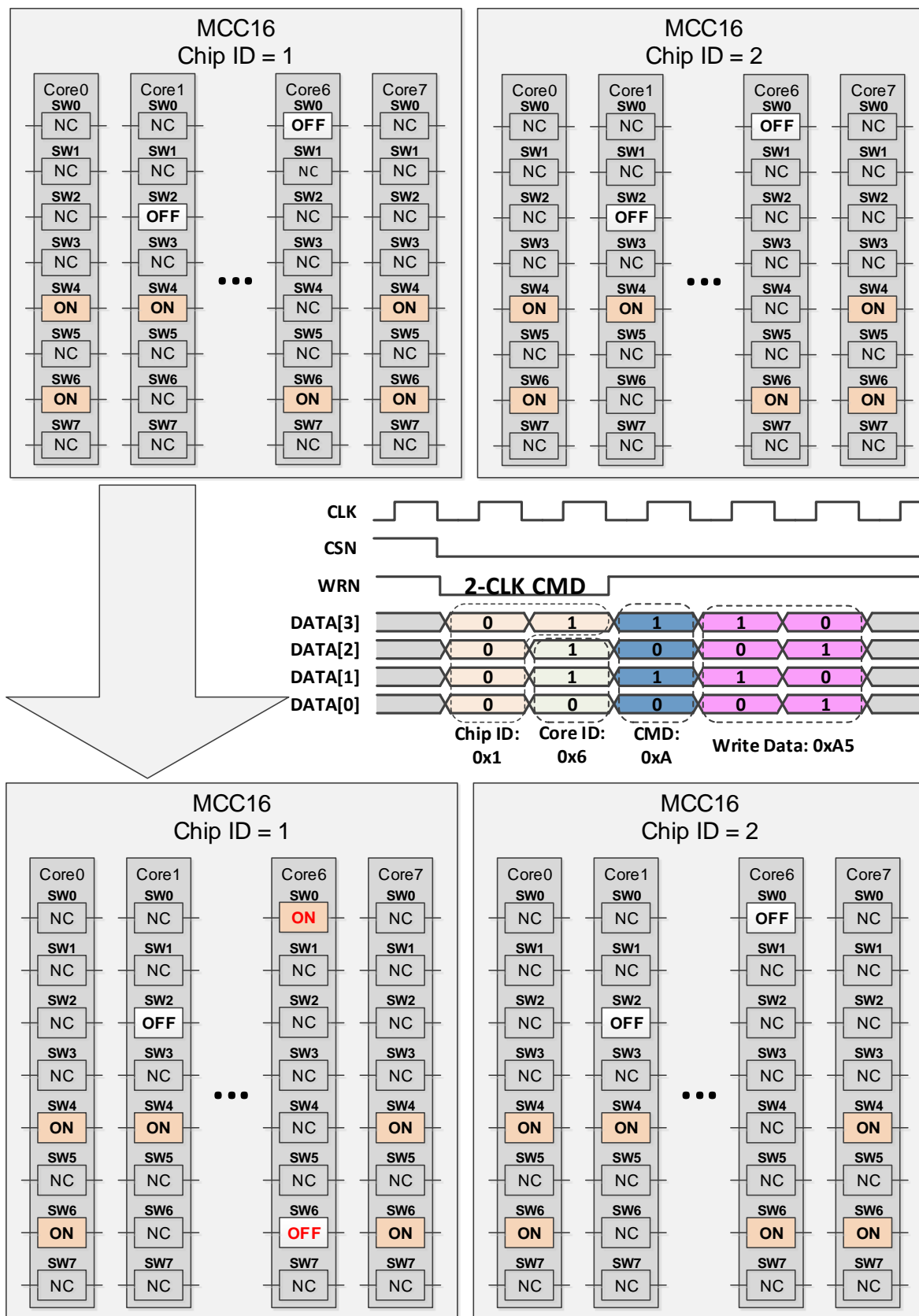


Figure 19. Example for DIRECT\_COR\_SW Command.

In Figure 19, the input Chip-ID from the command is 0x1, and Core-ID is 0x6. According to the input Chip-ID and Core-ID, Core6 of the MCC16 whose Chip-ID is 0x1, is updated with the value of WData[7:0] (= 0xA5). Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.

For more information about the connection between control bits and switches, refer to *Figure 6. Internal Structure of MCC16*.

### ■ DIRECT\_CHN\_SW (0xB)

DIRECT\_CHN\_SW command changes the ON-OFF states of a Channel in the target MCC16. The input WData value is written to the target Channel of the specified MCC16. The target MCC16 is specified by Chip-ID, and the target Channel by Core-ID. Figure 20 shows an example for DIRECT\_CHN\_SW command.

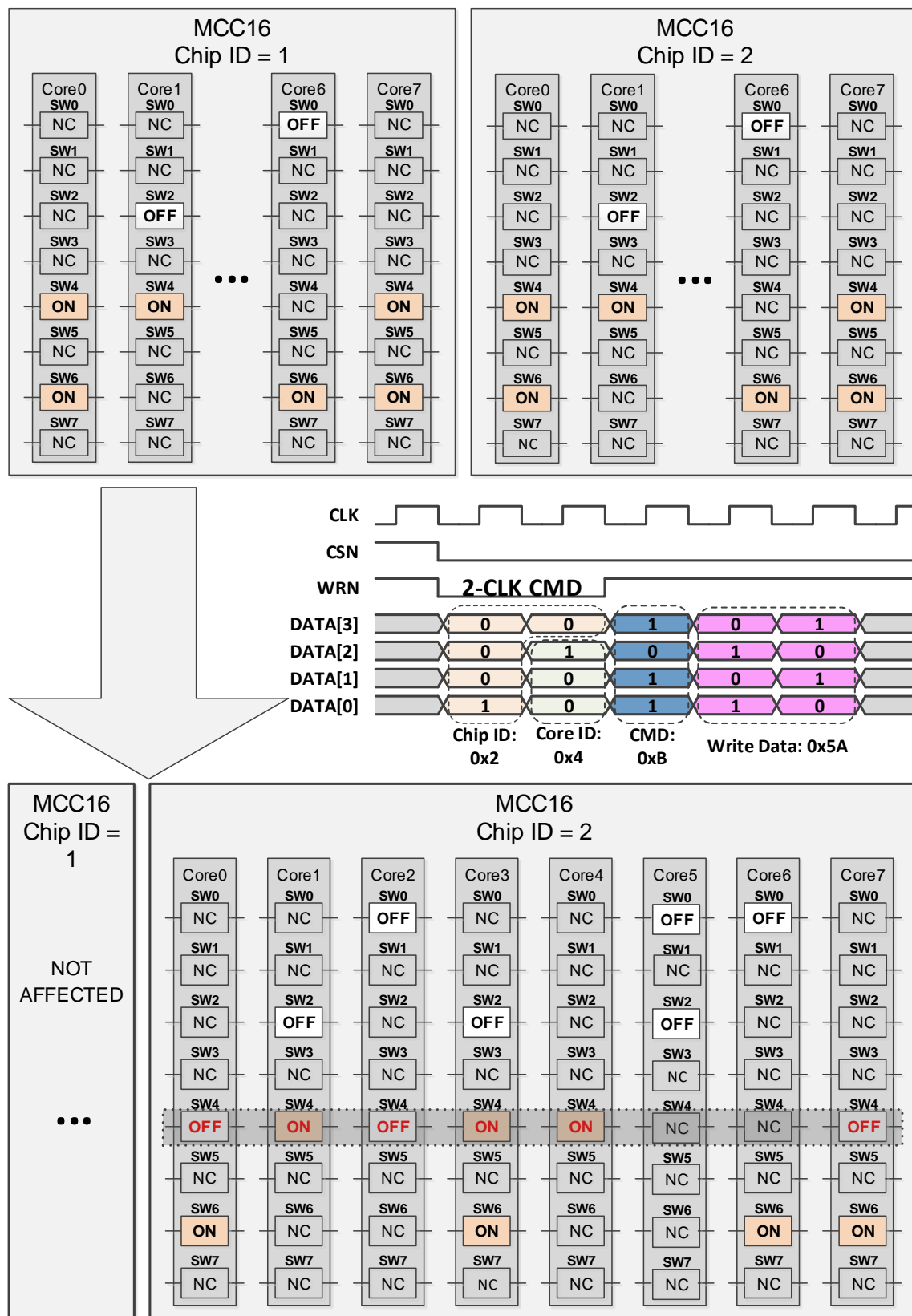


Figure 20. Example for DIRECT\_CHN\_SW Command.

In Figure 20, the input Chip-ID from the command is 0x2, and Core-ID is 0x4. According to the input Chip-ID and Core-ID, Channel4 of the MCC16 whose Chip-ID is 0x2, is updated with the value of WData[7:0] (= 0x5A). Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.

For more information about the connection between control bits and switches, refer to *Figure 6. Internal Structure of MCC16*.



### ■ REJECT\_COR\_SW (0xC)

REJECT\_COR\_SW command updates REJECT flags of the specified Core. It receives Chip-ID and Core-ID, and uses them to specify the target Channel in the target MCC16. According to each bit's value of WData[7:0], it sets REJECT flags of each switch of the selected Core. Figure 21 shows an example for REJECT\_COR\_SW command.

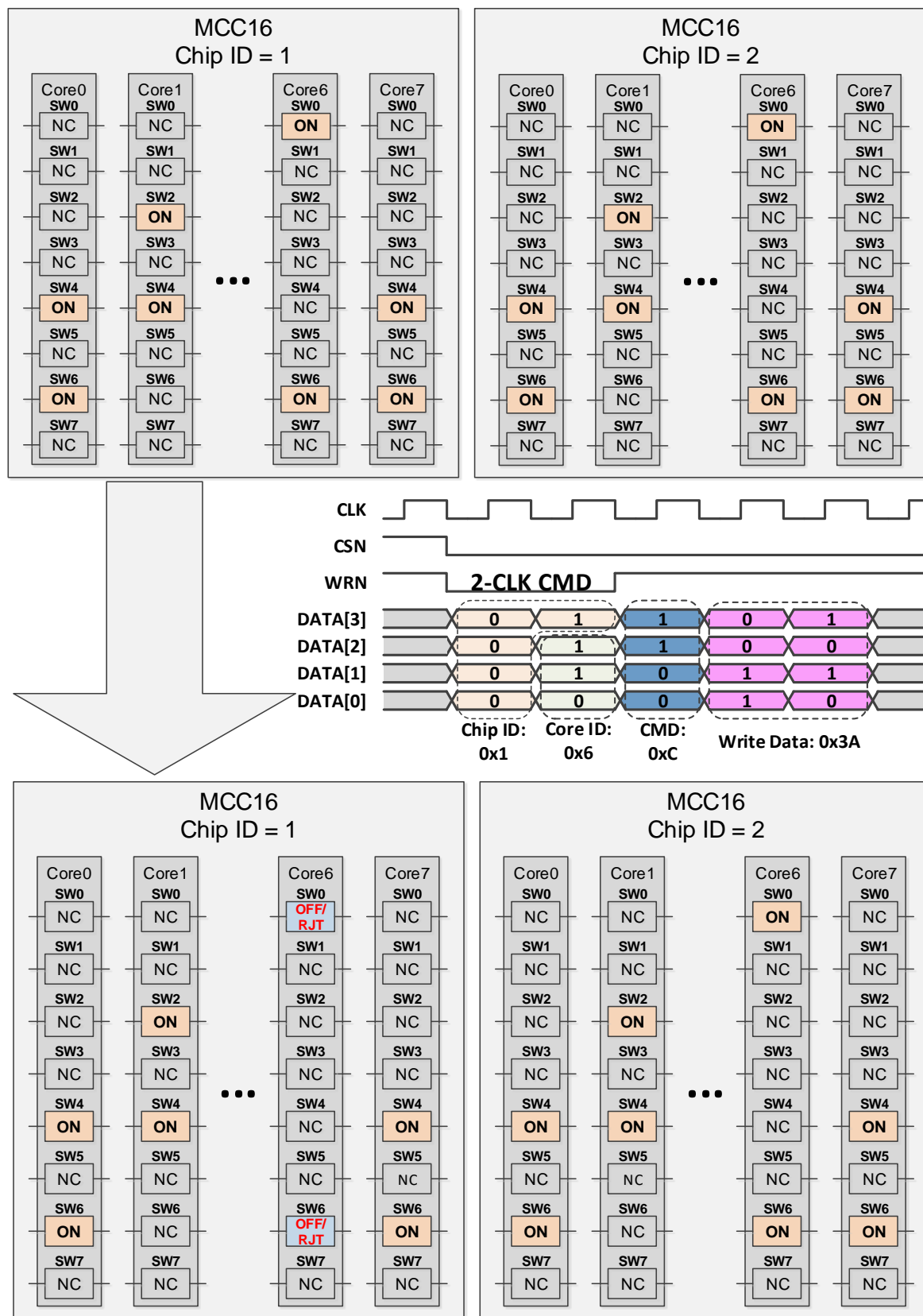


Figure 21. Example for REJECT\_COR\_SW Command.

In Figure 21, since Chip-ID is 0x1, the one with Chip-ID is 0x1 is selected as the target (i.e. the one with Chip-ID = 0x2 is not affected). Core-ID (= 0x6) specifies the target Core as Core6.

WData[7:0] contains the actual update value of REJECT flags. If a bit of WData is '0', it indicates that the corresponding switch's REJECT flag should be set to '1'. In Figure 21, WData is 0x3A, and bit7, bit6, bit2, bit0 of WData are ZERO. Since even numbered bits control the state of each corresponding switch, it results in that REJECT flags of switch6, switch2 and switch0 are set to '1'. ON-OFF states of those switches are also set to OFF.

Note that WData bit's value '1' does not mean 'Clear REJECT flag', but 'No Change'. Once REJECT flags are set, they can be cleared only by 1-clock commands.

For more information about the connection between control bits and switches, refer to *Figure 6. Internal Structure of MCC16*.

### ■ REJECT\_CHN\_SW (0xD)

REJECT\_CHN\_SW command updates REJECT flags of the specified Channel. It receives Chip-ID and Core-ID, and uses them to specify the target Channel in the target MCC16. The Core-ID is used as the Channel-ID. According to each bit's value of WData[7:0], it sets REJECT flags of each switch of the selected Channel. Figure 22 shows an example for REJECT\_CHN\_SW command.

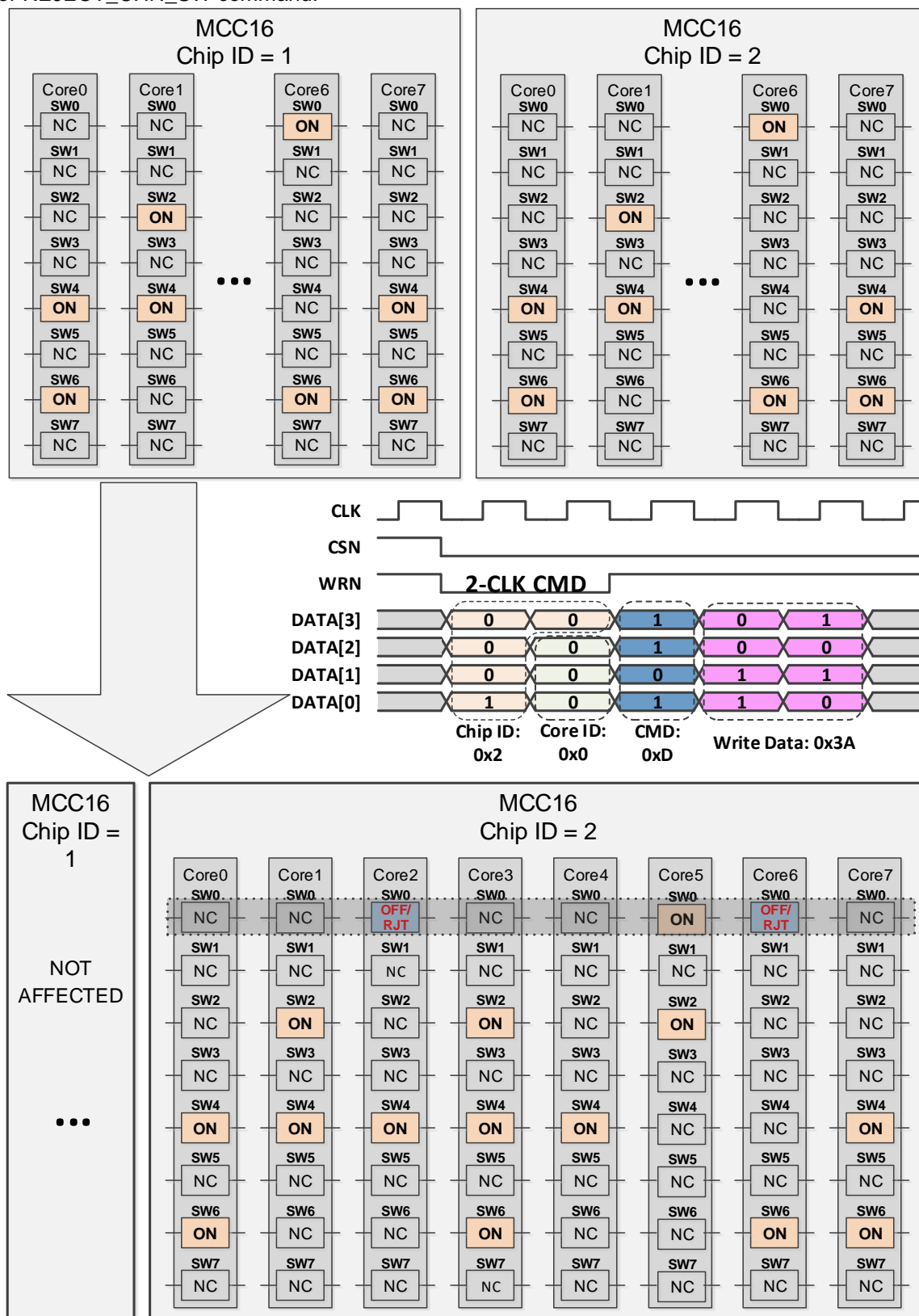


Figure 22. Example for REJECT\_CHN\_SW Command.

In Figure 22, since Chip-ID is 0x2, the one with Chip-ID is 0x2 is selected as the target (i.e. the one with Chip-ID = 0x1 is not affected). Core-ID (= 0x0) specifies the target Channel as Channel0, which includes all switch0 s from Core0 to Core7.

WData[7:0] contains the actual update value of REJECT flags. If a bit of WData is '0', it indicates that the corresponding switch's REJECT flag should be set to '1'. In Figure 22, since WData is 0x3A, bit7, bit6, bit2, bit0 of WData are ZERO. This results in that REJECT flags of switch0 s in Core7, Core6, Core2, Core0 are set to '1'. ON-OFF states of those switches are also set to OFF.

Note that WData bit's value '1' does not mean 'Clear REJECT flag', but 'No Change'. Once REJECT flags are set, they can be cleared only by 1-clock commands.

For more information about the connection between control bits and switches, refer to *Figure 6. Internal Structure of MCC16*.

## PACKAGE INFORMATION

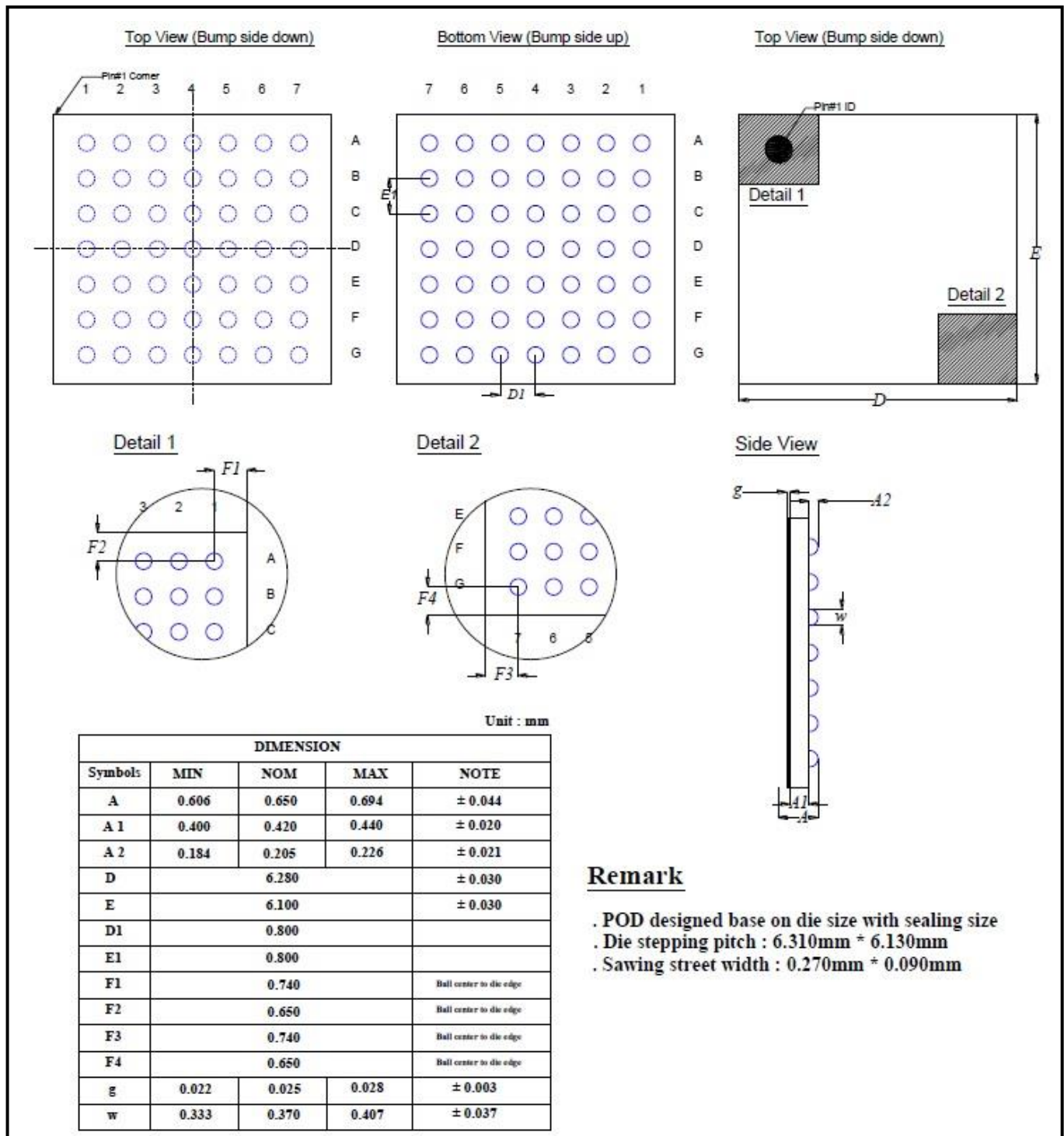


Figure 23. Package Information.

## APPLICATION EXAMPLE

## IC and Package Information

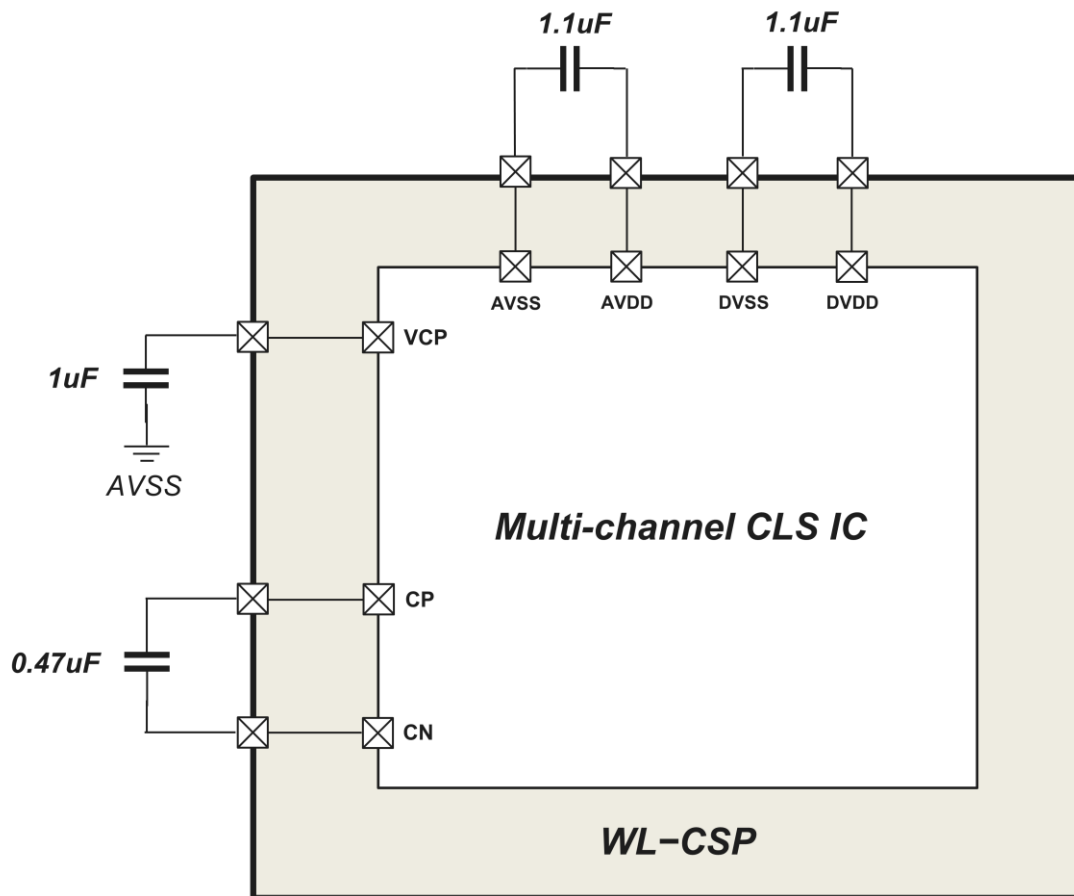
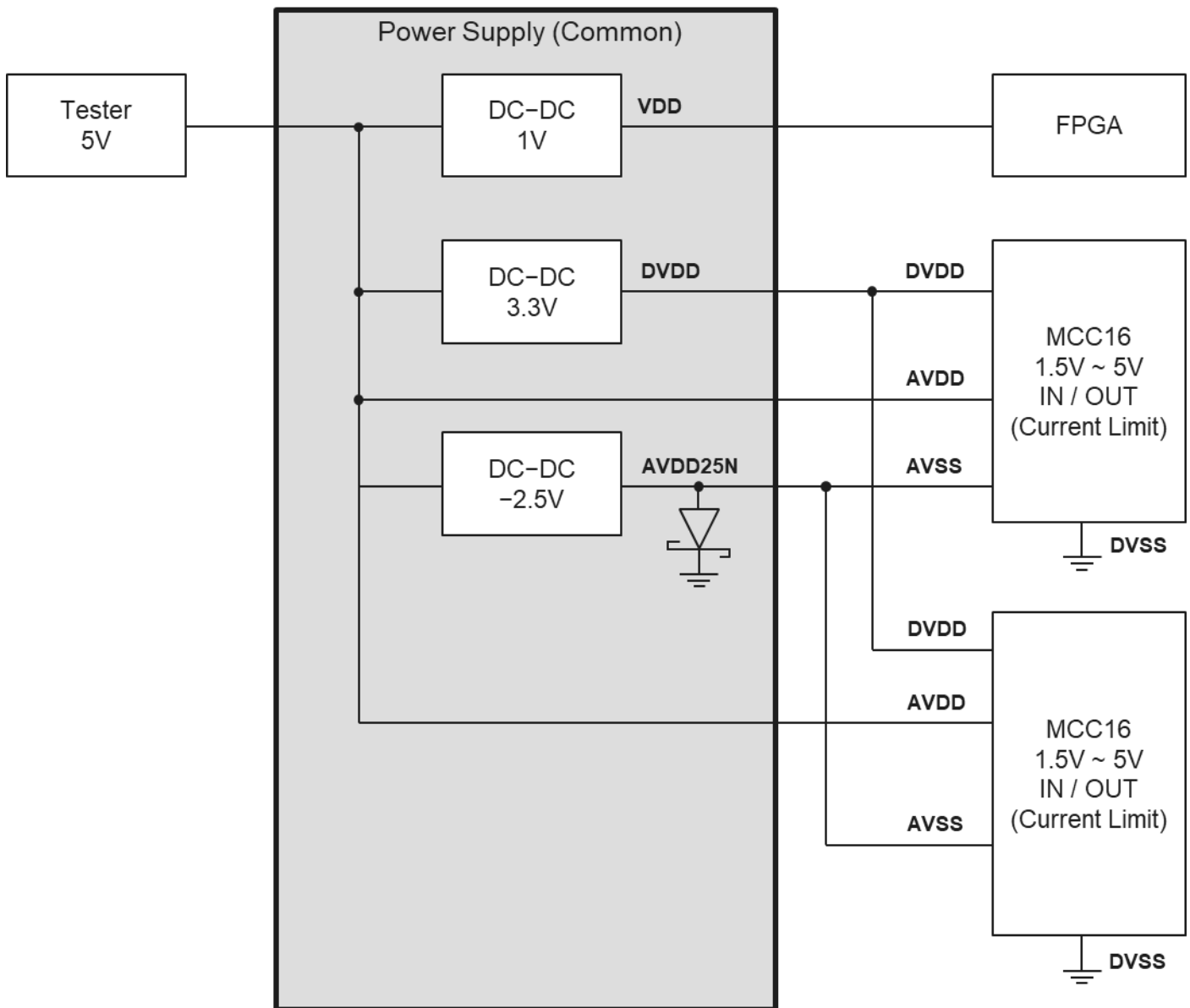


Figure 24. IC and package information.

1. MCC16 includes all the pull-up and pull-down resistors are included in the I/O block of the IC.
2.  $1\mu F$  and  $0.1\mu F$  decoupling capacitors should be connected to between AVDD and AVSS, and the same capacitors to between DVDD and DVSS
3. VCP pin should be connected to AVSS through  $1\mu F$  capacitor.
4.  $0.47\mu F$  capacitor should be connected to between CP and CN

## Power Supply Configuration

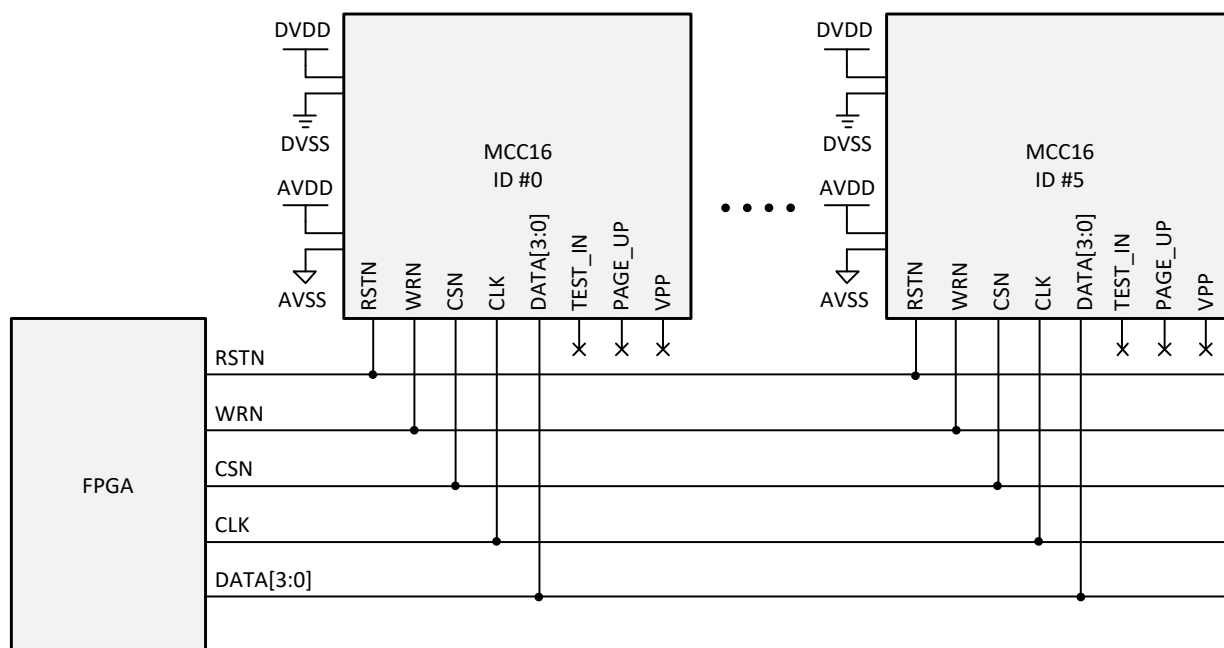


(a) In case of using 5V power supply directly for AVDD

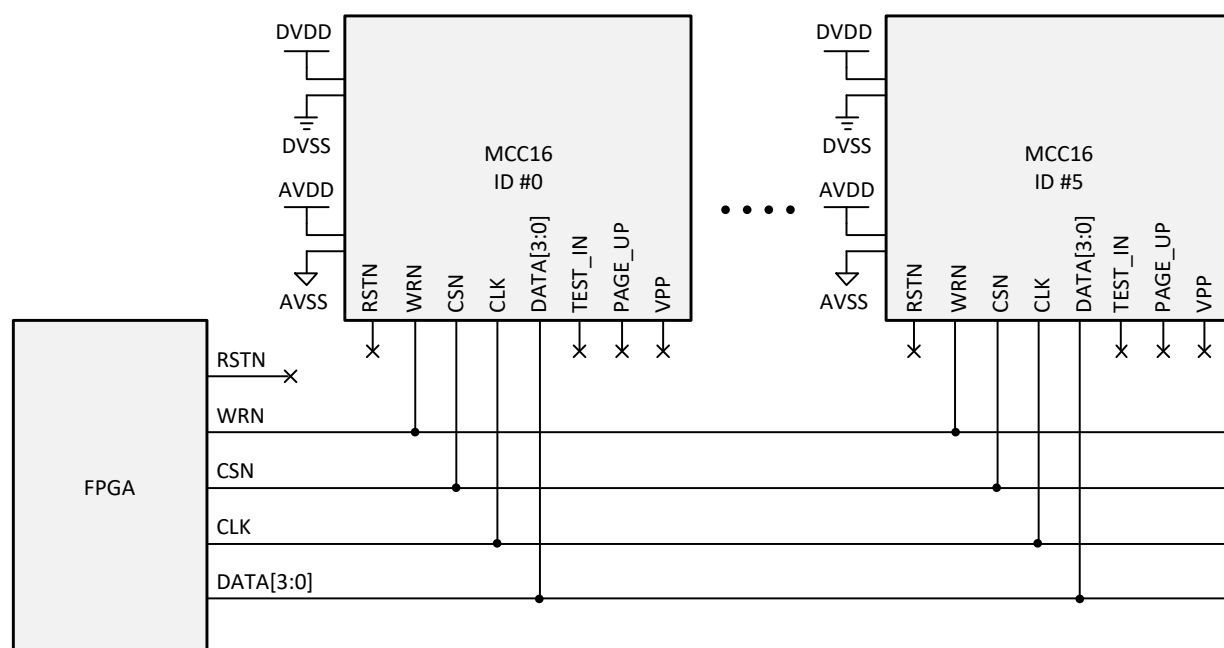
**Figure 25. Application Example.**

MCC16 IC support bipolar configuration that negative voltage less than ground level can be applied to AVSS. With maintaining maximum operating voltage between AVDD and AVSS as 5.5V, AVSS can be maximally lowered to -2.5V. When using the negative voltage to AVSS, to prevent latch-up phenomenon of MCC16 IC, a Schottky barrier diode should be attached between AVSS (anode) and DVSS (cathode). Without this protection diode, permanent malfunction of MCC16 IC may occur occasionally.

## Control I/O Pin Connection



(a) In case of using the external RSTN signal from FPGA



(b) In case of not using the external RSTN signal from FPGA but using the internal reset

**Figure 26. Recommended I/O connection.**

MCC16 ICs can share their control pins such as CSN, RSTN, WRN, CLK, and DATA[3:0]. Figure 26 (a) shows the I/O pin configuration in case of using the external RSTN signal from FPGA. And Figure 26 (b) shows the I/O pin configuration in case of not using the external RSTN signal from FPGA but using the internal reset signal generated by internal power-on-reset (POR) circuit. Any pull-up/down resistor or bypass capacitor is not required to be attached.



**REVISION HISTORY**

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Revision	Date	Description
0.0	2019-09	Initial draft
0.1	2020-01	Modified description for ELECTRICAL CHARACTERISTICS
0.2	2020-06	Modified description for ELECTRICAL CHARACTERISTICS
0.3	2021-01	Modified description for ELECTRICAL CHARACTERISTICS

**DOCUMENT INFORMATION**

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Product code: MCC16  
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The world is driven by analog

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