PS1120 Datasheet

60-in/120-out CMOS Multi Channels Switch IC

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The world is driven by analog

GENERAL DESCRIPTION

The PS1120 is a monolithic CMOS device containing 120 independently selectable switches. These switches are fabricated with an advanced submicron CMOS process that provides low power dissipation, low on resistance, low leakage currents, and small size. The PS1120 is designed to operate in 1.8V for digital circuits and 5V for analog switches. Each switch can operate with a wide input and output voltage range. The off-leakage current is only 10nA at room temperature of 25°C.

All digital input pins adopt the Schmitt trigger I/O, which has 0.5-V to 1.3-V input noise margin to ensure TTL/CMOS-logic compatibility when using a 1.8-V power supply. It is embedded DVDD to DVSS and AVDD to AVSS 0.1uF bypass capacitor into the PKG.

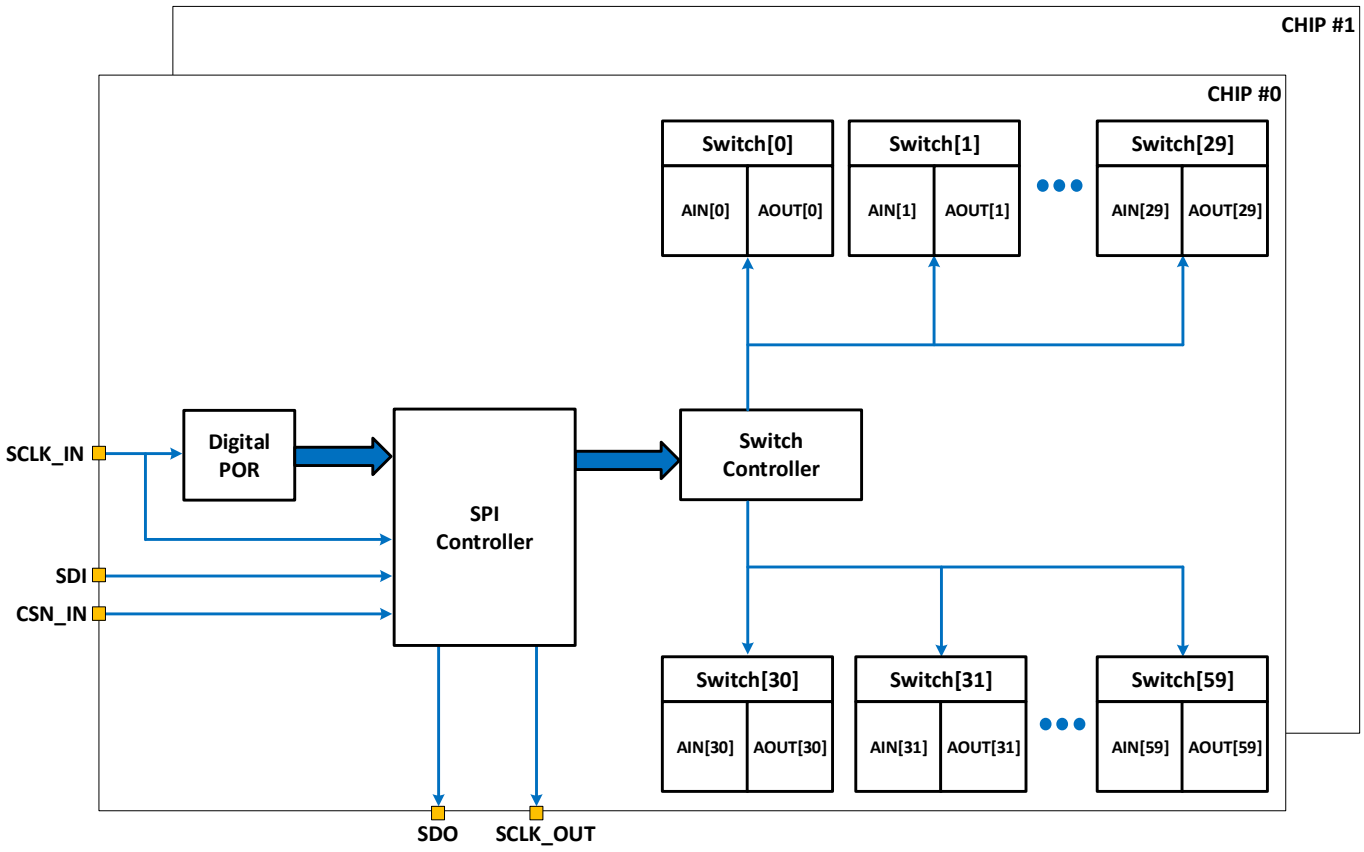
FEATURE

Multi channels (120ea) analog switch IC
1.8V logic-compatible input (V_{IH}=1.3V, V_{IL}=0.5V)
Dual supply operation: 1.8V for digital, 5V for analog.
Analog signal frequency: DC-to-1MHz
Low on-resistance: 2Ω (@typ)
Wide range analog input from -1.5V to 5V or 0V to 5.5V
Switching control using serial peripheral interface(SPI) command
192-pin FC-FBGA package
Embedded bypass capacitors (0.1uF)

APPLICATIONS

Data-acquisition systems
Mechanical reed-relay replacement
Communication systems

FUNCTIONAL BLOCK DIAGRAM



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PIN MAPPING TABLE (TOP View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	AVDD	AOUT3	AOUT2	AIN2	AOUT1	AOUT58	DVSS	SCLK_IN	SCLK_OUT	DVDD	AOUT63	AOUT62	AOUT61	AOUT118	AOUT119	AVDD	A
B	AOUT7	AOUT5	AOUT4	AIN4	AIN1	AOUT56	AOUT59	SDI	SDO	AOUT64	AIN64	AIN62	AIN61	AIN116	AOUT116	AOUT117	B
C	AOUT8	AOUT6	AIN6	AOUT0	AIN0	AIN56	AOUT57	DVSS	CSN_IN	AOUT65	AIN66	AOUT60	AIN60	AIN114	AOUT114	AOUT115	C
D	AOUT9	AIN11	AOUT10	AIN10	AIN52	AOUT52	AIN54	AOUT54	AOUT69	AOUT67	AOUT68	AOUT66	AIN110	AIN112	AOUT112	AOUT113	D
E	AOUT11	AOUT13	AOUT12	AIN12	AIN50	AOUT50	AOUT53	AOUT55	AOUT71	AIN71	AOUT70	AIN70	AOUT108	AOUT110	AIN111	AOUT111	E
F	AOUT17	AOUT15	AOUT14	AIN14	AOUT46	AOUT48	AIN51	AOUT51	AOUT73	AOUT72	AIN72	AIN74	AIN106	AOUT106	AOUT107	AOUT109	F
G	AOUT19	AOUT18	AOUT16	AIN16	AOUT44	AIN46	AOUT47	AOUT49	AOUT77	AOUT76	AOUT75	AOUT74	AIN102	AIN104	AOUT104	AOUT105	G
H	AOUT21	AIN21	AOUT20	AIN20	AIN44	AOUT45	AIN42	AOUT43	AOUT79	AOUT78	AIN76	AIN80	AIN92	AOUT102	AOUT103	AOUT101	H
J	AOUT23	AOUT22	AIN22	AIN30	AIN40	AOUT40	AIN41	AOUT42	AOUT81	AIN81	AOUT80	AIN90	AOUT92	AIN100	AOUT100	AIN101	J
K	AOUT25	AOUT24	AIN24	AOUT30	AIN32	AIN36	AOUT38	AOUT41	AOUT83	AOUT82	AIN82	AOUT90	AOUT93	AIN96	AOUT98	AOUT99	K
L	AOUT27	AIN26	AOUT28	AIN31	AOUT32	AIN34	AOUT36	AOUT39	AOUT85	AOUT84	AIN84	AOUT88	AIN91	AIN94	AOUT96	AOUT97	L
M	AVSS	AOUT26	AOUT29	AOUT31	AOUT33	AOUT34	AOUT35	AOUT37	AOUT87	AOUT86	AIN86	AOUT89	AOUT91	AOUT94	AOUT95	AVSS	M
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

PIN DESCRIPTION

D: Digital, A: Analog

IO: Input and Output(Bi-direction), O: Output, I: Input, P: Power, G: Ground

Power

Name	I/O	Description
AVDD	P	Analog Power
DVDD	P	Digital Power
AVSS	G	Analog Ground
DVSS	G	Digital Ground

SPI Interface

Name	I/O	Description
SCLK_IN	I	SPI Clock In
SCLK_OUT	O	SPI Clock Out
CSN_IN	I	SPI Chip Selection In.
SDI	I	SPI Data In
SDO	O	SPI Data Out

Analog

Name	I/O	Description
IN[59:0]	I	Analog Switch Input
OUT[119:0]	O	Analog Switch Output

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND, Unless Otherwise Noted.)

AVSS to AVDD (for Analog Switch).....-0.3V to +7V
DVDD (for Digital Control).....-0.3V to +2.0V
Voltage at any digital pin .....-0.3V to +2.0V
Voltage at any analog pin ……- 0.3V to +6V
Continuous current into any terminal 50mA
Peak current into analog switch I/O…….....100mA
(current pulse with 1ms and 10% duty cycle)

Operating temperature range .....-40°C to +125°C
Storage temperature range .....-55°C to +125°C
Junction temperature.....+150°C
ESD protection on all pins (HBM, MM)……..…≥ TBD

Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at those or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (AVDD = 4.0V, AVSS = -1.5V, TA = +25°C)

AVDD=4.0V, AVSS=-1.5V, DVDD=1.8V, DVSS=0V, and TA = +25°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
POWER SUPPLIES							
Analog Supply Voltage		AVDD		3.9	4.0	4.1	V
Digital Supply Voltage		DVDD		1.62	1.8	1.98	V
Analog Ground Voltage		AVSS		-1.65	-1.5	-1.35	V
Digital Ground Voltage		DVSS			0		V
ANALOG SWITCH							
Input Signal Range		V_{AIN}		-1.3		3.0	V
Channel On Current		I_{CH_ON}				50	mA
Switch On-resistance		R_{ON}	V_{AIN}=-1.3V~3.0V, I_{CH_ON}=10mA		0.6	2.3	Ω
Active Discharge Resistance		R_{DIS}	Discharge to GND		10.5		kΩ
Switch Leakage Current	Channel Off Leakage Current Input	I_{CH_OFFI}	V_{AIN}=-1.3V, Input measure, *fig.1, Each switch	-10	-5.0		nA
	Channel Off Leakage Current Output	I_{CH_OFFO}	V_{AIN}=-1.3V, Output measure, *fig.1, Each switch	-10	-1.0		nA
	Channel On Leakage Current	I_{CH_ON}	V_{AIN}=-1.3V, Input and output values are same, Each switch	-10	-2.0		nA
	Channel Off Leakage Current Input	I_{CH_OFFI}	V_{AIN}=3.0V, Input measure, *fig.1, Each switch		1.0	10	nA
	Channel Off Leakage Current Output	I_{CH_OFFO}	V_{AIN}=3.0V, Output measure, *fig.1, Each switch		1.0	10	nA

	Channel On Leakage Current	I_{CH_ON}	V_{AIN}=3.0V, Input and output values are same, Each switch		1.0	10	nA
DIGITAL I/O							
Logic Input Voltage	Input High	V_{IH}		0.7* DVDD			V
	Input Low	V_{IL}				0.3* DVDD	V
Logic Input Current	Input High	I_{IH}		-1		1	uA
	Input Low	I_{IL}		-1		1	uA
SWITCH DYNAMIC CHARACTERISTICS							
Switching Time	Turn ON Time	t_{ON}	Clock base Load C/R = 20pF / 1Kohm		30		ns
	Turn OFF Time	t_{OFF}	Load C/R = 20pF / 1Kohm		150		ns
Capacitance	Input Off-Capacitance	C_{AIN_OFF}	Each switch		55		pF
	Output Off-Capacitance	C_{AOUT_OFF}	Each switch		55		pF
	Output On-Capacitance	C_{AOUT_ON}	Each switch		110		pF
Switching Frequency		f_{SW}	f_{CLK}=10MHz			156	KHz
POWER CONSUMPTION							
Analog Operating Current (AVDD)	Static	I_{AVDD_ST}			1.0	3.0	uA
	Dynamic	I_{AVDD_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.1	0.15	mA
			f_{CLK}=10MHz, f_{SW}=100KHz,		1.0	1.5	
Analog Operating Current (AVSS)	Static	I_{AVSS_ST}			1.0	3.0	uA
	Dynamic	I_{AVSS_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.1	0.15	mA
			f_{CLK}=10MHz, f_{SW}=100KHz,		1.0	1.5	
Digital Operating Current (DVDD)	Static	I_{DVDD_ST}			0.15		mA
	Dynamic	I_{DVDD_DYN}	f_{CLK}=10MHz, f_{SW}=100KHz, Cp* = 50pF Single Command : ALL_SW_ON/OFF Cp* : Parasitic Capacitance		3.5	5.0	mA

ELECTRICAL CHARACTERISTICS (AVDD = 4.0V, AVSS = -1.5V, TA = +125°C)

AVDD=4.0V, AVSS=-1.5V, DVDD=1.8V, DVSS=0V, and TA = +125°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
POWER SUPPLIES							
Analog Supply Voltage		AVDD		3.9	4.0	4.1	V
Digital Supply Voltage		DVDD		1.62	1.8	1.98	V
Analog Ground Voltage		AVSS		-1.65	-1.5	-1.35	V
Digital Ground Voltage		DVSS			0		V
ANALOG SWITCH							
Input Signal Range		V_{AIN}		-1.3		3.0	V
Channel On Current		I_{CH_ON}				50	mA
Switch On-resistance		R_{ON}	V_{AIN}=-1.3V~3.0V, I_{CH_ON}=10mA		1	3	Ω
Active Discharge Resistance		R_{DIS}	Discharge to GND		10.5		kΩ
Switch Leakage Current	Channel Off Leakage Current Input	I_{CH_OFFI}	V_{AIN}=-1.3V, Input measure, *fig.1, Each switch	-50	-25		nA
	Channel Off Leakage Current Output	I_{CH_OFFO}	V_{AIN}=-1.3V, Output measure, *fig.1, Each switch	-50	-4.0		nA
	Channel On Leakage Current	I_{CH_ON}	V_{AIN}=-1.3V, Input and output values are same, Each switch	-50	-5.0		nA
	Channel Off Leakage Current Input	I_{CH_OFFI}	V_{AIN}=3.0V, Input measure, *fig.1, Each switch		3.0	20	nA
	Channel Off Leakage Current Output	I_{CH_OFFO}	V_{AIN}=3.0V, Output measure, *fig.1, Each switch		3.0	20	nA
	Channel On Leakage Current	I_{CH_ON}	V_{AIN}=3.0V, Input and output values are same, Each switch		3.0	20	nA
DIGITAL I/O							
Logic Input Voltage	Input High	V_{IH}		0.7* DVDD			V
	Input Low	V_{IL}				0.3* DVDD	V
Logic Input Current	Input High	I_{IH}		-1		1	uA
	Input Low	I_{IL}		-1		1	uA
SWITCH DYNAMIC CHARACTERISTICS							
Switching Time	Turn ON Time	t_{ON}	Clock base Load C/R = 20pF / 1Kohm		40		ns

	Turn OFF Time	t_{OFF}	Load C/R = 20pF / 1Kohm		170		ns
Capacitance	Input Off-Capacitance	C_{AIN_OFF}	Each switch		55		pF
	Output Off-Capacitance	C_{AOUT_OFF}	Each switch		55		pF
	Output On-Capacitance	C_{AOUT_ON}	Each switch		110		pF
Switching Frequency		f_{SW}	f_{CLK}=10MHz			156	KHz
POWER CONSUMPTION							
Analog Operating Current (AVDD)	Static	I_{AVDD_ST}			2.0	5.0	uA
	Dynamic	I_{AVDD_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.1	0.2	mA
			f_{CLK}=10MHz, f_{SW}=100KHz,		1.0	2.0	
Analog Operating Current (AVSS)	Static	I_{AVSS_ST}			2.0	5.0	uA
	Dynamic	I_{AVSS_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.1	0.2	mA
			f_{CLK}=10MHz, f_{SW}=100KHz,		1.0	2.0	
Digital Operating Current (DVDD)	Static	I_{DVDD_ST}			0.15	0.2	mA
	Dynamic	I_{DVDD_DYN}	f_{CLK}=10MHz, f_{SW}=100KHz, Cp = 50pF Single Command : ALL_SW_ON/OFF Cp* : Parasitic Capacitance		4.0	5.5	mA

ELECTRICAL CHARACTERISTICS (AVDD = 5.0V, AVSS = -1.5V, TA = +25°C)

AVDD=5.0V, AVSS=-1.5V, DVDD=1.8V, DVSS=0V, and TA = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
POWER SUPPLIES						
Analog Supply Voltage	AVDD		4.5	5.0	5.5	V
Digital Supply Voltage	DVDD		1.62	1.8	1.98	V
Analog Ground Voltage	AVSS		-1.65	-1.5	-1.35	V
Digital Ground Voltage	DVSS			0		V
ANALOG SWITCH						
Input Signal Range	V_{AIN}		-1.3		4.0	V
Channel On Current	I_{CH_ON}				50	mA
Switch On-resistance	R_{ON}	V_{AIN}=-1.3V~4.0V, I_{CH_ON}=10mA		0.6	2	Ω
Active Discharge Resistance	R_{DIS}	Discharge to GND		10.5		kΩ

Switch Leakage Current	Channel Off Leakage Current Input	I_{CH_OFFI}	V_{AIN}=-1.3V, Input measure, *fig.1, Each switch	-100	-60		nA
	Channel Off Leakage Current Output	I_{CH_OFFO}	V_{AIN}=-1.3V, Output measure, *fig.1, Each switch	-10	-3.0		nA
	Channel On Leakage Current	I_{CH_ON}	V_{AIN}=-1.3V, Input and output values are same, Each switch	-30	-15		nA
	Channel Off Leakage Current Input	I_{CH_OFFI}	V_{AIN}=3.0V, Input measure, *fig.1, Each switch		1.0	10	nA
	Channel Off Leakage Current Output	I_{CH_OFFO}	V_{AIN}=3.0V, Output measure, *fig.1, Each switch		1.0	10	nA
	Channel On Leakage Current	I_{CH_ON}	V_{AIN}=3.0V, Input and output values are same, Each switch		1.0	10	nA
DIGITAL I/O							
Logic Input Voltage	Input High	V_{IH}		0.7* DVDD			V
	Input Low	V_{IL}				0.3* DVDD	V
Logic Input Current	Input High	I_{IH}		-1		1	uA
	Input Low	I_{IL}		-1		1	uA
SWITCH DYNAMIC CHARACTERISTICS							
Switching Time	Turn ON Time	t_{ON}	Clock base Load C/R = 20pF / 1Kohm		30		ns
	Turn OFF Time	t_{OFF}	Load C/R = 20pF / 1Kohm		150		ns
Capacitance	Input Off-Capacitance	C_{AIN_OFF}	Each switch		60		pF
	Output Off-Capacitance	C_{AOUT_OFF}	Each switch		60		pF
	Output On-Capacitance	C_{AOUT_ON}	Each switch		120		pF
Switching Frequency		f_{SW}	f_{CLK}=10MHz			156	KHz
POWER CONSUMPTION							
Analog Operating Current (AVDD)	Static	I_{AVDD_ST}			2.0	6.0	uA
	Dynamic	I_{AVDD_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.15	0.3	mA
			f_{CLK}=10MHz, f_{SW}=100KHz,		1.1	1.8	
Analog Operating Current (AVSS)	Static	I_{AVSS_ST}			2.0	6.0	uA
	Dynamic	I_{AVSS_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.15	0.3	mA

			f_{CLK}=10MHz, f_{SW}=100KHz,		1.1	1.8	
Digital Operating Current (DVDD)	Static	I_{DVDD_ST}			0.15		mA
	Dynamic	I_{DVDD_DYN}	f_{CLK}=10MHz, f_{SW}=100KHz, Cp* = 50pF Single Command : ALL_SW_ON/OFF Cp* : Parasitic Capacitance		3.5	5.0	mA

ELECTRICAL CHARACTERISTICS (AVDD = 5.0V, AVSS = -1.5V, TA = +125°C)

AVDD=5.0V, AVSS=-1.5V, DVDD=1.8V, DVSS=0V, and TA = +125°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
POWER SUPPLIES							
Analog Supply Voltage		AVDD		4.5	5.0	5.5	V
Digital Supply Voltage		DVDD		1.62	1.8	1.98	V
Analog Ground Voltage		AVSS		-1.65	-1.5	-1.35	V
Digital Ground Voltage		DVSS			0		V
ANALOG SWITCH							
Input Signal Range		V_{AIN}		-1.3		4.0	V
Channel On Current		I_{CH_ON}				50	mA
Switch On-resistance		R_{ON}	V_{AIN}=-1.3V~4.0V, I_{CH_ON}=10mA		1	3	Ω
Active Discharge Resistance		R_{DIS}	Discharge to GND		10.5		kΩ
Switch Leakage Current	Channel Off Leakage Current Input	I_{CH_OFFI}	V_{AIN}=-1.3V, Input measure, *fig.1, Each switch	-250	-160		nA
	Channel Off Leakage Current Output	I_{CH_OFFO}	V_{AIN}=-1.3V, Output measure, *fig.1, Each switch	-50	-15		nA
	Channel On Leakage Current	I_{CH_ON}	V_{AIN}=-1.3V, Input and output values are same, Each switch	-50	-35		nA
	Channel Off Leakage Current Input	I_{CH_OFFI}	V_{AIN}=3.0V, Input measure, *fig.1, Each switch		3.0	20	nA
	Channel Off Leakage Current Output	I_{CH_OFFO}	V_{AIN}=3.0V, Output measure, *fig.1, Each switch		3.0	20	nA
	Channel On Leakage Current	I_{CH_ON}	V_{AIN}=3.0V, Input and output values are same, Each switch		3.0	20	nA
DIGITAL I/O							
Logic Input Voltage	Input High	V_{IH}		0.7* DVDD			V

	Input Low	V_{IL}				0.3* DVDD	V
Logic Input Current	Input High	I_{IH}		-1		1	uA
	Input Low	I_{IL}		-1		1	uA
SWITCH DYNAMIC CHARACTERISTICS							
Switching Time	Turn ON Time	t_{ON}	Clock base Load C/R = 20pF / 1Kohm		40		ns
	Turn OFF Time	t_{OFF}	Load C/R = 20pF / 1Kohm		170		ns
Capacitance	Input Off-Capacitance	C_{AIN_OFF}	Each switch		60		pF
	Output Off-Capacitance	C_{AOUT_OFF}	Each switch		60		pF
	Output On-Capacitance	C_{AOUT_ON}	Each switch		120		pF
Switching Frequency		f_{SW}	f_{CLK}=10MHz			156	KHz
POWER CONSUMPTION							
Analog Operating Current (AVDD)	Static	I_{AVDD_ST}			3.0	8.0	uA
	Dynamic	I_{AVDD_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.15	0.4	mA
			f_{CLK}=10MHz, f_{SW}=100KHz,		1.5	2.0	
Analog Operating Current (AVSS)	Static	I_{AVSS_ST}			3.0	8.0	uA
	Dynamic	I_{AVSS_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.15	0.4	mA
			f_{CLK}=10MHz, f_{SW}=100KHz,		1.5	2.0	
Digital Operating Current (DVDD)	Static	I_{DVDD_ST}			0.15	0.2	mA
	Dynamic	I_{DVDD_DYN}	f_{CLK}=10MHz, f_{SW}=100KHz, Cp = 50pF Single Command : ALL_SW_ON/OFF Cp* : Parasitic Capacitance		4.0	5.5	mA

ELECTRICAL CHARACTERISTICS (AVDD = 5.5V, AVSS = 0V, TA = +25°C)

AVDD=5.5V, AVSS=0V, DVDD=1.8V, DVSS=0V, and TA = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
POWER SUPPLIES						
Analog Supply Voltage	AVDD		5.4	5.5	5.6	V
Digital Supply Voltage	DVDD		1.62	1.8	1.98	V
Analog Ground Voltage	AVSS			0		V
Digital Ground Voltage	DVSS			0		V
ANALOG SWITCH						

Input Signal Range		V_{AIN}		3.0		5.3	V
Channel On Current		I_{CH_ON}				50	mA
Switch On-resistance		R_{ON}	V_{AIN}=3.0V~5.3V, I_{CH_ON}=10mA		1.3	2.5	Ω
Active Discharge Resistance		R_{DIS}	Discharge to GND		10.5		kΩ
Switch Leakage Current	Channel Off Leakage Current Input	I_{CH_OFFI}	V_{AIN}=5.3V, Input measure, *fig.1, Each switch		2.0	20	nA
	Channel Off Leakage Current Output	I_{CH_OFFO}	V_{AIN}=5.3V, Output measure, *fig.1, Each switch	-30	-10		nA
	Channel On Leakage Current	I_{CH_ON}	V_{AIN}=5.3V, Input and output values are same, Each switch		1.0	10	nA
DIGITAL I/O							
Logic Input Voltage	Input High	V_{IH}		0.7* DVDD			V
	Input Low	V_{IL}				0.3* DVDD	V
Logic Input Current	Input High	I_{IH}		-1		1	uA
	Input Low	I_{IL}		-1		1	uA
SWITCH DYNAMIC CHARACTERISTICS							
Switching Time	Turn ON Time	t_{ON}	Clock base (calculated for special condition) Load C/R = 20pF / 1Kohm		30		ns
	Turn OFF Time	t_{OFF}	Load C/R = 20pF / 1Kohm		150		ns
Capacitance	Input Off-Capacitance	C_{AIN_OFF}	Each switch		55		pF
	Output Off-Capacitance	C_{AOUT_OFF}	Each switch		55		pF
	Output On-Capacitance	C_{AOUT_ON}	Each switch		110		pF
Switching Frequency		f_{SW}	f_{CLK}=10MHz			156	KHz
POWER CONSUMPTION							
Analog Operating Current (AVDD)	Static	I_{AVDD_ST}			1.0	3.0	uA
	Dynamic	I_{AVDD_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.1	0.15	mA
			f_{CLK}=10MHz, f_{SW}=100KHz,		1	1.5	
Analog Operating Current (AVSS)	Static	I_{AVSS_ST}			1.0	3.0	uA
	Dynamic	I_{AVSS_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.1	0.15	mA
			f_{CLK}=10MHz, f_{SW}=100KHz,		1	1.5	
Digital	Static	I_{DVDD_ST}			0.15		mA

Operating Current (DVDD)	Dynamic	I_{DVDD_DYN}	f_{CLK}=10MHz, f_{SW}=100KHz, Cp* = 50pF Single Command : ALL_SW_ON/OFF Cp* : Parasitic Capacitance		3.5	5.0	mA

ELECTRICAL CHARACTERISTICS (AVDD = 5.5V, AVSS = 0V, TA = +125°C)

AVDD=5.5V, AVSS= 0V, DVDD=1.8V, DVSS=0V, and TA = +125°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
POWER SUPPLIES							
Analog Supply Voltage		AVDD		5.4	5.5	5.6	V
Digital Supply Voltage		DVDD		1.62	1.8	1.98	V
Analog Ground Voltage		AVSS			0		V
Digital Ground Voltage		DVSS			0		V
ANALOG SWITCH							
Input Signal Range		V_{AIN}		3.0		5.3	V
Channel On Current		I_{CH_ON}				50	mA
Switch On-resistance		R_{ON}	V_{AIN}=3.0V~5.3V, I_{CH_ON}=10mA		1.9	3	Ω
Active Discharge Resistance		R_{DIS}	Discharge to GND		10.5		kΩ
Switch Leakage Current	Channel Off Leakage Current Input	I_{CH_OFFI}	V_{AIN}=5.3V, Input measure, *fig.1, Each switch		15	50	nA
	Channel Off Leakage Current Output	I_{CH_OFFO}	V_{AIN}=5.3V, Output measure, *fig.1, Each switch	-100	-45		nA
	Channel On Leakage Current	I_{CH_ON}	V_{AIN}=5.3V, Input and output values are same, Each switch		2	50	nA
DIGITAL I/O							
Logic Input Voltage	Input High	V_{IH}		0.7* DVDD			V
	Input Low	V_{IL}				0.3* DVDD	V
Logic Input Current	Input High	I_{IH}		-1		1	uA
	Input Low	I_{IL}		-1		1	uA
SWITCH DYNAMIC CHARACTERISTICS							
Switching Time	Turn ON Time	t_{ON}	Clock base (calculated for special condition) Load C/R = 20pF / 1Kohm		40		ns
	Turn OFF Time	t_{OFF}	Load C/R = 20pF / 1Kohm		170		ns

Capacitance	Input Off-Capacitance	C_{AIN_OFF}	Each switch		55		pF
	Output Off-Capacitance	C_{AOUT_OFF}	Each switch		55		pF
	Output On-Capacitance	C_{AOUT_ON}	Each switch		110		pF
Switching Frequency		f_{SW}	f_{CLK}=10MHz			156	KHz
POWER CONSUMPTION							
Analog Operating Current (AVDD)	Static	I_{AVDD_ST}			2.0	5.0	uA
	Dynamic	I_{AVDD_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.1	0.2	mA
			f_{CLK}=10MHz, f_{SW}=100KHz,		1	2	
Analog Operating Current (AVSS)	Static	I_{AVSS_ST}			2.0	5.0	uA
	Dynamic	I_{AVSS_DYN}	f_{CLK}=10MHz, f_{SW}=10KHz,		0.1	0.2	mA
			f_{CLK}=10MHz, f_{SW}=100KHz,		1	2	
Digital Operating Current (DVDD)	Static	I_{DVDD_ST}			0.15	0.2	mA
	Dynamic	I_{DVDD_DYN}	f_{CLK}=10MHz, f_{SW}=100KHz, Cp* = 50pF Single Command : ALL_SW_ON/OFF Cp* : Parasitic Capacitance		4.0	5.5	mA

TEST CIRCUITS

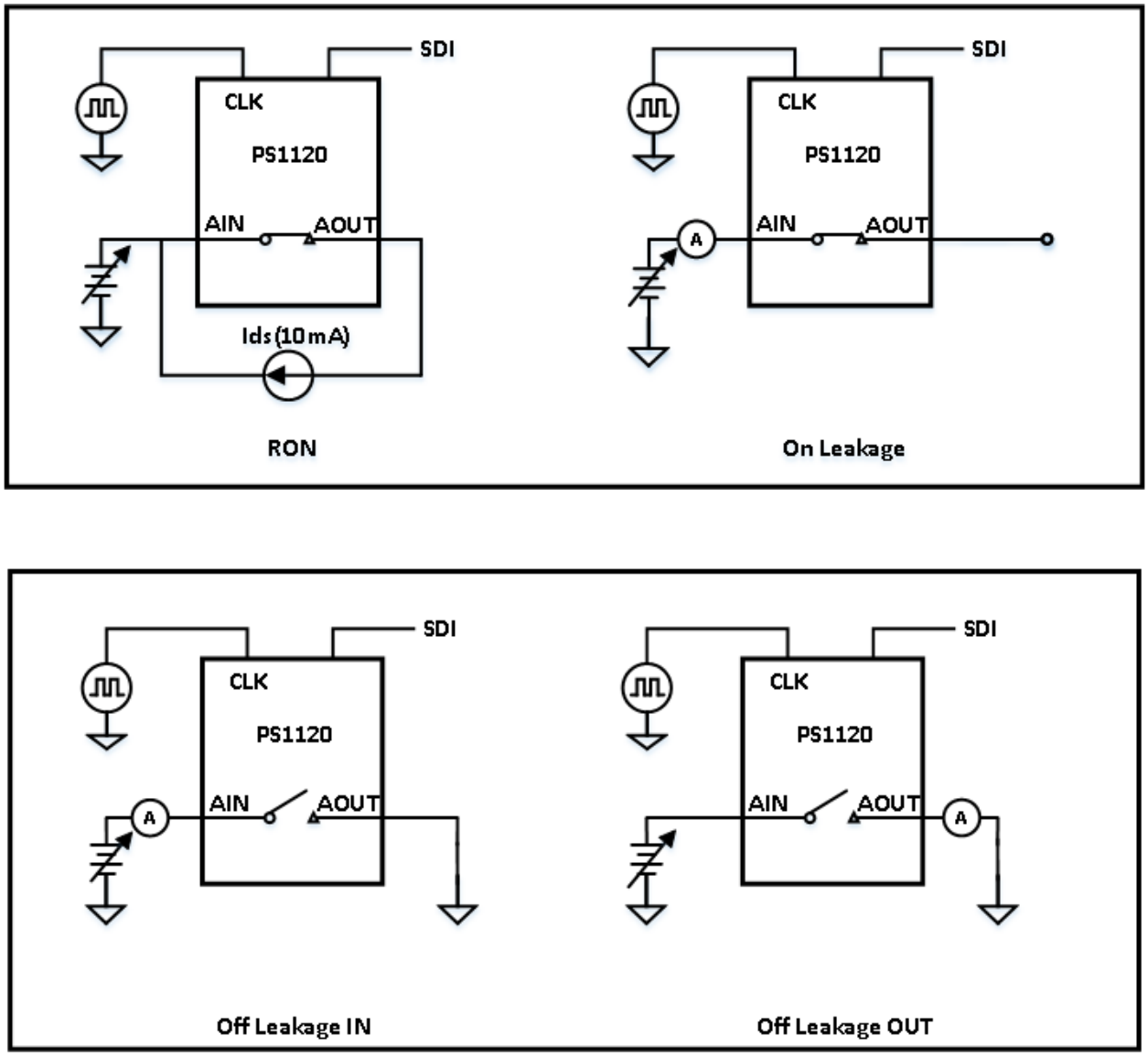
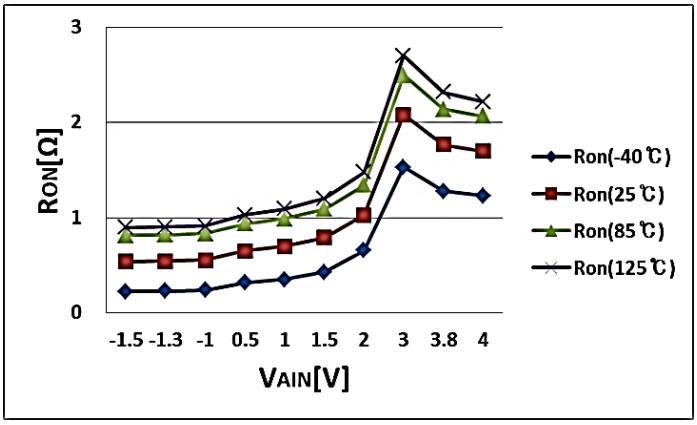


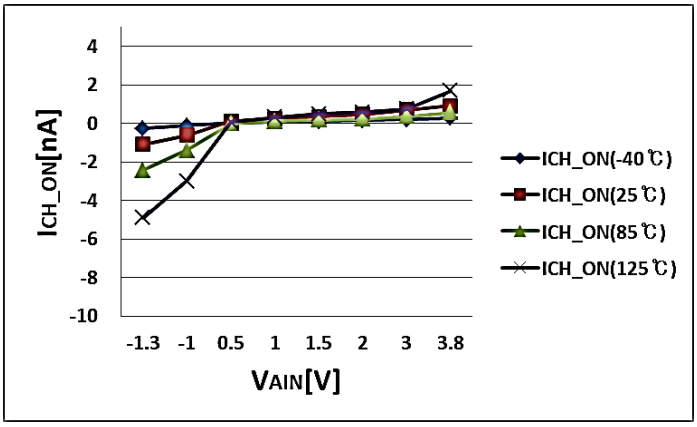
Figure 1. TEST Circuits

TEST RESULTS

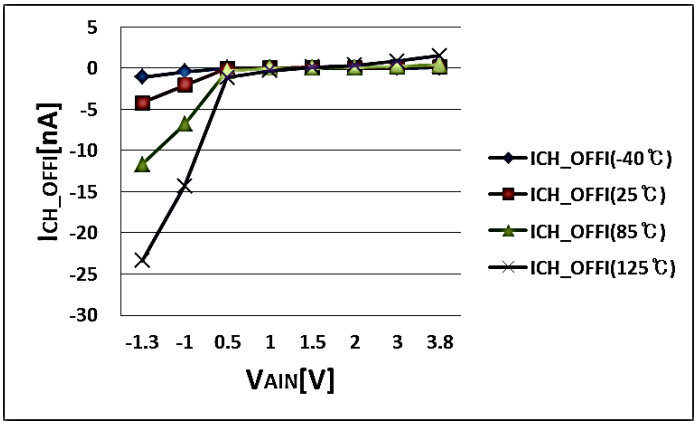
AVDD=4.0V, AVSS=-1.5V, DVDD=1.8V, DVSS=0V



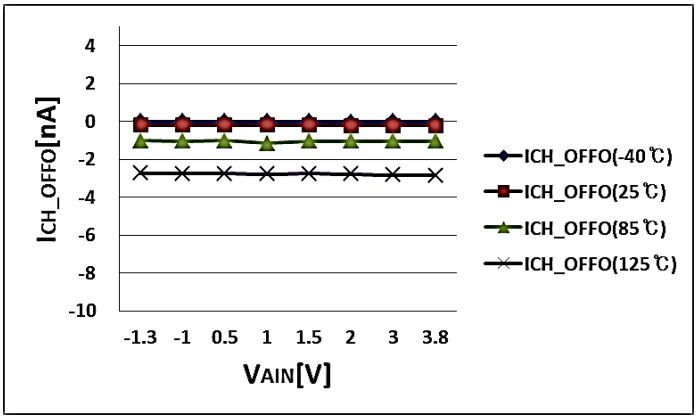
RON VS. VAIN



ICH_ON VS. VAIN



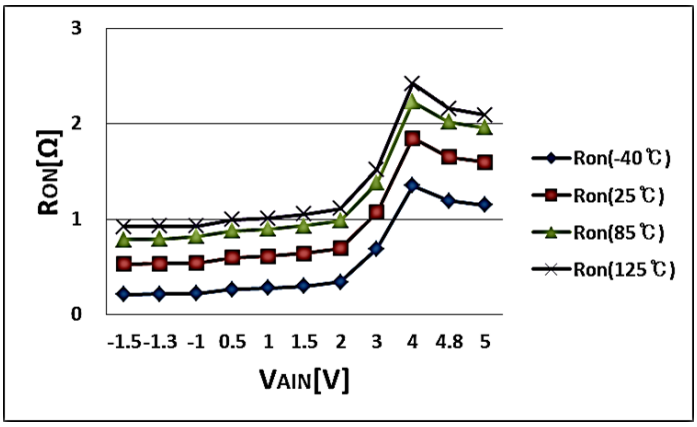
ICH_OFFI VS. VAIN



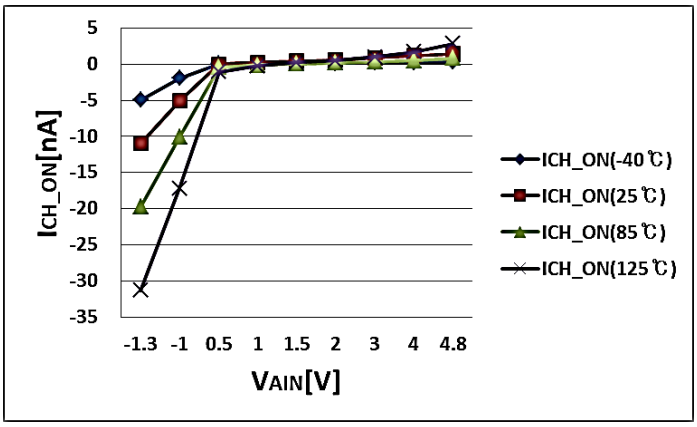
ICH_OFFO VS. VAIN

Figure 2. Test Results (AVDD=4.0V, AVSS=-1.5V)

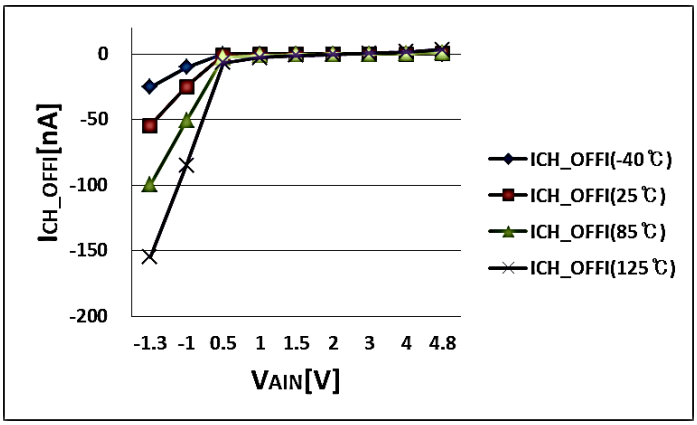
AVDD=5.0V, AVSS=-1.5V, DVDD=1.8V, DVSS=0V



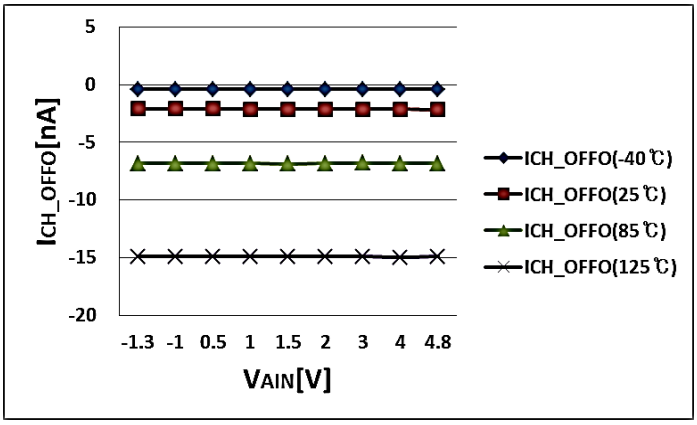
RON VS. VAIN



ICH_ON VS. VAIN



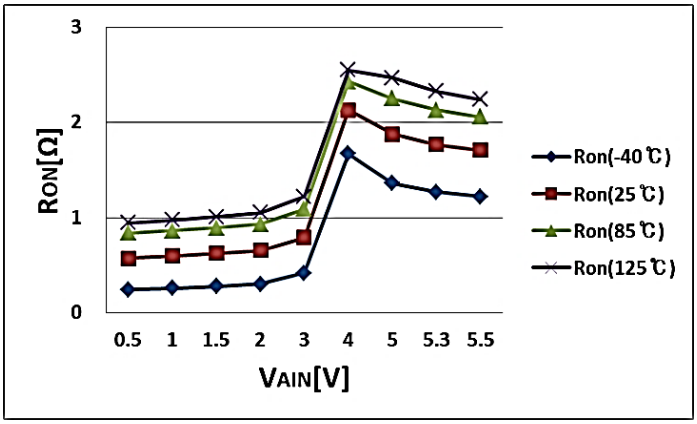
ICH_OFFI VS. VAIN



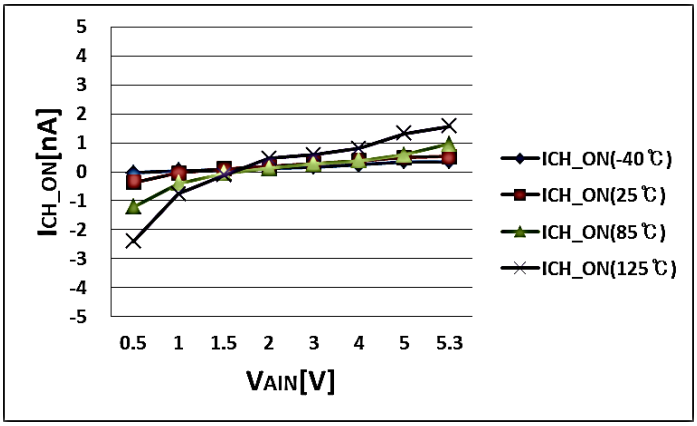
ICH_OFFO VS. VAIN

Figure 3. Test Results (AVDD=5.0V, AVSS=-1.5V)

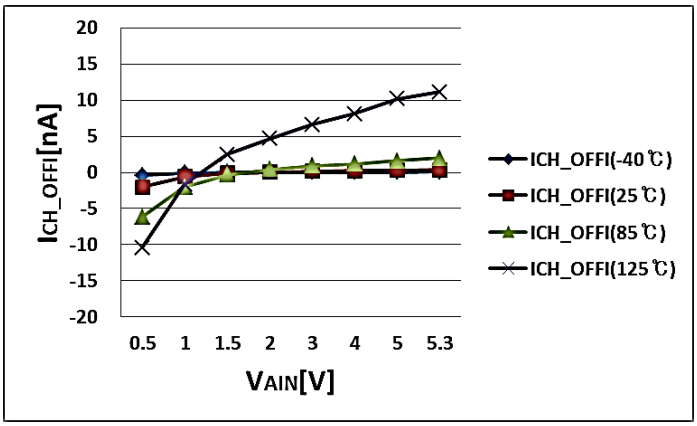
AVDD=5.5V, AVSS=0V, DVDD=1.8V, DVSS=0V



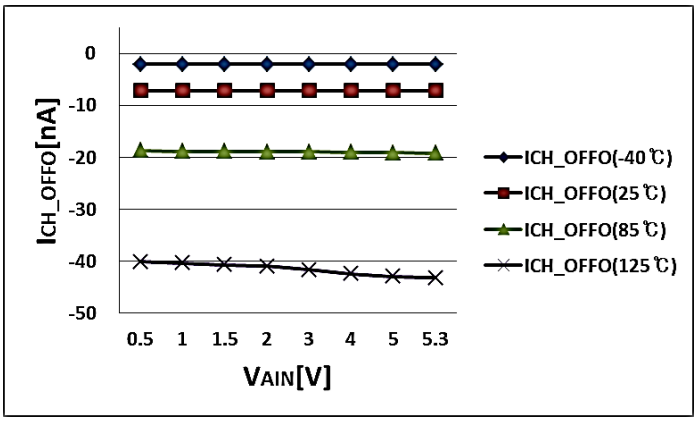
RON VS. VAIN



ICH_ON VS. VAIN



ICH_OFFI VS. VAIN



ICH_OFFO VS. VAIN

Figure 4. Test Results (AVDD=5.5V, AVSS=0V)

Timing Diagram of Digital SPI I/O Signals

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
SCLK_IN Period	t_{PERIOD}	SPI Clock Speed 10MHz	-		100	ns
SDI Setup Time	t_{SS}		5		25	ns
SDI Hold Time	t_{SH}		5		25	ns
CSN Setup Time	t_{CS}		10		50	ns
CSN Hold Time	t_{CH}		10		50	ns
SCLK_OUT Setup Time	t_{SOS}		1		7	ns
SCLK_IN High Pulse	t_{PH}	ratio of SCLK_IN	40		60	%
SCLK_IN Low Pulse	t_{PL}	ratio of SCLK_IN	60		40	%

Write Timing

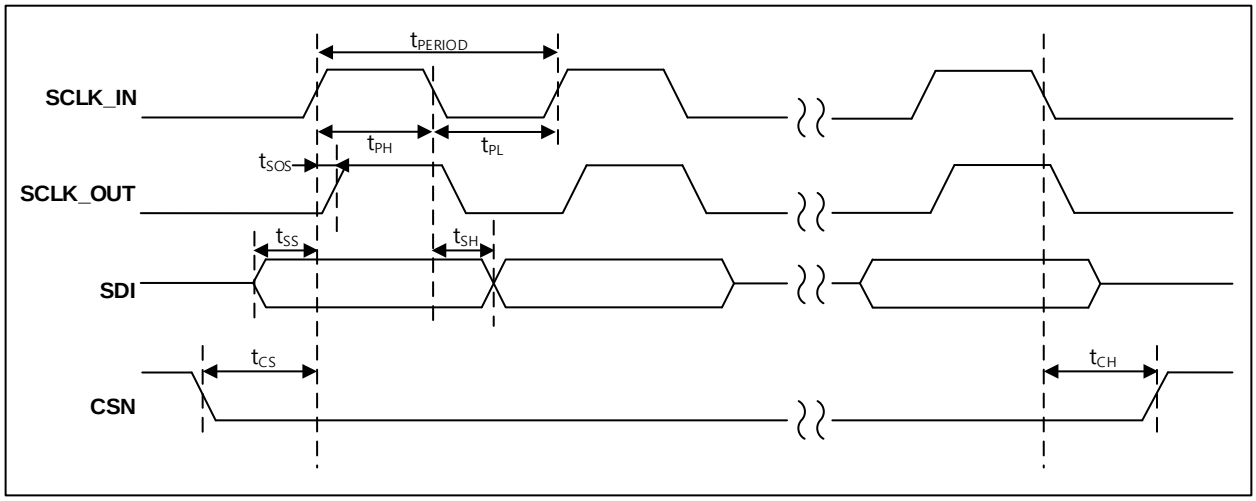
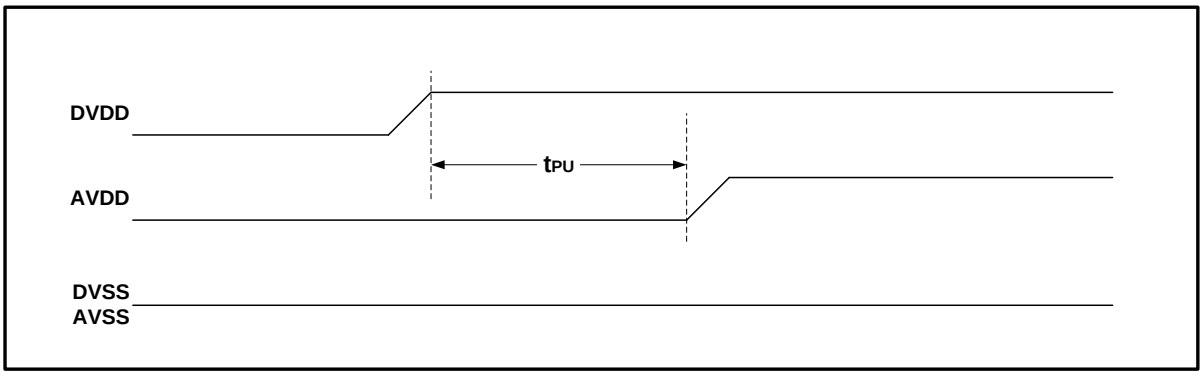


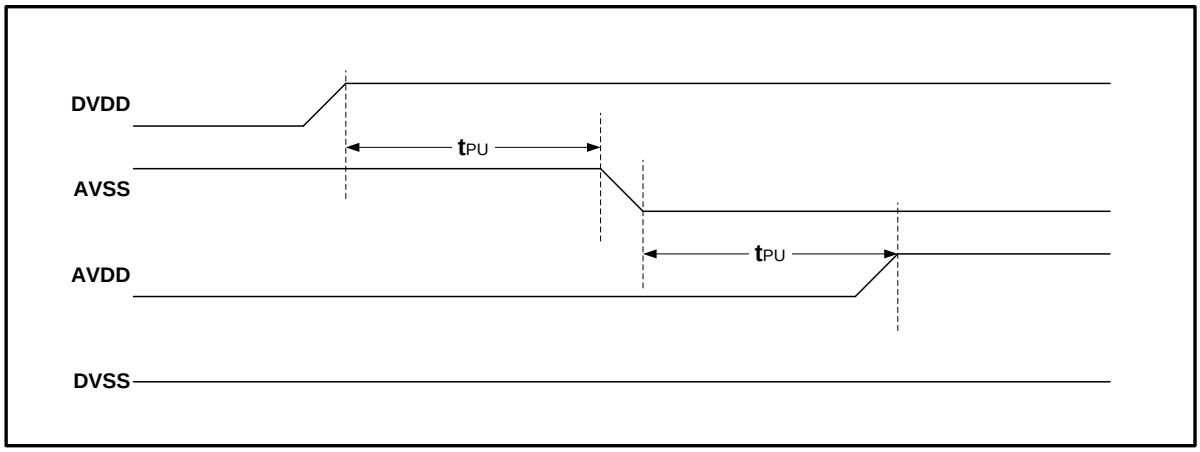
Figure 5. Timing Diagram of Digital Signals

Timing Diagram of Power Sequence

Power-up Sequence (tPU = 500us)



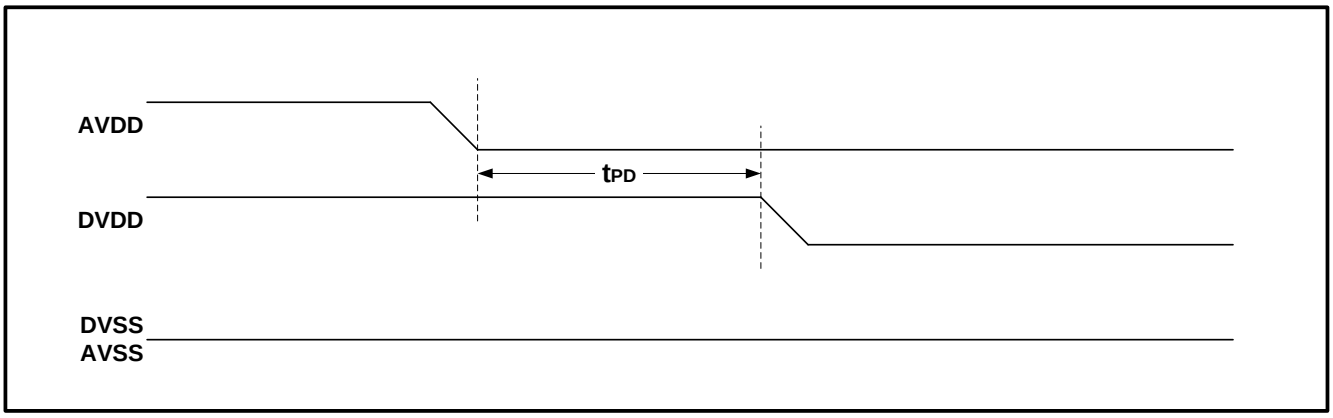
(a) In case AVSS = 0 V



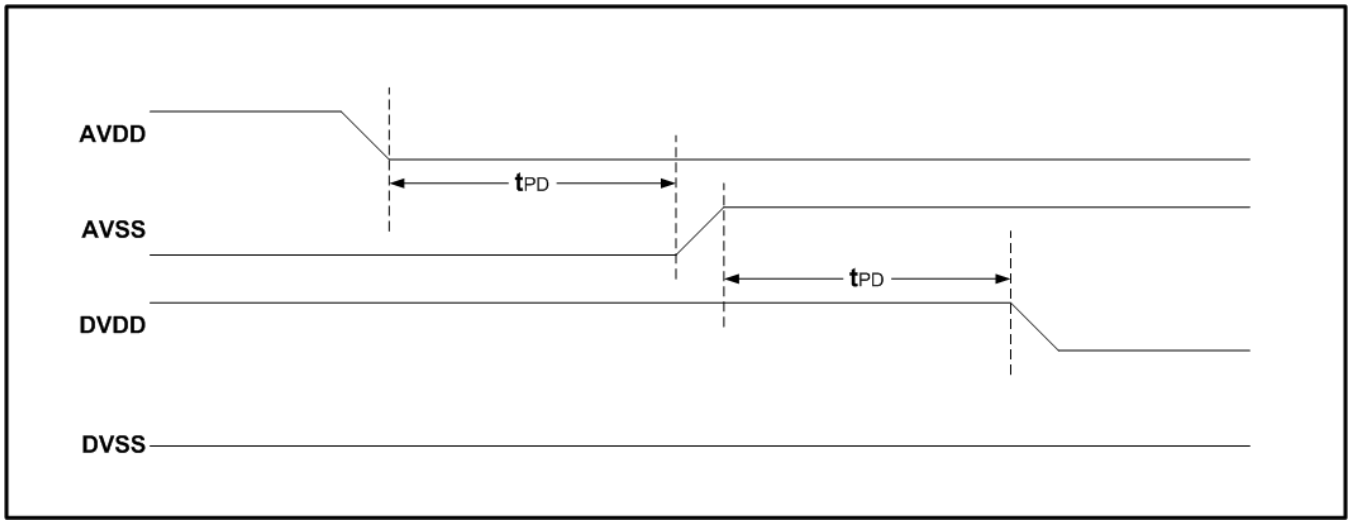
(b) In case AVSS = -1.5 V

Figure 6. Power-up Sequence

Power-down Sequence (tPD = 500us)



(a) In case AVSS = 0 V



(a) In case AVSS = -1.5 V

Figure 7. Power-down Sequence

Functional Description

Example Connecting PS1120

- 120 channel Stack Structure

Figure 8 shows the stack structure of the 120 channel PS1120.

The 120-channel stack has a structure in which two PS1120 chips are connected.

The chip #0 executes a switch operation of 0CH to 59CH, and the chip #1 executes a switch operation of 60CH to 119CH.

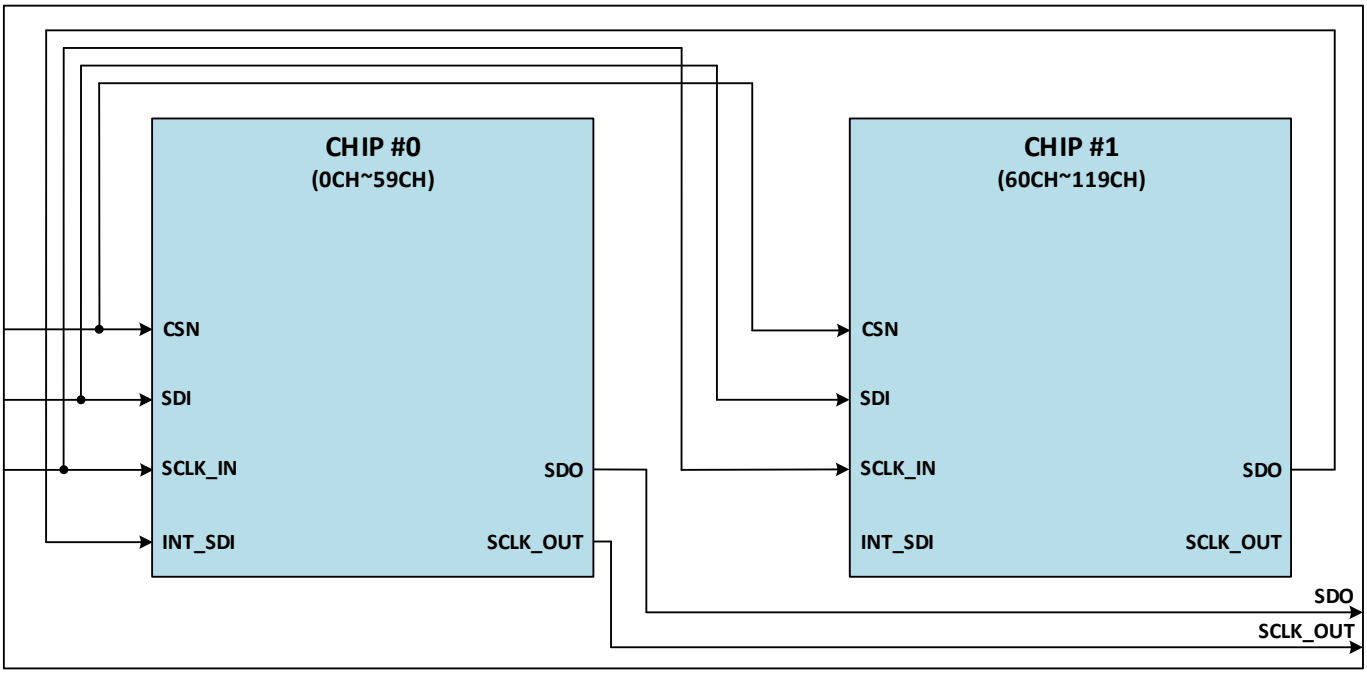


Figure 8. Block Diagram of 120CH Stack Structure

- Connection of 8-chip Daisy Chain with FPGA

Figures 9 and figure 10 show how to configure a daisy chain using the PS1120. In this case, it requires more Operation (OP) cycles than operating commands using one PS1120 chip.

See the Operating (OP) Cycle section for more information on the OP cycle.

■ *No Shared PIN Daisy Chain*

Figure 9 shows a structure in which eight daisy chains are composed of n groups.

The SCLK, SDI and CSN coming from the host (FPGA) independently connected to each group.

In this case, the number of host (FPGA) pins for controlling the group increases, but since different pins used for each group, there is an advantage that the user can control the chain as desired.

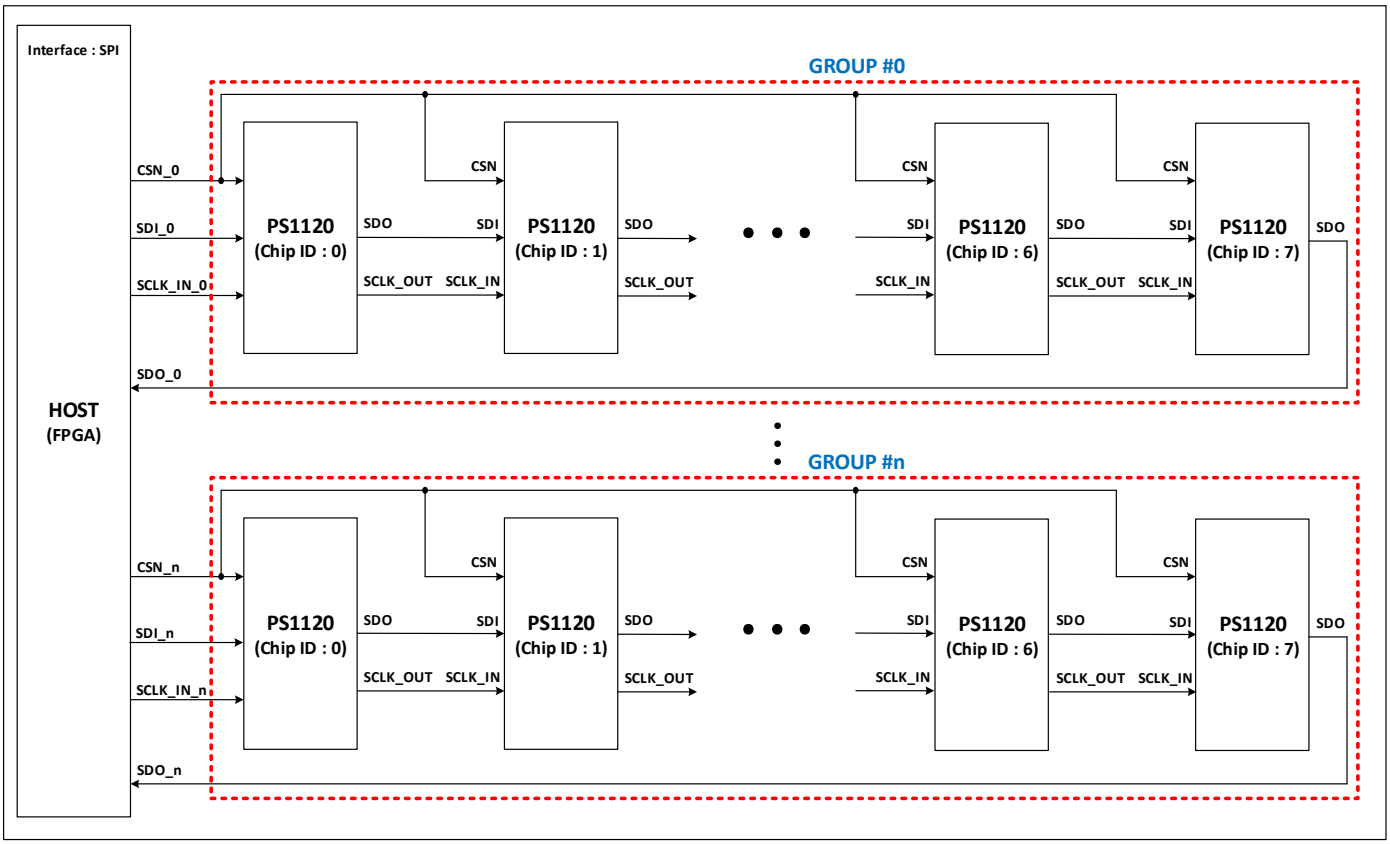


Figure 9. Connection of No Shared Pin Daisy Chain

- ***Shared Pin Daisy Chain***

Figure 10 shows a structure in which eight daisy chains organized into n groups. The SCLK and SDI coming from the host (FPGA) shared and only CSN used independently.

You can use different CSNs for each group to control the chain usage, but you have to share the SDI and SCLK to operate the chain.

In this case, each group has the same SDI and SCLK inputs, but it has the advantage of reducing the number of host (FPGA) pins to control the group.

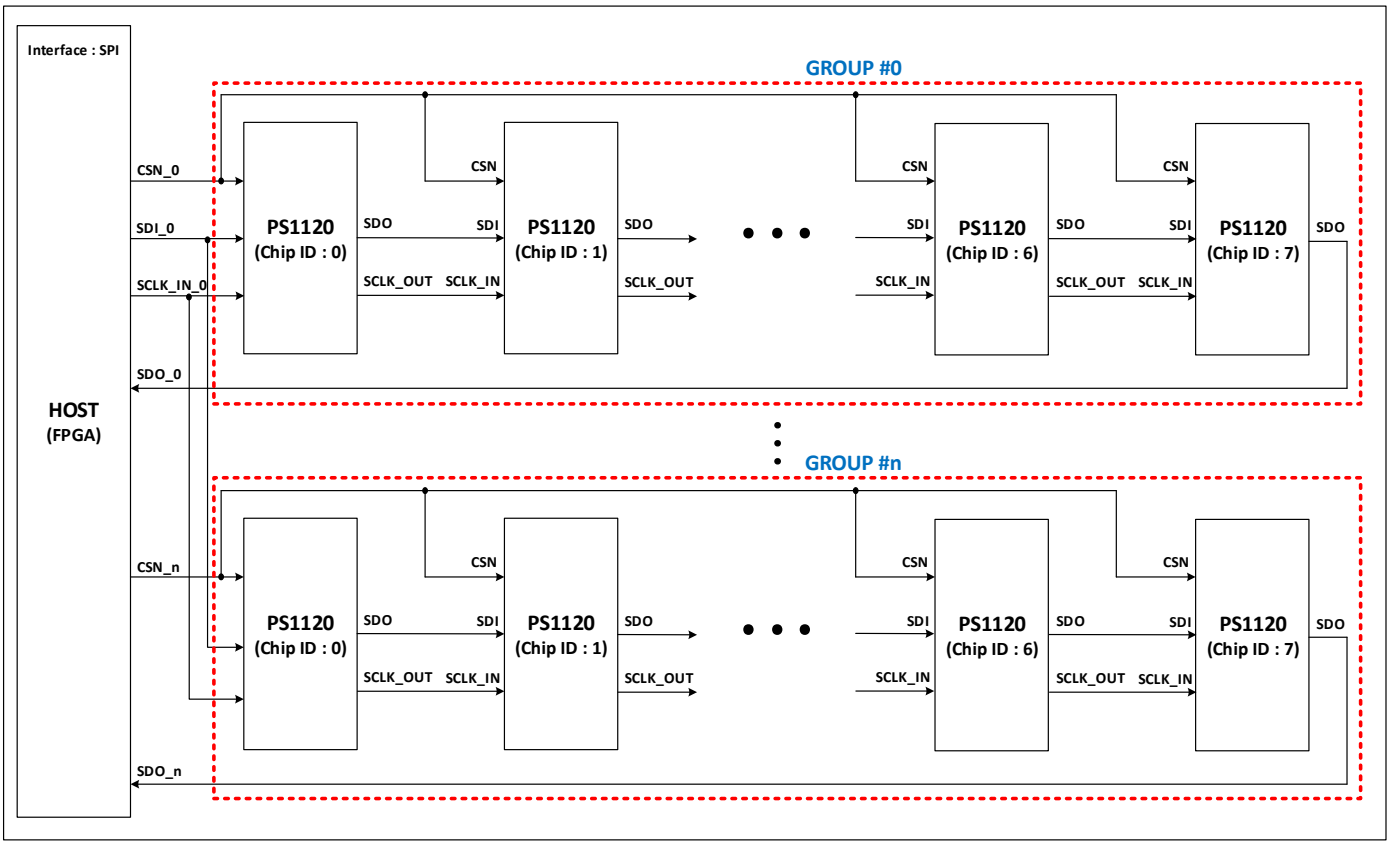


Figure 10. Connection of Shared Pin Daisy Chain

Power-up Sequence

The PS1120 operates at a frequency of 10MHz by default.

The power up sequence of the PS1120 must be greater than 102us (period 100ns * 1024 cycles) on the SCLK pin after DVDD, AVSS and AVDD are applied.

PS1120 is a structure that does not have a reset pin and creates a system reset by using Digital POR.

System reset is release after at least 1100 clock based on SCLK.

Figure 11 shows the flow diagram for the power-up sequence.

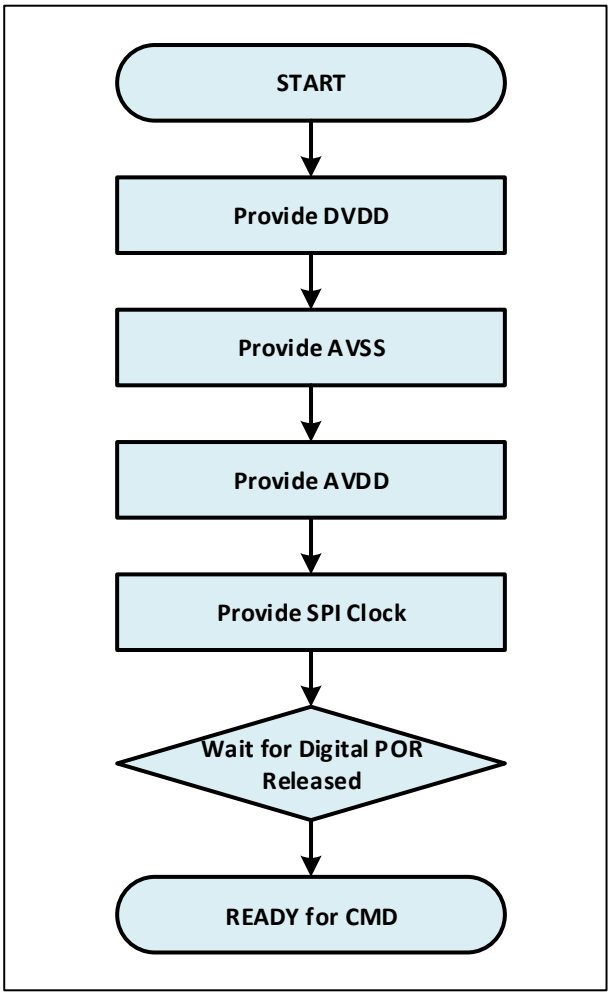


Figure 11. Flow Diagram of Power-up Sequence

Analog & Digital TOP Block Diagram

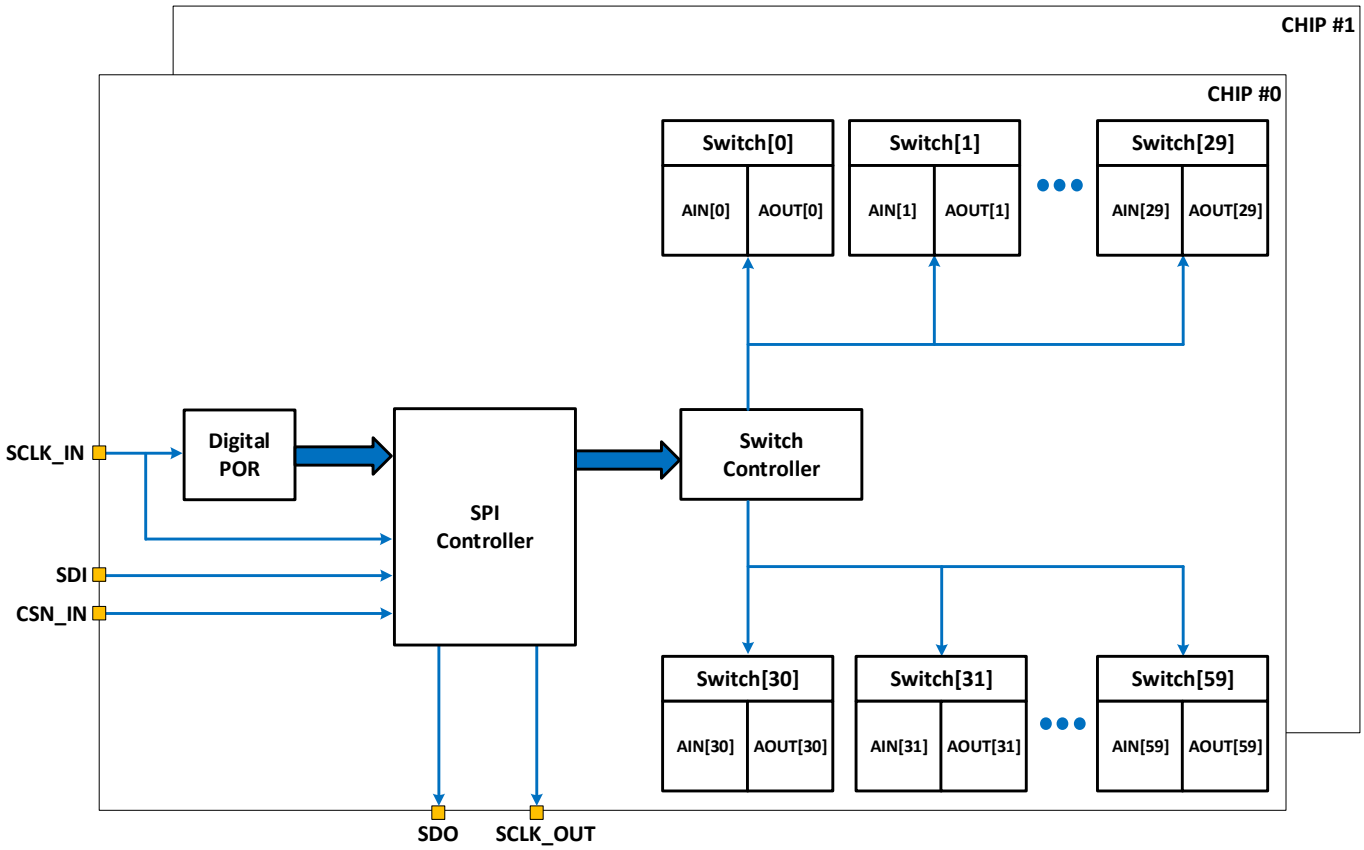


Figure 12. PS1120 Analog & Digital TOP Block Diagram

Figure 12 shows the analog and digital top block diagram of the PS1120.

The PS1120 has an SPI interface without an external reset input. Thus, when power is applied and the SPI clock comes in, the POR reset will be output via the digital POR block after a specific time based on the power-on sequence.

The SPI clock and reset are used as inputs for digital logic such as the SPI controller and the switch controller. After that, the switch operation commands can be received via the SPI interface to control the switch.

Hardware Branch Block Diagram

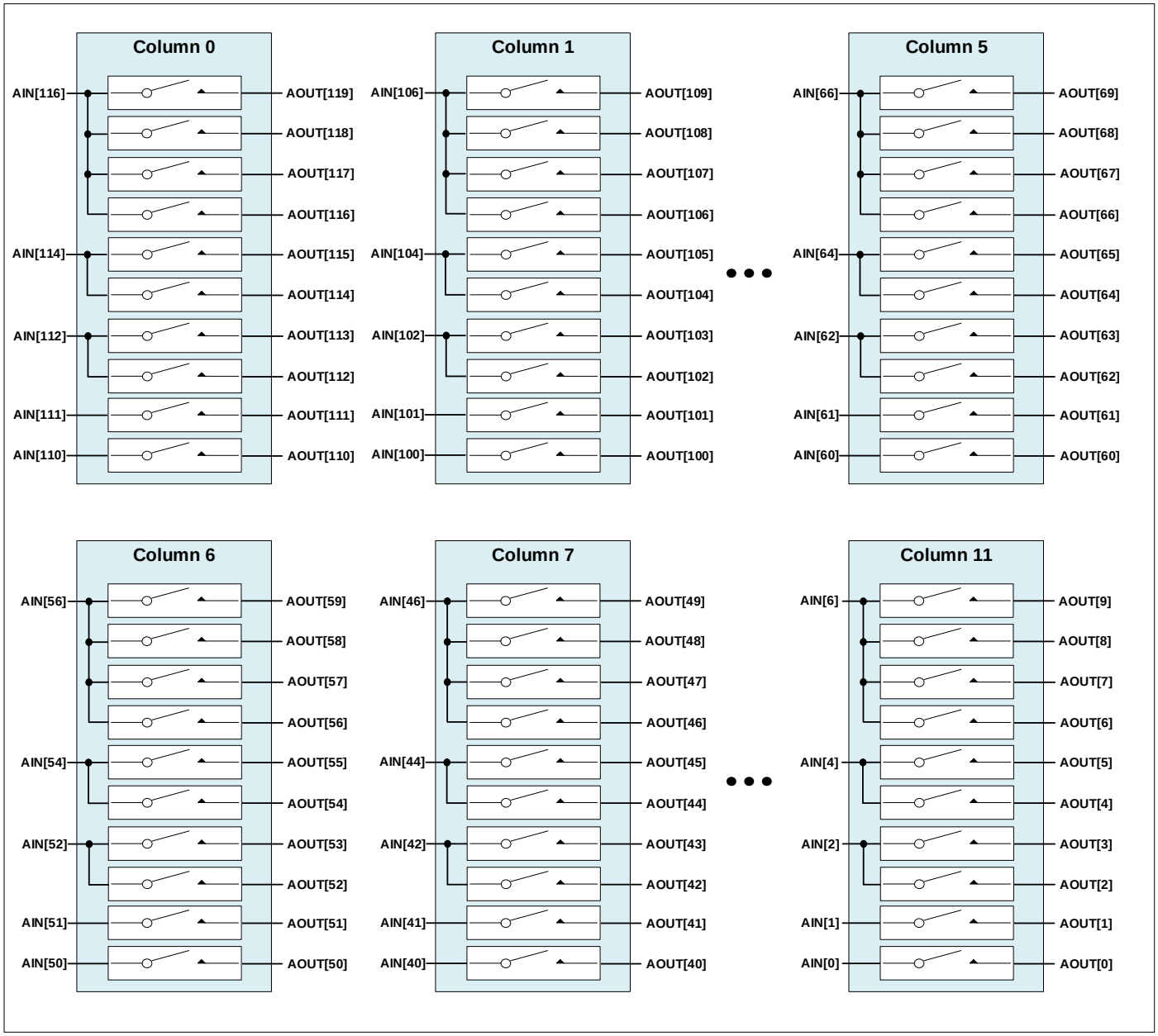


Figure 13. PS1120 Hardware Branch Block Diagram of 120 channel PS1120

Figure 13 is a block diagram of a 120-channel PS1120 configured for a 1: 1: 2: 2: 4 hardware branches.

Hardware branching is a method of connecting the input AIN on the package to the output AOUT.

This method allows AOUT to be controlled using a small number of AIN instead of 1: 1 matching when connecting AIN and AOUT.

Using this hardware branch reduces the number of AINs that control AOUT for 120 channels.

Internal Structure Block Diagram

Figure 14 is a block diagram of a 120-channel PS1120 internal structure and consists of 10 rows and 12 columns.

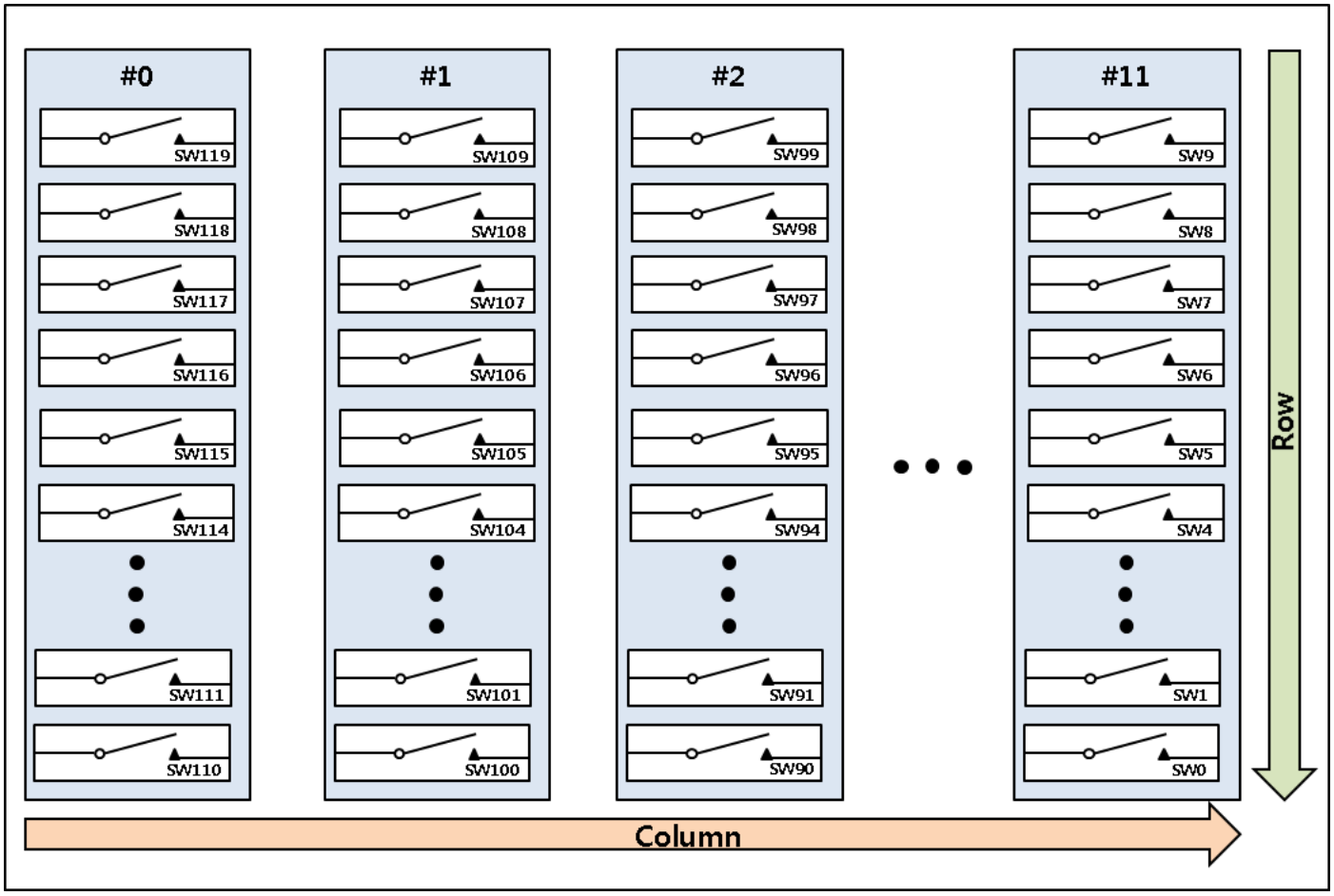


Figure 14. PS1120 Internal Structure Block Diagram

Command Sequence

Figure 15 and figure 16 show the command frames used on a 120-channel PS1120.

The Select Chip Command is used to execute only the selected chip if up to eight chips are in a daisy chain and the All Chip Command is used to perform the same operation for all chips.

All Chip Command

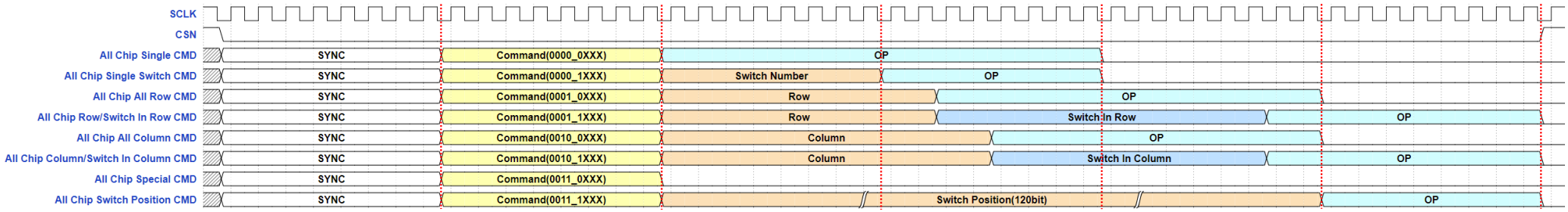


Figure 15. All Chip Command Sequence

Select Chip Command

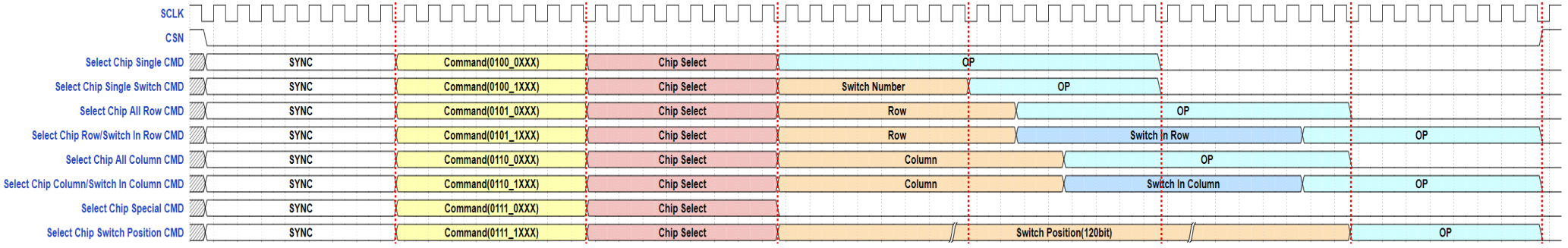


Figure 16. Select Chip Command Sequence

Functional Description of Field

SYNC Field

The reason for the synchronization field in the command frame is as follows

1. To find the starting point of the command because there is no synchronous clock inside PS1120
2. To minimize the noise of the SPI interface signal
3. Because frame length are different for each command, command frame need the sync value to determine the starting and ending point.

The data structure of the synchronization field consists of 0xAA. Figure 17 shows the timing diagram for the sync field.

After 0xAA is input, PS1120 can execute the received command for switch operation.

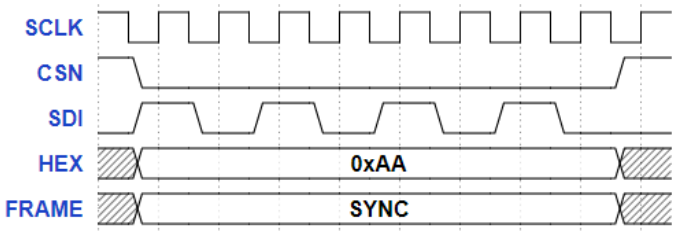


Figure 17. Timing Diagram of Sync Field

Command Field

The command field consists of a combination of CMD [4: 0] and SW_ST [2: 0] as shown in the timing diagram of figure 18.

The CMD [4: 0] field contains the value of the switch operating range.

The SW_ST [2: 0] field contains values that change the status of the switch, such as ON, OFF, HOLD, RELEASE, and FORCE.

The command field can also be composed of special commands.

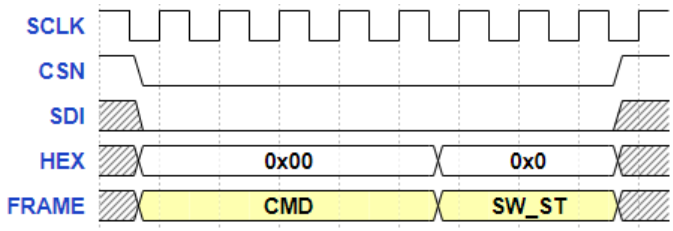


Figure 18. Timing Diagram of Command field

- **User Command Field**

  - ***CMD Value***

Table 1 shows the CMD value. For each CMD value, user can configure the command for the desired operation.

Table 1. CMD Value

CMD	Description
b’00000	Operating all switches on all chip
b’00001	Operating only one switch on all chip
b’00010	Operating all switches of the selected row on all chip
b’00011	Operating only the selected switches in the selected row on all chip
b’00100	Operating all switches of the selected column on all chip
b’00101	Operating only the selected switches in selected column on all chip
b’00110	Operating special command on all chip
b’00111	Operating only the selected switches on all chip
b’01000	Operating all switches on selected chip
b’01001	Operating only one switch on selected chip
b’01010	Operating all switches of the selected row on selected chip
b’01011	Operating only the selected switches in the selected row on selected chip
b’01100	Operating all switches of the selected column on selected chip
b’01101	Operating only the selected switches in the selected column on selected chip
b’01110	Operating special command on selected chip
b’01111	Operating only the selected switches on selected chip

- ***Switch Status Value***

Table 2 shows the SW_ST values that define the behavior of the switch status.

Based on the value, user can turn the switch ON or OFF, create a HOLD flag, RELEASE the hold flag, or execute a FORCE command to force the switch to operate.

Table 2. SW_ST Value

SW_ST	Description
b’000	OFF (Switch OFF the Normal switch except HOLD Switch)
b’001	ON (Switch ON the Normal switch except HOLD Switch)
b’010	HOLD OFF (Switch OFF and Enable HOLD FLAG for the Normal switch)
b’011	HOLD ON (Switch ON and Enable HOLD FLAG for the Normal switch)
b’100	RELEASE OFF (Switch OFF and Remove HOLD FLAG only for the HOLD switch)
b’101	RELEASE ON (Switch ON and Remove HOLD FLAG only for the HOLD switch)
b’110	FORCE OFF (All Switch OFF, Remove HOLD FLAG)
b’111	FORCE ON (All Switch ON, Remove HOLD FLAG)

- **Special Command Field**

Table 3 shows the fields for special commands.

The special command fields describe chip ID assignment, disable of active discharge and enable of active discharge and a pattern reset command for initializing the status of the switch.

Table 3. Special Command Field

CMD	SW_ST	Description
b’00110	b'000	Reserved
	b'001	Reserved
	b'010	Reserved
	b'011	Reserved
	b'100	Active Discharge Disable
	b'101	Active Discharge Enable
	b'110	Reserved
	b'111	Chip Address Assignment
b’01110	b'000	Reserved
	b'001	Reserved
	b'010	Reserved
	b'011	Reserved
	b'100	Select Chip Active Discharge Disable
	b'101	Select Chip Active Discharge Enable
	b'110	Reserved
	b'111	Reserved
b’11111	b’111	Pattern Reset

List of Command

Below is a list of commands for the operation of the PS1120 switch consisting of 120 channels.

The command frame sent through the SPI interface, so it becomes valid data only when the CSN is low and keep the input data at zero before executing the command or if the CSN is high.

The OP (operation cycle) indicates the operation time of the command at the time of command input, and the size of the OP differs depending on the type of command.

See Operating (OP) Cycle Field for consist of frame.

- All Chip Command

Table 4 shows a list of commands executed on all chip.

Table 4. All Chip Command List

Command	Name	Frame
b'0000_0xxx	ALL_SW	SYNC[7:0] + Command[7:0] + OP[15:0]
b'0000_1xxx	ONE_SW	SYNC[7:0] + Command[7:0] + SW_NUM[7:0] + OP[7:0]
b'0001_0xxx	SEL_ROW_SW	SYNC[7:0] + Command[7:0] + ROW[9:0] + OP[13:0]
b'0001_1xxx	SEL_ROW_SEL_ROW_IN_SW	SYNC[7:0] + Command[7:0] + ROW[9:0] + SW_IN_ROW[11:0] + OP[9:0]
b'0010_0xxx	SEL_COL_SW	SYNC[7:0] + Command[7:0] + COL[11:0] + OP[11:0]
b'0010_1xxx	SEL_COL_SEL_COL_IN_SW	SYNC[7:0] + Command[7:0] + COL[11:0] + SW_IN_COL[9:0] + OP[9:0]
b'0011_1xxx	SEL_SW_POS	SYNC[7:0] + Command[7:0] + SW_POS[119:0] + OP[7:0]

- Select Chip Command

Table 5 shows a list of commands executed on select chip.

Table 5. Select Chip Command List

Command	Name	Frame
b'0100_0xxx	CS_ALL_SW	SYNC[7:0] + Command[7:0] + CS[7:0] + OP[15:0]
b'0100_1xxx	CS_ONE_SW	SYNC[7:0] + Command[7:0] + CS[7:0] + SW_NUM[7:0] + OP[7:0]
b'0101_0xxx	CS_SEL_ROW_SW	SYNC[7:0] + Command[7:0] + CS[7:0] + ROW[9:0] + OP[13:0]
b'0101_1xxx	CS_SEL_ROW_SEL_ROW_IN_SW	SYNC[7:0] + Command[7:0] + CS[7:0] + ROW[9:0] + SW_IN_ROW[11:0] + OP[9:0]
b'0110_0xxx	CS_SEL_COL_SW	SYNC[7:0] + Command[7:0] + CS[7:0] + COL[11:0] + OP[11:0]
b'0110_1xxx	CS_SEL_COL_SEL_COL_IN_SW	SYNC[7:0] + Command[7:0] + CS[7:0] + COL[11:0] + SW_IN_COL[9:0] + OP[9:0]
b'0111_1xxx	CS_SEL_SW_POS	SYNC[7:0] + Command[7:0] + CS[7:0] + SW_POS[119:0] + OP[7:0]

- **Special Command**

Table 6 lists special commands. The frame configuration differs for each command.

Table 6. Special Command

Command	Name	Frame
b’0011_0100	ACTIVE_DISCHAR_DIS	SYNC[7:0] + Command[7:0] + OP[7:0]
b’0011_0101	ACTIVE_DISCHAR_ENA	SYNC[7:0] + Command[7:0] + OP[7:0]
b’0011_0111	CHIP_ASSIGN	SYNC[7:0] + Command[7:0] + CHIP_ADDR[7:0] + OP[7:0]
b’0111_0100	CS_ACTIVE_DISCHAR_DIS	SYNC[7:0] + Command[7:0] + CS[7:0] + OP[7:0]
b’0111_0101	CS_ACTIVE_DISCHAR_ENA	SYNC[7:0] + Command[7:0] + CS[7:0] + OP[7:0]
b’1111_1111	PATTERN_RST	0xFFFF_FFFF_FFFF_FFFF_FFFF_FFFF_FFFF_FFFF_ FFFF_00 + OP[15:0]

CHIP Address Field

Chip address field is a field to set chip ID of PS1120. As shown in figure 19, the chip address field is composed of 8 bits. If the chip assign is incorrect, you need to re-execute the chip assign command after pattern reset to reassign the chip ID of each PS1120.

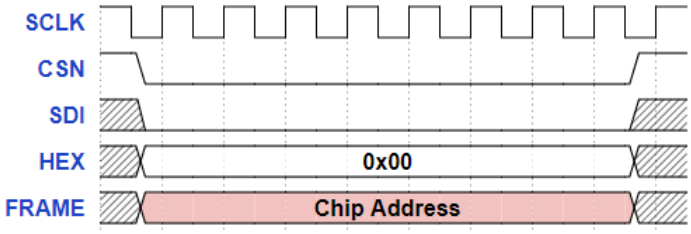


Figure 19. Timing Diagram of Chip Address

Table 7 shows the chip ID values assigned based on the value of the chip address field. The chip ID is continuously assigned with a value between 0 and 7 according to the chip address value.

Table 7. Chip ID Assignment Value

Value	Description	Value	Description
b'1xxxxxxx	Chip ID assign 0	b'xxxx1xxx	Chip ID assign 4
b'x1xxxxxx	Chip ID assign 1	b'xxxxx1xx	Chip ID assign 5
b'xx1xxxxx	Chip ID assign 2	b'xxxxxx1x	Chip ID assign 6
b'xxx1xxxx	Chip ID assign 3	b'xxxxxxx1	Chip ID assign 7

Figure 20 shows an example where chip IDs 0 to 7 assigned when the address value is 0xFF for eight PS1120 chips connected in a daisy chain.

See the Chip Assignment section for more information on the Chip Assignment command.

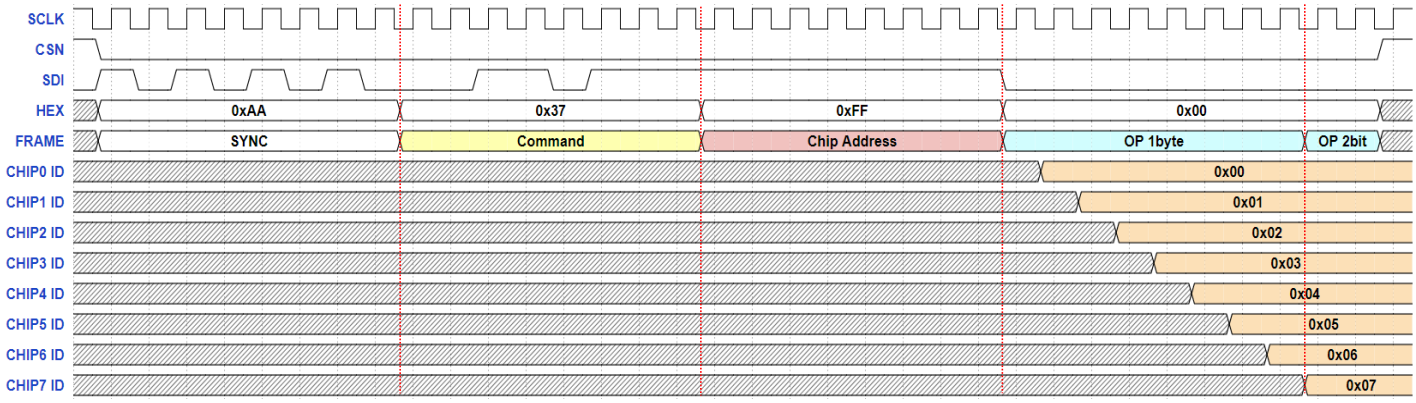


Figure 20. Chip ID Assignment Example

CHIP Select Field

The chip selection field is a data field for selecting one of the multiple PS1120 chips.

As shown in figure 21, the value of the chip select field is 8-bits.

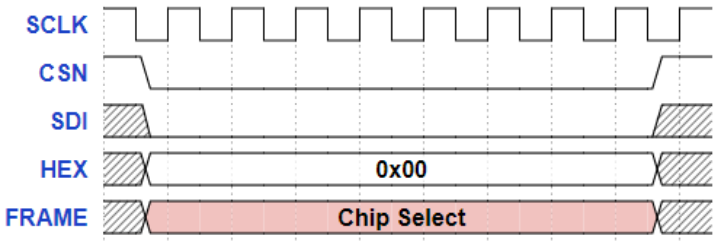


Figure 21. Timing Diagram of Chip Select Field

If eights PS1120 are daisy chained, you can choose one of the PS1120 with chip IDs 0-7 based on the values defined in table 8.

Table 8. Chip Select Value

Value	Description	Value	Description
b’10000000	0th chip Select	b’00001000	4th chip Select
b’01000000	1st chip Select	b’00000100	5th chip Select
b’00100000	2nd chip Select	b’00000010	6th chip Select
b’00010000	3th chip Select	b’00000001	7th chip Select

Special Command Frame

Chip Assignment

Figure 22 shows the command frame for performing all PS1120 chip assignments.

A frame consists of 1-byte sync field, 1-byte command field, and 1-byte op field.

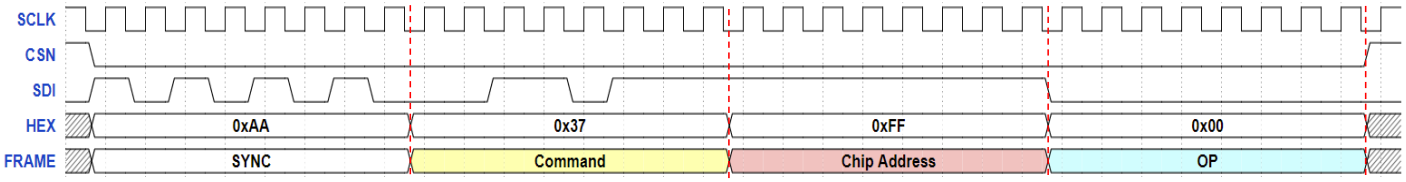


Figure 22. Timing Diagram of Chip Assignment

Looking at the framing, the sync field sends 0xAA, the command field sends 0x37 and chip address field sends 0xFF to execute the chip ID assignment command. Figure 23 shows eight PS1120 daisy-chained. The chip ID 0 ~ 7 assign during the operation (OP) cycle.

The detailed description of the operation is as follows.

1. SCLK and CSN is input to eight PS1120 at the same timing. The SDO output of each PS1120 is the one clock delay value of the SDI.
2. When 0xFF is input as the chip address value and the 1st ID is updated, the first 1 of SDO is changed to 0 and 1st PS1120 is assigned to ID # 0.
3. When 0x7F is input as the chip address value of 2nd PS1120 and the second ID is updated, the first 1 of SDO is changed to 0 and 2nd PS1120 is assigned to ID # 1.
4. When 0x3F is input as the chip address value of 3rd PS1120 and the third ID is updated, the first 1 of SDO is changed to 0 and 3rd PS1120 is assigned to ID # 2.
5. From 4th PS1120 to 8th PS1120 perform as described above from the 4th to 8th update intervals, and then from chip ID #3 to #7 assigned.

Operating (OP) Cycle Field

An operation (OP) cycle is required when executing the PS1120 command. Figure 23 shows eight PS1120 daisy-chained to execute the chip ID assignment command. The chip ID #0 ~ #7 assign during the operation cycle (OP).

Performing the actual chip allocation task and applying the ID value requires a certain amount of work. This is called an operation cycle. From now on, it is called OP cycle.

For example, when executing the chip assignment command for one PS1120, only the 2-bit OP cycle is required after entering the initial chip address field and after that, the actual ID is applied. However, when executing the chip assignment command for eight PS1120, a 9-bit OP cycle is required because the SDI input of each PS1120 delay by one clock cycle when sent to the next chip.

As shown in figure 23, from chip ID #0 of PS1120 to chip ID #6 of PS1120 are assigned IDs within a 1-byte OP cycle. But in the case of chip ID #7 of PS1120, ID is assigned at the 9th clock edge of the OP cycle.

If it is a daisy chain or not, refer to Appendix B for details on the command operation cycle time other than the chip assignment command.

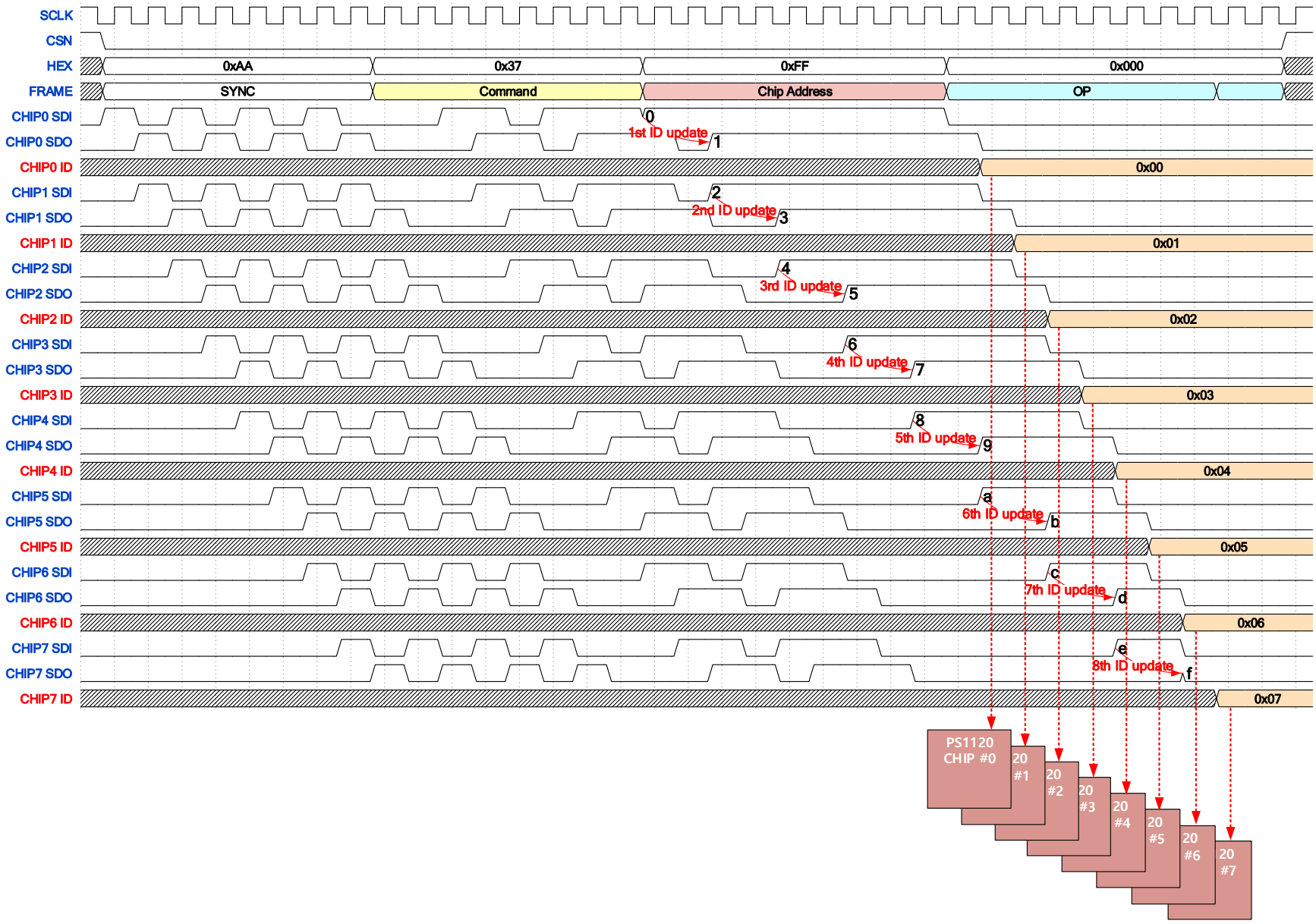


Figure 23. Assignment CHIP ID 0~7 of eight PS1120

Pattern Reset

Figure 24 shows an example of pattern reset. A frame consists of 19-byte data field and 2-byte op field.

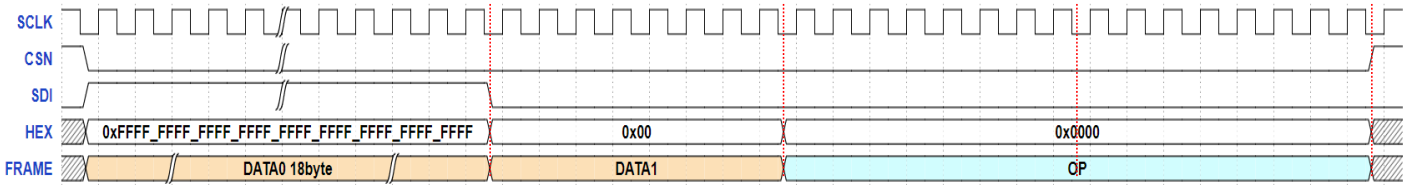


Figure 24. Timing Diagram of Pattern Reset

Table 9 shows the initialization value information when executing pattern reset.

Table 9. Operation of Initialization Commands

Command	ON-OFF States	HOLD Flags	Logic Control Register
PATTERN_RESET	OFF	CLEARED	Initial default value of all

Executing the pattern reset, initializes all values such as chip ID, switch status and registers.

To re-execute the command after the pattern reset, after executing the chip initial command, a chip assignment command shall be executing to reassign the chip ID of each PS1120.

All Chip Active Discharge Disable (Default)

Figure 25 shows an example of active discharge disable for all PS1120.

A frame consists of 1-byte synchronization field, 1-byte command field and 1-byte op field.

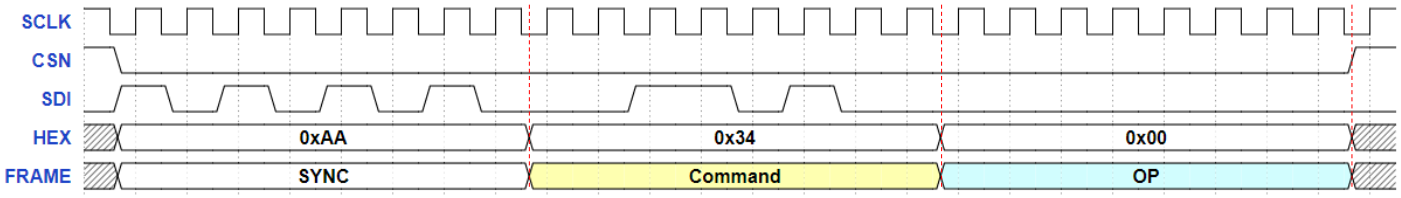


Figure 25. Timing Diagram of All Chip Active Discharge Disable

Select Chip Active Discharge Disable (Default)

Figure 26 shows an example of active discharge disable for selected PS1120.

A frame consists of 1-byte synchronization field, 1-byte command field, 1-byte chip select field and 1-byte op field.

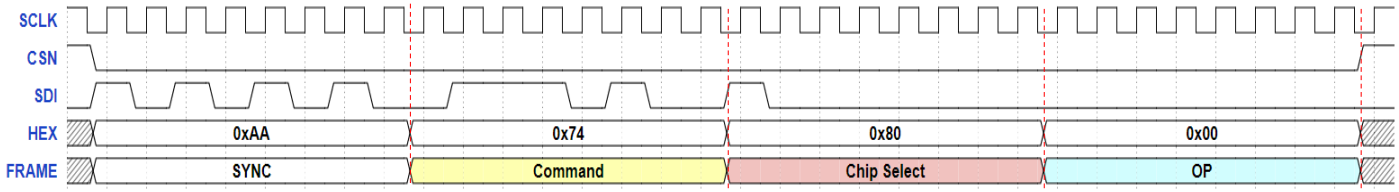


Figure 26. Timing Diagram of Select Chip Active Discharge Disable

All Chip Active Discharge Enable

Figure 27 shows an example of active discharge enable for all PS1120.

A frame consists of 1-byte synchronization field, 1-byte command field and 1-byte op field.

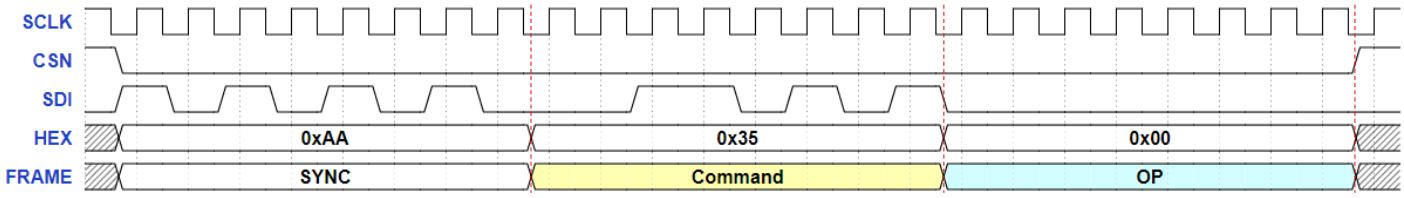


Figure 27. Timing Diagram of All Chip Active Discharge Enable

Select Chip Active Discharge Enable

Figure 28 shows an example of active discharge enable for selected PS1120.

A frame consists of 1-byte synchronization field, 1-byte command field, 1-byte chip select field and 1-byte op field.

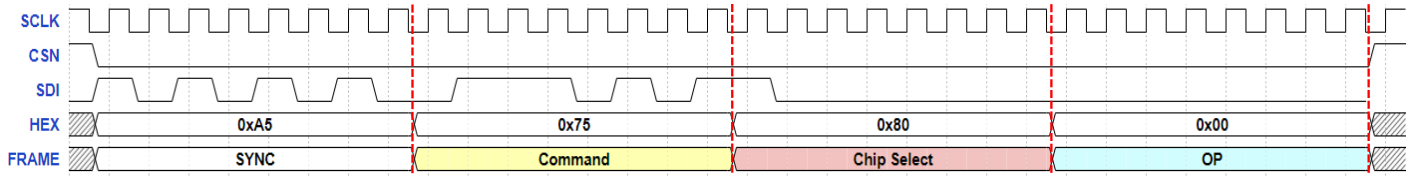


Figure 28. Timing Diagram of Select Chip Active Discharge Enable

User Command Frame

The user command frame indicates the type of command the user can use to operate the PS1120's switch.

Switch Operation of Common Command

- All Chip Operation

■ *Turn on of the all switch of all chip*

Figure 29 shows a command frame that turns on all switches on all PS1120.

Frame consists of 1-byte sync field, 1-byte command field and 2-byte op field.

In the command frame, 0x01 is input, and the ON command execute for all switches of all PS1120.

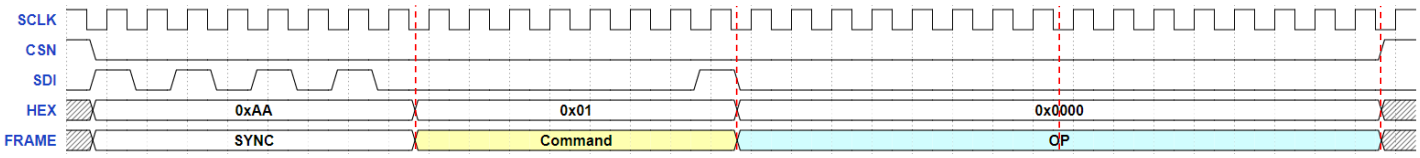


Figure 29. Timing Diagram of ALL_ON of All Chip

Figure 30 shows the result of executing the command in figure 29.

This shows that the status of all eight PS1120 switches change from OFF to ON.

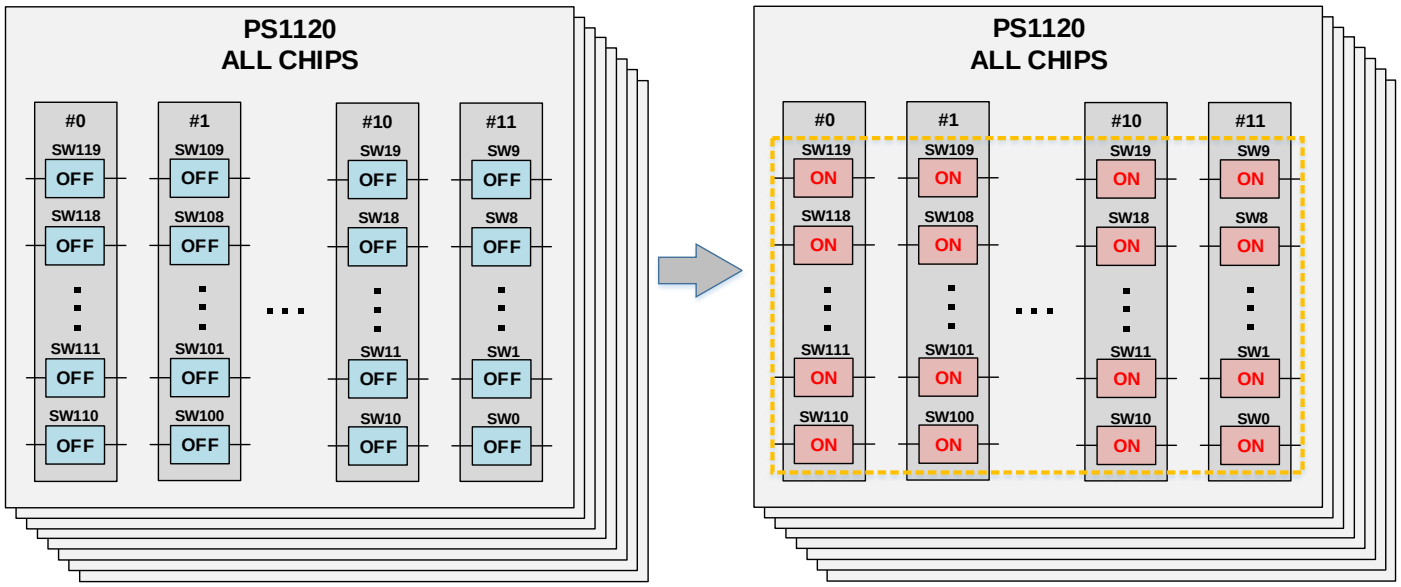


Figure 30. Switch Operation of ALL_ON of All Chip

- ***Turn on of the one switch of all chip***

Figure 31 shows a command frame that turns on selected one switch on all PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 1-byte switch number field and 1-byte op field.

The Switch Number field can have 0x00 to 0x77, and this value represents switch number 0 to 119 of PS1120.

In the command frame, 0x09 is input, and the ON command execute for selected one switch of all PS1120.

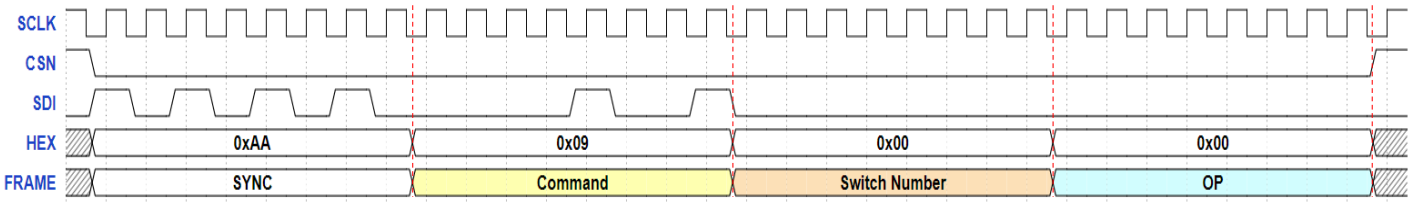


Figure 31. Timing Diagram of ONE_SW_ON of All Chip

Figure 32 shows the result of executing the command in figure 31.

This shows that the status of the selected 0th switch of the eight PS1120 change from OFF to ON.

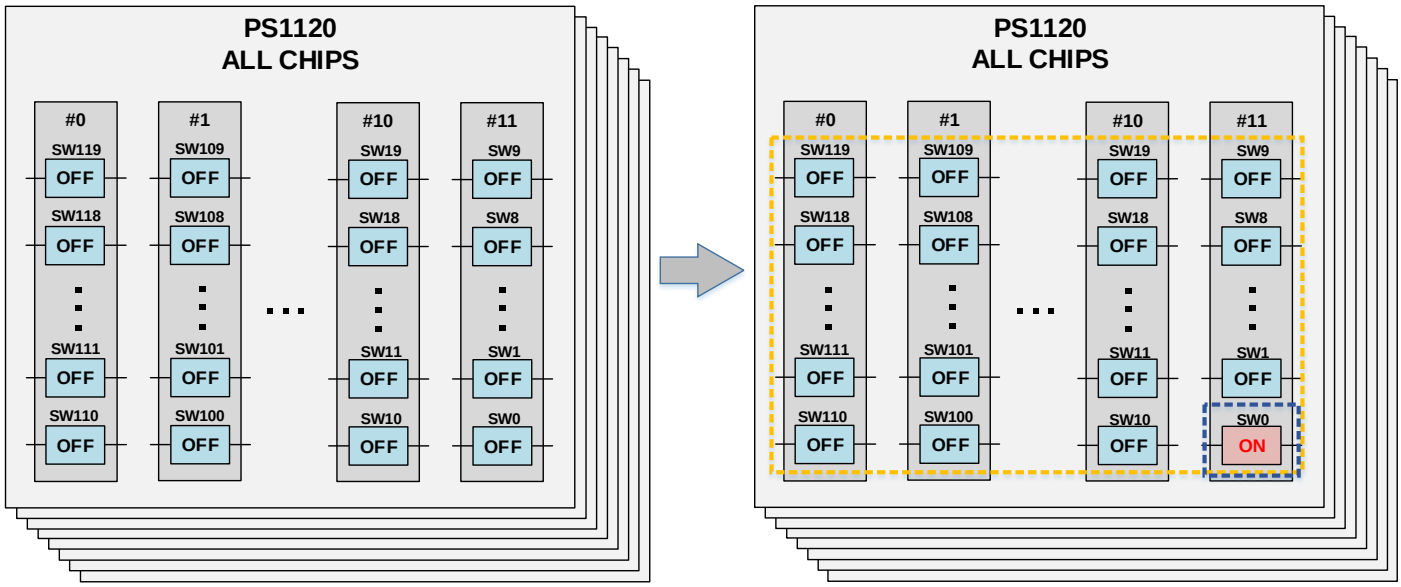


Figure 32. Switch Operation of ONE_SW_ON of All Chip

- ***Turn on of the switch position of all chip***

Figure 33 shows a command frame that turns on selected switch positions on all PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 120-bit switch position and 1-byte op field.

The Switch Position frame uses values corresponding to each bit in the order of MSB to LSB from switch 0 to switch 119.

In the Command frame, 0x39 is input, and the ON command execute for selected switch positions of all PS1120.

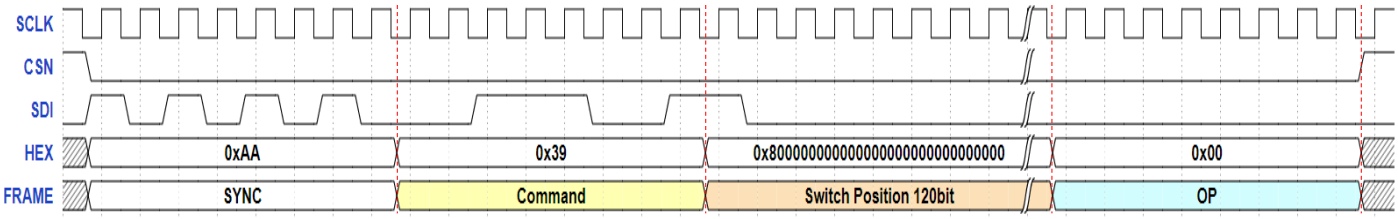


Figure 33. Timing Diagram of SW_POS_ON of All Chip

Figure 34 shows the result of executing the command in figure 33.

This shows that the status of the selected 0th switch position of the eight PS1120 change from OFF to ON.

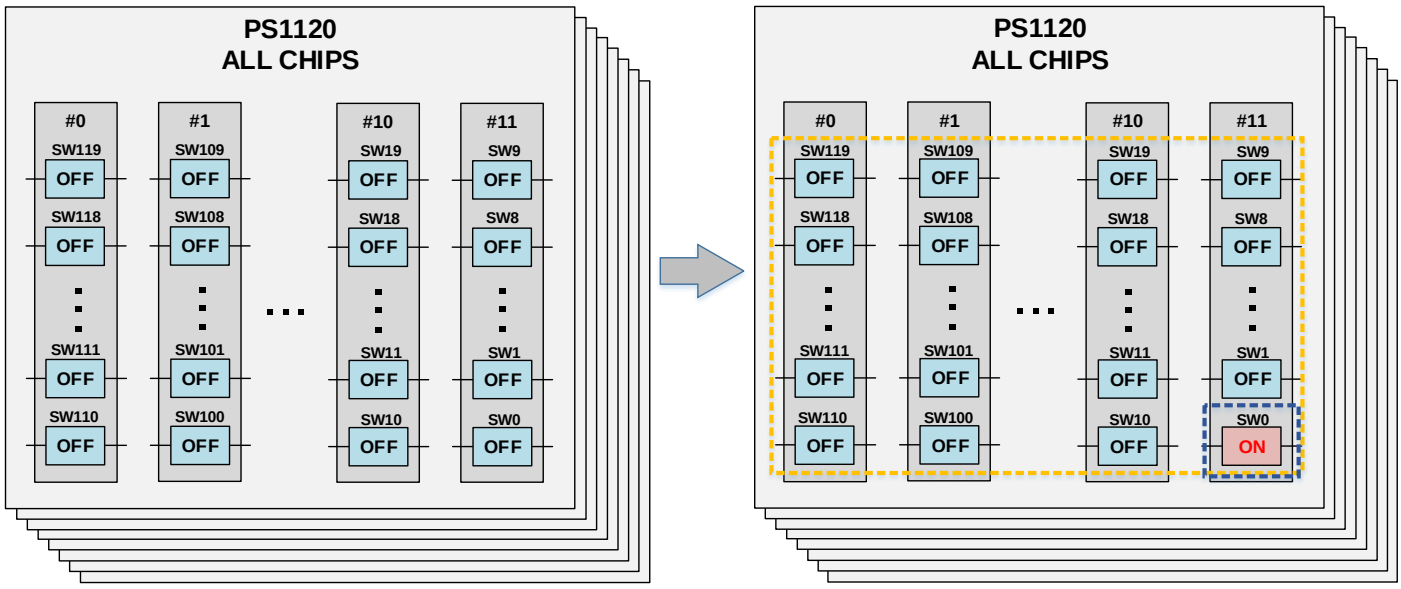


Figure 34. Switch Operation of SW_POS_ON of All Chip

- **Selected Chip Operation**

  - ***Turn on of the all switch of selected chip***

Figure 35 shows a command frame that turns on all switches on selected PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 1-byte chip select field and 2-byte op field.

In the Command frame, 0x41 is input, and the ON command execute for all switches of selected PS1120.

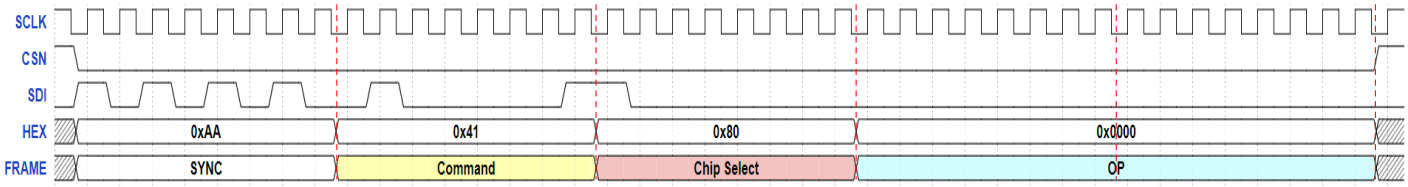


Figure 35. Timing Diagram of ALL_ON of Select Chip

Figure 36 shows the result of executing the command in figure 35.

This shows that the state of all switches on the selected PS1120 #0 change from OFF to ON and the switches of PS1120 #1 to PS1120 #7 remain in the previous state without being affected by the command.

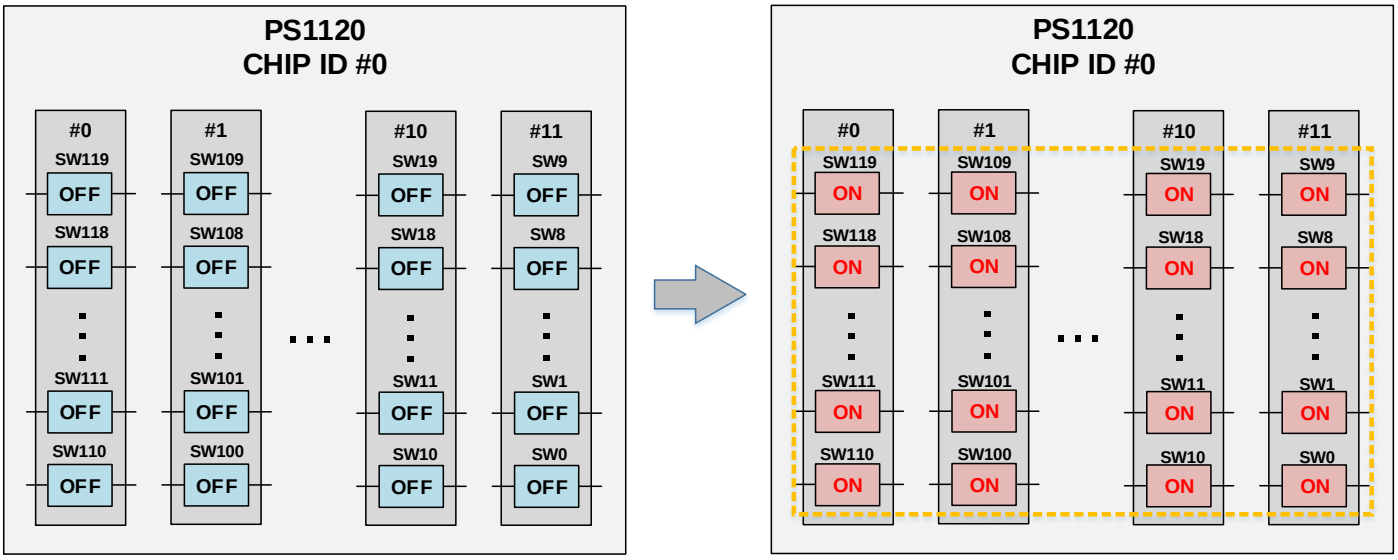


Figure 36. Switch Operation of ALL_ON of Select Chips

■ ***Turn on of the one switch of selected chip***

Figure 37 shows a command frame that turns on selected one switch on selected PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 1-byte chip select field, 1-byte switch number field and 1-byte op field.

The Switch Number field can have 0x00 to 0x77, and this value represents switch number 0 to 119 of PS1120.

In the Command frame, 0x49 is input, and the ON command execute for selected one switch of selected PS1120.

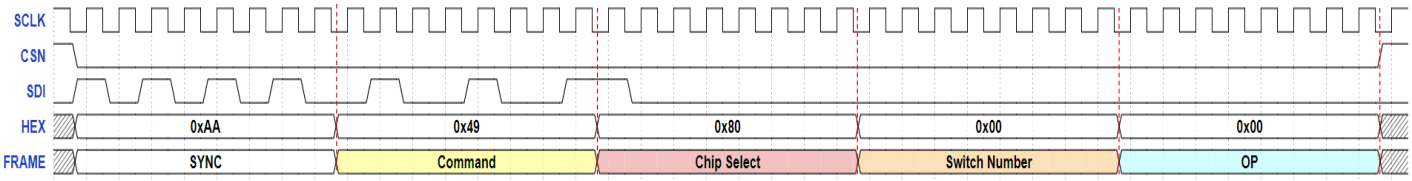


Figure 37. Timing Diagram of ONE_SW_ON of Select Chip

Figure 38 shows the result of executing the command in figure 37.

This shows that the status of the selected 0th switch of the selected PS1120 #0 change from OFF to ON and the switches of PS1120 #1 to PS1120 #7 remain in the previous state without being affected by the command.

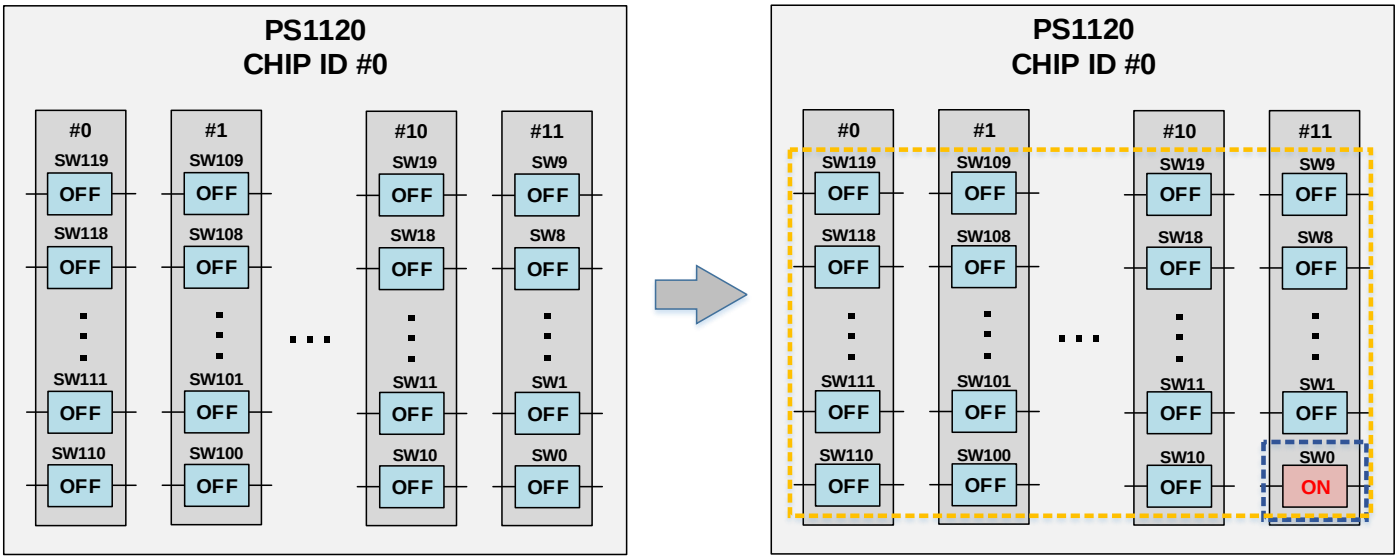


Figure 38. Switch Operation of ONE_SW_ON of Select Chip

- ***Turn on of the switch position of selected chip***

Figure 39 shows a command frame that turns on selected switch positions on selected PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 1-byte chip select field, 120-bit switch position and 1-byte op field.

The Switch Position frame uses values corresponding to each bit in the order of MSB to LSB from switch 0 to switch 119.

In the Command frame, 0x79 is input, and the ON command execute for selected switch positions of selected PS1120.

Switch position

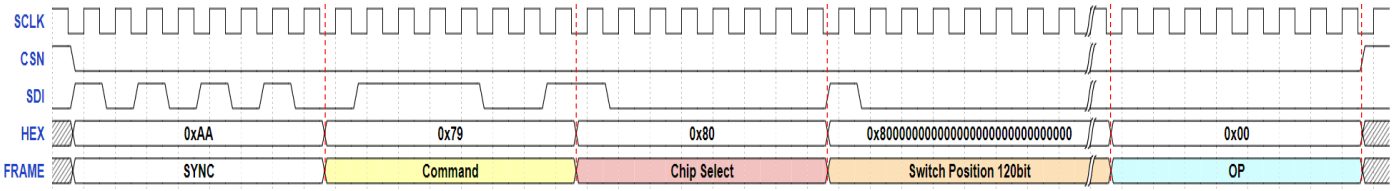


Figure 39. Timing Diagram of SW_POS_ON of Select Chip

Figure 40 shows the result of executing the command in figure 39.

This shows that the status of the selected 0th switch position of the selected PS1120 #0 change from OFF to ON and the switches of PS1120 #1 to PS1120 #7 remain in the previous state without being affected by the command.

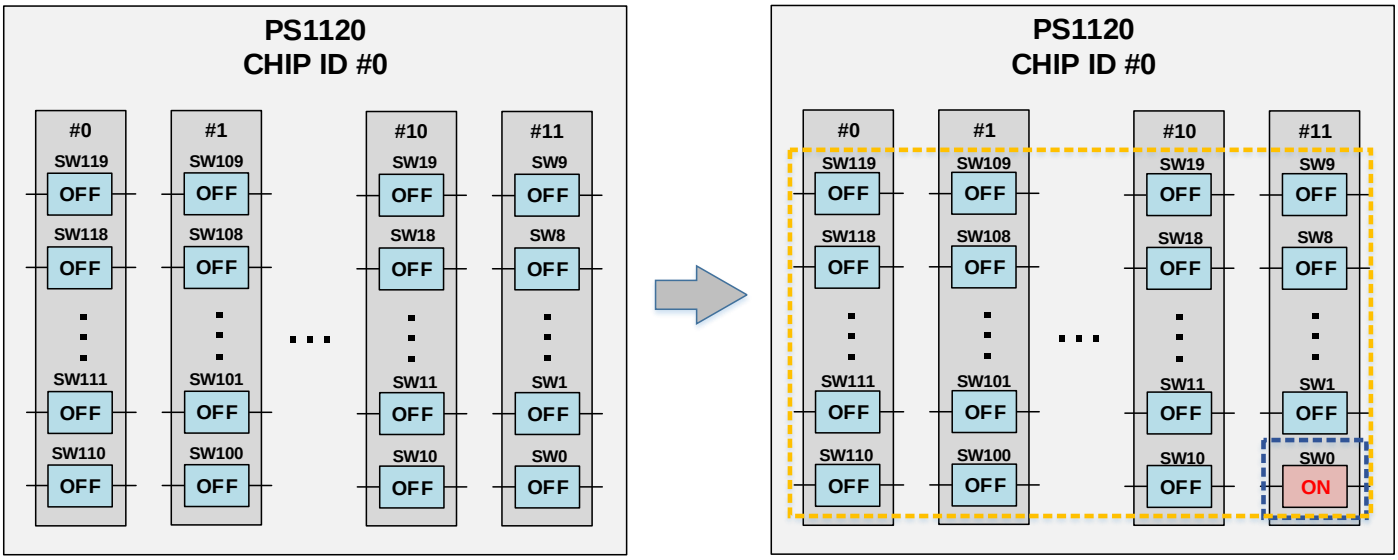


Figure 40. Switch Operation of SW_POS_ON of Select Chips

Switch Operation of Row or Column Command

- **All Chip Operation**

  - ***Turn on of the all switch of selected rows of all chip***

Figure 41 shows a command frame that turns on all switches in the selected row for all PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 10-bit row field and 14-bit op field.

In the Command frame, 0x11 is input, and the ON command execute for all switches in the selected row of all PS1120.

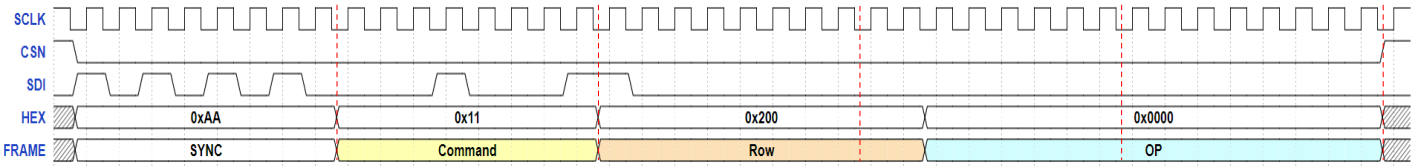


Figure 41. Timing Diagram of SEL_ROW_ON of All Chip

Figure 42 shows the result of executing the command in figure 41.

The row value is 10-bit 0x200.

This shows that the status of all switches in the first row of all PS1120 change from OFF to ON.

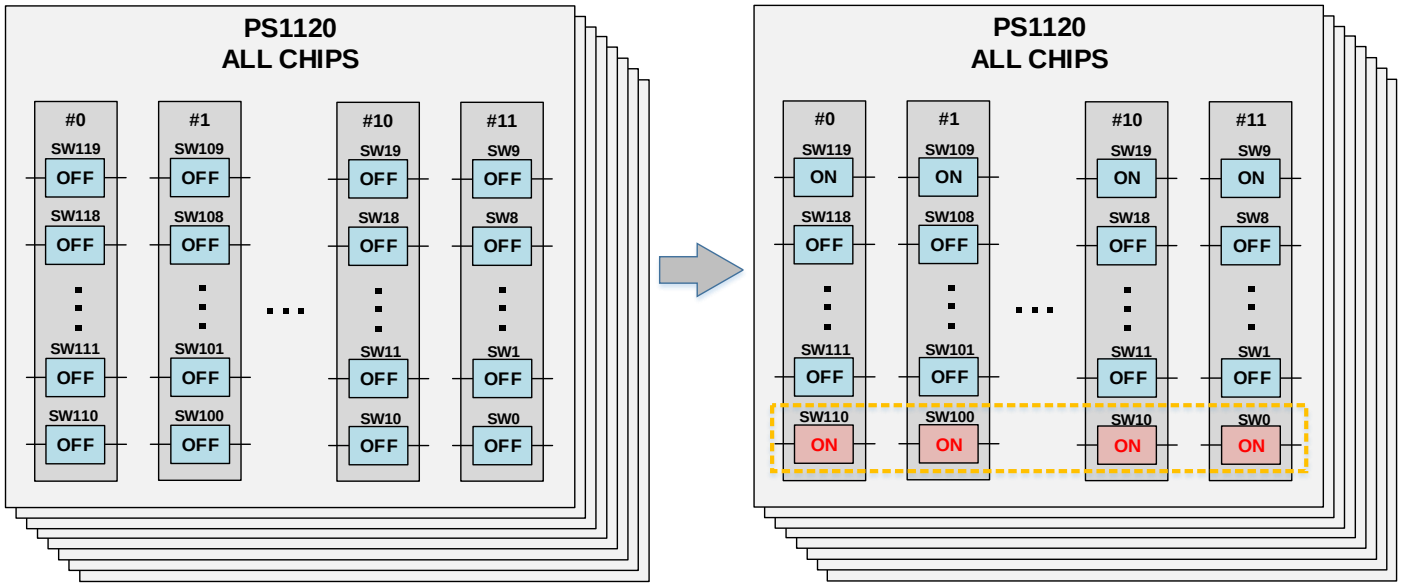


Figure 42. Switch Operation of SEL_ROW_ON of All Chip

- ***Turn on of the all switch of selected columns of all chip***

Figure 43 shows the command frame that switches on all the switches in the selected column for all PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 12-bit column field and 12-bit op field.

In the Command frame, 0x21 is input, and the ON command execute for all switches in the selected column of all PS1120.

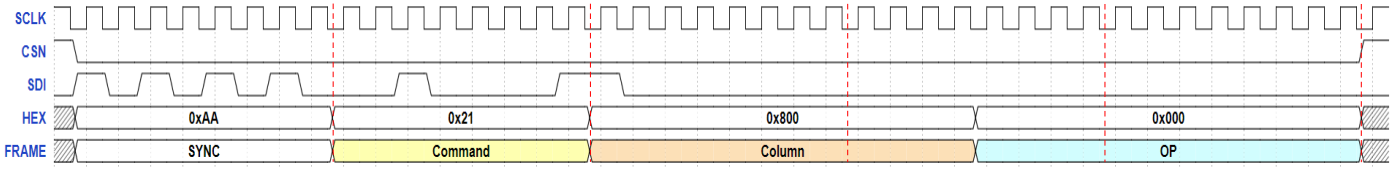


Figure 43. Timing Diagram of SEL_COL_ON of All Chip

Figure 44 shows the result of executing the command in figure 43.

The column value is 12-bit 0x800.

This shows that the status of all switches in the first column of all PS1120 change from OFF to ON.

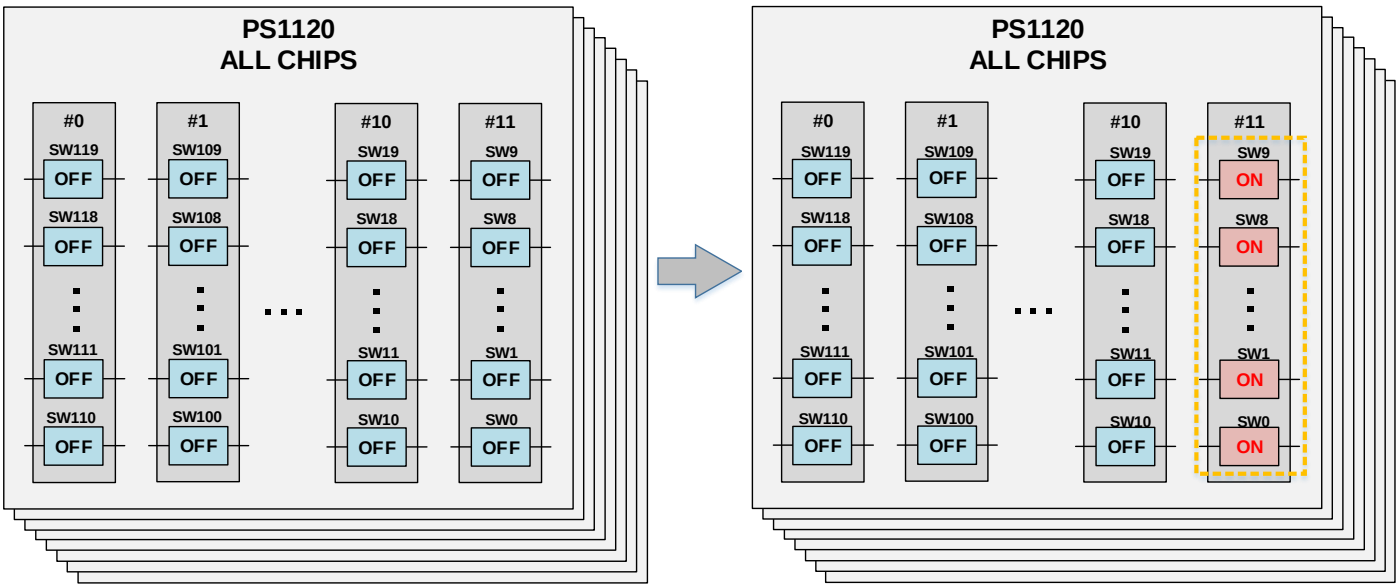


Figure 44. Switch Operation of SEL_COL_ON of All Chip

- ***Turn on of the selected switch of the selected row of all chip***

Figure 45 shows a command frame that turns on the selected switch among the selected row for all PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 10-bit row field, 12-bit switch in row field and 10-bit op field.

In the Command frame, 0x19 is input, and the ON command execute for the selected switch from the selected rows for all PS1120.

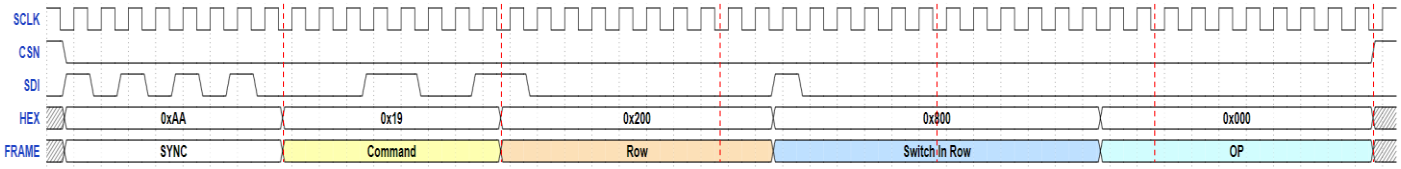


Figure 45. Timing Diagram of SEL_ROW_SEL_SW_IN_ROW_ON of All Chip

Figure 46 shows the result of executing the command in figure 45.

The row value is 10-bit 0x200 and switch in row value is 12-bit 0x800.

This shows that the status of the first switch in the first row of the all PS1120 change from OFF to ON.

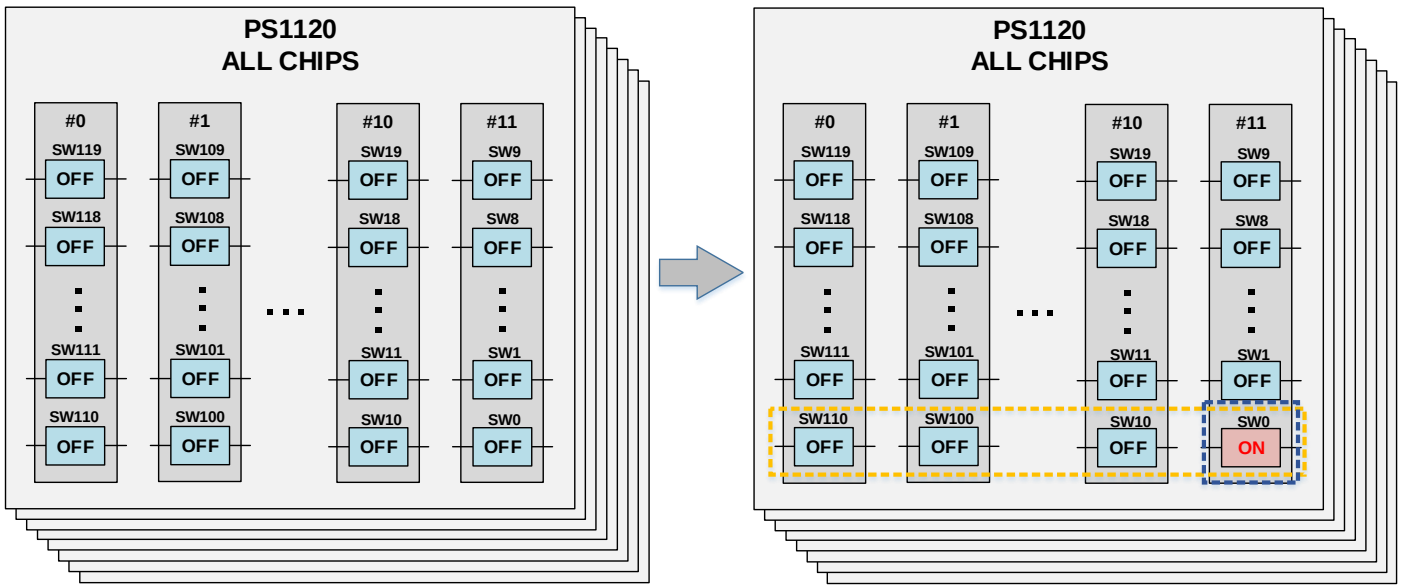


Figure 46. Switch Operation of SEL_ROW_SEL_SW_IN_ROW_ON of All Chip

- ***Turn on of the selected switch of the selected column of all chip***

Figure 47 shows a command frame that turns on the selected switch among the selected column for all PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 12-bit column field, 10-bit switch in column field and 10-bit op field.

In the Command frame, 0x29 is input, and the ON command execute for the selected switch from the selected columns for all PS1120.

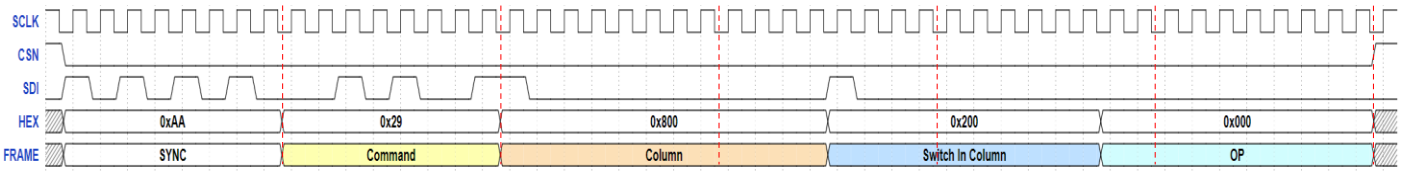


Figure 47. Timing Diagram of SEL_COL_SEL_SW_IN_COL_ON of All Chip

Figure 48 shows the result of executing the command in figure 47.

The column value is 12-bit 0x800 and switch in column value is 10-bit 0x200.

This shows that the status of the first switch in the first column of the all PS1120 change from OFF to ON.

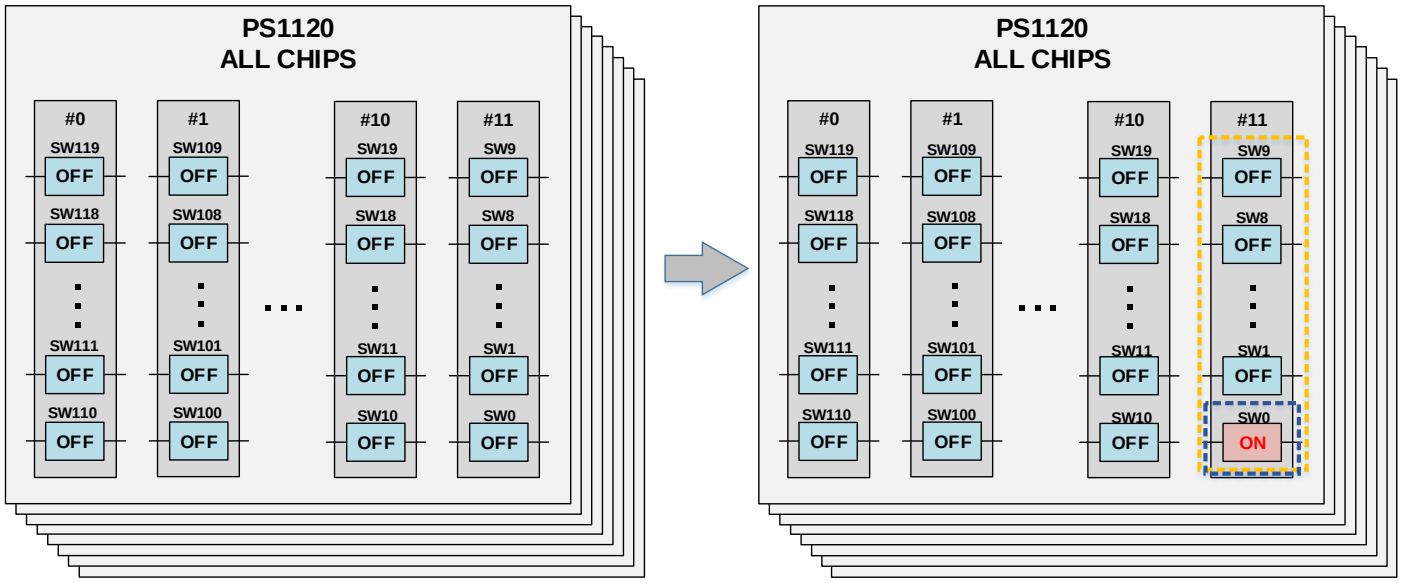


Figure 48. Switch Operation of SEL_COL_SEL_SW_IN_COL_ON of All Chip

- **Selected Chip Operation**

  - ***Turn on of the all switch of selected rows of selected chip***

Figure 49 shows a command frame that turns on all switches in the selected row for selected PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 1-byte chip select field, 10-bit row field and 14-bit op field.

In the Command frame, 0x51 is input, and the ON command execute for all switches in the selected row of selected PS1120.

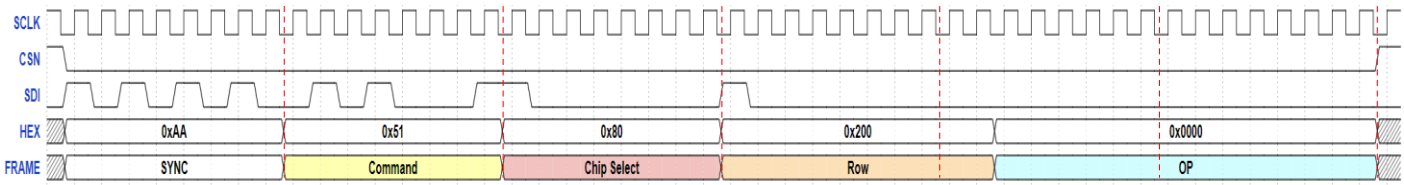


Figure 49. Timing Diagram of SEL_ROW_ON of Select Chip

Figure 50 shows the result of executing the command in figure 49.

The row value is 10-bit 0x200 and chip select value is 8-bit 0x80.

This shows that the status of all switches in the first row of selected PS1120 #0 change from OFF to ON and the switches of PS1120 # 1 to PS1120 # 7 remain in the previous state without being affected by the command.

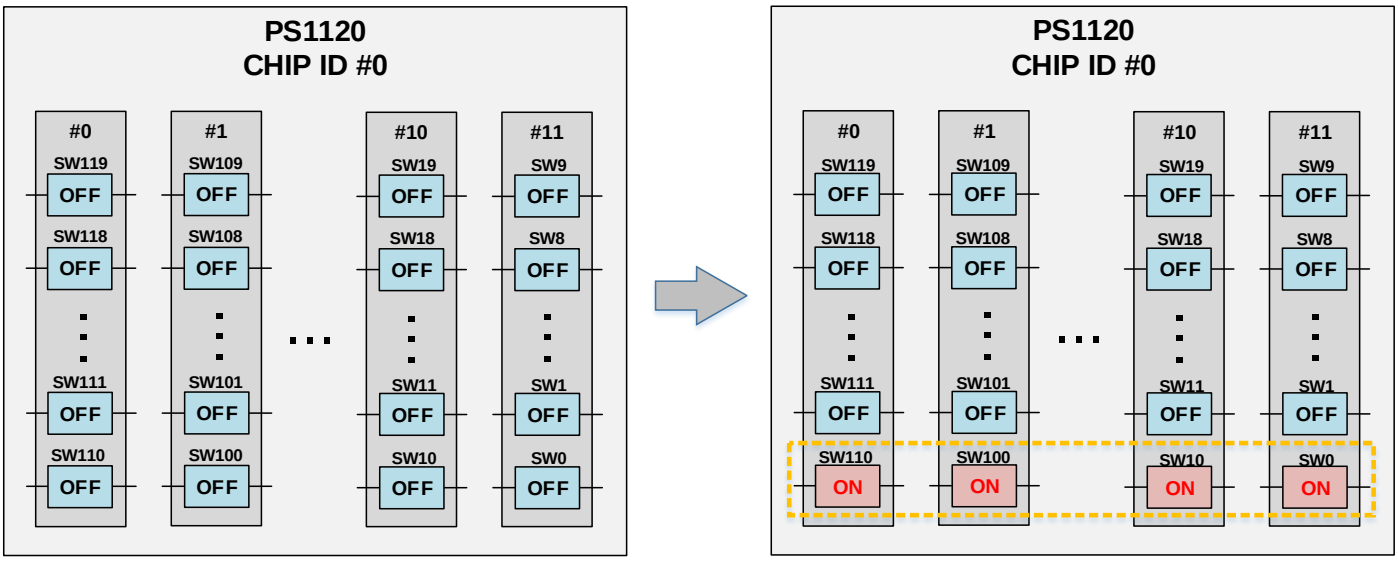


Figure 50. Switch Operation of SEL_ROW_ON of Select Chip

- ***Turn on of the all switch of selected columns of selected chip***

Figure 51 shows the command frame that switches on all the switches in the selected column for selected PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 1-byte chip select field, 12-bit column field and 12-bit op field.

In the Command frame, 0x61 is input, and the ON command execute for all switches in the selected column of selected PS1120.

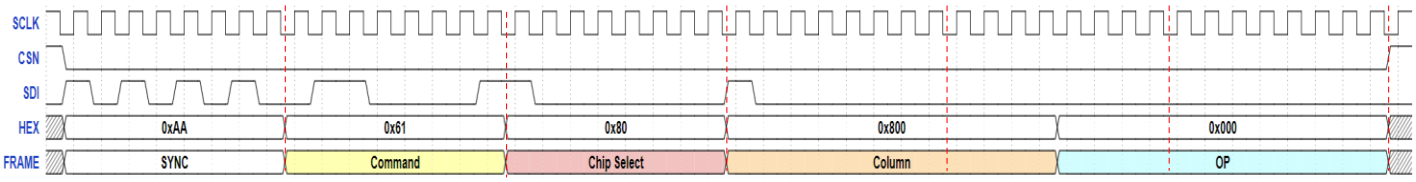


Figure 51. Timing Diagram of SEL_COL_ON of Select Chip

Figure 52 shows the result of executing the command in figure 51.

The chip select value is 8-bit 0x80 and column value is 12-bit 0x800.

This shows that the status of all switches in the first column of selected PS1120 #0 change from OFF to ON and the switches of PS1120 #1 to PS1120 #7 remain in the previous state without being affected by the command.

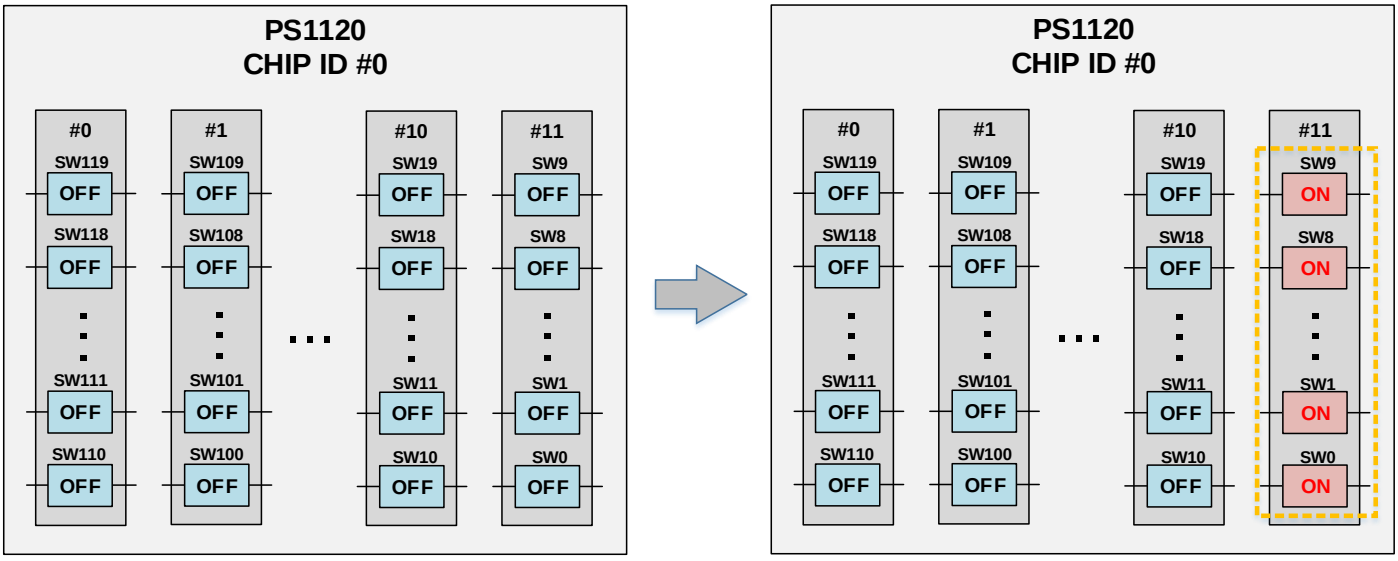


Figure 52. Switch Operation of SEL_COL_ON of Select Chip

- ***Turn on of the selected switch of the selected row of selected chip***

Figure 53 shows a command frame that turns on the selected switch among the selected row for selected PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 1-byte chip select field, 10-bit row field, 12-bit switch in row field and 10-bit op field.

In the Command frame, 0x59 is input, and the ON command execute for the selected switch from the selected rows for selected PS1120.

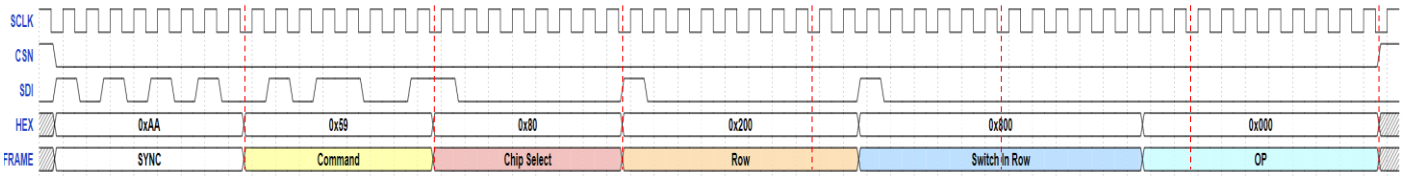


Figure 53. Timing Diagram of SEL_ROW_SEL_SW_IN_ROW_ON of Select Chip

Figure 54 shows the result of executing the command in figure 53.

The chip select value is 8-bit 0x80, row value is 10-bit 0x200 and switch in row value is 12-bit 0x800.

This shows that the status of the first switch in the first row of the selected PS1120 #0 change from OFF to ON and the switches of PS1120 #1 to PS1120 #7 remain in the previous state without being affected by the command.

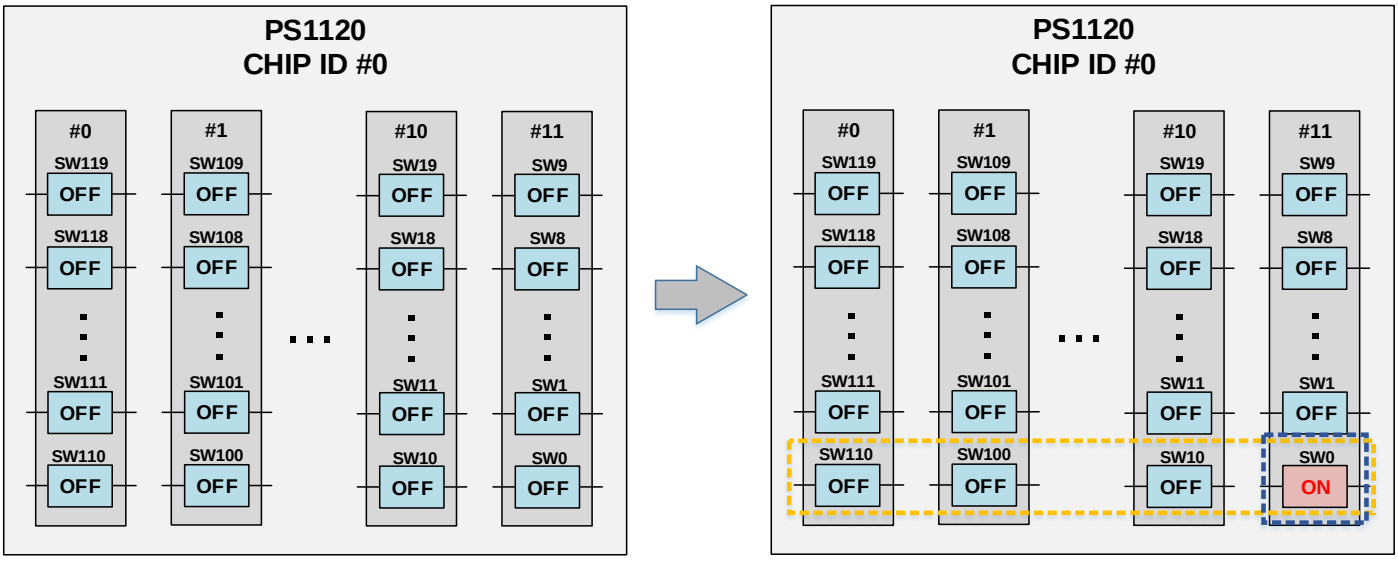


Figure 54. Switch Operation of SEL_ROW_SEL_SW_IN_ROW_ON of Select Chip

- ***Turn on of the selected switch of the selected column of selected chips***

Figure 55 shows a command frame that turns on the selected switch among the selected column for selected PS1120.

Frame consists of 1-byte sync field, 1-byte command field, 1-byte chip select field, 12-bit column field, 10-bit switch in column field and 10-bit op field.

In the Command frame, 0x69 is input, and the ON command execute for the selected switch from the selected columns for selected PS1120.

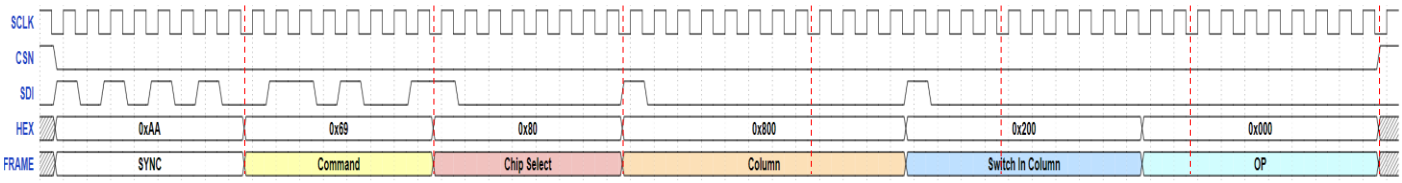


Figure 55. Timing Diagram of SEL_COL_SEL_SW_IN_COL_ON of Select Chip

Figure 56 shows the result of executing the command in figure 55.

The chip select value is 8-bit 0x80, column value is 12-bit 0x800 and switch in column value is 10-bit 0x200.

This shows that the status of the first switch in the first column of the selected PS1120 #0 change from OFF to ON and the switches of PS1120 #1 to PS1120 #7 remain in the previous state without being affected by the command.

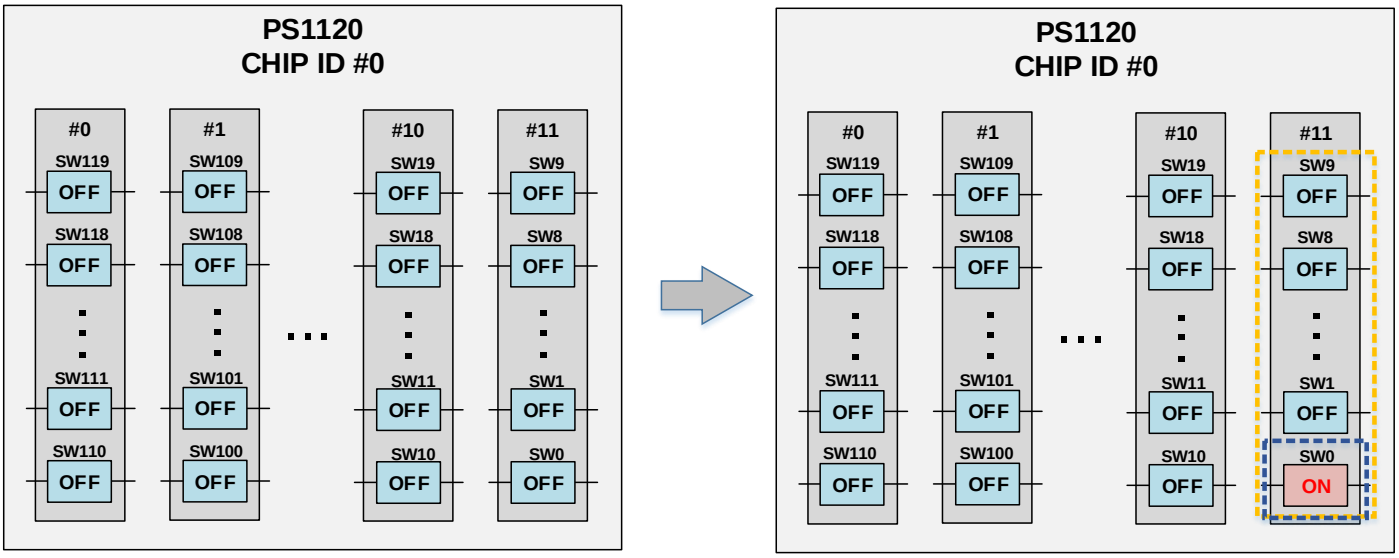
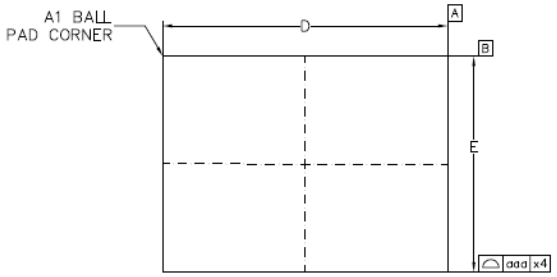


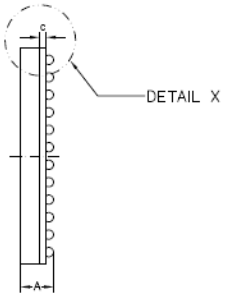
Figure 56. Switch Operation of SEL_COL_SEL_SW_IN_COL_ON of Select Chip

PACKAGE INFORMATION (DEMENSION)

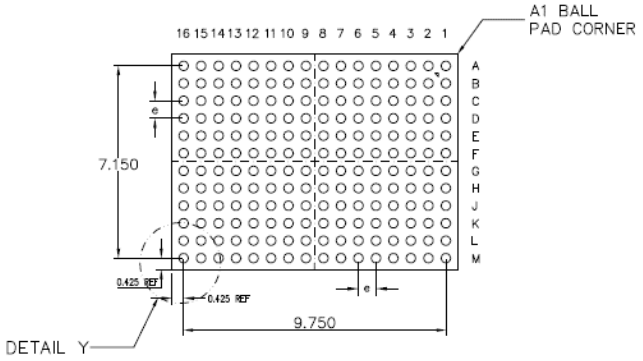
REV.	DESCRIPTION	DATE	ENG	APPROVAL
–	GENERATE	02/20/'20	TS KIM	
A	CHANGE THE "c" VALUE 0.26 TO 0.25	03/31/'20	TS KIM	



TOP VIEW

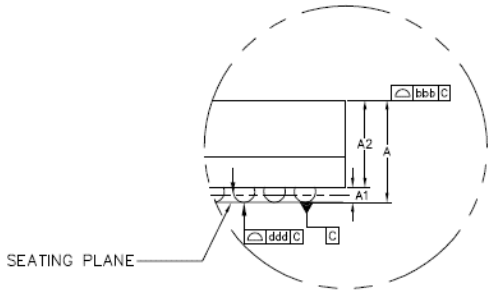


SIDE VIEW

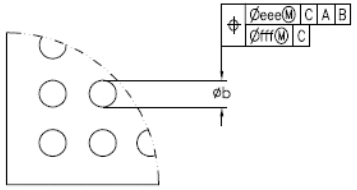


BOTTOM VIEW

SYMBOL	MIN.	NOM.	MAX.
A	1.09	1.22	1.35
A1	0.22	0.27	0.32
A2	0.87	0.95	1.03
D	10.50	10.60	10.70
E	7.90	8.00	8.10
M	16x12 <FULL>		
aaa			0.15
bbb			0.10
ddd			0.10
eee			0.15
fff			0.08
øb	0.30	0.35	0.40
e	0.65 REF.		
c	0.25 REF.		
Raw ball size	ø0.35		



DETAIL X



DETAIL Y

NOTES:
1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M–1994.
2. COMPLIANT TO JEDEC REGISTERED OUTLINE DR–4.5, NO EXACT VARIATION AND WITH EXCEPTION TO DIA "A"
3. APPLY THE SPECIFIC CUSTOMER'S PKG TOTAL THICKNESS
4. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE.
5. A1 CORNER MUST BE IDENTIFIED BY INK OR LASER MARK.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: N/S	DATE: 02/20/'20	DRAWN: TS KIM	TITLE: FCFBGA 10.6X8.0MM 192 BALL 0.65MM BALL PITCH PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: TS KIM	
PROJECTION UNLESS SPECIFIED	FRAC: .X ±0.10, .XX ±0.05, .XXX ±0.03, ANGLE ± 1°	CHECKED: TH LEE	
		APPROVED: BS CHOI	
	CAD NAME: OCB–10601	DRAWING NUMBER: OCB–10601	REV. A, SHEET: 1 OF 1

APPLICATION EXAMPLE

IC and Package Information

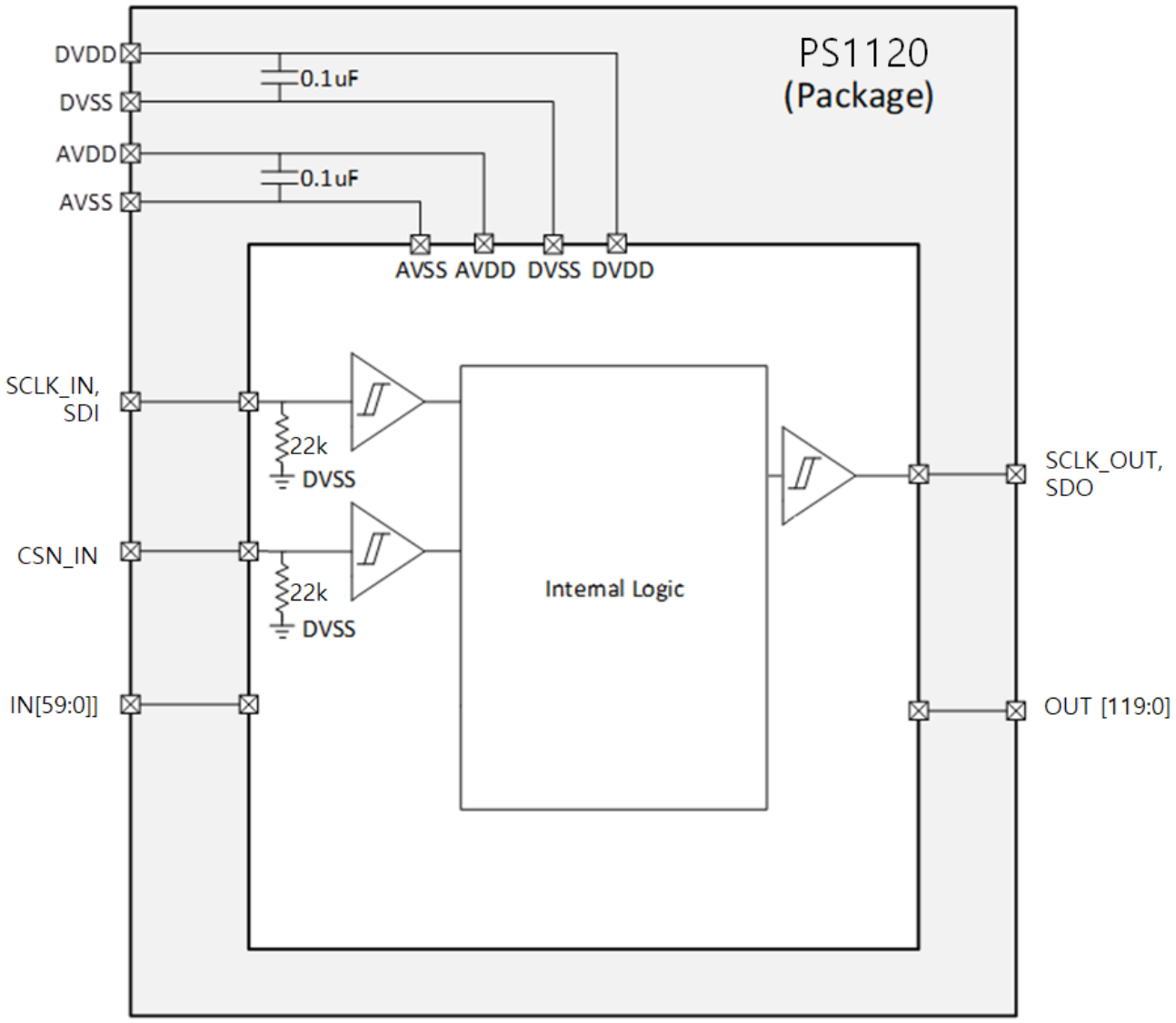


Figure 57. IC and package internal information

PS1120 includes all the passive components required for more stable operation. All the bypass capacitors, between AVDD and AVSS and between DVDD and DVSS, are embedded in the package. If necessary, additional bypass capacitors can be added. All the pull-down resistors are included in the input I/O block of the IC.

REVISION HISTORY

Revision	Date	Description
0.0	2020-02	Initial draft
0.1	2020-06	Select chip active discharge enable frame modify Digital SPI interface timing modify Switch block diagram and operation diagram modify APPENDIX C modify Electrical characteristics addition
0.2	2020-08	Digital command description modify Added by ELECTRICAL CHARACTERISTICS for each power source Added by TEST RESULTS Graph
0.3	2020-10	Added by Application Example

DOCUMENT INFORMATION

Document name: PS1120 Datasheet
Product code: PS1120
Product description: Multi-channel Switch IC
Document revision: 0.3

The world is driven by analog

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Phone: 82-2-581-5510
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APPENDIX A

120CH Switch MAP

		Column											
		[0]	**[1]**	**[2]**	**[3]**	**[4]**	**[5]**	**[6]**	**[7]**	**[8]**	**[9]**	**[10]**	**[11]**
Row	**[0]**	119	109	99	89	79	69	59	49	39	29	19	9
	[1]	118	108	98	88	78	68	58	48	38	28	18	8
	[2]	117	107	97	87	77	67	57	47	37	27	17	7
	[3]	116	106	96	86	76	66	56	46	36	26	16	6
	[4]	115	105	95	85	75	65	55	45	35	25	15	5
	[5]	114	104	94	84	74	64	54	44	34	24	14	4
	[6]	113	103	93	83	73	63	53	43	33	23	13	3
	[7]	112	102	92	82	72	62	52	42	32	22	12	2
	[8]	111	101	91	81	71	61	51	41	31	21	11	1
	[9]	110	100	90	80	70	60	50	40	30	20	10	0

APPENDIX B

CMD Operating Cycle (@10MHz, 100ns)

Value	Frame	1-Chip OP Cycle		8-Chip Chain OP Cycle(*)	
		Byte	Time(us)	Byte	Time(us)
CMD : 0000_0xxx	Operate all switches on all chip	4	3.2	4	3.2
CMD : 0000_1xxx	Operate only one switch on all chip	4	3.2	5	4.0
CMD : 0001_0xxx	Operate all switches of the selected row on all chip	5	4.0	5	4.0
CMD : 0001_1xxx	Operate only the selected switches in the selected row on all chip	6	4.8	7	5.6
CMD : 0010_0xxx	Operate all switches of the selected column on all chip	5	4.0	6	4.8
CMD : 0010_1xxx	Operate only the selected switches in selected column all chip	6	4.8	7	5.6
CMD : 0011_1xxx	Operate only the selected switches on all chip	18	144.0	19	152.0
CMD : 0100_0xxx	Operate all switches on selected chip	5	4.0	5	4.0
CMD : 0100_1xxx	Operate only one switch on selected chip	5	4.0	6	4.8
CMD : 0101_0xxx	Operate all switches of the selected row on selected chip	6	4.8	6	4.8
CMD : 0101_1xxx	Operate only the selected switches in the selected row on selected chip	7	5.6	8	6.4
CMD : 0110_0xxx	Operate all switches of the selected column on selected chip	6	4.8	7	5.6
CMD : 0110_1xxx	Operate only the selected switches in the selected column on selected chip	7	5.6	8	6.4
CMD : 0111_1xxx	Operate only the selected switches on selected chip	19	152.0	20	160.0
CMD : 0011_0111	Chip Address Assignment	4	3.2	5	4.0
CMD : 0011_0100	All Chip Active Discharge Disable	3	2.4	4	3.2
CMD : 0111_0100	Select Chip Active Discharge Disable	4	3.2	5	4.0
CMD : 0011_0101	All Chip Active Discharge Enable	3	2.4	4	3.2
CMD : 0111_0101	Select Chip Active Discharge Enable	4	3.2	5	4.0

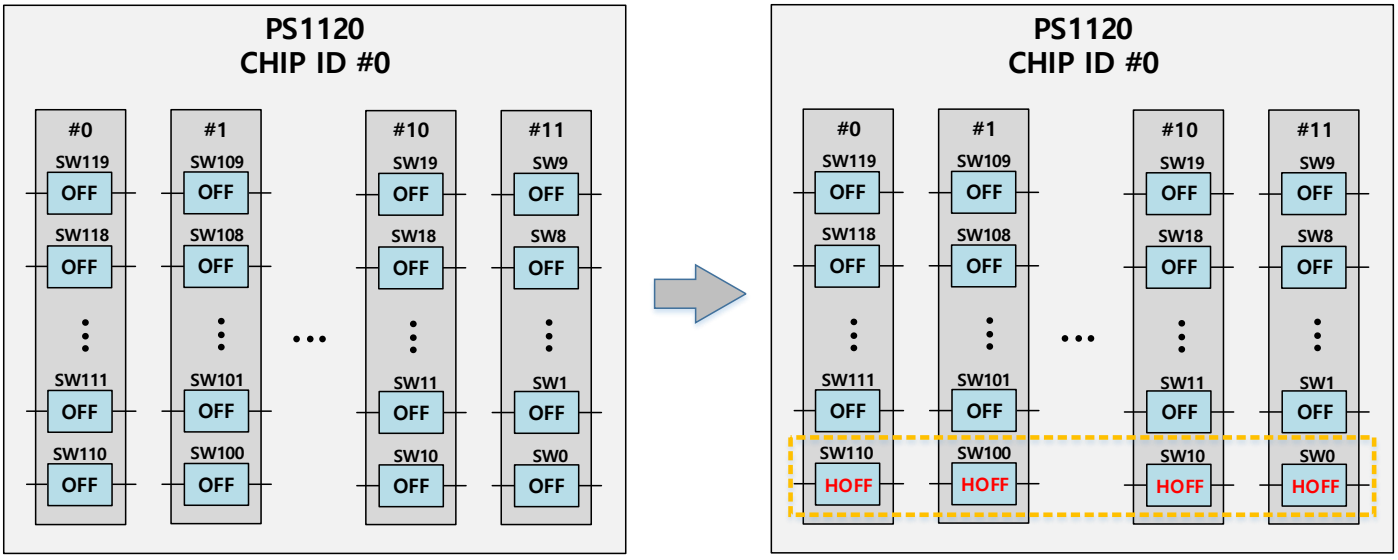
- 1 Byte is 8-CLK operation time.
- (*) The OP cycle of daisy chain is the end of the last chip's instruction execution time.

APPENDIX C

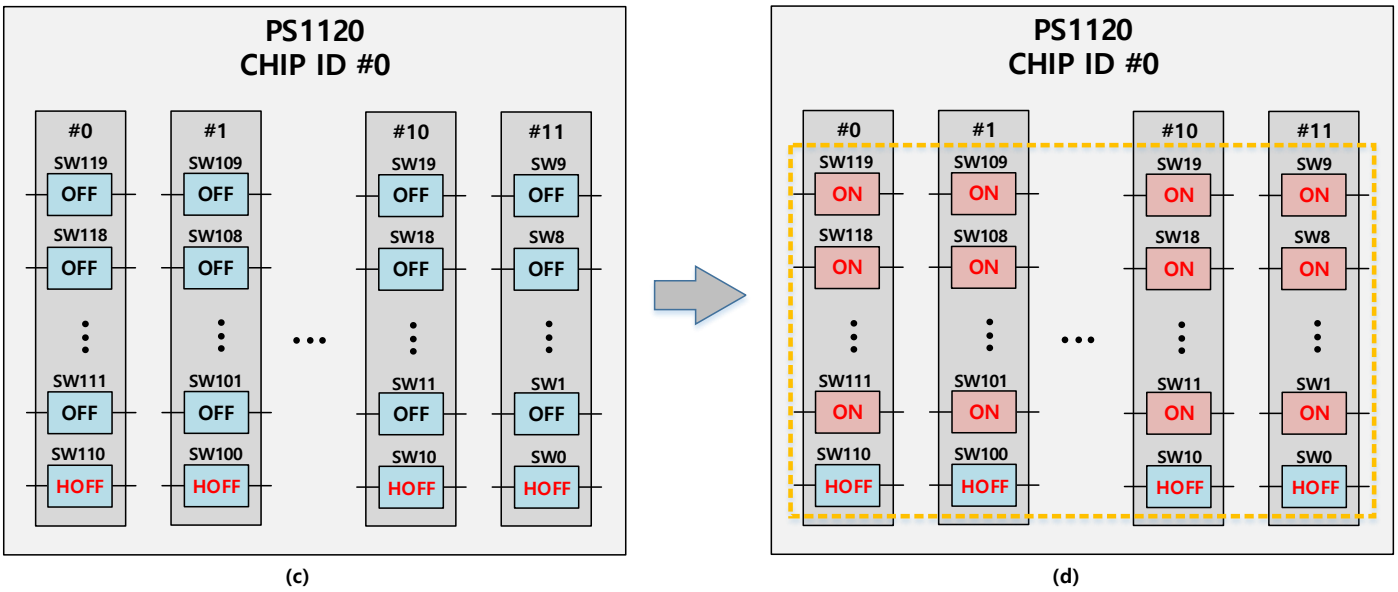
HOLD/FORCE/RELEASE Operation Example

- **HOLD example**

■ ***ROW #0 ~ #8 OFF, ROW #9 HOLD OFF***

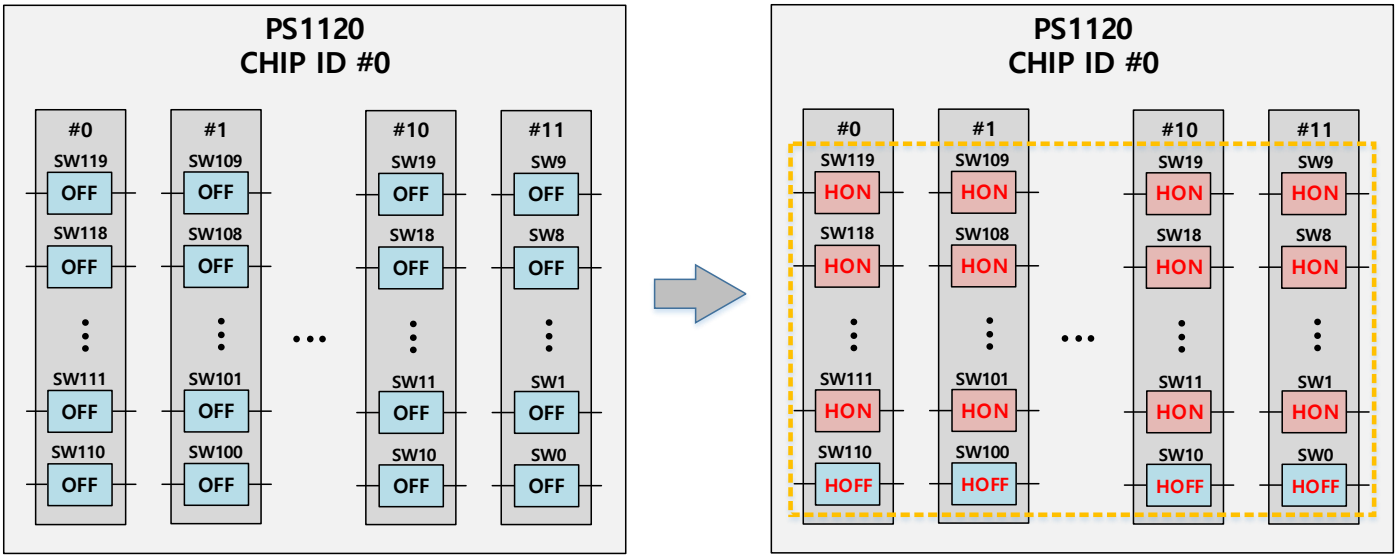


■ ***ALL ON***

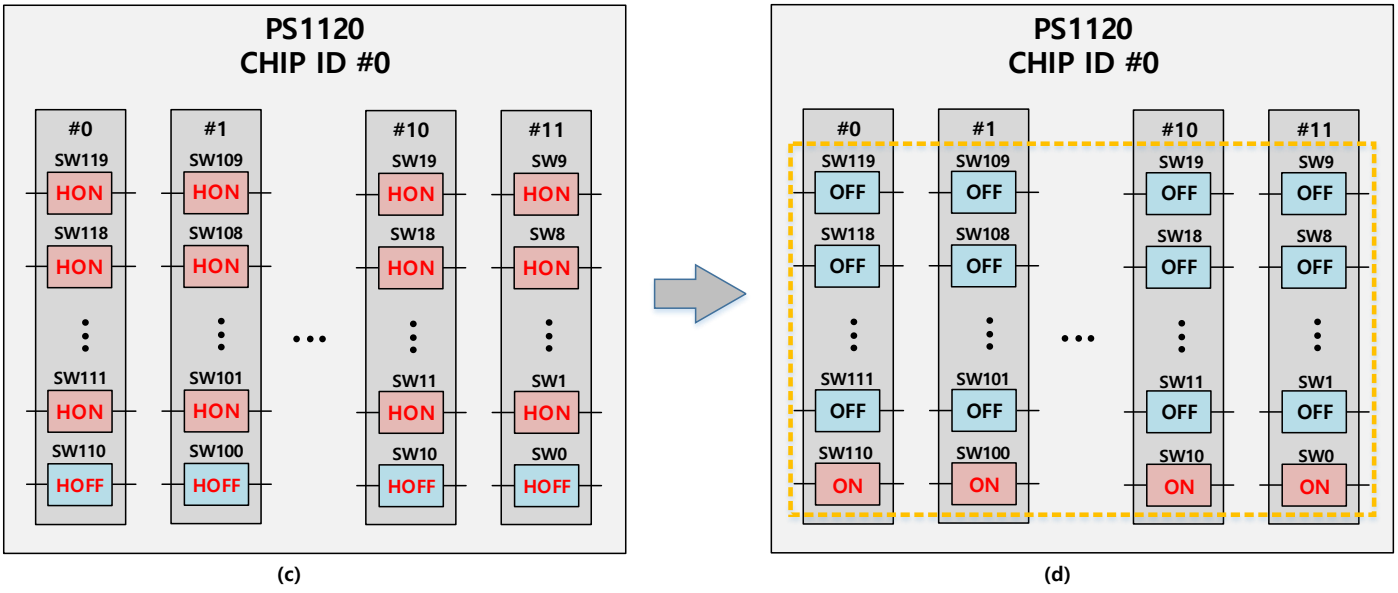


- **FORCE example**

■ ***ROW #0 ~ #8 HOLD ON, ROW #9 HOLD OFF***

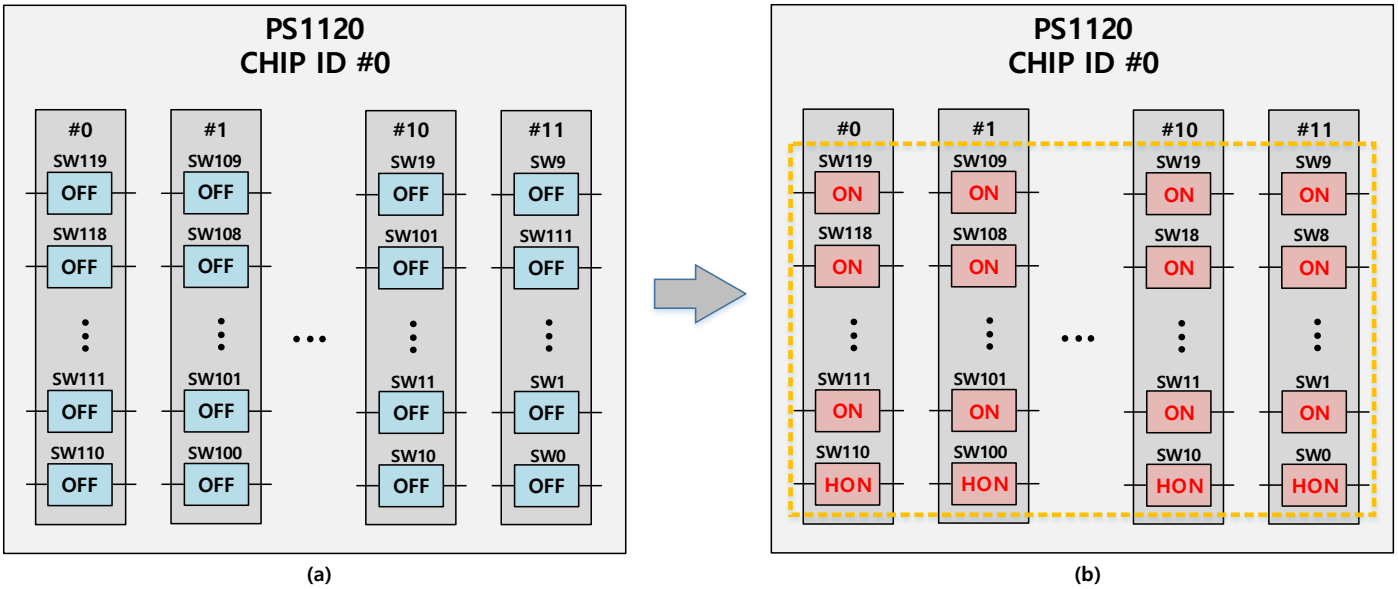


■ ***ROW #0 ~ #8 FORCE OFF, ROW #9 FORCE ON***



- **RELEASE example**

■ ***ROW #0 ~ #8 ON, ROW #9 HOLD ON***



■ ***ALL RELEASE OFF***