

STA30 Datasheet

64-Channel CMOS Analog Switch IC

04 January 2019

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Preliminary



The world is driven by analog

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GENERAL DESCRIPTION

The STA30 is a monolithic CMOS device containing 64 independently selectable switches. These switches are fabricated with an advanced submicron CMOS process that provides low power dissipation, low on resistance, low leakage currents, and high signal bandwidth. The STA30 is designed to operate in 3.3V for digital circuits and 5V for analog switches. Each switch can operate with a wide input and output voltage range. In addition, the thermal shutdown function will automatically turn off the channel temperature exceeds 150°C. The off-leakage current is only 50nA at room temperature of 25°C.

All digital input pins adopt the Schmitt trigger I/O, which has 1.0-V to 2.3-V input noise margin to ensure TTL/CMOS-logic compatibility when using a 3.3-V power supply.

FEATURE

- 3.3V logic-compatible input ($V_{IH}=2.3V$, $V_{IL}=1.0V$)
- Dual supply operation: 3.3V for digital, 5V for analog.
- Analog signal frequency: DC-to-30MHz
- Low on-resistance: 12Ω (@typ)
- Wide range analog input from -2.5V to 7V (@max)
- Thermal shutdown temperature: 150°C
- Chip-ID programmable with OTP memory
- Multi-channel switch control
- Switching control using CMOS interface command
- 180-pin FC-FBGA package

APPLICATIONS

- Data-acquisition systems
- Mechanical reed-relay replacement

FUNCTIONAL BLOCK DIAGRAM

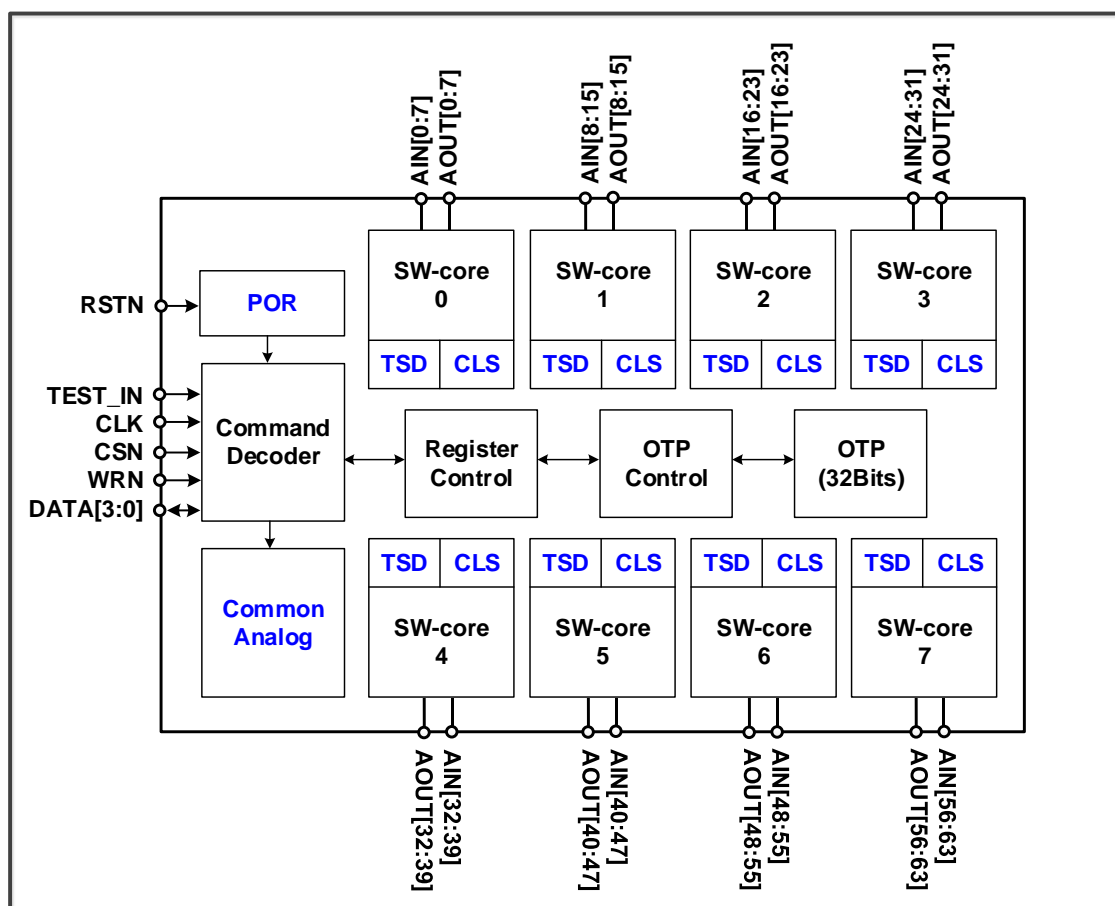


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PIN MAPPING TABLE

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DATA[2]	DATA[1]	CLK	WRN	VPP	AOUT[60]	AIN[60]	AOUT[56]	AIN[56]	AOUT[52]	AIN[55]	AIN[54]	AIN[53]	AIN[52]	A
B	DATA[3]	DATA[0]	PAGE_UP	CSN	DVSS	AOUT[61]	AIN[61]	AOUT[57]	AIN[57]	AOUT[53]	AOUT[51]	AOUT[50]	AOUT[49]	AOUT[48]	B
C	DVDD	DVSS	TEST_IN	RSTN	DVDD	AOUT[62]	AIN[62]	AOUT[58]	AIN[58]	AOUT[54]	AIN[51]	AIN[50]	AIN[49]	AIN[48]	C
D	AVSS	AVDD	AVSS	AVSS	DVSS	AOUT[63]	AIN[63]	AOUT[59]	AIN[59]	AOUT[55]	AVSS	AVSS	AVDD	AVSS	D
E	AIN[0]	AIN[1]	AIN[2]	AIN[3]	AVDD	AVSS	AVSS	AVDD	AVSS	AVDD	AOUT[47]	AOUT[46]	AOUT[45]	AOUT[44]	E
F	AOUT[0]	AOUT[1]	AOUT[2]	AOUT[3]	AVSS	STA30 (Top View)				AVSS	AIN[47]	AIN[46]	AIN[45]	AIN[44]	F
G	AIN[4]	AIN[5]	AIN[6]	AIN[7]	AVDD					AVSS	AOUT[43]	AOUT[42]	AOUT[41]	AOUT[40]	G
H	AOUT[4]	AOUT[5]	AOUT[6]	AOUT[7]	AVSS					AVDD	AIN[43]	AIN[42]	AIN[41]	AIN[40]	H
J	AIN[8]	AIN[9]	AIN[10]	AIN[11]	AVSS					AVSS	AOUT[39]	AOUT[38]	AOUT[37]	AOUT[36]	J
K	AOUT[8]	AOUT[9]	AOUT[10]	AOUT[11]	AVDD	AVSS	AVDD	AVSS	AVSS	AVDD	AIN[39]	AIN[38]	AIN[37]	AIN[36]	K
L	AIN[12]	AIN[13]	AIN[14]	AIN[15]	AOUT[19]	AIN[23]	AOUT[23]	AIN[27]	AOUT[27]	AIN[31]	AOUT[31]	AVSS	AIN[35]	AOUT[35]	L
M	AOUT[12]	AOUT[13]	AOUT[14]	AOUT[15]	AOUT[18]	AIN[22]	AOUT[22]	AIN[26]	AOUT[26]	AIN[30]	AOUT[30]	AVSS	AIN[34]	AOUT[34]	M
N	AVSS	AVDD	AVSS	AVSS	AOUT[17]	AIN[21]	AOUT[21]	AIN[25]	AOUT[25]	AIN[29]	AOUT[29]	AVDD	AIN[33]	AOUT[33]	N
P	AIN[16]	AIN[17]	AIN[18]	AIN[19]	AOUT[16]	AIN[20]	AOUT[20]	AIN[24]	AOUT[24]	AIN[28]	AOUT[28]	AVSS	AIN[32]	AOUT[32]	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PIN DESCRIPTIONS

PIN NAME	I/O	Descriptions
CLK	DI	System clock
RSTN	DI	System reset. Active Low
CSN	DI	Chip select. Active Low
WRN	DI	Data write enable. Active Low
DATA[3:0]	DIO	Data bus
TEST_IN	DI	Tied to GND in Normal mode
PAGE_UP	DI	Tied to GND in Normal mode
VPP	PWR	Tied to GND in Normal mode
AIN[63:0]	AI	Analog switch input
AOUT[63:0]	AO	Analog switch output
AVDD	PWR	Analog Power
AVSS	GND	Analog Ground
DVDD	PWR	Digital Power
DVSS	GND	Digital Ground

AI: analog input
DI: digital Input
PWR: power

AO: analog output
DIO: digital Input / Output
GND: ground

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND, Unless Otherwise Noted.)

AVDD (for Analog Switch).....-0.3V to +6V
 DVDD (for Digital Control).....-0.3V to +4.5V
 Voltage at any digital pin-0.3V to +4.5V
 Voltage at any analog pin- 0.3V to +6V
 Continuous current into any terminal50mA
 Peak current into analog switch I/O.....100mA
 (current pulse with 1ms and 10% duty cycle)

Operating temperature range-40°C to +125°C
 Storage temperature range-55°C to +125°C
 Junction temperature.....+150°C
 ESD protection on all pins (HBM, MM).....≥2kV, 200V

Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at those or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

AVDD=5.0V, AVSS=0V, DVDD=3.3V, DVSS=0V, and TA = +25°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
POWER SUPPLIES							
Analog Supply Voltage		AVDD	AVSS=0V	4.5	5	5.5	V
			AVSS=-2.5V	2.5	5	5.5	V
Digital Supply Voltage		DVDD		3.0	3.3	3.6	V
Analog Ground Voltage		AVSS		-3	-2.5	0	V
Digital Ground Voltage		DVSS		-	0	-	V
ANALOG SWITCH							
Input Signal Range		V _{AIN1}	AVSS=0V, AVDD=5V	0		5	V
		V _{AIN2}	AVSS=-2.5V, AVDD=2.5V	-2.5		2.5	V
		V _{AIN3}	AVSS=-2.5V, AVDD=5V	-2.5		7	V
Channel On Current		I _{CH_ON}	AVDD=5V, V _{AIN} =0V or 5V			50	mA
Switch On-resistance		R _{ON}	I _{CH_ON} =10mA		12	15	Ω
Leakage Current	Source Off Leakage Current	I _{S_OFF}	AVDD=5V, V _{AIN} =5, V _{AO} UT=0V		0.05	0.1	uA
	Drain Off Leakage Current	I _{D_OFF}	AVDD=5V, V _{AIN} =0V, V _{AO} UT=5V		0.05	0.1	uA
	Channel On Leakage Current	I _{CH_OFF}	AVDD=5V, V _{AIN} =0V or 5V		0.05	0.1	uA
Thermal Shutdown Temperature		T _{ST}			+150		°C
Thermal Shutdown Hysteresis		T _{SH}			20		°C

ELECTRICAL CHARACTERISTICS (Continued)

AVDD=5.0V, AVSS=0V, DVDD=3.3V, DVSS=0V, and TA = +25°C, unless otherwise noted.

PARAMETER		SYMBOL	CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
DIGITAL I/O							
Logic Input Voltage	Input High	V _{IH}		0.7* DVDD			V
	Input Low	V _{IL}				0.3* DVDD	V
Logic Input Current	Input High	I _{IH}		-1		1	uA
	Input Low	I _{IL}		-1		1	uA
SWITCH DYNAMIC CHARACTERISTICS							
Switching Time	Turn ON Time	t _{ON}	Clock base (calculate for special condition)		175		ns
	Turn OFF Time	t _{OFF}			235		ns
Capacitance	Input Off-Capacitance	C _{AIN_OFF}			5		pF
	Output Off-Capacitance	C _{AOUT_OFF}			5		pF
	Output On-Capacitance	C _{AOUT_ON}			10		pF
Off-Isolation			No Load, f _{SW} =1MHz		TBD		dB
Channel-to-Channel Crosstalk			No Load, f _{SW} =1MHz		TBD		dB
Switching Frequency		f _{SW}				1.25	MHz

POWER CONSUMPTION							
Analog Operating Current (AVDD)	Static	I_{AVDD_ST}	AVDD=5V, AVSS= 0V		4	5	mA
			AVDD=5V, AVSS= -2.0V		4	5	
			AVDD=5V, AVSS= -2.5V		13	15	
	Dynamic	I_{AVDD_DYN}	AVDD=5V, AVSS= 0V, $f_{CLK}=10MHz$, $f_{SW}=10KHz$,		4	5	mA
			AVDD=5V, AVSS= 0V, $f_{CLK}=10MHz$, $f_{SW}=100KHz$,		4	5	
			AVDD=5V, AVSS= 0V, $f_{CLK}=10MHz$, $f_{SW}=1.25MHz$,		11	15	
			AVDD=5V, AVSS= -2.0V, $f_{CLK}=10MHz$, $f_{SW}=10KHz$,		6	10	
			AVDD=5V, AVSS= -2.0V, $f_{CLK}=10MHz$, $f_{SW}=100KHz$,		6	10	
			AVDD=5V, AVSS= -2.0V, $f_{CLK}=10MHz$, $f_{SW}=1.25MHz$,		17	20	
			AVDD=5V, AVSS= -2.5V, $f_{CLK}=10MHz$, $f_{SW}=10KHz$,		14	15	
			AVDD=5V, AVSS= -2.5V, $f_{CLK}=10MHz$, $f_{SW}=100KHz$,		14	15	
			AVDD=5V, AVSS= -2.5V, $f_{CLK}=10MHz$, $f_{SW}=1.25MHz$,		23	25	
Analog Operating Current (AVSS)	Static	I_{AVSS_ST}	AVDD=5V, AVSS= 0V		4	5	mA
			AVDD=5V, AVSS= -2.0V		4	5	
			AVDD=5V, AVSS= -2.5V		13	15	
	Dynamic	I_{AVSS_DYN}	AVDD=5V, AVSS= 0V, $f_{CLK}=10MHz$, $f_{SW}=10KHz$,		4	5	mA
			AVDD=5V, AVSS= 0V, $f_{CLK}=10MHz$, $f_{SW}=100KHz$,		4	5	
			AVDD=5V, AVSS= 0V, $f_{CLK}=10MHz$, $f_{SW}=1.25MHz$,		11	15	
			AVDD=5V, AVSS= -2.0V, $f_{CLK}=10MHz$, $f_{SW}=10KHz$,		6	10	
			AVDD=5V, AVSS= -2.0V, $f_{CLK}=10MHz$, $f_{SW}=100KHz$,		6	10	
			AVDD=5V, AVSS= -2.0V, $f_{CLK}=10MHz$, $f_{SW}=1.25MHz$,		17	20	
			AVDD=5V, AVSS= -2.5V, $f_{CLK}=10MHz$, $f_{SW}=10KHz$,		14	15	
			AVDD=5V, AVSS= -2.5V, $f_{CLK}=10MHz$, $f_{SW}=100KHz$,		14	15	
			AVDD=5V, AVSS= -2.5V, $f_{CLK}=10MHz$, $f_{SW}=1.25MHz$,		23	25	
Digital Operating Current (DVDD)	Static	I_{DVDD_ST}	DVDD=3.3V		4	5	mA
	Dynamic	I_{DVDD_DYN}	DVDD=3.3V, $f_{CLK}=10MHz$, Combined operation of Reset, and DUT-Reject		6	10	mA

All switch On/Off operating simultaneously

TIMING CHARACTERISTICS

AVDD=5.0V, AVSS=0V, DVDD=3.3V, DVSS=0V, and TA = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
DIGITAL I/O SIGNALS						
CLK Period	t _{PERIOD}		20			ns
CLK Frequency	f _{CLK}				50	MHz
DATA to CLK Setup Time	t _{DS}		10			ns
DATA to CLK Hold Time	t _{DH}		5			ns
CSN to CLK Setup Time	t _{CS}		10			ns
CSN to CLK Hold Time	t _{CH}		5			ns
WRN to CLK Setup Time	t _{WS}		10			ns
WRN to CLK Hold Time	t _{WH}		5			ns
POWER AND RESET SEQUENCE						
Power-up Period	t _{PU}		500			us
Power-down Period	t _{PD}		500			us
Power-on Reset Time	t _{RST}		500			us
OTP Read Time	t _{ORD}	CLK freq. >= 10MHz	200			us
		CLK freq. < 10MHz	2000			cycle
SWITCH ON/OFF TIMING DIAGRAM						
1-Clock Command Control Time	t _{SW1}				3	cycle
2-Clock Command Control Time	t _{SW2}				6	cycle

Timing Diagram of Digital I/O Signals

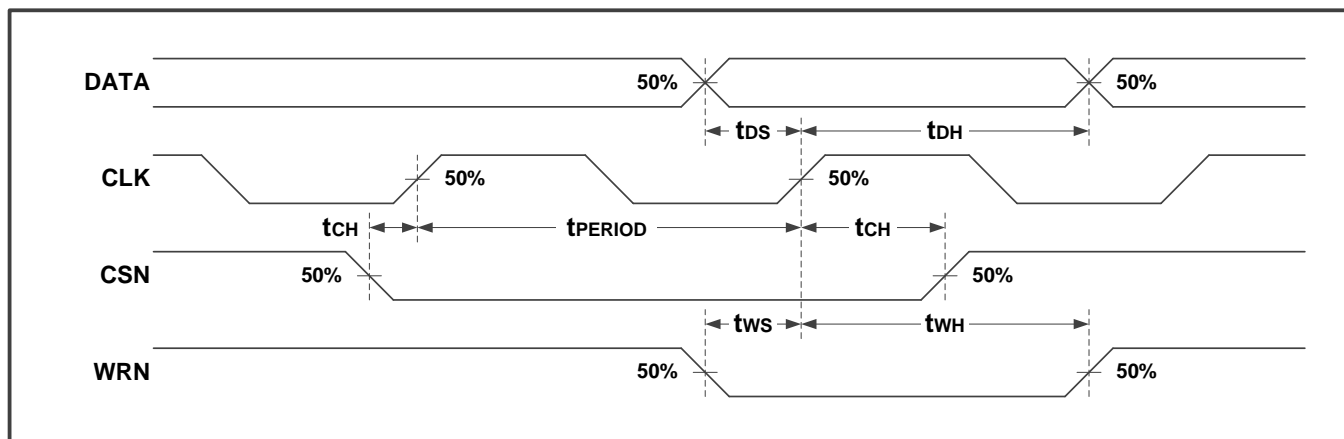
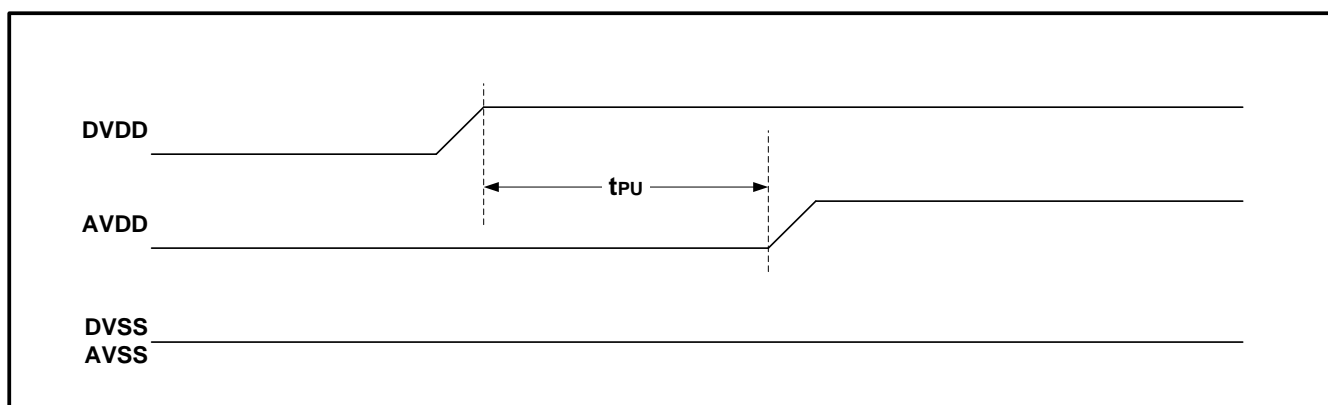
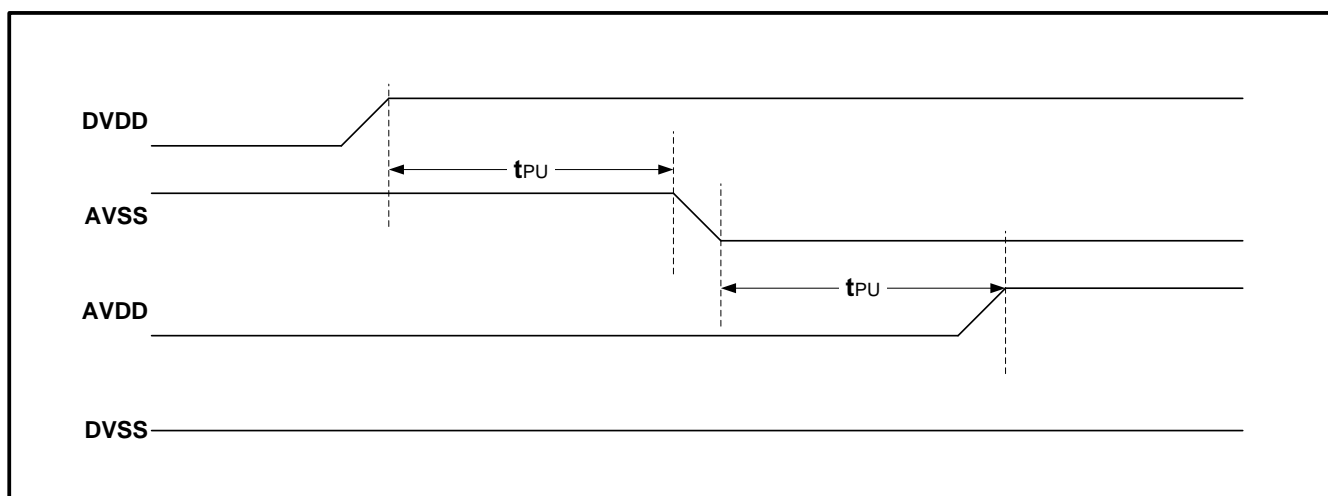


Figure 1. Timing Diagram of Digital Signals.

Power and Reset sequence



(a) In case $AVSS = 0\text{ V}$



(b) In case $AVSS < 0\text{ V}$

Figure 2. Power-up Sequence.

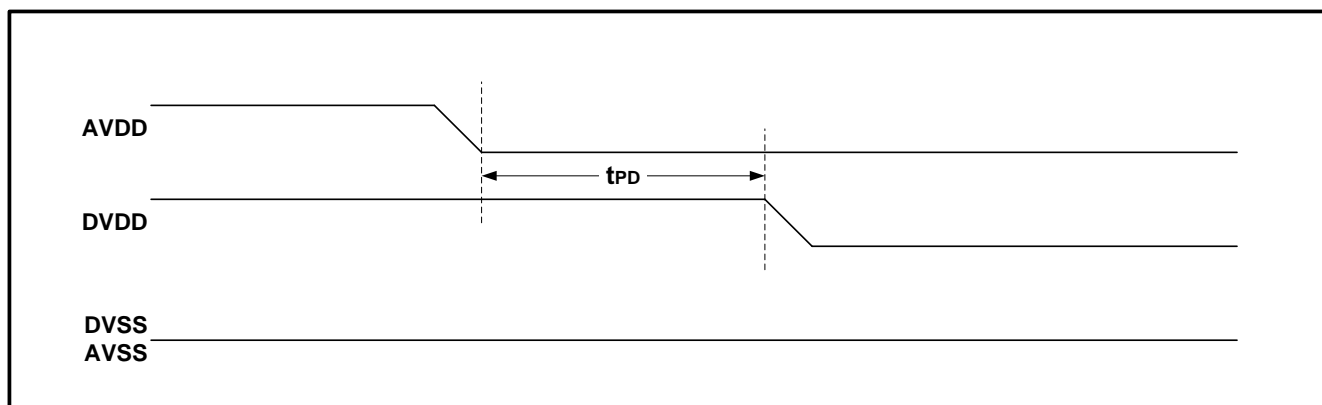
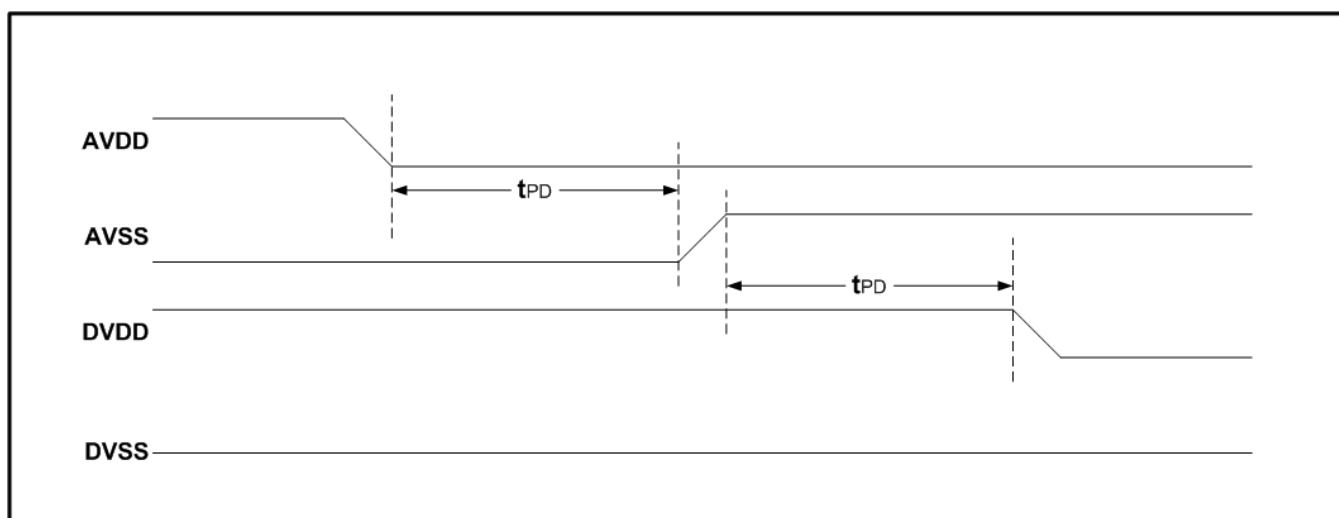
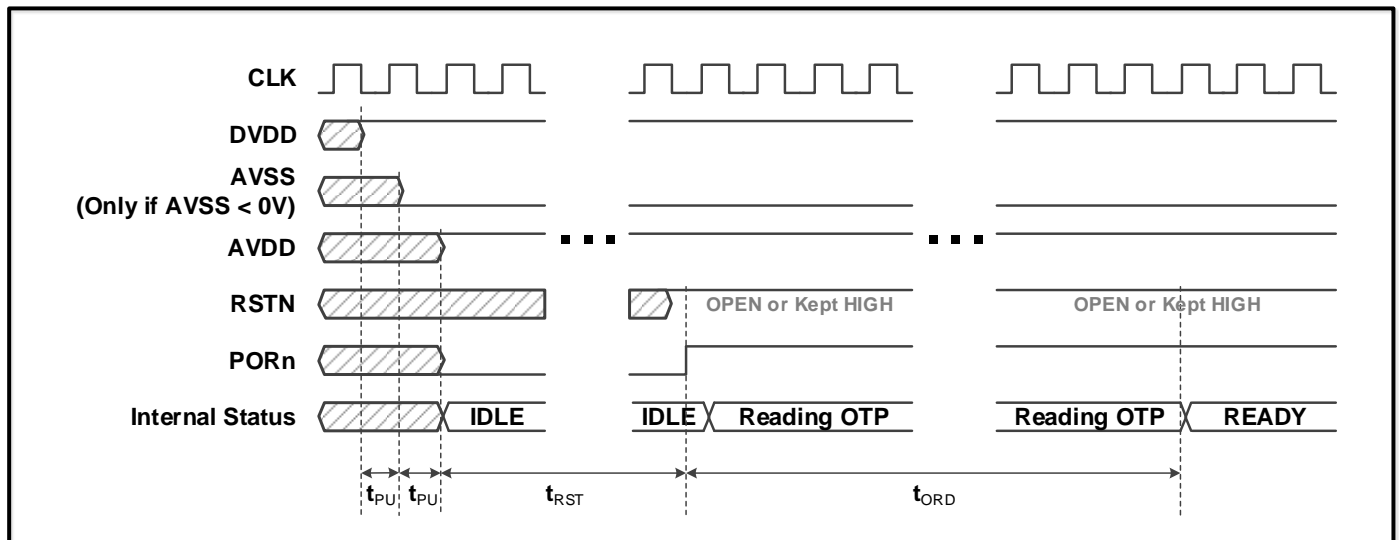
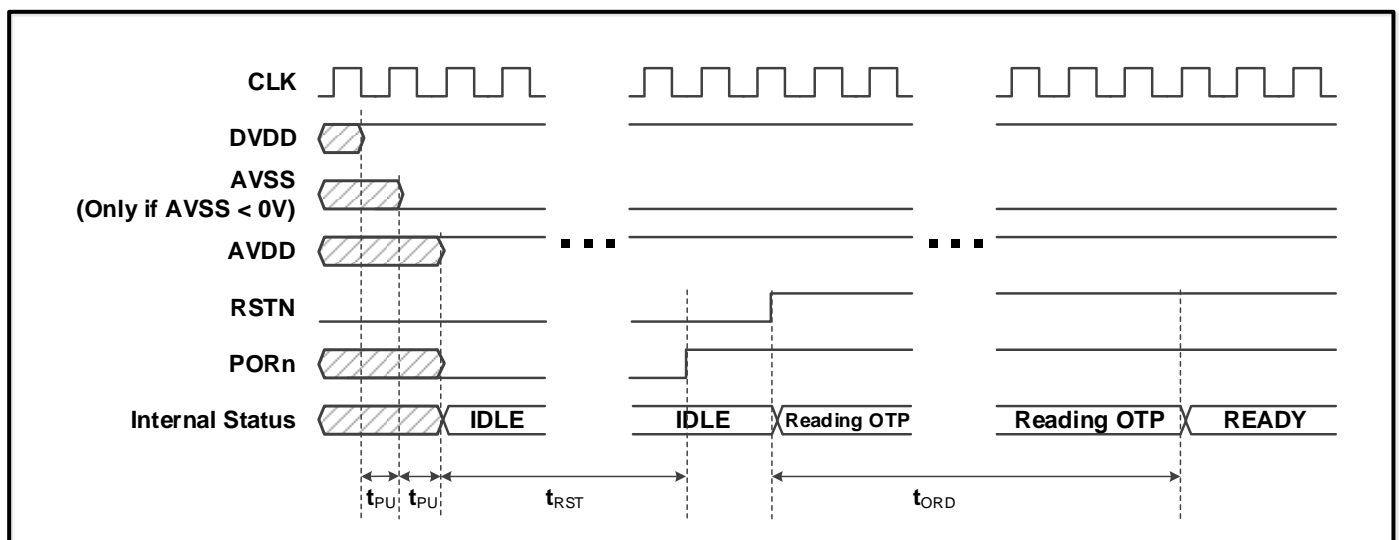
(a) In case $AVSS = 0\text{ V}$ (b) In case $AVSS < 0\text{ V}$

Figure 3. Power-down Sequence.



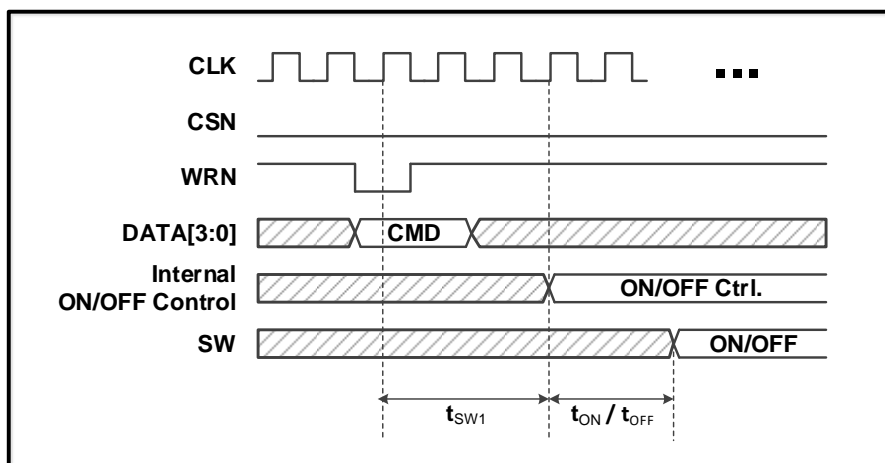
(a) In case RSTN is OPEN or kept HIGH before $(t_{PU} + t_{PU} + t_{RST})$.



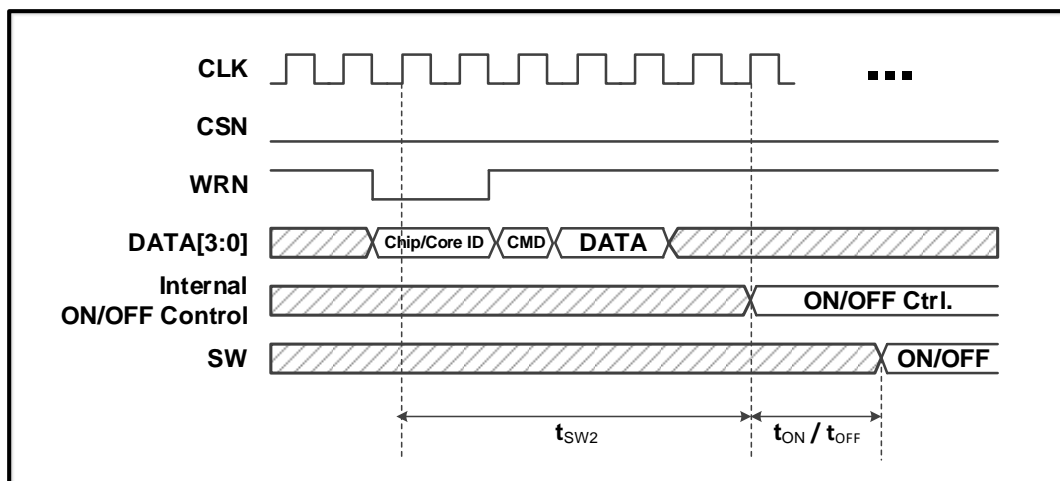
(b) In case RSTN changes from LOW to HIGH after $(t_{PU} + t_{PU} + t_{RST})$.

Figure 4. Reset and Stand-by Sequence.

Switch On/Off Timing Diagram



(a) 1-clock command switch on/off timing diagram.



(b) 2-clock command switch on/off timing diagram.

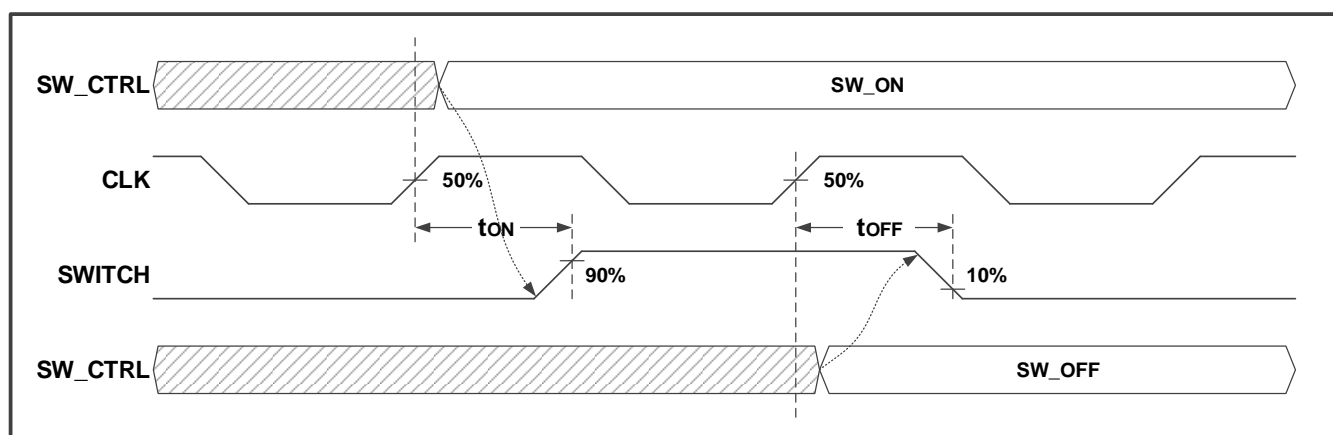
(c) Detail t_{ON} / t_{OFF} timing diagram.

Figure 5. Switch On/Off Timing Diagram.

TEST CIRCUITS

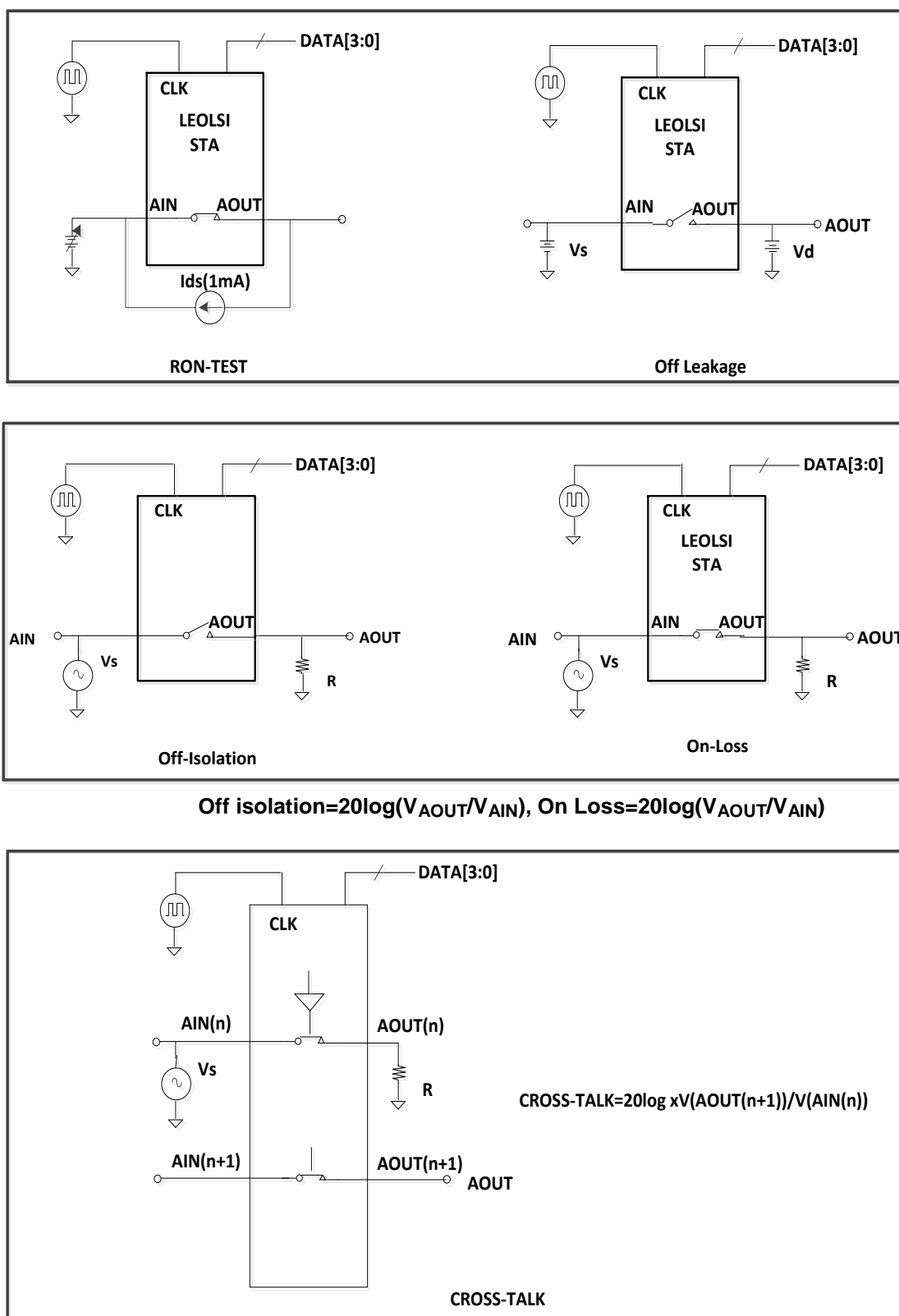
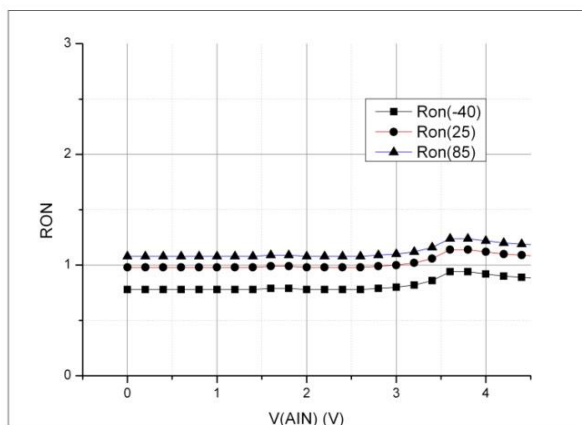
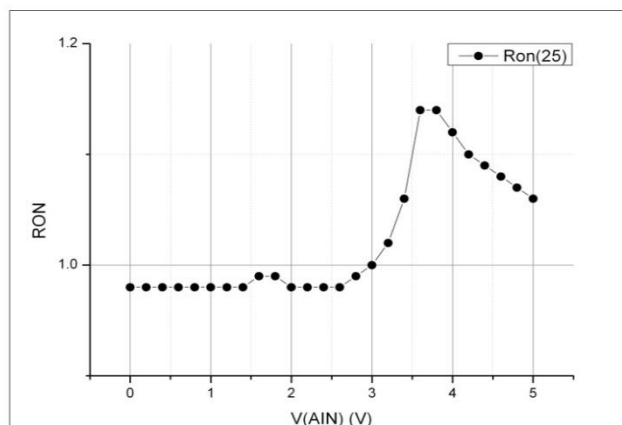


Figure 6. Test Circuits.

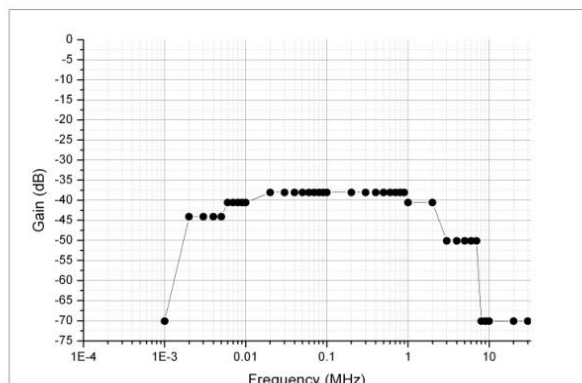
TEST RESULTS



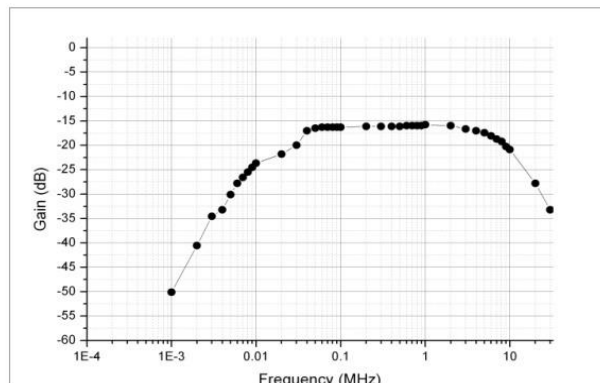
On-resistance vs. VAIN



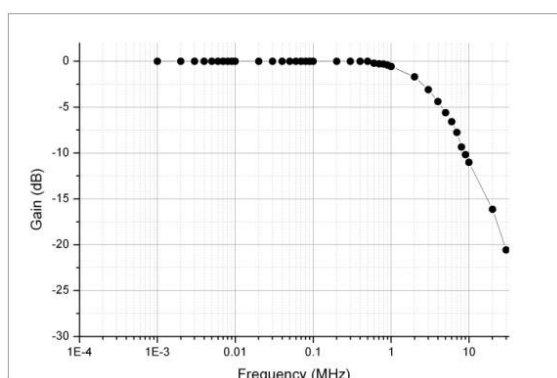
On-resistance(room temp) vs. VAIN



Cross talk vs. Frequency



Isolation vs. Frequency



On Loss vs. Frequency

Figure 7. Test Results.

FUNCTIONAL DESCRIPTION

Internal Structure

STA30 is analog switches with control logic. It consists of 8 switching Cores and control logics. Since each switching Core has 8 switches, a STA30 contains 64 switches. Each switch has an ID from 0 to 7.

The switches in STA30 can also be grouped into Channels. A Channel indicates the switches of the same ID in all cores. For example, Channel1 indicates Switch1s in Core0, Core1, Core2, ..., and Core7. The host can control the switches either by Cores or Channels. Figure 8 shows the internal structure of Cores, Channels, and Switches.

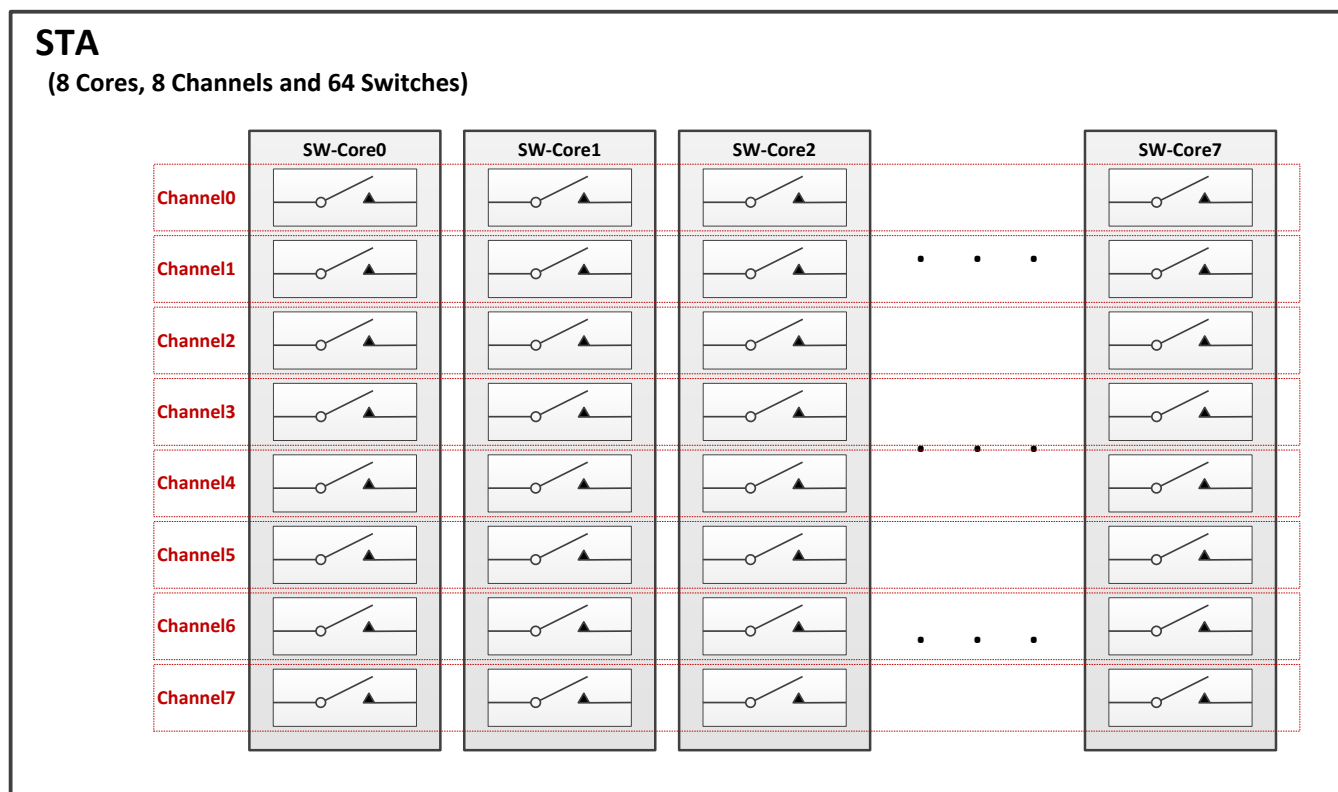


Figure 8. Internal Structure of STA30.

Connection

In system application, control signals can be shared among multiple STA30s. Figure 9 shows an example for the connection of multiple STA30s.

STA30s with the same control signals are called Bank. Since there are multiple STA30s in a Bank, there should be a way to specify the target chip for the control commands. To support this, Chip-ID is used.

Chip-ID is a 5-bit number decided either from the internal OTP memory. Each STA30 acquires its Chip-ID on bootstrap, and user can specify the target chip of the control commands by sending target Chip-ID with them. Since Chip-ID is a 5-bit number, the maximum number of STA30s in one bank is 32.

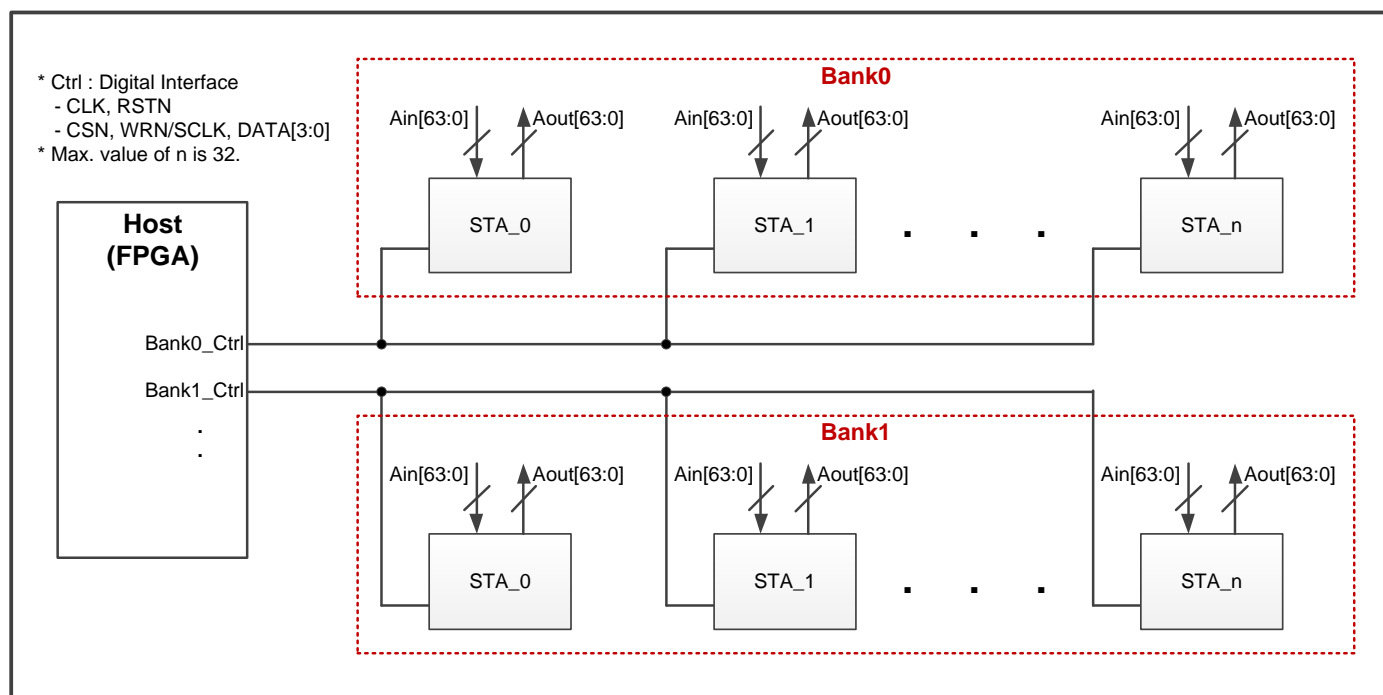


Figure 9. Example for connecting STA30s.

Power-up Sequence

STA30 requires two kinds of Power/Ground pairs – AVDD/AVSS and DVDD/DVSS. As the names imply, AVDD/AVSS pair is for Analog circuits, and DVDD/DVSS pair is for Digital logic. To ensure reliable operation on power-up, it is required that each Power and Ground should be provided in proper order. Figure 10 shows the Power-up sequence of STA30.

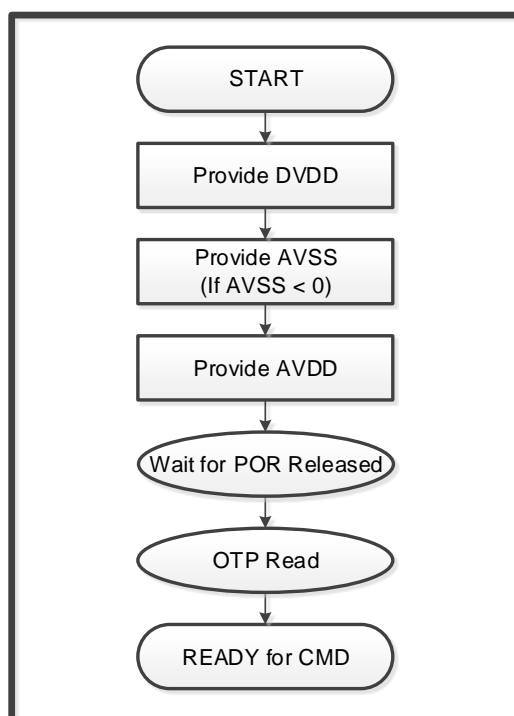


Figure 10. Power-up Sequence.

As depicted in Figure 10, the logic power, DVDD, should be provided first. If AVDD is provided prior to DVDD, the switch control logic's state is undefined until DVDD is supplied, which may unintentionally turn on the switches before DVDD is supplied. Note that for negative AVSS, AVSS also should be provided after DVDD, because negative AVSS means a certain voltage ($AVDD - AVSS$) is applied to the analog circuit.

If STA30 is supplied with DVDD and AVDD, the internal POR of STA30 generates RESET signal internally, and STA30 changes to RESET state until the RESET signal from POR is released. RESET from POR is released after t_{RST} , and STA30 starts reading its own internal OTP memory.

External RESET is also supported through a pin named RSTN, and actual RESET signal is generated from both POR and RSTN signals. This leads to that on power-up, if RSTN is released before POR is released (i.e. RSTN changes from LOW to HIGH before $t_{PU} + t_{PU} + t_{RST}$ is elapsed), actual RESET signal is still active (i.e. RESET is being issued) until RESET from POR is released. On the other hand, if RSTN is kept LOW though POR is released, actual RESET signal is still active until RSTN is released.

However, since RSTN pin is internally pulled-up, user may leave RSTN pin OPEN in most of the cases. For the detailed timing of power-up sequence, refer to Figure 2. *Power-up Sequence*.

Interface Protocol & Types of Commands

Controlling STA30s is performed through commands from the host. The host sends commands through two control signals (CSN and WRN) and 4-bit wide data pins. CSN signal is used to select the target Bank, and WRN signal decides the type of the command. The protocol for each command is decided by the type of the command – 1/2 clock commands.

- 1-Clock Commands (Writing Commands Only)

1-clock commands are the commands for which WRN signal goes LOW for single cycle. Figure 11 shows the timing diagram for 1-clock commands.

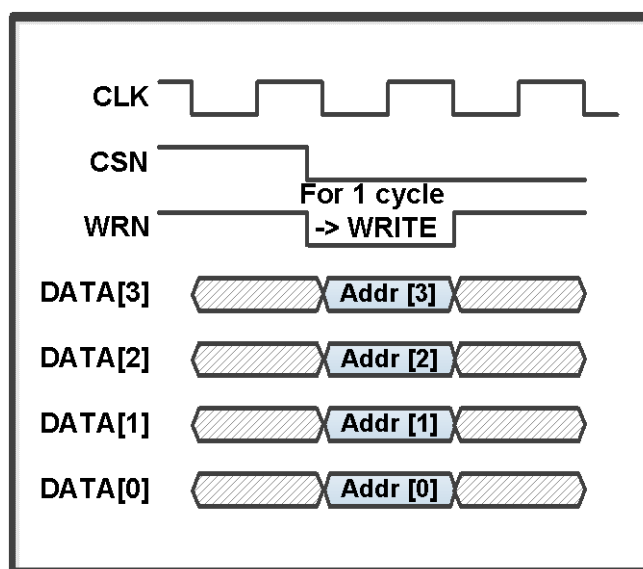


Figure 11. Timing Diagram for 1-Clock Commands.

The 1-clock commands consist of the commands which are applied to all switches of all STA30s in the bank. Since the target for the 1-clock command is all switches in all Cores of all STA30s, they require neither Chip ID nor Core ID.

- 2-Clock commands (Writing Commands Only)

2-clock commands are the commands for which WRN signal goes LOW for two clocks. Each command includes Chip-ID, Core-ID, Command, and Parameters, and it is mainly used to control the switches. Figure 12 shows the timing diagram for 2-clock commands.

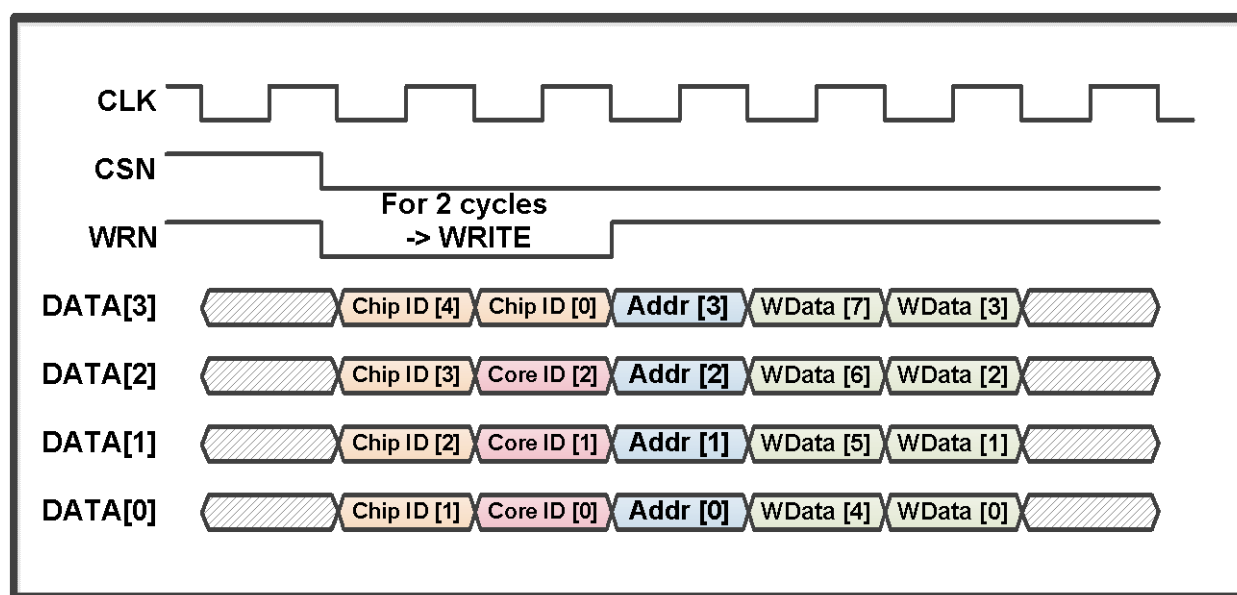


Figure 12. Timing Diagram for 2-Clock commands.

As shown in Figure 12, IDs and commands are received through DATA[3:0] pins. Chip-ID specifies the target STA30 in the bank, and Core-ID specifies the target Core / Channel of the target chip. Addr[3:0] is the actual command, and WData[7:0] is a parameter to control the states of the 8 switches specified by Chip-ID and Core-ID. All of the 2-clock commands are for writing WData[7:0] to target registers.

Controlling Switches

- States of Switches

The main usage of STA30 is to control AIN – AOUT connection by changing the states of its switches. Each switch can be in one of two states – ON, OFF.

In **ON** state, the switch is turned-on, and the AIN signal is CONNECTED to the corresponding AOUT signal.

In **OFF** state, the switch is turned-off, and the AIN signal is DISCONNECTED from the corresponding AOUT signal.

Besides ON/OFF states, each switch has an additional flag named **REJECT**. If REJECT flag is set for a switch, the switch changes to OFF state automatically, and further commands to turn on the switch are ignored. Only special 1-clock commands or external reset (RSTN) can clear the REJECT flag.

- Initialization of Switches

The initialization of the switches can be done through initialization commands. There are four initialization commands. They are,

- > 1-clock command 0x2: RESET_ALL
- > 1-clock command 0x3: CLEAR_ALL
- > 1-clock command 0x4: ENABLE_ALL
- > 1-clock command 0x5: INITIAL_ALL

Since all of these commands are 1-clock commands, they are executed by all STA30s in the selected bank by CSN signal. The states of all switches in the bank are simultaneously changed by these commands, and it helps set the initial states of all switches with less commands. For the detailed information about each command, refer to *Commands Descriptions*.

- Changing States of Switches

To change the states of switches, DIRECT_XXX commands are used.

- > 2-clock command 0x2: DIRECT_CHP_COR
- > 2-clock command 0x3: DIRECT_BNK_COR
- > 2-clock command 0x5: DIRECT_CHP_CHN
- > 2-clock command 0x6: DIRECT_BNK_CHN
- > 2-clock command 0xA: DIRECT_COR_SW
- > 2-clock command 0xB: DIRECT_CHN_SW

DIRECT_XXX commands directly specify the ON-OFF states of the target switches. The target switches are specified using Chip-ID and Core-ID in the transmitted command, combined with the suffix of the command. The intended ON-OFF states for the target switches are transmitted through WData[7:0]. To turn on the switch, corresponding bit of WData should be '1', and to turn off, it should be '0'. For the detailed information about each DIRECT_XXX commands, refer to *Commands Descriptions*.

- Setting REJECT Flags

A REJECT flag is used to let the switch ignore further ON-OFF related commands. It is useful when we want some switches to stay OFF while we control many switches simultaneously with commands such as DIRECT_BNK_COR. REJECT flags can be controlled by REJECT_XXX commands. There are four commands to set REJECT flags.

- > 2-clock command 0x4: REJECT_CHP_COR
- > 2-clock command 0x7: REJECT_CHP_CHN
- > 2-clock command 0xC: REJECT_COR_SW
- > 2-clock command 0xD: REJECT_CHN_SW

REJECT flags are set to '1' according to the transmitted WData[7:0] of REJECT_XXX commands. If a bit of WData is '0', corresponding REJECT flag(s) is set to '1'. Otherwise, corresponding REJECT flag(s) does not change. The target switches are specified by Chip-ID and Core-ID of the transmitted command. For the detailed information about REJECT_XXX commands, refer to *Commands Descriptions*.

Protection from Excessive Current

- Current Limiting (Default: Disable)

STA30 supports Current Limiting to protect itself from excessive high current. If current more than the threshold flows through a switch, the switch is automatically DISCONNECTED by internal protection circuit. The threshold is 60mA at 25°C.

Once the switch is disconnected by Current Limiting, the switch does not work until it is turned off. To make the disconnected switch work again, it should be turned off first, then it can work after it is turned on again.

Current Limiting feature is enabled by CL_EN bit (bit 1) of General Control Register (i.e. enabled if CL_EN = 1). For more information about CL_EN bit, refer to WR_GCON (0x1) of *Commands Descriptions*.

- Thermal Shutdown (Default: Disable)

STA30 supports thermal shutdown to protect itself from excessive high current. If the temperature of a switch goes above the threshold (+150°C, typ.), the switch is automatically DISCONNECTED by internal thermal shutdown circuit. The threshold is loaded from internal OTP memory programmed during manufacturing. Thermal Shutdown is the secondary protection scheme for the case that Current Limiting does not work for some reasons even though excessive high current flows. The switch turns on again after the device temperature drops by approximately 20°C (typ.).

Once the switch is disconnected by Thermal Shutdown, the switch does not work until the temperature goes below the

threshold.

Thermal Shutdown feature is enabled by TS_EN bit (bit 0) of General Control Register (i.e. enabled if TS_EN = 1). For more information about TS_EN bit, refer to *WR_GCON* of *Commands Descriptions*.

Commands Descriptions

- Suffixes of the Commands

Most of STA30's commands are to control the states of the switches. Basically, each command can control switches in Core unit. However, to reduce the number of commands for setting the states of the switches, several variations of commands are supported, and they can address target switches in different ways from basic command (i.e. in Core unit). To represent this easily, commands have suffixes which represent the range of the target switches. The suffixes are,

- > *_ALL
- > *_BNK_COR / *_BNK_CHN
- > *_CHP_COR / *_CHP_CHN
- > *_COR_SW / *_CHN_SW

_ALL suffix is for 1-clock commands. It represents that the target switches for this command is ALL SWITCHES IN THE BANK.

_BNK_COR / _BNK_CHN suffixes are for 2-clock commands. They represent that the target switches for this command are ALL SWITCHES IN THE BANK. While WData for _BNK_COR commands are in Core unit, WData for _BNK_CHN commands are in Channel unit. Since WData is applied to all Cores / Channels in all STA30s in the Bank, Chip-ID / Core-ID are ignored.

_CHP_COR / _CHP_CHN suffixes are for 2-clock commands. They represent that the target switches for this command are ALL SWITCHES IN THE SPECIFIED CHIP. While WData for _CHP_COR commands are in Core unit, WData for _CHP_CHN commands are in Channel unit. Since WData is applied to all Cores / Channels in the specified STA30, Core-ID is ignored.

_COR_SW / _CHN_SW suffixes are for 2-clock commands. They represent that the target switches for this command are SWITCHES OF THE SPECIFIED CORE / CHANNEL IN THE SPECIFIED CHIP. While WData for _COR_SW commands are in Core unit, WData for _CHN_SW commands are in Channel unit. Since WData is applied to single Core / Channel in the specified STA30, both Chip-ID / Core-ID are used.

- 1-Clock Commands

Table 1 shows the list of the 1-clock commands.

Table 1. 1-Clock Commands List.

Addr	Command	Description
0x0	RSVD	Reserved
0x1	RSVD	Reserved
0x2	RESET_ALL	Turns-off all switches of all chips in the Bank (i.e. OFF state). REJECT flags are cleared.
0x3	CLEAR_ALL	Turns-off all switches of all chips in the Bank (i.e. OFF state). REJECT flags are NOT affected.
0x4	ENABLE_ALL	Turns-on all switches of all chips in the Bank (i.e. ON state). Switches with REJECT flags remain in OFF state.
0x5	INITIAL_ALL	Turns-on all switches of all chips in the Bank (i.e. ON state). REJECT flags are cleared. Switches with REJECT flags are also changed to ON state.
0x6 ~ 0xA	RSVD	Reserved
0xB	EN1_WCON	First sequence to enable writing to control register. Should be followed by EN2_WCON command to enable writing. Otherwise, both EN1_WCON and EN2_WCON commands are canceled.
0xC	EN2_WCON	Enables writing to control registers. Should be preceded by EN1_WCON. If not preceded by EN1_WCON, EN2_WCON is ignored. Note) To enable writing to control registers, EN1_WCON -> EN2_WCON commands should be issued in order. Otherwise, both EN1_WCON and EN2_WCON commands are canceled.
0xD	DIS_WCON	Disables writing to control register.
0xE	RSVD	Reserved
0xF	RSVD	Reserved

■ **RESET_ALL (0x2) / CLEAR_ALL (0x3) / ENABLE_ALL (0x4) / INITIAL_ALL (0x5)**

RESET_ALL / CLEAR_ALL / ENABLE_ALL / INITIAL_ALL commands are mainly used for initialization of switches in the selected Bank. These commands are applied to all switches of all STA30s in the Bank simultaneously.

RESET_ALL / CLEAR_ALL commands turn off (i.e. change to OFF state) all switches of all STA30s in the Bank. The difference between these two commands is that while RESET_ALL command also clears REJECT flags altogether, CLEAR_ALL command does not affect REJECT flags.

INITIAL_ALL / ENABLE_ALL commands turn on (i.e. change to ON state) all switches of all STA30s in the Bank. The difference between these two commands is that while INITIAL_ALL command also clears REJECT flags of all switches, ENABLE_ALL command does not affect REJECT flags.

Table 2 shows the operation of the four initialization commands.

Table 2. Operation of Initialization Commands.

Command	ON-OFF States	REJECT Flags
RESET_ALL	OFF	CLEARED
CLEAR_ALL	OFF	NOT AFFECTED
INITIAL_ALL	ON	CLEARED
ENABLE_ALL	ON	NOT AFFECTED

■ **EN1_WCON (0xB) / EN2_WCON (0xC) / DIS_WCON (0xD)**

By default, writing to control registers is disabled to prevent unintentional corruption of them. Therefore, it is needed to enable writing to control registers before updating control registers. By issuing EN1_WCON and EN2_WCON commands in order, writing to control register is internally enabled, and control registers can be updated by following 2-clock commands. Figure 13 shows an example for writing to GCON register.

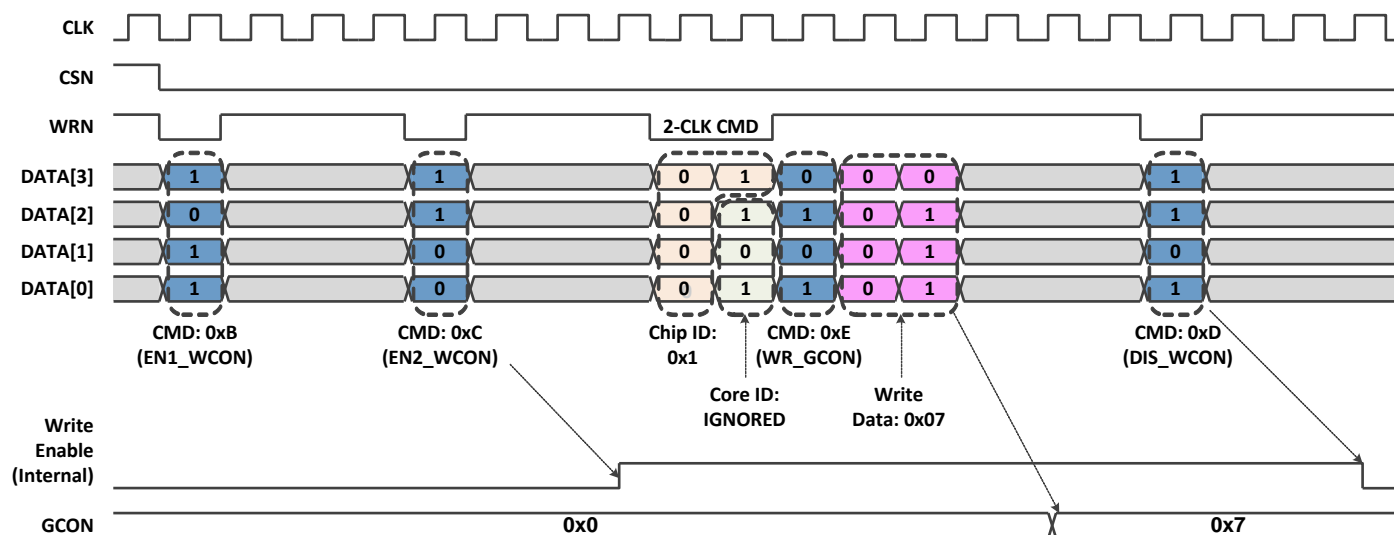


Figure 13. Example for Writing to Control Registers.

As shown in Figure 13, writing to control register is internally enabled by issuing EN1_WCON and EN2_WCON commands in order, and control registers are updated by WR_GCON command, a 2-clock command.

After updating the control register, DIS_WCON command is issued to disable writing to control register again.

- 2-Clock commands

Table 3 shows the list of 2-clock commands.

Table 3. 2-Clock commands List.

Addr	Command	Function
0x0	RSVD	Reserved
0x1	WR_GCON	Writes to General Control Register. Chip-ID specifies the target STA30. Core-ID is ignored. WData is the written value to GCON register.
0x2	DIRECT_CHP_COR	Changes ON-OFF states of all switches in the specified STA30. Updates all Cores' ON-OFF states of the target STA30. Switches whose REJECT flags are '1' remain in OFF state. Chip-ID specifies the target STA30. Core-ID is ignored. WData represents the update value for ON-OFF states of all Cores in the target STA30. 0: OFF, 1: ON
0x3	DIRECT_BNK_COR	Changes ON-OFF states of all switches of all STA30s in the selected Bank. Updates all Cores' ON-OFF states of all STA30s in the selected Bank. Switches whose REJECT flags are '1' remain in OFF state. Chip-ID is ignored. Core-ID is ignored. WData represents the update value for ON-OFF states of all Cores in the target STA30. 0: OFF, 1: ON
0x4	REJECT_CHP_COR	Changes the REJECT flags of the specified STA30. ON-OFF states are updated according to REJECT flags' values. Chip-ID specifies the target STA30. Core-ID is ignored. WData[0] represents the update value for REJECT flags of Core0. WData[1] represents the update value for REJECT flags of Core1. WData[2] represents the update value for REJECT flags of Core2. WData[3] represents the update value for REJECT flags of Core3. WData[4] represents the update value for REJECT flags of Core4. WData[5] represents the update value for REJECT flags of Core5. WData[6] represents the update value for REJECT flags of Core6. WData[7] represents the update value for REJECT flags of Core7. 0: REJECT, 1: No Change.
0x5	DIRECT_CHP_CHN	Changes ON-OFF states of all switches in the specified STA30. Updates all Channels' ON-OFF states of the target STA30. Switches whose REJECT flags are '1' remain in OFF state. Chip-ID specifies the target STA30. Core-ID is ignored. WData represents the update value for ON-OFF states of all Channels in the target STA30. 0: OFF, 1: ON

(Continued)

(Continued)

0x6	DIRECT_BNK_CHN	<p>Changes ON-OFF states of all switches of all STA30s in the selected Bank. Updates all Channels' ON-OFF states of all STA30s in the selected Bank. Switches whose REJECT flags are '1' remain in OFF state.</p> <p>Chip-ID is ignored. Core-ID is ignored. WData represents the update value for ON-OFF states of all Channels in the target STA30.</p> <p>0: OFF, 1: ON</p>
0x7	REJECT_CHP_CHN	<p>Changes the REJECT flags of the specified STA30. ON-OFF states are updated according to REJECT flags' values.</p> <p>Chip-ID specifies the target STA30. Core-ID is ignored. WData[0] represents the update value for REJECT flags of Channel 0. WData[1] represents the update value for REJECT flags of Channel 1. WData[2] represents the update value for REJECT flags of Channel 2. WData[3] represents the update value for REJECT flags of Channel 3. WData[4] represents the update value for REJECT flags of Channel 4. WData[5] represents the update value for REJECT flags of Channel 5. WData[6] represents the update value for REJECT flags of Channel 6. WData[7] represents the update value for REJECT flags of Channel 7.</p> <p>0: REJECT, 1: No Change.</p>
0x8	WR_CLCON	<p>Writes to Current Limiting Control Register.</p> <p>Chip-ID specifies the target STA30. Core-ID is ignored. WData is the written value to CLCON register.</p>
0x9	WR_TSDCON	<p>Writes to Thermal Shutdown Control Register.</p> <p>Chip-ID specifies the target STA30. Core-ID is ignored. WData is the written value to TSDCON register.</p>
0xA	DIRECT_COR_SW	<p>Changes ON-OFF states of the specified Core in the specified STA30. Switches whose REJECT flags are '1' remain in OFF state.</p> <p>Chip-ID specifies the target STA30. Core-ID specifies the target Core. WData represents the update value for ON-OFF states of the target Core in the target STA30.</p> <p>0: OFF, 1: ON</p>
0xB	DIRECT_CHN_SW	<p>Changes ON-OFF states of the specified Channel in the specified STA30. Switches whose REJECT flags are '1' remain in OFF state.</p> <p>Chip-ID specifies the target STA30. Core-ID specifies the target Channel. WData represents the update value for ON-OFF states of the target Channel in the target STA30.</p> <p>0: OFF, 1: ON</p>

(Continued)

(Continued)

0xC	REJECT_COR_SW	<p>Changes the REJECT flags of the specified Core of the specified STA30. ON-OFF states are updated according to REJECT flags' values.</p> <p>Chip-ID specifies the target STA30. Core-ID specifies the target Core. WData represents the update value for REJECT flags of the specified Core.</p> <p>0: REJECT, 1: No Change.</p>
0xD	REJECT_CHN_SW	<p>Changes the REJECT flags of the specified Channel of the specified STA30. ON-OFF states are updated according to REJECT flags' values.</p> <p>Chip-ID specifies the target STA30. Core-ID specifies the target Channel. WData represents the update value for REJECT flags of the specified Channel.</p> <p>0: REJECT, 1: No Change.</p>
0xE ~ 0xF	RSVD	Reserved

■ **WR_GCON (0x1)**

WR_GCON command is used to update General Control Register. Table 4 shows the contents of General Control Register.

Table 4. General Control Register.

Bit Name	Bits	Descriptions	Reset	Remarks
RSVD	[7:2]	Reserved	-	-
CL_EN	1	Current Limiting Enable. 0: Disable, 1: Enable.	0	Initialized from OTP
TS_EN	0	Thermal Shutdown Enable. 0: Disable, 1: Enable.	0	Initialized from OTP

Though the default values for CL_EN / TS_EN registers are loaded from internal OTP memory on bootstrap, their values can be changed by WR_GCON command.

Note that writing to General Control Register is prohibited by default. To write to General Control Register, EN1_WCON / EN2_WCON commands should be preceded. For more information about EN1_WCON / EN2_WCON commands, refer to *EN1_WCON / EN2_WCON / DIS_WCON* of *Commands Descriptions*.

■ DIRECT_CHP_COR (0x2)

DIRECT_CHP_COR command changes all of the ON-OFF states in the target STA30. The input WData value is written to all Cores of the specified STA30. The target STA30 is specified by Chip-ID. Figure 14 shows an example for DIRECT_CHP_COR command.

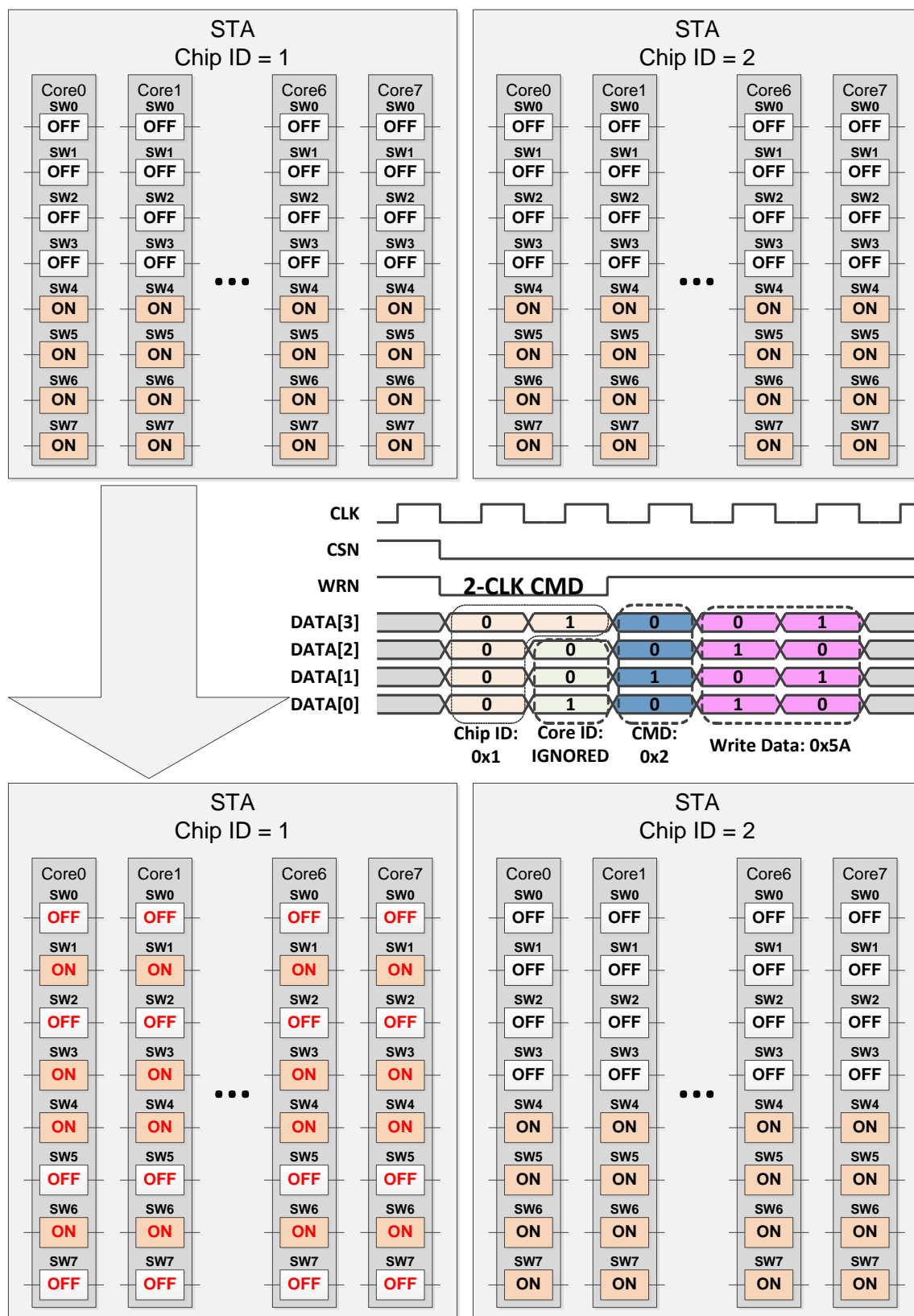


Figure 14. Example for DIRECT_CHP_COR Command.

In Figure 14, the input Chip-ID from the command is 0x1. All Cores of the STA30 whose Chip-ID is 0x1, is updated with the value of WData[7:0] (= 0x5A). Since all Cores are updated, the Core-ID included in the command is ignored. Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.

■ DIRECT_BNK_COR (0x3)

DIRECT_BNK_COR command changes all of the ON-OFF states in STA30s in the selected Bank. The input WData value is written to all Cores of the STA30s. Figure 15 shows an example for DIRECT_BNK_COR command.

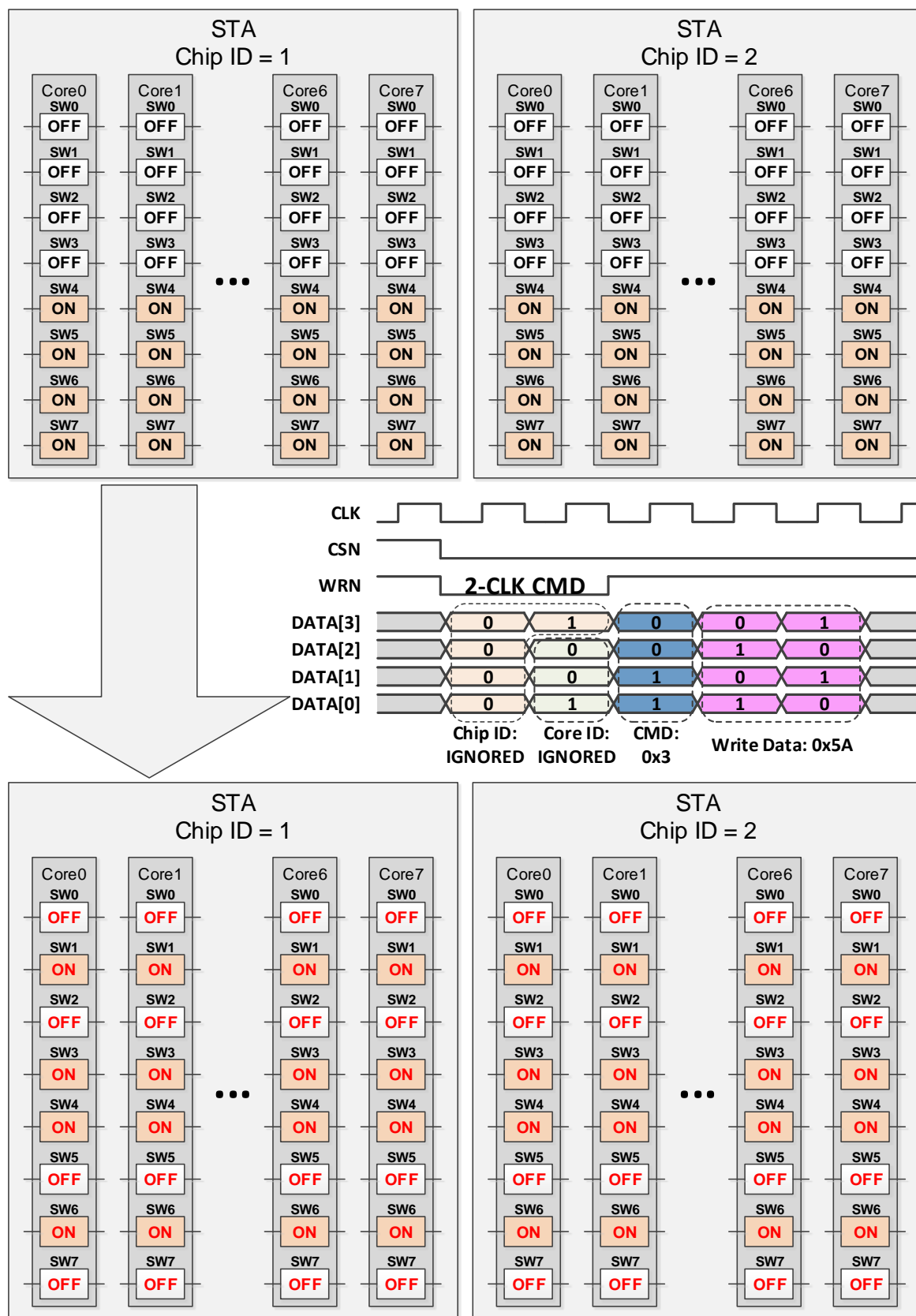


Figure 15. Example for DIRECT_BNK_COR Command.

In Figure 15, WData[7:0] is written to all Cores of all STA30s in the Bank. Since all Cores of all STA30s are the target of DIRECT_BNK_COR command, Chip-ID and Core-ID are ignored. Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.

REJECT_CHP_COR (0x4)

REJECT_CHP_COR command controls REJECT flags of the specified STA30 in Core unit. According to each bit's value of WData[7:0], it sets REJECT flags of each Core's eight switches. Figure 16 shows an example for REJECT_CHP_COR command.

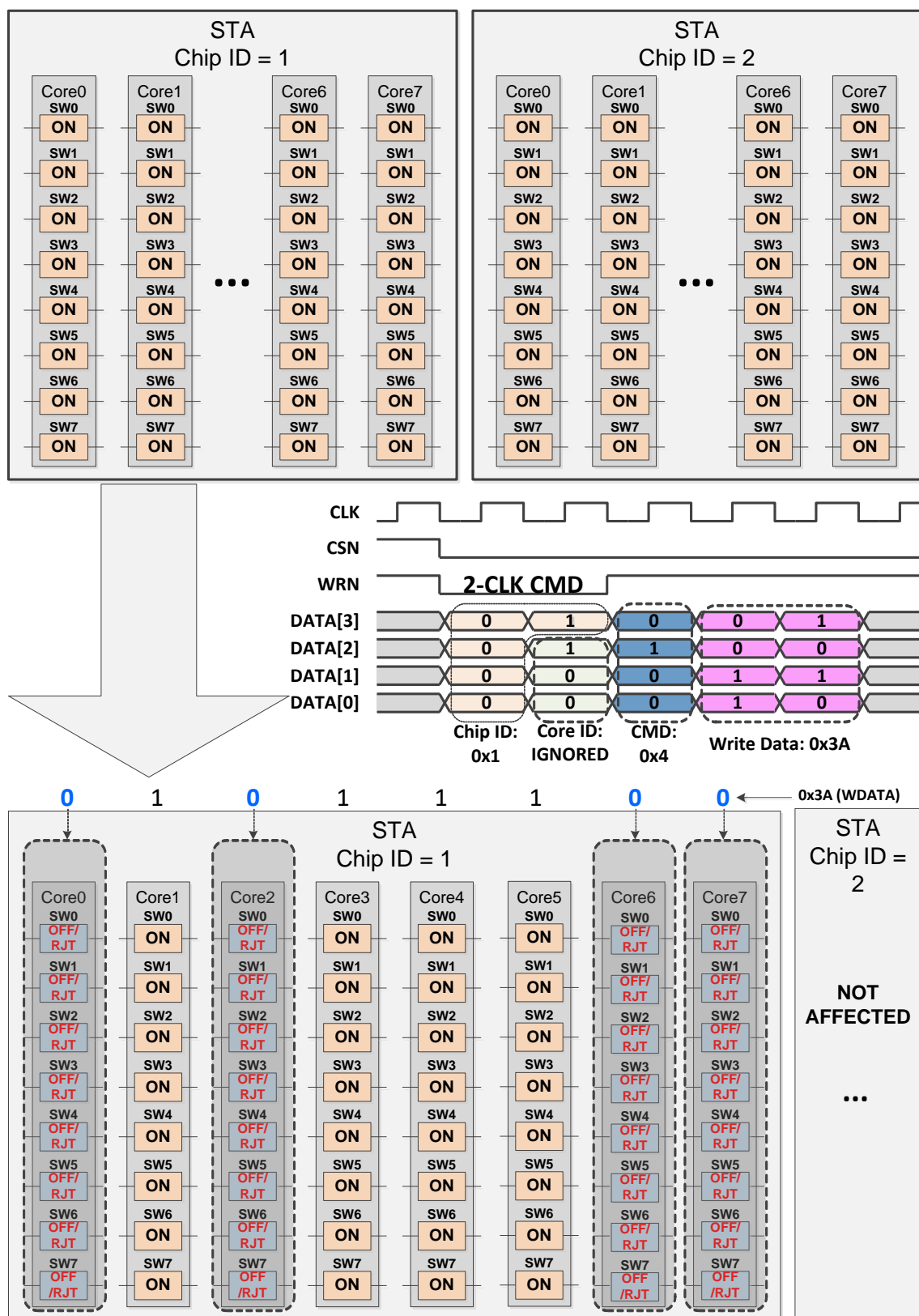


Figure 16. Example for REJECT_CHP_COR Command.

In Figure 16, target STA30 is selected by the Chip-ID (= the one with Chip-ID is 0x1). Each bit of WData decides REJECT flags of each Core. From bit0 to bit7 of WData[7:0] corresponds to Core0 to Core7. Since bit0, bit2, bit6, and bit7 are '0's, REJECT flags of Core0, Core2, Core6, Core7 are set to '1'.

Note that WData bit's value '1' does not mean 'Clear REJECT flag', but 'No Change'. Once REJECT flags are set, they can be cleared only by 1-clock commands.

■ DIRECT_CHP_CHN (0x5)

DIRECT_CHP_CHN command changes all of the ON-OFF states in the target STA30. The input WData value is written to all Channels of the specified STA30. The target STA30 is specified by Chip-ID. Figure 17 shows an example for DIRECT_CHP_CHN command.

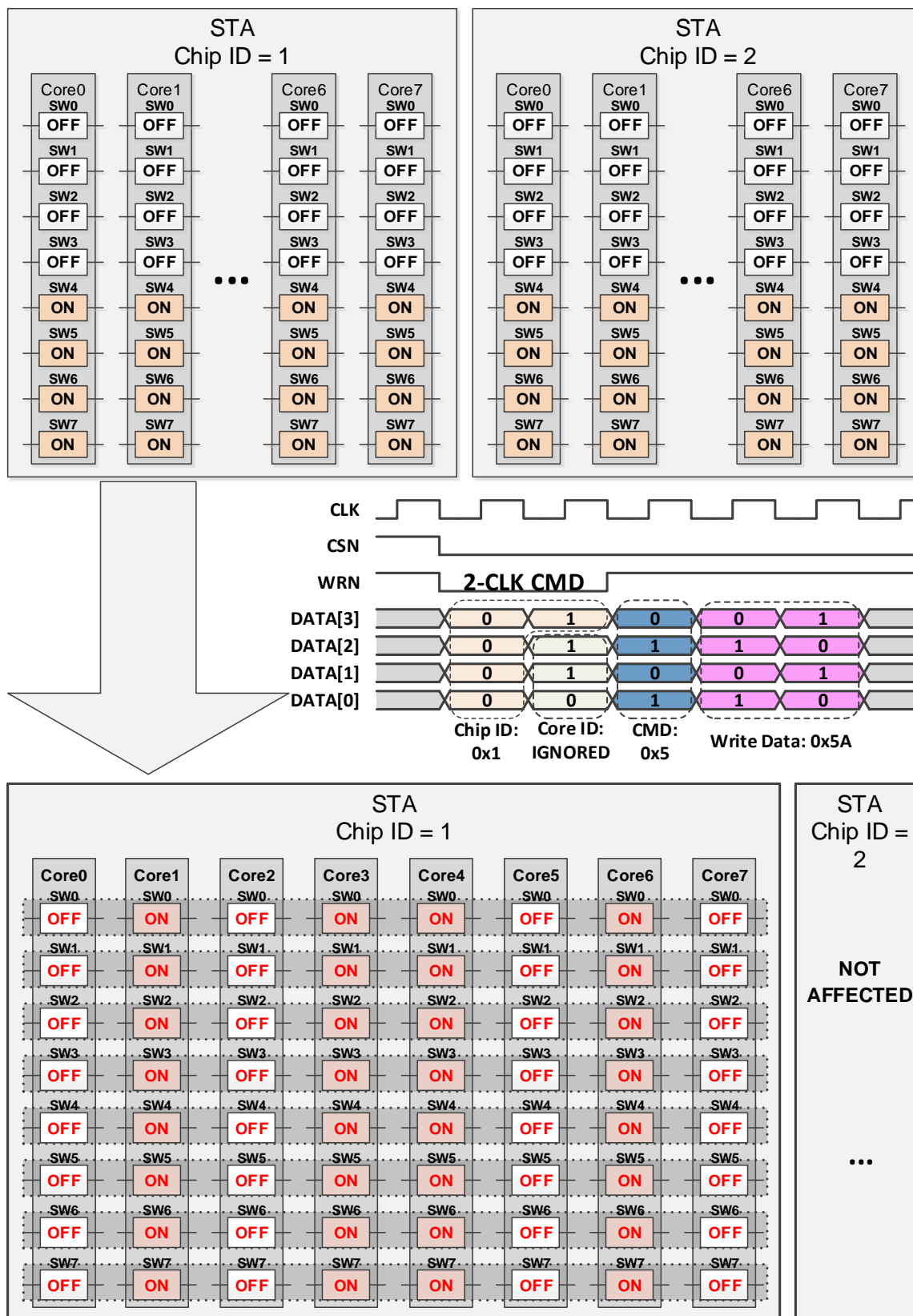


Figure 17. Example for DIRECT_CHP_CHN Command.

In Figure 17, the input Chip-ID from the command is 0x1. All Channels of the STA30 whose Chip-ID is 0x1, is updated with the value of WData[7:0] (= 0x5A). Since all Channels are updated, the Core-ID included in the command is ignored. Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.

■ DIRECT_BNK_CHN (0x6)

DIRECT_BNK_CHN command changes all of the ON-OFF states in STA30s in the selected Bank. The input WData value is written to all Channels of the STA30s. Figure 18 shows an example for DIRECT_BNK_CHN command.

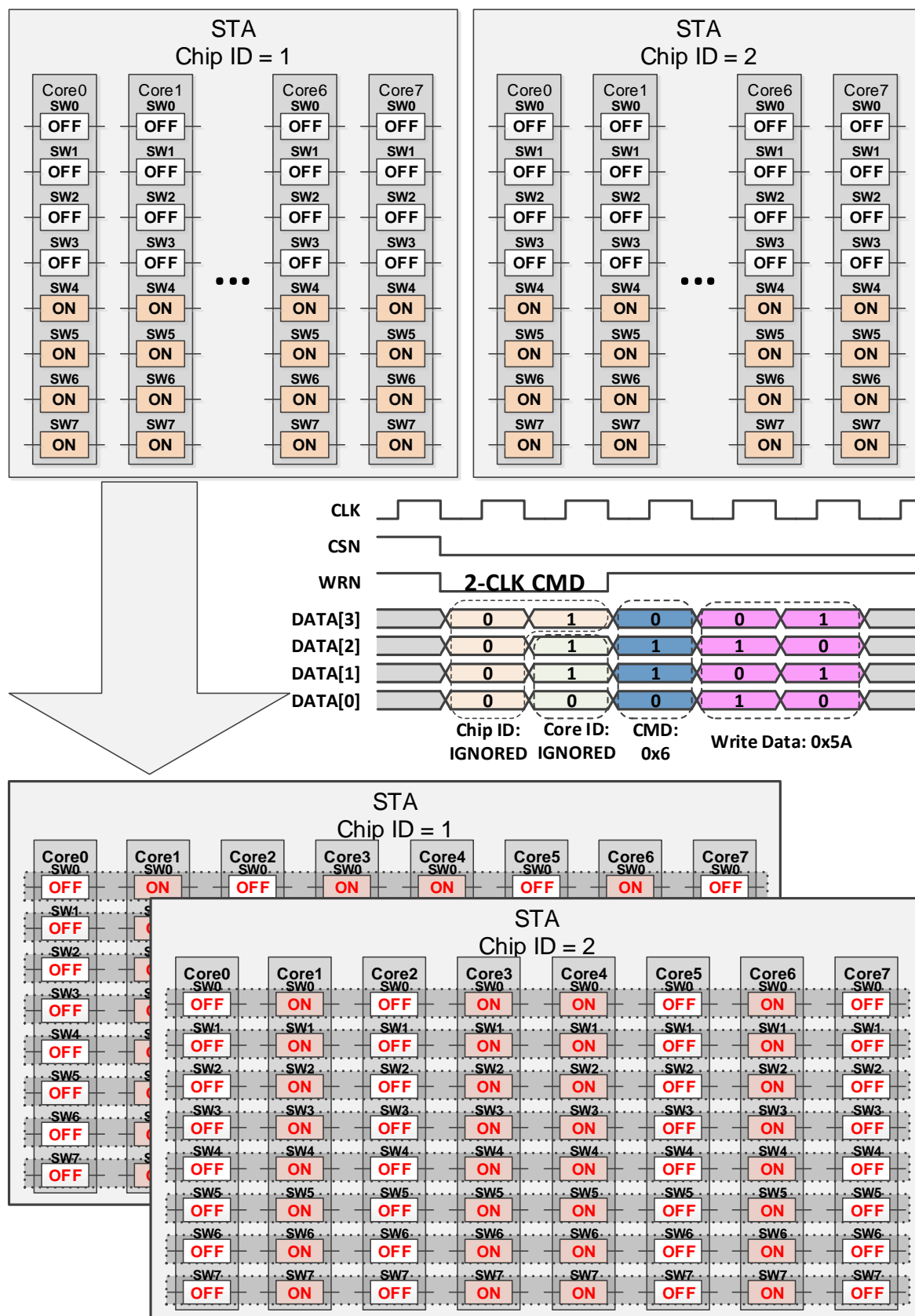


Figure 18. Example for DIRECT_BNK_CHN Command.

In Figure 18, WData[7:0] is written to all Channels of all STA30s in the Bank. Since all Channels of all STA30s are the target of DIRECT_BNK_CHN command, Chip-ID and Core-ID are ignored. Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.

REJECT_CHP_CHN (0x7)

REJECT_CHP_CHN command controls REJECT flags of the specified STA30 in Channel unit. According to each bit's value of WData[7:0], it sets REJECT flags of each Channel's eight switches. Figure 19 shows an example for REJECT_CHP_CHN command.

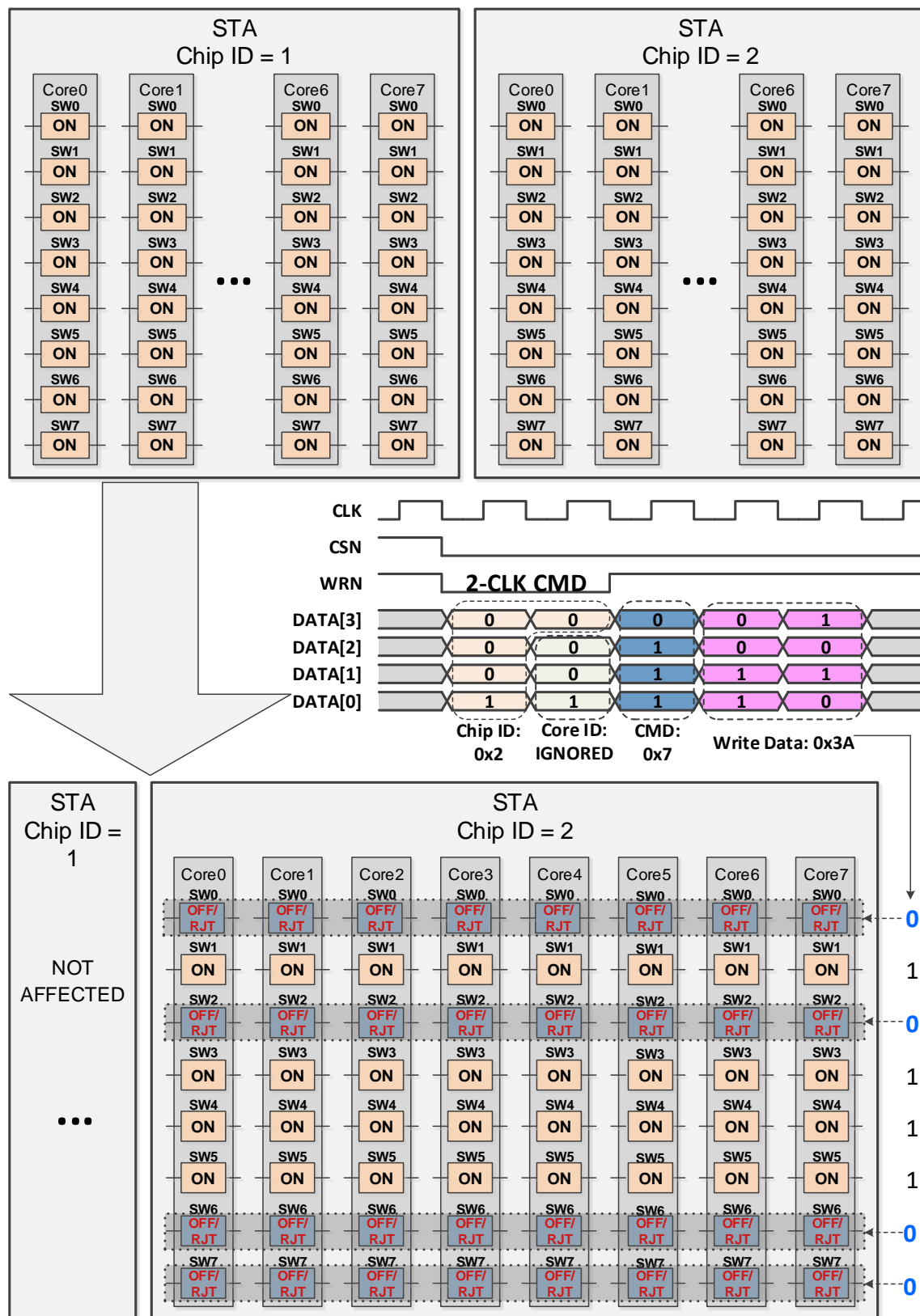


Figure 19. Example for REJECT_CHP_CHN Command.

In Figure 19, target STA30 is selected by the Chip-ID (= the one with Chip-ID is 0x1). Each bit of WData decides REJECT flags of each Channel. From bit0 to bit7 of WData[7:0] corresponds to Channel0 to Channel7. Since bit0, bit2, bit6, and bit7 are '0's, REJECT flags of Channel0, Channel2, Channel6, Channel7 are set to '1'.

Note that WData bit's value '1' does not mean 'Clear REJECT flag', but 'No Change'. Once REJECT flags are set, they can be cleared only by 1-clock commands.

■ WR_CLCON (0x8)

WR_CLCON command is used to update Current Limiting Control Register. Table 5 shows the contents of Current Limiting Control Register.

Table 5. Current Limiting Control Register.

Bit Name	Bits	Descriptions	Reset	Remarks
TV_WEN	7	TRM_VAL write enable. TRM_VAL is updated only if the written value of TV_WEN is '1'.	-	-
TRM_VAL	[6:4]	Current limit trimming (8step). Specifies the trimming value for Current Limiting target limit current. Used for the trimming of target limit current. Note) UPDATED ONLY IF TV_WEN == '1'.	000	Initialized from OTP
CS_WEN	3	CS write enable. CS is updated only if the written value of CS_WEN is '1'.	-	-
CS	[2:0]	Limit current select. Specifies the target limit current for Current Limiting. 000: 50 mA 001: 100 mA 010: 150 mA 011: 200 mA 100: 250 mA 101: 300 mA 110: 350 mA 111: 400 mA Note) UPDATED ONLY IF CS_WEN == '1'.	000	Initialized from OTP

TRM_VAL register is the trimming value for target limit current. The target limiting current is specified by CS register. However, actual temperature which triggers Current Limiting can be different from the target limiting current. Current Limiting circuit is trimmed with TRM_VAL register to minimize this difference.

CS register specifies the actual target limit current for Current Limiting. Current limiting occurs if current flows more than specified in CS register.

Though the default values for TRM_VAL / CS registers are loaded from internal OTP memory on bootstrap, their values can be changed by WR_CLCON command. To make it possible to update TRM_VAL / CS registers respectively, TV_WEN / CS_WEN bits are supported. To update TRM_VAL register, TV_WEN should be HIGH. To update CS register, CS_WEN should be HIGH. The write-enable feature helps update either TRM_VAL or CS register keeping the other register's value not changed.

Note that writing to Current Limiting Control Register is prohibited by default. To write to Current Limiting Control Register, EN1_WCON / EN2_WCON commands should be preceded. For more information about EN1_WCON / EN2_WCON commands, refer to EN1_WCON / EN2_WCON / DIS_WCON of *Commands Descriptions*.

■ WR_TSDCON (0x9)

WR_TSDCON command is used to update Thermal Shutdown Control Register. Table 6 shows the contents of Thermal Shutdown Control Register.

Table 6. Thermal Shutdown Control Register.

Bit Name	Bits	Descriptions	Reset	Remarks
TT_WEN	7	TSD_TRIM write enable. TSD_TRIM is updated only if the written value of TT_WEN is '1'.	-	-
TSD_TRIM	[6:4]	Thermal shutdown temp. trim (8step). Specifies the trimming value for Thermal Shutdown target temperature. Used for the trimming of target temperature of Thermal Shutdown. Note) UPDATED ONLY IF TT_WEN == '1'.	000	Initialized from OTP
RSVD	[3:2]	Reserved	-	-
TS_WEN	1	TSS write enable. TSS is updated only if the written value of TS_WEN is '1'.	-	-
TSS	0	Thermal shutdown hysteresis select. 0: Selects Hysteresis A (about 20°C) 1: Selects Hysteresis B (about 10°C) NOTE) UPDATED ONLY IF TS_WEN == '1'.	0	Initialized from OTP

TSD_TRIM register is the trimming value for Thermal Shutdown target temperature. The target temperature of LSW9X00 Thermal Shutdown circuit is 150°C. However, actual temperature which triggers Thermal Shutdown can be different from the target temperature (i.e. 150°C). Thermal Shutdown circuit is trimmed with TSD_TRIM register to minimize this difference.

TSS register selects Thermal Shutdown Hysteresis. If a switch is turned off by Thermal Shutdown, the switch can be turned on after the temperature goes below (150 – Thermal Shutdown Hysteresis) °C.

Though the default values for TSD_TRIM / TSS registers are loaded from internal OTP memory on bootstrap, their values can be changed by WR_TSDCON command. To make it possible to update TSD_TRIM / TSS registers respectively, TT_WEN / TS_WEN bits are supported. To update TSD_TRIM register, TT_WEN should be HIGH. To update TSS register, TS_WEN should be HIGH. The write-enable feature helps update either TSD_TRIM or TSS register keeping the other register's value not changed.

Note that writing to Thermal Shutdown Control Register is prohibited by default. To write to Thermal Shutdown Control Register, EN1_WCON / EN2_WCON commands should be preceded. For more information about EN1_WCON / EN2_WCON commands, refer to *EN1_WCON / EN2_WCON / DIS_WCON* of *Commands Descriptions*.

■ DIRECT_COR_SW (0xA)

DIRECT_COR_SW command changes the ON-OFF states of a Core in the target STA30. The input WData value is written to the target Core of the specified STA30. The target STA30 is specified by Chip-ID, and the target Core by Core-ID. Figure 20 shows an example for DIRECT_COR_SW command.

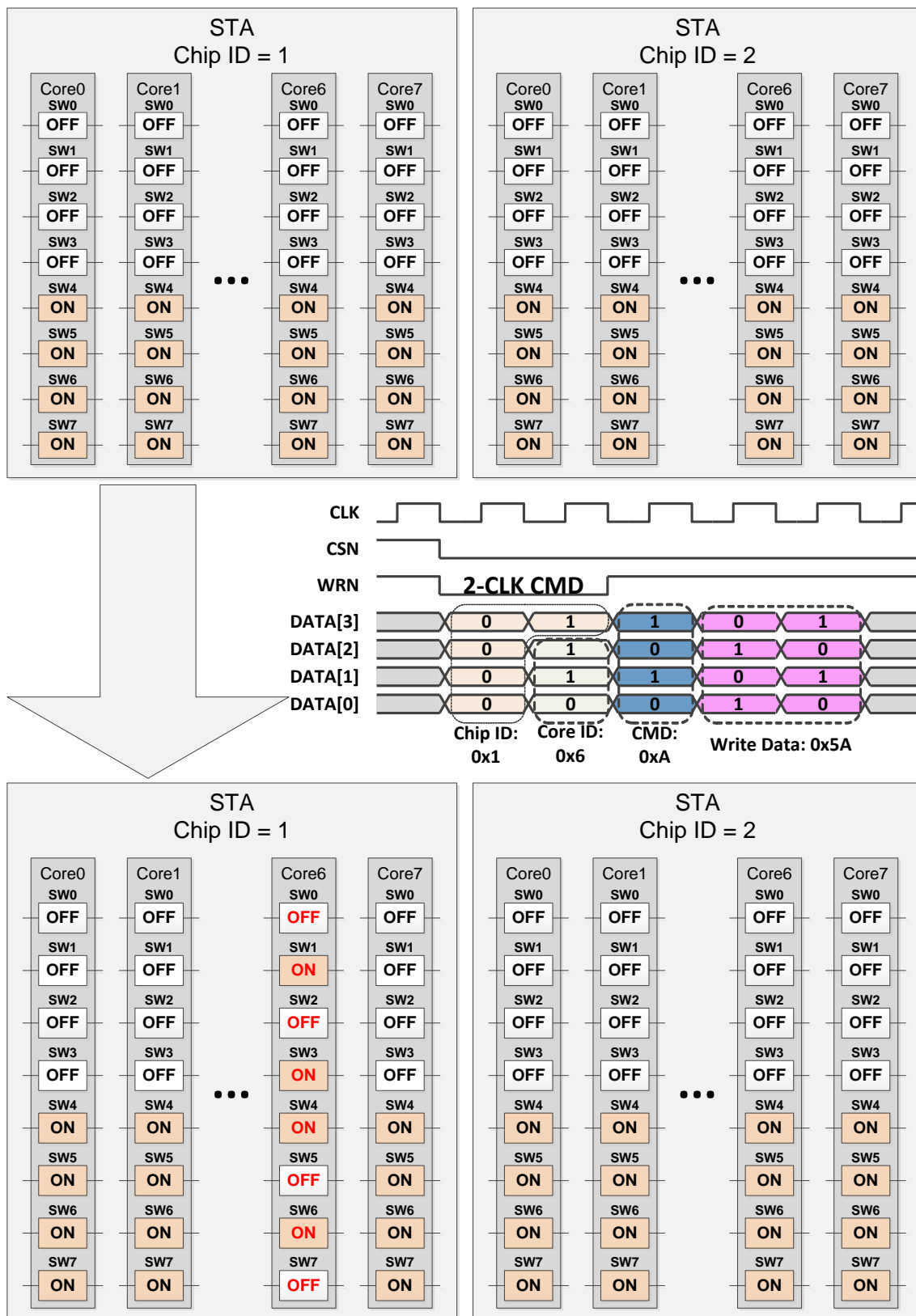


Figure 20. Example for DIRECT_COR_SW Command.

In Figure 20, the input Chip-ID from the command is 0x1, and Core-ID is 0x6. According to the input Chip-ID and Core-ID, Core6 of the STA30 whose Chip-ID is 0x1, is updated with the value of WData[7:0] (= 0x5A). Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.

■ DIRECT_CHN_SW (0xB)

DIRECT_CHN_SW command changes the ON-OFF states of a Channel in the target STA30. The input WData value is written to the target Channel of the specified STA30. The target STA30 is specified by Chip-ID, and the target Channel by Core-ID. Figure 21 shows an example for DIRECT_CHN_SW command.

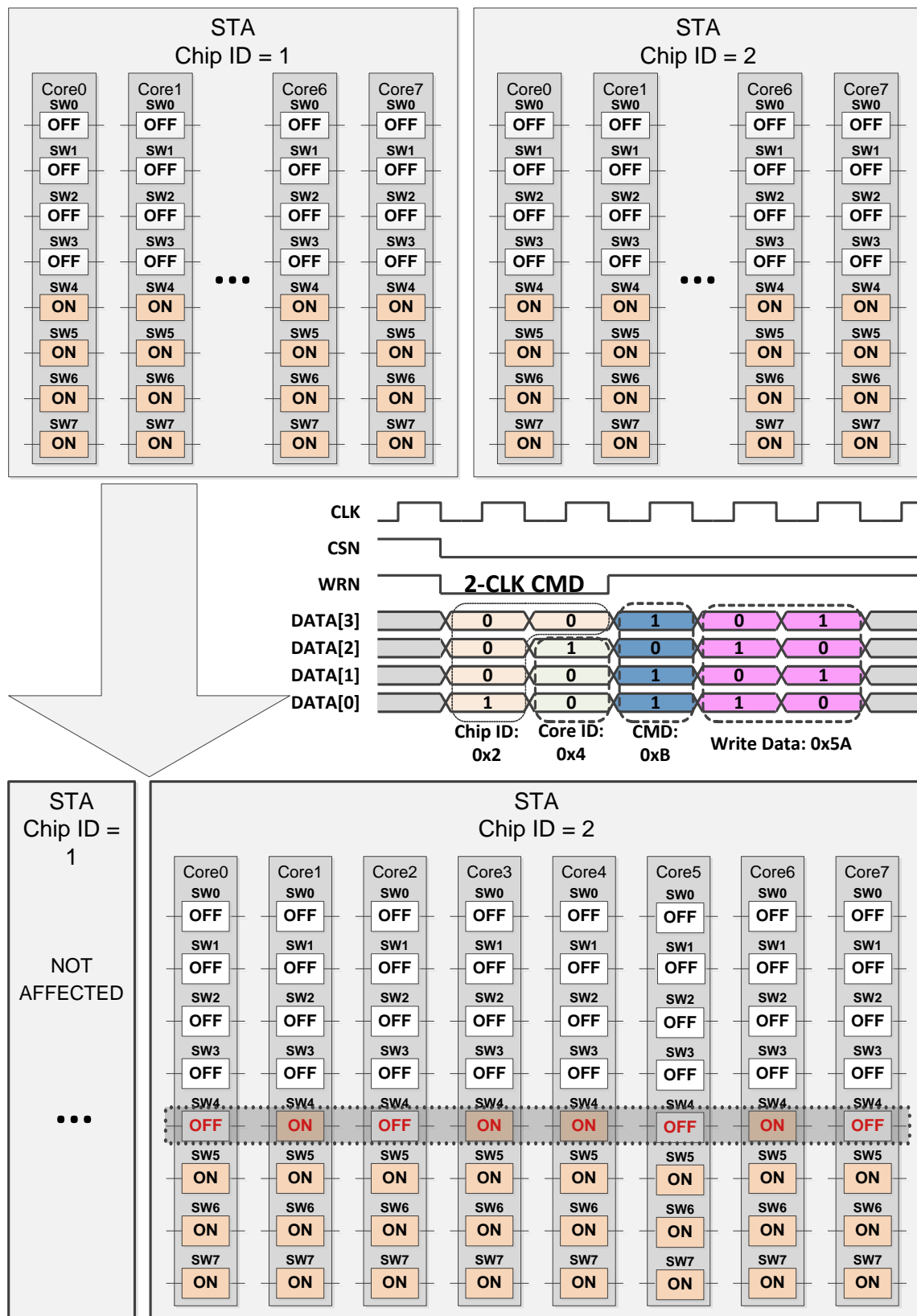


Figure 21. Example for DIRECT_CHN_SW Command.

In Figure 21, the input Chip-ID from the command is 0x2, and Core-ID is 0x4. According to the input Chip-ID and Core-ID, Channel4 of the STA30 whose Chip-ID is 0x2, is updated with the value of WData[7:0] (= 0x5A). Note that the switches whose REJECT flags are set to '1' are not updated, and remain in OFF state.

■ REJECT_COR_SW (0xC)

REJECT_COR_SW command updates REJECT flags of the specified Core. It receives Chip-ID and Core-ID, and uses them to specify the target Channel in the target STA30. According to each bit's value of WData[7:0], it sets REJECT flags of each switch of the selected Core. Figure 22 shows an example for REJECT_COR_SW command.

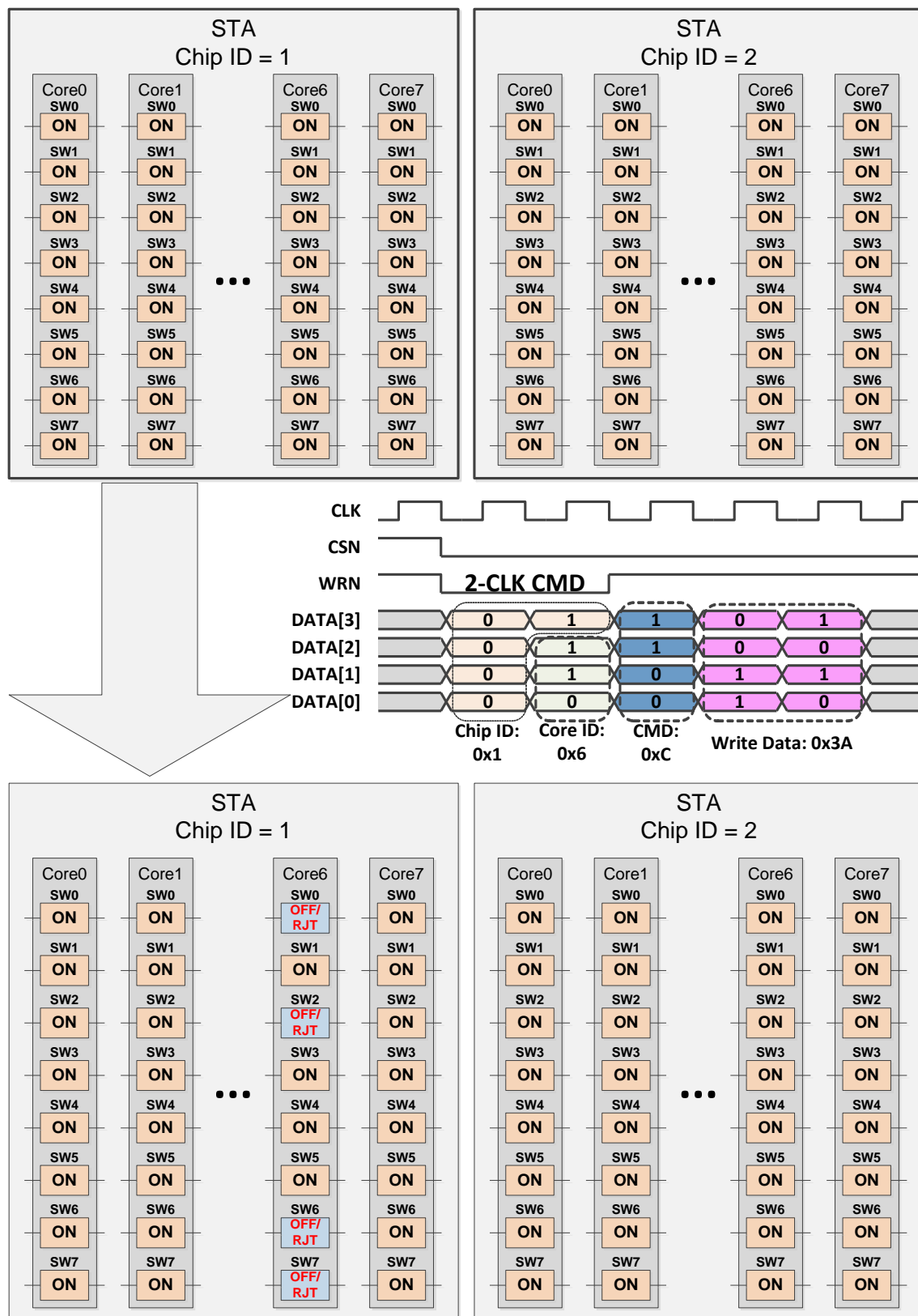


Figure 22. Example for REJECT_COR_SW Command.

In Figure 22, since Chip-ID is 0x1, the one with Chip-ID is 0x1 is selected as the target (i.e. the one with Chip-ID = 0x2 is not affected). Core-ID (= 0x6) specifies the target Core as Core6.

WData[7:0] contains the actual update value of REJECT flags. If a bit of WData is '0', it indicates that the corresponding switch's REJECT flag should be set to '1'. In Figure 22, since WData is 0x3A, bit7, bit6, bit2, bit0 of WData are ZERO. This results in that REJECT flags of switch7, switch6, switch2, switch0 are set to '1'. ON-OFF states of those switches are also set to OFF.

Note that WData bit's value '1' does not mean 'Clear REJECT flag', but 'No Change'. Once REJECT flags are set, they can be cleared only by 1-clock commands.

■ REJECT_CHN_SW (0xD)

REJECT_CHN_SW command updates REJECT flags of the specified Channel. It receives Chip-ID and Core-ID, and uses them to specify the target Channel in the target STA30. The Core-ID is used as the Channel-ID. According to each bit's value of WData[7:0], it sets REJECT flags of each switch of the selected Channel. Figure 23 shows an example for REJECT_CHN_SW command.

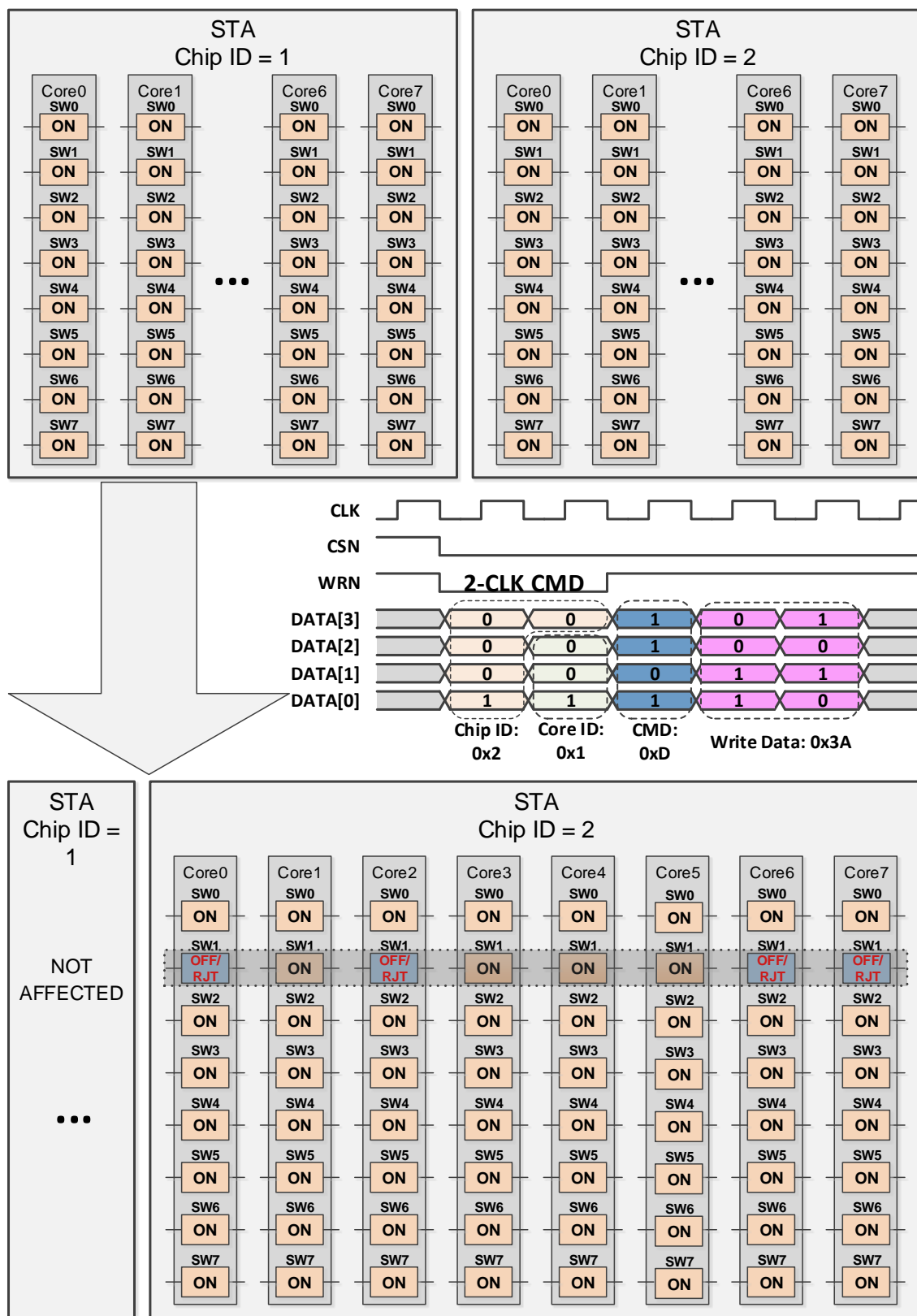


Figure 23. Example for REJECT_CHN_SW Command.

In Figure 23, since Chip-ID is 0x2, the one with Chip-ID is 0x2 is selected as the target (i.e. the one with Chip-ID = 0x1 is not affected). Core-ID (= 0x1) specifies the target Channel as Channel1, which includes all switch1 s from Core0 to Core7.

WData[7:0] contains the actual update value of REJECT flags. If a bit of WData is '0', it indicates that the corresponding switch's REJECT flag should be set to '1'. In Figure 23, since WData is 0x3A, bit7, bit6, bit2, bit0 of WData are ZERO. This results in that REJECT flags of switch1s in Core7, Core6, Core2, Core0 are set to '1'. ON-OFF states of those switches are also set to OFF.

Note that WData bit's value '1' does not mean 'Clear REJECT flag', but 'No Change'. Once REJECT flags are set, they can be cleared only by 1-clock commands.

PACKAGE INFORMATION

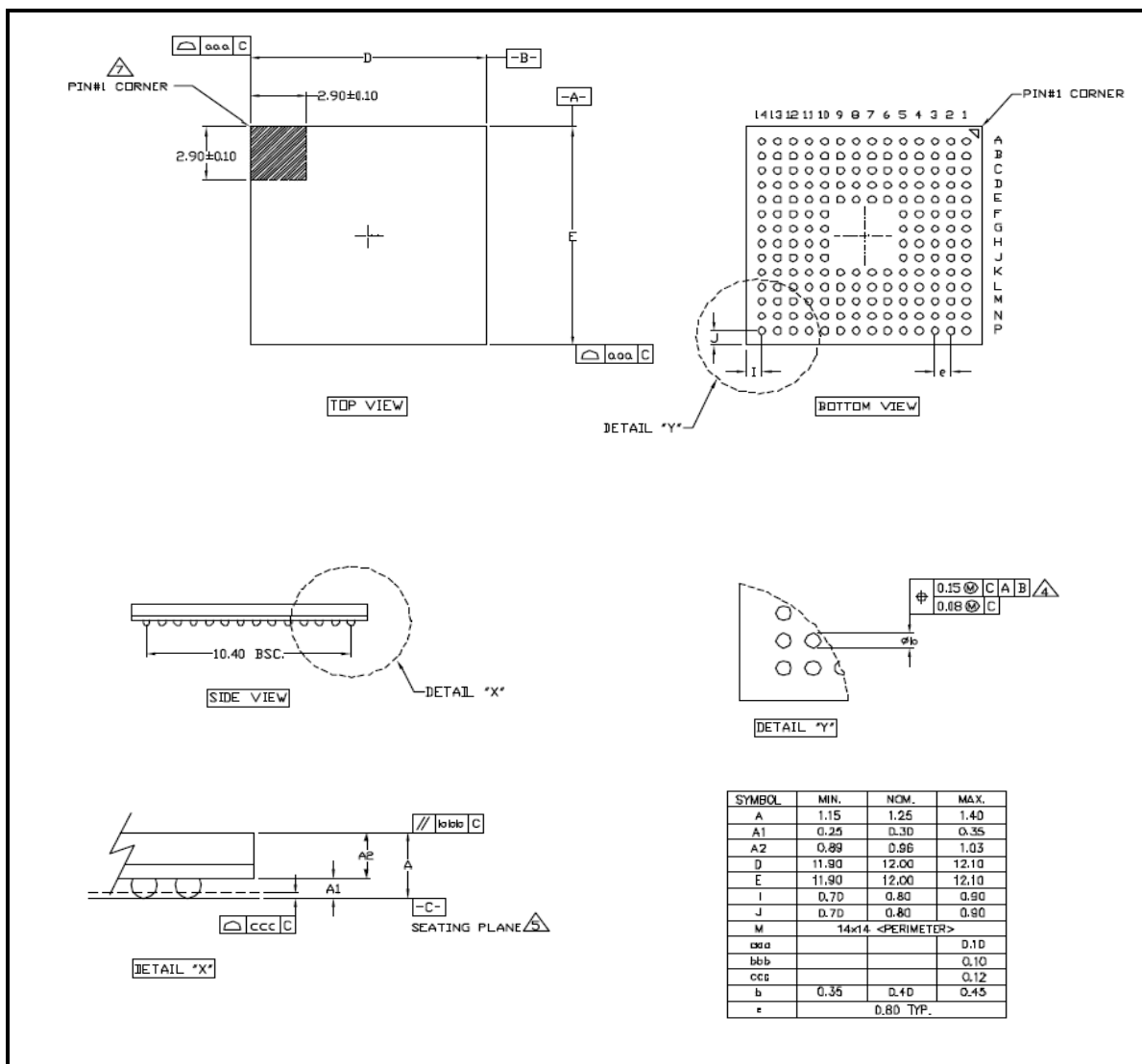


Figure 24. Package Information.

APPLICATION EXAMPLE

■ IC and Package Information

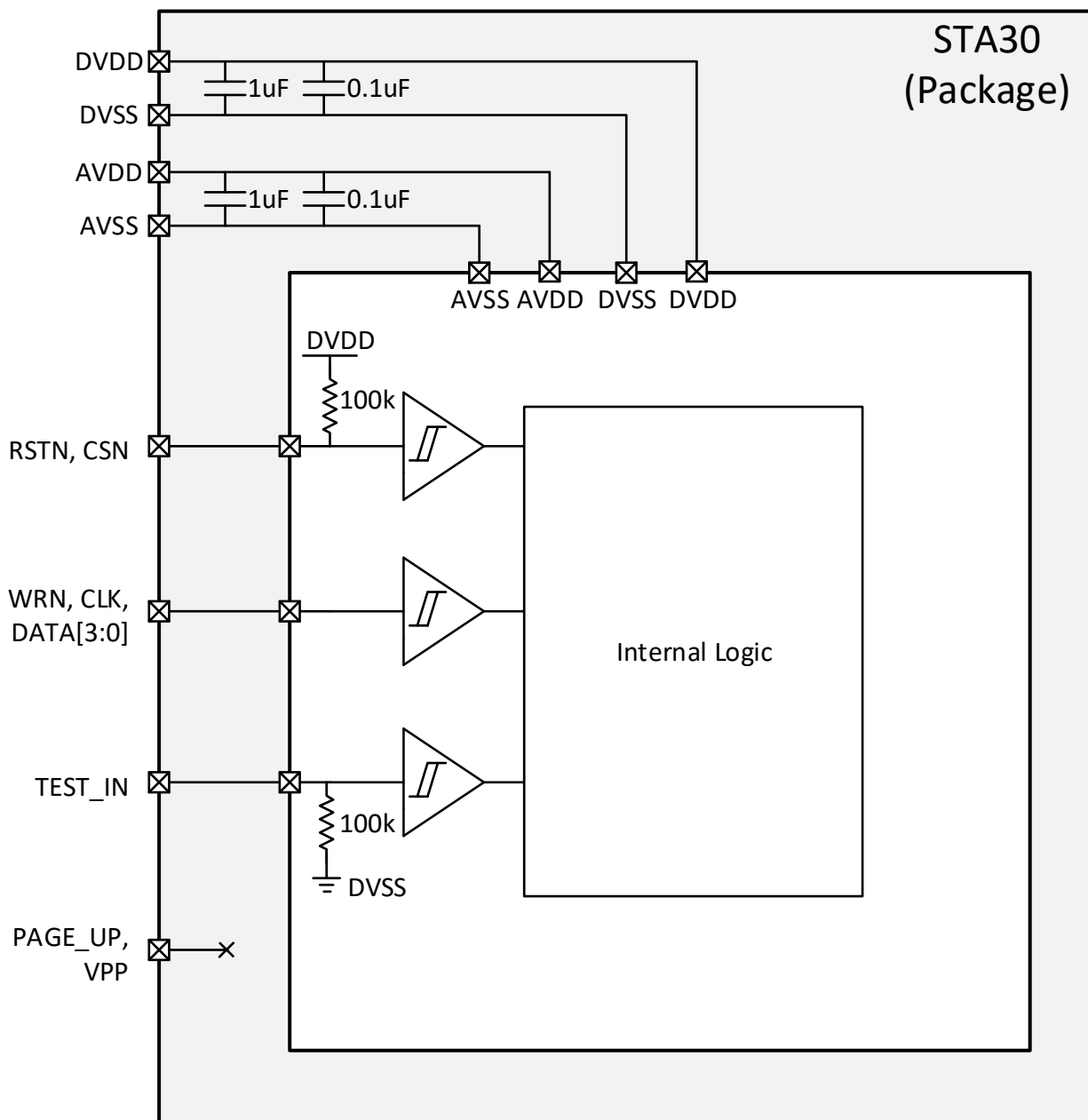
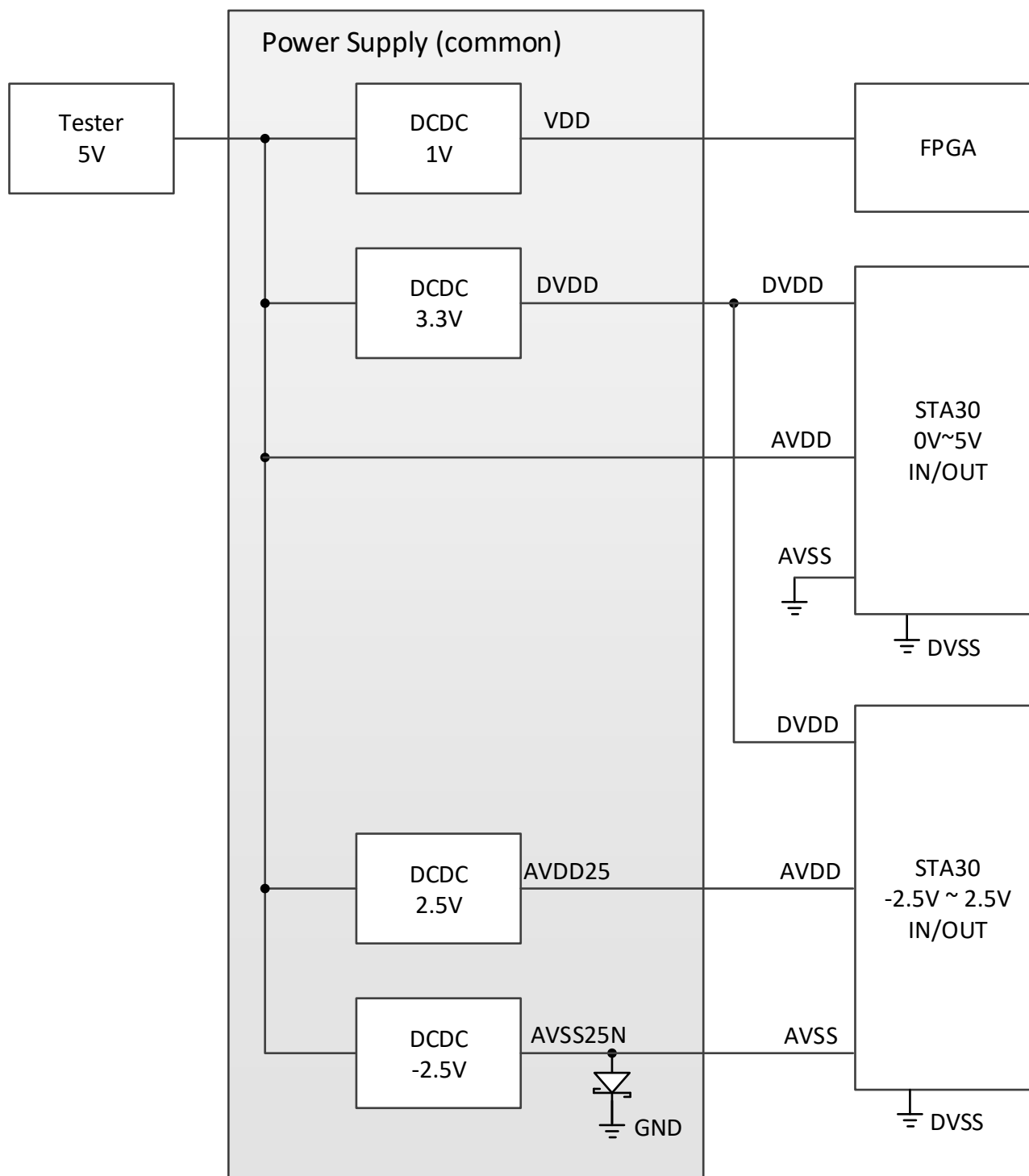


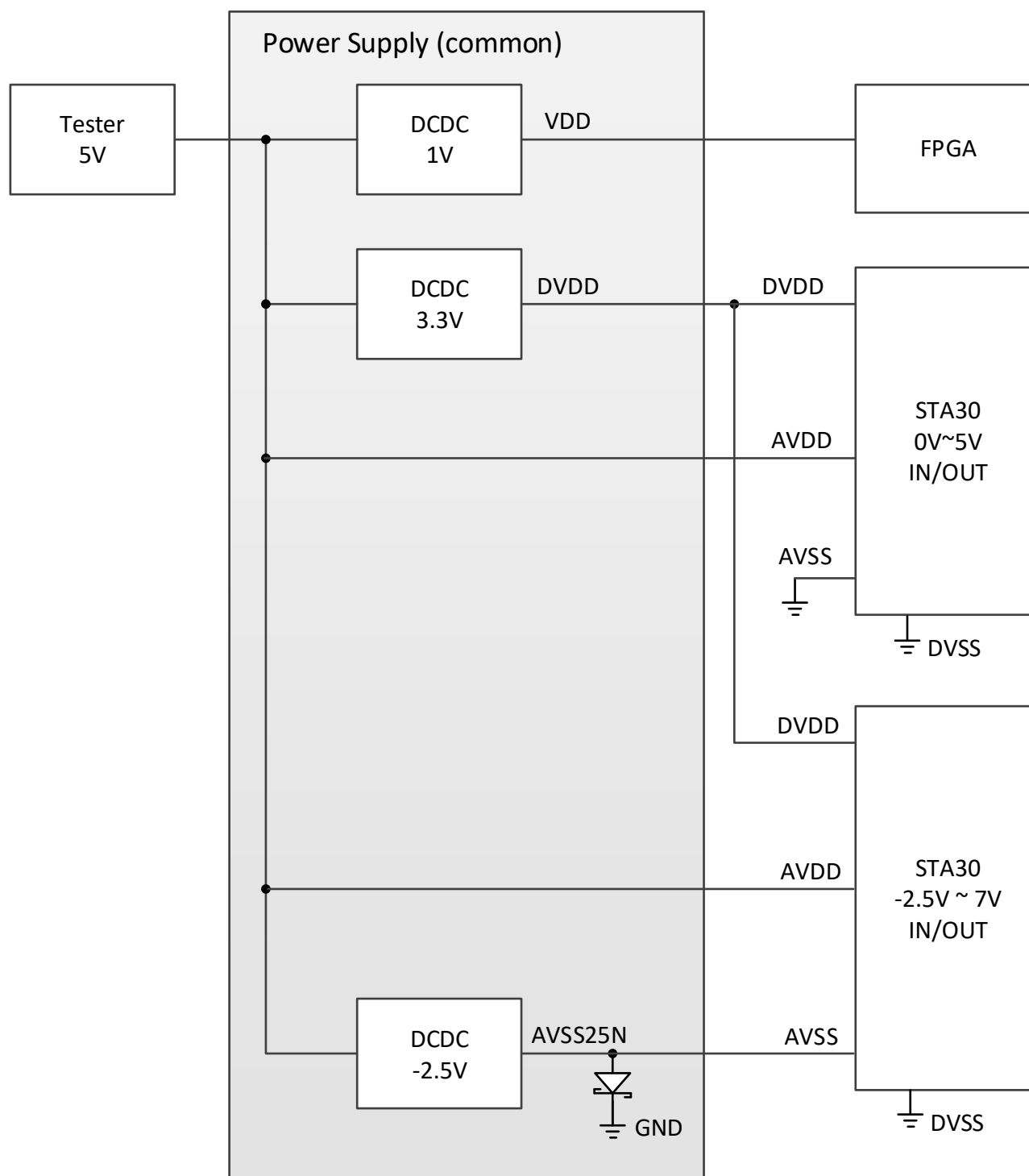
Figure 25. IC and package information

STA30 includes all the passive components required for more stable operation. All the bypass capacitors, between AVDD and AVSS and between DVDD and DVSS, are embedded in the package. All the pull-up and pull-down resistors are included in the I/O block of the IC.

■ Power Supply Configuration



(a) In case of using 2.5V power supply for AVDD

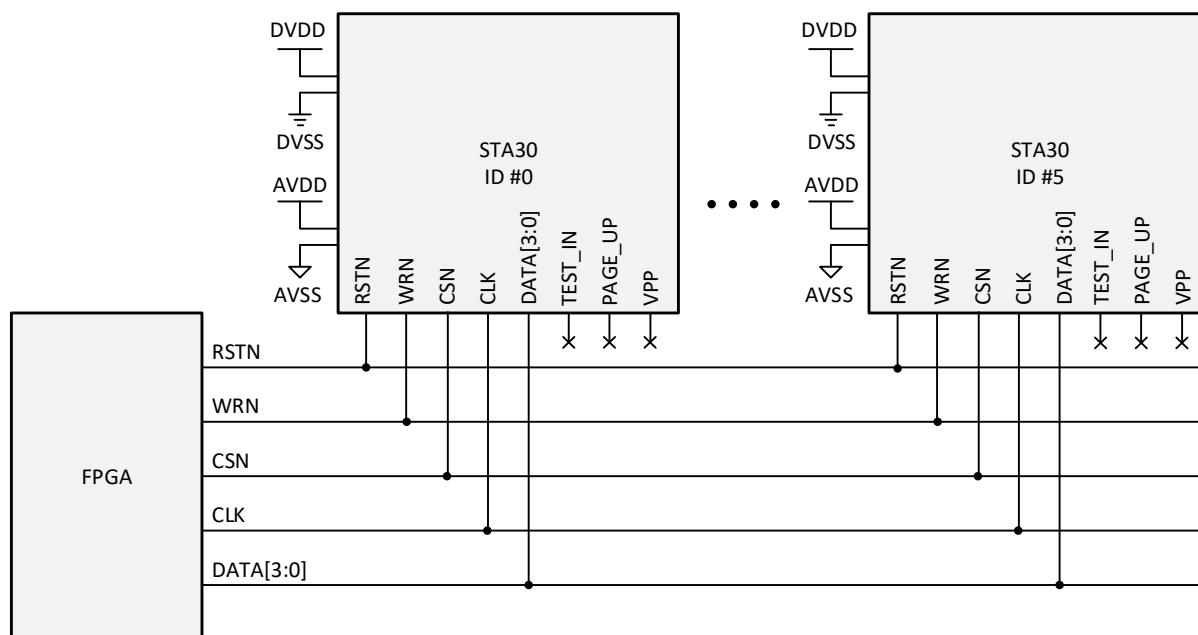


(b) In case of using 5V power supply directly for AVDD

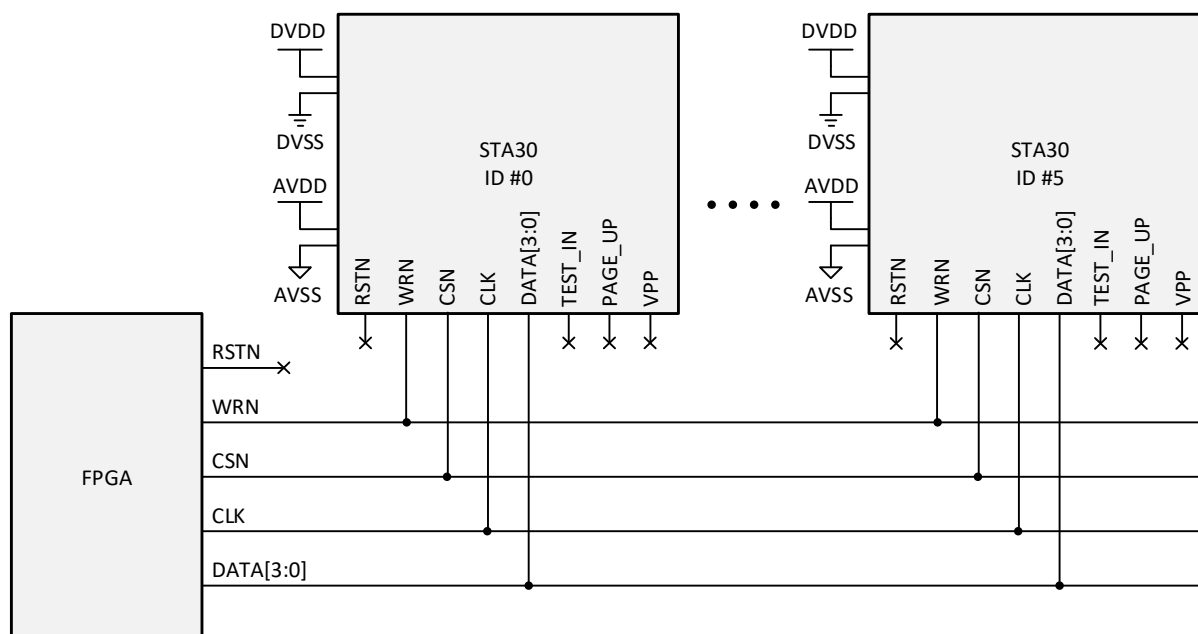
Figure 26. Application Example

STA30 IC supports unipolar configuration. That is, each switch in the STA30 IC can pass a signal having the voltage level between AVDD and ground level (AVSS=GND). Moreover, STA30 IC can also support bipolar configuration that negative voltage less than ground level can be applied to AVSS. With maintaining maximum operating voltage between AVDD and AVSS as 5.5V, AVSS can be maximally lowered to -2.5V. When using the negative voltage to AVSS, to prevent latch-up phenomenon of STA30 IC, a Schottky barrier diode should be attached between AVSS (anode) and DVSS (cathode). Without this protection diode, permanent malfunction of STA30 IC may occur occasionally.

■ Control I/O Pin Connection



(a) In case of using the external RSTN signal from FPGA



(b) In case of not using the external RSTN signal from FPGA but using the internal reset

Figure 27. Recommended I/O connection

STA30 ICs can share their control pins such as CSN, RSTN, WRN, CLK, and DATA[3:0]. Figure 27 (a) shows the I/O pin configuration in case of using the external RSTN signal from FPGA. And Figure 27 (b) shows the I/O pin configuration in case of not using the external RSTN signal from FPGA but using the internal reset signal generated by internal power-on-reset (POR) circuit. Any pull-up/down resistor or bypass capacitor is not required to be attached.

REVISION HISTORY

Revision	Date	Description
0.0	2015-08	Initial draft
0.1	2015-10	Changes Figure 4. Reset and Stand-by Sequence., and related timing parameters (t_{RST} , t_{ORD}).
0.2	2015-11	Corrects waveforms in Figure 17, Figure 18, and Figure 19.
0.3	2016-02	Divides the waveform in Figure 4 into two cases. Added maximum clock frequency. Added description for <i>Power-up Sequence</i> . Changed title to Current Limiting (Default: Disable). Modified description for Current Limiting (Default: Disable). Changed title to Thermal Shutdown (Default: Disable).
0.4	2016-03	Corrects <i>TIMING CHARACTERISTICS</i> title hierarchy. Added f_{CLK} , f_{SW} in <i>TIMING CHARACTERISTICS</i> , and modified related Notes. Added f_{CLK} condition for dynamic current measurement. Added <i>APPLICATION EXAMPLE</i> . Removed t_{SWEN} . Added Figure 5 (a), and (b).
0.5	2019-01	Added maximum clock frequency (1.25MHz to 10KHz) Changed Company Address

DOCUMENT INFORMATION

Document name: STA30 Datasheet
 Product code: STA30
 Product description: Analog Switch IC
 Document revision: 0.5
 Revision date: 2019-01



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