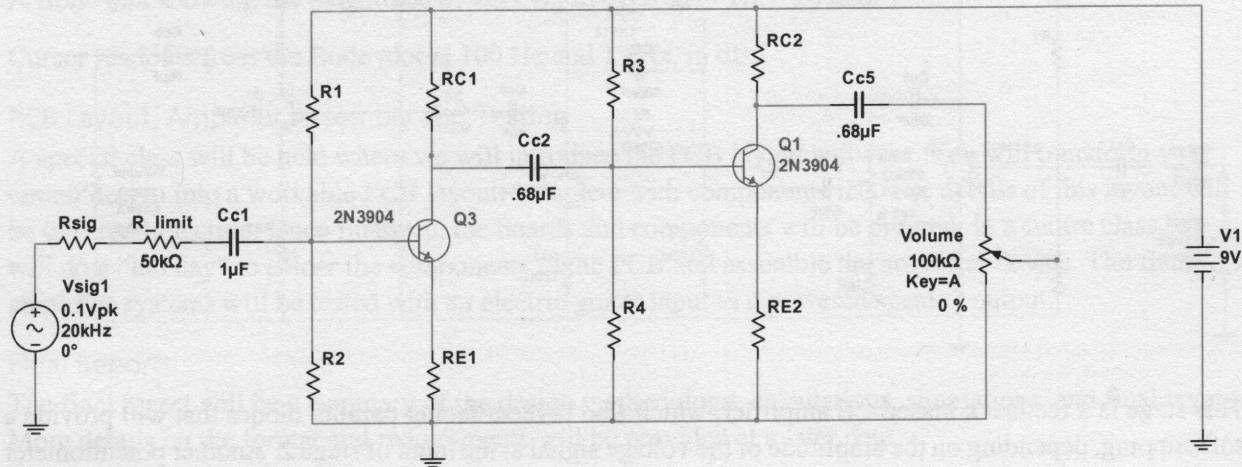


Overview:

For this design project, we will investigate a cascaded common-emitter amplifier system that uses emitter resistances to stabilize the DC bias point and gain parameters while sacrificing some maximum overall gain values. The design target is an audio amplifier that takes the input from a typical electric guitar pickup and provide a stable, amplified output. You will form groups of 3 to complete this design project.

Goal: Design a multistage amplifier that achieves between 20 - 30 V/V overall gain, including source and stage matching, while maintaining signal fidelity (i.e. preventing distortion or clipping) from input to output. Use 2N3904 NPN BJTs along with passive components in the configuration shown below:



Design appropriate values for all resistors and capacitors to achieve the requirements listed below. All resistor and capacitor values must be standard values.

Requirements / Assumptions:

$A_{v,T}$	V_{cc}	v_{sig}	R_{sig}	I_{B1}	I_{B2}	V_{Cl}, V_{C2}	f_L	r_o
20-30 V/V	9 V	0.1 V _{pk}	10 kΩ	2-6 μA	5-15 μA	~0.5* V_{cc}	<100 Hz	infinity

Deliverables:

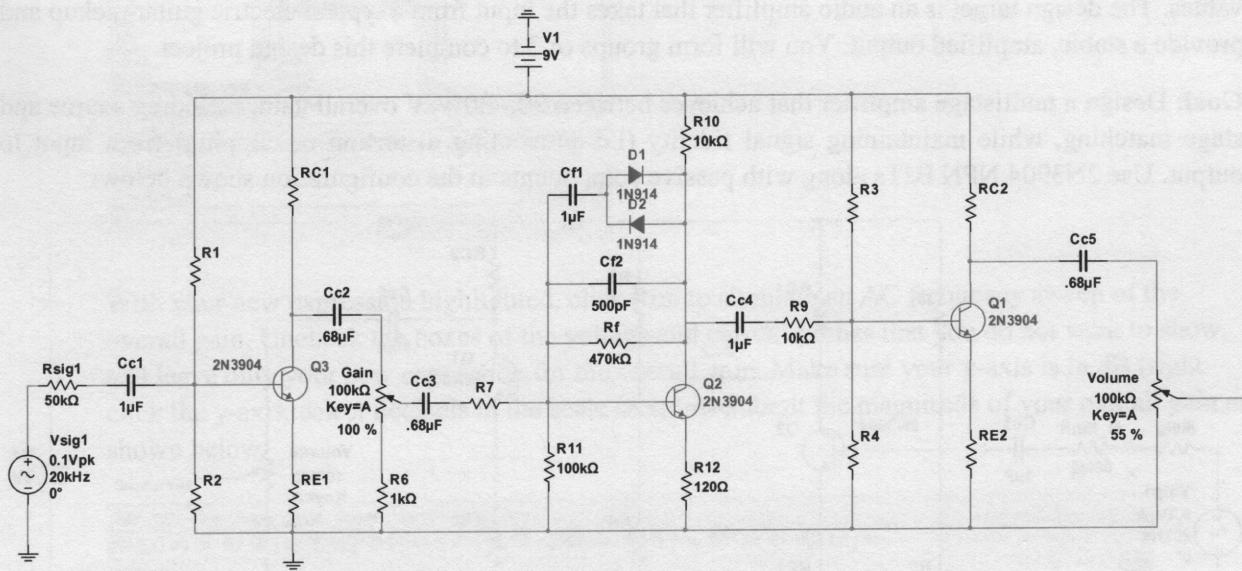
This project will have 3 deliverables:

- 1) Design including hand calculations and MultiSim simulation – Due **Nov 17th**
- 2) Layout file completed for PCB integration – Due **Nov 22th**
- 3) Final Report – Due **Dec 8th**

In addition, due to the quick turn around between design and PCB layout, I will be reviewing your design and MultiSim file **at the end of class on Nov 17th. Your group must have the MultiSim simulation working and displaying the waveforms.**

Bonus design including clipping and gain control

If your 2-stage amplifier is working well and your group desires to spice up the design, the following stage can be inserted into your design:



This stage is a feedback biased CE amplifier, which also reverse-facing parallel diodes that will provide a soft clipping, depending on the amplitude of the voltage signal at the input of stage 2. Another potentiometer is added here to adjust this intermediate voltage stage, which in effect controls how much clipping will be present.

Design Calculations

The design report will contain all your hand calculations for the following parameters:

All DC bias parameters:

3 currents and 3 voltages for each transistor bias

Input and output resistances for both stages:

$R_{in,1}$, $R_{out,1}$, $R_{in,2}$, $R_{out,2}$

Open circuit voltage gain for stage 1:

$A_{vo,1}$ (where stage 2 is disconnected)

Voltage gain for stage 1:

A_{v1} (where stage 2 is connected)

Open circuit voltage gain for stage 2:

A_{vo2} (where load is open circuit)

Total voltage gain from v_s to v_{out} :

$A_{v,T}$ (including source and matching, both stage gains)

Low frequency s-poles:

ω_{p1} , ω_{p2} , ω_{p3} from C_{C1} , C_{C2} and C_{C3} , respectively

Low frequency cut-off:

f_L

Simulations

The simulation of the design within Multisim should display probes for the following:

Base currents (I_{B1}, I_{B2})

Collector currents (I_{C1}, I_{C2})

Collector voltages (V_{C1}, V_{C2})

Four oscilloscope outputs ($v_{sig}, v_{in,1}, v_{in,2}, v_{out}$) with Peak-Peak measurements displayed

A Bode plot showing the magnitude of v_{out} / v_{sig} in dB from 1 Hz – 20 kHz

Cursor readouts from the Bode plot at 100 Hz and 1 kHz, in dB.

PCB Layout, Amplifier Assembly and Testing

A special class will be held where we will introduce the PCB layout software. You will transform your circuit design into a workable PCB layout, complete with components list. The details of this layout will be covered in lecture. Once finalized, the boards and components will be ordered. In a future class, we will do a “lab day” to solder the components to the PCB and assemble the amplifier device. The final amplifier systems will be tested with an electric guitar input to a powered speaker output.

Final Report

The final report will be a summary of the design methodology, calculations, simulations, and final layout. More details on the format and requirements will be provided at a later date.

Procedure:

- 1) Begin with DC analysis, using the requirements for base currents and collector voltages to inform your decisions for resistances.

Do your research! Chapter 4 covers BJT Circuits at DC has equations and examples of BJTs that include the emitter resistance.

Simulate in tandem with your design – Create the MultiSim layout while you are designing so you can verify your calculations and prepare for the simulation deliverable at the same time.

Note: You must select standard resistance values so we can order them – do some research to make sure you pick the correct values close to your optimum design.

- 2) Calculate each stage's input and output resistances from the AC / small signal equivalent model.
- 3) Calculate your various gain parameters next. One great benefit of using an emitter resistance is that it makes these gain parameters less dependent on fluctuations in the transistor β .

Do your research, again! Chapter 5 has all the equations you will need to determine your gain parameters. Make sure to find the section that details the CE amplifier with emitter resistance.

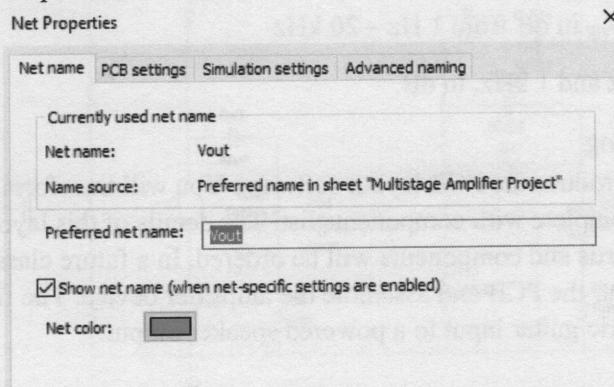
- 4) Design the appropriate coupling capacitor values to achieve a low cutoff frequency of 100 Hz.

The cleanest way to do this is to let two of the capacitors be large enough to not affect the cutoff,

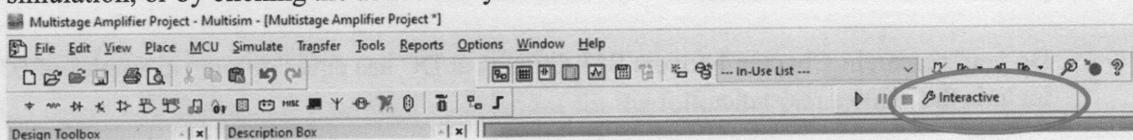
and then design a single coupling capacitor to achieve the s-pole corresponding to 100 Hz. Remember to select only standard capacitor values!

5) Simulating your circuit (a visual guide)

To perform the Bode plot simulation, first define the nodes you wish to examine. Do this by right-clicking the node at the input (v_{sig}) and select Properties, then fill in the box for Preferred net name. Optionally, choose Show net name to display it on the circuit. Do the same of the output node.



Next, change the simulation to AC Sweep by navigating the menu to Simulate → Analysis and simulation, or by clicking the active analysis button shown below:



In the simulation menu, select AC Sweep, and set start and stop frequency to 1 Hz and 20 kHz, respectively. Leave sweep type as decade and set vertical scale to Decibel (dB).

Analyses and Simulation

Active Analysis:

- Interactive Simulation
- DC Operating Point
- AC Sweep**
- Transient
- DC Sweep
- Single Frequency AC
- Parameter Sweep
- Noise
- Monte Carlo
- Fourier
- Temperature Sweep
- Distortion

AC Sweep

Frequency parameters Output Analysis options Summary

Start frequency (FSTART):

1

Hz

Reset to default

Stop frequency (FSTOP):

20

kHz

Sweep type:

Decade

Number of points per decade:

10

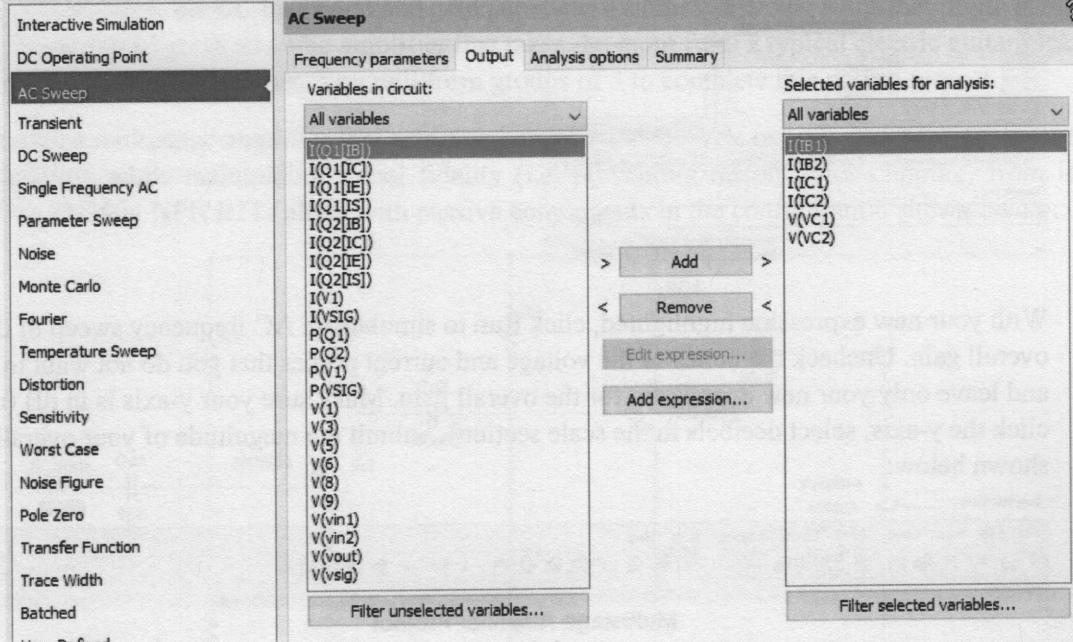
Vertical scale:

Decibel

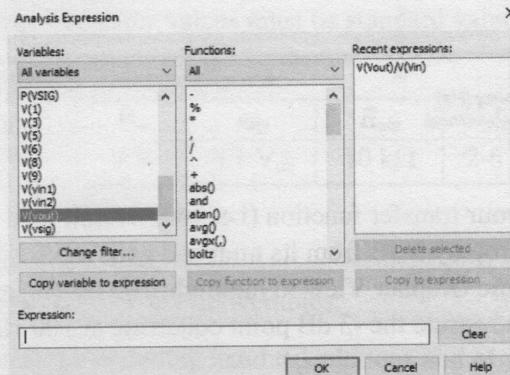
Select the Output tab to bring up a menu of available nodes to include in the simulation.

Analyses and Simulation

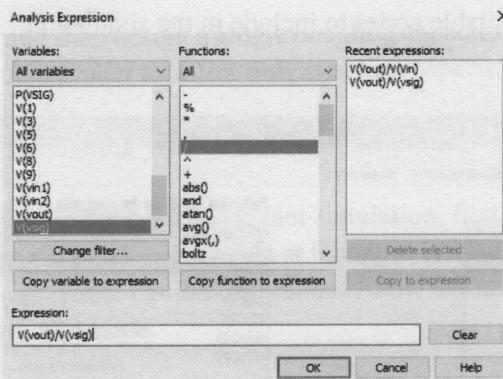
Active Analysis:



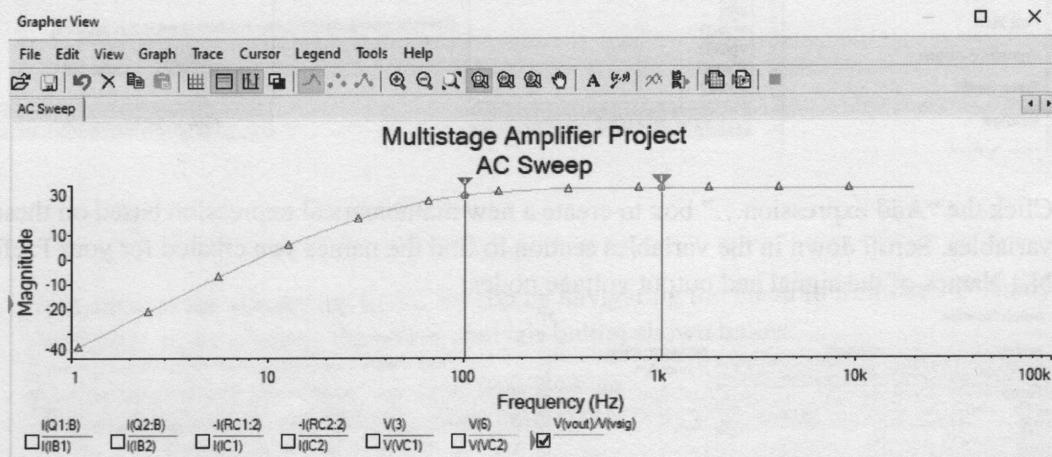
Click the “Add expression...” box to create a new mathematical expression based on these probe variables. Scroll down in the variables section to find the names you created for your Preferred Net Names of the signal and output voltage nodes.



We want to analyze the magnitude of the output voltage / signal voltage. Click on “Copy variable to expression” to bring that variable into the Expression form. Scroll through the functions to find the “/” and copy that function to expression to build the valid expression for our overall gain.



With your new expression highlighted, click Run to simulate an AC frequency sweep of the overall gain. Uncheck the boxes of the voltage and current probes that you do not want to show, and leave only your new expression for the overall gain. Make sure your y-axis is in dB (right click the y-axis, select decibels in the scale section). Submit the magnitude of your overall gain as shown below:



Verify that your low frequency cutoff causes your transfer function (i.e. your overall gain magnitude, including frequency response) to drop by 3 dB from its midband gain value right at your cutoff frequency. Use the cursors within the Grapher View to highlight 100 Hz (f_L) and 1 kHz (midband), and submit the readout to demonstrate the -3 dB point occurring at 100 Hz.

Cursor	
	V(vout) / V(vsig)
x1	1.0363k
y1	28.7435
x2	101.9397
y2	25.8248
dx	-934.3821
dy	-2.9187
dy/dx	3.1237m
1/dx	-1.0702m